SB686BX Series
Single Board Computer Manual

MANUAL NUMBER : 00431-248-1C

6260 Sequence Drive · San Diego, CA 92121-4371 · 800 523-2320 · fax 858 677-0895 · www.icsadvent.com

Mission Critical Applied Computing Solutions

Errata Sheet

November 1999

Manual Numbers:
00431-220-xx, SB586T Series Single Board Computer
00431-244-xx, P2BX/P3BX Series Feature Card
00431-248-xx, SB686BX Series Single Board Computer

The boards listed in the **SB586T Manual** have been renumbered as follows:

SB586T replaces -	SB586T100	**SB586TS** replaces -	SB586TS100	**SB586TS2V** replaces -	SB586TS2V100
	SB586T133		SB586TS133		SB586TS2V133
	SB586T166		SB586TS166		SB586TS2V166
	SB586T166X		SB586TS166X		SB586TS2V200X
	SB586T200		SB586TS200		SB586TS2V166X
	SB586T200X		SB586TS200X		SB586TS2V233X
	SB586T233X		SB586TS233X		SB586TS2V266K
	SB586T266K		SB586TS266K		SB586TS2V300K
	SB586T300K		SB586TS300K		
SB586TT replaces -	SB586TT100	**SB586T2V** replaces -	SB586T2V100	**SB586TU** replaces -	SB586TU100
	SB586TT133		SB586T2V133		SB586TU133
	SB586TT166X		SB586T2V166		SB586TU166
	SB586TT200X		SB586T2V166X		SB586TU166X
	SB586TT233X		SB586T2V200X		SB586TU200X
	SB586TT266K		SB586T2V233X		SB586TU233X
	SB586TT300K		SB586T2V266K		SB586TU266K
			SB586T2V300K		SB586TU300K

Note: Processors are now identified separately from the boards. Processors are supported up to Intel Pentium 233MHz and 300MHz AMD K6-2.

The boards listed in the **P2BX/P3BX Manual** have been renumbered as follows:

P3BXSUT replaces -	P3BXSVT500	**P3BXVT** replaces -	P3BXVT500	**P3BXST** replaces -	P3BXST500
	P3BXSVT450		P3BXVT450		P3BXST450
	P2BXSVT450		P2BXVT450		P2BXST450
	P2BXSVT400		P2BXVT400		P2BXST400
	P2BXSVT350		P2BXVT350		P2BXST350
P3BX replaces -	P3BX500				
	P3BX450				
	P2BX450				
	P2BX400				
	P2BX350				

Note: Processors are now identified separately from the boards. Processors are supported up to 600MHz.

The boards listed in the **SB686BX Manual** have been renumbered as follows:

SB686BX replaces -	SB686BX3500	**SB686BXV** replaces -	SB686BXV3500
	SB686BX3450		SB686BXV3450
	SB686BX450		SB686BXV450
	SB686BX400		SB686BXV400
	SB686BX350		SB686BXV350
Obsoleted numbers -	SB686XC400		
	SB686XC366		
	SB686XVC400		
	SB686XVC366		

Note: Processors are now identified separately from the boards. Processors are supported up to 600MHz.

Errata Sheet

February 2000

Manual Number:
00431-248-xx, SB686BX Series Single Board Computer Manual

- Please refer to the ICS Advent Web site *(www.icsadvent.com)* for available processor speeds. Additional processor speeds may be available.

FOREWORD

This product manual provides information to install, operate and or program the referenced product(s) manufactured or distributed by ICS Advent. The following pages contain information regarding the warranty and repair policies.

Check our Web site (***http://www.icsadvent.com/techsupport***) for technical information, manual, and BIOS updates. Technical assistance is also available at: **800-480-0044** (U.S. and Canada) or **858-677-0877** (international).

Manual errors, omissions, bugs, and/or comments: A Customer Comments section is included at the end of this manual. If you experience any problems with the manual or just want to give us some feedback, please review the information in this section. It will tell you how to easily access our web site and provide immediate feedback online.

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Guarantee

A thirty day money-back guarantee is provided on all **standard** products sold. **Special order products** are covered by our Limited Warranty, *however they may not be returned for refund or credit. EPROMs, RAM, Flash EPROMs or other forms of solid electronic media are not returnable for credit - but for replacement only. Extended Warranty available. Consult factory.*

Refunds

In order to receive a refund on a product purchase price, the product must not have been damaged by the customer or by the common carrier chosen by the customer to return the goods, and the product must be returned complete (meaning all manuals, software, cables, etc.) within 30 days of receipt and in as-new and resalable condition. The **Return Procedure** must be followed to assure prompt refund.

Restocking Charges

Product returned *after* 30 days, and *before* 90 days, of the purchase will be subject to a **minimum** 20% restocking charge and any charges for damaged or missing parts.

Products not returned within 90 days of purchase, or products which are not in as-new and re-saleable condition, are not eligible for credit return and will be returned to the customer.

Limited Warranty

Effective April 1, 1998, all products carry a two-year limited warranty with the exception of the "Performance Series" I/O products, which are warranted to the original purchaser for as long as they own the product, subject to all other conditions below, including those regarding neglect, misuse and acts of God. Within one year of purchase, ICS Advent will repair or replace, at our option, any defective product. At any time after one year, we will repair or replace, at our option, any defective "Performance Series" I/O product sold. This does not include products damaged in shipment, or damaged through customer neglect or misuse. ICS Advent will service the warranty for all standard catalog products for the first year from the date of shipment. After the second year, for products not manufactured by ICS Advent, the remainder of the manufacturer's warranty, if any, will be serviced by the manufacturer directly.

The **Return Procedure** must be followed to assure repair or replacement. ICS Advent will normally return your replacement or repaired item via Second Day Air. *Overnight delivery or delivery via other carriers is available at additional charge.*

The limited warranty is void if the product has been subjected to alteration, neglect, misuse, or abuse; if any repairs have been attempted by anyone other than ICS Advent or its authorized agent; or if the failure is caused by accident, acts of God, or other causes beyond the control of ICS Advent or the manufacturer. Neglect, misuse, and abuse shall include any installation, operation, or maintenance of the product other than in accordance with the owners' manual.

No agent, dealer, distributor, service company, or other party is authorized to change, modify, or extend the terms of this Limited Warranty in any manner whatsoever. ICS Advent reserves the right to make changes or improvements in any product without incurring any obligation to similarly alter products previously purchased.

Shipments not in compliance with this Guarantee and Limited Warranty Return Policy will not be accepted by ICS Advent.

Return Procedure

For any Limited Warranty or Guarantee return, please contact ICS Advent's Customer Service at **800-480-0044** (U.S. and Canada) or **858-677-0877** (international) and obtain a Return Material Authorization (RMA) Number. All product(s) returned to ICS Advent for service or credit **must** be accompanied by a Return Material Authorization (RMA) Number. Freight on all returned items **must** be prepaid by the customer who is responsible for any loss or damage caused by common carrier in transit. Returns for Warranty **must** include a Failure Report for each unit, by serial number(s), as well as a copy of the original invoice showing date of purchase.

> To reduce risk of damage, returns of product must be in an ICS Advent shipping container. If the original container has been lost or damaged, new shipping containers may be obtained from ICS Advent Customer Service at a nominal cost.

Limitation of Liability

In no event shall ICS Advent be liable for any defect in hardware or software or loss or inadequacy of data of any kind, or for any direct, indirect, incidental, or consequential damages in connection with or arising out of the performance or use of any product furnished hereunder. ICS Advent liability shall in no event exceed the purchase price of the product purchased hereunder. The foregoing limitation of liability shall be equally applicable to any service provided by ICS Advent or its authorized agent.

Some *Sales Items* and *Customized Systems* are **not** subject to the guarantee and limited warranty. However in these instances , any deviations will be disclosed prior to sales and noted in the original invoice. ***ICS Advent reserves the right to refuse returns or credits on software or special order items.***

Advisories

Three types of advisories are used throughout the manual to stress important points or warn of potential hazards to the user or the system. They are the ***Note***, the ***Caution***, and the ***Warning***. Following is an example of each type of advisory:

Note: The note is used to present information which may provide special instruction or extra information which may help to simplify the use of the product.



CAUTION!



A Caution is used to alert you of a situation which if ignored may cause injury or damage equipment.



WARNING!



A Warning is used to alert you of a situation which if ignored will cause serious injury.

Cautions and Warnings are accented with triangular symbols. The excalmation symbol is used in all cautions and warnings to help alert you to the important instructions. The lightning flash symbol is used on the left hand side of a caution or a warning if the advisory relates to the presence of voltage which may be of sufficient magnitude to cause electrical shock.

Use caution when servicing any electrical component. We have tried to identify the areas which may pose a Caution or Warning condition in this manual; however, ICS Advent does not claim to have covered all situations which might require the use of a Caution or Warning.

You must refer to the documentation for any component you install into a computer system to insure proper precautions and procedures are followed.

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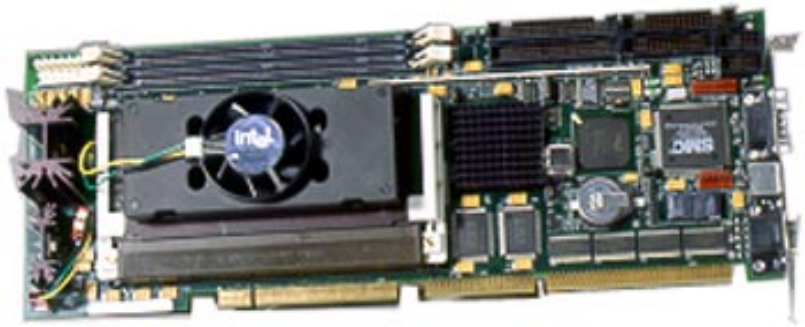
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Chapter 1: Introduction

This manual describes the SB686BX Series single board computers. A complete list of products covered by this manual appears at the end of this chapter. Chapter 1 provides general information. Chapter 2 contains specifications and dimensional drawings. Chapter 3 lists the connector pinouts and illustrates the board layout. Chapter 4 details component installation and switch settings. Chapter 5 describes maintenance and troubleshooting. Appendix A describes the BIOS and Appendix B provides sample code for the watchdog timer.

General

The SB686BX is a full featured, industrialized, single board computer with a high-frequency Intel® Pentium III®, Pentium II®, or Celeron® processor that brings advanced CPU technology and processing power to the latest ISA/PCI (PICMG) applications and to older ISA systems. The 440BX AGP set built in to the single board computer is the most efficient and reliable way to upgrade existing ISA systems to Pentium II technology for both the performance PC market (Pentium III) and the basic PC market (Celeron).



The Pentium III, Pentium II, and Celeron processors use the PICMG form factor with a right angle Slot 1 Connector. The PICMG design contains two gold leaf edge connectors compatible with PCI and ISA connectors to allow all peripherals to interface with the processor. This lets the SB686BX take advantage of the high pin density and strict electromechanical criteria imposed on PCI and ISA connectors. The ISA bus is buffered using 64mA drivers to ensure reliable operation for backplanes with more than five ISA slots.

The SB686BX combines the many features needed for system operation into one compact single board computer, including Ultra/DMA IDE drive controllers, high-performance serial ports, enhanced parallel port, and the latest BIOS features. Additional enhancements to the SB686BX include two USB ports and a programmable watchdog timer. Two dual in-line memory module (DIMM) sockets support up to 512MB of synchronous DRAM (SDRAM) memory. An internal 64-bit second level (L2) cache supports 512k of memory. The L2 cache speed is half the CPU core frequency. The Celeron L2 cache equals 128k running at full CPU core.

The 440BX AGPset in the SB686BX incorporates the latest microprocessing technology from Intel to provide the increased bandwidth needed to operate your system bus at speeds up to 100MHz. (The 440BX AGPset uses one chipset for both 66MHz and 100MHz system designs in Pentium III, Pentium II and Celeron processors with speeds of 366MHz and higher.)

The 440BX AGPset is a two-chip set comprised of the Intel 82443BX (PAC) host bridge and the Intel 82371EB (PIIX4E) I/O subsystem. The 64-bit main memory interface in the PAC provides optimized support for SDRAM at 100 and 66/60MHz. The PAC also includes the 32-bit PCI bus interface, the AGP interface with 133MHz data transfer capability, and extensive data buffering for increased throughput and concurrent operations.

The PIIX4E is a PCI Rev 2.1 compliant PCI-ISA bridge that supports 3.3V and 5V 33MHz PCI operations. Like the PAC, the PIIX4E chip includes Desktop Power Management support, enhanced DMA controller and an integrated IDE controller with Ultra DMA/33 support. In addition, it provides USB host interface support for two USB ports and a System Management Bus (SMB) with support for DIMM Serial PD.

The SB686BXV single board computer is further enhanced by the Intel 740 Graphics Accelerator for the Accelerated Graphics Port (AGP) to deliver the most advanced graphics and video support available. The 740 delivers exceptional 2D capabilities and pipelined 3D images to maximize graphics performance. The dedicated video engines support video conferencing and other video applications.

SB686BX and SB686BXC

The SB686BX single board computer combines the high-frequency Pentium III or Pentium II processor with the exceptional bandwidth capability of the dual independent bus (DIB) and the 100MHz system bus to deliver the high performance needed for the most demanding system applications. By using the Intel 440BX AGPset, the SB686BX with a Pentium III or Pentium II processor can increase the bandwidth of the system bus from 66MHz to 100MHz to provide substantial improvements to system performance.

The SB686BXC series single board computer with a Celeron processor delivers the best performance in the basic PC. The Celeron processor combines the benefits of P6 architecture and Intel MMX technology to deliver the best balance of performance and price. The Celeron processor provides a maxium bus speed of 66 MHz.

SB686BXV and SB686BXVC

The SB686BXV and SB686BXVC single board computers have been enhanced with the Intel 740 Graphics Accelerator for the Accelerated Graphics Port (AGP). The 740 AGP provides the most advanced graphics and video support available. Detailed information about the 740 Graphics Accelerator is available at *http://developer.intel.com/design/graphics/740.*

Year 2000 Compliance

ICS Advent warrants that the SB686BX Series has been tested for Year 2000 compliance. The boards have been verified to "roll over" to the year 2000 properly and to indicate the proper date for the leap year. This warranty applies to the board components only and does not guarantee that improperly written application software will report the year correctly.

Models Covered by this Manual

The following models include the single board computer with a Pentium III processor:

SB686BX3500 – Pentium III processor, 500MHz, 100MHz CPU bus
SB686BX3450 – Pentium III processor, 450MHz, 100MHz CPU bus

The following models include the single board computer with a Pentium II processor:

SB686BX450 – Pentium II processor, 450MHz, 100MHz CPU bus
SB686BX400 – Pentium II processor, 400MHz, 100MHz CPU bus
SB686BX350 – Pentium II processor, 350MHz, 100MHz CPU bus

The following models include the single board computer with a Celeron processor:

SB686BXC400 – Celeron Processor, 400MHz, 66MHz CPU bus
SB686BXC366 – Celeron Processor, 366MHz, 66MHz CPU bus

The following models include the single board computer with a Pentium III processor and Intel 740 AGP Graphics Accelorator with SVGA video:

SB686BXV3500 – Pentium III processor, 500MHz, 100MHz CPU bus
SB686BXV3450 – Pentium III processor, 450MHz, 100MHz CPU bus

The following models include the single board computer with a Pentium II processor and Intel 740 AGP Graphics Accelorator with SVGA video:

SB686BXV450 – Pentium II processor, 450MHz, 100MHz CPU bus
SB686BXV400 – Pentium II processor, 400MHz, 100MHz CPU bus
SB686BXV350 – Pentium II processor, 350MHz, 100MHz CPU bus

The following models include the single board computer with a Celeron processor and Intel 740 AGP Graphics Accelorator:

SB686BXVC400 – Celeron Processor, 400MHz, 66MHz CPU bus
SB686BXVC366 – Celeron Processor, 366MHz, 66MHz CPU bus

Chapter 2: Specifications

This chapter provides the specifications and an illustration of the SB686BX Series single board computer. Unless indicated, the following specifications apply to all models in the SB686BX Series.

Processors Supported

- Intel Pentium III with 512K L2 cache
- Intel Pentium II with 512K L2 cache
- Intel Celeron with 128K L2 cache

Processor Clock Frequency and Bus Speed

- Pentium III - 450MHz or 500MHz internal frequency and bus speed is 100MHz
- Pentium II - 350MHz, 400MHz, or 450MHz internal frequency and bus speed is 100MHz
- Celeron - 366MHz or 400MHz internal frequency and bus speed is 66MHz

Memory Capacity

- 16MB minimum
- 256MB maximum (non-ECC)
- 512MB maximum (ECC)

DIMM Support

- 2 banks, gold contacts, 168-pin
- Non-EC/EC/ECC compatible

Memory Speed Required

- 64/72-bit SDRAM (100 MHz)

BIOS

- Hi-Flex Pentium AMIBIOS, Flash EPROM support, Plug-and-Play compatible
- 2Mb flash upgradeable supporting BIOS upgrade via software
- Full support for Year 2000 and leap-year date functions

Chip Set

- Intel 440BX AGPset
  - 82443BX Host Bridge Controller (PCI/AGP)
  - 82371EB PCI/ISA/IDE Accelerator (PIIX4E)

Graphics Controller (SB686BXV and SB686BXVC only)

- Intel 740 AGP SVGA 3D accelerated graphics controller
- 8MB high-speed, 64bit SGRAM with 100MHz interface
- Integrated 24-bit 220MHz RAMDAC
- Rear panel DB-15, high density, 15-pin connector, female
- Display resolutions up to 1600 x 1200 (see **Table 2-1**)

Table 2-1: 740 AGP Video Resolutions

Resolution	Bits per Pixel (Hz)		
	8-bit Indexed	16-bit Indexed	24-bit Indexed
320 x 200	60, 72, 75, 85	60, 72, 75, 85	60, 72, 75, 85
320 x 240	60, 72, 75, 85	60, 72, 75, 85	60, 72, 75, 85
512 x 384	60, 72, 75, 85	60, 72, 75, 85	60, 72, 75, 85
640 x 350	85	85	85
640 x 480	60, 72, 75, 85	60, 72, 75, 85	60, 72, 75, 85
800 x 600	56, 60, 72, 75, 85	56, 60, 72, 75, 85	56, 60, 72, 75, 85
1024 x 768	60, 72, 75, 85	60, 72, 75, 85	60, 72, 75, 85
1280 x 1024	60, 72, 75, 85	60, 72, 75, 85	N/A
1600 x 1200	60, 75	N/A	N/A

EIDE Disk Controller (dual port)

- Four fixed disk drives supported (two each on primary and secondary PCI buses)
- PIO Mode 4 and Ultra DMA/33 support
- Full support for LS-120 HD floppy drive

Floppy Diskette Controller (dual port)

- Supports 1.44MB and 720K floppy drives, as well as LS-120 HD floppy drives.

Serial Ports

- Two RS232, 16C550-compatible, FIFO buffer
- ESD protected to ±15kV

Parallel Port

- Single parallel port controller with bidirectional compatibility
- EPP and ECP enhanced port modes

Keyboard, speaker, and reset port

- Single 8-pin header connector for system interface
- Keyboard power supplied through +5VDC self-healing fuse

PS/2 Mouse controller

- Microsoft compatible
- Six-pin mini-DIN connector at rear panel
- Single 8-pin header connector for system interface
- Power supplied through +5VDC self-healing fuse

Universal Serial Bus (USB)

- Universal Host Controller Interface (UHCI) configuration
- Dual USB connectors at rear panel via separate cable and bracket assembly (optional)
- Power supplied through +5VDC self-healing fuse

Watchdog Timer

- Reset CPU automatically if CPU stops operating
- Reset CPU automatically if +5VDC varies more than 5%
- Programmable to 100ms, 250ms, or 500ms
- Jumper or software disable/enable

Realtime Clock

- Motorola MC146818A compatible
- 256 bytes of battery-backed RAM
- Clock source at 14.318MHz accurate to ±1720Hz

CMOS Battery

- Onboard lithium 3.0V battery with diode protection circuitry.

Supported Operating Systems

- Windows 95, Windows 98–full support.
- Windows NT V4.0 and later, server or workstation–full support.
- QNX V4.24-video support limited to a maximum of 800 x 600 by operating system.
- Red Hat Linux V5.2-video support limited to 80x25 text mode.

Use offboard ISA or PCI video controllers with the following operating systems:

- SCO Unix V5.0 and later.
- SCO UnixWare V2.1 and later.
- Solaris V2.5.1 and later.
- OS/2 V2.0 and later.

Operating Environment

Temperature

- 5 to 50°C

Humidity

- 5 to 95% RHNC

Shock

- 2G, any axis

Vibration

- 0.5G, 10 to 2000Hz, any axis

Storage Environment

Temperature

- -40 to 85°C

Humidity

- 5 to 90% RHNC

MTBF

- 110,000 P.O.H. @ 25°C

Current Requirements

- +5V typical current draw: 6.4 – 8.1A
- +5V maximum current draw: 14.81–16.93A
- +12V maximum current draw: 200mA

Note: 1) +5V current draw is processor dependent.
2) Onboard +3.3 V is regulated down from the +5V source.

Agency Approvals

FCC conformity with:

47 CFR Part 15, Subpart B, Class A

CE conformity with:

EU EMC Directive 89/336/EEC

EU Low Voltage Directive 72/23/EEC

UL/cUL Recognized to

Ul 1950, 2nd Ed: 1993

cUL/CAN/CSA-C22.2 No. 950.93

Locations of Major Components on the SB686BX Series

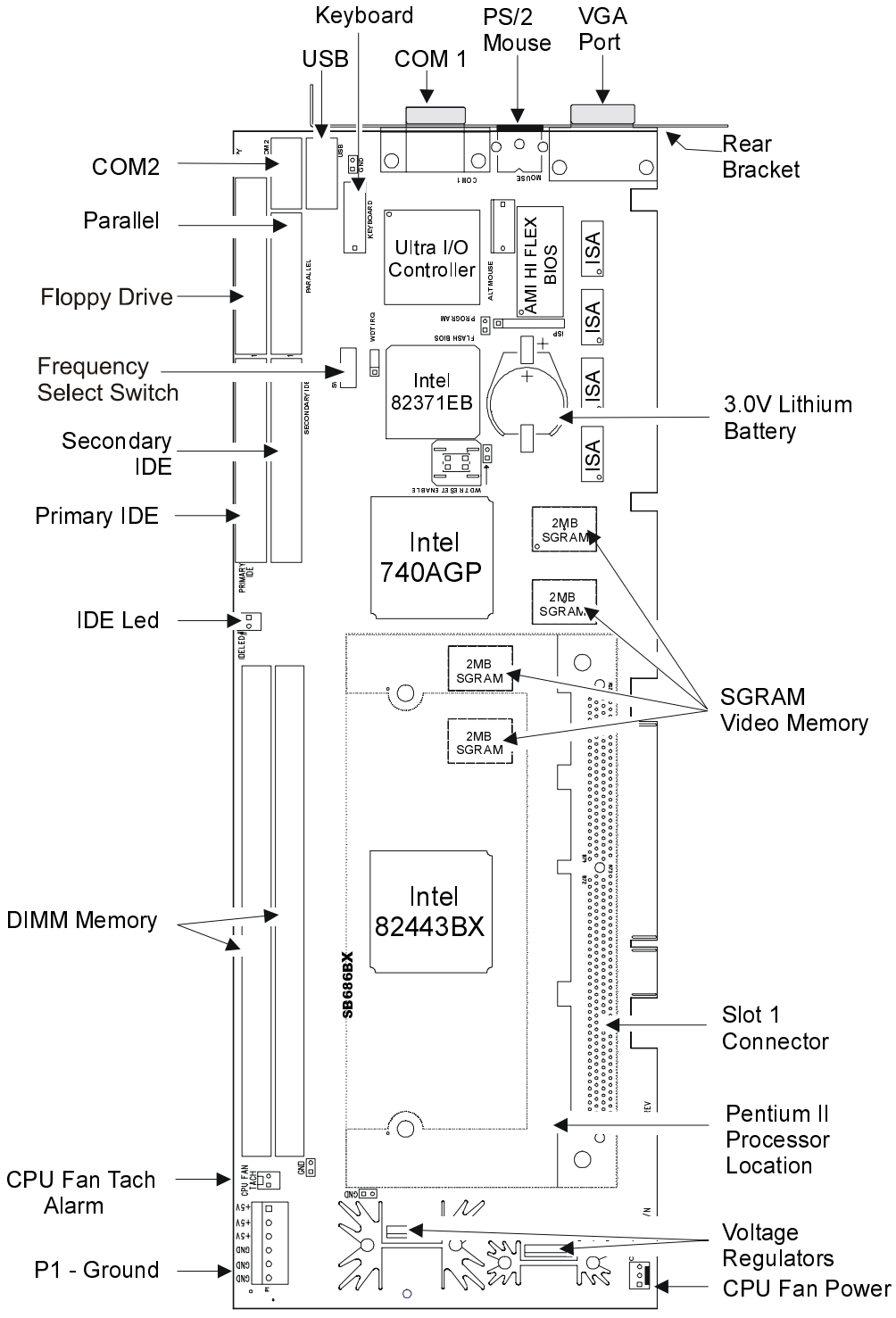


Figure 2-1: SB686BX Series Major Components

Chapter 3: Major Components

This section describes the major components, connectors, and layouts on the SB686BX single board computer. As you are reading this chapter refer to **Figure 3-1** for the diagram of the board components and connectors.

Features

Bus Support

The SB686BX single board computer includes the following bus support:

- 8.33 MHz ISA-AT Bus (64mA source with 32mA sink)
- 33MHz PCI 2.1 compliant PCI bus
- Switch-selectable 100MHz or 66MHz GTL+ for FSB
- 100MHz local memory AGP

Onboard Controllers

The onboard controllers for disk drives, serial ports, and parallel ports are incorporated into the design of the SB686BX single board computer. The SB686BXV also contains the advanced Intel 740 Graphics controller to take advantage of the 440BX chipset AGP port. All onboard controllers can be enabled or disabled through the system BIOS. Unless indicated, the following controllers are present in all models of the SB686BX single board computer.

Dual EIDE Disk Drive Controller (J4, J7)

The Primary IDE fixed disk drive interface is located at **J4** with the Secondary IDE connector placed at **J7**. Both EIDE connectors are located on the PCI local bus and support dual drives. The interface includes logical block addressing (LBA), PIO mode 4 support, and Ultra DMA/33 allowing up to 33Mb/sec data transfer rate throughput speeds.

Dual Diskette Drive Controller (J5)

The diskette drive controller at **J5** supports up to two drives. The diskette drive can support floppy disk formats from 360K to 2.88MB. Support is also offered for the LS-120 HD format floppy disk drive.

I/O Ports

The SB686BX(V) single board computer has two serial ports and one parallel port for I/O communications.

Serial Ports (J9, J16)

The serial ports are located at **J9** and **J16**. They are both compatible with the16550 UART. The serial port at J9 is extended through a 10-pin header on the board. J16 is extended through a DB-9 connector. Both serial ports are ESD protected to ±15kV on signal lines.

Enhanced Parallel Port (J8)

The SB686BX also includes an enhanced parallel port at **J8**, which is capable of bidirectional communication. The parallel port is extended through a 26-pin header on the board to a bracket-mounted DB-25 connector.

Watchdog Circuit (U28)-Not Shown

The watchdog circuit, located at **U28** on the back of the SBC, is a hardware timer that resets the CPU if the timer is not refreshed periodically. The circuit uses a trigger pulse provided by the onboard Eprom Flash (ISP1032E) programmable logic device to refresh itself. The watchdog timout period is software programmable to 100ms, 250ms, or 500ms. This timer is enabled by a switch setting on the back of the board. When enabled, the software needs to toggle bit "0" once every preselected millisecond period to prevent the timer from resetting the CPU. The watchdog circuit will also reset the CPU if the +5VDC power input falls below +4.75VDC. The watchdog prefail signal output can be routed to IRQ10 or IRQ11 via jumper to trigger the ISA bus IRQ if the watchdog time I/O space is not written to within half of the timeout period.

Universal Serial Bus (J12)

The high-speed, high-capacity Universal Serial Bus (USB) is located at **J12** and supports ISA/PCI passive backplanes with up to 6 PCI expansion slots. The USB supports data transfer rates of 12 Mbps(12 million bits per second) and is capable of connecting up to 127 peripheral devices, such as mice, modems, and keyboards. USB also allows Plug-and-Play installation and hot plugging where supported by the operating system. Refer to Chapter 4 for special installation instructions if you purchased the SB686BXV or the SB686BXVC with the Intel 740 AGP Graphics controller and your choice of operating systems is Windows 95. To operate the USB feature you must follow these instructions.

SB686BX Onboard Controllers (U9, U11)

The SB686BX(V) is designed around the Intel 440BX AGPset. It consists of the Intel 82443BX PCI/AGP controller (PAC) at **U9** and the Intel 82371EB PCI/ISA IDE accelerator (PIIX4E) bridge chip at **U11**.

The 440BX PAC chip is a 492-pin BGA (Ball Grid Array), which interfaces the Pentium II and Pentium III host address and data bus to the local PCI bus and memory section. The PAC chip integrates the main memory controller with support for 3.3V SDRAM DIMM modules with EC, ECC, and non-ECC capabilities. The SB686BX(V) contains two DIMM sockets and is configured as a Small Memory Array, which supports 6 rows for x8 and x16 single sided and dual sided DIMMs. The PAC operates the system bus at 66/100MHz and the PCI bus at 33MHz.

The PIIX4E is the other half of the chipset. It consists of a 324-pin BGA, which is a multifunction PCI device that acts as a PCI-to-ISA bridge function and a PCI-IDE controller. The PIIX4E also contains an enhanced DMA controller, two 82C59 interrupt controllers, an 8254 timer/counter, and a real time clock. The battery source for the real time clock is supplied by an industry standard CR2032 3.0 Volt lithium battery.

Main Memory (J1, J6)

The SB686BX has two dual in-line memory module (DIMM) sockets located at **J1** and **J6**. Minimum memory size is 16MB; maximum memory size is 512MB.

The SB686BX(V) supports the following memory particulars:

- 168-pin DIMMs with gold-plated contacts
- SDRAM (66MHz or 100MHz)
- Non-ECC (64-bit) and EC or ECC (72-bit) memory
- 3.3 Volt memory – unbuffered DRAM only
- Single- or double-sided DIMMs in the following sizes:

DIMM Size	Non-ECC Configuration	EC or ECC Configuration
16MB	2Mbit x 64	2Mbit x 72
32MB	4Mbit x 64	4Mbit x 72
64MB	8Mbit x 64	8Mbit x 72
128MB	16Mbit x 64	16Mbit x 72
256MB	(ECC only)	32Mbit x 72

Memory may be installed in one or two sockets and may vary in memory size between sockets.

Display Controller (U10)

Note: The display controller is installed only in the SB686BXV and SB686BXVC models.

The Intel 740 graphics accelerator, located at **U10**, works through the Accelerated Graphics Port (AGP) in the 440BX AGPset. The 740 supports perspective-correct texture mapping, MIP-Mapping, Gouraud shading, alpha-blending, stippling, anti-aliasing, fogging, and Z Buffering. 8MB of high-speed 64-bit SGRAM memory is built in to the SB686BXV and SB686BXVC to provide the utmost in graphics capabilities and speed. In addition, the video controller has a 100MHz interface to deliver video resolutions up to 1600 x 1200 with 256 colors. **Table 2-1** lists the refresh rates and maximum colors available for the supported resolutions.

The analog video is routed through a high density DB15 VGA connector located on the rear bracket at J23. See the section for connector locations and pinouts later in this chapter. Along with the controller, you will receive a set of diskettes containing video display drivers and display-enhancement utilities. The diskettes also contain documentation for installing and configuring the drivers.

Flash ROM (U30)

The flash ROM used for BIOS and Plug and Play (PnP) functionality in the SB686BX(V) is a 40-pin TSOP (Thin Small Outline Package) 2Mb chipset. It also allows more BIOS-embedded features, such as video. All device programming is managed through the floppy disk drive (see Appendix A for more flash ROM information). In addition, all flash writes are qualified through the use of the onboard PLD (Programmable Logic Device) and Ultra I/O general purpose register to avoid accidental BIOS corruption.

Onboard PLD (J19)

The onboard PLD is a multifunction in-circuit-programmable 100 pin TQFP from Lattice Semiconductor.

I/O Port Controller (U12)

A 160-pin ultra I/O controller at **U12** processes much of the I/O functionality of the SB686BX series. The ultra I/O controller is an ISA PnP compatible controller that contains the keyboard and PS/2 mouse controllers, floppy disk controller, UARTs for serial ports, parallel port, and general purpose I/O registers. The PS/2 mouse connector at **J2**1 is a 6-pin mini-DIN located at the rear bracket. The keyboard (located at **J13**) signals are onboard the SBC connector. Filters have been placed where the mouse and keyboard signals to reduce EMI. The floppy disk connector (**J5**), parallel port connector (**J8**), and COM Port 2 (**J9**) connector all consist of headers located on the SBC. The COM Port 1 (**J16**) connector uses a DB9 located on the rear bracket of the feature card. See the following section for exact connector locations and pinout details.

Real-Time Clock, CMOS SRAM, and Battery

The real-time clock is compatible with the Motorola MC146818A. This clock provides time-of-day, alarm features, and a multi-century calendar with century rollover. It supports 256 bytes of battery-backed CMOS SRAM in two banks that are reserved for BIOS use.

A lithium coin-cell battery powers the real-time clock and CMOS memory . The battery has an estimated life of seven years. When the computer is on, current from the power supply (3.3V) will extend the life of the battery. The 14.318MHz clock is accurate to ± 1720Hz or ± 13 minutes/year at 25ºC with 3.3V applied.

Note: The time, date, and CMOS values should be defined in the setup program. Also, the CMOS values may be returned to their default settings via the setup program.

Connectors

The SB686BX and SB686BXV have several rear panel and onboard connectors. Silkscreened numbers identify the connectors and square pads mark each pin 1 to prevent improper connection. All pins that supply power to an external connection are fused for protection.

Note: The # symbol in the following pinouts indicates an active low signal.

J1: DIMM Memory Socket

168-pin "Small Memory Array" socket to support 6 rows for x8 and x16 single-sided and dual-sided SDRAM Dimms.

J2: IDE Hard Drive LED Connector

The J2 connector (*2-pin header*) provides the IDE hard drive access signal. This connector has a 5V differential to activate any IDE hard drive access LED used in the chassis.

1	LED OUT	2	GND (tied to +5V via 330 ohms)

J3: Not Used

J4: Primary EIDE Hard Drive Connector

The J4 connector (*40-pin dual row header*) supplies signals from an onboard EIDE controller to interface up to two EIDE hard drives.

1	RESET	2	GND
3	DATA 7	4	DATA 8
5	DATA 6	6	DATA 9
7	DATA 5	8	DATA 10
9	DATA 4	10	DATA 11
11	DATA 3	12	DATA 12
13	DATA 2	14	DATA 13
15	DATA 1	16	DATA 14
17	DATA 0	18	DATA 15
19	GND	20	N/C (Key)
21	DMA Request	22	GND
23	I/O Write	24	GND
25	I/O Read	26	GND
27	IORDY	28	Cable Select
29	DMA ACK	30	GND
31	IRQ 14	32	N/C
33	Address 1	34	N/C
35	Address 0	36	Address 2
37	Chip Select 0	38	Chip Select 1
39	LED	40	GND

J5: Floppy Drive Connector

The J5 connector (*34-pin dual row header*) supplies the signal from an onboard diskette drive controller for one or two diskette drives.

1	GND	2	DRVEN0
3	GND	4	N/C (Reserved)
5	GND	6	DRVEN1
7	GND	8	INDEX#
9	GND	10	FDME0#
11	GND	12	FDSEL1#
13	GND	14	FDSEL0#
15	GND	16	FDME1#
17	GND	18	DIR#
19	GND	20	STEP#
21	GND	22	WRDATA#
23	GND	24	WRGATE#
25	GND	26	TRK0#
27	GND	28	WRPRO#
29	GND	30	RDDATA#
31	GND	32	HDSEL#
33	GND	34	DSKCHG#

The "#" after a signal indicates an active low signal.

J6: DIMM Memory Socket

168-pin "Small Memory Array" socket to support rows for x8 and x16 single-sided and dual-sided SDRAM Dimms.

J7: Secondary EIDE Hard Drive Connector

The J7 connector (*40-pin dual row header*) supplies signals from an onboard EIDE controller to interface up to two EIDE hard drives.

1	RESET	2	GND
3	DATA 7	4	DATA 8
5	DATA 6	6	DATA 9
7	DATA 5	8	DATA 10
9	DATA 4	10	DATA 11
11	DATA 3	12	DATA 12
13	DATA 2	14	DATA 13
15	DATA 1	16	DATA 14
17	DATA 0	18	DATA 15
19	GND	20	N/C (Key)
21	DMA Request	22	GND
23	I/O Write	24	GND
25	I/O Read	26	GND
27	IORDY	28	Cable Select
29	DMA ACK	30	GND
31	IRQ 14	32	N/C
33	Address 1	34	N/C
35	Address 0	36	Address 2
37	Chip Select 0	38	Chip Select 1
39	LED	40	GND

J8: Parallel Port Connector

The J8 connector (*26-pin dual row header*) allows the use of parallel devices, typically printers. Your computer will be delivered with this port already connected to a slot filler bracket for easier access.

1	STROBE#	2	AUTOFEED#
3	DATABIT0	4	FAULT#
5	DATABIT1	6	INIT#
7	DATABIT2	8	SLCTIN#
9	DATABIT3	10	GND
11	DATABIT4	12	GND
13	DATABIT5	14	GND
15	DATABIT6	16	GND
17	DATABIT7	18	GND
19	ACK#	20	GND
21	BUSY	22	GND
23	PERR	24	GND
25	SELECT	26	N/C

The "#" after a signal indicates an active low signal.

J9: COM2 Connector

The J9 connector (*10-pin dual row header*) is the second system serial port, which allows the use of serial devices or serial communications. Your SB686BX will be delivered with this port already connected to a slot filler bracket for easier access.

1	CD	2	DSR
3	RX	4	RTS
5	TX	6	CTS
7	DTR	8	RI
9	GND	10	N/C

J10: GND

J11: Not Used

J12: USB Port 1 & 2 Connector

The J12 connector (*10-pin dual row shrouded header*) allows the use of the universal serial bus, port 1 and 2.

1	USB1 +5V	2	USB0 +5V
3	USB1 -	4	USB0 -
5	USB1 +	6	USB0 +
7	USB1 GND	8	USB0 GND
9	N/C	10	USB Shield GND

An optional bracket is offered for use with the dual USB port to provide rear panel connections.

J13: Keyboard Connector

The J13 connector (*8-pin header*) is the place to connect your keyboard connector that routes to the location on your chassis where you plug in your keyboard.

1	PBRST#	2	GND
3	N/C	4	KBDCLOCK
5	KBDDATA	6	KBDLOCK
7	+5V (Fused)	8	SPKR#

J14: GND

J15: GND

J16: COM1 Connector

The J16 connector (*DB9*) is the first system serial port. Typically it provides connection for a serial mouse or for serial communications.

1	CD	2	RX
3	TX	4	DTR
5	GND	6	DSR
7	DTR	8	CTS
9	RI		

J17: WatchDog Timer Reset Enable

The J17 connector (*2-pin header*) provides the enable for the watchdog timer reset. The SB686BX boards are delivered with the jumper in the default setting (the jumper is only on pin 1). When you need to enable the watchdog timer reset, you must place the jumper across pins 1 and 2.

J18: Not Used

J19: PLD ISP Connector

Reserved for company use

J20: Alternate P/S-2 Mouse Connector

The J20 connector (*6-pin header*) provides an alternate connection to a P/S-2–type mouse.

1	MDATA	2	N/C
3	GND	4	+5V (fused)
5	MCLOCK	6	Shield GND

J21: P/S-2 Connector

The J21 connector (*6-pin mini-DIN*) allows you to connect a P/S-2 type mouse.

1	MDATA	2	N/C
3	GND	4	+5V (fused)
5	MCLOCK	6	N/C

J22: Not Used

J23: VGA Connector

The J23 connector (*HDB15*) supplies the signal from the *optional* video graphics controller to the monitor.

1	RED	2	GREEN
3	BLUE	4	N/C (Reserved)
5	GND	6	GND
7	GND	8	GND
9	N/C	10	GND
11	N/C	12	DDCDAT
13	HSYNC	14	VSYNC
15	DDCCLK		

Jumper Connectors

JP1: Fan Tachometer Connector

The JP1 connector is a 2-pin single row friction lock type connector. The SB686BX models are delivered with a fan tachometer for the microprocessor. This tachometer receives its power through the JP6 connector.

1	GND	2	TACH

This connection is used to provide an alarm signal for Industrial Computer Source chassis which provide the monitoring function.

JP2: CMOS Setup Jumper

JP2 is 3-pin connector used to clear the CMOS. All SB686BX boards delivered with the jumper in the default setting. Pins 2 and 3 will have the jumper across them in the default setting. When it is necessary to clear the CMOS settings the shut will be applied to pins 1 and 2 as described in chapter 4 (see the section on CMOS Clear).

JP3: WDT IRQ Select Jumper

JP3 is 3-pin connector used to select the IRQ-10 or IRQ-11. The jumper should be placed on pins 1-2 if you are selecting IRQ-10. If you want to select IRQ-11, place the jumper on pins 2-3.

1	IRQ-10	2	WDT signal
3	IRQ-11		

JP4: Flash Mode Jumper

The JP4 is 3-pin connector used in the process to update the Flash ROM. All SB686BX boards delivered with the jumper in the default setting. Pins 2 and 3 will have the jumper across them in the the default setting. Do not place the jumper on pins 1 and 2, this is for company use only.

JP6: Fan Power Connector

The SB686BX models are delivered with a fan appropriate for the microprocessor. This fan is powered through the JP6 connector (*3-pin single row friction lock*) with +12VDC.

1	GND	2	+12V
3	TACH		

P1: +5 Volt Input Connector

The P1 connector (*6-pin header*) is the voltage input connector.

1	+5V	2	+5V
3	+5V	4	GND
5	GND	6	GND

Board Layout

Figure 3-1 illustrates the SB686BXV single board computer. Standard PICMG dimensions are used for all boards. Notice in particular the connectors listed in the previous section.

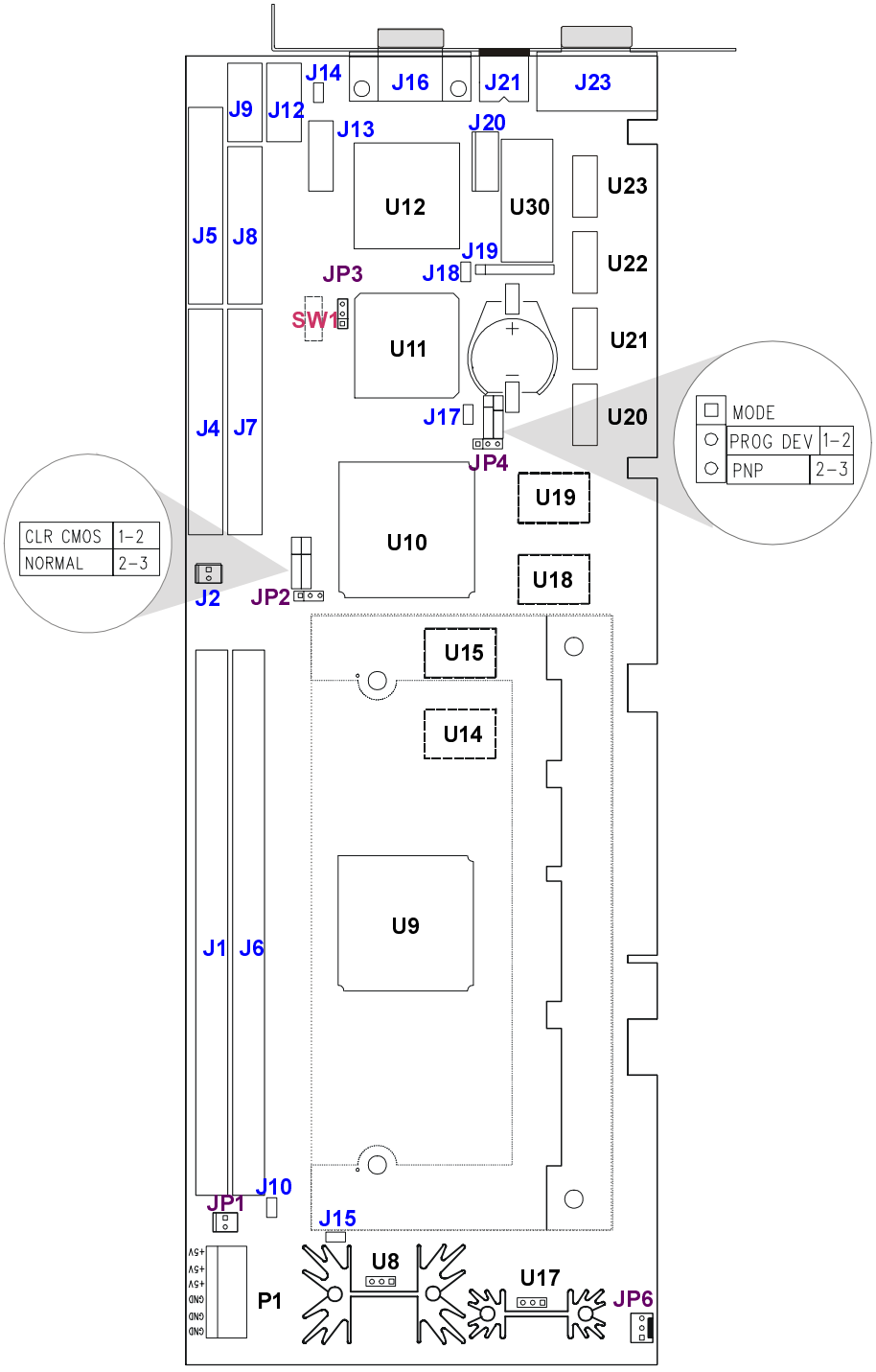


Figure 3-1: SB686BX Jumpers and Connections

Chapter 4: Installation and Configuration

If you purchased a SB686BX Series single board computer with a chassis, the board and its components were tested for you prior to shipment. However, if you upgrade or replace components, this chapter covers the steps necessary to ensure that the new items will work properly with your single board computer.

Upgrading your system may require installing board components (such as the memory), configuring the system (setting DIP switches for component compatibility or to enable functions), connecting the input/output devices, and setting up the operating system. Depending on your system, you may only need to do part of this process, but each part of the computer is interdependent, so please check related topics for compatibility. For example, if you are upgrading your processor from 333 to 450MHz, you must change DIP switch settings for the faster processor speed.

For the location of the components and connectors discussed in this chapter please refer to **Figure 3-1** in the previous chapter.

Installing the SDRAM DIMM Memory (J1, J6)

One of the user-changeable board components is the Synchronous Dynamic Random Access Memory (SDRAM) at **J1** and **J6**, shown in **Figure 3-1**. Follow the steps below to install the SDRAM correctly.

The SB686BX Series single board computer accepts from 16MB up to 512MB of SDRAM. The two 168-pin SDRAM Dual Inline Memory Module (DIMM) sockets will accept 64- and 72-bit DIMM modules (3.3V memory – unbuffered SDRAM only).

The single board computer will accept only DIMMs with gold-plated contacts. To ensure reliable operation at zero wait states, use only 10ns or faster SDRAM DIMMs for bus speeds less than 100MHz. For 100MHz or higher, use only 8ns or faster SDRAM DIMMs. If both memory DIMM sockets are used, they may be filled with different size memory, but the DIMMs should be made by the same manufacturer and be of the same speed.

Note: Before performing the following procedures, remove the board from the backplane and lay it on a flat ESD protected, non-static surface.



CAUTION!



DIMM sockets are very durable but can be broken. Use extreme care when removing a DIMM from the socket. Never force a DIMM into a socket and make sure the DIMM is in the correct orientation before installation. **Any DIMM sockets broken due to ABUSE, MISHANDLING, or ACCIDENT are not covered under the warranty.**

CAUTION!

Be sure to take proper electrostatic discharge precautions ***before*** starting any work.

1. Move the module release levers (one on each end of the socket) outward, away from the socket (**Figure 4-1**).

2. Place the DIMM so that the two notches on the contact edge line up with the two alignment nodes in the DIMM socket. Insert the DIMM into the socket at a 90-degree angle.

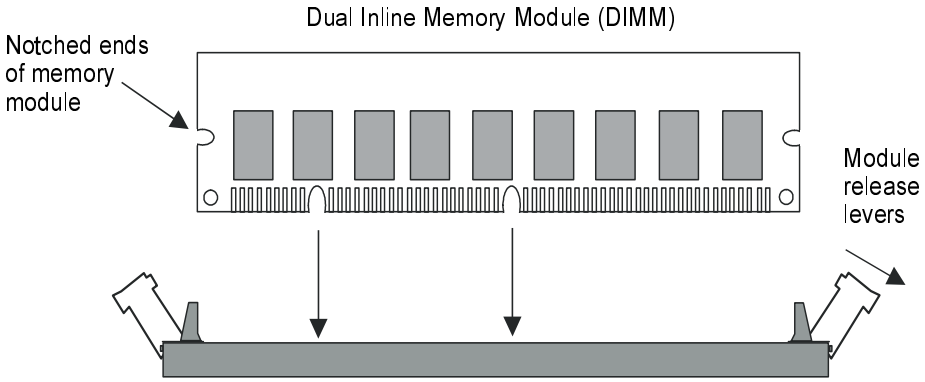


Figure 4-1: DIMM Orientation

3. Using both hands, press downward and guide the DIMM into the socket. The module release levers will return to their upright position when the DIMM is completely seated in the socket. The pegs on the tips of the release levers should align with the notches on both ends of the DIMM (**Figure 4-2**).

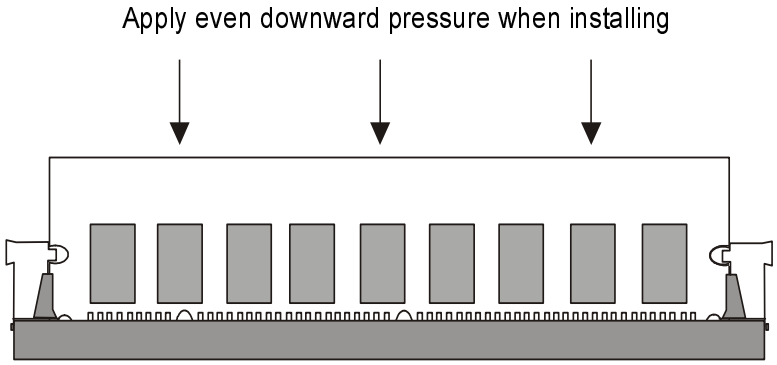


Figure 4-2: DIMM Installation

Dual EIDE and Floppy Drive Connections (J4, J7, J5)

The primary EIDE connector is **J4**, and the secondary EIDE connector is **J7**. Both support LBA mode, and each will connect up to two devices. **J5** is the floppy connector. It will also connect up to two devices. The connectors are keyed so the cables will only connect in the correct direction (**Figure 3-1**).

COM1 and COM2 Dual Serial Ports (J16,J9)

COM1 and COM2, located at **J16** and **J9** respectively (**Figure 3-1**), are dual serial ports set to RS232 standards. The ports use a 16550 compatible dual serial port controller and have 16 byte transmit/receive FIFO buffers. Both ports are ESD protected to ±15kV

Bus Speed (SW1)

SW1 on the SB686BX Series allows you to set the bus speed for the CPU, please see **Figure 3-1** for the location of the switch on the circuit board. **Table 4-1** lists the settings for both Celeron, Pentium II, and Pentium III processors. **Figure 4-3** shows a detail of the switch configured for a Pentium II 350MHz processor.

Table 4-1: SW1 Settings

System Bus Frequency Multiplier	Processor Speed (MHz)	Switch Settings				
		1-1	1-2	1-3	1-4	1-5
11/2	Celeron 366MHz	ON	N/A	N/A	N/A	N/A
6	Celeron 400MHz	ON	N/A	N/A	N/A	N/A
7/2	Pentium II 350MHz	OFF	OFF	ON	OFF	ON
4	Pentium II 400MHz	OFF	ON	ON	ON	OFF
9/2	Pentium II 450MHz	OFF	OFF	ON	ON	OFF
9/2	Pentium III 450MHz	OFF	N/A	N/A	N/A	N/A
5	Pentium III 500MHz	OFF	N/A	N/A	N/A	N/A
All other combinations are reserved.						

Notes: 1) Celeron and Pentium III are autosensing and only require a setting of switch **1-1**. This sets the bus speed (66 or 100).
2) Pins 6, 7, and 8 on SW1 are reserved for factory use.



Figure 4-3: SW1 Settings for 350MHz Pentium II Processor

Watchdog Timer Configuration (J17)

The watchdog timer is embedded in the onboard PLD as described in Chapter 3. The timer can be configured by software using a general-purpose decode register on the Ultra I/O controller. (Refer to Appendix B for information on configuring the watchdog timer via software). You can select one of three timeout periods: 100ms, 250ms, or 500ms.

To enable the timer, you must configure it by software and place a shunt over **J17**. You must use this jumper if you want to use the watchdog timer feature.

To select an optional pre-timeout interrupt, place a shunt on **JP3**. Place the shunt over pins 1 and 2 to select IRQ10 *or* over pins 2 and 3 to select IRQ11. Program the selected IRQ with the same software used to configure the timer. The pre-timeout interrupt signal triggers if it is not refreshed within half of the specified timeout period. For example, if you select a timeout period of 500ms, the refresh signal must be received within 250ms. Otherwise, the interrupt will be generated.

In addition to its programmable features, the watchdog timer also has a +5VDC monitor. If VCC falls between 4.5VDC and 4.75VDC then a hard reset may occur. If VCC falls below 4.5VDC, a hard reset will definitely be performed.

Flash BIOS (JP4)

If you upgrade your flash BIOS make sure that the jumper is in place on pins 2 and 3. You should not need to change the jumper settings. When you receive your board, it should already have the jumper on pins 2 and 3, this is the default setting.

- Do not place the jumper on pins 1 and 2. These pins are reserved for factory use.
- To upgrade your flash ROM via floppy, ensure the jumper is over pins 2 and 3. This is the default setting and it should not be changed.

CMOS Clear (JP2)

JP2 clears the CMOS.

- To clear CMOS, turn off the power and place a shunt over pins 1 and 2 for approximately five seconds.
- To resume normal operation, replace the shunt over pins 2 and 3 and power on the system.

Windows 95 Installation

If you purchased the SB686BXV or the SB686BXVC with the Intel 740 AGP Graphics controller, you must take an additional step when installing Windows 95. (Of the operating systems listed in Chapter 2, only Windows 95 requires these changes.)

Note: Make sure your Windows 95 software includes USB support, and take the extra steps listed below *before* installing your video drivers.

USB Supplement

OSR 2.1

For OSR 2.1, locate a folder on the CD labeled OTHER/USB. In that folder, locate the README.TXT file. Follow the instructions in the file.

OSR 2.5

For OSR 2.5, locate a folder on the CD labeled OTHER/UPDATES/USB. In that folder, locate the USB.TXT file. Follow the instructions in the file.

Intel .INF Update

For best results, obtain the latest Windows 95 .INF update utility for the 440BX chipset. The .INF update allows Windows 95 to recognize and fully utilize the 440BX chipset. The file is available from the Intel website *(http://developer.intel.com/design/chipsets/drivers/inf_update.htm)*.

SB686BX Series Current Requirements

The SB686BX Series current requirements vary according to the backplane option selected as shown in **Table 4-2**. See **Table 4-3** for the minimum number of conductors (+5V wires) that must to be connected to **P1** (auxiliary 5V supply) to supply adequate current to operate the single board computer properly.

ISA-only backplanes have three +5V pins on the ISA connector. Each ISA pin is rated for 3 Amps, providing a total of only 9A to any ISA card. Therefore, it is necessary to use the extra power connector on the SB686BX to supply an additional +5V input via HDD power connectors from the system power supply. An accessory power connector is included with your SB686BX Series which provides 3 HDD connectors to adapt to the P1 connector.

The ISA/PCI backplanes are designed with three +5V pins on the ISA connector and 13 +5V pins on the PCI connector. Each ISA pin is rated for 3A while each PCI pin is rated for 1A. This allows for a total of 22A that can be supplied to the SB686BX using the following equation:

$$(3 \text{ ISA pins} \times 3A) + (13 \text{ PCI pins} \times 1A) = 22A$$

The more power you supply to the SB686BX Series via P1, the less power your system will have to supply via the backplane. If your system is heavily loaded with expansion boards, consider using more connections at P1 than the minimum number specified in **Table 4-3**.

Table 4-2: Power Matrix

Processor Speed	Amperes Required	
	Maximum	Typical
Celeron 366MHz	15.17	7.5
Celeron 400MHz	15.57	7.4
Pentium II 350MHz	14.81	7.7
Pentium II 400MHz	15.73	6.4
Pentium II 450MHz	16.37	8.1
Pentium III 450MHz	16.19	7.2
Pentium III 500MHz	16.93	7.5

Table 4-3: Conductor Matrix

Processor Speed	Minimum Number of 5V Conductors	
	ISA	ISA/PCI
Celeron 366MHz	1	0
Celeron 400MHz	1	0
Pentium II 350MHz	1	0
Pentium II 400MHz	1	0
Pentium II 450MHz	2	0
Pentium III 450MHz	1	0
Pentium III 500MHz	1	0

Chapter 5: Maintenance and Troubleshooting

This chapter provides minimal maintenance and troubleshooting information for your SB686BX single board computer. If you need assistance with these procedures, please call Technical Support at **800-480-0044** (U.S. and Canada) or **858-677-0877** (international).

FCC Compliance Statement for Class A Devices

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference, and
2. This device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and radiates radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference, in which case the user will be required to correct the interference at his or her own expense.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Note: The assembler of a personal computer system may be required to test the system and/or make necessary modifications if a system is found to cause harmful interference or to be non-compliant with the appropriate standards for its intended use.

How to Remain CE Compliant

The SB686BX Series single board computer is designed to be CE compliant when used in a CE compliant chassis. Maintaining CE compliance also requires proper cable and cabling techniques. Although ICS Advent offers accessories, the customer must ensure that these products are installed with proper shielding to maintain CE compliance. ICS Advent does not offer engineering services for designing cabling systems. In addition, ICS Advent will not retest or recertify systems or components that have been reconfigured by customers.

Troubleshooting

All components of a computer are interrelated. That is, a "video" problem may be caused by the disk controller. The simplest diagnostic technique involves replacing the suspect card with a new one. If that doesn't fix the problem, remove all cards except the minimum required by the system. Then run the system, replacing each card until the problem is repeated.

Note: The assembler of a personal computer system may be required to test the system and/or make necessary modifications if a system is found to cause harmful interference or to be non-compliant with the appropriate standards for its intended use.



WARNING!



The following procedures involve working near high voltage. Contact with this voltage can seriously injure you. Accidental shorting of the circuits can damage the computer.



CAUTION!



The following procedures involve working with a device that is sensitive to static electricity. Use proper precautions to protect against electrostatic discharge (ESD). Only qualified personnel should attempt these procedures.

CPU does not boot, there is no beep, and there is no video.

A. Ensure that the SB686BX Series single board computer is fully and correctly seated into the backplane.

B. Turn the power off and clear the CMOS via JP2.

C. Contact the ICS Advent to receive the latest BIOS flash file. Please refer to Appendix A for BIOS upgrade instructions.

D. Check the SB686BX Series single board computer to ensure that all jumpers are installed as indicated in Chapter 4.

Hard disk drive controller failure on bootup.

A. If you are using an IDE hard drive to boot, ensure that the power connector and the ribbon cable are properly connected.

B. Check that the drive is configured properly as master or slave by jumpers on the drive.

C. Check that the HDD parameters are set up correctly in the CMOS Setup. (You can use auto-detect hard disk to auto-detect the correct HDD parameters.)

Non Plug-and-Play ISA card is not functioning properly.

A. If this card uses an IRQ, make sure that the particular IRQ is reserved to the 'ISA' bus in PCI/PnP setup in CMOS.

When booting, the CPU reports No ROM BASIC.

A. The system cannot find a proper bootable sector on either drive A or C. You need to install an operating system on the hard drive or insert a bootable diskette in the A drive.

When booting, the System gives eight beeps.

A. These beeps indicate a video adapter problem. Try the video card in a different slot.

B. Try a different video card.

C. If you are installing an external video card, determine if your board has onboard video. If it does, you need to disable the video in the CMOS PCI/PnP setup before installing the external video card.

D. If the problem persists, clear CMOS and re-flash the BIOS as discussed in the AMI BIOS Manual (Appendix A).

Note: If your SB686BX Series single board computer has onboard video and you are using a separate video card, clearing the CMOS enables the onboard PCI video option in CMOS (default setting).

When booting the system, you hear two beeps.

A. Two beeps signify a memory error. Re-seat the DIMMs into the DIMM sockets and reboot.

B. If the problem persists, swap DIMMs from one memory bank to the other. If the problem goes away after the swap, then switch the memory back to the original installation and see if the original error occurs.

C. If the problem continues to persist, replace the modules with your spare memory modules.

D. If the problem still persists after installing new memory, then the SB686BX Series board may have faulty DIMM sockets and may need to be returned for repair.

The system runs very slow.

A. The system will run significantly slower if the cache memory has been disabled in the Advanced Setup in CMOS. (Cache memory is automatically disabled when you choose the Fail-Safe option in CMOS setup.)

B. Check that the DIP switch settings are correct for the CPU speed as described in Chapter 4.

Returns

If you need to return a product to ICS Advent for any reason, the following applies:

1. Call Customer Service for a Return Material Authorization (RMA) number. The RMA number must be visible on the outside of the box in which you pack the product. Shipments without an RMA number will not be accepted by Customer Service Receiving.
2. Properly pack the product. Put the computer board into an appropriate ESD protective bag and seal to prevent moisture and dirt from entering.
3. Provide adequate packaging and use standard ESD precautions. If possible, use the original box and packing in which the product arrived. A minimum of four inches of proper packing material is required around all sides of computer products. Double-thick cardboard is preferred. **Do not use styrofoam peanuts or loose fill to pack.** Assume the box will be dropped several feet during shipping.
4. Do not ship by motor freight. Use a carrier such as Burlington, Airborne, or Federal Express.

Appendix A

AMIBIOS

for the Intel 440BX Chipset

for PCI, PnP, and ISA Systems

with Flash ROM Support

User's Guide

Modified for use with the SB686BX Series products from ICS Advent

Based on the 07/15/95 V6.31.00 Core AMIBIOS

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Chapter 1: Introduction

This manual documents the AMIBIOS for the Intel 440BX chipset based on the 07/15/95 V6.31.00 core AMIBIOS. This AMIBIOS is designed for a Pentium II-based ISA computer system with an SMC 932 Super I/O controller. This AMIBIOS also suppports IDE on the PCI local bus.

Plug and Play Support

This AMIBIOS supports the Plug and Play Version 1.0A specification. ESCD (Extended System Configuration Data) write is supported.

PCI Bus Support

This AMIBIOS also supports Version 2.1 of the Intel PCI (Peripheral Component Interconnect) local bus specification. Please see the Intel technical documentation for additional information.

DRAM Support

SDRAM (Synchronous DRAM) is supported.

Flash ROM Support

Flash ROM support is also included in this AMIBIOS. To reprogram the flash ROM, get an updated BIOS ROM file from ICS Advent. Copy this file to a floppy. Insert the floppy into drive A: and press <Ctrl> <Home> while powering on.

Supported CPUs

This AMIBIOS supports a single Intel Pentium II CPU.

System BIOS

The BIOS is the basic input output system used in all IBM® PC-, XT®-, AT®-, and PS/2®-compatible computers. The AMIBIOS is a high-quality example of a system BIOS.

How Data is Configured

AMIBIOS provides a Setup utility in ROM that is accessed by pressing <Del> at the appropriate time during system boot. Setup configures data in CMOS RAM. The main menu options are described below.

Setup Options	Description
Standard CMOS Setup	Sets time, date, hard disk type, types of floppy drives, monitor type, and detects if keyboard is connected (see Chapter 2).
Advanced CMOS Setup	Sets Quick Boot, System Boot Up Sequence, and many other options (see Chapter 3).
Advanced Chipset Setup	Sets chipset-specific options and features (see Chapter 4).
PCI/Plug and Play Setup	Sets options related to the PCI bus and Plug and Play options (see Chapter 5).
Peripheral Setup	Controls I/O Controller-related options (see Chapter 6).

Setup Options	Description
Auto Detect Hard Disks	Automatically detects the connected IDE drives.
Change User Password	This option is grayed until you change the supervisor password. If the option is available, the default is no user password.
Change Supervisor Password	Allows you to set or change a supervisor password that restricts access to the AMIBIOS main menu. The default is no supervisor password, which also means that no user password is required.
Auto Configuration with Optimal Settings	When you save your settings and exit the main menu, AMIBIOS automatically configures your system to optimal settings. This option is recommended as the most efficient choice for implementing AMIBIOS.
Auto Configuration with Fail Safe Settings	When you save your settings and exit the main menu, AMIBIOS automatically configures your system to fail-safe settings.
Save Settings and Exit	Saves any changes you made from the main menu, exits, and reboots your system with the new settings.
Exit without Saving	Exits the main menu and reboots without saving changes to AMIBIOS settings.

Keys	Function
Esc	Exits the main menu and reboots your system without saving changes.
F10	Saves your changes, exits, and reboots your system.
↑ and ↓	Scroll up and down the main menu.
F2 and F3	Toggle through video color or monochrome options.

Chapter 2: Standard CMOS Setup

Select the AMIBIOS Setup options by choosing Standard Setup from the AMIBIOS Setup main menu. Standard Setup options are described below.

Floppy Drive A: and/or B:

Move the cursor to these fields via ↑ and ↓ keys and select the floppy type. The settings are *360 KB 5¼ inch*, *1.2 MB 5¼ inch*, *720 KB 3½ inch*, *1.44 MB 3½ inch*, *2.88 MB 3½ inch*.

Primary Master, Primary Slave, Secondary Master, and Secondary Slave

Select these options to configure the drive named in the option. Select *Auto Detect IDE* to let AMIBIOS automatically configure the drive. A screen with a list of drive parameters appears. Click on *OK* to configure the drive.

Type	How to Configure
SCSI	Select *Type*. Select *Not Installed* on the drive parameter screen. The SCSI drivers provided by the SCSI manufacturer should allow you to configure the SCSI drive.
IDE	Select *Type.* Select *Auto* to let AMIBIOS determine the parameters. Click on *OK* when AMIBIOS displays the drive parameters. Select *LBA Mode*. Select *On* if the drive has a capacity greater than 540 MB. Select *Block Mode*. Select *On* to allow block mode data transfers. Select *32-Bit Mode*. Select *On* to allow 32-bit data transfers. Select the *PIO Mode*. It is best to select *Auto* to allow AMIBIOS to determine the PIO mode. If you select a PIO mode that is not supported by the IDE drive, the drive will not work properly. If you are absolutely certain that you know the drive's PIO mode, select PIO mode 0 – 4, as appropriate.
CD-ROM	Select *Type*. Select *CDROM*. Click on *OK* when AMIBIOS displays the drive parameters.
Standard MFM	Select *Type.* You must know the drive parameters. Select the drive type that exactly matches your drive's parameters.
Non-Standard MFM	Select *Type.* If the drive parameters do not match the drive parameters listed for drive types 1– 46, select *User* and enter the correct hard disk drive parameters.

Entering Drive Parameters

You can also enter the hard disk drive parameters. The drive parameters are:

Parameter	Description
Type	The number for a drive with certain identification parameters.
Cylinders	The number of cylinders in the disk drive.
Heads	The number of heads.
Write Precompensation	The actual physical size of a sector gets progressively smaller as the track diameter diminishes. Yet each sector must still hold 512 bytes. Write precompensation circuitry on the hard disk compensates for the physical difference in sector size by boosting the write current for sectors on inner tracks. This parameter is the track number on the disk surface where write precompensation begins.
Landing Zone	This number is the cylinder location where the heads normally park when the system is shut down.
Sectors	The number of sectors per track. MFM drives have 17 sectors per track. RLL drives have 26 sectors per track. ESDI drives have 34 sectors per track. SCSI and IDE drives have even more sectors per track.
Capacity	The formatted capacity of the drive is the number of heads times the number of cylinders times the number of sectors per track times 512 (bytes per sector).

Hard Disk Drive Types

Type	Cylinders	Heads	Write Precompensation	Landing Zone	Sectors	Capacity
1	306	4	128	305	17	10 MB
2	615	4	300	615	17	20 MB
3	615	6	300	615	17	31 MB
4	940	8	512	940	17	62 MB
5	940	6	512	940	17	47 MB
6	615	4	65535	615	17	20 MB
7	462	8	256	511	17	31 MB
8	733	5	65535	733	17	30 MB
9	900	15	65535	901	17	112 MB
10	820	3	65535	820	17	20 MB
11	855	5	65535	855	17	35 MB
12	855	7	65535	855	17	50 MB
13	306	8	128	319	17	20 MB
14	733	7	65535	733	17	43 MB
16	612	4	0	663	17	20 MB
17	977	5	300	977	17	41 MB
18	977	7	65535	977	17	57 MB
19	1024	7	512	1023	17	60 MB
20	733	5	300	732	17	30 MB
21	733	7	300	732	17	43 MB
22	733	5	300	733	17	30 MB
23	306	4	0	336	17	10 MB
24	925	7	0	925	17	54 MB
25	925	9	65535	925	17	69 MB
26	754	7	754	754	17	44 MB
27	754	11	65535	754	17	69 MB
28	699	7	256	699	17	41 MB
29	823	10	65535	823	17	68 MB
30	918	7	918	918	17	53 MB
31	1024	11	65535	1024	17	94 MB
32	1024	15	65535	1024	17	128 MB
33	1024	5	1024	1024	17	43 MB
34	612	2	128	612	17	10 MB
35	1024	9	65535	1024	17	77 MB
36	1024	8	512	1024	17	68 MB
37	615	8	128	615	17	41 MB
38	987	3	987	987	17	25 MB
39	987	7	987	987	17	57 MB
40	820	6	820	820	17	41 MB
41	977	5	977	977	17	41 MB
511	981	5	981	981	17	41 MB
43	830	7	512	830	17	48 MB
44	830	10	65535	830	17	69 MB
45	917	15	65535	918	17	114 MB
46	1224	15	65535	1223	17	152 MB

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Chapter 3: Advanced CMOS Setup

The Advanced CMOS Setup options included in the AMIBIOS Setup are described in this chapter. Select Advanced CMOS Setup from the AMIBIOS Setup main menu to display the Advanced Setup options.

Default Settings

Every option in AMIBIOS Setup contains two default values: a Fail-Safe default and the Optimal default value.

Default	Description
Optimal	The Optimal default values provide optimum performance settings for all devices and system features.
Fail-Safe	The Fail-Safe default settings consist of the safest set of parameters. Use them if the system is behaving erratically. They should always work but do not provide optimal system performance characteristics.

Quick Boot

Set this option to *Enabled* to instruct AMIBIOS to boot quickly when the computer is powered on. This option replaces the old **Above 1MB Memory Test** Advanced Setup option. The Optimal and Fail-Safe default settings are *Disabled.* The settings are:

Setting	Description
Disabled	AMIBIOS tests all system memory. AMIBIOS waits up to 40 seconds for a READY signal from the IDE hard disk drive. AMIBIOS waits for .5 seconds after sending a RESET signal to the IDE drive to allow the IDE drive time to get ready again. AMIBIOS checks for a <Del> key press and runs AMIBIOS Setup if the key has been pressed.
Enabled	AMIBIOS does not test system memory above 1 MB. AMIBIOS does not wait up to 40 seconds for a READY signal from the IDE hard disk drive. If a READY signal is not received immediately from the IDE drive, AMIBIOS does not configure that drive. AMIBIOS does not wait for .5 seconds after sending a RESET signal to the IDE drive to allow the IDE drive time to get ready again.

Pri Master ARMD Emulated As

This option specifies the type of emulation used for a non-disk device attached as the primary master IDE device. The settings are *Auto* (AMIBIOS automatically determines the proper emulation), *floppy,* or *hard disk*. The Optimal and Fail-safe default settings are *Auto*.

Pri Slave ARMD Emulated As

This option specifies the type of emulation used for a non-disk device attached as the primary slave IDE device. The settings are *Auto* (AMIBIOS automatically determines the proper emulation), *floppy,* or *hard disk*. The Optimal and Fail-safe default settings are *Auto*.

Sec Master ARMD Emulated As

This option specifies the type of emulation used for a non-disk device attached as the secondary master IDE device. The settings are *Auto* (AMIBIOS automatically determines the proper emulation), *floppy,* or *hard disk*. The Optimal and Fail-safe default settings are *Auto*.

Sec Slave ARMD Emulated As

This option specifies the type of emulation used for a non-disk device attached as the secondary slave IDE device. The settings are *Auto* (AMIBIOS automatically determines the proper emulation), *floppy,* or *hard disk*. The Optimal and Fail-safe default settings are *Auto*.

1st Boot Device

This option sets the type of device for the first boot drive that the AMIBIOS attempts to boot from after AMIBIOS POST completes. The Optimal and Fail-Safe default settings are *Floppy*.

2nd Boot Device

This option sets the type of device for the second boot drive that the AMIBIOS attempts to boot from after AMIBIOS POST completes. The Optimal and Fail-Safe default settings are *1st IDE-HDD.*

3rd Boot Device

This option sets the type of device for the third boot drive that the AMIBIOS attempts to boot from after AMIBIOS POST completes. The Optimal and Fail-Safe default settings are *ATAPI CDROM.*

Try Other Boot Devices

Set this option to *Yes* to instruct AMIBIOS to attempt to boot from any other drive in the system if it cannot find a boot drive among the drives specified in the **1st Boot Device, 2nd Boot Device,** and **3rd Boot Device.**

The settings are *Yes* or *No.* The Optimal and Fail-Safe default settings are *Yes*.

Initial Display Mode

This option specifies the initial display mode when the system boots. The Optimal and Fail-Safe default settings are *BIOS*. The settings are:

Setting	Description
BIOS	The messages that AMIBIOS displays before booting the system will appear on the system monitor.
Silent	The messages that AMIBIOS displays will not appear on the system monitor.

Display Mode At Add-On ROM Init

This option specifies the system display mode that is set at the time that AMIBIOS POST initializes an optional ROM. The Optimal and Fail-Safe default settings are *Force BIOS*. The settings are:

Setting	Description
Force BIOS	The display mode currently being used by AMIBIOS is used.
Keep Current	The current display mode is used.

Floppy Access Control

This option specifies the read/write access that is set when booting from a floppy drive. The settings are *Read/Write* or *Read-Only*. The Optimal and Fail-Safe default settings are *Read/Write.*

Hard Disk Access Control

This option specifies the read/write access that is set when booting from a hard disk drive. The settings are *Read/Write* or *Read-Only*. The Optimal and Fail-Safe default settings are *Read/Write.*

S.M.A.R.T. For Hard Disks

Set this option to *Enabled* to permit AMIBIOS to use the S.M.A.R.T. (System Management and Reporting Technologies) protocol for reporting server system information over a network. The settings are *Enabled* or *Disabled.* The Optimal default setting is *Enabled*. The Fail-Safe default setting is *Disabled.*

Boot Up Num Lock

Set this option to *Off* to turn the Num Lock key off when the computer is booted so you can use the arrow keys on both the numeric keypad and the keyboard. The settings are *On* or *Off.* The Optimal and Fail-Safe default settings are *On.*

Floppy Drive Swap

Set this option to *Enabled* to permit drives A: and B: to be swapped. The settings are *Enabled* or *Disabled.* The Optimal and Fail-Safe default settings are *Disabled.*

PS/2 Mouse Support

Set this option to *Enabled* to enable AMIBIOS support for a PS/2-type mouse. The settings are *Enabled* or *Disabled.* The Optimal and Fail-Safe default settings are *Enabled.*

Primary Display

This option configures the type of monitor attached to the computer. The settings are *Mono, CGA40x25, CGA80x25, VGA/EGA,* or *Absent*. The Optimal and Fail-Safe default settings are *VGA/EGA*.

Password Check

This option enables password checking every time the system boots or when you run AMIBIOS Setup. If *Always* is chosen, a user password prompt appears every time the computer is turned on. If *Setup* is chosen, the password prompt appears if AMIBIOS is executed. The Optimal and Fail-Safe defaults are *Setup.*

Boot To OS/2

Set this option to *Yes* if running the OS/2 operating system and using more than 64 MB of system memory on the motherboard. The settings are *Yes* or *No*. The Optimal and Fail-Safe default settings are *No.*

CPU Microcode Update

Set this option to *Enabled* to permit the CPU to be updated online at any time. The settings are *Enabled* or *Disabled*. The Optimal and Fail-Safe default settings are *Enabled.*

Internal Cache

This option sets the type of caching algorithm used by the L1 internal cache memory. The settings are *WriteBack, WriteThru*, or *Disabled*. The Optimal and Fail-Safe default settings are *WriteBack*.

External Cache

This option sets the type of caching algorithm used by the L2 secondary (external) cache memory. The settings are *WriteBack, WriteThru*, or *Disabled*. The Optimal default setting is *WriteBack*. The Fail-Safe default setting is *Disabled*.

System BIOS Cacheable

When set to *Enabled,* the contents of the F0000h system memory segment can be read from or written to cache memory. The contents of this memory segment are always copied from the BIOS ROM to system RAM for faster execution. The settings are *Enabled* or *Disabled.* The Optimal default setting is *Enabled*. The Fail-Safe default setting is *Disabled.*

C000,16K Shadow

C400,16K Shadow

These options specify how the 32KB of video ROM at C0000h is treated. The Optimal default setting is *Cached* and the Fail-Safe default settings is *Disabled.* The settings are:

Setting	Description
Disabled	The contents of the video ROM are not copied to RAM.
Enabled	The contents of the video ROM area from C0000h – C7FFFh are copied (shadowed) from ROM to RAM for faster execution.
Cached	The contents of the video ROM area from C0000h – C7FFFh are copied from ROM to RAM and can be written to or read from cache memory.

C800,16K Shadow

CC00,16K Shadow

D000,16K Shadow

D400,16K Shadow

D800, 16K Shadow

DC00,16K Shadow

These options enable shadowing of the contents of the ROM area named in the option. The ROM area not used by ISA adapter cards is allocated to PCI adapter cards. The Optimal and Fail-Safe default settings are *Disabled*. The settings are:

Setting	Description
Disabled	The contents of the adapter ROM are not copied to RAM.
Cached	The contents of the ROM area are copied from ROM to RAM and can be written to or read from cache memory.
Enabled	The contents of the ROM area are copied (shadowed) from ROM to RAM for faster execution.

Chapter 4: Advanced Chipset Setup

Choose Advanced Chipset Setup on the AMIBIOS Setup main menu. All Advanced Chipset Setup options are then displayed.

USB Function

Set this option to *Enabled* to enable USB (Universal Serial Bus) support. The settings are *Enabled* or *Disabled*. The Optimal and Fail-Safe default settings are *Enabled*.

USB Keyboard/Mouse Legacy Support

Set this option to *Enabled* to enable support for older keyboards and mouse devices if the **USB Function** option is set to *Enabled*. The settings are *Auto, Keyboard, Keyb+Mouse,* or *Disabled*. The Optimal and Fail-Safe default settings are *Auto.*

Port 64/60 Emulation

Use this option to *Enable* or *Disable* Port 64/60 Emulation. The Optimal and Fail-Safe default settings are *Disabled*.

SERR#

Set this option to *Enabled* to enable the SERR# signal on the bus. The settings are *Enabled* or *Disabled*. The Optimal and Fail-Safe default settings are *Disabled*.

PERR#

Set this option to *Enabled* to enable the PERR# signal on the bus. The settings are *Enabled* or *Disabled*. The Optimal and Fail-Safe default settings are *Disabled*.

DRAM Integrity Mode

This option sets the type of system memory checking. The Optimal and Fail-Safe default settings are *ECC Hardware*. The settings are:

Setting	Description
None	No error checking or error reporting is done.
ECC	Multibit errors are detected and reported as parity errors. Single-bit errors are corrected by the chipset. Corrected bits of data from memory are not written back to DRAM system memory.
ECC Hardware	Multibit errors are detected and reported as parity errors. Single-bit errors are corrected by the chipset and are written back to DRAM system memory. If a soft (correctable) memory error occurs, writing the fixed data back to DRAM system memory will resolve the problem. Most DRAM errors are soft errors. If a hard (uncorrectable) error occurs, writing the fixed data back to DRAM system memory does not solve the problem. In this case, the second time the error occurs in the same location, a Parity Error is reported, indicating an uncorrectable error.

DRAM Refresh Rate

This option specifies the interval between Refresh signals to DRAM system memory. The settings are *15.6µs* (microseconds), *31.2µs, 62.4µs, 124.8µs,* or *249.6µs*. The Optimal and Fail-Safe default settings are *15.6µs.*

Memory Hole

This option specifies the location of an area of memory that cannot be addressed on the ISA bus. The settings are *Disabled, 15MB–16MB,* or *512KB–640KB*. The Optimal and Fail-Safe default settings are *Disabled*.

SDRAM RAS# to CAS# Delay

This option specifies the length of the delay inserted between the RAS and CAS signals of the DRAM system memory access cycle if SDRAM is installed. The settings are *Auto* (AMIBIOS automatically determines the optimal delay), *2 SCLKs* or *3 SCLKs*. The Optimal default setting is *Auto* and the Fail-Safe default setting is *3SCLKs*.

SDRAM RAS Precharge

This option specifies the length of the RAS precharge part of the DRAM system memory access cycle when Synchronous DRAM system memory is installed in the computer. The settings are *Auto* (AMIBIOS automatically determines the optimal delay), *2 SCLKs,* or *3 SCLKs*. The Optimal default setting is *Auto* and the Fail-Safe default setting is *3SCLKs*.

Gated Clock

Set this option to *Enabled* to enable the gated clock. The settings are *Enabled* or *Disabled.* The Optimal and Fail-Safe default settings are *Enabled.*

Graphics Aperture Size

This option specifies the amount of system memory that can be used by the Accelerated Graphics Port (AGP). The settings are *4 MB, 8 MB, 16 MB, 32 MB, 64 MB, 128 MB,* or *256 MB*. The Optimal and Fail-Safe default settings are *64 MB.*

AGP Multi-Trans Timer (AGP Clocks)

This option sets the AGP multi-trans timer. The settings are in units of AGP Clocks. The settings are *32, 64, 96, 128, 160, 192,* or *224.* The Optimal and Fail-Safe default settings are *32.*

AGP Low-Priority Timer (AGP Clocks)

this option sets the AGP low-priority timer. The settings are in units of AGP clocks. The settings are *16, 32, 48, 64, 80, 96, 112, 128, 144, 176, 192, 208, 224,* or *240*. The Optimal and Fail-Safe settings are *16*.

8-Bit I/O Recovery Time

This option specifies the length of a delay inserted between consecutive 8-bit I/O operations. The settings are *Disabled, 1 SYCLK, 2 SYSCLKs, 3 SYSCLKs, 4 SYSCLKs, 5 SYSCLKs, 6 SYSCLKs, 7 SYSCLKs,* or *8 SYSCLKs.* The Optimal and Fail-Safe default settings are *Disabled.*

16-Bit I/O Recovery Time

This option specifies the length of a delay inserted between consecutive 16-bit I/O operations. The settings are *Disabled, 1 SYCLK, 2 SYSCLKs, 3 SYSCLKs,* or *4 SYSCLKs.* The Optimal and Fail-Safe default settings are *Disabled.*

TypeF DMA Buffer Control1

TypeF DMA Buffer Control2

These options specify the DMA channel where TypeF buffer control is implemented. The settings are *Disabled, Channel-0, Channel-1, Channel-2, Channel-3, Channel-5, Channel-6,* or *Channel-7.* The Optimal and Fail-Safe default settings are *Disabled.*

DMA-0 Type

DMA-1 Type

DMA-2 Type

DMA-3 Type

DMA-5 Type

DMA-6 Type

DMA-7 Type

These options specify the bus on which the specified DMA channel can be used. The settings are *PC/PCI, Distributed,* or *Normal ISA.* The Optimal and Fail-Safe default settings are *Normal ISA.*

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Chapter 5: PCI / Plug and Play Setup

Choose PCI/Plug and Play Setup from the AMIBIOS Setup screen to display the PCI and Plug and Play Setup options, described below.

Plug and Play Aware O/S

Set this option to *Yes* to inform AMIBIOS that the operating system can handle Plug and Play (PnP) devices. The settings are *No* or *Yes.* The Optimal and Fail-Safe default settings are *No.*

PCI Latency Timer (PCI Clocks)

This option specifies the latency timings (in PCI clocks) for PCI devices installed in the PCI expansion slots. The settings are *32, 64, 96, 128, 160, 192, 224,* or *248.* The Optimal and Fail-Safe default settings are *64.*

PCI VGA Palette Snoop

When this option is set to *Enabled,* multiple VGA devices operating on different buses can handle data from the CPU on each set of palette registers on every video device. Bit 5 of the command register in the PCI device configuration space is the VGA Palette Snoop bit (0 is disabled). For example, if there are two VGA devices in the computer (one PCI and one ISA) and the VGA Palette Snoop Bit is:

VGA Palette Snoop Bit	Action
Disabled	Data read and written by the CPU is only directed to the PCI VGA device's palette registers.
Enabled	Data read and written by the CPU is directed to both the PCI VGA device's palette registers and the ISA VGA device palette registers, permitting the palette registers of both devices to be identical.

This option must be set to *Enabled* if any ISA adapter card installed in the system requires VGA palette snooping. The Optimal and Fail-Safe default settings are *Disabled.*

Offboard PCI IDE Card

This option specifies whether an offboard PCI IDE controller adapter card is used in the computer. You must also specify the PCI expansion slot on the motherboard where the offboard PCI IDE controller card is installed. If an offboard PCI IDE controller is used, the motherboard onboard IDE controller is automatically disabled. The settings are *Disabled, Auto, Slot1, Slot2, Slot3, Slot4, Slot5,* or *Slot6.* If *Auto* is selected, AMIBIOS automatically determines the correct setting. The Optimal and Fail-Safe default settings are *Auto.* This option forces IRQ 14 and 15 to a PCI slot on the PCI local bus. This is necessary to support non-compliant PCI IDE adapter cards.

Offboard PCI IDE Primary IRQ

This option specifies the PCI interrupt used by the primary IDE channel on the offboard PCI IDE controller. The settings are *Disabled, Hardwired, INTA, INTB, INTC*, or *INTD*. The Optimal and Fail-Safe default settings are *Disabled.*

Offboard PCI IDE Secondary IRQ

This option specifies the PCI interrupt used by the secondary IDE channel on the offboard PCI IDE controller. The settings are *Disabled, Hardwired, INTA, INTB, INTC*, or *INTD*. The Optimal and Fail-Safe settings are *Disabled.*

DMA Channel 0

DMA Channel 1

DMA Channel 3

DMA Channel 5

DMA Channel 6

DMA Channel 7

These options allow you to specify the bus type used by each DMA channel. The settings are *PnP* or *ISA/EISA* . The Optimal and Fail-Safe default settings are *PnP.*

IRQ3

IRQ4

IRQ5

IRQ7

IRQ9

IRQ10

IRQ11

IRQ12

IRQ14

IRQ15

These options specify the bus on which the specified IRQ line is used. These options allow you to reserve IRQs for legacy ISA adapter cards. These options determine whether AMIBIOS should remove an IRQ from the pool of available IRQs passed to devices that are configurable by the system BIOS. The available IRQ pool is determined by reading the ESCD NVRAM. If more IRQs must be removed from the pool, the end user can use these options to reserve the IRQ by assigning an *ISA/EISA* setting to it. Onboard I/O is configured by AMIBIOS. All IRQs used by onboard I/O are configured as *PCI/PnP*. *IRQ12* only appears if the **Mouse Support** option in Advanced Setup is set to *Disabled.* If all IRQs are set to *ISA/EISA,* and *IRQ14* and *15* are allocated to the onboard PCI IDE, *IRQ9* will still be available for PCI and PnP devices. At least one IRQ must be available for PCI and PnP devices. The settings are *ISA/EISA* or *PCI/PnP.* The Optimal and Fail-Safe default settings are *PCI/PnP.*

Reserved Memory Size

This option specifies the size of the memory area reserved for legacy ISA adapter cards. The settings are *Disabled, 16K, 32K,* or *64K.* The Optimal and Fail-Safe default settings are *Disabled.*

Reserved Memory Address

This option specifies the beginning address (in hex) of the reserved memory area. The specified ROM memory area is reserved for use by legacy ISA adapter cards. This option does not appear if the **Reserved Memory Size** option is set to *Disabled.* The settings are *C0000, C4000, C8000, CC000, D0000, D4000, D8000,* or *DC000.* The Optimal and Fail-Safe default settings are *C8000.*

Chapter 6: Peripheral Setup

Peripheral Setup options are displayed by choosing Peripheral Setup from the AMIBIOS Setup main menu. All Peripheral Setup options are described here.

Onboard Video Controller

This option is used to either enable or disable the onboard video device. The options are *Enabled* or *Disabled.* The Optimal and Fail-Safe default settings are *Enabled.*

Onboard SCSI Controller

This option is used to either enable or disable the onboard SCSI controller. The options are *Enabled* or *Disabled.* The Optimal and Fail-Safe default settings are *Disabled.*

Onboard Network Controller

This option is used to either enable or disable the onboard network device. The options are *Enabled* or *Disabled.* The Optimal and Fail-Safe default settings are *Enabled.*

Onboard FDC

Set this option to *Enabled* to enable the floppy drive controller on the motherboard. The settings are *Auto* (AMIBIOS automatically determines if the floppy controller should be enabled)*, Enabled,* or *Disabled.* The Optimal and Fail-Safe default settings are *Auto.*

Onboard Serial Port1

This option specifies the base I/O port address of serial port 1. The settings are *Auto* (AMIBIOS automatically determines the correct base I/O port address), *Disabled, 3F8h, 2F8h, 2E8h,* or *3E8h.* The Optimal and Fail-Safe default settings are *Auto.*

Onboard Serial Port2

This option specifies the base I/O port address of serial port 2. The settings are *Auto* (AMIBIOS automatically determines the correct base I/O port address)*, Disabled, 3F8h, 2F8h, 2E8h,* or *3E8h.* The Optimal and Fail-Safe default settings are *Auto.*

Onboard Parallel Port

This option specifies the base I/O port address of the parallel port on the motherboard. The settings are *Auto, Disabled, 378h, 278h,* or *3BCh.* The Optimal and Fail-Safe default settings are *Auto*.

Parallel Port Mode

This option specifies the parallel port mode. The Optimal and Fail-Safe default settings are *ECP*. The settings are:

Setting	Description
Normal	The normal parallel port mode is used.
EPP	The parallel port can be used with devices that adhere to the Enhanced Parallel Port (EPP) specification. EPP uses the existing parallel port signals to provide asymmetric bidirectional data transfer driven by the host device.
ECP	The parallel port can be used with devices that adhere to the Extended Capabilities Port (ECP) specification. ECP uses the DMA protocol to achieve data transfer rates up to 2.5 Mb per second. ECP provides symmetric bidirectional communication.

EPP Version

This option specifies the Enhanced Parallel Port specification version number that is used in the system. This option only appears if the **Parallel Port Mode** option is set to *EPP*.

The settings are *1.7* or *1.9*. There are no Optimal and Fail-Safe default settings because the default setting for the **Parallel Port Mode** option is not *EPP*.

Parallel Port IRQ

This option specifies the IRQ used by the parallel port. The settings are *Auto, IRQ5,* or *IRQ 7*. The Optimal and Fail-Safe default settings are *Auto*.

Parallel Port DMA Channel

This option is only available if the setting for the **Parallel Port Mode** option is *ECP*. This option sets the DMA channel used by the parallel port. The settings are *Auto, DMA Channel 0, 1,* or *3*. The Optimal and Fail-Safe default settings are *Auto*.

Onboard IDE

This option specifies the IDE channel used by the onboard IDE controller. The settings are *Disabled, Primary,* or *Both*. The Optimal and Fail-Safe default settings are *Both*.

Appendix B

Watchdog Timer Code

```
/*********************************************************************/
// wdt.cpp - WatchDog Timer simple test utility
//                for Advent/ICS SB686BX
//
// VERSION: 1.00
// Date:          1/14/1999
//           (c) 1999 Advent Design
//
// History:
//          Ver. 1.00 - Initial version 1/14/1999
//
// Description:
//    This is a utility used to test the functionality of the watchdog
//    timer on the Advent/ICS SB686BX motherboard design.  When enabled,
//    The watchdog timer simply monitors an I/O port for activity counting
//    the time elapsed between I/O activity.  If no activity is detected
//    within a given timespan it first toggles an IRQ line (either 10 or 11)
//    when 1/2 of the time before reset occurs, then when the timespan
//    elapses, it will reset the computer.  This program demonstrates how to:
//
//       1.) Set up the timings of the WDT & disable the WDT
//       2.) Set the base address of the WDT
//       3.) Install & uninstall a handler for an IRQ
//
/*********************************************************************/

#include <stdlib.h>
#include <stdio.h>
#include <conio.h>
#include <ctype.h>
#include <dos.h>
#include <time.h>

// Macro used to refresh the watchdog timer
#define  REFRESH_WDT(baseaddr)          outp(baseaddr, 0)

#ifdef __cplusplus
    #define __CPPARGS ...
#else
    #define __CPPARGS
#endif

void interrupt WDT_isr(__CPPARGS);           // Handler for WDT interrupt
void interrupt (*old_isr)(__CPPARGS) = NULL; // Old interrupt handler pointer

void SetTimings(int);            // Routine to set reset & irq times
void DisableWDT();               // Routine to reset/disable timings
void SetIRQ(int);                // Routine to set the WDT handler
void RestoreIRQ(int);            // Routine to reset the IRQ handler
int io_delay();                  // Delay for sequential I/O operations

void SetTimingSignals(int);      // Routine to setup the WDT timing signals
```

```
void SetReg(int, unsigned char); // Routine to write to an AUX I/O regisger
void SetBaseAddress(unsigned);   // Routine to write the WDT's base address

void IrqTest(int, int, int);
void ResetTest(int, int);

int IRQCounter = 0;              // Global counter for the WDT ISR
int OldIRQCounter = 0;           //  and old counter to check changes

int hi_old_mask;                 // The old interrup masks for the
int lo_old_mask;                 //  slave (hi) and master (lo) PIC's
int Hi_Irq = 0;                  // Flag denoting the IRQ is hi (IRQ 8-15)


/*************************************************************/
// Main routine:  This displays the current values for the IRQ,
//    timing and base address and a menu to select the two watchdog
//    timer tests.  The tests include an IRQ and a reset test.
//    To test different timings, either change the hard-coded
//    variables iIRQ, iTiming, and iBaseAddr to your desired
//    values or add routines which do this during runtime.
/*************************************************************/
void main()
{
   char chChoice;

   int                           // Default settings defined here:
      iIRQ = 10,                 //  The IRQ to use (10 or 11 only for
SB686BX)
      iTiming = 2,               //  The Timing to use for the Watchdog timer
      iBaseAddr = 0x300;         //  The base I/O address to refresh the WDT

   do{
      clrscr();
      printf("WATCHDOG TIMER TEST PROGRAM:\n");
      printf("————————————————————\n\n");
      printf("  CURRENT SETTINGS:\n\n");
      printf("   %15s %d\n", "Timing :", iTiming);
      printf("   %15s %d\n", "IRQ :", iIRQ);
      printf("   %15s 0x%03X\n", "Base Address :", iBaseAddr);
      printf("  ————————————————\n\n");
      printf("  MENU:\n\n");
      printf("  1.) Run IRQ test\n");
      printf("  2.) Run reset test\n\n");
      printf("  Q.) Exit Program\n");
      printf("  ————————————————\n\n");
      printf("Choice: ");
      chChoice = getche();
      printf("\n");

      switch(chChoice)
      {
      case 'q': case 'Q':
         exit(0);
         break;

      case '1':
```

```
         IrqTest(iIRQ, iTiming, iBaseAddr);
         break;

      case '2':
         ResetTest(iTiming, iBaseAddr);
         break;

      default:
         clrscr();
         printf("\aInvalid entry: %c\n", chChoice);
      }

      printf("\nPress any key to continue:\n");
      getch();
   } while(1);

}

/*************************************************************/
// void interrupt WDT_isr()
//
// The Watchdog Timer interrupt service routine.  This simply
//    increments the IRQCounter which then may be in turn checked
//    against the OldIRQCounter for interrupt activity.
/*************************************************************/
void interrupt WDT_isr(__CPPARGS)
{
   IRQCounter++;                  // This simple ISR just increments a counter
                                  //  here is where application specific code
                                  //  should be placed to handle the watchdog
                                  //  timer interrupt.

   if(Hi_Irq)                     // Send an end of interrupt signal
   {                              //  to the programmable interrupt
      outportb(0xA0, 0x20);       //  controller (PIC).
      io_delay();
   }
   outportb(0x20, 0x20);          // non-specific end of interrup signal

   old_isr();
}



/*************************************************************/
// void IrqTest(int, int, int)
//
// Routine which tests the functionality of the watchdog timer
//  to generate an IRQ signal.  If the IRQ is being generated,
//  the user will see a spinning cursor display, if it is not
//  spinning, the IRQ is not being generated.  This test will
//  end when the user presses a key.
//
// INPUT: int Irq          - The a IRQ to test
//        int Timing       - The watchdog timing to use
//        int BaseAddress  - The watchdog timer base address
/*************************************************************/
```

```
void IrqTest(int Irq, int Timing, int BaseAddress)
{
   int error = 0;
   const char waitchars[5] = "|/-\\";

   clrscr();
   printf("IRQ TEST\n");
   printf("————————————————————\n\n");

   // Check if the Timing is set for disable
   //  if so prompt and return
   if( !((Timing < 3) && (Timing >= 0)) )
   {
      printf("Watchdog timer is disabled, test will not continue\n");
      return;
   }

   printf("PRESS ANY KEY TO QUIT.\n");

   SetBaseAddress(BaseAddress);
   SetIRQ(Irq);
   SetTimings(Timing);
      /* NOTE, as soon as we set the timings, we must */
      /* refresh the watchdog timer often so the      */
      /* computer will not reset.                     */
      /* Use the REFRESH_WDT() macro to do this       */

   REFRESH_WDT(BaseAddress);
   printf("\n-  Performing Test: ");
   // Test time below reset time
   // loop a certain number of times
   REFRESH_WDT(BaseAddress);
   int x = wherex(), y = wherey();
   clock_t start;

   REFRESH_WDT(BaseAddress);
   putch(waitchars[0]);
   REFRESH_WDT(BaseAddress);
   gotoxy(x,y);
   REFRESH_WDT(BaseAddress);

   for(int i = 1; ; i = (i == 3 ? 0: i+1) )
   {
      REFRESH_WDT(BaseAddress);           // Make sure to refresh the WDT
      OldIRQCounter = IRQCounter;         // Reset the old counter
      start = clock();                    // Reset the timeout time

      REFRESH_WDT(BaseAddress);

      while(IRQCounter == OldIRQCounter)  // Wait for an IRQ to occur
      {
         if(clock() - start > 1000)       // If we wait too long, timeout
         {                                //  error, the IRQ should have
            error = 1;                    //  occured by now.
            break;                        //
         }                                //
      }                                   //
```

```
      REFRESH_WDT(BaseAddress);
      if(!error)                    // Check if IRQ handler updated the
counter
      {                             //
         REFRESH_WDT(BaseAddress);  //
         putch(waitchars[i]);       // On the screen, a rotating cursor
         REFRESH_WDT(BaseAddress);  //  indicates that the IRQ is properly
         gotoxy(x,y);               //  toggling.
         REFRESH_WDT(BaseAddress);  //
      }

      REFRESH_WDT(BaseAddress);
      if (kbhit())
      {
         REFRESH_WDT(BaseAddress);
         getch(); // flush out the kbhit()
         REFRESH_WDT(BaseAddress);
         break;
      }
   }

   REFRESH_WDT(BaseAddress);        // Check whether an error occurred...
   if(!error)                       //
      printf("PASSED\n");           //
   else                             //  ... or not
   {                                //
      REFRESH_WDT(BaseAddress);     //
      printf("\aFAILED\n\n");
      printf("* Error: One or more IRQs did not occur in specified time\n");
      REFRESH_WDT(BaseAddress);
   }

   REFRESH_WDT(BaseAddress);        //
   DisableWDT();                    // Disable the WDT
   REFRESH_WDT(BaseAddress);        //  and
   RestoreIRQ(Irq);                 // Restore the IRQ to its original state
}



/*************************************************************/
// void ResetTest(int Timing, int BaseAddress)
//
// Routine which tests the ability of the watchdog timer to reset
//    the computer after the reset time has elapsed
//
// INPUT: int Timing - The timing to set the WDT to
//        int BaseAddress - Base address of the WDT
/*************************************************************/
void ResetTest(int Timing, int BaseAddress)
{
   char ch;

   clrscr();
   printf("RESET TEST\n");
```

```
   printf("————————————————————\n\n");

   // If timing is set to 3 (disabled) quit the test
   if(Timing == 3)
   {
      printf("Watchdog timer is disabled, test will not continue\n");
      return;
   }

   printf("WARNING:\n");
   printf("This should reset your system.\n");
   printf("Make sure to close all programs and files before this test.\n\n");

   printf("Continue with test? Y/N: ");      // Prompt the user of the danger
   int x = wherex(), y = wherey();           //  of this test & prompt
whether
   while(1)                                  //  to continue or not.
   {                                         //
      gotoxy(x, y);                          //
      ch = toupper(getch());                 //
      if( (ch == 'N') || (ch == 'Y') )       //
      {
         putch(ch);
         printf("\n");
         break;
      }
   }

   if( ch == 'N' )
      return;

   SetBaseAddress(BaseAddress);
   SetTimings(Timing);

   // Wait until reset should occur
   clock_t start = clock();
   while(clock() - start < 2000)
      ; // nothing

   // Computer should reset at this point
   DisableWDT();

   printf("\n\aError: Computer should have reset by now.\n");
}



/*************************************************************/
// void SetTimings(int)
//
// Routine which sets up the timings for the Watchdog timer
//
// INPUT: int Timing - Integer number between and including 0-3
//    which denotes the timing to set the watchdog timer
//
// Settings:   Timing   IRQ time (ms)  Reset time (ms)
//             0        250            500
```

```
//              1         50              100
//              2         5               10
//              3         Disabled        Disabled
//
// NOTE: Invalid timings disable the WDT
/*************************************************************/
void SetTimings(int Timing)
{
   if( (Timing >= 0) && (Timing <= 3) )
   {
      printf("\n Current watchdog timing settings:\n");
      printf(" %-10s %-10s\n", "Reset (ms)", "IRQ (ms)");

      switch(Timing)
      {
      case 0:                                   // Reset at 500 ms, IRQ 250 ms
         printf(" %-10d %-10d\n", 500, 250);
         break;

      case 1:                                   // Reset at 100 ms, IRQ at 50 ms
         printf(" %-10d %-10d\n", 250, 100);
         break;

      case 2:                                   // Reset at 10 ms, IRQ at 5 ms
         printf(" %-10d %-10d\n", 100, 50);
         break;

      default:                                  // Disabled
         printf(" %-10s %-10s\n", "Disabled", "Disabled");
      }

      SetTimingSignals(Timing);                 // Set the actual timing
      printf("\n");
   }
}


/*************************************************************/
// void DisableWDT()
//
// Routine to disable the watchdog timer
/*************************************************************/
void DisableWDT()
{
   SetTimingSignals(3);
   printf("Watch Dog Timer is now disabled\n");
}



/*************************************************************/
// void SetIRQ(int)
//
// Routine which sets up the master and slave programmable
//  interrupt controllers (8259A PIC).  Given an IRQ number,
//  this routine unmasks the interrupt lines to allow an IRQ
//  interrupt to occur.  To do so, make sure that the required
```

```
//  IRQ lines are dedicated to ISA and not PCI.  This also
//  installs an interrupt service routine for the watchdog timer
//
// INPUT: int irq - The IRQ number to attach an interrupt
//          service routine to.  Valid lines are 0-15 only.
//
// NOTE: This routine does no validity check on the input
/*************************************************************/
void SetIRQ(int irq)
{
   int
      lo_irq_mask = 0,
      hi_irq_mask = 0;

   disable();

   lo_old_mask = inportb(0x21);                    // Get the old interrupt
   io_delay();                                     //  masks
   hi_old_mask = inportb(0xA1);                    //

   if(irq > 7)                                     // IRQ's 8-15 are con-
nected
   {                                               //  to the slave PIC, so
      Hi_Irq = 1;                                  //  set up the slave and
                                                   //  master PICs.
      lo_irq_mask = 0xFB;                          // unmask master's IRQ 2
      hi_irq_mask = ~(1 <<(irq - 8));              // unmask slave's IRQ N

      old_isr = getvect(irq + 0x68);               // Save the old handler
      setvect(irq + 0x68, WDT_isr);                // Install the WDT handler

      outportb(0xA1, hi_old_mask & hi_irq_mask);   // Set new slave PIC mask
      io_delay();
      outportb(0xA0, 0x20);                        // send Non-specific EOI
   }
   else
   {
      lo_irq_mask = ~(1 << irq);                   // unmask master's IRQ N
      old_isr = getvect(irq + 0x08);               // Save the old handler
      setvect(irq + 0x08, WDT_isr);                // Install the WDT handler
   }

   outportb(0x21, lo_old_mask & lo_irq_mask);      // Set new master PIC mask
   io_delay();
   outportb(0x20, 0x20);                           // send Non-specific EOI

   enable();
}


/*************************************************************/
// void RestoreIRQ(int)
//
// Routine which restores the master and slave PIC's to their
//    original state, and re-installs the old interrupt service
//    routine for the given IRQ.
/*************************************************************/
```

```
void RestoreIRQ(int irq)
{
   disable();

   if(irq > 7)
   {
      Hi_Irq = 0;
      setvect(irq + 0x68, old_isr);
      outportb(0xA1, hi_old_mask);
      io_delay();
      outportb(0xA0, 0x20);
      io_delay();
   }
   else
      setvect(irq + 0x08, old_isr);

   outportb(0x21, lo_old_mask);
   io_delay();
   outportb(0x20, 0x20);

   enable();
}

/*************************************************************/
// int io_delay()
//
// Routine which is used in sequential I/O reads or writes
/*************************************************************/
int io_delay()
{
   int a = 0;
   a++;
   return a;
}


/*************************************************************/
// void SetTimingSignals(int)
//
// Routine which sets the signlas which set the timings for the
//    watchdog timer.  This routine basically sets the two general
//    purpose I/O pin signals of the SMC FDC37C932 Ultra I/O (TM)
//    device to some logical combination describing the watchdog
//    timer timing.
//
// INPUT: int timing - value to set the watchdog timer to.
//
// Settings:   Timing   IRQ time (ms)  Reset time (ms)
//             0        250            500
//             1        50             100
//             2        5              10
//             Default  Disabled       Disabled
/*************************************************************/
void SetTimingSignals(int timing)
{
   switch(timing)                      // Select a RST/IRQ timing
   {                                   //
```

```
   case 0:                              // Set the timing to 0
      SetReg(0xEC, 0);                  //
      SetReg(0xEB, 0);                  //
      break;                            //

   case 1:                              // Set the timing to 1
      SetReg(0xEC, 0);                  //
      SetReg(0xEB, 1);                  //
      break;                            //

   case 2:                              // Set the timing to 2
      SetReg(0xEC, 1);                  //
      SetReg(0xEB, 0);                  //
      break;                            //

   default:                             // Disable the watchdog timer
      SetReg(0xEC, 1);                  //
      SetReg(0xEB, 1);                  //
   }
}


/************************************************************/
// void SetReg(int, unsigned char)
//
// Routine which sets a specific auxiliary I/O register within
//    the SMC FDC37C932 Ultra I/O (TM) Controller.
/************************************************************/
void SetReg(int reg, unsigned char value)
{
   outp(0x03F0, 0x55);                      // Enter Config mode
   outp(0x03F0, 0x55);                      //

   outp(0x03F0, 0x07);                      // Select device 8,
   outp(0x03F1, 0x08);                      //  the auxiliary I/O device

   outp(0x03F0, reg);                       // Select the register and
   outp(0x03F1, value);                     // update its data

   outp(0x03F0, 0xAA);                      // Exit config mode
}


/************************************************************/
// void SetBaseAddress(unsigned BaseAddr)
//
// Routine which sets up the base address for the watchdog timer
//  such that after setup, when there is a read or write to
//  I/O port BaseAddr+0, the watchdog timer is restarted
/************************************************************/
void SetBaseAddress(unsigned BaseAddr)
{
      outportb(0x03F0, 0x55);                 // Enter Config
      outportb(0x03F0, 0x55);                 //

      outportb(0x03F0, 0x07);                 // Select Device 8 (AUX I/O)
      outportb(0x03F1, 0X08);                 //
```

```
      outportb(0x03F0, 0x062+1);                // Setup the actual base
address
      outportb(0x03F1, BaseAddr & 0x00ff);      //  Setup the low byte
      outportb(0x03F0, 0x062);                  //
      outportb(0x03F1, (BaseAddr >> 8));        //  Setup the high byte

      outportb(0x03F0, 0xE5);                   // Set bit3 to enable alt
output
      outportb(0x03F1, 0x08);                           //  function (GPW)
of GP 15

   outportb(0x03F0, 0x30);                  // Activate the device
   outportb(0x03F1, 0x01);                  //

      outportb(0x03F0, 0xF1);                   // Enable GPW (write strobe)
      outportb(0x03F1, 0x02);                   // Set bit0 to enable GPW ->
0x02

      outportb(0x03F0, 0xE4);                   // Set up GP 14 as a LOW
signal
      outportb(0x03F1, 0x00);                           //

      outportb(0x03F0, 0xAA);                   // Exit Config
}
```

Declaration of Conformity

(according to ISO/IEC Guide 22 and EN 45014)

6260 Sequence Drive
San Diego, CA 92121-4371
(800) 523-2320 / (858) 677-0877

declares that the product:

SB686BXC366	**SB686BXC400**	**SB686BXVC366**	**SB686BXVC400**
SB686BX350	**SB686BX400**	**SB686BX450**	**SB686BX3450**
SB686BX3500	**SB686BXV350**	**SB686BXV400**	**SB686BXV450**
SB686BXV3450	**SB686BXV3500**		

to which this declaration relates, meets the essential health and safety requirements and is in conformity with the relevant EU Directives listed below:

EU EMC Directive 89/336/EEC
EU Low Voltage Directive 73/23/EEC

using the relevant section of the following EU standards and other normative documents:

EN 50081-1:1992 Emissions, Generic Requirements.
-EN 55022 Measurement of radio interference characteristics of information technology equipment.

EN 50082-1:1992 Immunity, Generic Requirements.
-IEC 1000-4-2:1995 Immunity for radiated electromagnetic fields.
(Supersedes IEC 801-2)
-IEC 1000-4-3:1995 Immunity for radiated RF electromagnetic fields.
(Supersedes IEC 801-3)
-IEC 1000-4-4:1995 Immunity for AC and I/O lines, fast transients common mode.
(Supersedes IEC 801-4)

EN 60950:1992 Safety of Information Technology Equipment.

Mr. Jim Jameson
President and Chief Executive Officer

July 30, 1999
San Diego, CA

Information supporting this declaration is contained in the applicable Technical Construction file available from:

ICS Advent Europe
Ben Turner Industrial Road
Oving Road
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PO194ET, UK

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