Modular Computers®

CPCI Backplane Manual

PRODUCT DOCUMENTATION

PD08

CP3-BP11-P47

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CE

The product described in this manual is in compliance with all applied CE standards.

Revision History

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Rev. Index	Brief Description of Changes	Date of Issue
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Imprint

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This manual was realized by: **TPD/Engineering, PEP Modular Computers GmbH**.

1. Introduction

The specific product description provided with this product documentation is part of the PEP's CPCI Backplane manual. For further information, in particular regarding general details as well as safety and warranty statements, refer to the CPCI Backplane Manual, ID 24229.

2. CP3-BP11-P47 Positronic Type Backplane

The main features of the 3U, 11-slot, Positronic type backplane CP3-BP11-P47 are described in the table below.

Table 1: Distinctive Features of Backplane CP3-BP11-P47

Feature	Specification
Form Factor	3U
Size	283.0*128.7mm
Number of Slots	11
Bus Resolution	64 bits: right segment: slots 1 to 4 left segment: slot 1 32 bits: left segment: slots 2 to 7
Bus Frequency	66MHz: right segment: slots 1 to 4 33MHz: left segment: slots 1 to 7
Rear I/O Connectivity	Left segment: P2 on slots 2 to 7
Hot-Swap Capability	Yes
Power Supply Connector	Positronic PCIH47
Redundant Power Supply	—
Flexible Grounding Option	Yes
Fan Connector	Yes
MSD Connector	Yes
Power LED Connector	Yes
PS-ON Connector	Yes
Reset Function Connector	Yes

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The CP3-BP11-P47 backplane is divided into two segments (left and right) which are, except for a common power supply, electrically isolated from one another. When viewed from the front, the left segment is comprised of seven slots and the right segment of four slots. Logical slot numbering is from right to left beginning with one and going to eleven. The following table indicates the configuration of the individual slots.

Table 2: CP3-BP11-P47 Backplane Configuration (no bridge)

SEG	LOG SLOT NR	SLOT TYPE	BUS WIDTH		BUS FREQ		BUS EXT	RIO	REMARKS
			32-BIT	64-BIT	33 MHz	66 MHz			
RIGHT	1	SC		X	X	X	X		System Master only
	2	P		X	X	X			
	3	P		X	X	X			
	4	P		X	X	X			
LEFT	1	SC		X	X		X		System Master only
	2	P	X		X			X	
	3	P	X		X			X	
	4	P	X		X			X	
	5	P	X		X			X	
	6	P	X		X			X	
	7	P	X		X			X	

Legend: SLOT TYPE: SC = system controller; P = peripheral

BUS FREQ: indicates capability of backplane

BUS EXT: slot can be configured for extension of CPCI-bus

RIO: indicates that slot has Rear I/O capability

The design of this backplane coupled with several bus extension possibilities allows for three different modes of operation.

1. Standard operation: two completely separate CompactPCI systems on one backplane (one 7 slot system and one 4 slot system)
2. Single system master operation: one 11 slot CompactPCI system (achieved through the use of a transparent bridge)
3. Dual system master operation: two separate CompactPCI systems communicating directly with one another via the backplane (achieved through the use of a non-transparent bridge)

Further information concerning the operation modes and the bridges employed is provided in chapters 6 and 7.

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3. Board Layouts

Figure 1: CP3-BP11-P47 Board Layout (Front)

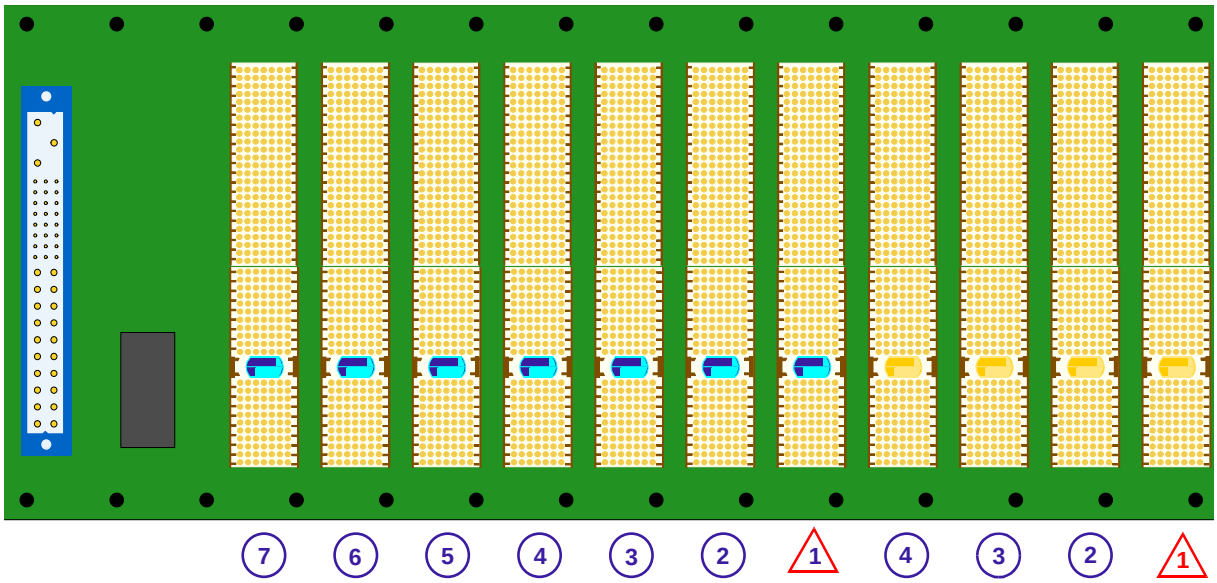
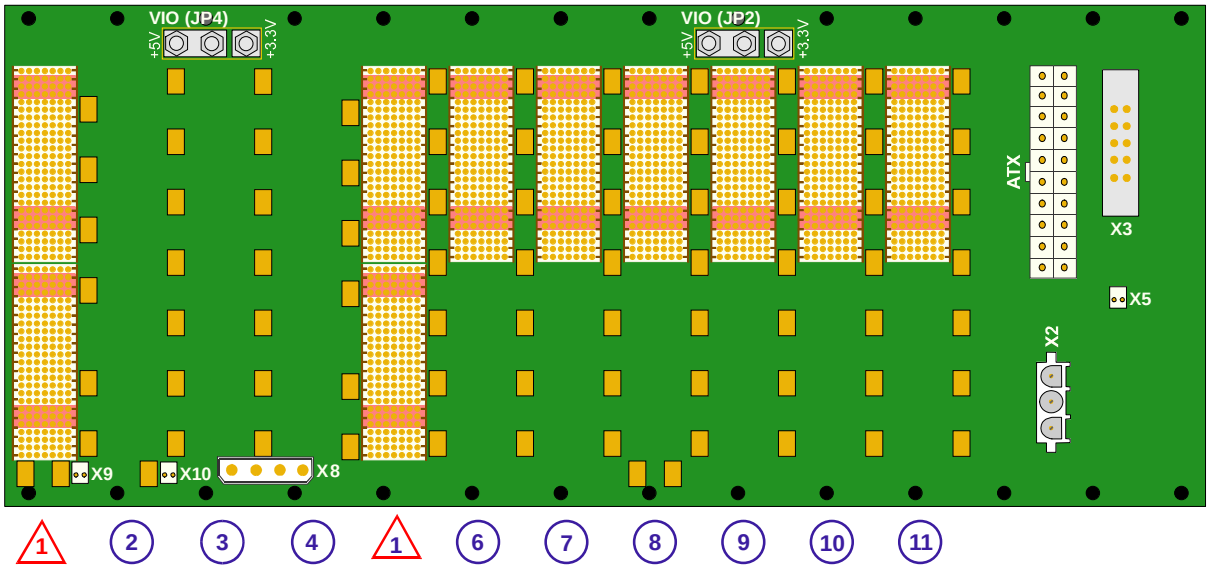


Figure 2: CP3-BP11-P47 Board Layout (Reverse)



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4. Signalling Environment

4.1 V(I/O) Setting

For each backplane segment there is block of three high-current terminals (designated as V(I/O)) for connecting V(I/O) to either the +5V or +3.3V power supply. V(I/O) must be connected either to the +5V or the +3.3V input power. It is the responsibility of the system integrator to ensure that the required signalling voltage is implemented and that the backplane P1 connector coding corresponds to the implemented signalling voltage.



Warning!

Using both 3.3V and 5V boards within the same backplane segment may result in damage to your equipment. Please note that the presence of only one 5V board determines a 5V signalling environment. The default setting is 5V.

4.2 P1 Connector Coding for V(I/O)

The CompactPCI Specification foresees coding of the P1 connector to correspond to the signalling environment of the PCI bus. For this reason, only boards with universal or the corresponding coding can be physically inserted into the backplane. PEP's factory default setting for the left backplane segment V(I/O) is +5V and male, 1567 code, brilliant blue coding keys are used. For the right backplane segment, V(I/O) is +3.3V and male, 3456 code, cadmium yellow coding keys are used.



Warning!

Using boards with an inadequate signalling voltage may result in damage to your equipment. Therefore, when changing the signalling environment from 5V to 3.3V or vice versa, it is mandatory that proper coding keys are used (refer to chapter 3 of the CPCI Backplane Manual, ID 24229, for details).

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5. Interfaces

5.1 Line Connector

The power supply to the backplane is connected by means of the 3-pole Mate-N-Lok connector marked ”X2” on the reverse side of the backplane.

Figure 3: Orientation and Pinouts of CP3-BP11-P47 Connector X2

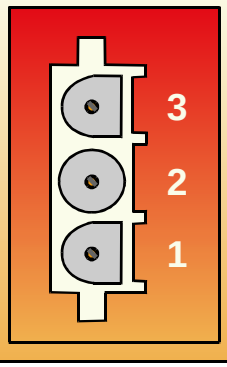


Table 3: Pinouts of CP3-BP11-P47 Connector X2

Pin	Function
1	L or +DC
2	N or -DC
3	PE

5.2 ATX Power Supply Connector

The main input power voltage is fed directly to the ATX power supply unit without any throughput via a backplane power supply connector. The power supply unit’s V1 ... V4 output power is distributed to the backplane by means of the 20-contact, male, Molex Mini-Fit Junior Connector ”ATX”.

Figure 4: Orientation and Pinouts of CP3-BP11-P47 ATX Connector

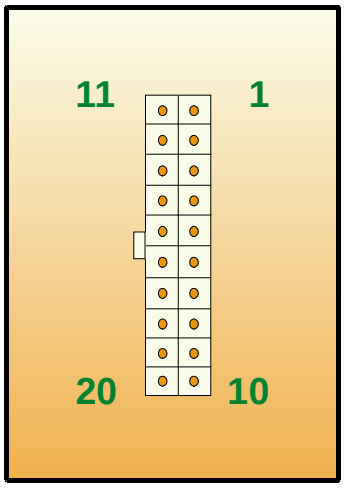


Table 4: ATX Connector Pinouts

Pin	Function	Pin	Function
1	+3.3V	11	+3.3V
2	+3.3V	12	-12V
3	GND	13	GND
4	+5V	14	PS_ON#
5	GND	15	GND
6	+5V	16	GND
7	GND	17	GND
8	PWR_OK	18	-5V
9	+5 VSB	19	+5V
10	+12V	20	+5V

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5.3 Positronic PCIH47 Type Power Supply Connector

The input voltages to the power supply unit and the V1 ... V4 output voltages from the power supply unit to the backplane are connected via a 47-position, Positronic PCIH47, female power supply connector.

Figure 5: Orientation and Pinouts of CP3-BP11-P47 Positronic Type Power Supply Connector

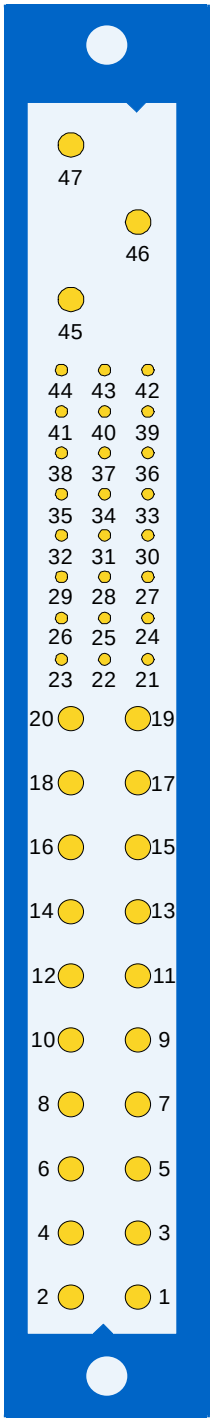


Table 5: Positronic 47-Pin Connector Pinout

PIN	SIGNAL NAME	DESCRIPTION	PIN	SIGNAL NAME	DESCRIPTION
1 - 4	V1	V1 Output (+5v)	32	NC	Not Connected
5 - 12	RTN	V1 and V2 Return	33	V2 SENSE	V2 Remote Sense
13 - 18	V2	V2 Output (+3.3v)	34	S RTN	Sense Return
19	RTN	V3 Return	35	V1 SHARE	V1 Current Share
20	V3	V3 Output (+12v)	36	V3 SENSE	V3 Remote Sense
21	V4	V4 Output (-12v)	37	NC	Not Connected
22	RTN	Signal Return	38	DEG#	Degrade Signal
23	RESERVED	Reserved	39	INH#	Inhibit
24	RTN	V4 Return	40	NC	Not Connected
25	NC	Not Connected	41	V2 SHARE	V2 Current Share
26	RESERVED	Reserved	42	FAL#	Fail Signal
27	EN#	Enable	43	NC	Not Connected
28	NC	Not Connected	44	V3 SHARE	V3 Current Share
29	NC	Not Connected	45	CGND	Chassis Ground
30	V1SENSE	V1 Remote Sense	46	ACN	Ac Input Neutral
31	NC	Not Connected	47	ACL	Ac Input Line

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5.4 Fan Connector

The backplane is equipped with the lockable Molex male connector X9 for the connection of fans to the 12V power supply of the bus.

Figure 6: Orientation and Pinouts of CP3-BP11-P47 Connector X9

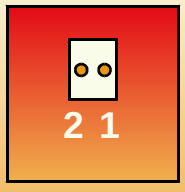


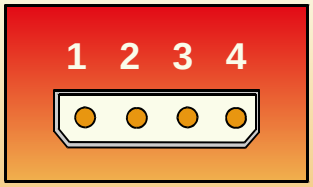
Table 6: Pinouts of CP3-BP11-P47 Connector X9

Pin	Function
1	GND
2	+12V

5.5 MSD Connectors

One 4-pole Molex male connector is equipped on the backplane for the connection of mass storage devices (drives) to the +5V/+12V power supply of the bus.

Figure 7: Orientation and Pinouts of CP3-BP11-P47 MSD Connector X8



Legend:

This connector is available optionally.

Table 7: Pinouts of CP3-BP11-P47 MSD Connector X8

Pin	Function
1	+12V
2	GND
3	GND
4	+5V

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5.6 Auxiliary Signal Connector

The connection of the auxiliary signals is accomplished by means of the 10-pole LPV male connector X3.

Figure 8: Orientation and Pinouts of CP3-BP11-P47 Connector X3

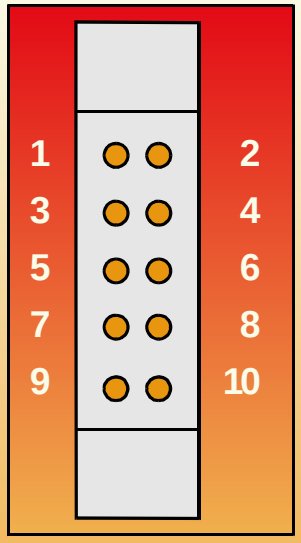


Table 8: Pinouts of CP3-BP11-P47 Connector X3

Pin	Function
1	GND
2	EN# or PS_ON#
3	GND
4	INH#
5	DEG#
6	FAL#
7	GND
8	PRST#
9	GND
10	+5V

5.7 Power Supply Remote Enabling

The Molex male connector X5 has a double function. It can be used as a power supply remote enable connector or, if bridged, as a wire jumper. If used as a connector, X5 offers the possibility of remote ON/OFF via an external power supply enable switch.

Figure 9: Orientation and Pinouts of CP3-BP11-P47 Connector X5

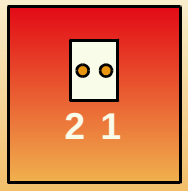


Table 9: Pinouts of CP3-BP11-P47 Connector X5

Pin	Function
1	GND
2	PS_ON# or EN#

If X5 is used as a wire jumper, the remote ON/OFF commuting is accomplished by closing X5. No external power supply enable switch is required in this case.

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5.8 Power LED Connector

The 2-pole, 2.54 mm, pin-row male connector X10 offers the possibility of connecting a ”Power ON/OFF” LED. The connector pinouts are identical to those of PC connectors customary in trade. Voltage is supplied by the 5V line.

Note...

By default, the power supply line is equipped with a resistor that is serially connected to the LED. Such a resistor is necessary to protect the LED from possible overcurrents.

Figure 10: Orientation and Pinouts of CP3-BP11-P47 Connector X10

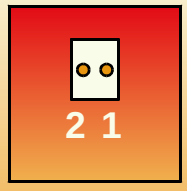


Table 10: Pinouts of CP3-BP11-P47 Connector X10

Pin	Function
1	GND
2	+ 5V

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6. Operational Modes

As indicated in chapter 2, the CP3-BP11-P47 backplane provides the possibility to be configured for three different operational modes.

- Standard operation
- Single system master operation
- Dual system master operation

The standard operation mode is the basic configuration of the CP3-BP11-P47 backplane and requires no additional hardware to be achieved. The other two modes require additional hardware in order to be implemented. For single system master operation, a PCI-to-PCI transparent bridge is required. For dual sytem master operation, a PCI-to-PCI non-transparent bridge is required.

6.1 Standard Operation Mode

The standard operation mode allows for the implementation of two independent CompactPCI systems on one backplane. The left backplane segment is comprised of seven slots (one system master and six peripheral slots) whereby the peripheral slots all have rear I/O capability. The right backplane segment is comprised of four slots (one system master and three peripheral slots) with no rear I/O capability. Both backplane segments have their own VIO signalling voltage capability which allows them to be configured independently.

6.2 Single System Master Operation

To implement this operational mode, a special adapter board comprised of a standard PCI-to-PCI transparent bridge and associated hardware is required. This adapter, the CP-BP-BRT1, bridges the right and left backplane segments (slot 1 to slot 5) creating a single CompactPCI system with a total of ten peripheral slots. No driver software is required for this mode of operation.

6.3 Dual System Master Operation

To implement this operational mode, a special adapter board comprised of a non-transparent PCI-to-PCI bridge and associated hardware is required. This adapter, the CP-BP-BRN1, bridges the right and left backplane segments (slot 1 to slot 5) creating the basis for a dual CompactPCI system with two system masters communicating with each other via the non-transparent PCI-to-PCI bridge. In this configuration the bridge primary side is routed to slot 1 and the secondary side to slot 5. In order to operate in this mode, each system master must have its own appropriate driver software which must take into consideration the physical location of the system master with respects to the primary and secondary side of the bridge.



Note...

The non-transparent bridge does not transmit the system clock frequency of a system master controller to the second system slot. Therefore, no peripheral master controllers may be used in the system slots 1 and 5.

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Figure 11: Schematic Overview of CP3-BP11-P47 Backplane and Bridge Modules

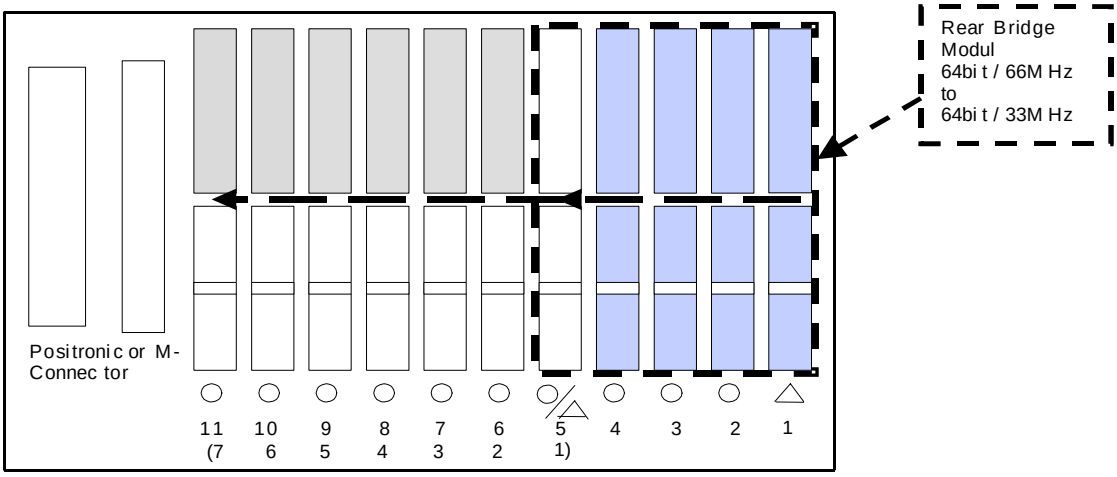


Table 11: Bus Segmentation and Slot Assignment on CP3-BP11-P47 Backplane

Slots	PCI Bus	Function
1	66MHz, 64-bit	System slot
2-4	66MHz, 64-bit	Peripheral slots (no rear I/O)
5 (1)	33MHz, 64-bit	System slot without bridge module or with CP-BP-BRN1 Peripheral slot with CP-BP-BRT1
6-11 (2-7)	33MHz, 32-bit	Peripheral slots (rear I/O on P2)

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7. Bridge Adapters

There are two different types of PCI-to-PCI bridging adapters available for the CP3-BP11-P47 backplane:

- CP-BP-BRT1: a transparent bridge
- CP-BP-BRN1: a non-transparent bridge

Both of these adapters are installed on the rear side of the backplane and bridge slots 1 and 5.

The bridge adapter CP-BP-BRT1 is used to create a single CompactPCI system backplane of eleven slots (7 and 4).

The bridge adapter CP-BP-BRN1 makes it possible for both backplane segments to communicate with one another and at the same time be operated independently.

7.1 CP-BP-BRT1 Transparent Bridge Adapter

The CP-BP-BRT1 transparent bridge adapter which is designed around the Intel© DEC21154 PCI-to-PCI chip is fully compliant with “PCI Local Bus Specification, Revision 2.1”. It is this capability which provides PCI bus extension from the right segment to the left segment of the CP-BP11-P47 backplane. The table below indicates the backplane configuration with this adapter installed.

Table 12: CP3-BP11-P47 Backplane Configuration With CP-BP-BRT1 Installed

SEG	LOG SLOT NR	SLOT TYPE	BUS WIDTH		BUS FREQ		BUS EXT	RIO	REMARKS
			32-BIT	64-BIT	33 MHz	66 MHz			
RIGHT	1	SC		X	X	X	X		System Master
	2	P		X	X	X			
	3	P		X	X	X			
	4	P		X	X	X			
LEFT	5	P		X	X		X		No peripheral master allowed
	6	P	X		X			X	
	7	P	X		X			X	
	8	P	X		X			X	
	9	P	X		X			X	
	10	P	X		X			X	
	11	P	X		X			X	

Legend: SLOT TYPE: SC = system controller; P = peripheral
BUS FREQ: indicates capability of backplane
BUS EXT: slot can be configured for extension of CPCI-bus
RIO: indicates that slot has Rear I/O capability

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7.2 CP-BP-BRN1 Non-Transparent Bridge Adapter

The CP-BP-BRN1 non-transparent bridge adapter which is designed around the Intel© DEC21554 PCI-to-PCI chip is fully compliant with “PCI Local Bus Specification, Revision 2.1”. It is this capability which makes it possible to have communications between the system master slots on this backplane. The table below indicates the backplane configuration with this adapter installed.

Table 13: CP3-BP11-P47 Backplane Configuration With CP-BP-BRN1 Installed

SEG	LOG SLOT NR	SLOT TYPE	BUS WIDTH		BUS FREQ		BUS EXT	RIO	REMARKS
			32-BIT	64-BIT	33 MHz	66 MHz			
RIGHT	1	SC		X	X	X	X		System Master
	2	P		X	X	X			
	3	P		X	X	X			
	4	P		X	X	X			
LEFT	1	SC		X	X		X		System Master
	2	P	X		X			X	
	3	P	X		X			X	
	4	P	X		X			X	
	5	P	X		X			X	
	6	P	X		X			X	
	7	P	X		X			X	

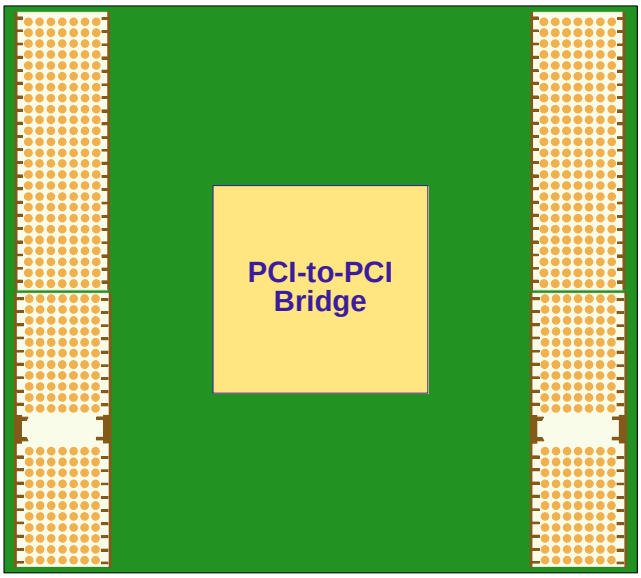
Legend: SLOT TYPE: SC = system controller; P = peripheral
BUS FREQ: indicates capability of backplane
BUS EXT: slot can be configured for extension of CPCI-bus
RIO: indicates that slot has Rear I/O capability

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7.3 Board Layout

The following board layout applies both to the CP-BP-BRT1 transparent and to the CP-BP-BRN1 non-transparent bridge module.

Figure 12: Board Layout of CP3-BP11-P47 Bridge Modules (Reverse)



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