AM4001

Processor AMC Module based on Intel® Pentium® M Processor and Intel® E7320 Chipset

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User Guide

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CE Conformity

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Caution, Electric Shock!

This symbol and title warn of hazards due to electrical shocks (> 60V) when touching products or parts of them. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your material.

Please refer also to the section “High Voltage Safety Instructions” on the following page.



Warning, ESD Sensitive Device!

This symbol and title inform that electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Please read also the section “Special Handling and Unpacking Instructions” on the following page.



Warning!

This symbol and title emphasize points which, if not fully understood and taken into consideration by the reader, may endanger your health and/or result in damage to your material.



Note ...

This symbol and title emphasize aspects the reader should read through carefully for his or her own advantage.

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Caution, Electric Shock!

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Serious electrical shock hazards can exist during all installation, repair and maintenance operations with this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing work.

Special Handling and Unpacking Instructions



ESD Sensitive Device!

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Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

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This device should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This applies also to the operational temperature range of the specific board version, which must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, please follow only the instructions supplied by the present manual.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the board, please re-pack it as nearly as possible in the manner in which it was delivered.

Special care is necessary when handling or unpacking the product. Please consult the special handling and unpacking instruction on the previous page of this manual.

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Chapter 1

Introduction

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1. Introduction

1.1 AdvancedTCA System Overview

The Advanced Mezzanine Card (AMC) described in this manual operates with the Advanced Telecom Computing Architecture (AdvancedTCA® or ATCA) defined by the *PCI Industrial Computer Manufacturers Group (PICMG).* The main advantages of AdvancedTCA include high throughput, multi-protocol support, high-power capability, hot swappability, high scalability, and integrated system management. For further information regarding the AdvancedTCA standards and their use, please consult the complete AdvancedTCA specification or visit the *PICMG* web site.

The Kontron Modular Computers AMC cards can be integrated not only on Kontron ATCA carrier boards, but also on a variety of AMC-supporting ATCA and proprietary carrier boards providing them with superior processing power and maximum design options. To learn more about the outstanding features and advantages of Kontron ATCA carrier boards, please contact Kontron Modular Computers or visit the Kontron web site.

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1.2 Board Overview

1.2.1 Board Introduction

The AM4001 is a highly integrated CPU board implemented as a single-width, half-height, full-height, and extended full-height processor Advanced Mezzanine Card (AMC) module. The design is based on the low-power, high-performance Intel® Celeron® M and Pentium® M processors combined with the high-performance E7320 and 6300ESB server-class chipsets.

The board supports Intel® Celeron® M and Pentium® M processor versions in 90 nm technology and 479 µFCBGA package with frequencies ranging from 1.0 GHz up to 2.0 GHz providing front side bus speeds of 400 MHz and 533 MHz. The processor is soldered on the AM4001 and cannot be exchanged.

The board includes a dedicated memory module for up to 4 GB registered Double Data Rate (DDR2) memory with Error Checking and Correcting (ECC) running at 400 MHz. A dual Gigabit Ethernet controller utilizing a x4 lane PCI Express interconnection to the E7320 chipset ensures maximum data throughput between processor and memory. The AM4001 further provides up to 1GB Flash memory via an onboard CompactFlash controller.

The AM4001 has full hot swap capability, which enables the board to be replaced, monitored and controlled without having to shut down the ATCA carrier board or the system. A dedicated Module Management Controller (MMC) is used to manage the board and support a defined subset of Intelligent Platform Management Interface (IPMI) commands and PICMG (ATCA/AMC) command extensions, which enables operators to detect and eliminate faults faster at module level. This includes monitoring several onboard temperature conditions, board voltages and the power supply status, managing hot swap operations, rebooting the board, etc. All in all, IPMI enhances the board's availability and reliability while reducing the operating costs and the mean-time-to-repair.

As a "headless" AMC design (no onboard graphics controller), the AM4001 supports two USB interfaces to the front, namely one USB 2.0 host interface and one USB 1.1 serial-to-USB interface, and a variety of high-speed interconnect topologies to the system, such as Dual Gigabit SerDes connection and Dual Serial ATA storage interface in the common options region of the AMC port mapping, and x4 PCI Express in the fat pipes of the AMC port mapping.

Optimized for high-performance, packet-based telecom systems, the AM4001 is targeted towards, but not limited to the telecom market application such as radio network controllers, storage control, routing and switching. The AM4001 also fits into all applications situated in industrial environments, including I/O intensive applications. The careful design and selection of high temperature resistant components ensure a high product availability. This, together with a high level of scalability, reliability, and stability, make this state-of-the-art product a perfect core technology for long-life embedded applications.

The board is offered with the generic Linux Board Support Package which supports various Linux distributions including the Carrier Grade Linux (CGL) operating system. Please contact Kontron Modular Computers for further information concerning other operating systems.

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1.2.2 Board-Specific Information

Due to the outstanding features of the AM4001, such as superior processing power and flexible interconnect topologies, this AMC board provides a highly scalable solution not only for a wide range of telecom and data network applications, but also for several highly integrated industrial environment applications with solid mechanical interfacing.

Some of the AM4001's outstanding features are:

- Intel® Celeron® M and Pentium® M microprocessors up to 2.0 GHz in a 479 µFCBGA package
- Up to 2048 kB L2 cache on-die, running at CPU speed
- 400 MHz and 533 MHz processor system bus
- E7320 and 6300ESB chipsets
- Dedicated memory module for up to 4 GB DDR2 SDRAM memory running at 400 MHz (PC3200)
- AMC interconnection
  - Dual Gigabit SerDes connection in the common options region of the AMC port mapping
  - Dual SATA storage interface in the common options region of AMC port mapping
  - x4 PCI Express in the fat pipes region of the AMC port mapping (operates only as a root complex controller)
- Full hot swap support
- Dual Gigabit Ethernet controller (82571EB-style)
- CompactFlash controller for up to 1GB NAND Flash memory
- Two front Mini USB connectors
  - One USB 2.0 host port
  - One USB 1.1 serial-to-USB port
- Console redirection via a serial-to-USB converter
- Two redundant onboard FWH Flash chips for BIOS (2x1MB)
- Dedicated IPMI Module Management Controller with redundant Firmware Flash (2x128kB)
- Thermal management
- Watchdog timer
- JTAG interface for debugging and manufacturing
- Standard temperature range: -5°C to + 55°C
- Passive heat sink solution
- Single-width, half-height, full-height and extended full-height AMC module
- Designed to be compliant with the following specifications:
  - PICMG AMC.0, Advanced Mezzanine Card Specification R1.0
  - PICMG AMC.1, PCI Express and Advanced Switching R1.0
  - PICMG AMC.2, Gigabit Ethernet R1.0
  - PICMG AMC.3, Storage Interfaces R1.0
- AMI BIOS

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1.3 System Relevant Information

The following system relevant information is general in nature but should still be considered when developing applications using the AM4001.

Table 1-1: System Relevant Information

SUBJECT	INFORMATION

Hardware Requirements	The AM4001 can be installed on any AMC-supporting carrier board with the following AMC connector port mapping:
	• Common options region port 0-1
	  • Two Gigabit Ethernet SerDes (1000BASE-BX) ports
	• Common options region port 2-3
	  • Two Serial ATA 150 ports
	• Fat pipes region port 4-7
	  • One x4 PCI Express interface
	For further information on the AMC interconnection, refer to section 2.4, “AMC Interconnection”.

PCI Express Configuration	The AM4001 only supports the PCI Express root complex configuration; the non-transparent bridge functionality is not supported.
Operating Systems	The AM4001 is offered with the generic Linux Board Support Package which supports various Linux distributions including the Carrier Grade Linux (CGL) operating system. Please contact Kontron Modular Computers for further information concerning other operating systems.

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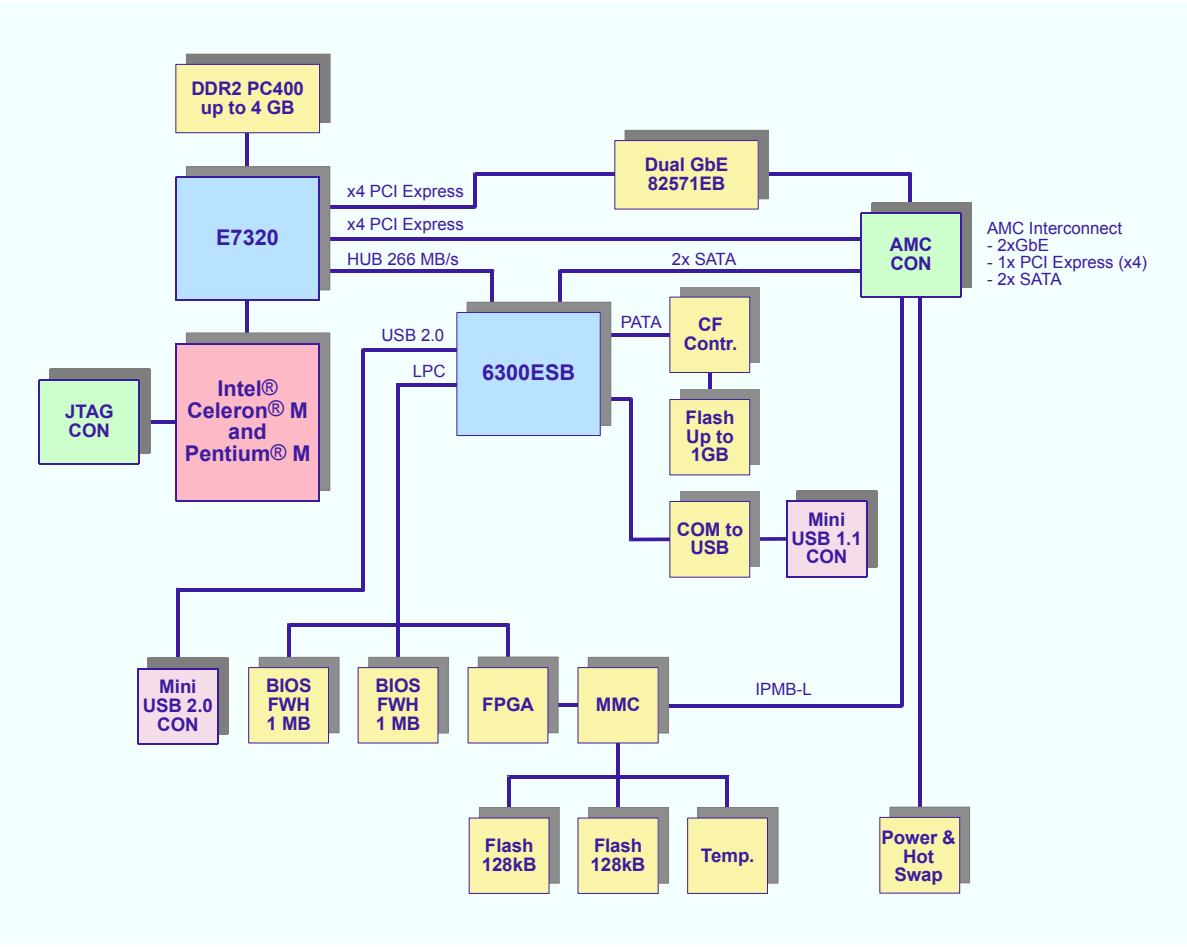
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1.4 Board Diagrams

The following diagrams provide additional information concerning board functionality and component layout.

1.4.1 Functional Block Diagram

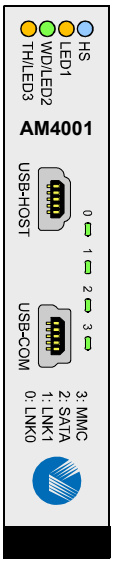
Figure 1-1: AM4001 Functional Block Diagram



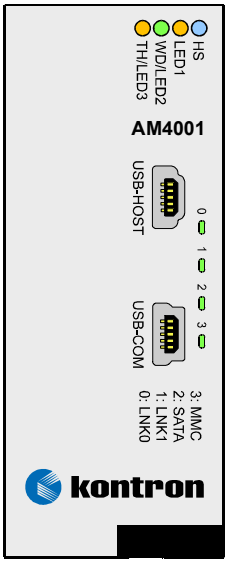
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1.4.2 Front Panels

Figure 1-2: Half-Height, Full-Height, and Extended Full-Height Front Panels



Half-Height Front Panel



Full-Height and Extended Full-Height Front Panel

LEGEND:

AMC LEDs

- HS (blue): The hot swap indicator provides basic feedback to the user on the hot swap state of the module. The HS LED states are off, short blink, long blink, and on.
- LED1 (amber): MMC control and debug LED
- WD/LED2 (green): Watchdog or General Purpose; when lit during boot-up, it indicates a PCI reset is active
- TH/LED3 (amber): Overtemperature Status or General Purpose; when lit during boot-up, it indicates a power failure

Module LEDs

- MLED0 (green): Ethernet port 0 link signal status or General Purpose / BIOS POST code LED.
- MLED1 (green): Ethernet port 1 link signal status or General Purpose / BIOS POST code LED.
- MLED2 (green): SATA and CompactFlash activity status or General Purpose / BIOS POST code LED.
- MLED3 (green): MMC Debug or General Purpose / BIOS POST code LED.

For further information on the LEDs used on the AM4001, refer to section 2.3.1, “Front Panel LEDs”.

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1.4.3 Board Layouts

Figure 1-3: AM4001 Board Layout (Top View)

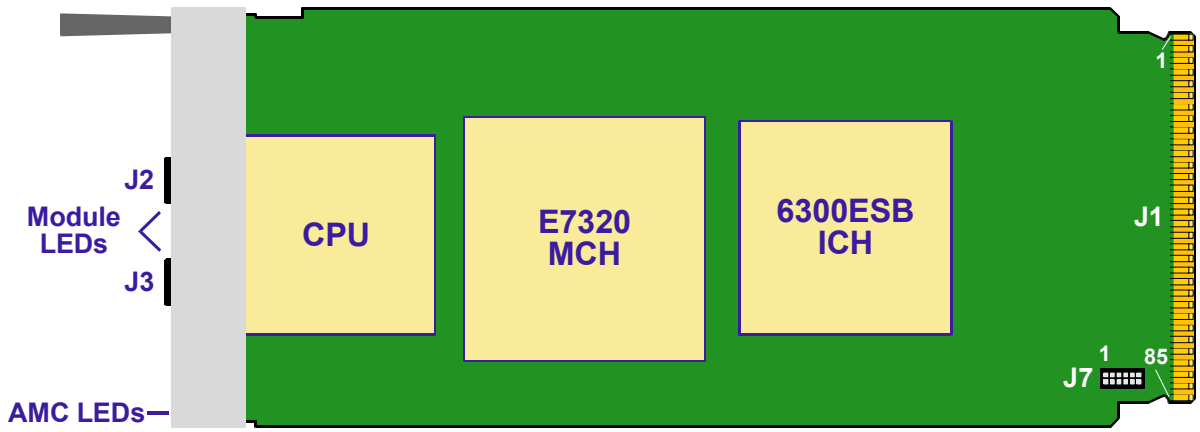
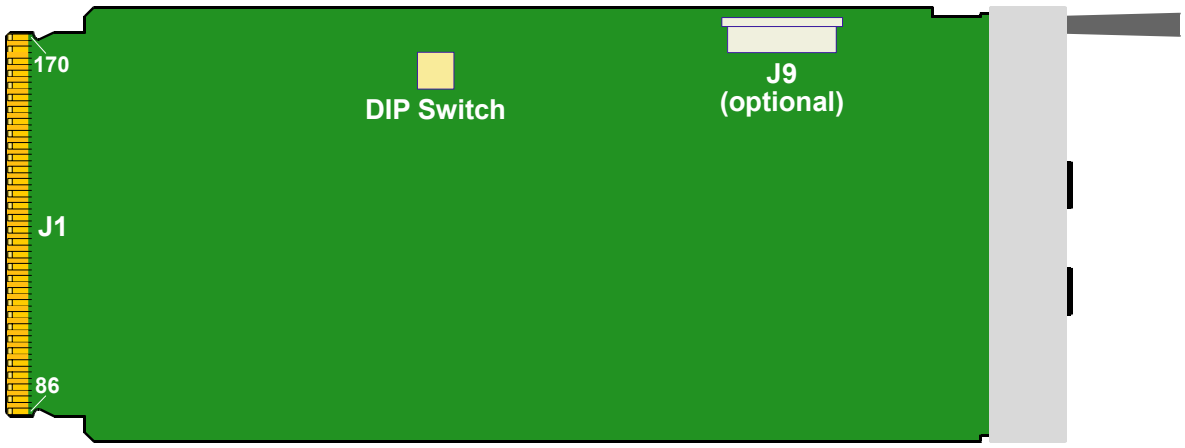


Figure 1-4: AM4001 Board Layout (Bottom View)



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1.5 Technical Specification

Table 1-2: AM4001 Main Specifications

	AM4001	SPECIFICATIONS

Processor and Memory	CPU	The AM4001 supports the following microprocessors:
		• Intel® Celeron® M processors (90 nm) with 400 MHz PSB (Processor Side Bus) in 479 µFCPGA packaging
		  • Intel® Celeron® M 1.0 GHz with 512 kB L2 cache (ultra low voltage)
		• Intel® Pentium® M processors (90 nm) with 400 MHz and 533 MHz PSB (Processor Side Bus) and SpeedStep® technology in 479 µFCBGA packaging
		  • Intel® Pentium® M 1.4 GHz, FSB: 400 MHz, 2 MB L2 cache, µFCBGA (low voltage)
		  • Intel® Pentium® M 1.8 GHz, FSB: 400 MHz, 2 MB L2 cache, µFCBGA
		  • Intel® Pentium® M 2.0 GHz, FSB: 533 MHz, 2 MB L2 cache, µFCBGA
		Please contact Kontron Modular Computers for further information concerning the suitability of other Intel processors for use with the AM4001.

	Memory	Main Memory:
		• Up to 4 GB registered DDR2 (PC3200) SDRAM memory with ECC on dedicated memory module
		Cache structure:
		• 64 kB L1 on-die full speed processor cache
		  • 32 kB for instruction cache
		  • 32 kB for data cache
		• Up to 2048 kB L2 on-die full speed processor cache
		FLASH Memory:
		• Two redundant Firmware Hub (FWH) Flash chips (2x1MB) controlled by the MMC
		Mass Storage Device:
		• Up to 1 GB NAND Flash via an onboard CompactFlash controller (true IDE mode)
		Serial EEPROM with 64 kbit

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Table 1-2: AM4001 Main Specifications (Continued)

	AM4001	SPECIFICATIONS

Chipset	Intel® E7320	Intel® E7320 Memory Controller Hub:
		• Support for a single Intel® Celeron® M or Pentium® M microprocessor
		• 64-bit AGTL/AGTL+ based System Bus interface at 400 MHz and 533 MHz
		• System Memory interface with optimized support for DDR2 SDRAM memory at 400 MHz with ECC
		• Two x4 PCI Express ports
		• RASUM (Reliability, Availability, Serviceability, Usability, and Manageability) features:
		  • Memory error detection and reporting of 1- and 2-bit errors including correction of 1-bit failures
		  • Integrated Memory Scrub Engine, which logs any uncorrectable memory errors
		  • Support for automatic read retry on uncorrectable errors
		  • Memory sparing allows for one memory bank per channel to be held in reserve and brought on-line if another memory bank in the channel becomes defective (only supported with 2 GB and 4 GB main memory configuration)

	Intel® 6300ESB	Intel® 6300ESB I/O Controller Hub: • Dual Channel SATA 150 interface • Integrated IDE controller Ultra ATA/100/66/33 (only the primary interface is used) • USB 2.0 host interface with up to four USB ports available (only one USB 2.0 port is used on the AM4001) • Firmware Hub (FWH) interface support • Low Pin Count (LPC) interface • PCI-X Rev. 1.0 with support for 64-bit/66 MHz PCI-X operations (not used on the AM4001) • PCI Rev. 2.2 compliant with support for 32-bit/33 MHz PCI operations (not used on the AM4001) • Power management logic support • Enhanced DMA controller, interrupt controller, and timer functions • System Management Bus (SMBus) compatible with most I²C™ devices
Onboard Controllers	Gigabit Ethernet	Intel® 82571EB Dual Gigabit Ethernet PCI Express bus controller with advanced management features, such as IDE and serial redirection over LAN
	Serial-to-USB Converter	Bridge between the legacy serial port and the USB port
AMC Interconnection	Gigabit Ethernet	Common options region port 0-1 • Two Gigabit Ethernet SerDes (1000BASE-BX) ports
	Serial ATA	Common options region port 2-3 • Two Serial ATA 150 ports
	PCI Express	Fat pipes region port 4-7 • One x4 PCI Express interface operating only as a root complex controller

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Table 1-2: AM4001 Main Specifications (Continued)

	AM4001	SPECIFICATIONS
Connectors	Front Panel Connectors	• One USB 2.0 port on 5-pin Mini USB type A connector • One USB 1.1 port (serial-to-USB converter) on 5-pin Mini USB type B connector
	AMC Edge Connector	The AMC edge connector is optimized for high-speed serial interconnects and supports 170 pins. The AM4001 communicates with the carrier board via the AMC edge connector, which supports a variety of fabric topologies divided into five functional groups: • Fabric interface • Synchronization clock interface • System management interface • JTAG interface • Module power interface
Switches	DIP Switch	DIP switch consisting of four switches for board configuration
LEDs	AMC LEDs	• HS/LED0 (blue): The hot swap indicator provides basic feedback to the user on the hot swap state of the module. The HS LED states are off, short blink, long blink, and on. • LED1 (amber): MMC control and debug LED • WD/LED2 (green): Watchdog or General Purpose; when lit during boot-up, it indicates a PCI reset is active • TH/LED3 (amber): Overtemperature Status or General Purpose; when lit during boot-up, it indicates a power failure
	Module LEDs	• MLED0 (green): Ethernet port 0 link signal status or General Purpose / BIOS POST code LED. • MLED1 (green): Ethernet port 1 link signal status or General Purpose / BIOS POST code LED. • MLED2 (green): SATA and CompactFlash activity status or General Purpose / BIOS POST code LED. • MLED3 (green): MMC Debug or General Purpose / BIOS POST code LED.
Timer	Watchdog Timer	• Software-configurable, two-stage watchdog with programmable timeout ranging from 125 msec to 256 sec in 12 steps • Serves for generating IRQ, NMI, or hardware reset
	System Timer	• The 6300ESB contains three 8254-style counters which have fixed uses • In addition to the three 8254-style counters, the 6300ESB includes three individual multimedia event timers that may be used by the operating system. They are implemented as a single counter each with its own comparator and value register. • Hardware delay timer for short reliable delay times

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Table 1-2: AM4001 Main Specifications (Continued)

	AM4001	SPECIFICATIONS
IPMI	Module Management Controller	• Renesas H8 microcontroller with 4 kB RAM and redundant 128 kB Firmware Flash with automatic roll-back strategy • The MMC carries out IPMI commands such as monitoring several onboard temperature conditions, board voltages and the power supply status, and managing hot swap operations • The MMC is accessible via a local IPMB (IPMB-L) and two host Keyboard Style Interfaces (KCS) interfaces
	Hot Swap	The AM4001 has full hot swap capability.
	Thermal Management	CPU and board overtemperature protection is provided by: • Five temperature sensors for monitoring the board temperature • Internal processor temperature control unit • CPU shut down via hardware monitor • Specially designed heat sinks
General	Mechanical	Single-width compliant form factor: • Half-height versions • Full-height versions • Extended full-height versions (with large heat sink)
	Power Consumption	For further information, refer to Chapter 6, “Power Considerations”.
	Temperature Range	Operational: -5°C to +55°C Storage: -40°C to +70°C
	Dimensions	181.5 mm x 73.5 mm
	Board Weight	152 grams (without heat sink)
	JTAG	The JTAG interface is routed to the onboard debug interface or the AMC edge connector for debugging and manufacturing purposes.

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Table 1-2: AM4001 Main Specifications (Continued)

	AM4001	SPECIFICATIONS
Software	Software BIOS	AMI BIOS with 1 MB of Flash memory and having the following features: • Serial console redirection via serial-to-USB converter or LAN • QuickBoot • QuietBoot • BootBlock • LAN boot capability for diskless systems (standard Etherboot/PXE on demand) • Boot from USB floppy disk drive • BIOS boot support for USB keyboards • Plug and Play capability • BIOS parameters are saved in the EEPROM • Board serial number is saved within the EEPROM • ACPI
	Software IPMI	PICMG AMC.0 R1.0 compliant Module Management Controller Firmware with the following features: • The MMC is accessible via IPMB-L and two KCS interfaces with interrupt support • The MMC Firmware can be updated in field through all supported interfaces using the Kontron FirmWare Upgrade Manager (FWUM) • Two MMC Flash banks with automatic roll-back capability in case of an upgrade Firmware failure • Board supervision and control extensions such as board reset, power and Firmware Hub Flash control, and boot order configuration
	Operating System	The AM4001 is offered with the generic Linux Board Support Package which supports various Linux distributions including the Carrier Grade Linux (CGL) operating system. Please contact Kontron Modular Computers for further information concerning other operating systems.

1.6 Kontron Software Support

Kontron is one of the few AdvancedTCA and CompactPCI vendors providing inhouse support for most of the industry-proven real-time operating systems that are currently available. Due to its close relationship with the software manufacturers, *Kontron* is able to produce and support BSPs and drivers for the latest operating system revisions thereby taking advantage of the changes in technology.

Finally, customers possessing a maintenance agreement with *Kontron* can be guaranteed hotline software support and are supplied with regular software updates. A dedicated web site is also provided for online updates and release downloads.

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1.7 Applied Standards

The *Kontron Modular Computers'* AMC boards comply with the requirements of the following standards.

Table 1-3: Applied Standards

COMPLIANCE	TYPE	STANDARD	TEST LEVEL
CE	Emission	EN55022 EN61000-6-3 EN300386	--
	Immission	EN55024 EN61000-6-2 EN300386	--
	Electrical Safety	EN60950	--
Mechanical	Mechanical Dimensions	IEEE 1101.10	--
Environmental and Health Aspects	Vibration (sinusoidal, operating)	IEC60068-2-6	5-100 [Hz] / 1 [g] / 0.25 [oct/min] 100-500 [Hz] / 1 [g] / 1 [oct/min] 10 [cycles/axis] 3 [directions: x,y,z]
	Vibration (sinusoidal, non-operating)	IEC60068-2-6	2-50 [Hz] / 1 [g] / 0.1 [oct/min] 50-500 [Hz] / 3 [g] / 0.25 [oct/min] 10 [cycles/axis] 3 [directions: x,y,z]
	Shock (operating)	IEC60068-2-27	4 [g] 22 [ms] 3 [shocks per direction] 5 [s] recovery time 6 [directions, ±x, ±y, ±z]
	Shock (non-operating)	IEC60068-2-27	10 [g] 11 [ms] 3 [shocks per direction] 5 [s] recovery time 6 [directions, ±x, ±y, ±z]
			30 [g] 6 [ms] 3 [shocks per direction] 5 [s] recovery time 6 [directions, ±x, ±y, ±z]
	Climatic Humidity	IEC60068-2-78	93% RH at 40°C, non-condensing
	WEEE	Directive 2002/96/EC	Waste electrical and electronic equipment
	RoHS	Directive 2002/95/EC	Restriction of the use of certain hazardous substances in electrical and electronic equipment

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1.8 Related Publications

The following publications contain information relating to this product.

Table 1-4: Related Publications

PRODUCT	PUBLICATION
ATCA	PICMG 3.0 R1.0 AdvancedTCA Base Specification, December 30, 2002
AMC	PICMG AMC.0, Advanced Mezzanine Card Specification R1.0 PICMG AMC.1, PCI Express and Advanced Switching R1.0 PICMG AMC.2, Gigabit Ethernet R1.0 (draft version) PICMG AMC.3, Storage Interfaces R1.0
IPMI	IPMI - Intelligent Platform Management Interface Specification, v1.5 Document Revision 1.1, February 20, 2002 IPMI - Platform Management FRU Information Storage Definition, V1.0 Document Revision 1.1, September 27, 1999 IPMI - Intelligent Platform Management Bus Communications Protocol Specification V1.0 Document Revision 1.0, November 15, 1999
PCI Express	PCI Express Base Specification Revision 1.0a
Serial ATA	Serial ATA 1.0a Specification

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Chapter 2

Functional Description

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2. Functional Description

2.1 CPU, Memory and Chipset

2.1.1 CPU

The AM4001 supports the latest Intel® Celeron® M and Pentium® M processor family up to speeds of 2.0 GHz. The Intel® Celeron® M and Pentium® M microprocessors offer exceptional performance with low power consumption. These processors are based on a new core which is optimized for low power consumption.

The Intel® Pentium® M supports the latest Intel® SpeedStep® technology, which enables real-time dynamic switching of the voltage and frequency between several modes. This is achieved by switching the bus ratios, core operating voltage, and core processor speeds without resetting the system. The frequency for the Intel® Pentium® M processor may also be selected in the BIOS.

The following list sets out some of the key features of this processor:

- Intel Architecture with Dynamic Execution
- High-performance, low-power core
- On-die, primary 32 kB instruction cache and 32 kB write-back data cache
- On-die, second level cache with Advanced Transfer Cache Architecture
  - Intel® Celeron® M with 512 kB L2 cache
  - Intel® Pentium® M with 2048 kB L2 cache
- Advanced Branch Prediction and Data Prefetch Logic
- Streaming SIMD Extensions 2 (SSE2)
- 400 MHz and 533 MHz, processor system bus
- Advanced Power Management features including Enhanced Intel® SpeedStep® Technology (only Intel® Pentium® M processors)

The following tables provide information on the Intel® Celeron® M processor supported on the AM4001 and its maximum power dissipation.

Table 2-1: Intel® Celeron® M Processor Supported on the AM4001

SPEED	1.0 GHz - ULV[1)]
L2 CACHE	512 kB
CORE VOLTAGE	0.940 V
PROCESSOR SIDE BUS	400 MHz

[1)] ULV Ultra Low Voltage

Table 2-2: Maximum Power Dissipation of Intel® Celeron® M (CPU only)

FREQUENCY MODE	1.0 GHz - ULV
Maximum Power	5 W



Note ...

The Intel® Celeron® M processor does not support the Intel® SpeedStep® feature. This processor always runs with a fixed frequency.

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The following tables indicate the Intel® Pentium® M processors supported on the AM4001, their maximum power dissipation and their core voltage in the various frequency modes.

Table 2-3: Intel® Pentium® M Processors Supported on the AM4001

SPEED	1.4 GHz - LV[2)]	1.8 GHz	2.0 GHz
PACKAGE	µFCPGA	µFCPGA	µFCPGA
L2 CACHE	2048 kB	2048 kB	2048 kB
CORE VOLTAGE	0.988 - 1.116 V	0.988 - 1.276 V	0.988 - 1.276 V
PROCESSOR SIDE BUS	400 MHz	400 MHz	533 MHz

Table 2-4: Maximum Power Dissipation of Intel® Pentium® M (CPU only)

FREQUENCY MODE	1.4 GHz - LV	1.8 GHz	2.0 GHz
Maximum Power HFM[3)]	10 W	21 W	27 W
Maximum Power LFM[4)]	7.5 W	7.5 W	10.8 W

[2)] LV Low Voltage

[3)] HFM High Frequency Mode (maximum frequency of the CPU)

[4)] LFM Low Frequency Mode (frequency is 600 MHz for 1.4 GHz and 1.8 GHz processors, and 800 MHz for 2.0 GHz processor)

2.1.2 Memory

The AM4001 supports a single-channel (72-bit), registered Double Data Rate (DDR2) memory with Error Checking and Correcting (ECC) running at 400 MHz (PC3200). It provides one 240-pin, high-density connector for the memory module that supports up to 4 GB system memory. The available memory module configuration can be either 1 GB, 2 GB, or 4 GB.

There are several Reliability, Availability, Serviceability, Usability, and Manageability (RASUM) features available for the memory interface:

- Memory error detection and reporting of 1 and 2 bit errors and correction of 1 bit failures
- Integrated Memory Scrub Engine, the scrub engine logs any uncorrectable memory error
- Support for automatic read retry on uncorrectable errors
- Memory sparing allows for one memory bank per channel to be held in reserve and brought on-line if another memory bank in the channel becomes defective (only supported with 2 GB and 4 GB main memory configuration).

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2.1.3 Intel® E7320 Chipset Overview

The Intel® E7320 chipset consists of the following devices:

- Intel® E7320 memory controller hub (MCH)
- Intel® 6300ESB I/O controller hub (ICH)

The MCH provides the processor interface for the Intel® Celeron® M and Pentium® M microprocessors and the memory bus. The ICH is a centralized controller for the boards' I/O peripherals such as the USB 2.0 and the IDE port. The Firmware Hub Flash provides the non-volatile storage for the BIOS.

2.1.4 Memory Controller Hub E7320

The E7320 Memory Controller Hub (MCH) is a highly integrated hub that provides the CPU interface, a dual-channel DDR2 SDRAM system memory interface (optimized for DDR400/PC3200), two x4 PCI Express, and a high-speed hub link interface to the 6300ESB I/O controller hub. The AM4001 uses single-channel DDR2 memory configuration.

2.1.5 I/O Controller Hub 6300ESB

The 6300ESB is a highly integrated multifunctional I/O Controller Hub that provides the interface to the PCI and PCI-X Bus, and integrates many of the functions needed in today's PC platforms, such as Ultra DMA 100/66/33 controller, SATA 150, USB host controller supporting USB 2.0, LPC interface and FWH Flash BIOS interface controller. The 6300ESB communicates with the host controller over a dedicated hub interface.

The I/O controller hub feature set comprises:

- Dual channel SATA 150 interface
- Integrated IDE controller Ultra ATA/100/66/33 (only the primary interface is used)
- USB 2.0 host interface with up to four USB ports available (only one USB 2.0 port is used on the AM4001)
- Firmware Hub interface support
- Low pin count interface
- PCI-X Rev. 1.0 with support for 64-bit/66 MHz PCI-X operations (not used on the AM4001)
- PCI Rev. 2.2 compliant with support for 32-bit/33 MHz PCI operations (not used on the AM4001)
- Power management logic support
- Enhanced DMA controller, interrupt controller, and timer functions
- System Management Bus (SMBus) compatible with most I²C™ devices
- Hub interface for the E7320 MCH
- RTC controller

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2.2 Peripherals

The following standard peripherals are available on the AM4001 board:

2.2.1 Timer

The AM4001 is equipped with the following timers:

- Real-Time Clock
  The 6300ESB integrates a MC146818A compatible real-time clock with 256 Byte CMOS RAM. The AM4001 does not include a dedicated 3V lithium battery power source for RTC backup. Alternatively, the RTC can be powered from the management power. But, if the power is switched off, the RTC will lose its data. All CMOS RAM data remain stored in an additional EEPROM device to prevent data loss.
- Counter/Timer
  Three 8254-style counter/timers are included on the AM4001 as defined for the PC/AT.
- In addition to the three 8254-style counters, the 6300ESB includes three individual multimedia event timers that may be used by the operating system. They are implemented as a single counter each with its own comparator and value register.
- Hardware delay timer for short reliable delay times

2.2.2 Watchdog Timer

The AM4001 provides a watchdog timer that is programmable for a timeout period ranging from 125 msec to 256 sec in 12 steps. Failure to trigger the watchdog timer in time results in a system reset, an interrupt, or NMI. In the dual-stage mode, a combination of both NMI, and reset if the watchdog is not serviced. A hardware status flag will be provided to determine if the watchdog timer generated the reset.

2.2.3 Battery

The AM4001 does not provide a battery. All CMOS RAM data remain stored in an additional EEPROM device to prevent data loss.

2.2.4 Power Monitor and Reset Generation

All onboard voltages on the AM4001 are supervised, which guarantees controlled power-up of the board. This is done by activating a stable power-up reset signals after the threshold voltages have been passed.

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2.2.5 SMBus Devices

The AM4001 provides a System Management Bus (SMBus) for access to six onboard devices. The SMBus consists of a two-wire I^2C bus interface. The following table indicates the function and address of every onboard SMBus device.

Table 2-5: SMBus Device Addresses

DEVICE	SMBus ADDRESS
EEPROM	1010101xb
Clock generator	1101001xb
PCI Express clock buffer	1101110xb
DDR2 SPD	1010011xb
6300ESB slave	1000100xb
E7320	0110000xb

2.2.6 Serial EEPROM

A serial EEPROM with 64 kbit is provided for storing CMOS data and saving the board serial number. The EEPROM is connected to the 6300ESB SMBus interface.

Table 2-6: EEPROM Address Map

ADDRESS	FUNCTION
0x000 - 0x0FF	CMOS backup
0x100 - 0x1FF	Production data
0x200 - 0x3FF	OS Bootparameter
0x400 - 0x7FF	User

2.2.7 FLASH Memory

There are two Flash devices available as described below, one for the BIOS and one for the CompactFlash controller.

2.2.7.1 BIOS FLASH (Firmware Hub)

The AM4001 provides two redundant Firmware Hub Flash chips (2x1MB). The fail-over mechanism for the BIOS recovery can be controlled via the MMC controller or the DIP switch. If one Firmware Hub Flash is corrupted, the MMC can enable the second Firmware Hub Flash and boot the system again.

2.2.7.2 CompactFlash Controller

The AM4001 supports up to 1 GB of soldered IDE Flash, i.e. NAND Flash in combination with a dedicated IDE Flash controller is connected to the primary IDE port of the 6300ESB I/O controller hub. The controller supports true IDE mode.

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2.3 Board Interfaces

2.3.1 Front Panel LEDs

The AM4001 is equipped with four AMC LEDs and four module LEDs, which can be configured via two onboard registers. For further information on configuring the LEDs, refer to section 4.4.11, “Module LED Configuration Register 0”, and 4.4.12, “AMC LED Configuration Register 1”.

Figure 2-1: Front Panel LEDs

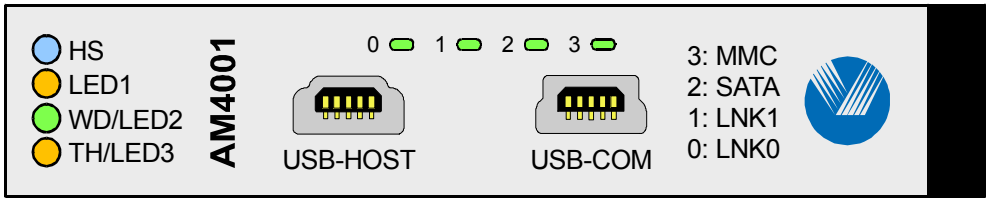


Table 2-7: AMC LEDs Function

AMC LED	FUNCTION DURING BOOT-UP	DEFAULT FUNCTION AFTER BOOT-UP
HS (blue)	--	The hot swap indicator provides basic feedback to the user on the hot swap state of the module. The HS LED states are off, short blink, long blink, and on.
LED1 (amber)	If this LED does not turn off, the MMC does not operate.	MMC Control LED
WD/LED2 (green)	When lit during boot-up, it indicates a PCI reset is active.	Watchdog or General Purpose
TH/LED3 (amber)	When lit during boot-up, it indicates a power failure.	Overtemperature Status or General Purpose

Table 2-8: Module LEDs Function

MODULE LED	FUNCTION DURING BOOT-UP	FUNCTION DURING BIOS POST (if POST code configuration is enabled)	DEFAULT FUNCTION AFTER BOOT-UP
MLED0 (green)	When lit up during boot-up, it indicates a CPU power failure	BIOS POST bit 3 and bit 7	Ethernet port 0 link signal status or General Purpose
MLED1 (green)	When lit up during boot-up, it indicates a clock power failure	BIOS POST bit 2 and bit 6	Ethernet port 1 link signal status or General Purpose
MLED2(green)	When lit up during boot-up, it indicates a dramatic system fail-ure (no access to the FHW Flash)	BIOS POST bit 1 and bit 5	SATA and CompactFlash activity status or General Purpose
MLED3 (green)	When lit up during boot-up, it indicates a FWH Flash failure	BIOS POST bit 0 and bit 4	MMC Control or General Purpose

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How to Read the 8-Bit POST Code

Due to the fact that only 4 bits are available and 8 bits must be displayed, the module LEDs are multiplexed.

The following is an example of the module LEDs' operation if BIOS POST configuration is enabled (see also table 2-8, "Module LEDs Function").

Table 2-9: POST Code Example

STATE	MODULE LEDs
0	All module LEDs are OFF; start of POST sequence
1	High nibble
2	Low nibble; state 2 is followed by state 0

The following table shows the description of the MMC Control LEDs.

Table 2-10: MMC Control LEDs Description

MMC CONTROL LED	DEFAULT	ERROR CONDITION	BLINKING SPEED	SIGNIFICATION
LED1(amber)	Slow blinking	ON	Slow: 250 msec ON 3 sec OFF	The management controller is running normally; it is a heart beat
			Fast: 8x 150 msec ON 8x 50 msec OFF	Send/receive data through the IPMB-L bus
MLED3 (green)	OFF	--	Slow: 100 msec ON 1.4 sec OFF	Management controller request attention to SMS/SMM (this may occur when there is a message waiting for the SMS)
			Fast: 8x 150 msec ON 8x 50 msec OFF	Send/receive data through the KCS interface



Note ...

Under normal operating conditions, the LEDs should not remain lit during boot-up. They are intended to be used only for debug purposes. If the AM4001 is correctly inserted and operating properly, only the LED1 and the MLED3 are blinking (MMC heart beat).

In the event that an LED lights up during boot-up and the AM4001 does not boot, please contact the Kontron Modular Computers' Technical Support.



Note ...

If the overtemperature LED flashes on and off at regular intervals, it indicates that the processor junction temperature has reached a level beyond which permanent silicon damage may occur. Upon assertion of Thermtrip, the processor will shut off its internal clocks (thus halting program execution) in an attempt to reduce the processor junction temperature.

Once activated, Thermtrip remains latched until a cold restart of the AM4001 is undertaken (all power off and then on again).

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2.3.2 General Purpose DIP Switch

The AM4001 is equipped with a general purpose 4-bit DIP switch which enables the user to configure the AM4001 according to his individual needs.

The following table indicates the functions of the four switches integrated in the DIP switch.

Table 2-11: DIP Switch Functions

SWITCH	FUNCTION
1	General purpose LED or POST code display during bootup
2	BIOS Firmware Hub configuration
3	Boot order configuration
4	Clearing BIOS CMOS parameters

For further information on the DIP switch configuration, refer to section 4.1, “DIP Switch Configuration”.

2.3.3 Debug Interface

The AM4001 provides several onboard options for hardware and software debugging, such as:

- Two debug LEDs indicating a system reset and a power failure
- Four debug LEDs for POST code
- JTAG interface J7 for logic updating
- An optional ITP700 (processor JTAG) connector J9 is included to facilitate debug and BIOS software development.

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2.3.4 USB Interfaces

The AM4001 supports one USB 2.0 host port via the 5-pin Mini USB type A connector and one USB 1.1 port (serial-to-USB converter) via the 5-pin Mini USB type B connector on the front panel.

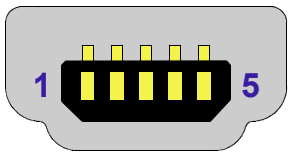
The two Mini USB connectors used on the AM4001 have different housings and require different adapters/cables in order to be connected to standard USB devices or to the host. Whereas the Mini USB type B connector requires merely a commercial USB cable, the Mini USB type A connector requires a special adapter. The following sections provide detailed information on the MinI USB connectors including the respective adapters/cables.

2.3.4.1 USB 2.0 Host Interface

The AM4001 supports one high-speed, full-speed, and low-speed capable USB 2.0 host port on the front panel. This port allows connecting USB peripheral devices to the AM4001.

The following figure illustrates the Mini USB type A Connector J3.

Figure 2-2: Mini USB Type A Connector J3



The following table indicates the pinout of the Mini USB type A connector J3.

Table 2-12: Mini USB Type A Connector J3

PIN	SIGNAL	FUNCTION	IN/OUT
1	VCC	VCC signal	--
2	UV0-	Differential USB-	I/O
3	UV0+	Differential USB+	I/O
4	NC	Not Connected	--
5	GND	GND signal	--

Note ...

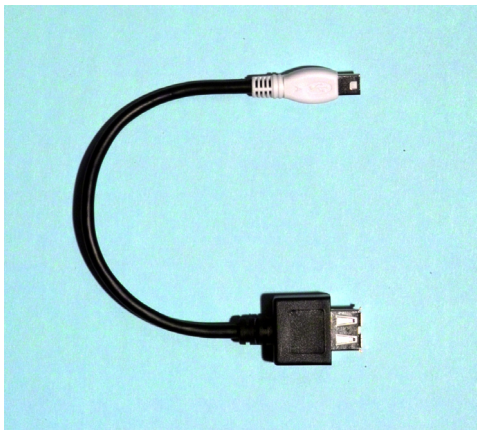
The USB host functionality is supported only on the J3 Mini USB type A connector, i.e. USB peripheral devices can only be connected to this connector.

The USB power supply to the Mini USB type A connector provides 500 mA continuous load current a short-circuit protection (900 mA). All the signal lines are EMI filtered.

In order to connect standard USB devices with a type A female connector to the Mini USB type A connector, a special adapter is required. The following figure illustrates the adapter required to connect standard USB devices with type A female connector to the Mini USB type A connector. For further technical or ordering information on the adapters please contact Kontron Modular Computers' Technical Support.

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Figure 2-3: Adapter for Mini USB Type A to USB Type A Male Connector



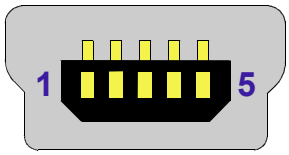
2.3.4.2 USB 1.1 Serial-to-USB Interface

The AM4001 supports one full-speed and low-speed capable USB 1.1 port on the front panel. This port is connected to a serial-to-USB converter, which provides the bridging between the onboard legacy serial interface and the USB 1.1 port. On the AM4001, the serial interface to the host is a legacy COM port. Therefore, the AM4001 does not require a driver to communicate with the host. However, the host requires a virtual USB COM port driver in order to communicate with the AM4001. By using this driver, the host's application software regards the serial interface on the AM4001 as standard COM port.

Furthermore, the serial-to-USB interface can also be used for BIOS console redirection; the default baudrate configuration is 115,000 baud/s.

The following figure illustrates the Mini USB type B Connector J2.

Figure 2-4: Mini USB Type B Connector J2



The following table indicates the pinout of the Mini USB type B connector J2.

Table 2-13: Mini USB Type B Connector J2

PIN	SIGNAL	FUNCTION	IN/OUT
1	VCC	VCC signal	--
2	UV0-	Differential USB-	I/O
3	UV0+	Differential USB+	I/O
4	NC	Not Connected	--
5	GND	GND signal	--

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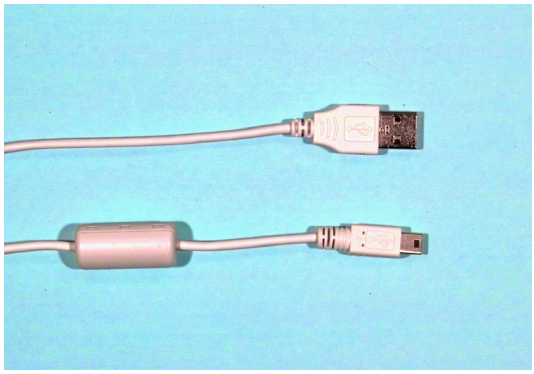
Note ...

The serial-to-USB functionality is only supported on the J2 Mini USB type B connector, i.e. only this connector can be used for data transfer from the AM4001 to the host. USB Peripheral devices cannot be connected to the J2 Mini USB type B connector.

To connect the USB 1.1 port to the host, a standard USB type A cable (on the host side) to a Mini USB type B (on the AM4001) is necessary. This is a commercial USB cable that can also be used with standard PC devices, such as digital cameras, MP3 players, etc.

The following figure illustrates the cable required to connect the Mini USB type B connector to an host USB port.

Figure 2-5: Cable for Mini USB Type B to USB Type A Female Connector



2.3.5 Gigabit Ethernet

The AM4001 board includes two redundant 1000BASE-BX, SerDes Ethernet ports based on the Intel® PCI Express 82571EB controller.

The Intel® 82571EB Dual Gigabit Ethernet Controller architecture is optimized to deliver high performance data throughput with the lowest power consumption. The controller's architecture includes a large packet buffer (48 kB per port) which maintains superior performance.

The Ethernet controller is directly connected to the E7320 chipset using x4 PCI Express lanes. The two 1000BASE-BX, SerDes Ethernet ports are connected to the common options region of the AMC edge connector. 1000BASE-BX (SerDes) is the AMC electrical specification for transmission of 1 Gb/s Ethernet over a single AMC port.

Additionally, the controller provides several advanced management features, such as IDE and serial-over-LAN redirection via the PCI Express interface. In the IDE configuration, the 82571EB explicitly looks like a regular IDE controller. The operating system identifies the 82571EB as a virtual hard disk or floppy disk. In the serial-over-LAN redirection, the 82571EB looks like a regular COM controller and the BIOS can send all serial packets to the remote console over LAN.

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2.4 AMC Interconnection

The AM4001 communicates with the carrier board via the AMC edge connector, which is a serial interface optimized for high-speed interconnects. The AMC edge connector supports a variety of fabric topologies divided into five functional groups:

- Fabric interface
- Synchronization clock interface
- System management interface
- JTAG interface
- Module power interface

These interfaces are compliant with the following specifications:

- PICMG AMC.0, Advanced Mezzanine Card Specification R1.0
- PICMG AMC.1, PCI Express and Advanced Switching R1.0
- PICMG AMC.2, Gigabit Ethernet R1.0
- PICMG AMC.3, Storage Interfaces R1.0

The following sections provide detailed information on these interfaces.

2.4.1 Fabric Interface

The Fabric interface is the real communication path and comprises 21 high-speed ports providing point-to-point connectivity for module-to-carrier and module-to-module implementations. The high-speed ports are separated in three logical regions as follows:

- Common options region
- Fat pipes region
- Extended options region

In the common options region, the AM4001 supports two redundant Gigabit Ethernet ports and a dual SATA interface. In the fat pipes region, the AM4001 provides a x4 PCI Express interface, which operates as a root-complex only and does not support non-transparent PCI bridge functionality. On the AM4001, the extended options region is not used.

The AM4001 Port Mapping is represented below:

- Port 0-1: Two redundant Gigabit SerDes (1000Base-BX) ports, common options region (according to PICMG AMC.2, Gigabit Ethernet R1.0)
- Port 2-3: dual SATA storage interface, common options region (according to PICMG AMC.3, Storage Interfaces R1.0)
- Port 4-7: PCI Express, fat pipes region (according to PICMG AMC.1, PCI Express and Advanced Switching R1.0)

The PICMG AMC.0, Advanced Mezzanine Card Specification R1.0 is the base specification for the fabric interface.

The following figure illustrates the port mapping of the AM4001.

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Figure 2-6: AM4001 Port Mapping

	Port No.	AMC Standard Port Mapping	AM4001 Port Mapping	AM4001 Interface Mapping
Basic Connector	CLK1	Clocks	not used	not used
	CLK2			
	CLK3		PCI Express Reference Clock	PCI Express Reference Clock
	0	Common Options Region	GbE-1	GbE-1 port from 82571EB controller
	1		GbE-2	GbE-2 port from 82571EB controller
	2		SATA -1	SATA-2 port from 6300ESB ICH
	3		SATA -2	SATA-1 port from 6300ESB ICH
	4	Fat Pipes Region	x4 PCI Express	x4 PCI Express port A1 from E7320 MCH
	5			
	6			
	7			
Extended Connector	8	Fat Pipes Region	not used	not used
	9			
	10			
	11			
	12	Extended Options Region	not used	not used
	13			
	14			
	15			
	16			
	17			
	18			
	19			
	20			

2.4.2 Synchronization Clock Interface

Many telecommunications applications using the AdvancedTCA and Advanced Mezzanine Card architectures need to interface to external networks that require strict timing relationships between multiple interfaces and the external network, such as PDH and SONET/SDH networks. Such interfaces typically require the AMC module to receive frame and bit rate clocks from the carrier, and to transmit a bit rate clock to the carrier.

According to the PCI Express Base Specification Revision 1.0a, either two separate 100 MHz reference clocks may be provided, one on the AM4001 and one on the carrier, or one common clock source may be provided for both the AM4001 and the carrier. If the common clock source is used for both devices, the AM4001 uses the AMC clock interface CLK3 (see figure 2-5, “AM4001 Port Mapping”). In this event, the carrier must provide the common reference clock (100 MHz) on the CLK3 pins. The AM4001 supports both clock configuration.



Note ...

The clock spectrum modulation can be enabled in the BIOS setup. If clock spectrum modulation is enabled or the deviation between the two reference clocks is greater than ± 300 ppm, a common clock configuration is mandatory. Without a common clock, the PCI Express interface does not work.

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2.4.3 System Management Interface

The system management interface is a port from the module to the carrier via the Local Intelligent Platform Management Bus (IPMB-L). The Module Management Controller uses this port for the communication with the carrier Intelligent Platform Management Controller (IPMC). The IPMB-L is a multi-master I²C bus.

2.4.4 JTAG Interface

JTAG support is provided on the AMC edge connector. The JTAG interface is supported for vendor product test and logic update.

On the AM4001, the FPGA JTAG port can be connected to the AMC JTAG port.

2.4.5 Module Power Interface

The module power interface provides the management power (MP) and payload power (PWR). These two supply voltages must have power-good indicators so that the system management can detect boot sequence events and nominal operating conditions.

The AM4001 operates with payload power in the range of 10.8 V to 13.2 V, and with management power of 3.3 V ± 5%.

The board supports removal and insertion in a powered slot as required by AMC.0.

2.4.6 Pinout of AMC Edge Connector J1

The AMC edge connector is a high-speed serial interface and supports 170 pins. The following table provides the pinout of the AMC edge connector J1. The shaded table cells indicate signals that are not used on the AM4001.

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Table 2-14: Pinout of AMC Edge Connector J1

BASIC SIDE (COMPONENT SIDE 1)				EXTENDED SIDE (COMPONENT SIDE 2)			
PIN	SIGNAL	FUNCTION	DRIVEN BY	PIN	SIGNAL	FUNCTION	DRIVEN BY
1	GND	Logic Ground	-	170	GND	Logic Ground	-
2	PWR	Payload Power	Carrier	169	TDI	JTAG Test Data Input	Carrier
3	PS1#	Presence 1	AMC	168	TDO	JTAG Test Data Output	AMC
4	MP	Management Power	Carrier	167	TRST#	JTAG Test Reset Input	Carrier
5	GA0	Geographic Address 0	Carrier	166	TMS	JTAG Test Mode Select In	Carrier
6	RSV	Reserved	-	165	TCK	JTAG Test Clock Input	Carrier
7	GND	Logic Ground	-	164	GND	Logic Ground	-
8	RSV	Reserved	-	163	Tx20+	Port 20 Transmitter +	AMC
9	PWR	Payload Power	Carrier	162	Tx20-	Port 20 Transmitter -	AMC
10	GND	Logic Ground	-	161	GND	Logic Ground	-
11	Tx0+	Port 0 Transmitter +	AMC	160	Rx20+	Port 20 Receiver +	Carrier
12	Tx0-	Port 0 Transmitter -	AMC	159	Rx20-	Port 20 Receiver -	Carrier
13	GND	Logic Ground	-	158	GND	Logic Ground	-
14	Rx0+	Port 0 Receiver +	Carrier	157	Tx19+	Port 19 Transmitter +	AMC
15	Rx0-	Port 0 Receiver	Carrier	156	Tx19-	Port 19 Transmitter -	AMC
16	GND	Logic Ground	-	155	GND	Logic Ground	-
17	GA1	Geographic Address 1	Carrier	154	Rx19+	Port 19 Receiver +	Carrier
18	PWR	Payload Power	Carrier	153	Rx19-	Port 19 Receiver -	Carrier
19	GND	Logic Ground	-	152	GND	Logic Ground	-
20	Tx1+	Port 1 Transmitter +	AMC	151	Tx18+	Port 18 Transmitter +	AMC
21	Tx1-	Port 1 Transmitter -	AMC	150	Tx18-	Port 18 Transmitter -	AMC
22	GND	Logic Ground	-	149	GND	Logic Ground	-
23	Rx1+	Port 1 Receiver +	Carrier	148	Rx18+	Port 18 Receiver +	Carrier
24	Rx1-	Port 1 Receiver -	Carrier	147	Rx18-	Port 18 Receiver -	Carrier
25	GND	Logic Ground	-	146	GND	Logic Ground	-
26	GA2	Geographic Address 2	Carrier	145	Tx17+	Port 17 Transmitter +	AMC
27	PWR	Payload Power	Carrier	144	Tx17-	Port 17 Transmitter -	AMC
28	GND	Logic Ground	-	143	GND	Logic Ground	-
29	Tx2+	Port 2 Transmitter +	AMC	142	Rx17+	Port 17 Receiver +	Carrier
30	Tx2-	Port 2 Transmitter -	AMC	141	Rx17-	Port 17 Receiver -	Carrier
31	GND	Logic Ground	-	140	GND	Logic Ground	-

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Table 2-14: Pinout of AMC Edge Connector J1 (Continued)

BASIC SIDE (COMPONENT SIDE 1)				EXTENDED SIDE (COMPONENT SIDE 2)			
PIN	SIGNAL	FUNCTION	DRIVEN BY	PIN	SIGNAL	FUNCTION	DRIVEN BY
32	Rx2+	Port 2 Receiver +	Carrier	139	Tx16+	Port 16 Transmitter +	AMC
33	Rx2-	Port 2 Receiver -	Carrier	138	Tx16-	Port 16 Transmitter -	AMC
34	GND	Logic Ground	-	137	GND	Logic Ground	-
35	Tx3+	Port 3 Transmitter +	AMC	136	Rx16+	Port 16 Receiver +	Carrier
36	Tx3-	Port 3 Transmitter -	AMC	135	Rx16-	Port 16 Receiver -	Carrier
37	GND	Logic Ground	-	134	GND	Logic Ground	-
38	Rx3+	Port 3 Receiver +	Carrier	133	Tx15+	Port 15 Transmitter +	AMC
39	Rx3-	Port 3 Receiver -	Carrier	132	Tx15-	Port 15 Transmitter -	AMC
40	GND	Logic Ground	-	131	GND	Logic Ground	-
41	ENABLE#	AMC Enable	Carrier	130	Rx15+	Port 15 Receiver +	Carrier
42	PWR	Payload Power	Carrier	129	Rx15-	Port 15 Receiver -	Carrier
43	GND	Logic Ground	-	128	GND	Logic Ground	-
44	Tx4+	Port 4 Transmitter +	AMC	127	Tx14+	Port 14 Transmitter +	AMC
45	Tx4-	Port 4 Transmitter -	AMC	126	Tx14-	Port 14 Transmitter -	AMC
46	GND	Logic Ground	-	125	GND	Logic Ground	-
47	Rx4+	Port 4 Receiver +	Carrier	124	Rx14+	Port 14 Receiver +	Carrier
48	Rx4-	Port 4 Receiver -	Carrier	123	Rx14-	Port 14 Receiver -	Carrier
49	GND	Logic Ground	-	122	GND	Logic Ground	-
50	Tx5+	Port 5 Transmitter +	AMC	121	Tx13+	Port 13 Transmitter +	AMC
51	Tx5-	Port 5 Transmitter -	AMC	120	Tx13-	Port 13 Transmitter -	AMC
52	GND	Logic Ground	-	119	GND	Logic Ground	-
53	Rx5+	Port 5 Receiver +	Carrier	118	Rx13+	Port 13 Receiver +	Carrier
54	Rx5-	Port 5 Receiver -	Carrier	117	Rx13-	Port 13 Receiver -	Carrier
55	GND	Logic Ground	-	116	GND	Logic Ground	-
56	SCL_L	IPMB-L Clock	IPMI Agent	115	Tx12+	Port 12 Transmitter +	AMC
57	PWR	Payload Power	Carrier	114	Tx12-	Port 12 Transmitter -	AMC
58	GND	Logic Ground	-	113	GND	Logic Ground	-
59	Tx6+	Port 6 Transmitter +	AMC	112	Rx12+	Port 12 Receiver +	Carrier
60	Tx6-	Port 6 Transmitter -	AMC	111	Rx12-	Port 12 Receiver -	Carrier
61	GND	Logic Ground	-	110	GND	Logic Ground	-

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Table 2-14: Pinout of AMC Edge Connector J1 (Continued)

BASIC SIDE (COMPONENT SIDE 1)				EXTENDED SIDE (COMPONENT SIDE 2)			
PIN	SIGNAL	FUNCTION	DRIVEN BY	PIN	SIGNAL	FUNCTION	DRIVEN BY
62	Rx6+	Port 6 Receiver +	Carrier	109	Tx11+	Port 11 Transmitter +	AMC
63	Rx6-	Port 6 Receiver -	Carrier	108	Tx11-	Port 11 Transmitter -	AMC
64	GND	Logic Ground	-	107	GND	Logic Ground	-
65	Tx7+	Port 7 Transmitter +	AMC	106	Rx11+	Port 11 Receiver +	Carrier
66	Tx7-	Port 7 Transmitter -	AMC	105	Rx11-	Port 11 Receiver -	Carrier
67	GND	Logic Ground	-	104	GND	Logic Ground	-
68	Rx7+	Port 7 Receiver +	Carrier	103	Tx10+	Port 10 Transmitter +	AMC
69	Rx7-	Port 7 Receiver -	Carrier	102	Tx10-	Port 10 Transmitter -	AMC
70	GND	Logic Ground	-	101	GND	Logic Ground	-
71	SDA_L	IPMB-L Data	IPMI Agent	100	Rx10+	Port 10 Receiver +	Carrier
72	PWR	Payload Power	Carrier	99	Rx10-	Port 10 Receiver -	Carrier
73	GND	Logic Ground	-	98	GND	Logic Ground	-
74	CLK1+	Synchronization Clock 1+	CLK1 driver	97	Tx9+	Port 9 Transmitter +	AMC
75	CLK1-	Synchronization Clock 1-	CLK1 driver	96	Tx9-	Port 9 Transmitter -	AMC
76	GND	Logic Ground	-	95	GND	Logic Ground	-
77	CLK2+	Synchronization Clock 2+	CLK2 driver	94	Rx9+	Port 9 Receiver +	Carrier
78	CLK2-	Synchronization Clock 2-	CLK2 driver	93	Rx9-	Port 9 Receiver -	Carrier
79	GND	Logic Ground	-	92	GND	Logic Ground	-
80	CLK3+	PCI Express Reference Clock 3+	Carrier	91	Tx8+	Port 8 Transmitter +	AMC
81	CLK3-	PCI Express Reference Clock 3-	Carrier	90	Tx8-	Port 8 Transmitter -	AMC
82	GND	Logic Ground	-	89	GND	Logic Ground	-
83	PS0#	Presence 0	Carrier	88	Rx8+	Port 8 Receiver +	Carrier
84	PWR	Payload Power	Carrier	87	Rx8-	Port 8 Receiver -	Carrier
85	GND	Logic Ground	-	86	GND	Logic Ground	-

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2.5 Module Management

A dedicated Module Management Controller (MMC) on the AM4001 manages the module and supports a defined subset of IPMI commands and sensors. For information on IPMI, refer to the AM4001-IPMI, MMC User Manual (30747_nn_SK-MAN-AM4001-IPMI-MMC-UM) software manual provided with the KIT-AM4001 software and documentation CD.

2.5.1 Module Management Controller

The Module Management Controller is based on the 16-bit H8 microcontroller with two redundant 128 kB Flash blocks and 4 kB RAM. The two redundant 128 kB Flash blocks provide an automatic roll-back strategy to the backup copy, for example, if a Firmware upgrade is interrupted or corrupted. In addition to the code Flash, the field replacement unit (FRU) inventory information is stored in the nonvolatile memory on the EEPROM. It is possible to store up to 4 KB within the FRU inventory information.

The Intel® Pentium® M processor communicates with the MMC using the Keyboard Controller Style (KCS) interface. The base address of the LPC KCS interface is 0xCA2 - 0xCA3 and 0xCA4 - 0xCA5. Furthermore, the MMC is able to communicate directly with the FPGA via the I²C interface. This can be used to read the POST codes and configure the BIOS default boot parameters.

The MMC provides four independent I²C bus interfaces. One interface is used for the IPMB-L bus connection to the carrier, one for LAN connections, one for onboard temperature sensors and FPGA host interface, and one for local EEPROM storage.

The MMC is used to manage the AM4001, for example, it monitors several onboard temperature conditions, board voltages and the power supply status, manages hot swap LEDs and operations, reboots the board, etc. Additionally, the MMC can intervene in the operating status of the system by reading temperature values, shutting down systems, generating alarm signals if fault conditions occur. These fault conditions are simultaneously logged in nonvolatile memory for analysis and for fault recovery.

To provide a reliable system, the AM4001 includes four temperature sensors distributed over the complete board to measure onboard temperature values and regulate the board's power consumption. The AM4001 uses the following temperature sensors:

- Intel® Pentium® M processor die temperature
- E7320 chipset die temperature
- Board temperature near DC/DC converter
- Memory module temperature near DDR2 chips

The MMC also includes an integrated watchdog to protect against CPU lockups. This enhances the board's characteristics and improves the system's reliability.

The MMC Firmware is designed and specially made for AMC environments, and is compliant with the PICMG 3.0 and IPMI v1.5 rev 1.1 specifications.

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2.5.1.1 MMC Signals Implemented on the AM4001

The MMC implements several signals to monitor and control the different board functions. The following tables indicate the signals implemented on the AM4001.

Table 2-15: Processor and Chipset Supervision

SIGNAL	DESCRIPTION	MMC FUNCTION
PCI reset	Status of PCI reset signal	Monitor reset status
Board reset	Reset the complete board	Control reset circuit
S3 Sleep state	Status of chipset sleep state	Monitor sleep state
Processor NMI	Status of processor NMI	Monitor NMI
Processor SMI	Status of processor SMI	Monitor SMI
FWH Flash control	FWH Flash fail-over control	Control FWHs
Post Code	BIOS POST code information from port x80	Monitor BIOS port x80
Boot order	Configure BIOS boot order	Configure boot

Table 2-16: AMC Signals

SIGNAL	DESCRIPTION	MMC FUNCTION
GA[0:2]	Geographic address	Monitor and control
Hot swap LED	Hot swap LED	Control LED
Hot swap switch	Status of hot swap switch	Monitor switch
Module LED	Basic feedback about failures	Control module LED
Debug LED	MMC Debug LED	Debug LED
Gigabit Ethernet 1	Gigabit Ethernet link1 status	Monitor link status
Gigabit Ethernet 2	Gigabit Ethernet link2 status	Monitor link status

Table 2-17: Onboard Power Supply Supervision

SIGNAL	DESCRIPTION	MMC FUNCTION
AMC power enable	Control AMC board supply	Control power supply
Onboard power supply	Status of various onboard supply voltages	Monitor power good signals
Processor power supply	Status of processor supply voltage	Monitor power good
Voltage 0.9 V	DDR termination supply (1%)	Monitor voltage
Voltage 1.5 V	Board 1.5 V supply (1%)	Monitor voltage
Voltage 1.8 V	Board 1.8 V supply (1%)	Monitor voltage
Voltage 3.3 V	Board 3.3 V supply (1%	Monitor voltage
Voltage 5 V	Board 5 V supply (1%)	Monitor voltage
Voltage AMC 3.3 V	AMC management power 3.3 V (1%)	Monitor voltage
Voltage AMC 12 V	AMC payload power 12 V (1%)	Monitor voltage

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Table 2-18: Temperature Signals

SIGNAL	DESCRIPTION	MMC FUNCTION
Processor temperature	Processor die temperature	Monitor temperature
E7320 MCH temperature	E7320 MCH die temperature	Monitor temperature
Board temperature	Board temperature	Monitor temperature
Memory module temperature	Memory module temperature	Monitor temperature
Processor throttling	Thermal over heat indication, processor throttling in action	Monitor processor thermtrip signal
Processor over temperature	Indicates a catastrophic cooling failure processor temperature > 135°C	Monitor processor overtemperature signal
Processor internal thermal monitor	Status of internal thermal monitor	Monitor processor hot signal

Figure 2-7: AM4001 Temperature Sensor Placement

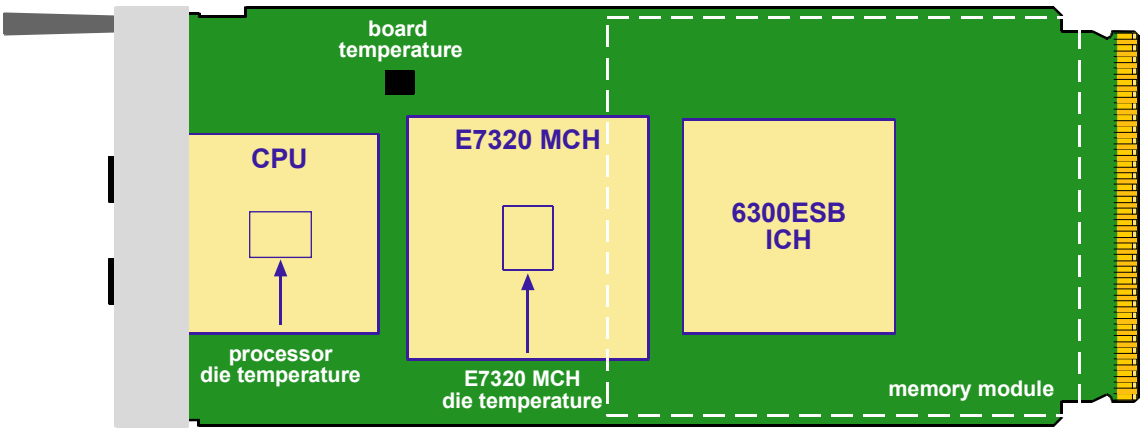
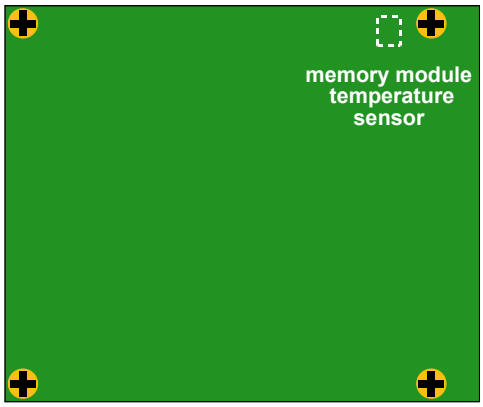


Figure 2-8: Memory Module Temperature Sensor



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Chapter 3

Installation

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3. Installation

The AM4001 has been designed for easy installation. However, the following standard precautions, installation procedures, and general information must be observed to ensure proper installation and to preclude damage to the board, other system components, or injury to personnel.

3.1 Safety Requirements

The following safety precautions must be observed when installing or operating the AM4001. Kontron assumes no responsibility for any damage resulting from failure to comply with these requirements.



Warning!

Due care should be exercised when handling the board due to the fact that the heat sink can get very hot. Do not touch the heat sink when installing or removing the board.

In addition, the board should not be placed on any surface or in any form of storage container until such time as the board and heat sink have cooled down to room temperature.



ESD Equipment!

This AMC board contains electrostatically sensitive devices. Please observe the necessary precautions to avoid damage to your board:

- Discharge your clothing before touching the assembly. Tools must be discharged before use.
- Do not touch components, connector-pins or traces.
- If working at an anti-static workbench with professional discharging equipment, please do not omit to use it.

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3.2 AM4001 Hot Swap Insertion Procedures

The AM4001 is designed for hot swap operation. Hot swapping allows the coordinated insertion and extraction of modules without disrupting other operational elements within the system. This allows for identified faulty elements to be removed and replaced without taking the carrier card out of service that will typically be hosting others modules.

The following procedures are applicable when inserting the AM4001 in a running system.

1. Ensure that the safety requirements indicated section 3.1 are observed.



Warning!

Failure to comply with the instruction above may cause damage to the board or result in improper system operation.

2. Ensure that the board is properly configured for operation in accordance with application requirements before installation. For information regarding the configuration of the AM4001 refer to Chapter 4. For the installation of AM4001 specific peripheral devices devices refer to the appropriate sections in Chapter 3.



Warning!

Care must be taken when applying the procedures below to ensure that neither the AM4001 nor other carrier boards are physically damaged by the application of these procedures.

3. To install the AM4001 perform the following:
   1. Carefully insert the board into the slot designated by the application requirements for the board until it makes contact with the AMC connector located on the carrier.
   2. Connect all external interfacing cables to the board as required.
   3. Using the handle on the front panel, engage the board with the carrier. When the handle is locked, the board is engaged and the following steps occur:
      1. The BLUE LED turns on.
         If the carrier recognizes that the module is fully seated, the carrier then enables the management power for the module and the BLUE LED turns on.
      2. Long blinks of the BLUE LED
         If the carrier detects the module, it sends a command to the module to perform long blinks of the BLUE LED.
      3. The BLUE LED turns off.
         The Intelligent Platform Management Controller on the carrier reads the Module Current Requirements record and AMC Point-to-Point Connectivity record. If the Module FRU information is valid and if the carrier can provide the necessary payload power, the BLUE LED will be turned off. If the module FRU information is invalid or if the carrier cannot provide the necessary payload power, the insertion process is stopped and the BLUE LED keeps blinking. Should this problem occur, please contact Kontron Modular Computers' Technical Support.
      4. Short blinks of the AMC LEDs and module LEDs
         The carrier enables the payload power for the module and the AMC LEDs and module LEDs emit a short blink.
   4. Ensure that the board and all required interfacing cables are properly secured.
4. The AM4001 is now ready for operation. For operation of the AM4001, refer to appropriate AM4001 specific software, application, and system documentation.

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3.3 AM4001 Hot Swap Extraction Procedures

To extract the board proceed as follows:

1. Ensure that the safety requirements indicated in section 3.1 are observed. Particular attention must be paid to the warning regarding the heat sink!
2. Pull the handle on the module's front panel initiating deactivation. This changes the state of the handle to open. Now, the following steps occur.
    1. Short blinks of the BLUE LED
        - When the carrier receives the handle opened event, the carrier sends a command to the MMC in the module with a request to perform short blinks of the BLUE LED. This indicates to the operator that the module is waiting to be deactivated.
        - Now the module waits for a permission from higher level management (Shelf Manager or System Manager) to proceed with the module's deactivation.
        - Once the module receives the permission to continue the deactivation, all used ports are disabled.
        - The Intelligent Platform Management Controller on the Carrier disables the module's Payload Power.
    2. The BLUE LED turns on
       Now the module is ready to be safely extracted.
3. Disconnect any interfacing cables that may be connected to the board.
4. Pull the module out of the slot. Now the carrier disables the management power for the module.



Warning!

Due care should be exercised when handling the board due to the fact that the heat sink can get very hot. Do not touch the heat sink when changing the board.

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3.4 Installation of AM4001 Peripheral Devices

The AM4001 is designed to accommodate several peripheral devices whose installation varies considerably. The following sections provide information regarding installation aspects and not detailed procedures.

3.4.1 USB Device Installation

The AM4001 supports one USB 2.0 host port via the 5-pin Mini USB type A connector and one USB 1.1 port (serial-to-USB converter) via the 5-pin Mini USB type B connector on the front panel.

The two Mini USB connectors used on the AM4001 have different housings and require different adapters/cables in order to be connected to standard USB devices or to the host. Whereas the Mini USB type B connector requires merely a commercial USB cable, the Mini USB type A connector requires a special adapter. The following sections provide detailed information on the respective adapters/cables used with the MinI USB connectors.

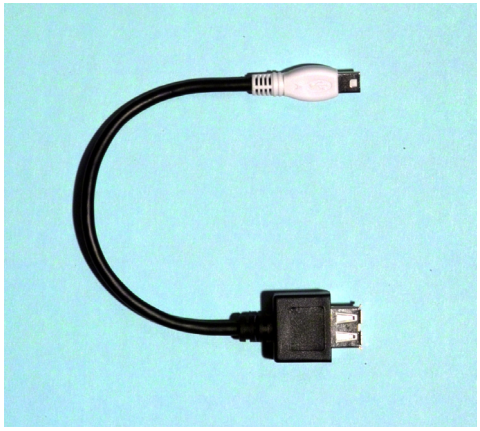
3.4.1.1 Installation of USB 2.0 Host Devices

The AM4001 supports all USB plug and play computer peripherals (e.g. keyboard, mouse, printer, etc.) via the USB 2.0 host port and the adapter described below.

In order to connect standard USB devices with a type A female connector to the Mini USB type A connector, a special adapter is required. For further technical or ordering information on the adapters, please contact Kontron Modular Computers' Technical Support.

The following figure illustrates the adapter required to connect standard USB devices with type A female connector to the Mini USB type A connector.

Figure 3-1: Adapter for Mini USB Type A to USB Type A Male Connector



Note ...

All USB devices may be connected or removed while the host or other peripherals are powered up.

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3.4.1.2 Installation of USB 1.1 Serial-to-USB Device

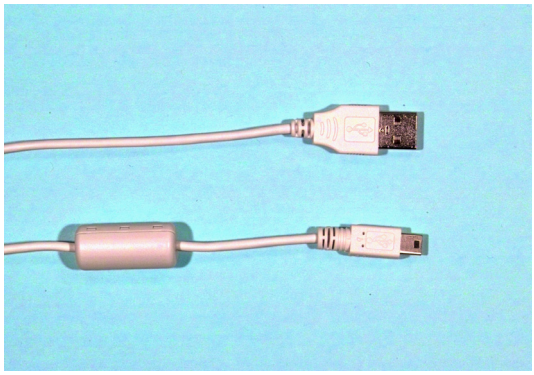
The AM4001 includes one onboard serial-to-USB device accessible via the Mini USB type B connector on the front panel.

The host requires a virtual USB COM port driver in order to communicate with the AM4001. By using this driver, the host's application software regards the serial interface on the AM4001 as standard COM port. On the AM4001, the serial interface to the host is a legacy COM port. Therefore, the AM4001 does not require a driver to communicate with the host.

To connect the Mini USB type B connector to the host, a standard USB type A cable (on the host side) to a Mini USB type B (on the AM4001) is necessary. This cable is a commercial USB cable that can also be used with standard PC devices, such as digital cameras, MP3 players, etc.

The following figure illustrates the cable required to connect the serial-to-USB device to the host USB port.

Figure 3-2: Cable for Mini USB Type B to USB Type A Female Connector



Note ...

The serial-to-USB device may be connected or removed while the AM4001 is powered up.

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3.5 Software Installation

The installation of the Ethernet and all other onboard peripheral drivers is described in detail in the relevant Driver Kit files.

Installation of an operating system is a function of the OS software and is not addressed in this manual. Refer to appropriate OS software documentation for installation.



Note ...

Users working with pre-configured operating system installation images for Plug and Play compliant operating systems must take into consideration that the stepping and revision ID of the chipset and/or other onboard PCI devices may change. Thus, a re-configuration of the operating system installation image deployed for a previous chipset stepping or revision ID is in most cases required. The corresponding operating system will detect new devices according to the Plug and Play configuration rules.

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Chapter 4

Configuration

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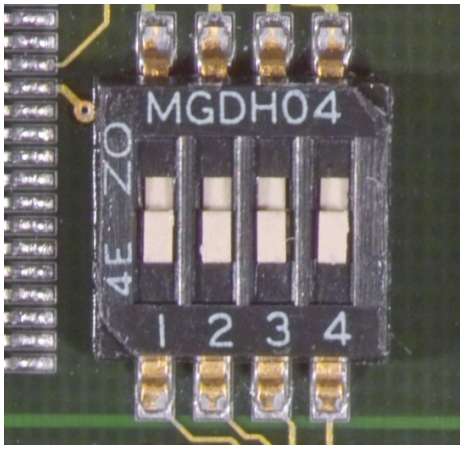
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4. Configuration

4.1 DIP Switch Configuration

The DIP switch consists of four switches for board configuration, namely switch 1 for general purpose LED or POST code display during boot-up, switch 2 for BIOS Firmware Hub Flash configuration, switch 3 for boot order configuration, and switch 4 for clearing the BIOS CMOS parameters.

Figure 4-1: DIP Switch



The following table indicates the functions of the four switches integrated in the DIP switch.

Table 4-1: DIP Switch Functions

SWITCH	FUNCTION
1	General purpose LED or POST code display during boot-up
2	BIOS Firmware Hub configuration
3	Boot order configuration
4	Clearing BIOS CMOS parameters

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4.1.1 General Purpose LED or POST Code Configuration

The general purpose LEDs are available for either general application use or indicating the POST code during boot-up. When POST code is selected, the general purpose LEDs indicate POST code during BIOS boot-up. If it is not required to indicate the POST code, they can be used as general purpose LEDs.

Table 4-2: General Purpose LED or POST Code Configuration

SWITCH 1	DESCRIPTION
OFF	***POST Code***
ON	General Purpose LEDs

The default setting is indicated by using italic bold.

4.1.2 BIOS Firmware Hub Flash Configuration

BIOS Firmware Hub Flash configuration means that there are two chips for the BIOS on the AM4001 board. One chip is intended to provide a backup in the event that the other gets corrupted. If the primary BIOS is corrupted due to physical damage or a faulty Flash upgrade, either the Module Management Controller or the DIP switch can select the 2nd Flash, and the system can boot from it.

Table 4-3: BIOS Firmware Hub Flash Configuration

SWITCH 2	DESCRIPTION
OFF	***Normal boot from the primary BIOS FWH Flash***
ON	Boot from the secondary BIOS FWH Flash

The default setting is indicated by using italic bold.

4.1.3 Boot Order Configuration

Switch 3 enables the user to set the BIOS boot order. For further information on the boot order configuration, refer to section 4.4.1, “BIOS Boot Order Control Register”.

Table 4-4: BIOS Boot Order Configuration

SWITCH 3	DESCRIPTION
OFF	***Boot order configured by the MMC***
ON	Normal BIOS boot order configuration

The default setting is indicated by using italic bold.

4.1.4 Clear BIOS CMOS Configuration

Switch 4 enables the user to clear the BIOS CMOS parameters.

Table 4-5: BIOS CMOS Configuration

SWITCH 4	DESCRIPTION
OFF	***Standard BIOS CMOS parameters***
ON	Clear BIOS CMOS parameters

The default setting is indicated by using italic bold.

AM4001-29143-02-060407-ml

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4.2 Interrupts

The AM4001 board uses the standard AT IRQ routing (8259 controller). This interrupt routing is the default configurations, but it can be modified via the BIOS settings.

Table 4-6: Interrupt Setting

IRQ	PRIORITY	STANDARD FUNCTION
IRQ0	1	System Timer
IRQ1	2	Free (Keyboard Controller)
IRQ2	--	Input of the second IRQ controller (IRQ8-IRQ15)
IRQ3	11	COM2
IRQ4	12	COM1
IRQ5	13	Watchdog
IRQ6	14	Free (Floppy Disk Controller)
IRQ7	15	Module Management Controller
IRQ8	3	System Real Time Clock
IRQ9	4	ACPI
IRQ10	5	Gigabit Ethernet
IRQ11	6	Gigabit Ethernet
IRQ12	7	Free
IRQ13	8	Coprocessor error
IRQ14	9	CompactFlash
IRQ15	10	Free
NMI		Watchdog

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4.3 Memory Map

The AM4001 board uses the standard AT ISA memory map.

4.3.1 Memory Map for the 1st Megabyte

The following table sets out the memory map for the first megabyte.

Table 4-7: Memory Map for the 1st Megabyte

MEMORY RANGE	SIZE	FUNCTION
0xE0000 – 0xFFFFF	128 k	BIOS implemented in Firmware Hub Flash Reset vector 0xFFFF0
0xD0000 – 0xDFFFF	64 k	Free
0xCC000 – 0xCFFFF	16 k	Free
0xC0000 – 0xCBFFF	48 k	Optional BIOS of the VGA card.
0xA0000 – 0xBFFFF	128 k	Normally used as video RAM as follows: CGA video: 0xB8000-0xBFFFF Monochrome video: 0xB0000-0xB7FFF EGA/VGA video: 0xA0000-0xAFFFF
0x000000 – 0x9FFFF	640 k	DOS reserved memory space

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4.3.2 I/O Address Map

The following table sets out the memory map for the I/O memory. The gray shaded table cells indicate AM4001-specific registers. The blue shaded table cells indicate MMC-specific registers.

Table 4-8: I/O Address Map

ADDRESS	DEVICE
0x000 - 0x00F	DMA controller #1
0x020 - 0x021	Interrupt controller #1
0x022 - 0x02F	Reserved
0x040 - 0x043	Timer
0x060 - 0x063	Keyboard interface
0x070 - 0x071	RTC port
0x080	BIOS POST
0x081 - 0x08F	DMA page register
0x0A0 - 0x0B0	Interrupt controller #2
0x0C0 - 0x0DF	DMA controller #2
0x0E0 - 0x0EF	Reserved
0x0F0 - 0x0FF	Math coprocessor
0x170 - 0x17F	Hard disk secondary
0x1F0 - 0x1FF	Hard disk primary
0x19C	MMC configuration register 0
0x19F	MMC interrupt configuration register
0x278 - 0x27F	Parallel port LPT2
0x280	BIOS boot order control register
0x281	Reserved
0x282	Watchdog timer control
0x283	AMC geographic addressing register
0x284	Hardware and logic index register
0x285	Reset status register
0x286	I/O status register
0x287	I/O configuration register
0x288	Board ID register
0x289	Board interrupt configuration register
0x28A	Hot swap status register
0x28B	Module LED configuration register 0
0x28C	AMC LED configuration register 1
0x28D	Module LED control register 0
0x28E	AMC LED control register 1

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Table 4-8: I/O Address Map (Continued)

ADDRESS	DEVICE
0x28F	Delay timer control/status register
0x2E8 - 0x2EF	Serial port COM4
0x2F8 - 0x2FF	Serial port COM2
0x378 - 0x37F	Parallel printer port LPT1
0x3BC - 0x3BF	Parallel printer port LPT3
0x3E8 - 0x3EF	Serial port COM3
0x3F0 - 0x3F7	Floppy Disk
0x3F8 - 0x3FF	Serial port COM1
0xCA2 - 0xCA3	IPMI SMS KCS interface
0xCA4 - 0xCA5	IPMI MSM KCS interface

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4.4 AM4001-Specific Registers

The following registers are special registers which the AM4001 uses to watch the onboard hardware special features and the AMC control signals.

Normally, only the system BIOS uses these registers, but they are documented here for application use as required.



Note ...

Take care when modifying the contents of these registers as the system BIOS may be relying on the state of the bits under its control.

4.4.1 BIOS Boot Order Control Register

The BIOS boot order control register is used to set the BIOS boot order. This register is read only and can be configured only by the MMC.

Table 4-9: BIOS Boot Order Control Register

REGISTER NAME		BIOS BOOT ORDER CONTROL REGISTER						SIZE	
ADDRESS		0x280						8 bits	
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		Res.	Res.	Res.	Res.	BOOT3	BOOT2	BOOT1	BOOT0
DEFAULT		0	0	0	0	0	0	0	0
ACCESS		R	R	R	R	R	R	R	R
BIT	NAME	DESCRIPTION / FUNCTION							
7 - 4	Res.	Reserved							
3 - 0	BOOT[3:0]	BIOS boot order settings: 0000 Default BIOS configuration (see note below) 0001 Ethernet boot 0010 CompactFlash 0011 External SATA device							



Note ...

The BIOS boot order control register is set to the default values by power-on reset, not by PCI reset. The BIOS boot order can also be set in the BIOS.

If the DIP switch 3 is OFF, the boot order is configured to the default value configured in the BIOS.

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4.4.2 Watchdog Timer Control Register

The AM4001 has one watchdog timer provided with a programmable timeout ranging from 125 msec to 256 sec. Failure to strobe the watchdog timer within a set time period results in a system reset, NMI or an interrupt. The NMI and interrupt mode can be configured via the board interrupt configuration register (0x289).

There are four possible modes of operation involving the watchdog timer:

- Timer only mode
- Reset mode
- Interrupt mode
- Dual stage mode

At power on the watchdog is not enabled. If not required, it is not necessary to enable it. If required, the bits of the watchdog control register (0x282) must be set according to the application requirements. To operate the watchdog, the mode and time period required must first be set and then the watchdog enabled. Once enabled, the watchdog can only be disabled or the mode changed by powering down and then up again. To prevent a watchdog timeout, the watchdog must be retriggered before timing out. This is done by writing a ’1’ to the WTR bit. In the event a watchdog timeout does occur, the WTE bit is set to ’1’. What transpires after this depends on the mode selected.

The four operational watchdog timer modes can be configured by the WMD[1:0] bits, and are described as follows:

Timer only mode - In this mode the watchdog is enabled using the required timeout period. Normally, the watchdog is retriggered by writing a ’1’ to the WTR bit. In the event a timeout occurs, the WTE bit is set to ’1’. This bit can then be polled by the application and handled accordingly. To continue using the watchdog, write a ’1’ to the WTE bit, and then retrigger the watchdog using WTR. The WTE bit retains its setting as long as no power down-up is done. Therefore, this bit may be used to verify the status of the watchdog.

Reset mode - This mode is used to force a hard reset in the event of a watchdog timeout. To be effective, the hard reset must not be masked or otherwise negated. In addition, the WTE bit is not reset by the hard reset, which makes it available if necessary to determine the status of the watchdog prior to the reset.

Interrupt mode - This mode causes the generation of an interrupt in the event of a watchdog timeout. The interrupt handling is a function of the application. If required, the WTE bit can be used to determine if a watchdog timeout has occurred.

Dual stage mode - This is a complex mode where in the event of a timeout two things occur: 1) an interrupt is generated, and 2) the watchdog is retriggered automatically. In the event a second timeout occurs immediately following the first timeout, a hard reset will be generated. If the watchdog is retriggered normally, operation continues. The interrupt generated at the first timeout is available to the application to handle the first timeout if required. As with all of the other modes, the WTE bit is available for application use.

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Table 4-10: Watchdog Timer Control Register

REGISTER NAME		WATCHDOG TIMER CONTROL REGISTER						SIZE	
ADDRESS		0x282						8 bits	
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		WTE	WMD1	WMD0	WEN/WTR	WTM3	WTM2	WTM1	WTM0
DEFAULT		0	0	0	0	0	0	0	0
ACCESS		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
BIT	NAME	DESCRIPTION / FUNCTION							
7	WTE	Watchdog timer expired status bit: 0 Watchdog timer has not expired 1 Watchdog timer has expired. Writing a '1' to this bit resets it to 0.							
6 - 5	WMD[1:0]	Watchdog mode settings: **WMD1 WMD0 Mode** 0 0 Timer only 0 1 Reset 1 0 Interrupt 1 1 Dual Stage							
4	WEN/WTR	Watchdog enable / watchdog trigger control bit: 0 Watchdog timer has not been enabled Prior to the watchdog being enabled, this bit is known as WEN. After the watchdog is enabled, it is known as WTR. Once the watchdog timer has been enabled, this bit cannot be reset to 0. As long as the watchdog timer is enabled, it will indicate a '1'. 1 Watchdog timer is enabled Writing a '1' to this bit causes the watchdog to be retriggered to the timer value indicated by bits WTM[3:0].							
3 - 0	WTM[3:0]	Watchdog timeout time settings: **WTM3 WTM2 WTM1 WTM0 Value** 0 0 0 0 125 ms 0 0 0 1 250 ms 0 0 1 0 500 ms 0 0 1 1 1 s 0 1 0 0 2 s 0 1 0 1 4 s 0 1 1 0 8 s 0 1 1 1 16 s 1 0 0 0 32 s 1 0 0 1 64 s 1 0 1 0 128 s 1 0 1 1 256 s 1 1 0 0 reserved 1 1 0 1 reserved 1 1 1 0 reserved 1 1 1 1 reserved The nominal timeout period is 5% longer than the above-stated values.							

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4.4.3 AMC Geographic Addressing Register

This register holds the AMC geographic address (site number) used to assign the Intelligent Platform Management Bus (IPMB) address to the AM4001.

Table 4-11: Geographic Addressing Register

REGISTER NAME		GEOGRAPHIC ADDRESSING REGISTER						SIZE	
ADDRESS		0x283						8 bits	
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		Res.	Res.	Res.	Res.	GA3	GA2	GA1	GA0
DEFAULT		0	0	0	0	0	0	0	0
ACCESS		R	R	R	R	R	R	R	R
BIT	NAME	DESCRIPTION / FUNCTION							
7 - 4	Res.	Reserved							
3 - 0	GA[3:0]	Geographic address							



Note ...

The AMC geographic addressing register is set to the default values by power-on reset, not by PCI reset.

4.4.4 Hardware and Logic Revision Index Register

The hardware and logic revision index register signals to the software when differences in the hardware require different handling by the software. It starts with the value 0x00 for the initial board prototypes and will be incremented with each change in hardware as development continues.

Table 4-12: Hardware and Logic Index Revision Index Register

REGISTER NAME		HARDWARE AND LOGIC REVISION INDEX REGISTER						SIZE	
ADDRESS		0x284						8 bits	
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		HWRI3	HWRI2	HWRI1	HWRI0	LRI3	LRI2	LRI1	LRI0
DEFAULT		0	0	0	0	0	0	0	0
ACCESS		R	R	R	R	R	R	R	R
7 - 4	HWRI[3:0]	Hardware revision ID: 0000 Index 0000							
3 - 0	LRI[3:0]	Logic revision ID: 0000 Index 0000							

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4.4.5 Reset Status Register

The reset status register is used to determine the reset source.

Table 4-13: Reset Status Register

REGISTER NAME		RESET STATUS REGISTER						SIZE	
ADDRESS		0x285						8 bits	
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		Res.	Res.	Res.	Res.	MRST	FRST	Res.	WRST
DEFAULT		0	0	0	0	0	0	0	0
ACCESS		R	R	R	R	R/WC*	R/WC*	R	R/WC*
BIT	NAME	DESCRIPTION / FUNCTION							
7 - 4	Res.	Reserved							
3	MRST	0 System reset generated by power-on reset 1 System reset generated by MMC							
2	FRST	0 System reset generated by power-on reset 1 System reset generated by front panel reset							
1	Res.	Reserved							
0	WRST	0 System reset generated by power-on reset 1 System reset generated by watchdog							

* Read/Write Clear. Writing a '1' to this bit clears the bit.



Note ...

The reset status register is set to the default values by power-on reset, not by PCI reset.

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4.4.6 I/O Status Register

This register describes the onboard and AMC control signals.

Table 4-14: I/O Status Register

REGISTER NAME		I/O STATUS REGISTER						SIZE	
ADDRESS		0x286						8 bits	
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		Res.	Res.	FSTA1	FSTA0	Res.	Res.	Res.	Res.
DEFAULT		0	0	0	0	0	0	0	0
ACCESS		R	R	R	R	R	R	R	R
BIT	NAME	DESCRIPTION / FUNCTION							
7 - 6	Res.	Reserved							
5 - 4	FSTA[1:0]	These bits indicate the active BIOS Firmware Hub Flash status: 00 BIOS boot from FWH0 01 BIOS boot from FWH1 10 BIOS boot from external Firmware Flash on I/O extension connector							
3 - 0	Res.	Reserved							

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4.4.7 I/O Configuration Register

The I/O configuration register holds a series of bits defining the onboard configuration.

Table 4-15: I/O Configuration Register

REGISTER NAME		I/O CONFIGURATION REGISTER						SIZE	
ADDRESS		0x287						8 bits	
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		THA	PLED	FSEL	Res.	EKC	Res.	Res.	Res.
DEFAULT		0	0	0	0	0	0	0	0
ACCESS		R/W	R/W	R/W	R	R/W	R	R	R
BIT	NAME	DESCRIPTION / FUNCTION							
7	THA	This bit is used to enable/disable the thermal throttling of the processor in case of overtemperature: 0 Disabled 1 Enabled							
6	PLED	Module LED configuration after booting: 0 Enabled (POST code information is displayed via the module LEDs) 1 Disabled (no POST code information is displayed)							
5	FSEL	With this bit, the active Firmware Hub Flash can be selected: 0 FWH0 is active 1 FWH1 is active In addition, the MMC and the DIP switch can also change the selection of the Firmware Hub Flash.							
4	Res.	Reserved							
3	EKC	Port 60/64 emulation: 0 Disable keyboard controller emulation 1 Enable keyboard controller emulation							
2 - 0	Res.	Reserved							

4.4.8 Board ID Register

This register describes the hardware and the board index. The content of this register is unique for each Kontron AMC board.

Table 4-16: Board ID Register

REGISTER NAME		BOARD ID REGISTER						SIZE	
ADDRESS		0x288						8 bits	
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		BID7	BID6	BID5	BID4	BID3	BID2	BID1	BID0
DEFAULT		1	0	1	0	0	0	0	0
ACCESS		R	R	R	R	R	R	R	R
7 - 0	BID[7:0]	Board ID: 0xA0 AM4001							

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4.4.9 Board Interrupt Configuration Register

The board interrupt configuration register holds a series of bits defining the interrupt routing for the watchdog. If the watchdog timer fails, it can generate two independent hardware events: NMI and IRQ5 interrupt.

Table 4-17: Board Interrupt Configuration Register

REGISTER NAME		BOARD INTERRUPT CONFIGURATION REGISTER						SIZE	
ADDRESS		0x289						8 bits	
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		Res.	Res.	Res.	Res.	Res.	Res.	WIRQ1	WIRQ0
DEFAULT		0	0	0	0	0	0	0	0
ACCESS		R	R	R	R	R	R	R/W	R/W
BIT	NAME	DESCRIPTION / FUNCTION							
7 - 2	Res.	Reserved							
1 - 0	WIRQ[1:0]	Watchdog interrupt routing: 11 NMI 10 Reserved 01 IRQ5 00 Disabled							

4.4.10 Hot Swap Status Register

The hot swap status register describes the AMC hot swap handle status.

Table 4-18: Hot Swap Status Register

REGISTER NAME		HOT SWAP STATUS REGISTER						SIZE	
ADDRESS		0x28A						8 bits	
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		Res.	HSH	Res.	Res.	Res.	Res.	Res.	Res.
DEFAULT		0	0	0	0	0	0	0	0
ACCESS		R	R	R	R	R	R	R	R
BIT	NAME	DESCRIPTION / FUNCTION							
7	Res.	Reserved							
6	HSH	0 AMC hot swap handle in closed position 1 AMC hot swap handle in open position							
5 - 0	Res.	Reserved							

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4.4.11 Module LED Configuration Register 0

The module LED configuration register 0 holds a series of bits defining the onboard configuration for the front panel module LEDs.

Table 4-19: Module LED Configuration Register 0

REGISTER NAME		MODULE LED CONFIGURATION REGISTER 0						SIZE	
ADDRESS		0x28B						8 bits	
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		Res.	Res.	Res.	Res.	CMLED3	CMLED2	CMLED1	CMLED0
DEFAULT		0	0	0	0	0	0	0	0
ACCESS		R	R	R	R	R/W	R/W	R/W	R/W
BIT	NAME	DESCRIPTION / FUNCTION							
7 - 4	Res.	Reserved							
3	CMLED3	Module LED3 configuration: 0 MMC debug LED 1 General purpose LED							
2	CMLED2	Module LED2 configuration: 0 SATA and CompactFlash activity 1 General purpose LED							
1	CMLED1	Module LED1 configuration: 0 Ethernet port 1 link signal 1 General purpose LED							
0	CMLED0	Module LED0 configuration: 0 Ethernet port 0 link signal 1 General purpose LED							

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4.4.12 AMC LED Configuration Register 1

The AMC LED configuration register 1 holds a series of bits defining the onboard configuration for the front panel AMC LEDs.

Table 4-20: AMC LED Configuration Register 1

REGISTER NAME		AMC LED CONFIGURATION REGISTER 1						SIZE	
ADDRESS		0x28C						8 bits	
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		Res.	Res.	Res.	Res.	CALED3	CALED2	Res.	Res.
DEFAULT		0	0	0	0	0	0	0	0
ACCESS		R	R	R	R	R/W	R/W	R	R
BIT	NAME	DESCRIPTION / FUNCTION							
7 - 4	Res.	Reserved							
3	CALED3	AMC LED3 configuration: 0 Overtemperature 1 General purpose LED							
2	CALED2	AMC LED2 configuration: 0 Watchdog 1 General purpose LED							
1 - 0	Res.	Reserved							

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4.4.13 Module LED Control Register 0

The module LED control register 0 enables the user to switch on and off the front panel module LEDs.

Table 4-21: Module LED Control Register 0

REGISTER NAME		MODULE LED CONTROL REGISTER 0						SIZE	
ADDRESS		0x28D						8 bits	
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		Res.	Res.	Res.	Res.	MLED3	MLED2	MLED1	MLED0
DEFAULT		0	0	0	0	0	0	0	0
ACCESS		R	R	R	R	R/W	R/W	R/W	R/W
BIT	NAME	DESCRIPTION / FUNCTION							
7 - 4	Res.	Reserved							
3	MLED3	Module LED3 control settings: 0 LED off 1 LED on							
2	MLED2	Module LED2 control settings: 0 LED off 1 LED on							
1	MLED1	Module LED1 control settings: 0 LED off 1 LED on							
0	MLED0	Module LED0 control settings: 0 LED off 1 LED on							



Note ...

This register can only be used if the Module LEDs indicated in the “Module LED Configuration Register 0” (table 4-19) are configured as General Purpose LEDs.

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4.4.14 AMC LED Control Register 1

The AMC LED control register 1 enables the user to switch on and off the AMC LED2 (amber) and AMC LED3 (green) on the front panel.

Table 4-22: AMC LED Control Register 1

REGISTER NAME		AMC LED CONTROL REGISTER 1						SIZE	
ADDRESS		0x28E						8 bits	
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		Res.	Res.	Res.	Res.	ALED3	ALED2	Res.	Res.
DEFAULT		0	0	0	0	0	0	0	0
ACCESS		R	R	R	R	R/W	R/W	R	R
BIT	NAME	DESCRIPTION / FUNCTION							
7 - 4	Res.	Reserved							
3	ALED3	AMC LED3 control settings: 0 LED off 1 LED on							
2	ALED2	AMC LED2 control settings: 0 LED off 1 LED on							
0 - 1	Res.	Reserved							



Note ...

This register can only be used if the AMC LEDs indicated in the “AMC LED Configuration Register 1” (table 4-20) are configured as General Purpose LEDs.

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4.4.15 Delay Timer Control/Status Register

The delay timer enables the user to realize short, reliable delay times. It runs by default and does not start again on its own. It can be restarted at anytime by writing anything else then a ’0’ to the delay timer control/status register. The hardware delay timer provides a set of outputs for defined elapsed time periods. The timer outputs reflected in the delay timer control/status register are set consecutively and remain set until the next restart is triggered again.

Table 4-23: Delay Timer Control/Status Register

REGISTER NAME		DELAY TIMER CONTROL/STATUS REGISTER						SIZE	
ADDRESS		0x28F						8 bits	
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		DTC7	DTC6	DTC5	DTC4	DTC3	DTC2	DTC1	DTC0
DEFAULT		0	0	0	0	0	0	0	0
ACCESS		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
BIT	NAME	DESCRIPTION/FUNCTION							
7 - 0	DTC[7:0]	The hardware delay timer is operated via one simple 8-bit control/status register. During normal operation, each of the 8 bits reflects a timer output which means defined elapsed time period after the last restart according to the following bit mapping: **DTC[7:0] Value Accuracy** Bit 0: 1 µs < + 40% Bit 1: 5 µs < + 8% Bit 2: 10 µs < + 4% Bit 3: 50 µs < + 0.8% Bit 4: 100 µs < + 0.4% Bit 5: 250 µs < + 0.16% Bit 6: 0.5 ms < + 0.08% Bit 7: 1 ms < + 0.04%							

Since the timer width and thus the availability of outputs varies over different implementations, it is necessary to be able to determine the timer capability. Therefore, writing a ’0’ to the delay timer control/status register followed by reading indicates the timer capability (not the timer outputs). For example, writing 0x00 and then reading 0xFF results in a 8-bit wide timer register. This status register mode can be switched off to normal timer operation by writing anything else then a ’0’ to this register.

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4.5 MMC-Specific Registers

The following registers are special registers which the AM4001 uses to monitor and configure the Module Management Controller.

4.5.1 MMC Configuration Register 0

The MMC configuration register 0 holds a series of bits defining the serial port routing and MMC configuration.

Table 4-24: MMC Configuration Register 0

REGISTER NAME		MMC CONFIGURATION REGISTER 0						SIZE	
ADDRESS		0x19C						8 bits	
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		MFUC	Res.	Res.	Res.	MTCOM	MCOM	MRST	MFUM
DEFAULT		0	0	0	0	1	0	0	0
ACCESS		R/W	R	R	R	R	R/W	R/W	R/W
BIT	NAME	DESCRIPTION / FUNCTION							
7	MFUC	MMC Firmware update configuration: 0 No MMC Firmware update 1 MMC Firmware updates the internal Flash from the external Flash							
6 - 4	Res.	Reserved							
3	MTCOM	MMC COM port configuration for debugging: 0 MMC COM port is connected to the serial-to-USB converter 1 MMC COM port is isolated							
2	MCOM	MMC COM port configuration for Firmware update (this bit is ignored if the MTCOM signal is 0): 0 6300ESB COM2 port is disabled 1 6300ESB COM2 port is connected to MMC							
1	MRST	MMC reset function: 0 MMC controller is running 1 Reset MMC controller							
0	MFUM	MMC Firmware update mode: 0 Set normal operating mode 1 Set MMC controller in Firmware update mode							

To allow updating the Firmware of the MMC controller, the software must set MRST and MFUM, and clear MRST after 10 msec. Now, the microcontroller boots from COM2. After programming is completed, MRST must be set and MFUM must be cleared. After 10 msec, MRST must be cleared again. The microcontroller now boots from its own Flash. To allow updating the Firmware of the MMC controller during regular Firmware operation, the software may use the appropriate FirmWare Upgrade Manager (FWUM) commands. FWUM API is the Kontron extension to the IPMI commands set and is available via both the KCS and IPMB-L interfaces.

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The following table indicates the Firmware update functions.

Table 4-25: Firmware Update Functions

MFUM	MCOM	MTCOM	MMC COM PORT	6300ESB COM2 PORT
0	0	1	Disabled	Disabled
0	1	1	6300ESB COM2	MMC
0	--	0	Serial-to-USB converter	Disabled
1	--	--	6300ESB COM2	MMC



Note ...

Setting MFUM inhibits the functionality of MCOM and MTCOM.

4.5.2 MMC Interrupt Configuration Register

The MMC interrupt configuration register holds a series of bits defining the interrupt routing for the MMC controller.

Table 4-26: MMC Interrupt Configuration Register

REGISTER NAME		MMC INTERRUPT CONFIGURATION REGISTER						SIZE	
ADDRESS		0x19F						8 bits	
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		Res.	Res.	Res.	Res.	Res.	MMC7	Res.	MMCS
DEFAULT		0	0	0	0	0	0	0	0
ACCESS		R	R	R	R	R	R/W	R	R/W
BIT	NAME	DESCRIPTION / FUNCTION							
7 - 3	Res.	Reserved							
2	MMC7	MMC ISA-style IRQ routing: 0 Disable IRQ7 1 Enable IRQ7							
1	Res.	Reserved							
0	MMCS	MMC SMI routing: 0 Disable SMI 1 Enable SMI							

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4.5.3 IPMI Keyboard Control Style Interface

The host processor communicates with the MMC using two Keyboard Control Style interfaces, which are defined in the IPMI specification. One interface is for the System Management Software (SMS) used within an operating system, and one for the System Management Mode (SMM) used only by the BIOS.

The KCS interface for the system management software is on the I/O location 0xCA2 and 0xCA3, and configured as regular ISA interrupt.

The KCS interface for the system management mode is on the I/O location 0xCA4 and 0XCA5, and configured as SMI interrupt.

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Chapter 5

BIOS

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5. BIOS

Detailed information concerning the BIOS for the AM4001 is contained in Appendix B.

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Chapter 6

Power Considerations

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6. Power Considerations

6.1 AM4001 Voltage Ranges

The AM4001 board itself has been designed for optimal power input and distribution. Still it is necessary to observe certain criteria essential for application stability and reliability.

The AM4001 requires two power sources, the module management power for the MMC, and a single payload power (typical 12V) for the module components. The payload power can be converted on the module to any voltage required.

The following table specifies the ranges for the different input power voltages within which the board is functional. The AM4001 is not guaranteed to function if the board is not operated within the operating range.

Table 6-1: DC Operational Input Voltage Ranges

INPUT SUPPLY VOLTAGE	ABSOLUTE RANGE	OPERATING RANGE
Payload Power	10.0 V min. to 14.0 V max.	10.8 V min. to 13.2 V max.
Module Management Power	2.97 V min. to 3.63 V. max. (±10%)	3.135 V min. to 3.465 V max. (±5%)



Warning!

The AM4001 must not be operated beyond the absolute range indicated in the table above. Failure to comply with the above may result in damage to your board.

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6.2 Carrier Power Requirements

6.2.1 Payload Power

Payload power is the power provided to the module from the carrier for the main function of the module. It is recommended that payload power voltage be designed at the higher end of the specified voltage range under no load conditions so that under high load conditions the current will be as low as possible. The continuous current limit value is based on the power limit of 60 W per module at the minimum supply value. The maximum current value for the payload power is derived from a 25% derating of the connector pins, which allow a total of 6.0 A (0.75 A per pin; 8 pins).

The payload power voltage shall be at least 10.8 V and not more than 13.2 V at the module contacts during normal conditions under all loads (see table 6-1, “DC Operational Input Voltage Ranges”). The bandwidth-limited periodic noise due to switching power supplies or any other source shall not exceed 200 mV peak to peak.

6.2.2 Voltage Ramp

Power supplies must comply with the following guidelines, in order to be used with the AM4001:

- Beginning at 10% of the nominal output voltage, the voltage must rise within > 0.1 ms to < 20 ms to the specified regulation range of the voltage. Typically: > 5 ms to < 15 ms.
- There must be a smooth and continuous ramp of each DC output voltage from 10% to 90% of the regulation band.

The slope of the turn-on waveform shall be a positive, almost linear voltage increase and have a value from 0 V to nominal Vout.

6.2.3 Management Power

The module management power is only used for the MMC, which has a very low power consumption. The management power voltage measured on the AMC at the connector shall be 3.3 V ± 5% and the maximum current is 150 mA (see table 6-1, “DC Operational Input Voltage Ranges”).

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6.3 Power Consumption of the AM4001

The goal of this description is to provide a method to calculate the power consumption for the AM4001 board with different configurations and applications. The Intel® Celeron® M and Pentium® M processors and the memory dissipate the majority of the thermal power.

The power consumption tables below list the voltage and power specifications for the AM4001 board using Intel® Celeron® M and Pentium® M processors. The values were measured using an AMC carrier with two power supplies: one for the AM4001 module, and the other for the hard disk and the peripheral devices. The operating systems used were BIOS/DOS and Linux/Windows® 2000. All measurements were conducted at a temperature of 25°C with a typical payload power of 12 V. The module management power is below 0.3 W and, therefore, it was not considered in these measurements. The measured values varied, because the power consumption was dependent on processor and memory module activity.

6.3.1 Power Consumption Using Intel® Celeron® M

The following table indicates the power consumption using Intel® Celeron® M 1.0 GHz with 1 GB and 2 GB memory module and the following operating systems:

- BIOS/DOS
- Linux/Windows® 2000 IDLE Mode
- Linux/Windows® 2000 100% CPU Usage
- Linux/Windows® 2000 Memory Test
- Windows® 2000 Intel® High-Power Tool

Table 6-2: Power Consumption Intel® Celeron® M, 1.0 GHz

MEMORY MODULE	BIOS/DOS	LINUX/WIN® 2000 IDLE MODE	LINUX/WIN® 2000 100% CPU USAGE	LINUX/WIN® 2000 MEMORY TEST	WIN® 2000 INTEL® HIGH-POWER TOOL
1 GB	18 - 19 W	17 - 18 W	18 - 20 W	20 - 23 W	21 - 22 W
2 GB	20 - 21 W	20 - 21 W	20 - 22 W	25 - 28 W	22 - 23 W



Note ...

The power consumption using Windows® 2000 and the Intel® High-Power Tool was measured with the processor running at a maximum power consumption (no real application). The Intel® High-Power Tool serves only for testing the onboard power supplies. Therefore, these values do not represent the power consumption of the AM4001 during normal operation.

A high power consumption was reached during memory tests as well, which is due to the fact the entire memory range was stressed.

In normal software applications these maximum power consumption levels will never be reached.

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6.3.2 Power Consumption Using Intel® Pentium® M

The following tables indicate the power consumption using Intel® Pentium® M 1.4 GHz, 1.8 GHz, 2.0 GHz with 1 GB and 2GB memory module and the following operating systems:

- BIOS/DOS
- Linux/Windows® 2000 IDLE Mode
- Linux/Windows® 2000 100% CPU Usage
- Linux/Windows® 2000 Memory Test
- Windows® 2000 Intel® High-Power Tool

Table 6-3: Power Consumption Intel® Pentium® M, 1.4 GHz

MEMORY MODULE	BIOS/DOS	LINUX/WIN® 2000 IDLE MODE	LINUX/WIN® 2000 100% CPU USAGE	LINUX/WIN® 2000 MEMORY TEST	WIN® 2000 INTEL® HIGH-POWER TOOL
1 GB	22 - 23 W	18 - 19 W	22 - 24 W	25 - 28 W	25 - 27 W
2 GB	24 - 25 W	20 - 21 W	24 - 26 W	29 - 32 W	27 - 29 W

Table 6-4: Power Consumption Intel® Pentium® M, 1.8 GHz

MEMORY MODULE	BIOS/DOS	LINUX/WIN® 2000 IDLE MODE	LINUX/WIN® 2000 100% CPU USAGE	LINUX/WIN® 2000 MEMORY TEST	WIN® 2000 INTEL® HIGH-POWER TOOL
1 GB	29 - 30 W	22 - 23 W	30 - 32 W	33 - 36 W	35 - 37 W
2 GB	31 - 32 W	24 - 25 W	32 - 34 W	36 - 39 W	36 - 40 W

Table 6-5: Power Consumption Intel® Pentium® M, 2.0 GHz

MEMORY MODULE	BIOS/DOS	LINUX/WIN® 2000 IDLE MODE	LINUX/WIN® 2000 100% CPU USAGE	LINUX/WIN® 2000 MEMORY TEST	WIN® 2000 INTEL® HIGH-POWER TOOL
1 GB	32 - 33 W	24 - 25 W	34 - 36 W	38 - 41 W	40 - 43 W
2 GB	34 - 35 W	25 - 27 W	36 - 38 W	41 - 45 W	42 - 46 W



Note ...

The power consumption using Windows® 2000 and the Intel® High-Power Tool was measured with the processor running at a maximum power consumption (no real application). The Intel® High-Power Tool serves only for testing the onboard power supplies. Therefore, these values do not represent the power consumption of the AM4001 during normal operation.

A high power consumption was reached during memory tests as well, which is due to the fact the entire memory range was stressed.

In normal software applications these maximum power consumption levels will never be reached.

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6.4 Start-Up Current of the AM4001

The following tables indicate the start-up current of the AM4001 during the first 2-3 seconds after the payload power has been switched on. The power consumption of the AM4001 during operation is indicated in tables 6-2 to 6-5.

Table 6-6: Start-Up Current of the AM4001 with Intel® Celeron® M Processor

PAYLOAD POWER	MEMORY MODULE	INTEL® CELERON® M 1.0 GHz
12 V (average)	1 GB	1.6 A
	2 GB	1.7 A

Table 6-7: Start-Up Current of the AM4001 with Intel® Pentium® M Processor

PAYLOAD POWER	MEMORY MODULE	INTEL® PENTIUM® M 1.4 GHz	INTEL® PENTIUM® M 1.8 GHz	INTEL® PENTIUM® M 2.0 GHz
12 V (average)	1 GB	1.6 A	1.6 A	1.7 A
	2 GB	1.7 A	1.8 A	1.9 A

For further information on the start-up current, contact Kontron Modular Computers' Technical Support.

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Appendix A

AMIBIOS8

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A. AMIBIOS8

Attached to this appendix is the original AMIBIOS8 description as modified by Kontron Modular Computers for the AM4001.

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AM4001 Setup for AMIBIOS8

MAN-EZP-80
07/12/02

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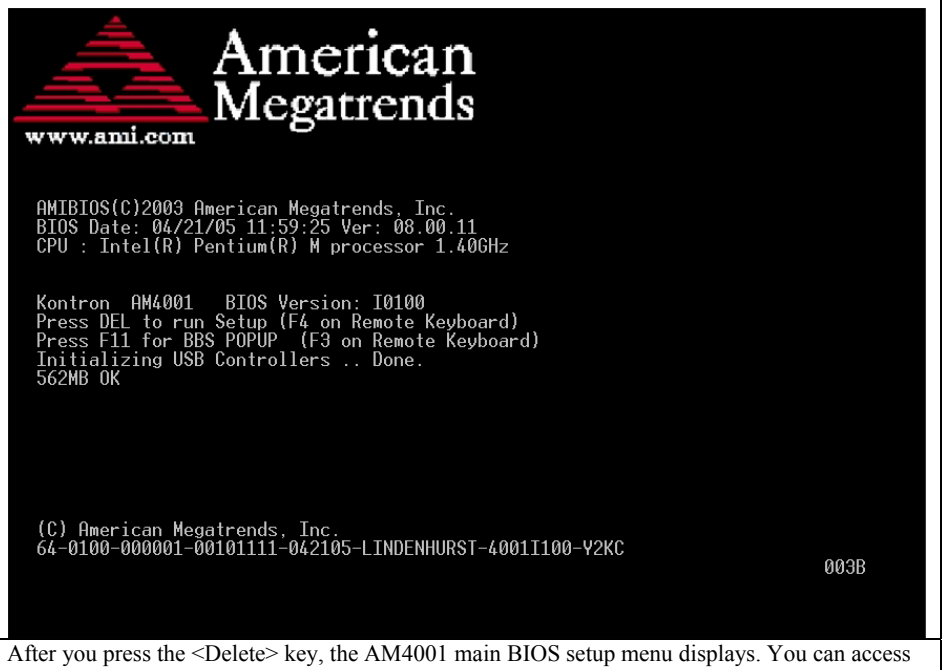
Chapter 1 Starting AM4001

AMIBIOS has been integrated into many motherboards for over a decade. In the past, people often referred to the AMIBIOS setup menu as BIOS, BIOS setup, or CMOS setup.

With the AMIBIOS **Setup** program, you can modify BIOS settings and control the special features of your computer. The Setup program uses a number of menus for making changes and turning the special features on or off.
Kontron refers to this setup as AM4001. This chapter describes the basic navigation of the AM4001 setup screens.

Starting AM4001

To enter the AM4001 setup screens, follow the steps below:

Step	Description
1	Power on the motherboard
2	Press the <Delete> key on your keyboard when you see the following text prompt: `Press DEL to run Setup` 
3	After you press the <Delete> key, the AM4001 main BIOS setup menu displays. You can access the other setup screens from the main BIOS setup menu, such as the Chipset and Power menus.

Note: This manual describes the standard look of the AM4001setup screen. The motherboard manufacturer has the ability to change any and all of the settings described in this manual. This means that some of the options described in this manual do not exist in your motherboard's AMIBIOS.

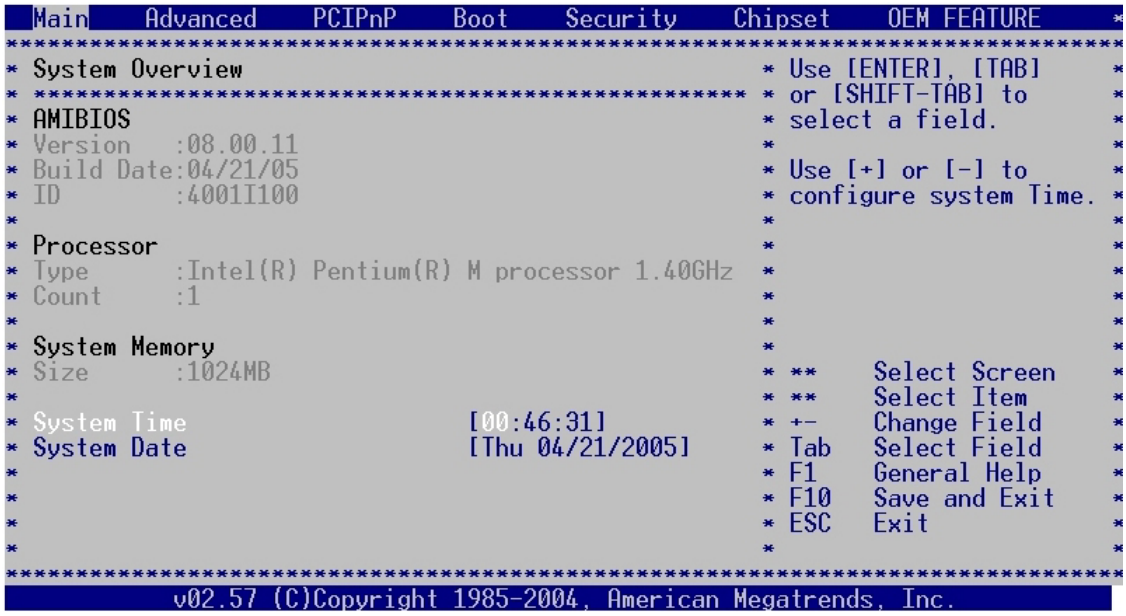
Note: In most cases, the <Delete> key is used to invoke the AM4001setup screen. There are a few cases that other keys are used, such as <F1>, <F2>, and so on.

AM4001 Setup Menu

The AM4001main BIOS setup menu is the first screen that you can navigate. Each main BIOS setup menu option is described in this user's guide.

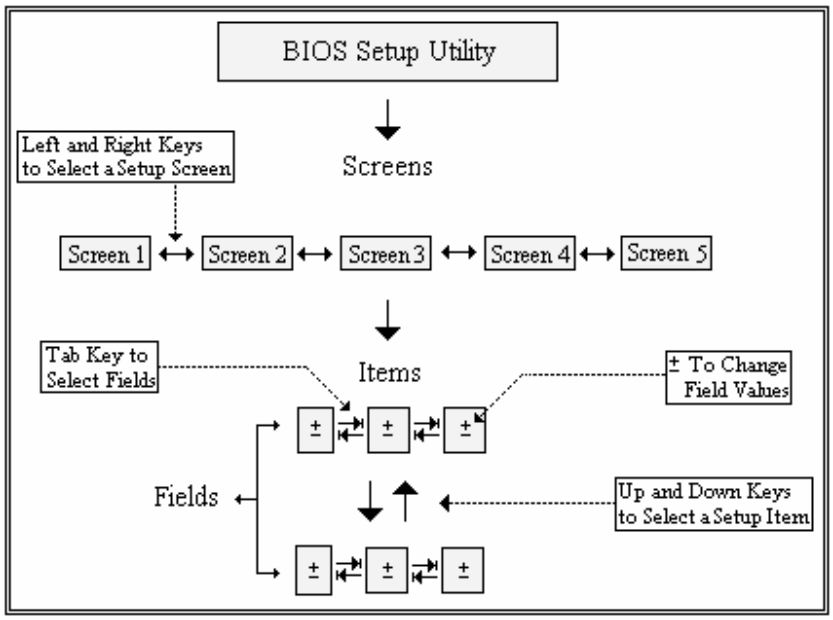
The Main BIOS setup menu screen has two main frames. The left frame displays all the options that can be configured. "Grayed-out" options cannot be configured. Options is blue can be.

The right frame displays the key legend. Above the key legend is an area reserved for a text message. When an option is selected in the left frame, it is highlighted in white. Often a text message will accompany it.



Navigation

The AM4001BIOS setup/utility uses a key-based navigation system called hot keys. Most of the AM4001BIOS setup utility hot keys can be used at any time during the setup navigation process. These keys include <F1>, <F10>, <Enter>, <ESC>, <Arrow> keys, and so on.

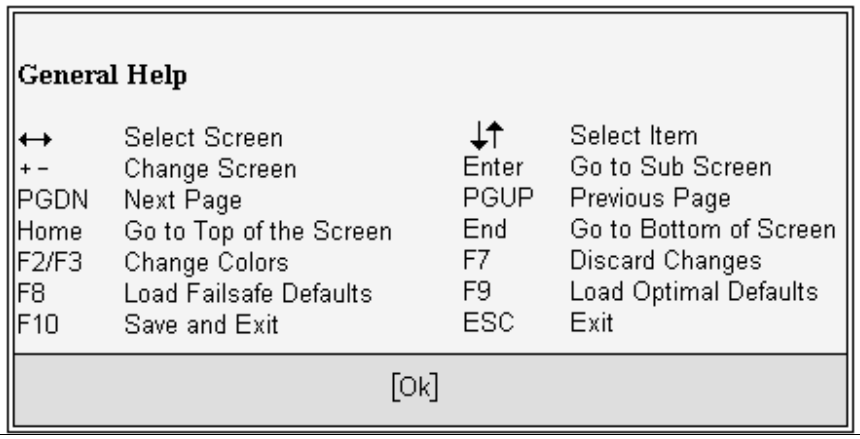
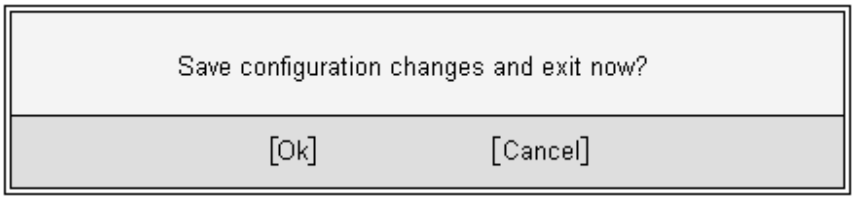
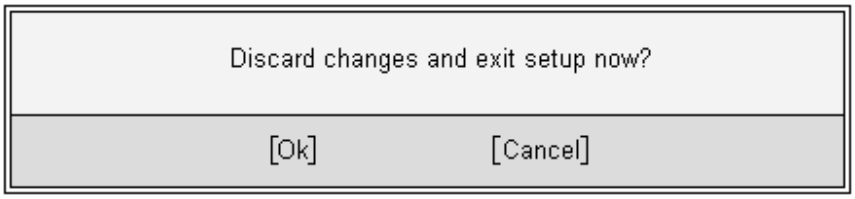


Note: There is a hot key legend located in the right frame on most AM4001setup screens.

Hot Key	Description
→← Left/Right	The *Left and Right* <Arrow> keys allow you to select an AM4001setup screen. For example: Main screen, Advanced screen, Chipset screen, and so on.
↑↓ Up/Down	The *Up and Down* <Arrow> keys allow you to select an AM4001setup item or sub-screen.
+- Plus/Minus	The *Plus and Minus* <Arrow> keys allow you to change the field value of a particular setup item. For example: Date and Time.
Tab	The <Tab> key allows you to select AM4001setup fields.

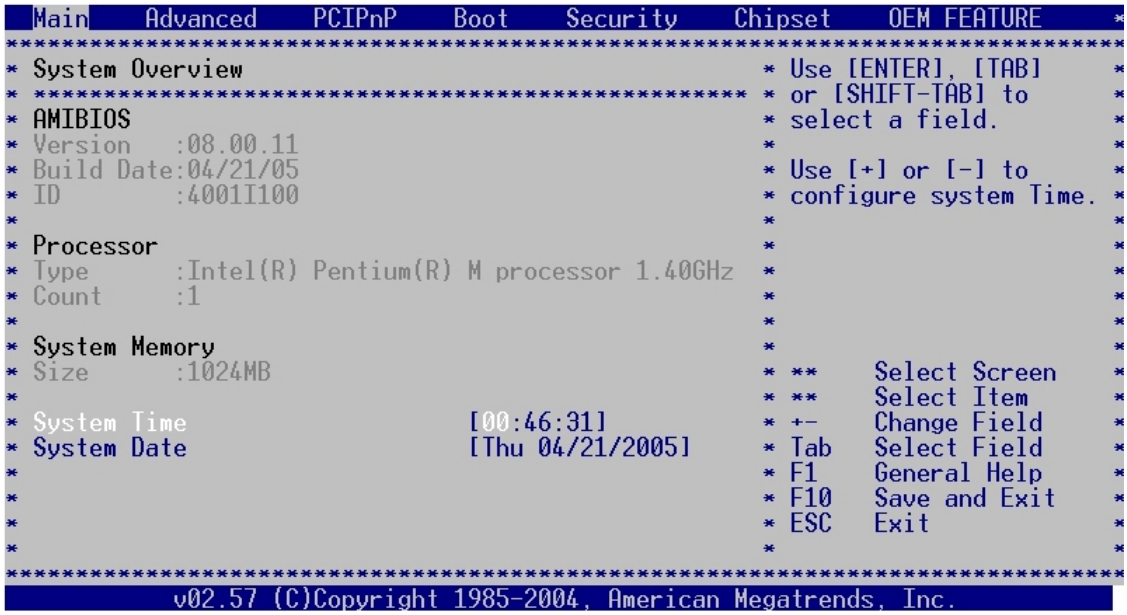
Note: The <F8> key on your keyboard is the Fail-Safe key. It is not displayed on the AM4001key legend by default. To set the Fail-Safe settings of the BIOS, press the <F8> key on your keyboard. It is located on the upper row of a standard 101 keyboard. The Fail-Safe settings allow the motherboard to boot up with the least amount of options set. This can lessen the probability of conflicting settings.

Navigation, Continued

Hot Key	Description
F1	The <F1> key allows you to display the *General Help screen*. Press the <F1> key to open the *General Help screen*. 
F10	The <F10> key allows you to save any changes you have made and exit AM4001Setup. Press the <F10> key to save your changes. The following screen will appear:  Press the <Enter> key to save the configuration and exit. You can also use the <Arrow> key to select *Cancel* and then press the <Enter> key to abort this function and return to the previous screen.
ESC	The <Esc> key allows you to discard any changes you have made and exit the AM4001Setup. Press the <Esc> key to exit the AM4001setup without saving your changes. The following screen will appear:  Press the <Enter> key to discard changes and exit. You can also use the <Arrow> key to select *Cancel* and then press the <Enter> key to abort this function and return to the previous screen.
Enter	The <Enter> key allows you to display or change the setup option listed for a particular setup item. The <Enter> key can also allow you to display the setup sub- screens.

Chapter 2 Main Setup

When you first enter the AM4001Setup Utility, you will enter the Main setup screen. You can always return to the Main setup screen by selecting the *Main* tab. There are two Main Setup options. They are described in this section. The Main BIOS Setup screen is shown below.



System Time/System Date

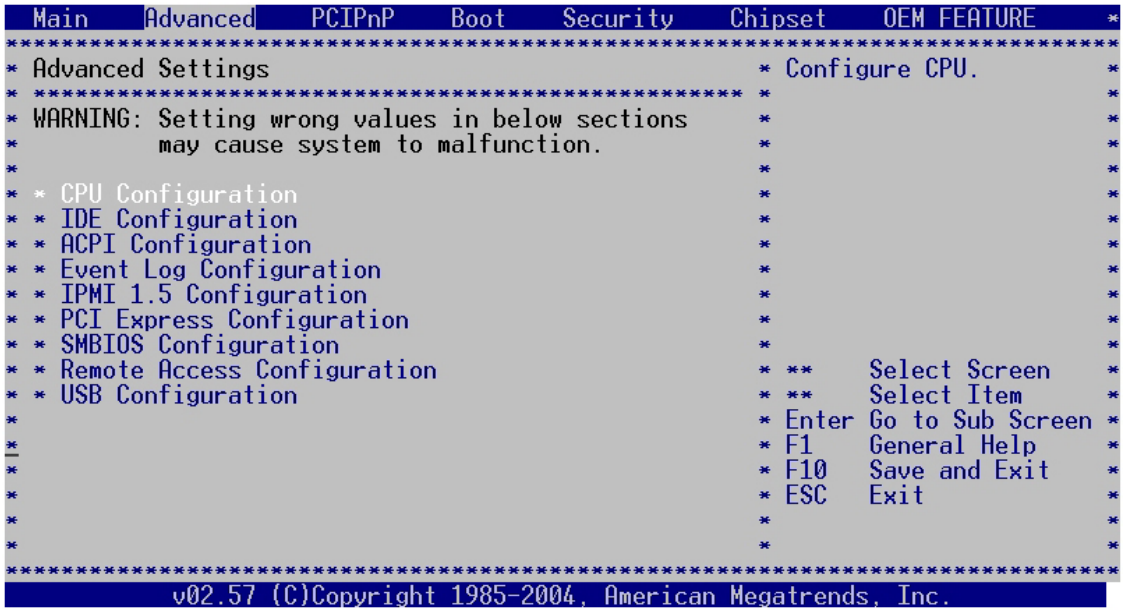
Use this option to change the system time and date. Highlight *System Time* or *System Date* using the <Arrow> keys. Enter new values through the keyboard. Press the <Tab> key or the <Arrow> keys to move between fields. The date must be entered in MM/DD/YY format. The time is entered in HH:MM:SS format.

Note: The time is in 24-hour format. For example, 5:30 A.M. appears as 05:30:00, and 5:30 P.M. as 17:30:00.

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Chapter 3 Advanced BIOS Setup

Select the *Advanced* tab from the AM4001setup screen to enter the Advanced BIOS Setup screen. You can select any of the items in the left frame of the screen, such as SuperIO Configuration, to go to the sub menu for that item. You can display an Advanced BIOS Setup option by highlighting it using the <Arrow> keys. All Advanced BIOS Setup options are described in this section. The Advanced BIOS Setup screen is shown below. The sub menus are described on the following pages.

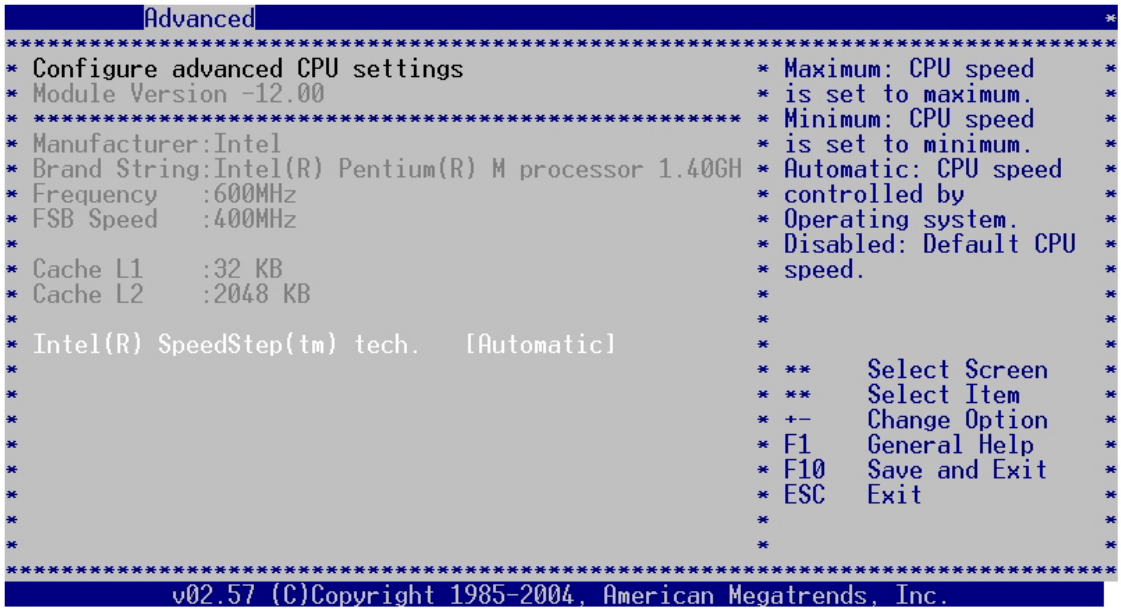


Advanced BIOS Setup

CPU CONFIGURATION SCREEN

CPU Configuration Settings

You can use this screen for Board information or to select the Intel Speed Step options. Use the <Plus> and <Minus> keys to change the value of the selected option. A description of the item appears on the right side of the screen. The setting is described on the following page. An example of the *CPU Configuration* screen is shown below.



Intel ® SpeedStep ™ tech.

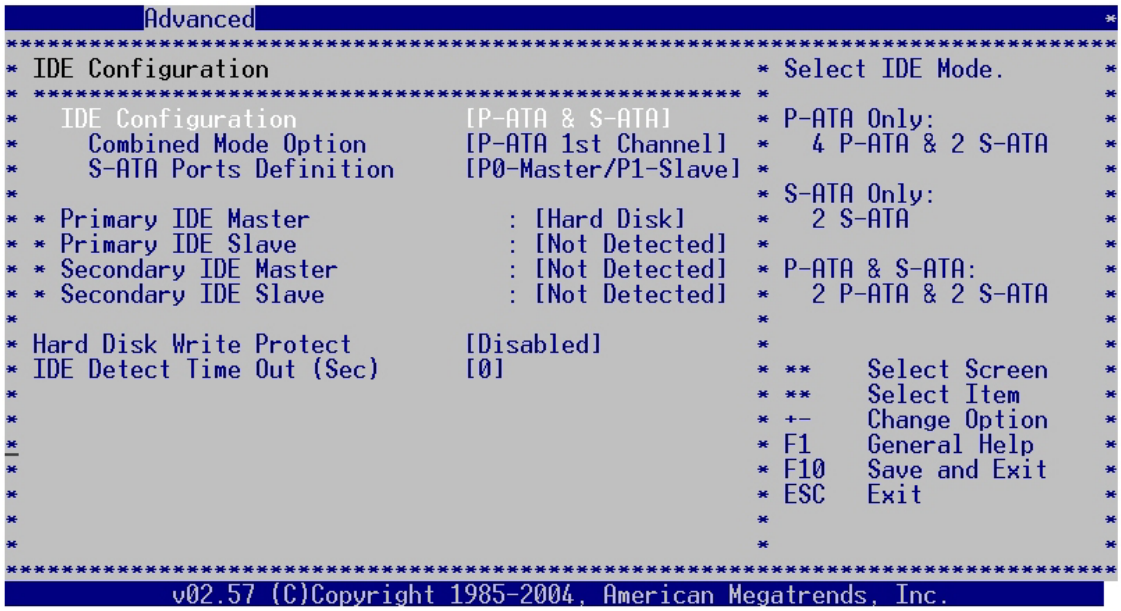
This item specifies the Intel SpeedStep feature.
The settings are *Maximum speed*, *Minimum Speed*, *Automatic* and *disabled*. The Optimal and Fail-Safe default setting is *Automatic*.
Using *Atomatic* allows the operating system to control the CPU speed.

Advanced BIOS Setup, Continued

IDE CONFIGUR ATION SCREEN

IDE Configuration

You can use this screen to select options for the IDE Configuration Settings. Use the up and down <Arrow> keys to select an item. Use the <Plus> and <Minus> keys to change the value of the selected option. A description of the selected item appears on the right side of the screen. The settings are described on the following pages. An example of the *IDE Configuration* screen is shown below.



Advanced BIOS Setup, Continued

IDE Configuration

This item specifies the IDE channels used by the onboard PCI IDE controller. The settings are *Disabled, P-ATA only, S-ATA only* or *P-ATA & S-ATA.* The Optimal and Fail-Safe default setting is *P-ATA & S-ATA.*

Option	Description
Disabled	Set this value to prevent the computer system from using the onboard IDE controller.
P-ATA only	Set this value to allow the computer system to detect 4 P-ATA & 2 S-ATA channels.
S-ATA only	Set this value to allow the computer system to detect 2 S-ATA channels.
P-ATA & S-ATA	Set this value to allow the computer system to detect the 2 P-ATA & 2 S-ATA channels. This is the default setting.

Primary IDE Master, Primary IDE Slave, Secondary IDE Master, Secondary IDE Slave

Select one of the hard disk drives to configure it. Press <Enter> to access its sub menu. The options on the sub menu are described in the following sections.

Hard disk drive Write Protect

Set this option to protect the hard disk drive from being overwritten. The Optimal and Fail-Safe default setting is *Disabled*.

Option	Description
Disabled	Set this value to allow the hard disk drive to be used normally. Read, write, and erase functions can be performed to the hard disk drive. This is the default setting.
Enabled	Set this value to prevent the hard disk drive from being erased.

IDE Detect Time Out (Seconds)

Set this option to stop the AMIBIOS from searching for IDE devices within the specified number of seconds. Basically, this allows you to fine-tune the settings to allow for faster boot times. Adjust this setting until a suitable timing that can detect all IDE disk drives attached is found.

The Optimal and Fail-Safe default setting is *0*.

Option	Description
0	This value is the best setting to use if the onboard IDE controllers are set to a specific IDE disk drive in the AMIBIOS.
5	Set this value to stop the AMIBIOS from searching the IDE bus for IDE disk drives in five seconds. A large majority of ultra ATA hard disk drives can be detected well within five seconds.
10	Set this value to stop the AMIBIOS from searching the IDE bus for IDE disk drives in 10 seconds.
15	Set this value to stop the AMIBIOS from searching the IDE bus for IDE disk drives in 15 seconds.
20	Set this value to stop the AMIBIOS from searching the IDE bus for IDE disk drives in 20 seconds.
25	Set this value to stop the AMIBIOS from searching the IDE bus for IDE disk drives in 25 seconds.
30	Set this value to stop the AMIBIOS from searching the IDE bus for IDE disk drives in 30 seconds.
35	*35* is the default value. It is the recommended setting when all IDE connectors are set to *AUTO* in the AMIBIOS setting.

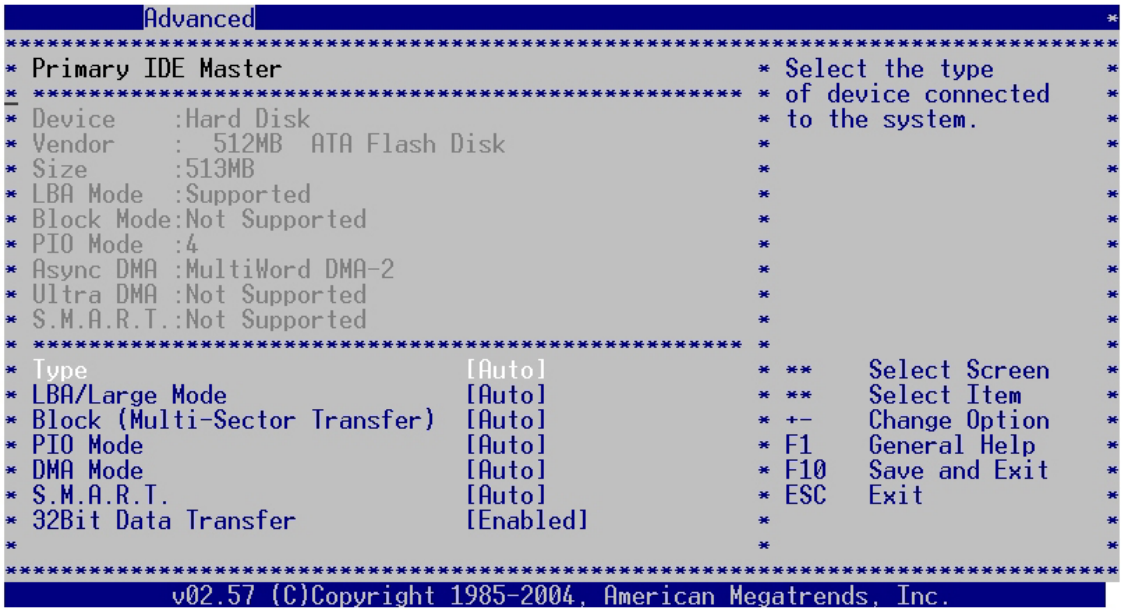
Note: Different IDE disk drives take longer for the BIOS to locate than others do.

Advanced BIOS Setup, Continued

PRIMARY AND SECONDARY IDE MASTER AND SLAVE SUB MENU

Primary and Secondary IDE Master and Slave Settings

From the IDE Configuration screen, press <Enter> to access the sub menu for the primary and secondary IDE master and slave drives. Use this screen to select options for the Primary and Secondary IDE drives. Use the up and down <Arrow> keys to select an item. Use the <Plus> and <Minus> keys to change the value of the selected option. The settings are described on the following pages. The screen for the Primary IDE Master is shown below.



Drive Parameters

The “grayed-out” items in the left frame are the IDE disk drive parameters taken from the firmware of the IDE disk drive selected. The drive parameters listed are as follows:

Parameter	Description
Device	Type of device, such as Hard disk drive.
Vendor	Manufacturer of the device.
Size	The size of the device.
LBA Mode	LBA (Logical Block Addressing) is a method of addressing data on a disk drive. In LBA mode, the maximum drive capacity is 137 GB. For drive capacities over 137 GB, your AMIBIOS must be equipped with 48-bit LBA mode addressing. If not, contact your motherboard manufacturer or install an ATA/133 IDE controller card that supports 48-bit LBA mode.

Advanced BIOS Setup, Continued

Parameter	Description
Block Mode	Block mode boosts IDE drive performance by increasing the amount of data transferred. Only 512 bytes of data can be transferred per interrupt if block mode is not used. Block mode allows transfers of up to 64 KB per interrupt.
PIO Mode	IDE PIO mode programs timing cycles between the IDE drive and the programmable IDE controller. As the PIO mode increases, the cycle time decreases.
Async DMA	This indicates the highest Asynchronous DMA Mode that is supported.
Ultra DMA	This indicates the highest Synchronous DMA Mode that is supported.
S.M.A.R.T.	Self-Monitoring Analysis and Reporting Technology protocol used by IDE drives of some manufacturers to predict drive failures.

Type

This option sets the type of device that the AMIBIOS attempts to boot from after the Power-On Self-Test (POST) has completed. The Optimal and Fail-Safe default setting is *Auto.*

Option	Description
Not Installed	Set this value to prevent the BIOS from searching for an IDE disk drive on the specified channel.
Auto	Set this value to allow the BIOS auto detect the IDE disk drive type attached to the specified channel. This setting should be used if an IDE hard disk drive is attached to the specified channel. This is the default setting.
CDROM	This option specifies that an IDE CD-ROM drive is attached to the specified IDE channel. The BIOS will not attempt to search for other types of IDE disk drives on the specified channel.
ARMD	This option specifies an ATAPI Removable Media Device. This includes, but is not limited to: • ZIP • LS-120

LBA/Large Mode

LBA (Logical Block Addressing) is a method of addressing data on a disk drive. In LBA mode, the maximum drive capacity is 137 GB. The Optimal and Fail-Safe default setting is *Auto.*

Note: For drive capacities over 137 GB, your AMIBIOS must be equipped with 48-bit LBA mode addressing. If not, contact your motherboard manufacturer or install an ATA/133 IDE controller card that supports 48-bit LBA mode.

Option	Description
Disabled	Set this value to prevent the BIOS from using Large Block Addressing mode control on the specified channel.
Auto	Set this value to allow the BIOS to auto detect the Large Block Addressing mode control on the specified channel. This is the default setting.

Advanced BIOS Setup, Continued

Block (Multi-Sector Transfer)

This option sets the block mode multi sector transfers option. The Optimal and Fail-Safe default setting is *Auto.*

Option	Description
Disabled	Set this value to prevent the BIOS from using Multi-Sector Transfer on the specified channel. The data to and from the device will occur one sector at a time.
Auto	Set this value to allow the BIOS to auto detect device support for Multi-Sector Transfers on the specified channel. If supported, Set this value to allow the BIOS to auto detect the number of sectors per block for transfer from the hard disk drive to the memory. The data transfer to and from the device will occur multiple sectors at a time. This is the default setting.

PIO Mode

IDE PIO (Programmable I/O) mode programs timing cycles between the IDE drive and the programmable IDE controller. As the PIO mode increases, the cycle time decreases. The Optimal and Fail-Safe default setting is *Auto*.

Option	Description
Auto	Set this value to allow the BIOS to auto detect the PIO mode. Use this value if the IDE disk drive support cannot be determined. This is the default setting.
0	Set this value to allow the BIOS to use PIO mode 0. It has a data transfer rate of 3.3 MBs.
1	Set this value to allow the BIOS to use PIO mode 1. It has a data transfer rate of 5.2 MBs.
2	Set this value to allow the BIOS to use PIO mode 2. It has a data transfer rate of 8.3 MBs.
3	Set this value to allow the BIOS to use PIO mode 3. It has a data transfer rate of 11.1 MBs.
4	Set this value to allow the BIOS to use PIO mode 4. It has a data transfer rate of 16.6 MBs. This setting generally works with all hard disk drives manufactured after 1999. For other disk drive, such as IDE CD-ROM drives, check the specifications of the drive.

Advanced BIOS Setup, Continued

DMA Mode

This setting allows you to adjust the DMA mode options. The Optimal and Fail-Safe default setting is *Auto*.

Option	Description
Auto	Set this value to allow the BIOS to auto detect the DMA mode. Use this value if the IDE disk drive support cannot be determined. This is the default setting.
SWDMA0	Set this value to allow the BIOS to use Single Word DMA mode 0. It has a data transfer rate of 2.1 MBs.
SWDMA1	Set this value to allow the BIOS to use Single Word DMA mode 1. It has a data transfer rate of 4.2 MBs.
SWDMA2	Set this value to allow the BIOS to use Single Word DMA mode 2. It has a data transfer rate of 8.3 MBs.
MWDMA0	Set this value to allow the BIOS to use Multi Word DMA mode 0. It has a data transfer rate of 4.2 MBs.
MWDMA1	Set this value to allow the BIOS to use Multi Word DMA mode 1. It has a data transfer rate of 13.3 MBs.
MWDMA2	Set this value to allow the BIOS to use Multi Word DMA mode 2. It has a data transfer rate of 16.6 MBs.
UDMA0	Set this value to allow the BIOS to use Ultra DMA mode 0. It has a data transfer rate of 16.6 MBs. It has the same transfer rate as PIO mode 4 and Multi Word DMA mode 2.
UDMA1	Set this value to allow the BIOS to use Ultra DMA mode 1. It has a data transfer rate of 25 MBs.
UDMA2	Set this value to allow the BIOS to use Ultra DMA mode 2. It has a data transfer rate of 33.3 MBs.
UDMA3	Set this value to allow the BIOS to use Ultra DMA mode 3. It has a data transfer rate of 44.4 MBs. To use this mode, it is required that an 80-conductor ATA cable is used.
UDMA4	Set this value to allow the BIOS to use Ultra DMA mode 4. It has a data transfer rate of 66.6 MBs. To use this mode, it is required that an 80-conductor ATA cable is used.
UDMA5	Set this value to allow the BIOS to use Ultra DMA mode 5. It has a data transfer rate of 99.9 MBs. To use this mode, it is required that an 80-conductor ATA cable is used.
UDMA6	Set this value to allow the BIOS to use Ultra DMA mode 6. It has a data transfer rate of 133.2 MBs. To use this mode, it is required that an 80-conductor ATA cable is used.

Advanced BIOS Setup, Continued

S.M.A.R.T. for Hard disk drives

Self-Monitoring Analysis and Reporting Technology (SMART) feature can help predict impending drive failures. The Optimal and Fail-Safe default setting is *Auto*.

Option	Description
Auto	Set this value to allow the BIOS to auto detect hard disk drive support. Use this setting if the IDE disk drive support cannot be determined. This is the default setting.
Disabled	Set this value to prevent the BIOS from using the SMART feature.
Enabled	Set this value to allow the BIOS to use the SMART feature on support hard disk drives.

32-Bit Data Transfer

This option sets the 32-bit data transfer option. The Optimal and Fail-Safe default setting is *Enabled*.

Option	Description
Disabled	Set this value to prevent the BIOS from using 32-bit data transfers.
Enabled	Set this value to allow the BIOS to use 32-bit data transfers on support hard disk drives. This is the default setting.

ARMD Emulation Type

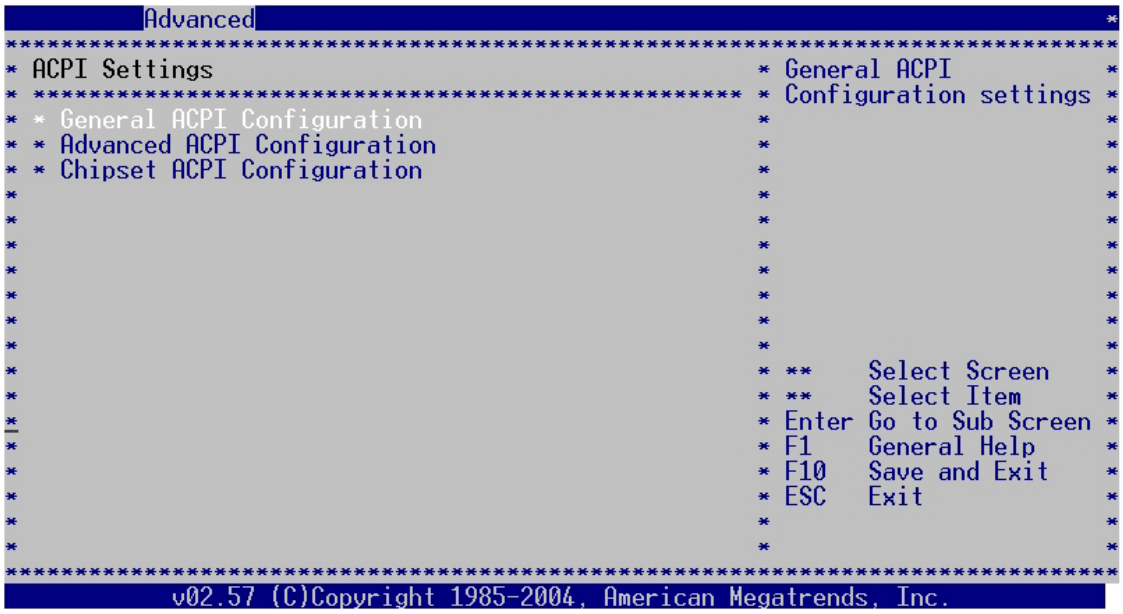
ATAPI Removable Media Device (ARMD) is a device that uses removable media, such as the LS120, MO (Magneto-Optical), or Iomega Zip drives. If you want to boot up from media on an ARMD, it is required that you emulate boot up from a floppy or hard disk drive. This is especially necessary when trying to boot to DOS. You can select the type of emulation used if you are booting from such a device. The Optimal and Fail-Safe default setting is *Auto*.

Option	Description
Auto	Set this value to allow the BIOS to automatically set the emulation used by ARMD. This is the default setting.
Floppy	Set this value for ARMD to emulate a floppy drive during boot up.
Hard disk drive	Set this value for ARMD to emulate a hard disk drive during boot up.

Advanced BIOS Setup, Continued

ACPI CONFIGURATION

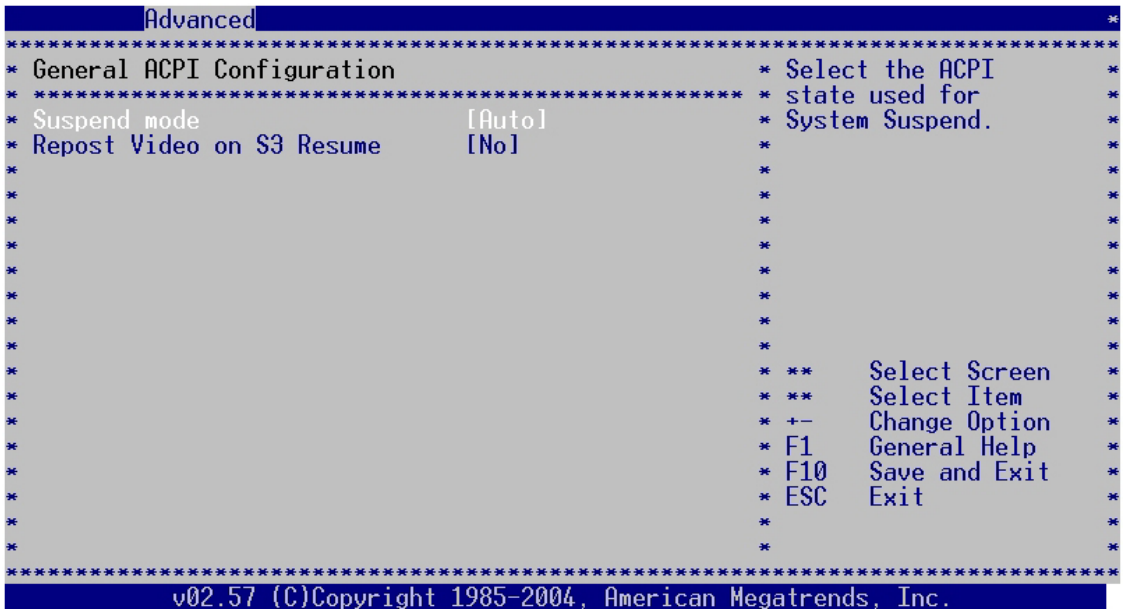
Select the *ACPI Configuration* Menu to enter the ACPI BIOS Setup screen. You can select Advanced ACPI Configuration in the left frame of the screen to go to the sub menus for this item. You can display an ACPI BIOS Setup option by highlighting it using the <Arrow> keys. All ACPI BIOS Setup options are described in this section. The ACPI BIOS Setup screen is shown below.



Advanced BIOS Setup, Continued

General ACPI Configuration

You can use this screen to select options for the General ACPI Configuration Settings. Use the up and down <Arrow> keys to select an item. Use the <Plus> and <Minus> keys to change the value of the selected option. A description of the selected item appears on the right side of the screen. The settings are described on this page. The screen is shown below.



Suspend Mode

Select the ACPI state used for System Suspend. The Optimal and Fail-Safe default setting is *S1 (Pos)*.

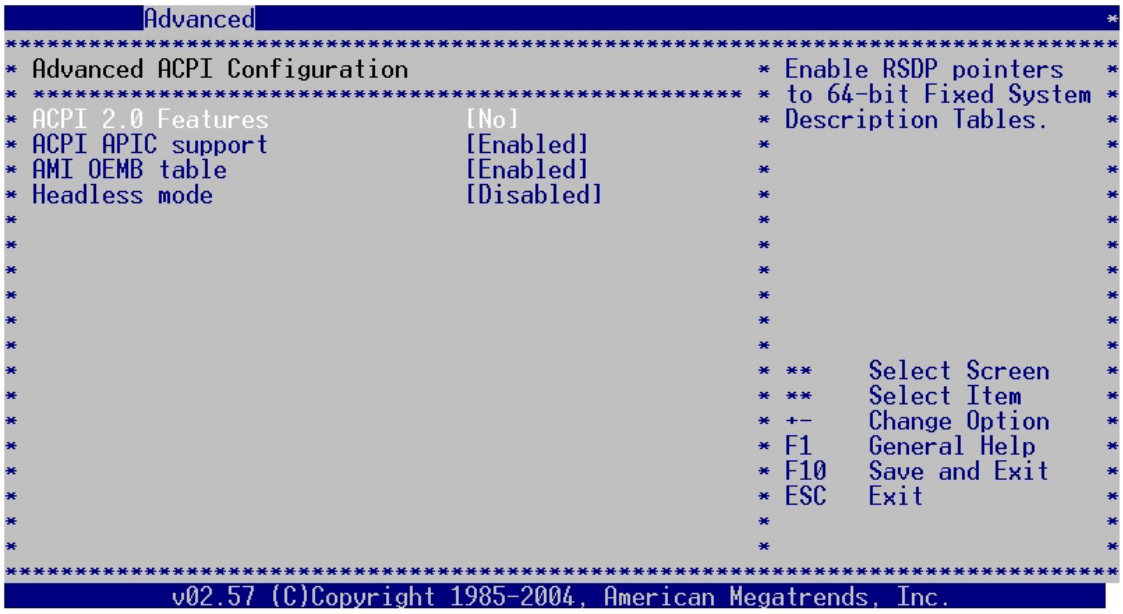
Repost Video on S3 Resume

Set this value to allow video repost support. This item is only visible when *S1 (Pos)* is not selected in Suspend Mode. The Optimal and Fail-Safe default setting is *No*.

Advanced BIOS Setup, Continued

Advanced ACPI Configuration

You can use this screen to select options for the ACPI Advanced Configuration Settings. Use the up and down <Arrow> keys to select an item. Use the <Plus> and <Minus> keys to change the value of the selected option. A description of the selected item appears on the right side of the screen. The settings are described on this page. The screen is shown below.



ACPI 2.0 Feature

Set this value to allow or prevent the system to be complaint with the ACPI 2.0 specification. The Optimal and Fail-Safe default setting is *No*.

Option	Description
No	This setting prevents the BIOS from supporting the ACPI 2.0 specification.
Yes	This setting allows the BIOS to support the ACPI 2.0 specification.

ACPI APIC Support

Include ACPI APIC table pointer to RSDT pointer list. The Optimal and Fail-Safe default setting is *Enabled*.

AMI OEMB Table

Include OEMB table pointer to R(X)SDT pointer list. The Optimal and Fail-Safe default setting is *Enabled*.

Headless Mode

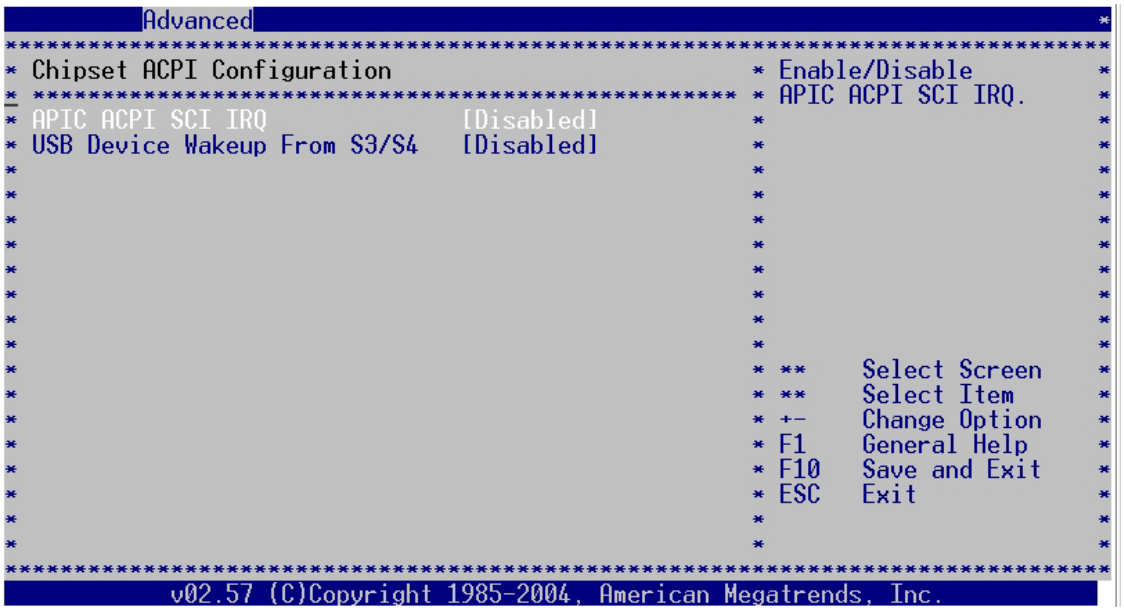
This option is used to update the ACPI FACP table to indicate the headless operations. The Optimal and Fail-Safe default setting is *Disabled*.

Option	**Description**
Disabled	This option disables updating the ACPI FACP table to indicate headless operation.
Enabled	This option enables updating the ACPI FACP table to indicate headless operation.

Advanced BIOS Setup, Continued

Chipset ACPI Configuration

You can use this screen to select options for the Chipset ACPI Configuration Settings. Use the up and down <Arrow> keys to select an item. Use the <Plus> and <Minus> keys to change the value of the selected option. A description of the selected item appears on the right side of the screen. The settings are described on this page. The screen is shown below.



APIC ACPI SCI IRQ

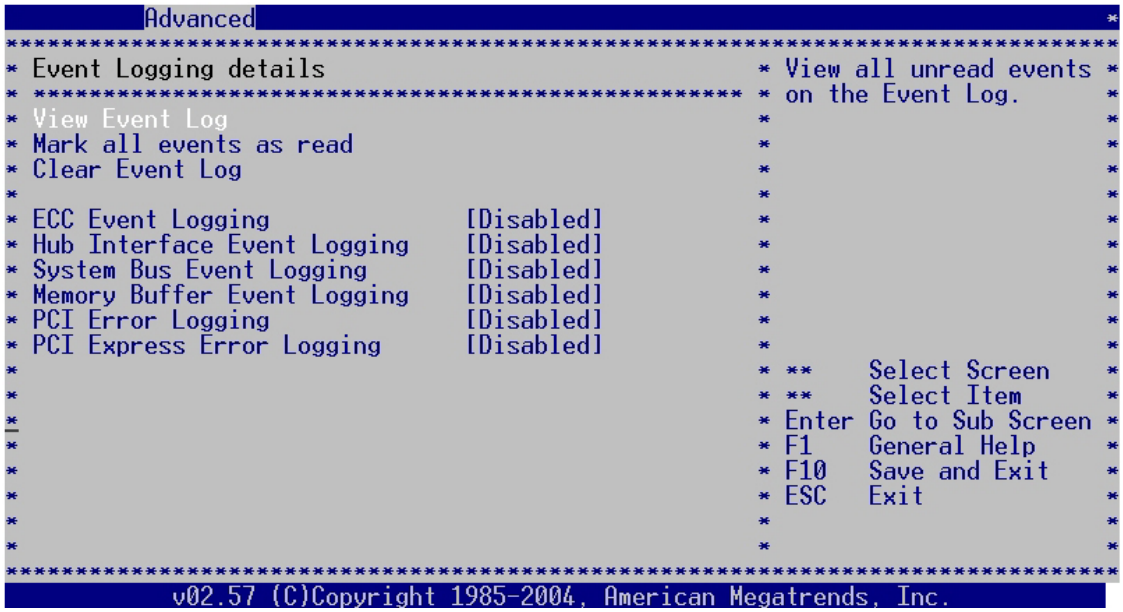
This function enables/disables the APIC. The Optimal and Fail-Safe default setting is *Disabled*.

USB Device Wakeup from S3/S4

This function enables/disables the USB device Wakeup from S3/S4. The Optimal and Fail-Safe default setting is *Disabled*.

Advanced BIOS Setup, Continued

EVENT LOG CONFIGURATION



View Event Log
A pop up window displays all unread events, e.g. 01/01/02 13:12:56 CMOS time not set

Mark all events as read
Mark all unread events as read and clear the Event Log buffer.

Clear Event Log
Discard all events in the Event Log.

Event Log Statistics
View details on the count of total unread events.

PCI Error Logging
Enables the PCI Error Logging.

Hub Interface Event Logging
Enables the Hub Interface Event Logging.

System Bus Event Logging
Enables the System Bus Error Event Logging.

Memory Buffer Event Logging
Enables the Memory Buffer Error Event Logging.

PCI Error Logging
Enables the PCI Error Logging.

PCI Express Error Logging
Enables the PCI Express Advanced Error Logging.

Advanced BIOS Setup, Continued

IPMI 1.5 CONFIGURATION

IPMI 1.5 Configuration

You can use this screen to select options for the IPMI 1.5 Configuration. Use the up and down <Arrow> keys to select an item. Use the <Plus> and <Minus> keys to change the value of the selected option. The settings are described on the following pages. The screen is shown below.



View IPMC System Event Log

View all events in the IPMC Event Log.

Clear IPMC System Event Log

Clears all events in the IPMC Event Log.

IPMC Watchdog Timer Action

This item specifies the IPMC watchdog timer actions. The settings are *Disabled*, *Reset System*, *Power Down,* or *Power Cycle*. The Optimal and Fail-Safe default setting is *Disabled.*

Option	Description
Disabled	Set this value to prevent the computer system from using the IPMC watchdog timer. This is the default setting.
Reset System	Set this value to reset the computer system.
Power Down	Set this value to power down the computer system.
Power Cycle	Set this value to power cycle the computer system.

Advanced BIOS Setup, Continued

IPMI Device and Firmware Information

This option is used to view the IPMI Device and Firmware Information.

System Management

This option is used to display the FRU board and product information, as well as the IPMC Device and Firmware Information.

KCS-SMS IRQ

This option is used to select the IRQ for the system management software. The Optimal and Fail-Safe default setting is *Disabled*.

Option	Description
Disabled	No IRQ is reserved. This is the default setting.
IRQ7	Set this value to allow the computer system to select IRQ7 for the System Management Software.

Management Controller Configuration

This option is used to select the Management Controller Configuration. The Optimal and Fail-Safe default setting is *Satellite*.

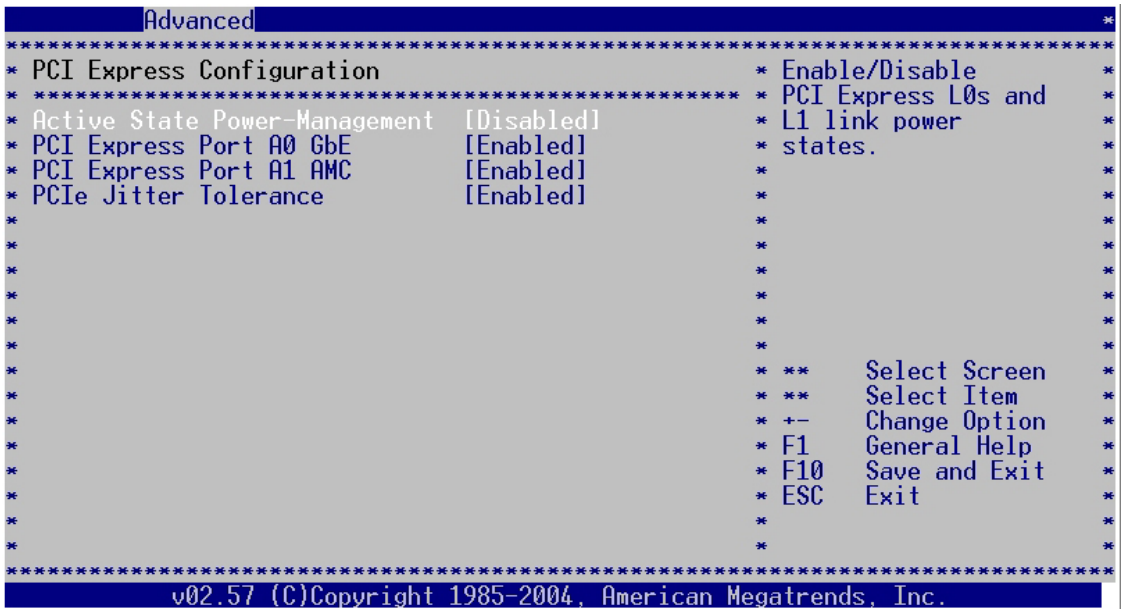
Option	Description
Baseboard	Set this value to allow the computer system to use the Management Controller located on the baseboard.
Satellite	Set this value to allow the computer system to use the Management Controller located on the satellite.

Advanced BIOS Setup, Continued

PCI EXPRESS CONFIGURATION

PCI Express Configuration

You can use this screen to select options for the PCI Express s Configuration. Use the up and down <Arrow> keys to select an item. Use the <Plus> and <Minus> keys to change the value of the selected option. The settings are described on the following pages. The screen is shown below.



Active State Power Management

Enables the PCI Express L0s and L1 link power states. The Optimal and Fail-Safe default setting is *Enabled.*

Option	Description
Disabled	This option disables the PCI Express L0s and L1 link power states.
Enabled	This option enables the PCI Express L0s and L1 link power states. This is the default setting.

PCI Express Port A0 / A1

This option is used to select the PCI Express Port. The Optimal and Fail-Safe default setting is *Enabled*.

Option	Description
Disabled	Select this option to always hide Port A0.
Enabled	Select this option to always make Port A1 visible. This is the default setting.
Auto	Select this option to make Port A0 visible when the PCI Express card is inserted.

PCIe Jitter Tolerance

This option is used to enable or disable the PCIe Jitter Tolerance. The Optimal and Fail-Safe default setting is *Enabled*.

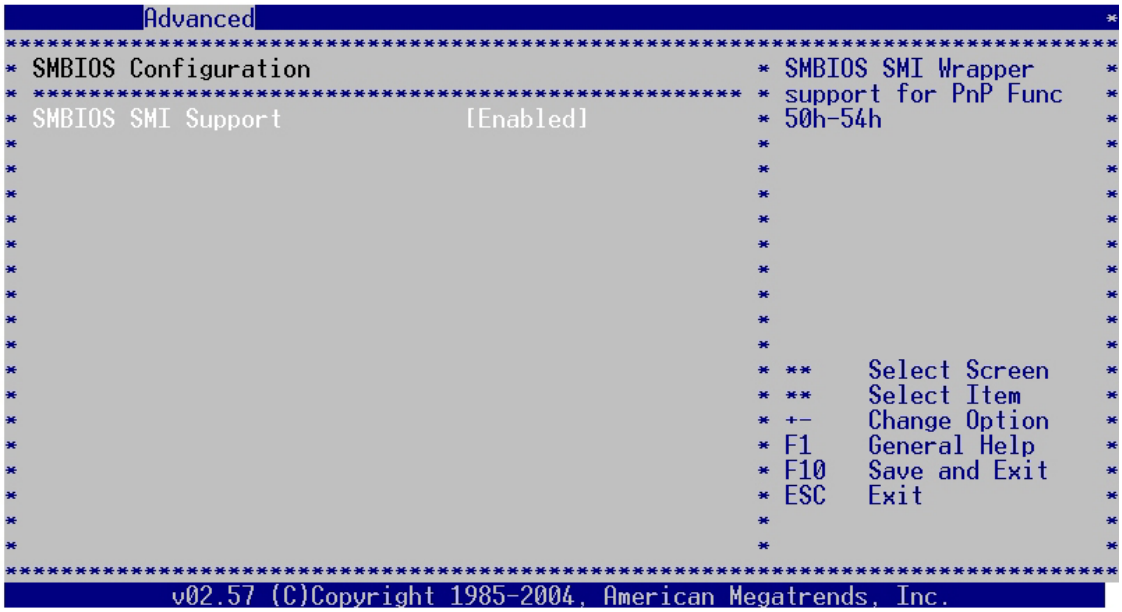
Option	Description
Disabled	This option disables the PCIe Jitter Tolerance.
Enabled	This option enables the PCIe Jitter Tolerance. This is the default setting.

Advanced BIOS Setup, Continued

SMBIOS CONFIGURATION

SMBIOS Configuration

You can use this screen to select options for the SMBIOS Configuration. Use the up and down <Arrow> keys to select an item. Use the <Plus> and <Minus> keys to change the value of the selected option. The settings are described on the following pages. The screen is shown below.



SMBIOS SMI Support

Enables the SMBIOS SMI Support. The Optimal and Fail-Safe default setting is *Enabled.*

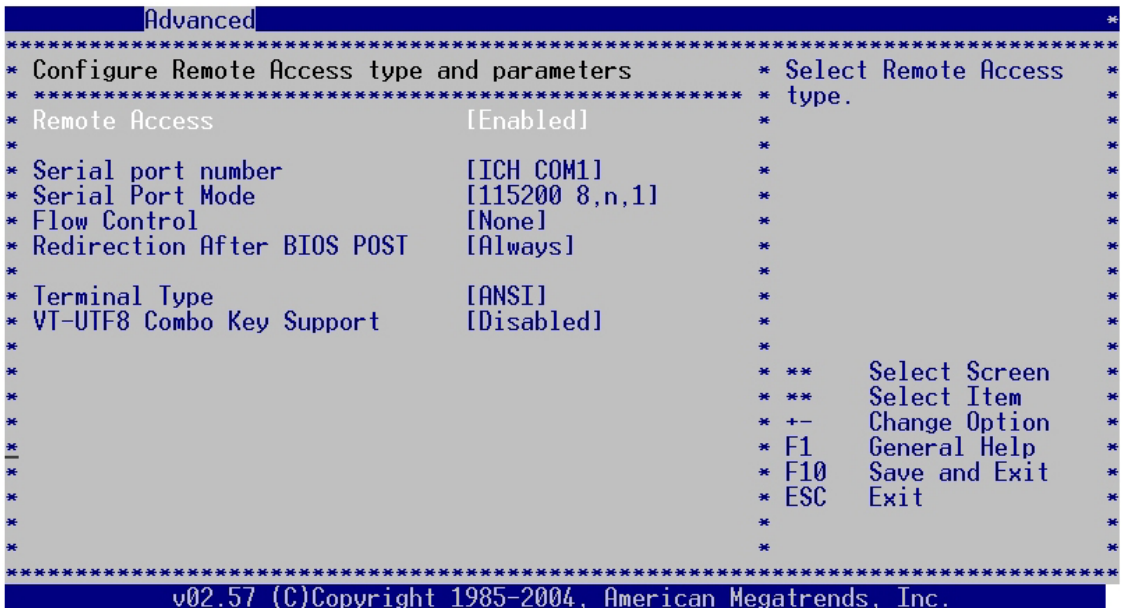
Option	Description
Disabled	This option disables the SMBIOS SMI Support.
Enabled	This option enables the SMBIOS SMI Support for the PNP Function 50 h – 54 h. This is the default setting.

Advanced BIOS Setup, Continued

REMOTE ACCESS CONFIGURATION

Remote Access Configuration

You can use this screen to select options for the Remote Access Configuration. Use the up and down <Arrow> keys to select an item. Use the <Plus> and <Minus> keys to change the value of the selected option. The settings are described on the following pages. The screen is shown below.



Remote Access

You can disable or enable the BIOS remote access feature here. The Optimal and Fail-Safe default setting is *Enabled.*

Option	Description
Disabled	Set this value to prevent the BIOS from using Remote Access.
Enabled	Set the value for this option to *Enabled* to allow the system to use the remote access feature. The remote access feature requires a dedicated serial port connection. This is the default setting.

Serial Port Number

Select the serial port you want to use for console redirection. You can set the value for this option to either *ICH COM1* or *ICH COM2*. The Optimal and Fail-Safe default setting is *ICH COM1*.

Option	Description
ICH COM1	Set this value to allow the system to use ICH COM1 (Communication port1) for the remote access interface. This is the default setting.
ICH COM2	Set this value to allow the system to use ICH COM2 (Communication port2) for the remote access interface.

Advanced BIOS Setup, Continued

Serial Port Mode

Select the baud rate you want the serial port to use for console redirection. The Optimal and Fail-Safe default setting is *115200 8,n,1.*

Option	Description
115200 8,n,1	Set this value to allow you to select 115200 as the baud rate (transmitted bits per second) of the serial port.
57600 8,n,1	Set this value to allow you to select 57600 as the baud rate (transmitted bits per second) of the serial port.
38400 8,n,1	Set this value to allow you to select 38400 as the baud rate (transmitted bits per second) of the serial port.
19200 8,n,1	Set this value to allow you to select 19200 as the baud rate (transmitted bits per second) of the serial port.
09600 8,n,1	Set this value to allow you to select 09600 as the baud rate (transmitted bits per second) of the serial port.

Flow Control

This option is used to select the flow control for console redirection. The Optimal and Fail-Safe default setting is *None.*

Option	Description
Hardware	Set this value to select the flow control by hardware.
Software	Set this value to select the flow control by software.
None	No flow control is activated.

Redirection After BIOS POST

This option is used to select redirection after BIOS POST. The Optimal and Fail-Safe default setting is *Always.*

Option	Description
Disabled	Set this value to turn off the redirection after POST.
BootLoader	Set this value to activate the redirection during POST and during BootLoader.
Always	The redirection is always active.

Terminal Type

This option is used to select the target terminal type. The Optimal and Fail-Safe default setting is *ANSI.*

Option	Description
ANSI	Set this value to select the target terminal type.
VT100	Set this value to select the target terminal type.
VT-UTF8	Set this value to select the target terminal type.

VT-UTF8 Combo Key Support

This option is used to enable or disable the VT-UTF8 combo key support. The Optimal and Fail-Safe default setting is *Disabled.*

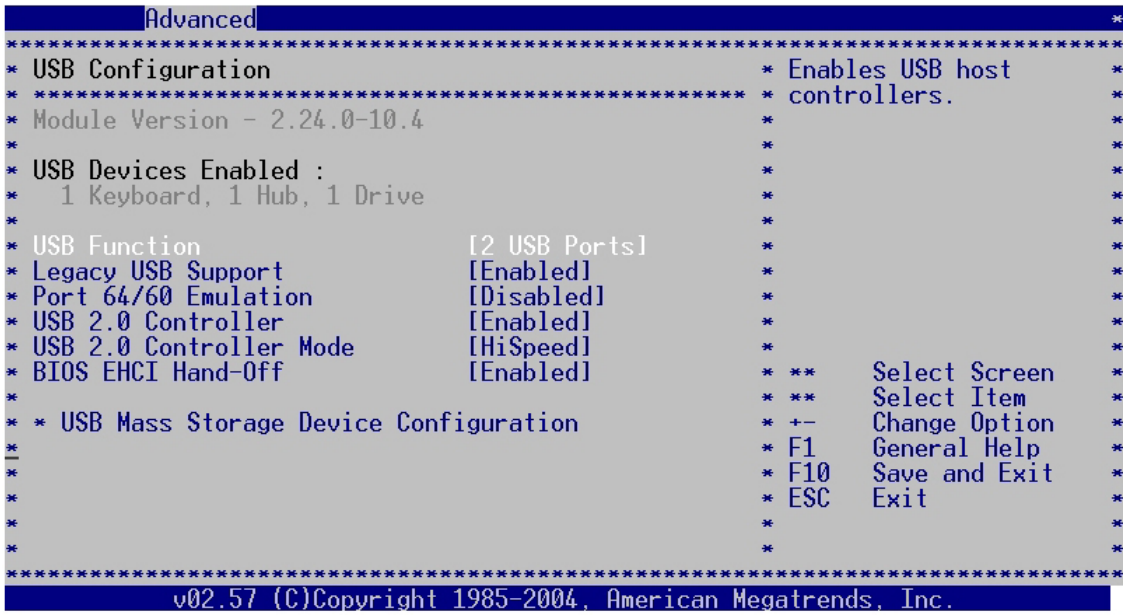
Option	Description
Disabled	Set this value to disable the VT-UTF8 combination key support for the ANSI/VT100 terminals.
Enabled	Set this value to enable the VT-UTF8 combination key support for the ANSI/VT100 terminals.

Advanced BIOS Setup, Continued

USB CONFIGURATION

USB Configuration

You can use this screen to select options for the USB Configuration. Use the up and down <Arrow> keys to select an item. Use the <Plus> and <Minus> keys to change the value of the selected option. The settings are described on the following pages. The screen is shown below.



USB Function

Set this value to allow the system to enable or disable the onboard USB ports. The Optimal and Fail-Safe default setting is *2 USB Ports*.

Option	Description
Disabled	This setting makes the onboard USB ports unavailable.
2 USB Ports	This setting allows the use of the two USB ports. This is the default setting.
All USB Ports	This setting allows the use of the all USB ports.

Legacy USB Support

Set this value to allow the system to enable or disable the legacy USB support. The Optimal and Fail-Safe default setting is *Enabled*.

Option	Description
Disabled	Set this value to disable the legacy USB support.
Enabled	Set this value to enable the legacy USB support. This is the default setting.
Auto	Set this value to disable the legacy USB support if no USB devices are connected.

Advanced BIOS Setup, Continued

Port 64/60 Emulation

Set this value to allow the system to enable or disable the I/O Port 64/60 emulation support. The Optimal and Fail-Safe default setting is *Disabled*.

Option	Description
Disabled	Set this value to disable the I/O Port 64/60 emulation support. This is the default setting.
Enabled	Set this value to enable the I/O Port 64/60 emulation support.

USB 2.0 Controller

Set this value to allow the system to enable or disable the USB 2.0 controller. The Optimal and Fail-Safe default setting is *Enabled*.

Option	Description
Disabled	Set this value to disable the USB 2.0 controller.
Enabled	Set this value to enable the USB 2.0 controller. This is the default setting.

USB 2.0 Controller Mode

Set this value to allow the system to configure the USB 2.0 controller. The Optimal default setting is *Full Speed*. The Fail-Safe default setting is *HiSpeed*.

Option	Description
Full Speed	Set this value to configure the USB 2.0 controller in Full Speed (12 Mbps).
HiSpeed	Set this value to configure the USB 2.0 controller in HiSpeed (480 Mbps).

BIOS EHCI Hand-Off

This is a workaround for OSs without EHCI hand-off support. The EHCI ownership change should claim by ECHI driver.

USB Mass Storage Device Configuration

Configure the USB Mass Storage Class Devices. More Information displays the BIOS help.

Chapter 4 PCI/PnP Setup

Select the *PCI/PnP* tab from the AM4001setup screen to enter the Plug and Play BIOS Setup screen. You can display a Plug and Play BIOS Setup option by highlighting it using the <Arrow> keys. All Plug and Play BIOS Setup options are described in this section. The Plug and Play BIOS Setup screen is shown below.



Clear NVRAM

Set this value to allow the system to clear the NVRAM during system boot. The Optimal and Fail-Safe default setting is *No*.

Option	Description
No	The *No* setting does not allow the BIOS to clear the NVRAM during system boot. This is the default setting.
Yes	The *Yes* setting allows the BIOS to clear the NVRAM during system boot.

Plug and Play O/S

Set this value to allow the system to modify the settings for Plug and Play operating system support. The Optimal and Fail-Safe default setting is *No*.

Option	Description
No	The *No* setting is for operating systems that do not meet the Plug and Play specifications. It allows the BIOS to configure all the devices in the system. This is the default setting.
Yes	The *Yes* setting allows the operating system to change the interrupt, I/O, and DMA settings. Set this option if the system is running Plug and Play aware operating systems.

PCI/PnP Setup, Continued

PCI Latency Timer

Set this value to allow the PCI Latency Timer to be adjusted. This option sets the latency of all PCI devices on the PCI bus. The Optimal and Fail-Safe default setting is *32*.

Option	Description
32	This option sets the PCI latency to 32 PCI clock cycles.
64	This option sets the PCI latency to 64 PCI clock cycles. This is the default setting.
96	This option sets the PCI latency to 96 PCI clock cycles.
128	This option sets the PCI latency to 128 PCI clock cycles.
160	This option sets the PCI latency to 160 PCI clock cycles.
192	This option sets the PCI latency to 192 PCI clock cycles.
224	This option sets the PCI latency to 224 PCI clock cycles.
248	This option sets the PCI latency to 248 PCI clock cycles.

Allocate IRQ to PCI VGA

Set this value to allow or restrict the system from giving the PCI VGA adapter card an interrupt address. The Optimal and Fail-Safe default setting is *Yes*.

Option	Description
Yes	Set this value to allow the allocation of an IRQ to a PCI VGA adapter card that uses the PCI local bus. This is the default setting.
No	Set this value to prevent the allocation of an IRQ to a PCI VGA adapter card that uses the PCI local bus.

Palette Snooping

Set this value to allow the system to modify the Palette Snooping settings. The Optimal and Fail-Safe default setting is *Disabled*.

Option	Description
Disabled	This is the default setting and should not be changed unless the VGA card manufacturer requires Palette Snooping to be Enabled.
Enabled	This setting informs the PCI devices that an ISA based Graphics device is installed in the system. It does this so the ISA based Graphics card will function correctly. This does not necessarily indicate a physical ISA adapter card. The graphics chipset can be mounted on a PCI card. Always check with your adapter card's manuals first, before modifying the default settings in the BIOS.

PCI IDE BusMaster

Set this value to allow or prevent the use of PCI IDE busmastering. The Optimal default setting is *Enabled*. The Fail-Safe default setting is *Disabled*.

Option	Description
Disabled	Set this value to prevent PCI bus mastering.
Enabled	This option specifies that the IDE controller on the PCI local bus hasmastering capabilities.

PCI/PnP Setup, Continued

OffBoard PCI/ISA IDE Card

Set this value to allow the OffBoard PCI/ISA IDE Card to be selected. The Optimal and Fail-Safe default setting is *Auto*.

Option	Description
Auto	This setting will auto select the location of an OffBoard PCI IDE adapter card. This is the default setting.
PCI Slot1	This setting will select PCI Slot 1 as the location of the OffBoard PCI IDE adapter card. Use this setting only if there is an IDE adapter card installed in PCI Slot 1.
PCI Slot2	This setting will select PCI Slot 2 as the location of the OffBoard PCI IDE adapter card. Use this setting only if there is an IDE adapter card installed in PCI Slot 2.
PCI Slot3	This setting will select PCI Slot 3 as the location of the OffBoard PCI IDE adapter card. Use this setting only if there is an IDE adapter card installed in PCI Slot 3. This option is available even if the motherboard does not have a PCI Slot 3. If the motherboard does not have a PCI Slot 3, do not use this setting.
PCI Slot4	This setting will select PCI Slot 4 as the location of the OffBoard PCI IDE adapter card. Use this setting only if there is an IDE adapter card installed in PCI Slot 4. This option is available even if the motherboard does not have a PCI Slot 4. If the motherboard does not have a PCI Slot 4, do not use this setting.
PCI Slot5	This setting will select PCI Slot 5 as the location of the OffBoard PCI IDE adapter card. Use this setting only if there is an IDE adapter card installed in PCI Slot 5. This option is available even if the motherboard does not have a PCI Slot 5. If the motherboard does not have a PCI Slot 5, do not use this setting.
PCI Slot6	This setting will select PCI Slot 6 as the location of the OffBoard PCI IDE adapter card. Use this setting only if there is an IDE adapter card installed in PCI Slot 6. This option is available even if the motherboard does not have a PCI Slot 6. If the motherboard does not have a PCI Slot 6, do not use this setting.

IRQ

Set this value to allow the IRQ settings to be modified. The Optimal and Fail-Safe default setting is *Available*.

Interrupt	Option	Description
IRQ3 IRQ4 IRQ5 IRQ7 IRQ9 IRQ10 IRQ11 IRQ14 IRQ15	Available	This setting allows the specified IRQ to be used by a PCI/PnP device. This is the default setting.
	Reserved	This setting allows the specified IRQ to be used by a legacy ISA device.

DMA

Set this value to allow the DMA setting to be modified. The optimal and Fail-Safe default setting is *Available.*

DMA Channel	Option	Description
DMA Channel 0 DMA Channel 1 DMA Channel 3 DMA Channel 5 DMA Channel 6 DMA Channel 7	Available	This setting allows the specified DMA to be used by PCI/PnP device. This is the default setting.
	Reserved	This setting allows the specified DMA to be used by a legacy ISA device.

PCI/PnP Setup, Continued

Reserved Memory Size

Set this value to allow the system to reserve memory that is used by ISA devices. The optimal and Fail-Safe default setting is *Disabled.*

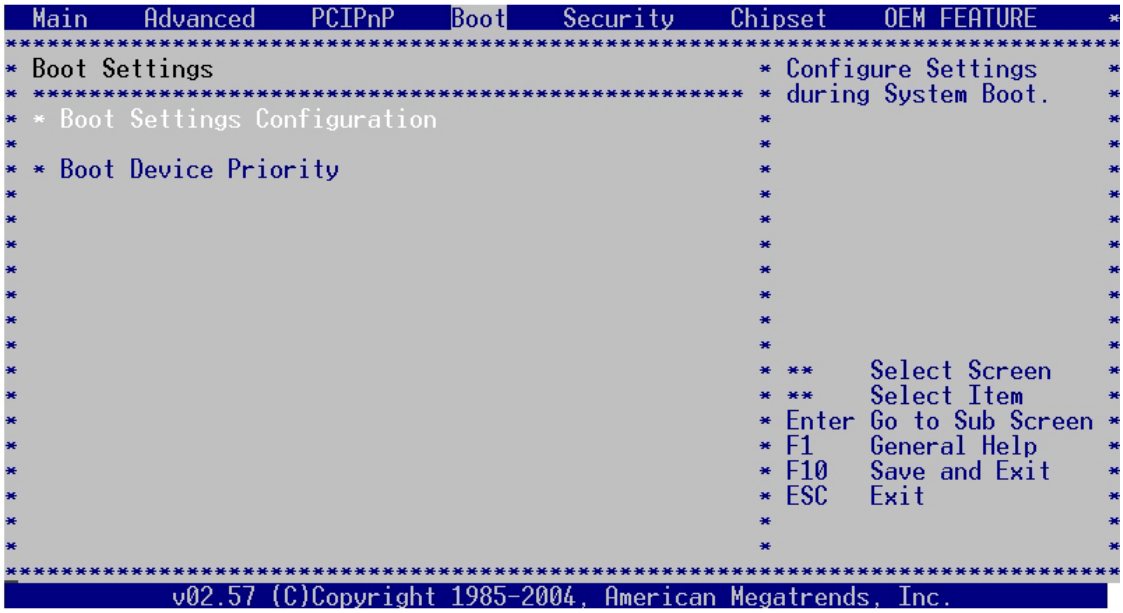
Option	Description
Disabled	Set this value to prevent BIOS from reserving memory to ISA devices.
16K	Set this value to allow the system to reserve 16K of the system memory to the ISA devices.
32K	Set this value to allow the system to reserve 32K of the system memory to the ISA devices.
64K	Set this value to allow the system to reserve 64K of the system memory to the ISA devices.

Chapter 5 Boot Setup

Select the *Boot* tab from the AM4001setup screen to enter the Boot BIOS Setup screen. You can select any of the items in the left frame of the screen, such as Boot Device Priority, to go to the sub menu for that item. You can display a Boot BIOS Setup option by highlighting it using the <Arrow> keys. All Boot Setup options are described in this section. Select an item on the Boot Setup screen to access the sub menu for:

- Boot Settings Configuration
- BIOS Boot Configuration Options

The Boot Setup screen is shown below:

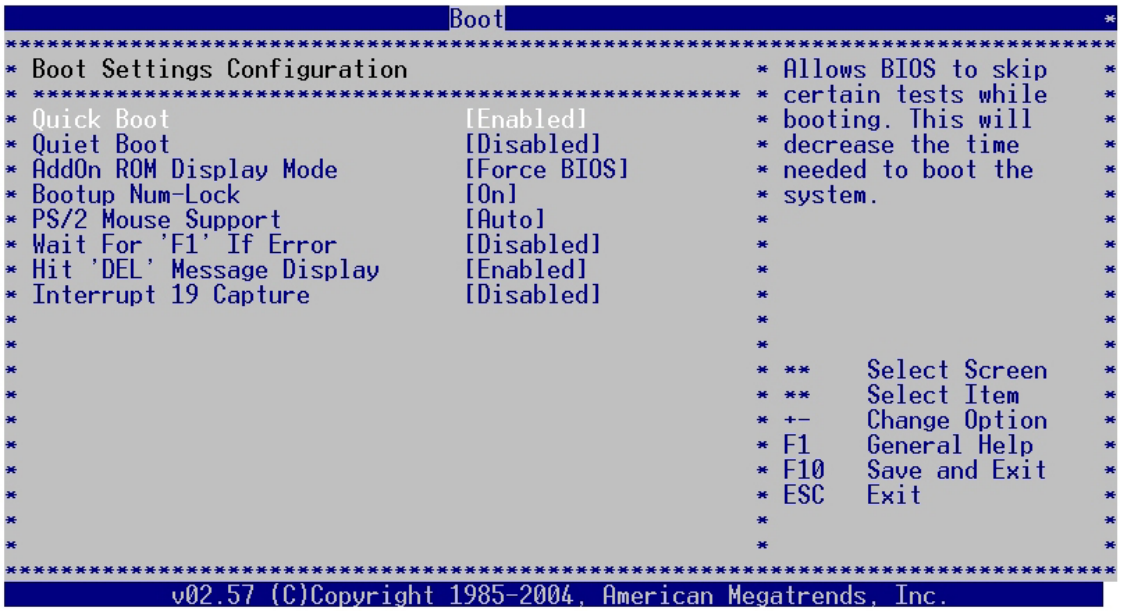


Boot Setup, Continued

BOOT SETTINGS CONFIGURATION

Boot Settings Configuration

Use this screen to select options for the Boot Settings Configuration. Use the up and down <Arrow> keys to select an item. Use the <Plus> and <Minus> keys to change the value of the selected option. The settings are described on the following pages. The screen is shown below.



Quick Boot

The Optimal and Fail-Safe default setting is *Enabled*.

Option	Description
Disabled	Set this value to allow the BIOS to perform all POST tests.
Enabled	Set this value to allow the BIOS to skip certain POST tests to boot faster. This is the default setting.

Quiet Boot

Set this value to allow the boot up screen options to be modified between POST messages or OEM logo. The Optimal and Fail-Safe default setting is *Disabled.*

Option	Description
Disabled	Set this value to allow the computer system to display the POST messages. This is the default setting.
Enabled	Set this value to allow the computer system to display the OEM logo.

Boot Setup, Continued

Add-On ROM Display Mode

Set this option to display add-on ROM (read-only memory) messages. The Optimal and Fail-Safe default setting is *Force BIOS*. An example of this is a SCSI BIOS or VGA BIOS.

Option	Description
Force BIOS	Set this value to allow the computer system to force a third party BIOS to display during system boot. This is the default setting.
Keep Current	Set this value to allow the computer system to display the AM4001information during system boot.

Bootup Num-Lock

Set this value to allow the Number Lock setting to be modified during boot-up. The Optimal and Fail-Safe default setting is *On.*

Option	Description
Off	This option does not enable the keyboard Number Lock automatically. To use the 10-keys on the keyboard, press the Number Lock key located on the upper left-hand corner of the 10-key pad. The Number Lock LED on the keyboard will light up when the Number Lock is engaged.
On	Set this value to allow the Number Lock on the keyboard to be enabled automatically when the computer system is boot up. This allows the immediate use of 10-keys numeric keypad located on the right side of the keyboard. To confirm this, the Number Lock LED light on the keyboard will be lit. This is the default setting.

PS/2 Mouse Support

Set this value to allow the PS/2 mouse support to be adjusted. The Optimal and Fail-Safe default setting is *Auto*.

Option	Description
Disabled	This option will prevent the PS/2 mouse port from using system resources and will prevent the port from being active. Use this setting if installing a serial mouse.
Enabled	Set this value to allow the system to use a PS/2 mouse.
Auto	Set this value to allow the system to automatically enable the PS/2 mouse support once a PS/2 mouse is connected. This is the default setting.

Wait for 'F1' If Error

Set this value to allow the Wait for 'F1' Error setting to be modified. The Optimal and Fail-Safe default setting is *Disabled*.

Option	Description
Disabled	This prevents the AM4001to wait on an error for user intervention. This setting should be used if there is a known reason for a BIOS error to appear. An example would be a system administrator must remote boot the system. The computer system does not have a keyboard currently attached. If this setting is set, the system will continue to boot up in to the operating system. If 'F1' is enabled, the system will wait until the BIOS setup is entered. This is the default setting.
Enabled	Set this value to allow the system BIOS to wait for any error. If an error is detected, pressing <F1> will enter Setup and the BIOS setting can be adjusted to fix the problem. This normally happens when upgrading the hardware and not setting the BIOS to recognize it.

Boot Setup, Continued

Hit 'DEL' Message Display

Set this value to allow the *Hit "DEL" to enter Setup* Message Display to be modified. The Optimal and Fail-Safe default setting is *Enabled*.

Option	Description
Disabled	This prevents the AM4001to display `Hit Del to enter Setup` during memory initialization. If Quiet Boot is enabled, the Hit 'DEL' message will not display.
Enabled	This allows the AM4001to display `Hit Del to enter Setup` during memory initialization. This is the default setting.

Interrupt 19 Capture

Set this value to allow option ROMs such as network controllers to trap BIOS interrupt 19. The Optimal and Fail-Safe default setting is *Disabled*.

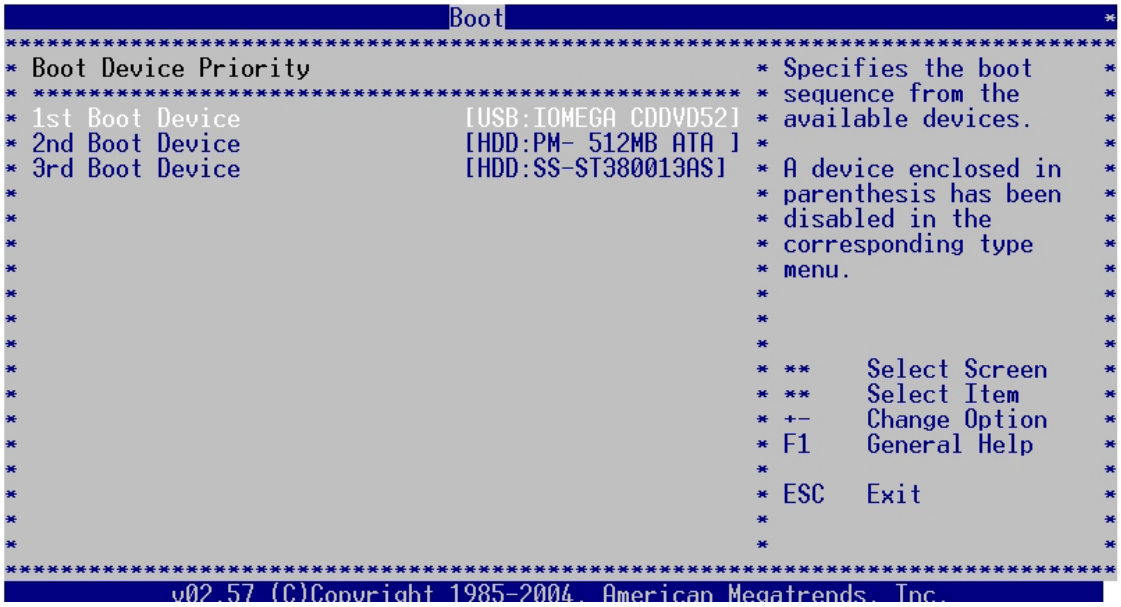
Option	Description
Disabled	The BIOS prevents option ROMs from trapping interrupt 19. This is the default setting.
Enabled	The BIOS allows option ROMs to trap interrupt 19.

Boot Setup, Continued

BOOT DEVICE PRIORITY

Boot Device Priority

Use this screen to specify the order in which the system checks for the device to boot from. To access this screen, select Boot Device Priority on the Boot Setup screen and press <Enter>. The following screen displays:



1st Boot Device
2nd Boot Device
3rd Boot Device

Set the boot device options to determine the sequence in which the computer checks which device to boot from. The settings are *Removable Dev., Hard Drive, or ATAPI CDROM.* The Optimal and Fail-Safe settings are:

- 1st boot device – Removable Device
- 2nd boot device – Hard Drive
- 3rd boot device – ATAPI CDROM

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Chapter 6 Security Setup

AM4001 Password Support

Two Levels of Password Protection

AM4001 provides both a Supervisor and a User password. If you use both passwords, the Supervisor password must be set first.

The system can be configured so that all users must enter a password every time the system boots or when AM4001 Setup is executed, using either or either the Supervisor password or User password.

The Supervisor and User passwords activate two different levels of password security. If you select password support, you are prompted for a one to six character password. Type the password on the keyboard. The password does not appear on the screen when typed. Make sure you write it down. If you forget it, you must drain NVRAM and reconfigure.

Remember the Password

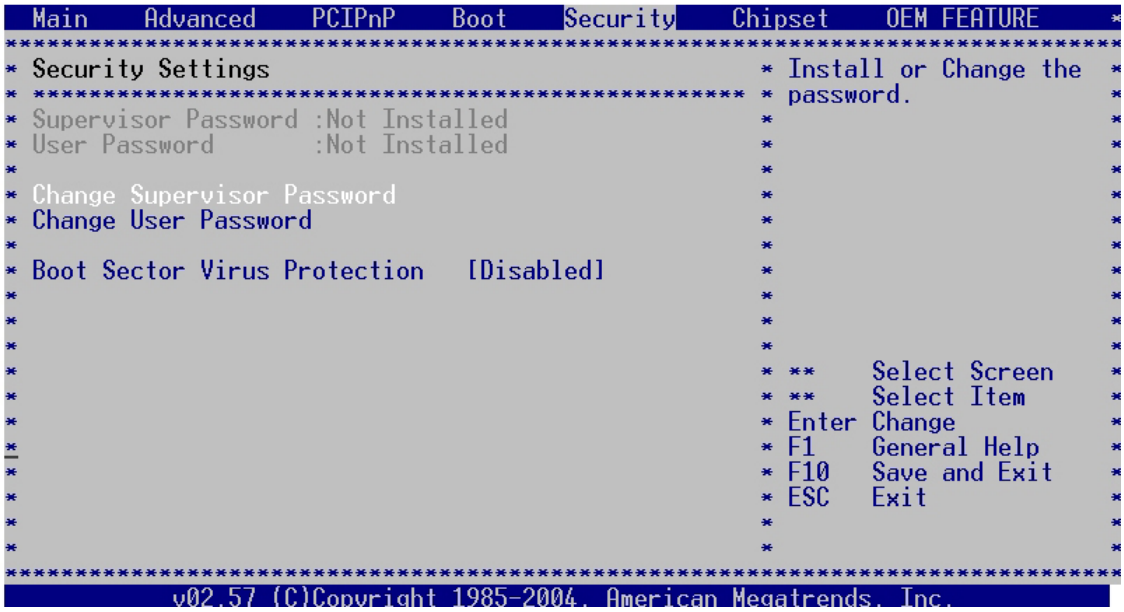
Keep a record of the new password when the password is changed. If you forget the password, you must erase the system configuration information in NVRAM. See (Deleting a Password) for information about erasing system configuration information.

Security Setup, Continued

Select Security Setup from the AM4001 Setup main BIOS setup menu. All Security Setup options, such as password protection and virus protection, are described in this section. To access the sub menu for the following items, select the item and press <Enter>:

- Change Supervisor Password
- Change User Password
- Clear User Password

The Security Setup screen is shown below. The sub menus are documented on the following pages.



Supervisor Password

Indicates whether a supervisor password has been set. If the password has been installed, *Installed* displays. If not, *Not Installed* displays.

User Password

Indicates whether a user password has been set. If the password has been installed, *Installed* displays. If not, *Not Installed* displays.

Cont'd

Security Setup, Continued

Change Supervisor Password

Select this option and press <Enter> to access the sub menu. You can use the sub menu to change the supervisor password.

Change User Password

Select this option and press <Enter> to access the sub menu. You can use the sub menu to change the user password.

Clear User Password

Select this option and press <Enter> to access the sub menu. You can use the sub menu to clear the user password.

Boot Sector Virus Protection

This option is near the bottom of the Security Setup screen. The Optimal and Fail-Safe default setting is *Disabled*

Option	Description
Disabled	Set this value to prevent the Boot Sector Virus Protection. This is the default setting.
Enabled	Select Enabled to enable boot sector protection. AM4001 displays a warning when any program (or virus) issues a Disk Format command or attempts to write to the boot sector of the hard disk drive. If enabled, the following appears when a write is attempted to the boot sector. You may have to type N several times to prevent the boot sector write. Boot Sector Write! Possible VIRUS: Continue (Y/N)? _ The following appears after any attempt to format any cylinder, head, or sector of any hard disk drive via the BIOS INT 13 Hard disk drive Service: Format!!! Possible VIRUS: Continue (Y/N)? _

CHANGE SUPERVISOR PASSWORD

Change Supervisor Password

Select Change Supervisor Password from the Security Setup menu and press <Enter>.

```
Enter New Password:
```

appears. Type the password and press <Enter>. The screen does not display the characters entered. Retype the password as prompted and press <Enter>. If the password confirmation is incorrect, an error message appears. The password is stored in NVRAM after AM4001 completes.

Change User Password

Select Change User Password from the Security Setup menu and press <Enter>.

```
Enter New Password:
```

appears. Type the password and press <Enter>. The screen does not display the characters entered. Retype the password as prompted and press <Enter>. If the password confirmation is incorrect, an error message appears. The password is stored in NVRAM after AM4001 completes.

Security Setup, Continued

Clear User Password

Select Clear User Password from the Security Setup menu and press <Enter>.

```
Clear New Password

[Ok] [Cancel]
```

appears. Type the password and press <Enter>. The screen does not display the characters entered. Retype the password as prompted and press <Enter>. If the password confirmation is incorrect, an error message appears. The password is stored in NVRAM after AM4001 completes.

Chapter 7 Chipset Setup

Select the *Chipset* tab from the AM4001 setup screen to enter the Chipset BIOS Setup screen. You can display a Chipset BIOS Setup option by highlighting it using the <Arrow> keys. All Chipset BIOS Setup options are described in this section. The Chipset BIOS Setup screen is shown below.



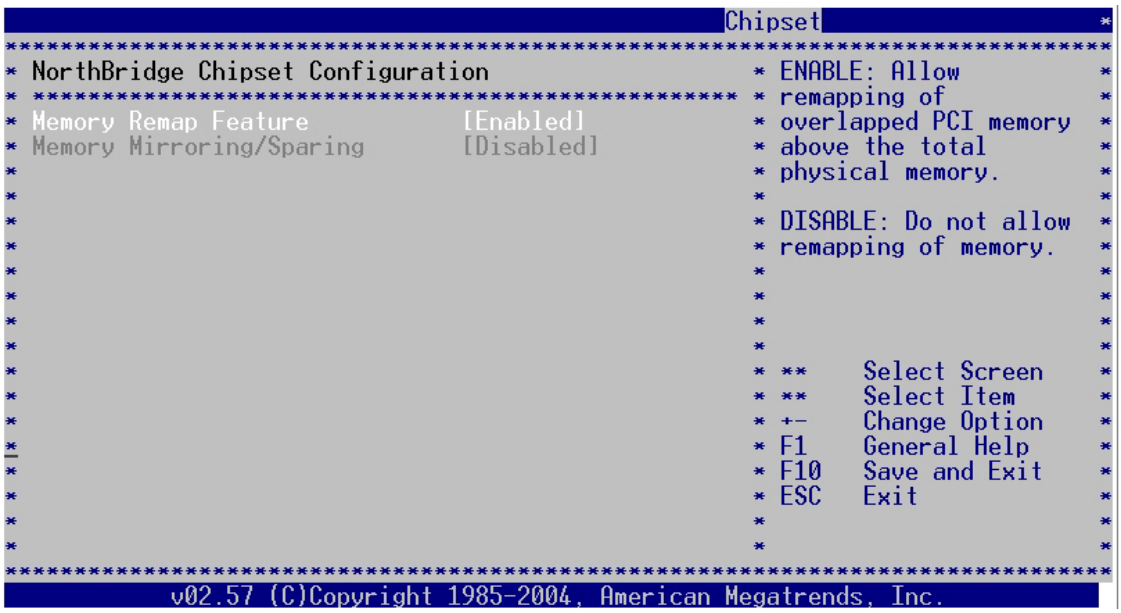
Chipset Setup, Continued

NORTH BRIDGE CONFIGURATION

North Bridge Configuration

You can use this screen to select options for the North Bridge Configuration. Use the up and down <Arrow> keys to select an item. Use the <Plus> and <Minus> keys to change the value of the selected option.

Note: The North Bridge Configuration setup screen varies depending on the supported North Bridge chipset.



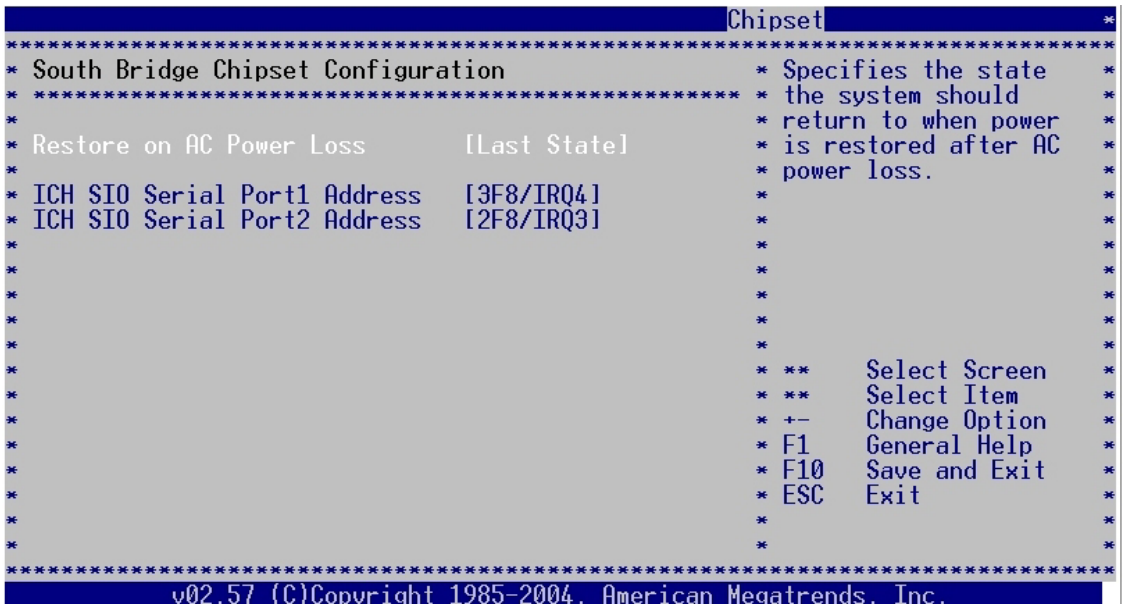
Chipset Setup, Continued

SOUTH BRIDGE CONFIGURATION

South Bridge Configuration

You can use this screen to select options for the South Bridge Configuration. South Bridge is a chipset on the motherboard that controls the basic I/O functions, USB ports, audio functions, modem functions, IDE channels, and PCI slots. Use the up and down <Arrow> keys to select an item. Use the <Plus> and <Minus> keys to change the value of the selected option.

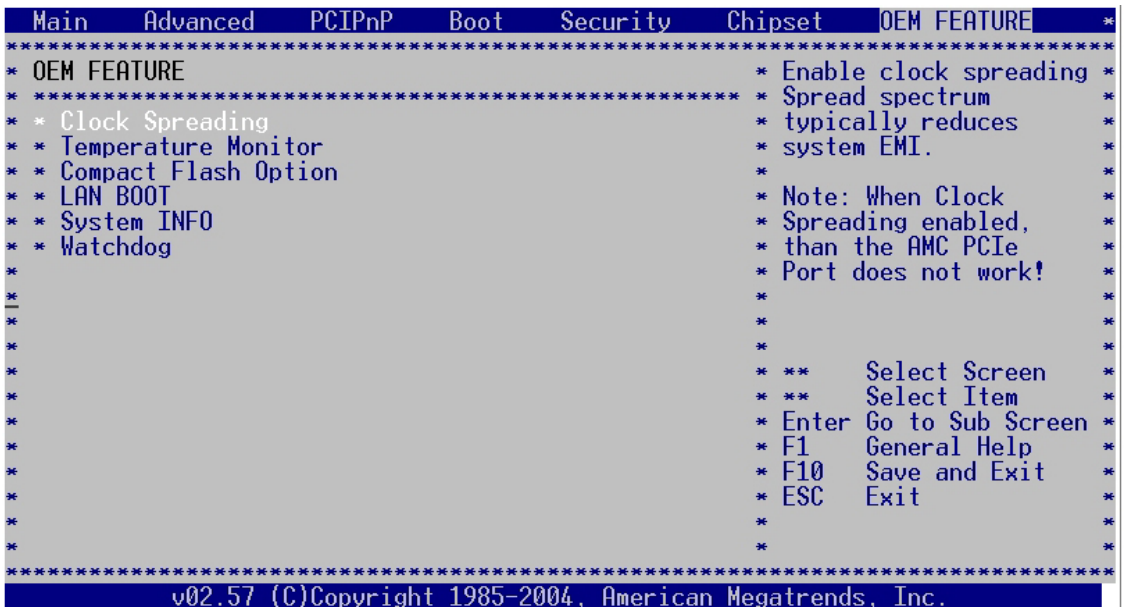
Note: The South Bridge Configuration setup screen varies depending on the supported South Bridge chipset.



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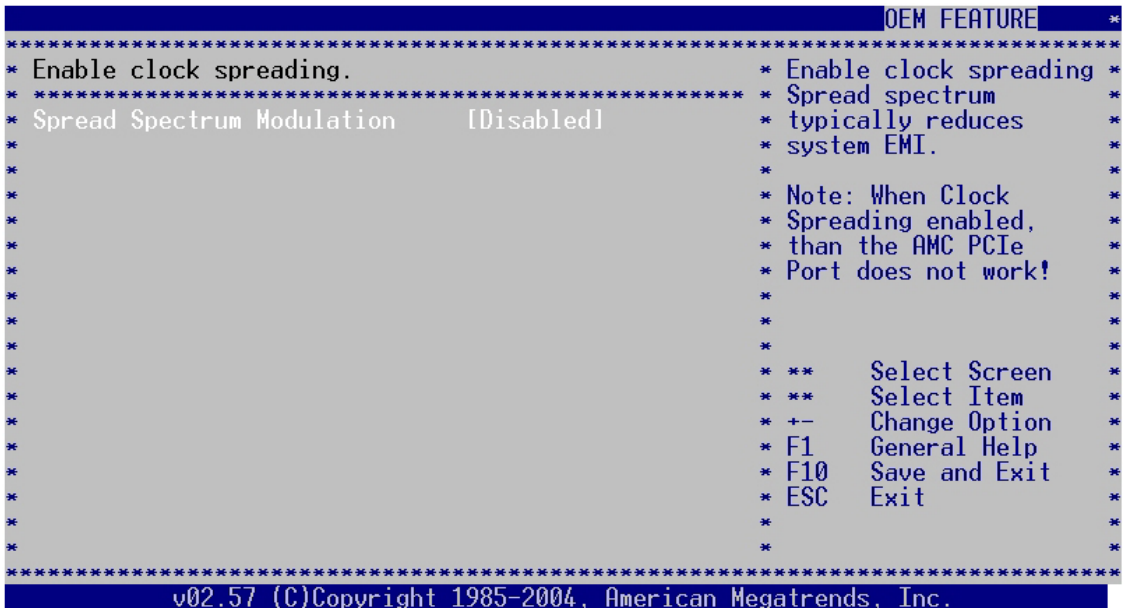
Chapter 8 OEM Feature

Select the OEM Feature tab from the AM4001 setup screen to enter the Kontron specific BIOS Setup screen. You can display a Kontron BIOS Setup option by highlighting it using the <Arrow>keys. All OEM Feature BIOS Setup options are described in this section.



CLOCK SPREADING

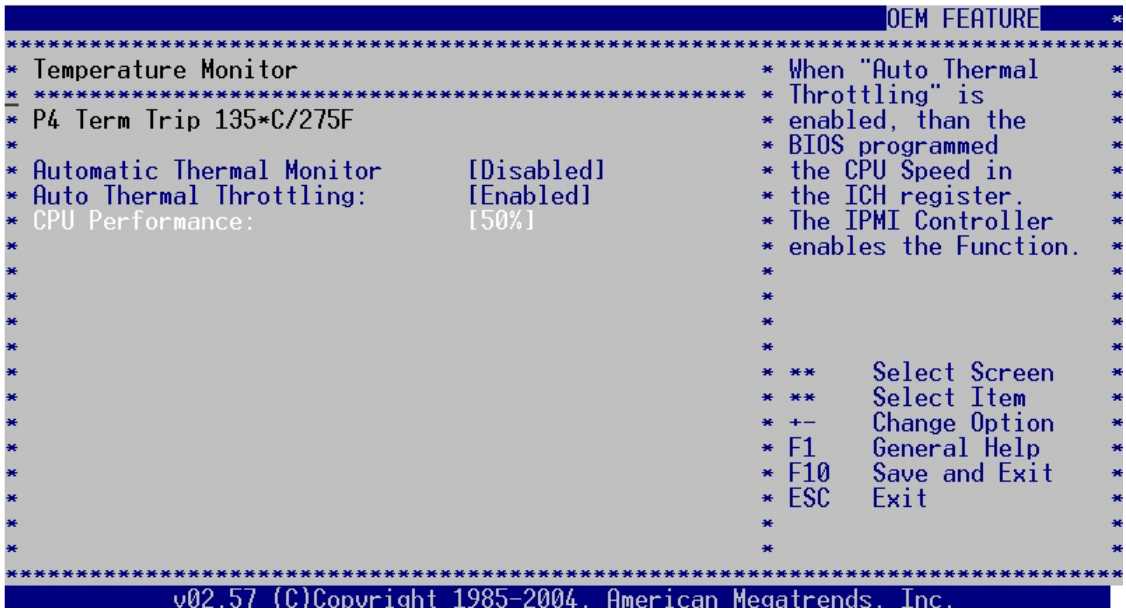
The Optimal and Fail-Safe default setting is *Disabled*.



Option	Description
Disabled	No Clock Spectrum Modulation. This is the default setting.
Enabled	0.5% Clock Spreading. Spread spectrum typically reduces system EMI

OEM Feature, Continued

TEMPERATURE MONITOR



P4 Term Trip 135°C/275F

Shows the P4 max. Temperature

Automatic Thermal Monitor

Thermal Monitor is enabled and when the die temperature is very near to the temperature limits of the processor, the clocks will be modulated by alternately turning the clocks off and on at a duty cycle of 50%. The Optimal and Fail-Safe default setting is *Disabled*.

Auto Thermal Throttling

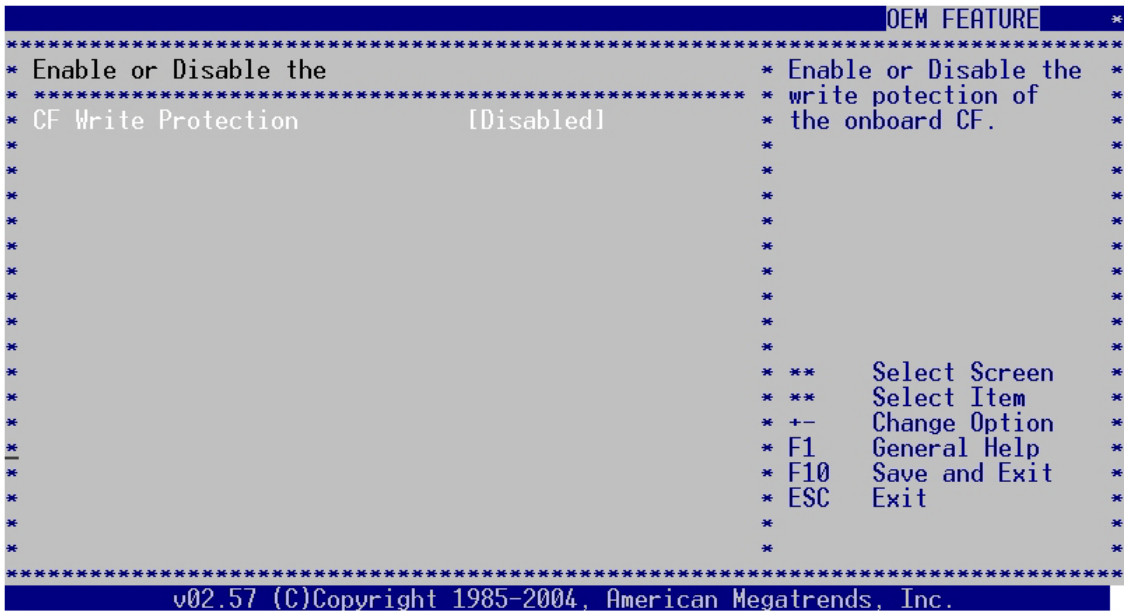
The BIOS programmed the CPU speed in the ICH register. The IPMI controller enables the throttling. The Optimal and Fail-Safe default setting is *Disabled*.

CPU Performance

The CPU performance will be reduced to the selected value when reaching the temperature threshold. CPU Performance 12.5%; 25%; 50%; 75%

OEM Feature, Continued

COMPACTFLASH OPTION

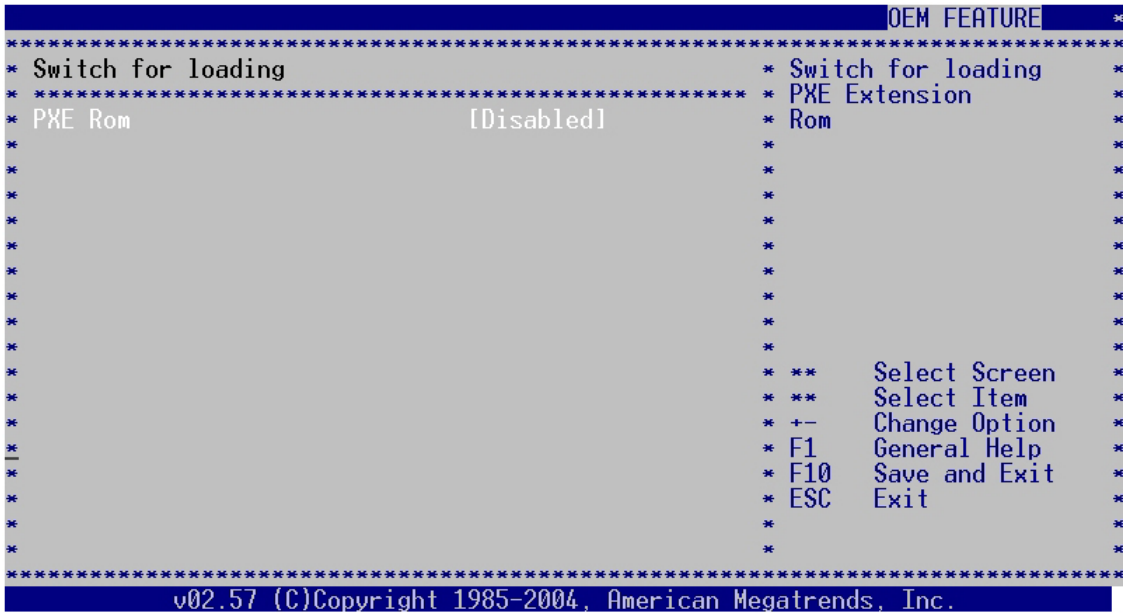


CF Write Protection

Enables the write protection for the onboard CompactFlash. The Optimal and Fail-Safe default setting is *Disabled.*

OEM Feature, Continued

LAN BOOT

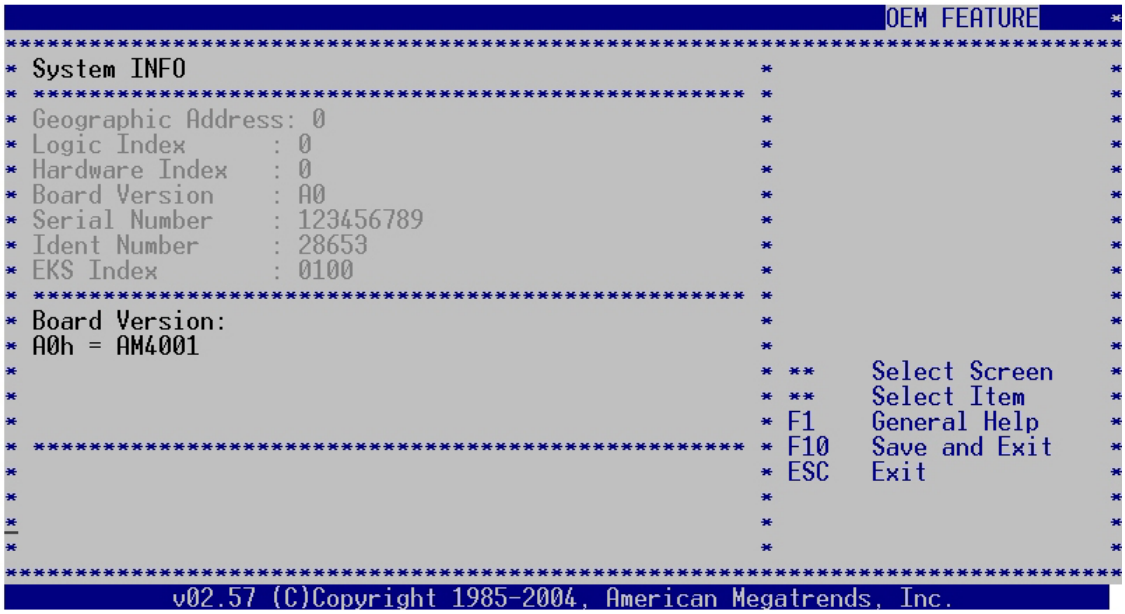


PXE ROM

Enable LAN Boot. When enabled, the BIOS loads the option ROM for PXE Boot. The Optimal and Fail-Safe default setting is *Disabled.*

OEM Feature, Continued

SYSTEM INFO



Geographic Addressing:

Displays the slot in which the card is placed starting on the Left side with address 0.

Logic Index

This is a display only field, which reflects the value of an onboard register. It shows the index of the onboard logic.

Hardware Index

This is a display only field, which reflects the value of an onboard register. It shows the index of the Hardware Index.

Board Version

This is a display only field, which reflects the value of an onboard register. This must always correspond with the CPU on which the BIOS is installed.
Compare the value with the table below**.**

System Slot

Displays whether the board is in a system slot or not.

Serial Number

This is a display only field, which shows Kontron internal information about the board. The serial number is unique to each board produced by Kontron Modular Computers. It could also be used by the customer to identify specific boards.

Ident Number

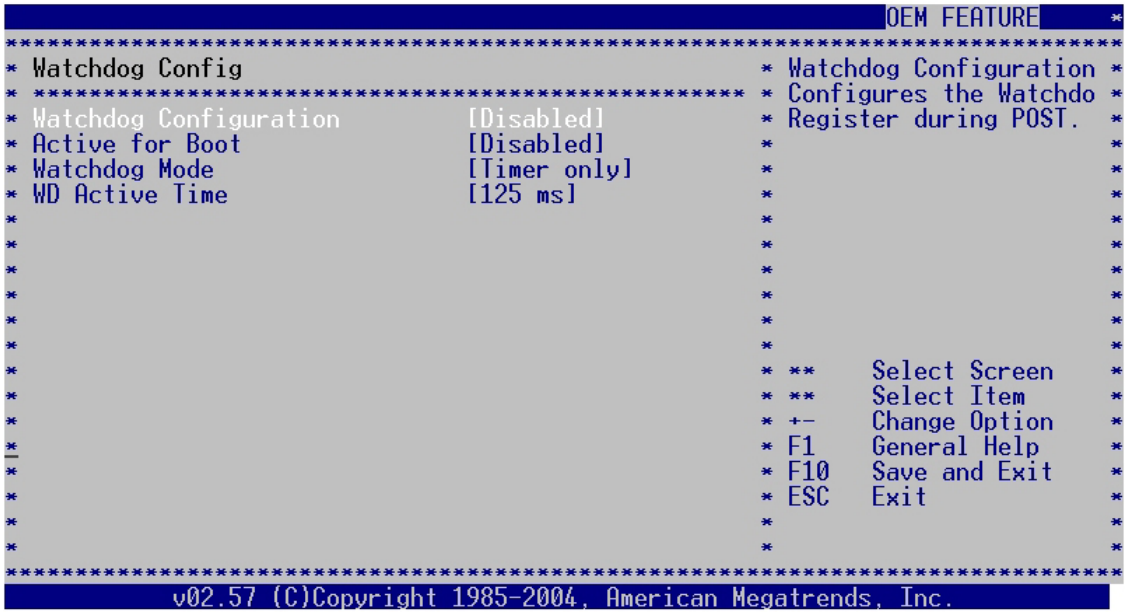
This is a display only field, which shows Kontron internal information about the board.

EKS Index

This is a display only field, which shows Kontron internal information about the board. The EKS index refers to the production number and version respectively. It could also be used by the customer to identify specific boards.

OEM Feature, Continued

WATCHDOG



Watchdog Configuration

The Optimal and Fail-Safe default setting is *Disabled.*

Option	Description
Disabled	No watchdog configuration during POST.
Enabled	BIOS configures the watchdog registers during POST

Active for boot

The Optimal and Fail-Safe default setting is *Disabled.*

Option	Description
Disabled	Watchdog must be started form the OS.
Enabled	Select Enabled if the watchdog timer requires to be started before the operating system is booted from the BIOS.

Watchdog Mode

The Optimal and Fail-Safe default setting is *Timer only.*

Option	Description
Timer only Reset Interrupt Cascade (INT + Reset)	Reserve resource 280 h and IRQ5 for watchdog function.

OEM Feature, Continued

WD Active Time

The Optimal and Fail-Safe default setting is *125 ms*.

Option	Description
125ms, 250 ms, 500ms, 1s, 2s, 4s, 8s, 16s, 32s, 64s, 128s, 256s	Select the time after which the action selected occurs., if watchdog timer is not retriggered.

Interrupt Configuration

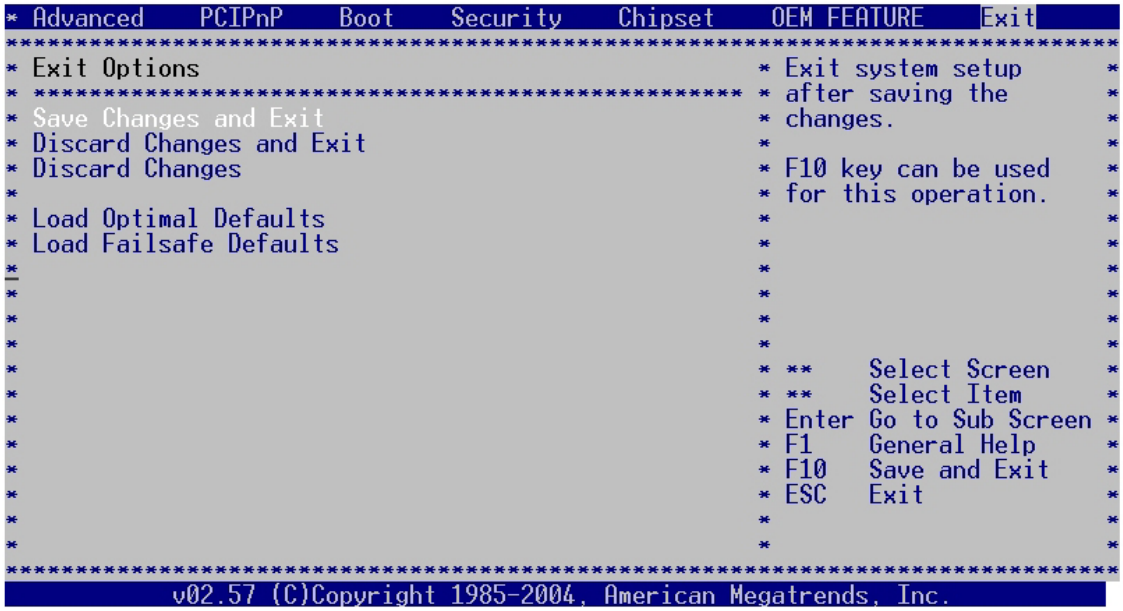
The Optimal and Fail-Safe default setting is *Disabled.*

Option	Description
Disabled	Watchdog must be started form the OS.
IRQ5	Watchdog routing to IRQ5
NMI	Watchdog routing to NMI

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Chapter 9 Exit Menu

Select the *Exit* tab from the AM4001 setup screen to enter the Exit BIOS Setup screen. You can display an Exit BIOS Setup option by highlighting it using the <Arrow> keys. All Exit BIOS Setup options are described in this section. The Exit BIOS Setup screen is shown below.



Save Changes and Exit

When you have completed the system configuration changes, select this option to leave AM4001 Setup and reboot the computer so the new system configuration parameters can take effect. Select Exit Saving Changes from the Exit menu and press <Enter>.

```
Save Configuration Changes and Exit Now?

[Ok]   [Cancel]
```

appears in the window. Select Ok to save changes and exit.

Exit Menu, Continued

Discard Changes and Exit

Select this option to quit AM4001 Setup without making any permanent changes to the system configuration. Select Exit Discarding Changes from the Exit menu and press <Enter>.

```
Discard Changes and Exit Setup Now?

[Ok]   [Cancel]
```

appears in the window. Select *Ok* to discard changes and exit.

Discard Changes

Select Discard Changes from the Exit menu and press <Enter>.



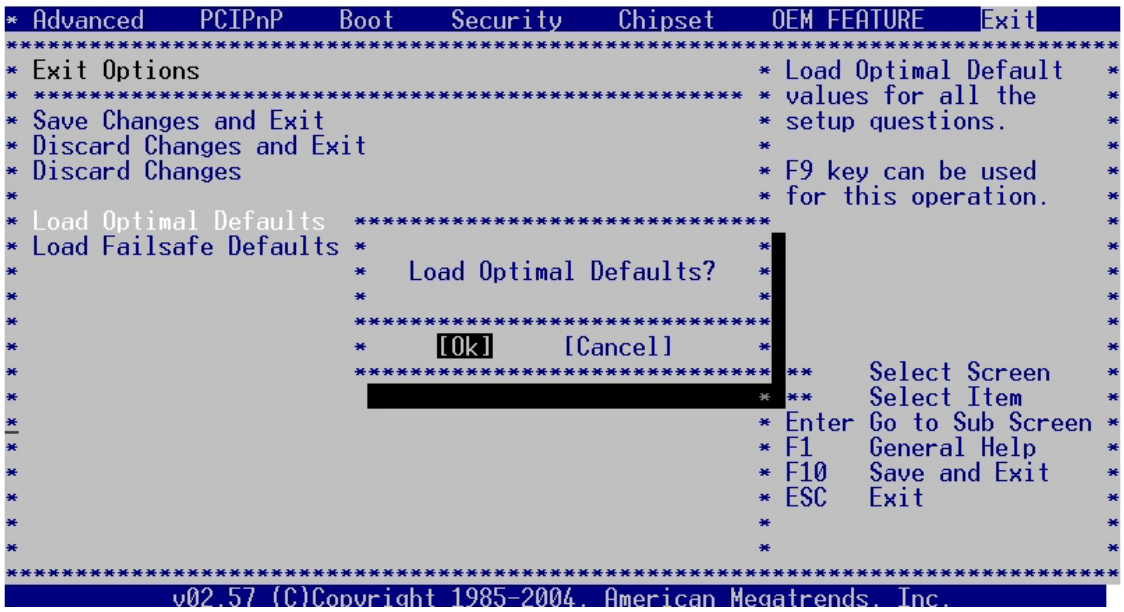
Select *Ok* to discard changes.

Exit Menu, Continued

Load Optimal Defaults

AM4001 automatically sets all AM4001 Setup options to a complete set of default settings when you Select this option. The Optimal settings are designed for maximum system performance, but may not work best for all computer applications. In particular, do not use the Optimal AM4001 Setup options if your computer is experiencing system configuration problems.

Select Load Optimal Defaults from the Exit menu and press <Enter>.



Select *Ok* to load optimal defaults.

Load Fail-Safe Defaults

AM4001 automatically sets all AM4001 Setup options to a complete set of default settings when you Select this option. The Fail-Safe settings are designed for maximum system stability, but not maximum performance. Select the Fail-Safe AM4001 Setup options if your computer is experiencing system configuration problems.
Select Load Fail-Safe Defaults from the Exit menu and press <Enter>.

```
Load Fail-Safe Defaults?

[Ok]    [Cancel]
```

appears in the window. Select *Ok* to load Fail-Safe defaults.

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Chapter 10 Deleting a Password

If you forget the passwords you set up through AM4001 Setup, the only way you can reset the password is to erase the system configuration information where the passwords are stored. System configuration data is stored in CMOS RAM, a type of memory that consumes very little power.

Erase Old Password

You can drain CMOS RAM power by using the CMOS drain jumper on the motherboard, or by removing the battery. CMOS RAM looses it content including the password when it is drained.

Note: For more information on draining CMOS using the drain jumper, see the motherboard user's manual.

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Chapter 11 POST Codes

Bootblock Initialization Code Checkpoints

The Bootblock initialization code sets up the chipset, memory and other components before system memory is available. The following table describes the type of checkpoints that may occur during the bootblock initialization portion of the BIOS:

Checkpoint	Description
Before D1	Early chipset initialization is done. Early super I/O initialization is done including RTC and keyboard controller. NMI is disabled.
D1	Perform keyboard controller BAT test. Check if waking up from power management suspend state. Save power-on CPUID value in scratch CMOS.
D0	Go to flat mode with 4GB limit and GA20 enabled. Verify the bootblock checksum.
D2	Disable CACHE before memory detection. Execute full memory sizing module. Verify that flat mode is enabled.
D3	If memory sizing module not executed, start memory refresh and do memory sizing in Bootblock code. Do additional chipset initialization. Re-enable CACHE. Verify that flat mode is enabled.
D4	Test base 512KB memory. Adjust policies and cache first 8MB. Set stack.
D5	Bootblock code is copied from ROM to lower system memory and control is given to it. BIOS now executes out of RAM.
D6	Both key sequence and OEM specific method is checked to determine if BIOS recovery is forced. Main BIOS checksum is tested. If BIOS recovery is necessary, control flows to checkpoint E0. See *Bootblock Recovery Code Checkpoints* section of document for more information.
D7	Restore CPUID value back into register. The Bootblock-Runtime interface module is moved to system memory and control is given to it. Determine whether to execute serial flash.
D8	The Runtime module is uncompressed into memory. CPUID information is stored in memory.
D9	Store the Uncompressed pointer for future use in PMM. Copying Main BIOS into memory. Leaves all RAM below 1MB Read-Write including E000 and F000 shadow areas but closing SMRAM.
DA	Restore CPUID value back into register. Give control to BIOS POST (ExecutePOSTKernel). See *POST Code Checkpoints* section of document for more information.

Bootblock Recovery Code Checkpoints

The Bootblock recovery code gets control when the BIOS determines that a BIOS recovery needs to occur because the user has forced the update or the BIOS checksum is corrupt. The following table describes the type of checkpoints that may occur during the Bootblock recovery portion of the BIOS:

Checkpoint	Description
E0	Initialize the floppy controller in the super I/O. Some interrupt vectors are initialized. DMA controller is initialized. 8259 interrupt controller is initialized. L1 cache is enabled.
E9	Set up floppy controller and data. Attempt to read from floppy.
EA	Enable ATAPI hardware. Attempt to read from ARMD and ATAPI CDROM.
EB	Disable ATAPI hardware. Jump back to checkpoint E9.
EF	Read error occurred on media. Jump back to checkpoint EB.
E9 or EA	Determine information about root directory of recovery media.
F0	Search for pre-defined recovery file name in root directory.
F1	Recovery file not found.
F2	Start reading FAT table and analyze FAT to find the clusters occupied by the recovery file.
F3	Start reading the recovery file cluster by cluster.
F5	Disable L1 cache.
FA	Check the validity of the recovery file configuration to the current configuration of the flash part.
FB	Make flash write enabled through chipset and OEM specific method. Detect proper flash part. Verify that the found flash part size equals the recovery file size.
F4	The recovery file size does not equal the found flash part size.
FC	Erase the flash part.
FD	Program the flash part.
FF	The flash has been updated successfully. Make flash write disabled. Disable ATAPI hardware. Restore CPUID value back into register. Give control to F000 ROM at F000:FFF0h.

POST Code Checkpoints

The POST code checkpoints are the largest set of checkpoints during the BIOS pre-boot process. The following table describes the type of checkpoints that may occur during the POST portion of the BIOS:

Checkpoint	Description
03	Disable NMI, Parity, video for EGA, and DMA controllers. Initialize BIOS, POST, Runtime data area. Also initialize BIOS modules on POST entry and GPNV area. Initialized CMOS as mentioned in the Kernel Variable "wCMOSFlags."
04	Check CMOS diagnostic byte to determine if battery power is OK and CMOS checksum is OK. Verify CMOS checksum manually by reading storage area. If the CMOS checksum is bad, update CMOS with power-on default values and clear passwords. Initialize status register A. Initializes data variables that are based on CMOS setup questions. Initializes both the 8259 compatible PICs in the system
05	Initializes the interrupt controlling hardware (generally PIC) and interrupt vector table.
06	Do R/W test to CH-2 count reg. Initialize CH-0 as system timer. Install the POSTINT1Ch handler. Enable IRQ-0 in PIC for system timer interrupt. Traps INT1Ch vector to "POSTINT1ChHandlerBlock."
08	Initializes the CPU. The BAT test is being done on KBC. Program the keyboard controller command byte is being done after Auto detection of KB/MS using AMI KB-5.
C0	Early CPU Init Start -- Disable Cache - Init Local APIC
C1	Set up boot strap proccessor Information
C2	Set up boot strap proccessor for POST
C5	Enumerate and set up application proccessors
C6	Re-enable cache for boot strap proccessor
C7	Early CPU Init Exit
0A	Initializes the 8042 compatible Key Board Controller.
0B	Detects the presence of PS/2 mouse.
0C	Detects the presence of Keyboard in KBC port.
0E	Testing and initialization of different Input Devices. Also, update the Kernel Variables. Traps the INT09h vector, so that the POST INT09h handler gets control for IRQ1. Uncompress all available language, BIOS logo, and Silent logo modules.
13	Early POST initialization of chipset registers.
24	Uncompress and initialize any platform specific BIOS modules.
30	Initialize System Management Interrupt.
2A	Initializes different devices through DIM. See *DIM Code Checkpoints* section of document for more information.
2C	Initializes different devices. Detects and initializes the video adapter installed in the system that have optional ROMs.
2E	Initializes all the output devices.
31	Allocate memory for ADM module and uncompress it. Give control to ADM module for initialization. Initialize language and font modules for ADM. Activate ADM module.

POST Code Checkpoints, Continued

Checkpoint	Description
33	Initializes the silent boot module. Set the window for displaying text information.
37	Displaying sign-on message, CPU information, setup key message, and any OEM specific information.
38	Initializes different devices through DIM. See *DIM Code Checkpoints* section of document for more information.
39	Initializes DMAC-1 & DMAC-2.
3A	Initialize RTC date/time.
3B	Test for total memory installed in the system. Also, Check for DEL or ESC keys to limit memory test. Display total memory in the system.
3C	Mid POST initialization of chipset registers.
40	Detect different devices (Parallel ports, serial ports, and coprocessor in CPU, … etc.) successfully installed in the system and update the BDA, EBDA…etc.
50	Programming the memory hole or any kind of implementation that needs an adjustment in system RAM size if needed.
52	Updates CMOS memory size from memory found in memory test. Allocates memory for Extended BIOS Data Area from base memory.
60	Initializes NUM-LOCK status and programs the KBD typematic rate.
75	Initialize Int-13 and prepare for IPL detection.
78	Initializes IPL devices controlled by BIOS and option ROMs.
7A	Initializes remaining option ROMs.
7C	Generate and write contents of ESCD in NVRam.
84	Log errors encountered during POST.
85	Display errors to the user and gets the user response for error.
87	Execute BIOS setup if needed / requested.
8C	Late POST initialization of chipset registers.
8D	Build ACPI tables (if ACPI is supported)
8E	Program the peripheral parameters. Enable/Disable NMI as selected
90	Late POST initialization of system management interrupt.
A0	Check boot password if installed.
A1	Clean-up work needed before booting to OS.
A2	Takes care of runtime image preparation for different BIOS modules. Fill the free area in F000h segment with 0FFh. Initializes the Microsoft IRQ Routing Table. Prepares the runtime language module. Disables the system configuration display if needed.
A4	Initialize runtime language module.
A7	Displays the system configuration screen if enabled. Initialize the CPU's before boot, which includes the programming of the MTRRs.
A8	Prepare CPU for OS boot including final MTRR values.
A9	Wait for user input at config display if needed.
AA	Uninstall POST INT1Ch vector and INT09h vector. Deinitializes the ADM module.
AB	Prepare BBS for Int 19 boot.
AC	End of POST initialization of chipset registers.
B1	Save system context for ACPI.
00	Passes control to OS Loader (typically INT19h).

DIM Code Checkpoints

The Device Initialization Manager module gets control at various times during BIOS POST to initialize different BUSes. The following table describes the main checkpoints where the DIM module is accessed:

Checkpoint	Description
2A	Initialize different buses and perform the following functions: Reset, Detect, and Disable (function 0); Static Device Initialization (function 1); Boot Output Device Initialization (function 2). Function 0 disables all device nodes, PCI devices, and PnP ISA cards. It also assigns PCI bus numbers. Function 1 initializes all static devices that include manual configured onboard peripherals, memory and I/O decode windows in PCI-PCI bridges, and noncompliant PCI devices. Static resources are also reserved. Function 2 searches for and initializes any PnP, PCI, or AGP video devices.
38	Initialize different buses and perform the following functions: Boot Input Device Initialization (function 3); IPL Device Initialization (function 4); General Device Initialization (function 5). Function 3 searches for and configures PCI input devices and detects if system has standard keyboard controller. Function 4 searches for and configures all PnP and PCI boot devices. Function 5 configures all onboard peripherals that are set to an automatic configuration and configures all remaining PnP and PCI devices.

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