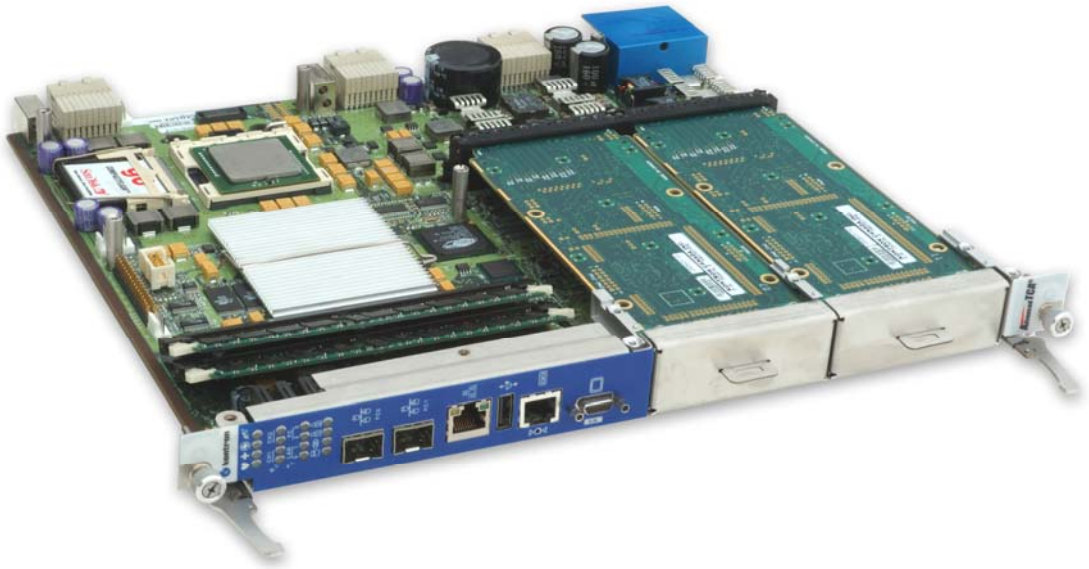
AT8001 User's Guide

AdvancedTCA

Document Revision 1.0



kontron

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Before You Begin

Before handling the board, read the instructions and safety guidelines on the following pages to prevent damage to the product and to ensure your own personal safety. Refer to the "Advisories" section in the Preface for advisory conventions used in this user's guide, including the distinction between Warnings, Cautions, Important Notes, and Notes.

- Always use caution when handling/operating the computer. Only qualified, experienced, authorized electronics service personnel should access the interior of the computer. The power supplies produce high voltages and energy hazards, which can cause bodily harm.

- Use extreme caution when installing or removing components. Refer to the installation instructions in this user's guide for precautions and procedures. If you have any questions, please contact Kontron Technical Support.

WARNING



High voltages are present inside the chassis when the unit's power cord is plugged into an electrical outlet. Turn off system power, turn off the power supply, and then disconnect the power cord from its source before removing the chassis cover. Turning off the system power switch does not remove power to components.



WARNING



This product may contain CLASS 1 LASER PRODUCT



When Working Inside a Computer

Before taking covers off a computer, perform the following steps:

Turn off the computer and any peripherals.

Disconnect the computer and peripherals from power sources or subsystems to prevent electric shock or systemboard damage. This does not apply to when hot-swapping parts.

Follow the guidelines provided in “Preventing Electrostatic Discharge“ on the following page.

Disconnect telephone or telecommunications lines from the computer.

In addition, take note of these safety guidelines when appropriate:

- To help avoid possible damage to system boards, wait five seconds after turning off the computer before removing a component, removing a system board, or disconnecting a peripheral device from the computer.

- When you disconnect a cable, pull on its connector or on its strain-relief loop, not on the cable itself. Some cables have a connector with locking tabs. If you are disconnecting this type of cable, press in on the locking tabs before disconnecting the cable. As you pull connectors apart, keep them evenly aligned to avoid bending any connector pins. Also, before connecting a cable, make sue both connectors are correctly oriented and aligned.

CAUTION



Do not attempt to service the system yourself, except as explained in this user’s guide. Follow installation and troubleshooting instructions closely.



Preventing Electrostatic Discharge

Static electricity can harm system boards. Perform service at an ESD workstation and follow proper ESD procedure to reduce the risk of damage to components. Kontron strongly encourages you to follow proper ESD procedure, which can include wrist straps and smocks, when servicing equipment.

Take the following steps to prevent damage from electrostatic discharge (ESD):

- When unpacking a static-sensitive component from its shipping carton, do not remove the component's antistatic packing material until you are ready to install the component in a computer. Just before unwrapping the antistatic packaging, be sure you are at an ESD workstation or grounded. This will discharge any static electricity that may have built up in your body.

- When transporting a sensitive component, first place it in an antistatic container or packaging.

- Handle all sensitive components at an ESD workstation. If possible, use antistatic floor pads and workbench pads.

- Handle components and boards with care. Don't touch the components or contacts on a board. Hold a board by its edges or by its metal mounting bracket.

- Do not handle or store system boards near strong electrostatic, electromagnetic, magnetic, or radioactive fields.

Preface

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How to Use This Guide

This user's guide is designed to be used as step-by-step instructions for installation, and as a reference for operation, troubleshooting, and upgrades.

You can find the latest release of this User's Guide at:
http://www.kontron.com or at: ftp://ftp.kontron.ca/support/

For the circuits, descriptions and tables indicated, Kontron assumes no responsibility as far as patents or other rights of third parties are concerned.

The following is a summary of chapter contents:

- Chapter 1, Product Description
- Chapter 2, Onboard Features
- Chapter 3, Installing the board
- Chapter 4, Building an ATCA System
- Chapter 5, Software Setup
- Appendix A, Memory & I/O Maps
- Appendix B, Interrupt Lines
- Appendix C Kontron Extension Registers
- Appendix D, Connector Pinout
- Appendix E, BIOS Setup Error Codes
- Appendix F, Software Update
- Appendix G, Getting Help

Customer Comments

If you have any difficulties using this user's guide, discover an error, or just want to provide some feedback, please send a message to: Tech.Writer@ca.kontron.com. Detail any errors you find. We will correct the errors or problems as soon as possible and post the revised user's guide on our Web site. Thank you.

Advisory Conventions

Seven types of advisories are used throughout the user guides to provide helpful information or to alert you to the potential for hardware damage or personal injury. They are Note, Signal Paths, Related Jumpers, BIOS Settings, Software Usage, Cautions, and Warnings. The following is an example of each type of advisory. Use caution when servicing electrical components.



Note :
Indicate information that is important for you to know



Signal Paths:
Indicate the places where you can fin the signal on the board



Related Jumpers:
Indicate the jumpers that are related to this sections



BIOS Settings :
Indicate where you can set this option in the BIOS



Software Usage :
Indicates how you can access this feature through software.

CAUTION



Indicate potential damage to hardware and tells you how to avoid the problem.



WARNING



Indicates potential for bodily harm and tells you how to avoid the problem.



Disclaimer: We have tried to identify all situations that may pose a warning or a caution condition in this user's guide. However, Kontron does not claim to have covered all situations that might require the use of a Caution or a Warning.

Unpacking

Follow these recommendations while unpacking:

- Remove all items from the box. If any items listed on the purchase order are missing, notify Kontron customer service immediately.
- Inspect the product for damage. If there is damage, notify Kontron customer service immediately.
- Save the box and packing material for possible future shipment.

Powering Up the System

Before any installation or setup, ensure that the board is unplugged from power sources or subsystems.
If you encounter a problem, verify the following items:

- Make sure that all connectors are properly connected.
- Verify your boot devices.
- If the system does not start properly, try booting without any other I/O peripherals attached, including AMC or PMC adapters.

If you still cannot start your system, please refer to the Emergency Procedure in the Appendix Section of this User's Guide.

Make sure your system provides the minimum DC voltages required at the board's slot, especially if DC power is carried by cables.

If you are still not able to get your board running, contact our Technical Support for assistance.

Adapter Cables

Because adapter cables come from various manufacturers, pinouts can differ. The direct crimp design offered by Kontron allows the simplest cable assembly. All cables are available from Kontron Sales Department.

Storing Boards

Electronic boards are sensitive devices. Do not handle or store device near strong electrostatic, electromagnetic, magnetic or radioactive fields.

Regulatory Compliance Statements

This section provides the FCC compliance statement for Class B devices and describes how to keep the system CE compliant.

FCC Compliance Statement for Class B Devices

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generated, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experience radio/TV technician for help.

WARNING



This is a Class B product. If not installed in a properly shielded enclosure and used in accordance with this User's Guide, this product may cause radio interference in which case users may need to take additional measures at their own expense.



UL Certification



This product bears the combined UL Recognized Component Mark for Canada and U.S. It indicates investigations to the UL Standard for Safety of Information Technology Equipment, Including Electrical Business Equipment. It is destinated to be used in end-product equipment where the acceptability of the combination is determined by Underwriters Laboratories Inc.

CE Certification



The product(s) described in this user's guide complies with all applicable European Union (CE) directives if it has a CE marking. For computer systems to remain CE compliant, only CE-compliant parts may be used. Maintaining CE compliance also requires proper cable and cabling techniques. Although Kontron offers accessories, the customer must ensure that these products are installed with proper shielding to maintain CE compliance. Kontron does not offer engineering services for designing cabling systems. In addition, Kontron will not retest or recertify systems or components that have been reconfigured by customers.

Limited Warranty

Kontron grants the original purchaser of Kontron's products a ***TWO YEAR LIMITED HARDWARE WARRANTY*** as described in the following. However, no other warranties that may be granted or implied by anyone on behalf of Kontron are valid unless the consumer has the express written consent of Kontron.

Kontron warrants their own products, excluding software, to be free from manufacturing and material defects for a period of 24 consecutive months from the date of purchase. This warranty is not transferable nor extendible to cover any other users or long- term storage of the product. It does not cover products which have been modified, altered or repaired by any other party than Kontron or their authorized agents. Furthermore, any product which has been, or is suspected of being damaged as a result of negligence, improper use, incorrect handling, servicing or maintenance, or which has been damaged as a result of excessive current/voltage or temperature, or which has had its serial number(s), any other markings or parts thereof altered, defaced or removed will also be excluded from this warranty.

If the customer's eligibility for warranty has not been voided, in the event of any claim, he may return the product at the earliest possible convenience to the original place of purchase, together with a copy of the original document of purchase, a full description of the application the product is used on and a description of the defect. Pack the product in such a way as to ensure safe transportation (see our safety instructions).

Kontron provides for repair or replacement of any part, assembly or sub-assembly at their own discretion, or to refund the original cost of purchase, if appropriate. In the event of repair, re-funding or replacement of any part, the ownership of the removed or replaced parts reverts to Kontron, and the remaining part of the original guarantee, or any new guarantee to cover the repaired or replaced items, will be transferred to cover the new or repaired items. Any extensions to the original guarantee are considered gestures of goodwill, and will be defined in the "Repair Report" issued by Kontron with the repaired or replaced item.

Kontron will not accept liability for any further claims resulting directly or indirectly from any warranty claim, other than the above specified repair, replacement or refunding. In particular, all claims for damage to any system or process in which the product was employed, or any loss incurred as a result of the product not functioning at any given time, are excluded. The extent of Kontron liability to the customer shall not exceed the original purchase price of the item for which the claim exists.

Kontron issues no warranty or representation, either explicit or implicit, with respect to its products' reliability, fitness, quality, marketability or ability to fulfil any particular application or purpose. As a result, the products are sold "as is," and the responsibility to ensure their suitability for any given task remains that of the purchaser. In no event will Kontron be liable for direct, indirect or consequential damages resulting from the use of our hardware or software products, or documentation, even if Kontron were advised of the possibility of such claims prior to the purchase of the product or during any period since the date of its purchase.

Please remember that no Kontron employee, dealer or agent is authorized to make any modification or addition to the above specified terms, either verbally or in any other form, written or electronically transmitted, without the company's consent.

1. Product Description

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1.1 Product Overview

The Kontron AT8001 ATCA PICMG 3.0/3.1 processor board is simply the most unique AdvancedTCA platform on the market. When first launched, it was the only AdvancedTCA blade to feature a low voltage, high performance Intel® Xeon® processor which scales up to 2.8 GHz, plus support two AdvancedMC modules. This became the start of Kontron's 'AMC Everywhere' approach to offering Telecom Equipment Manufacturers (TEMs) significantly increased design flexibility for any number of applications for wireless, wireline and data center network infrastructures.

The AT8001 feature-set includes dual Gigabit Ethernet and dual Fiber Channel on fabric interface, and dual Gigabit Ethernet base interface, and is loaded with up to 8 GB of DDR-II 400 SDRAM. Designed with the Intel® E7520 chipset, the AT8001 includes revolutionary PCI Express serial I/O technology and DDR2, the next generation memory technology, to help increase I/O bandwidth and reduce system latency for data-intensive applications. Its 800 MHz system bus also allows increased platform bus bandwidth (50% more than 533MHz) and delivers increased system performance.

'AMC Everywhere' strategy
Kontron ensures all of its next generation AdvancedTCA platforms are 'AMC Everywhere' enabled, offering support for AdvancedMC modules in its processor, hub and carrier products. This is a major factor in providing TEMs with unprecedented flexibility in the design of new, IMS-based applications, as well as increase economies of scale by freeing up valuable AdvancedTCA system slots for other payload blades.

AdvancedMC modules are the smallest Field Replaceable Units (FRU) on the market that are hot swappable and support the RASM concept of "Reliability, Availability, Serviceability, and Maintainability". Ultimately for Service Providers and Carriers, this translates into a significantly lower OPEX with easy upgrades in the field, reduced risk for the introduction of new subscriber services, and the ability to expand networks.

AdvancedMCs are also proving to be an attractive solution for proprietary form factor base boards. For example legacy telecom systems can be outfitted with COTS AdvancedMCs to enable a smooth migration from purely proprietary technology to a 100 per cent AdvancedTCA system in the future.

Faster-Go-To-Market strategy
Kontron shortens the application design process by ensuring that each open modular building block is fully interoperable and designed to be both the right technology and the right architecture in mind to suit any development needs. Pre-integrated and application ready right out-of-the-box, Kontron open modular solutions are customizable and also feature best-in-class carrier-grade software such as MontaVista® Linux® Carrier Grade Edition (CGE), and hot-standby Solid CarrierGrade® data manager from Solid Information Technology. This complements Kontron's existing offering of Intelligent Platform Management Interface (IPMI v1.5) firmware, Hardware Platform Interface (HPI) support, and operating system and applications software.

1.2 What's Included

This board is shipped with the following items:

1. One Quick Reference Sheet.
2. One CD-ROM containing drivers.
3. One AT8001 board
4. Cables that have been ordered

If any item is missing or damaged, contact the supplier.

1.3 Board Specifications

FEATURES	DESCRIPTION
Supported Microprocessors	• Single Intel® LV Xeon™ Processor at 800 MHz front side bus (FSB) at 2.80GHz • Passive heatsink
Cache Memory	• 1M L2 on-die cache
Chipset	• Intel E7520 MCH • Intel 6300ESB ICH • Intel 6700 PXH
Bus Interface	• Front side bus at 800MHz, 64-bit data, 36-bit address • Memory bus at 400 MHz, 144-bit data (2 channel) • Three onboard PCI-Express by eight (x8) • Two onboard 64-bit/133MHz PCI-X bus • One onboard 64-bit/66MHz PCI-X bus (for optional PMC) • One onboard 32-bit/33MHz bus for video interface and LAN management port
AMC/PMC Slot	• Slot B1 : PCI-Express x8 (AMC option) • Slot B2 : PCI-Express x8 (AMC option) • PMC I/O module support (PMC option) : PCI-X 64-bit/66MHz
System Memory	• Up to 8GB on 2 x 240-pin latching DDR-II 400 SDRAM (PC2-3200) • ECC support, support S4EC/D4ED when using x4 SDRAM • Two DDR channels 72-bit/200MHz for Interleave operation
Flash Memory	• Two Redundant 1MB BIOS (field software upgradeable) • Roll back functionality controlled by IPMC

Board Specifications (continued)

I/O

Description	Front Plate	Rear I/O	AMC	Total
Video	1	1	-	1
USB	1	1	-	2
Serial	1	1	-	1
PS/2 Mouse	-	1	-	1
PS/2 Keyboard	-	1	-	1
Ethernet Management	1	1		1
Ethernet Base	-	2 (backplane)	-	2
Ethernet Fabric	2*	2* (backplane)	2*	2
Reset Button	1	1	-	2
Fibre Channel (Optional)	2*	2*	2*	2

Description	Onboard	Rear I/O	Mezzanine	Total
Hard Disk (SATA)	-	2**	2**	2
Hard Disk (PATA)	1(PMC option)	-	-	1
Compact Flash	1	-	-	1

* Various combinations through cross point switches
** SATA routing depend on board configuration

F / R	Front or Rear
Video	PCI video controller (ATI Mobility-M) with 4MB video memory. Support CRT with resolution up to 1280 x 1024
USB	USB 2.0 compliant
Serial	COM1 (RS-232) COM 2 is routed to the IPMC
Ethernet	One 10/100 Base-TX (Intel 82551ER) configurable in Front or Rear through BIOS option. Two 10/100/1000 Base-T (Intel 82546GB) for the base interface. Two 10/100/1000 Base-T (Front RJ45) or 1000BAse-SX (Front SFP) or 1000Base-BX (Fabric I/F)(Intel 82546GB) Possible configuration depends on board option.
Fibre Channel**(Optional)**	Fiber channel based on LSIFC929X controller configurable in Front (SFP) or Rear Access (Frabric Interface)
Hard Disk	SATA interface available through each AMC mezzanine cards or through Rear I/O depending on board option. PATA interface available onboard depending on board option. SCSI Hard drive can be provided through a PMC module; no rear access possibility Fibre Channel hard drive can be access through front access SFP modules or using proper fabric interface switches.
CompactFlash	Can be installed on EIDE channel 0 through the onboard connector

Clock/Calendar	• Real-time clock with 256-byte battery backed-up by a supercap
Connectors on Front Panel	**Front Plate** COM1 — 1 x RJ-45 (Serial Port) Ethernet (100Mb) — 1 x RJ-45 (Ethernet) USB — 1 x 4-pin USB female VGA — 1 x Micro-D 15 Optic — 2 x Optical SFP Ethernet (1000Mb) — 2 x RJ-45
Interfaces on Rear I/O	**Rear I/O Connectors** **(Rear-panel transition module, AT5701 available separately)** CRT — Serial Ports (1) — USB (1) Speaker I/F — Reset Switch — Ethernet Managment (1) PS/2 Mouse &Keyboard — SATA (2)
Onboard Expansions	2 AMC or 1 PCI Mezzanine Card PMC & 1 Hard Disk Drive 1 CompactFlash.

Board Specifications (continued)

BIOS Features	• AMI BIOS • Save CMOS in Flash option • Boot from gigabit Ethernet (Base and Fabric) • Boot from USB 2.0 (floppy, CD-Rom, hard disk) • Auto configuration, extended setup and VGA disable by jumper • Diskless, keyboard less, and video less operation extensions • System, video and LAN BIOS shadowing • HDD S.M.A.R.T. support • Advanced Configuration and Power Interface (ACPI 1.0b and 2.0) • Advanced thermal management such as resume, overheat and auto slow down with CPU build-in Thermal Control Circuit • Setup console redirection to serial port (VT100 mode) with CMOS setup access • Redundant Field-updateable BIOS • Event (SERR, PERR, Memory SBE, POST errors) log support to IPMC
IPMI Features	• Management Controller compliant to PICMG 3.0, AMC.0 R1.0 and IPMI v1.5 rev 1.1. • Management Controller is run time field reprogrammable without payload impact. • Robust fail safe reprogramming implementation (which includes two firmware images) that could perform automatic or manual rollback if a problem occurs during critical reprogramming phase. • Remote upgrade capability from all IPMI interfaces (CPU Host Interface/IPMB-0/LAN). • Management Controller self test which can detect failure under its code integrity and trig an automatic rollback. • Can initiate a Host CPU reboot on a redundant BIOS image base on a BIOS-IPMC handshake result. • Fast interrupt driven SMS host interface compliant to IPMI-KCS v1.5 rev 1.1 • Serial Over LAN (SOL) redirection of the Host CPU serial controller traffic to enable asynchronous serial-based OS and pre-OS communication via standard RMCP LAN application through the Management Controller. • Standard Management Controller message bridging to AMC via IPMB-L • Management Controller support standard PCI Hot Plug for PCI-Express AMC. • Management Controller can initiate standard graceful OS shutdown via ACPI support. • Hardware config that allow activation of the blade or AMC without Shelf Manager intervention.
Supervisory	• Support a system management interface via an IPMI V1.5 compliant controller • Watchdog for BIOS execution and OS loading (through IPMI watchdog) • Hardware system monitor through IPMI (voltages,current, powertemperature), CPU temperature monitor / alarm; board temperature sensor, power failure,
OS Compatibility	• MontaVista Linux Carrier Grade Edition Version3.1
Mechanical	• Board is an 8U form factor mechanically compliant to PICMG3.0: 322.25mm x 280.00mm (12.687” x 11.024”). • Board pitch is 6HP.
Power Requirements	Typical 120W Maximum 200W with 2 AMC* * 55°C operation might not be possible with all AMC combinations.

Board Specifications (continued)

Environmental		Operating	Storage and Transit
	Temperature*	0-55°C/32-131°F	-40 to +70°C/-40 to 158°F
	Air Flow*	Consult table below	
	Humidity*	15% to 90% @55°C/131°F non-condensing	5% to 95% @ 40°C/104°F non-condensing
	Altitude*	4,000 m / 13,123 ft	15,000 m / 49,212 ft
	Shock*	30G, half-sine 11ms, each axis	Bellcore GR-63-CORE Section 4.3
	Vibration*	1.0G, 5-500Hz each axis	2.0G, 5-50Hz; 3.0G, 50-500Hz each axis
Reliability	• MTBF: > TBD hours @ 30°C / 77°F (Telcordia SR-332, Issue 1) • Whole board protected by active breaker • USB voltage protected by an active breakers		
Safety/EMC	Meet or exceed: • Safety: UL 60950 3rd Ed.; CSA C22.2 No 60950-00; EN 60950:2000; IEC60950-1 • EMI/EMC: FCC 47 CFR Part 15, Class B; CE Mark to EN55022/EN55024		
Warranty	Two year limited warranty		

* Designed to meet or exceed

1.4 Compliance

This product conforms to the following specifications:

- PICMG3.0R1.0 (Advanced TCA core specification)
- PICMG3.1R1.0 (Ethernet/Fiber Channel over Advanced TCA)
- AMC.0 R1.0 (Advanced mezzaninne card base specification)
- AMC.1 R1.0 (Advance mezzaninne card PCI-Express)
- IEEE STD 1386.1-2001 (PMC)
- IEEE STD 1386-2001 (CMC)
- ACPI rev 1.0

1.5 Hot-Plug Capability

The AT8001 supports **Full Hot Plug** capability as per PICMG3.0R1.0. It can be removed from or installed in the system while it is on (without powering-down the system). Please refer to the PICMG3.0R1.0 specification for additional details.

1.6 Interfacing with the Environment

1.6.1 RTM (rear transition module)

Some I/O can be accessed through the use of a RTM. RTM use a proprietary pinout in J30 (Zone 3 connector) to bring out some I/O of the SBC. Only use Kontron's RTM with the AT8001. Currently compatible RTM is the RT8000.

WARNING



RTM are not designed to be hot swapped. Always make sure that either the system is shut off or that the front board of the RTM is unpowered before removing or installing the RTM.



1.6.2 Mezzanine

The AT8001 supports two types of mezzanine depending on the ordered option. One option is two AMC slots, the second option is one PMC slot. Using a mezzanine allows to add storage or I/O not provided on board.

See Kontron's mezzanine offering for additional I/O capabilities.

1.6.2.1 PMC Expansion

The PMC mezzanine increases the I/O capability of the AT8001 by providing one slot with a PCI-X bus up to 66MHZ/64-bits. It supports up to 266MB/s I/O bandwidth. However, this bandwidth is shared with devices internal to the 6300ESB (SATA, USB) and devices hooked on the PCI 32 bit/33MHz bus (video & Fast Ethernet). For very high performance I/O, it is recommended to use AMC instead.

1.6.2.2 AMC Expansion

Both AMC sites provide the same feature set. Each slot provides a AMC.1 type 8SE2. This mean that the following signalling are supported:

- PCI-Express X8 on AMC port 4-11
- PCI-Express clock on CLK3
- Gigabit Ethernet on AMC port 0 and 1
- SATA on port 2
- Telco clock on CLK1 and CLK2

Possible I/O bandwidth on the PCI-Express is 8GB/s full duplex. Uses of PCI-X reference clock is not mandatory for AMC module. However, it is needed for spread spectrum clocking.

Gigabit Ethernet on port 0 and 1 are connected to T5002 cross point switches. This allow to route these signals to the front SFP modules, onboard LAN, to the backplane or between the two AMC. Moreover, it is possible to use different signaling than gigabit ethernet 1000Base-BX since cross point switches are not aware of data encoding. Any differential signals compliant with AMC.0 and ATCA 3.0 specification up to 6.5Gb/s can be used, provided a compatible endpoint exist.

The SATA interface on port 2 allow to use SATA AMC storage mezzanine. Note however that the 6300ESB doesn't support hot swap on SATA. It is correct electrically to hot swap a SATA AMC but it may cause driver problem in different operating system.

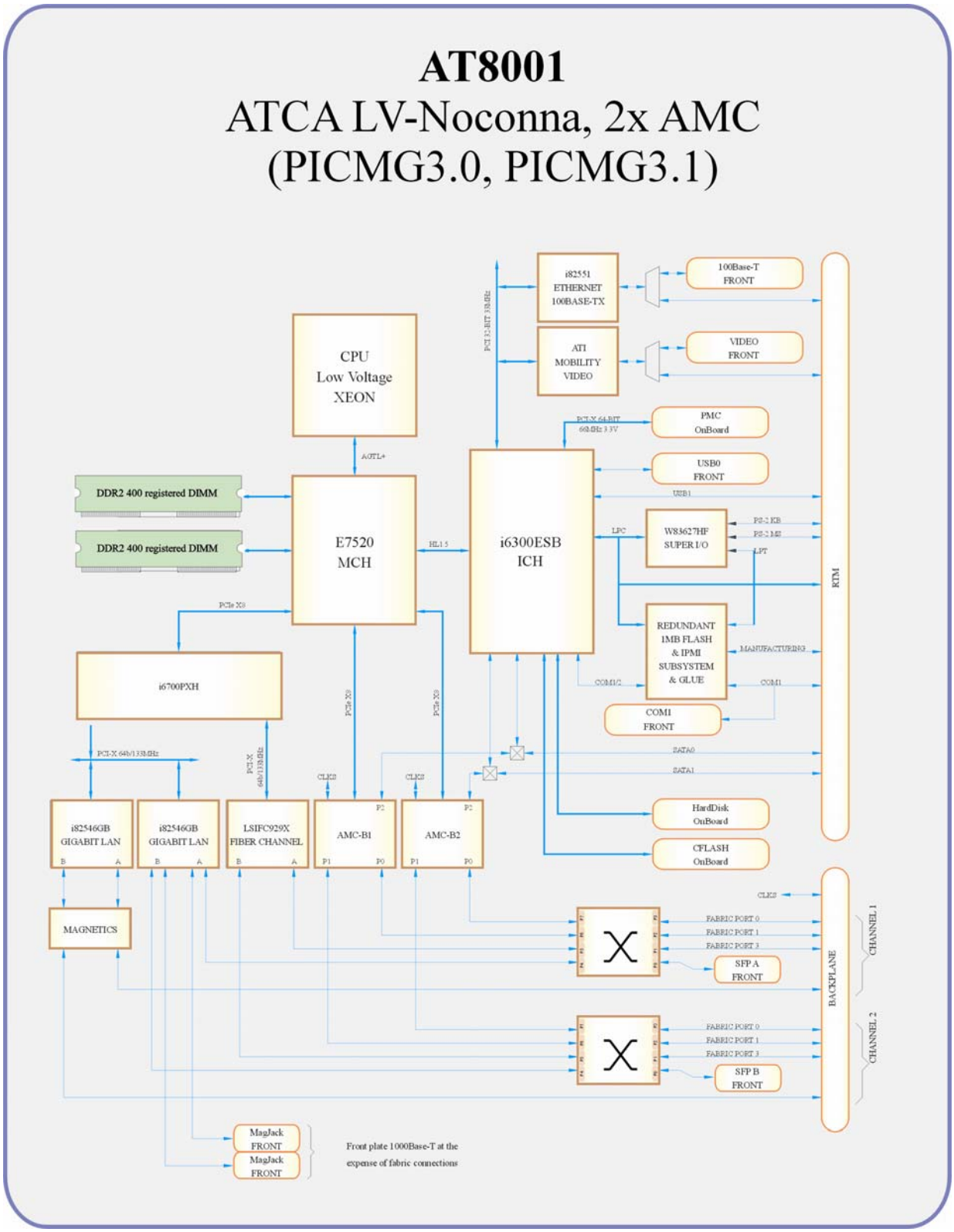
The telco clock signal allows the AT8001 to provide clock to the AMC on CLK1 and CLK2. It also allow an AMC to retrieve a clock an to provide it to the system through CLK2. For possible clock frequency and connection with the backplane, refer to section TBD.

2. Onboard Features

Contents

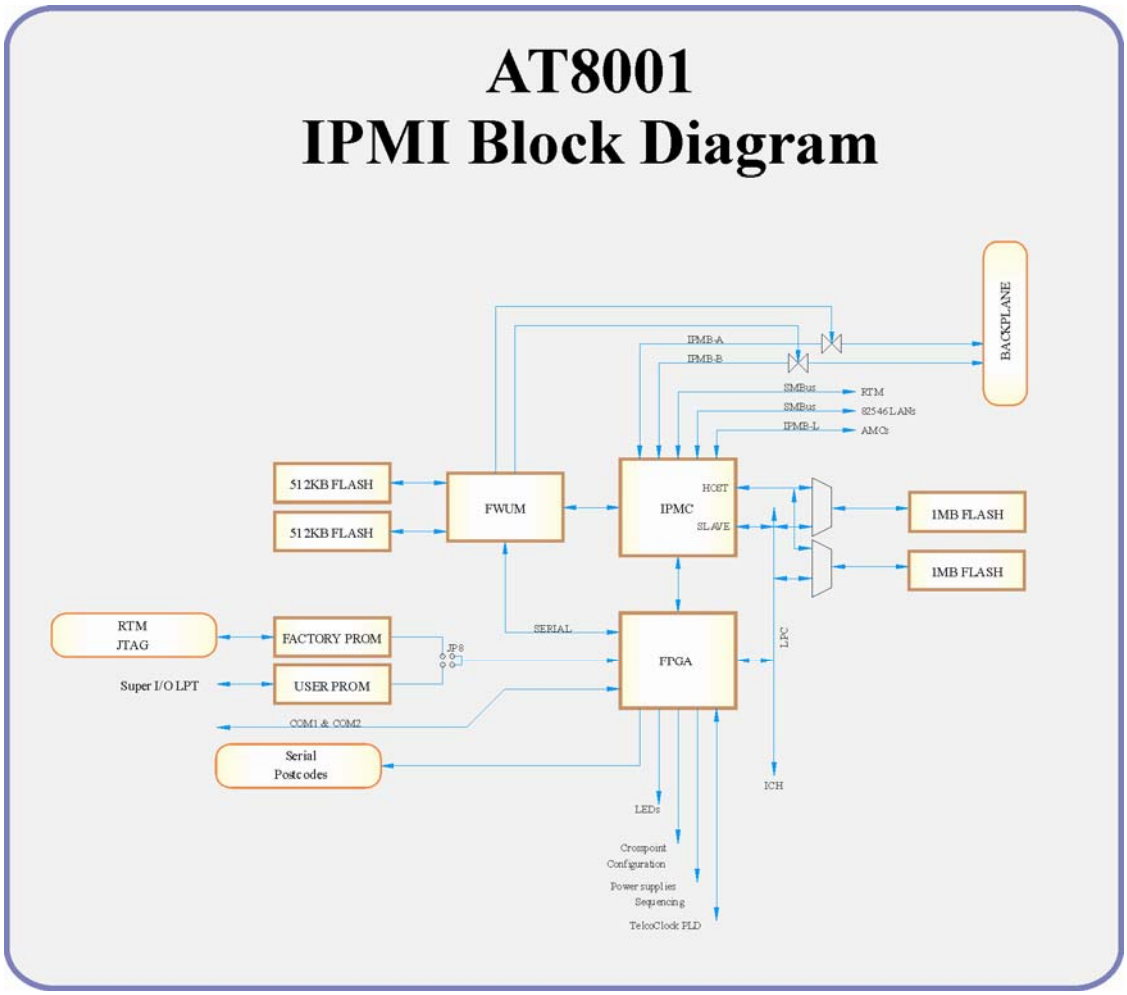
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2.1 Block Diagram



Some notes regarding the block diagram.

- Front/Rear connection for the video is selected with a jumper
- Front/Rear connection for 100Base-T LAN is selected in the BIOS setup
- Manufacturing option: PATA hard-disk and PMC Mezzanine or AMC-B1 and AMC-B2
- Manufacturing option: 1000Base-T or SFPs on front plate
- Manufacturing option: Serial ATA to AMCs or to RTM



2.2 System Core

2.2.1 Processors

The Intel® Xeon™ processor with 800 MHz system bus is designed for high-performance. Based on the Intel® NetBurst™ microarchitecture and the Hyper-Threading Technology, it is binary compatible with previous Intel Architecture (IA-32) processors.

The Intel Xeon processor with 800 MHz system bus delivers compute power at unparalleled value and flexibility for powerful workstations, internet infrastructure, and departmental server applications. The Intel NetBurst micro-architecture and Hyper-Threading Technology deliver outstanding performance and headroom for peak internet server workloads, resulting in faster response times, support for more users, and improved scalability.

The following list provides some of the key features on this processor:

- Intel LV Xeon 2.80GHz
- 90 nm process technology
- Binary compatible with applications running on previous members of Intel's IA-32 microprocessor line
- Intel® NetBurst™ micro-architecture
- Hyper-Threading Technology
- Hardware support for multithreaded applications
- Faster 800 MHz system bus
- Rapid Execution Engine: Arithmetic Logic Units (ALUs) run at twice the processor core frequency
- Hyper Pipelined Technology
- Advanced Dynamic Execution
- Very deep out-of-order execution
- Enhanced branch prediction
- Includes 16-KB Level 1 data cache
- Intel® Extended Memory 64 Technology
- 1-MB Advanced Transfer Cache (On-die, full speed Level 2 (L2) Cache) with 8-way associativity and Error Correcting Code (ECC)
- Enables system support of up to 64 GB of physical memory
- 144 Streaming SIMD Extensions 2 (SSE2) instructions
- 13 Streaming SIMD Extensions 3 (SSE3) instructions
- Enhanced floating-point and multimedia unit for enhanced video, audio, encryption, and 3D performance
- System Management mode
- Thermal Monitor
- Machine Check Architecture (MCA)
- Demand-Based Switching (DBS) with Enhanced Intel SpeedStep® Technology
- EMT64 ...

Please call Kontron to get the available CPU speed and configuration. See Intel's Web site for additional details about Intel® Xeon™ architecture and instruction set.

2.2.2 E7520 MCH

Supports Intel® Xeon™ Processors with 800 MHz system bus

- 800 MHz system bus(2X address, 4X data)
- Symmetric Multiprocessing Protocol (SMP) for up to two processors at 800 MHz
- Parity protection on address, data, request, and response signals
- Supports Hyper-Threading Technology
- Dynamic Bus Inversion (DBI)
- 36-bit host interface addressing support
- 12-deep in-order queue
- AGTL+ technology with on-die termination

Memory System

- Support for 256 Mb, 512 Mb, 1 Gb, 2 Gb and 4 Gb DRAM densities
- Two registered memory DDR channels operating in lock-step at DDR2-400
- Data bandwidth per channel of 3.2 GB/s
- Maximum memory size 8 GB DDR2-400

Integrated four-channel DMA engine with IOxAPIC functionality

High Speed Serial PCI Express* Interface

- Three x8 PCI Express interfaces.
- 32-bit CRC and hardware link-level retry
- Compatible with *PCI Express* Interface Specification*, Rev 1.0a
- High bandwidth connection of 4 GB/s per x8 port to I/O processor, PCI-X, Ethernet, or Infiniband* Technology bridge devices
- Supports 36-bit addressing using 64-bit semantics
- Support for peer segment destination write traffic between PCI Express ports
- Support for non-snooped traffic to memory
- Support for remote boot
- Support for link active-state and ACPI power management

Hub Interface to Intel® I/O Controller Hub

- 266 MB/s interface to Intel® 6300ESB ICH via HI 1.5
- Parity protected
- Support for differentiated, high priority requests
- 32-bit downstream addressing
- 64-bit upstream addressing (full DAC support) truncated to 36 bits internally
- Power management messaging

RASUM

- Support for automatic read retry on uncorrectable errors
- Support for memory mirroring
- Hardware periodic memory scrubbing, including demand scrub support
- Support for Intel® x4 Single Device Data Correction (x4 SDDC)
- Support for standard SEC-DED (72, 64) ECC on each channel when x4 SDDC technology is disabled



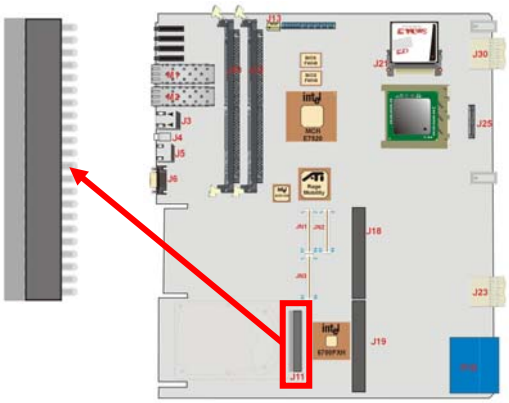
Note:
Many errors can be monitored by setting the DMI event BIOS menu such as ECC errors, parity errors on all PCI/PCI-X buses, and more. See the BIOS section for details.

2.3 6300ESB ICH

2.3.1 Enhanced IDE Interfaces

EIDE interface is part of 6300ESB south bridge. The interface conforms to the ATA specification and support ATA100 for 100MB/s burst transfer.
The board features two interfaces and it supports only one 2,5" hard disk in Master configuration.

Signal	Pin	Pin	Signal
OPT_A	45	46	OPT_B
OPT_C	47	48	OPT_D
N.C.	49	50	N.C.
RESET#	1	2	GND
DD7	3	4	DD8
DD6	5	6	DD9
DD5	7	8	DD10
DD4	9	10	DD11
DD3	11	12	DD12
DD2	13	14	DD13
DD1	15	16	DD14
DD0	17	18	DD15
GND	19	20	KEY
DMARQ	21	22	GND
DIOW#	23	24	GND
DIOR#	25	26	GND
IORDY	27	28	CSEL#
DMASK#	29	30	GND
INTRQ	31	32	RSV
DA1	33	34	PDIAG#
DA0	35	36	DA2
CS0#	37	38	CS1#
DASP#	39	40	GND
VCC	41	42	VCC
GND	43	44	RSV





Signal Paths:
This connector is present only if you have ordered the board with the PMC & HDD option.
The secondary IDE Interface is available through the 2.5inches hard disk connector.



Related Jumpers:
JP12 is used to set the hard disk in master or slave mode. Please consult the hard disk documentation for the proper configuration



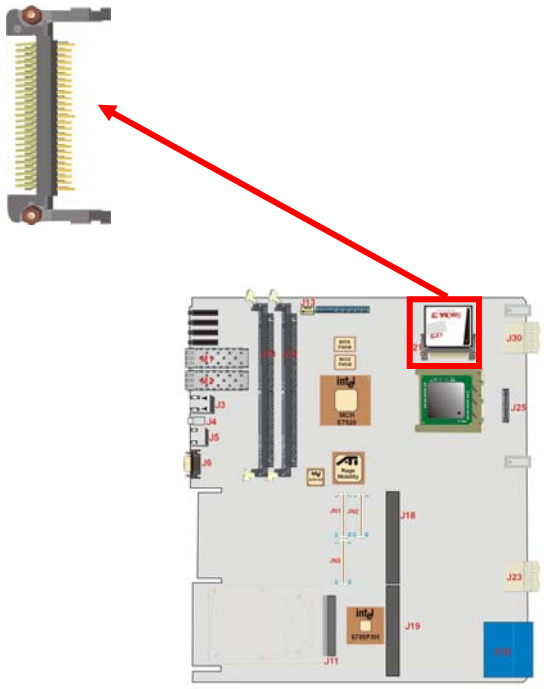
Bios Settings:
- Main
- Specify disk type
- Advanced → IDE Configuration
- Enabled or disabled the IDE controller, change legacy mode and detection options.

The IDE interfaces supports PIO mode 4 transfers up to 16.6MB/sec and Bus Master IDE transfer up to 100MB/sec (Ultra-DMA/100).

2.3.2 CompactFlash Interfaces (J21)

The board features a CompactFlash connector. Any Type 1 CompactFlash can be used. It is connected to the Primary IDE logical interfaces and is set in master mode.

Signal	Pin	Pin	Signal
GND	1	2	DD3
DD4	3	4	DD5
DD6	5	6	DD7
CS0#	7	8	GND
GND	9	10	GND
GND	11	12	GND
VCC3	13	14	GND
GND	15	16	GND
GND	17	18	DA2
DA1	19	20	DA0
DD0	21	22	DD1
DD2	23	24	N.C.
N.C.	25	26	N.C.
DD11	27	28	DD12
DD13	29	30	DD14
DD15	31	32	CS1#
N.C.	33	34	DIOR#
DIOW#	35	36	WE#(3.3V)
INTRq	37	38	VCC3
CSEL#(GND)	39	40	N.C.
RESET#	41	42	IORDY
DMARQ	43	44	DMACK#
DASP#	45	46	PDIAG#
DD8	47	48	DD9
DD10	49	50	GND



Signal Paths:
CompactFlash interface available through J21.

Bios Settings:
- Main
- Specify disk type
- Advanced → IDE Configuration
- Enabled or disabled the IDE controller, change legacy mode and detection options.

2.3.3 SATA Interfaces (J18 & J19)

The board features a two-channel Bus Master PCI SATA. Each channel supports one device and is available through each AMC mezzanine cards or through the RTM.

Signal Paths:
SATA interface available through both AMC or through the RTM depending on you board configuration.

Bios Settings:
- Main
- Specify disk type
- Advanced → IDE Configuration

2.3.4 USB 2.0 Interfaces

USB strengths include:

Capability to daisy chain as many as 127 devices per interface
Fast bi-directional
Isochronous/asynchronous interface
480 MBPS transfer rate
Standardization of peripheral interfaces into a single format
Retro compatible with USB 1.1 devices

USB supports Plug and Play and hot-swapping operations (OS level). These features allow USB devices to be automatically attached, configured and detached, without reboot or running setup.



Pin	Signal
1	VCC
2	DATA-
3	DATA+
4	GND

Signal Paths:
USB0 signals are available on the faceplate from the J4 connector.
USB1 signals are available through the RTM.

Bios Settings:
Advanced → USB Configuration

The AT8001 board supports the standard universal host controller interface (UHCI) for USB1.1. It supports the enhanced host controller interface (EHCI) for USB2.0.

2.3.5 Serial Ports

Two fully functional serial ports are provided on the board for asynchronous serial communications. They are 16C550 high-speed UART compatible and support 16-byte FIFO buffers for transfer rates from 50bps to 115Kbps.
Each serial port is specified as follows:

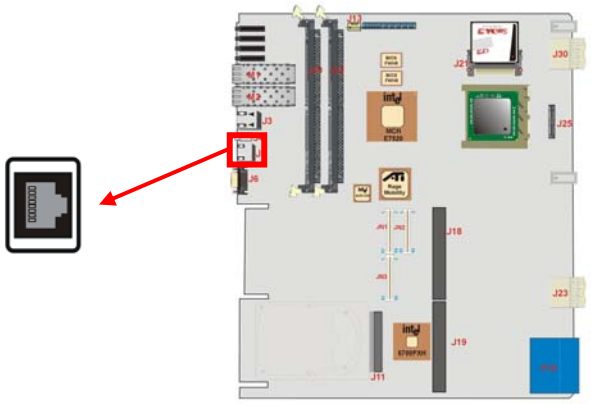
Designation	Communication Mode	Output Path
Serial Port A (COM1)	RS-232	Front Plate RJ-45 (J5) and RTM
Serial Port B (COM2)	RS-232	Onboard to IPMI only for VT100 over IPMI and over LAN

UART registers are individually addressable and fully programmable.

2.3.5.1 Serial Port 1 (J5)

Serial Port 1 is buffered directly for RS-232 operation. Signals include the complete signal set for handshaking, modem control, interrupt generation, and data transfer. When assigned as Serial Port 1, the port is 100% compatible with the IBM-AT serial port in RS-232 mode.

Pin	Signal
1	RTS
2	DTR
3	TXD
4	GND
5	GND
6	RXD
7	DSR
8	CTS



Note:
Standard product uses a RJ-45 8 pins connector. RI (ring indicator) and DCD (data carrier detect) signals are not available.
Optionally a RJ-45 10 pins connector may be populated which allow to use RI and DCD. Contact Kontron's technical support if you are interested with this option.
The pinout is a custum one, not the same as RS-232D EIA-561. Use the Kontron provided RJ45 to DB9 adapter.

Signal Paths:
The Serial Port 1 signal is always available in front and rear access.

Bios Settings:
Advanced → SuperIO Configuration→ ICH SIO Serial Port1 Address.

2.3.5.2 Serial Port 2

Serial Port 2 is internally connected to the IPMC. Serial port 2 is dedicated to Serial Over LAN (SOL) type of console redirection. (This feature will be implemented shortly)

2.3.6 Real Time Clock & NVRAM

The AT8001 is a battery less board. The real time clock and non-volatile RAM integrated in the 6300ESB ICH are powered by the main supply when available or by a double layer SuperCap when the main power is absent. The SuperCap will keep the real time clock running for a couple of hours.

Although it is possible to save the CMOS setup in NVRAM (or CMOS RAM), the default configuration saves the setup in flash. So, when the AT8001 in unpowered for too long, only the time will be lost.

2.4 W83627HF Super I/O

2.4.1 PS/2 Keyboard / PS/2 Mouse Interfaces

This board supports PS/2 keyboard and mouse through a RTM only.



Signal Paths:
The PS/2 Keyboard and PS/2 Mouse Interfaces are available through the RTM only.

2.4.2 Parallel Port

The parallel port is used to implement a Xilinx JTAG port to upgrade the FPGA user-prom in-circuit (see block diagram, IPMI subsystem). This interface also allows to update the CPLD (Telco clock interface).



Bios Settings:
Advanced → SuperIO Configuration→ PLD POD Device.
Advanced → SuperIO Configuration→ Parallel Port Address.

2.5 i6700PXH Bridge

The i6700PXH is a PCI-Express X8 bridge to two PCI-X 64bit/133MHz busses. Both PCI-X busses are used onboard only and always run at full speed: 64bit @ 133MHz. Bus A has one device, the LSIFC929X fibre channel controller; bus B has two devices, the i82546GB gigabit ethernet controller.

It is initialized by the BIOS and there is no parameter to set for this chip.

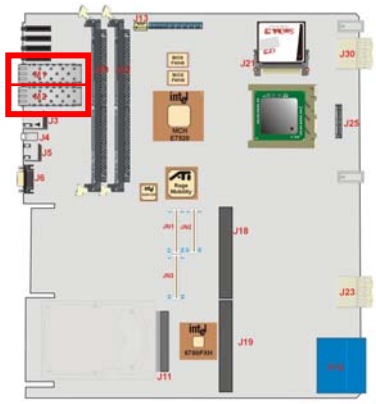
2.6 LSIFC929X Fibre Channel (optional)

The two fibre channel interfaces are based on the dual port LSIFC929X controller. Those can be use for storage and networking. Interfaces support for 2Gb/s and 1Gb/s signalling.

See Kontron's Web site: http://www.kontron.com for the latest drivers.
See LSI's Web site: http://www.lsi.com for the latest drivers for the LSIFC929X and for additional information on the Fibre Channel controller.

The fibre channel high speed differential signals are routed to the onboard cross point switches. This allows to route the fibre channel interface either to the front panel SFP connector, to the backplane fabric interface or to the AMC as needed.

Signal	Pin	Pin	Signal
VEET_1	1	11	VEER_3
TX_FAULT	2	12	RD-
TX_DIS	3	13	RD+
MODDEF2	4	14	VEER_4
MODDEF1	5	15	VCCR
MODDEF0	6	16	VCCT
R_SEL	7	17	VEET_2
LOS	8	18	TD+
VEER1	9	19	TD-
VEER2	10	20	VEET_3
cGND_1	21	22	cGND_2
cGND_3	23	24	cGND_4
cGND_5	25	26	cGND_6
cGND_7	27	28	cGND_8
cGND_9	29	30	cGND_10
cGND_11	31		



Signal Paths:
The fibre channel signals are routed to the cross point switches. See cross point switches section for details.

BIOS Settings:

Advanced → On-Board Devices Configuration → On-board Fibre Channel.

Advanced → ATCA Channel Routing (PICMG).

2.7 Ethernet Interfaces

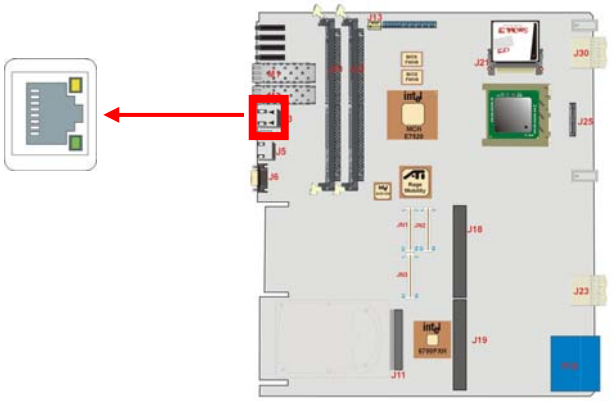
2.7.1 i82551ER 100Base-T Management LAN

The AT8001 has a 100Base-T LAN based on the 82551ER that can be accessed on the front plate or the RTM (if available). Use the BIOS setup to specify where the LAN will be used.

Note that this LAN has no boot from LAN support.

See Kontron's Web site: http://www.kontron.com for the latest drivers.
See Intel's Web site: http://www.intel.com for the latest drivers for the i82551ER and for additional information on the Ethernet controller.

Pin	Signal 10/100
1	TX+
2	TX-
3	RX+
4	N.C.
5	N.C.
6	RX-
7	N.C.
8	N.C.



Signal Paths:
The Ethernet Management RJ45 connector is on the faceplate or RTM.

BIOS Settings:
Advanced → On-Board Devices Configuration → LAN i82551er Routing.

2.7.2 i82546GB Base Interface

The ATCA base interface is implemented with a i82546GB twin-gigabit Ethernet chip. It supports a 10/100/1000 Base-T connection with autonegociation to the base interface channel 1 and 2.

The i82546GB features high performance with TCP/IP and UDP/IP checksum offloading for IPv4 and IPv6, packet filtering, and jumbo frame up to 16K. See www.intel.com for additional details on the i82546.

The AT8001 has boot from LAN capability (PXE) on those ports. Enable the option from the BIOS Set-up Program. Please refer to Section 5.1, AMI BIOS Set-up Program.



Signal Paths:
The Ethernet Management RJ45 connector is on the faceplate.



BIOS Settings:
Advanced → On-Board Devices Configuration → On-board Dual Ethernet 1

2.7.3 i82546GB Fabric/Front Interface

A second i82546GB is used in various configurations. The 2 ethernet ports are routed to the cross point switches allowing many configurations.

- Connection to the fabric interface (Fabric Channel 1 & 2 on port 0).
- Connection to the AMCs (AMC port 0 or 1).
- Connection to SFP modules on the front.

Depending on the board configuration, it is possible to have 2 RJ-45 connectors instead of 2 SFP modules on the frontplane. In this case, this additionnal connection is possible:

- Connection to 10/100/1000Base-T RJ45s on the front plate

The i82546GB features high performance with TCP/IP and UDP/IP checksum offloading for IPv4 and IPv6, packet filtering, and jumbo frame up to 16K. See www.intel.com for additional details on the i82546GB.

The AT8001 has boot from LAN capability (PXE) on those ports. Enable the option from the BIOS Set-up Program. Please refer to Section 5.1, AMI BIOS Set-up Program.

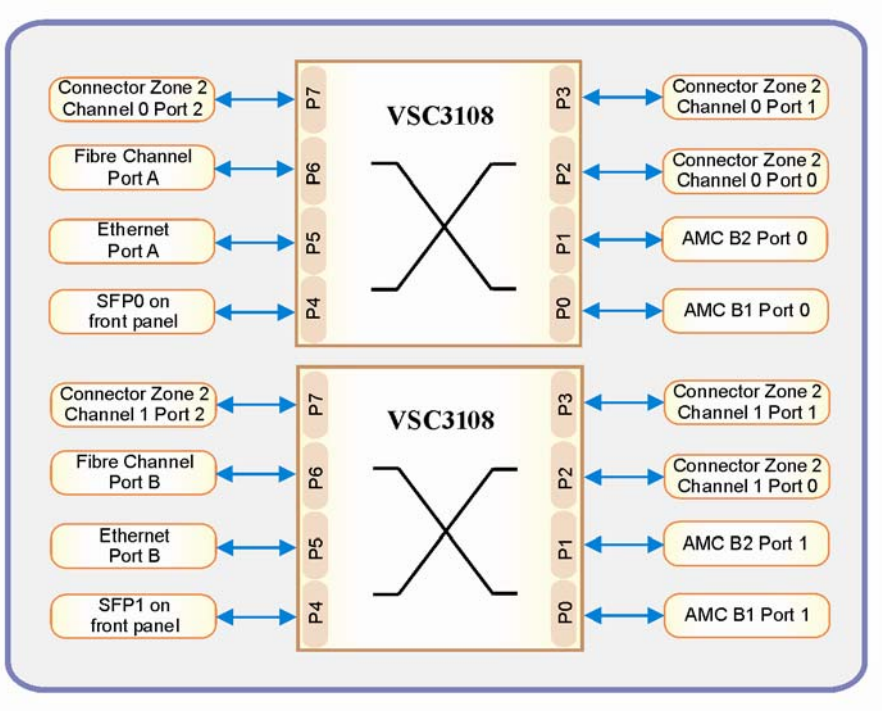


BIOS Settings:
Advanced → On-Board Devices Configuration → On-board Dual Ethernet. 2.

Advanced → ATCA Channel Routing (PICMG).

2.8 Crosspoint Switches

The crosspoint switches are multiport devices that allow connecting any inputs to any ouputs. By connecting LAN, Fibre Channel, SFP, AMC and Fabric Interfaces to such switch, many usefull configuration may be achieved by simple BIOS options.



Two 8x8 crosspoint switches are used (Vitesse VSC3108). Those switches are protocol-agnostic and can carry serdes type signals at up to 6.5Gb/s NRZ data. This mean that any compatible endpoint can be connected. If using two AMC with 6.5Gb/s signalling on AMC port 0, it is possible to connected those together since the VSC3108 are protocol-agnostic.

Common configurations have been included in the BIOS setup.

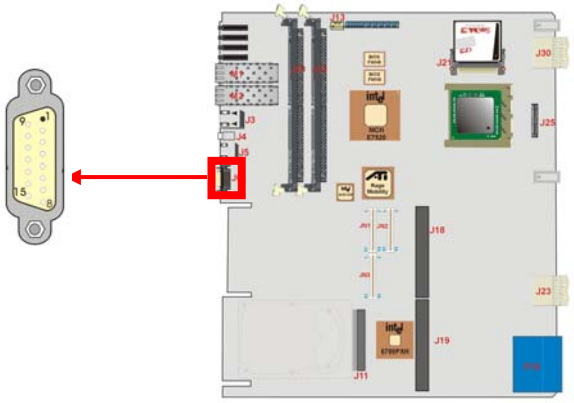
For unsupported configurations, consult Kontron Canada technical support.

Bios Settings:
Advanced → ATCA Channel Routing (PICMG).

2.9 Video Interface

The video controller is an ATI Mobility-M with 4MB; capable of CRT resolutions up to 1600x1200. The video interface features high performance 64-bit frame buffer PCI video.

Signal	Pin	Pin	Signal
RED	1	9	N.C.
GREEN	2	10	GND
BLUE	3	11	N.C.
N.C.	4	12	SDATA
GND	5	13	HSYNC
GND	6	14	VSYNC
GND	7	15	SCLCK
GND	8		





Signal Paths:
Video signals are available through J6 (Front panel connector) or from Rear I/O connector
If you use the front video connector you will need to use the appropriate adapter cable.



Related Jumpers:
JP4 enables or disables the onboard video.
JP5 is used to set the video position in front or rear.
See Section 3.1 – *Jumper Settings*.

2.9.1 Supported Resolutions

The maximum video resolution and performance depend directly on the drivers running with your software application. Resolution and number of colours specification are listed below:

Resolution	Number of Colours
640x480, 800x600, 1024x768, 1280x1024, 1600x1200	256 (8 bits)
640x480, 800x600, 1024x768, 1280x1024, 1600x1200	65,536 (16 bits)
640x480, 800x600, 1024x768, 1280x1024	16.8 million (24 bits)
640x480, 800x600, 1024x768	16.8 million (32 bits)

2.9.2 Major Features Description

- VGA Compatibility
  The video controller includes all registers and data paths required for the VGA controller and supports extensions to VGA, including resolutions up to 1600 x 1200 x 65K colours non-interlaced. The 24-bit images are displayed at up to 1280x1024 resolutions.

- 2D Graphics Engine
  The 2D graphics engine is an advanced 32-bit, three-operand engine that accelerates BitBLTs as line draws, polygon draw, and polygon fill. The 2D graphics engine also performs video and bitmap scaling, and data overlay.

2.10AMC Mezzanines(optional)

Depending on the board configuration, up to two AMC sites can be available. Characteristics of each AMC are as follow:

- Type B+
- Support full height single width mecanincal formet
- PCI-Express X8 with reference clock on AMC CLK3
- Fully compliant PCI hot-swap support
- Serial ATA on port 2
- Port 0 and 1 connected to crosspoint switches (LAN, fiber channel or other)
- Provision for telecom clocks on CLK1 and CLK2

As per AMC.1 R1.0, the carrier board (At8001) is required to provide PCI-E 100MHz reference clock to the AMC on CLK3. However, modules are not required to use it. Kontron recommend using AMC-Express modules that use the reference clock on CLK3. If the module makes its own reference clock, then the spread spectrum of the AT8001 clock synthesizer needs to be disabled in the BIOS setup, otherwise the behavior of the PCI-Express link will be erratic at best.

Note:
All electromagnetic compatibility testing has been done with spread spectrum. Disabling the spread spectrum can complicate EMC.

Bios Settings:

- Advanced → IDE Configuration

Advanced → On-Board Devices Configuration → On-board AMC B1.

Advanced → On-Board Devices Configuration → On-board AMC B1.

Advanced → ATCA Channel Routing (PICMG).
Advanced → PCI-Express Configuration
Chipset → Spread Spectrum Clocking Mode

2.11 PMC Mezzanine (optional)

The AT8001 supports configuration with a PMC mezzanine. Its characteristics are:

- 3.3V signaling only (not 5V tolerant)
- 64-bit bus, PCI 33MHz, PCI 66MHz or PCI-X 66MHz

Bios Settings:
Advanced → On-Board Devices Configuration → On-board PMC.

2.12 Redundant BIOS Flash

Two BIOS flash are present on the AT8001. If a BIOS update corrupts a flash and prevent the Xeon from completing the boot sequence, the IPMC will force a reboot from the other BIOS flash.

Note:
Since the CMOS setup is saved in flash, this will also restore the previous BIOS setup.

2.13 Redundant IPMC Flash & FWUM

The IPMC microcontroller runs a firmware from its internal 512KB flash. It is programmed by an other microcontroller named FWUM (FirmWare Update Manager). The FWUM keeps the last two copies of the IPMC firmware in dedicated flash memories. The FWUM act as a watchdog to the IPMC and can rollback a firmware update in the IPMC in case of problems.

The FWUM itself is a microcontroller with internal flash to store IPMC firmware image. This microcontroller is also an external watchdog for the IPMC. Functions of this microntroller is kept to a minimum. The FWUM firmware is field updatable.



Note:
The IPMC and the FWUM have an internal hardware watchdog.

2.14 FPGA

The FPGA has various functions. One of them is to act as a companion chip to the IPMC. The states of all the critical signals controlled by the IPMC are memorized in the FPGA and are preserved while the IPMC firmware is being updated.

The FPGA is a RAM-based chip that is preloaded from a separate PROM at power-up. Two such PROMs are provided. One that can only be programmed in factory and an other one that can be updated in the field. The PROM is selected through jumper JP8. Field updates require to cycle the power of the board.

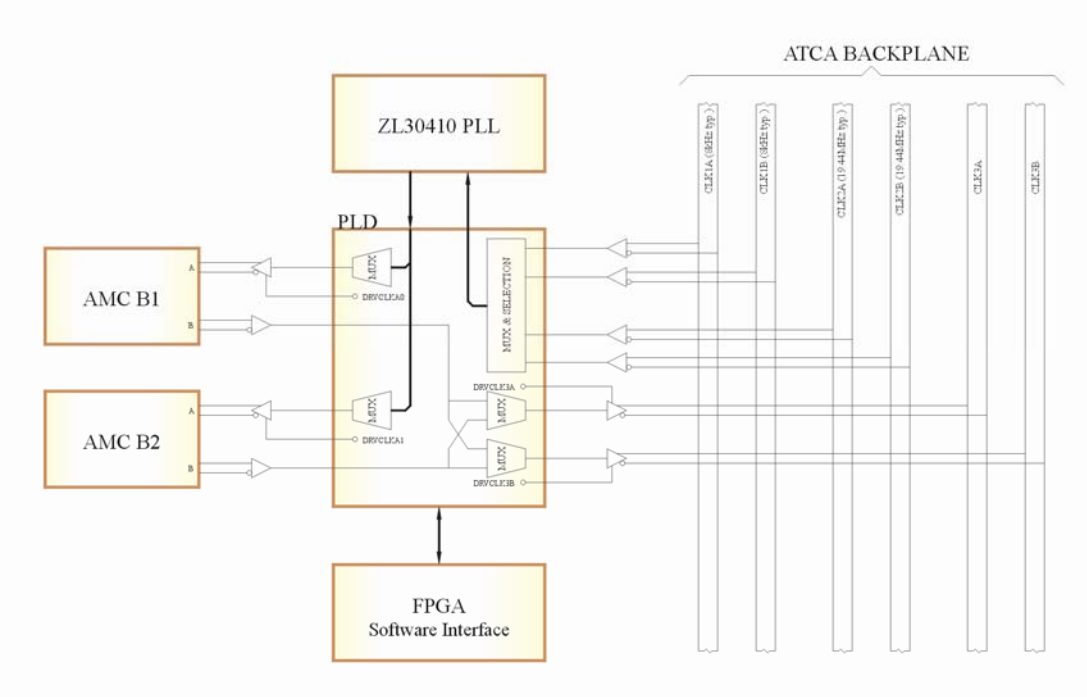
The appropriate procedure to upgrade the FPGA will be provided with the update code when needed.



Note:
FPGA version is displayed in the BIOS summary screen (you need to enter the BIOS setup).

2.15 Telecom Clock Option

The telecom clock option is not shown on the main block diagram. The circuit is made of MLVDS buffers, a PLD and a multi-service line card PLL. The PLD is hooked to the main FPGA with a fast serial link and from there, to the LPC bus.



The PLD receives clocks from the backplane (CLK1 or CLK2) and use it as a reference to Zarlink's ZL30410 PLL. Any one of the PLL clock outputs can be use to feed the AMCs CLK1. If a backplane clock is lost, the circuit will automatically switch to the redundant clock. If all backplane clocks are lost, the PLL will switch to holdover mode until a clock reaper.

Also, the clock circuit can receive a clock from an AMC CLK2 and distribute it to the backplane CLK3A or CLK3B.

In all error cases, alarms are reported through an interrupt.

This circuit is available on AT8001 with AMC support only.The PLD is field upgradable. Customization on this device for additionnal feature is possible. Contact Kontron's technical support for this service. If upgrade are necessary for this device, an appropriate procedure will be provided with the code update.

2.16 Hardware Management Overview

The main processors communicate with the Intelligent Management Controller (IPMC) using the Keyboard Controller Style (KCS) interface. BIOS uses SMM interface. The base address of the LPC interface for SMS is 0xCA2 and 0xCA4 for SMM operation. Besides that, the BIOS is able to communicate with the IPMC for POST error logging purposes and fault resilient purposes.

The memory subsystem of the IPMC consists of an integrated flash memory to hold the IPMC operation code and integrated RAM for data. The field replacement unit (FRU) inventory information is stored in the nonvolatile memory on an EEPROM connected via a local I2C interface to the IPMC microcontroller. It is possible to store up to 4 KBytes within the FRU inventory information. Event generation over IPMB bus to reach the ShMc SEL ensure that 'post-mortem' logging information is available even if the main processor becomes disabled.

The IPMC provides six I2C bus connections. Two are used as the redundant IPMB bus connections to the backplane, one is used for IPMB-L bus with AMC modules, two others I2C are used to LAN connections for IPMI over LAN support and the last one is for local EEPROM storage.

If an IPMB bus fault or IPMC failure occurs, IPMB isolators are used to switch and isolate the backplane/system IPMB bus from the faulted SBC board. Where possible, the IPMC will isolate the failure line and will use the other bus to re-establish system management communication to report the fault.

The onboard DC voltages, currents, and temperature are monitored by the IPMC microcontroller device. The IPMC will log an event into the ShMc SEL if any of the thresholds are exceeded.

To increase the reliability of the AT8001 SBC management subsystem, an external watchdog supervisor only for the IPMC is implemented. The IPMC must strobes the external watchdog at two-second intervals to ensure continuity of operation of the board's management subsystem. If the IPMC ceases to strobe the watchdog supervisor, the watchdog isolates the IPMC from the IPMBs and resets the IPMC. The watchdog supervisor does not reset the payload power and the restart of the IPMC will not affect the payload and will restore the previous Hot Swap state and power level negociated with the ShMc. The watchdog timeout expires after six seconds if strobes are not generated. The external watchdog supervisor is not configurable and must not be confused with the IPMI v1.5 watchdog timer commands.

This external watchdog of the IPMC is implemented in a second microcontroller. This microcontroller is responsible to monitor the IPMC and to manage IPMC fail safe firmware upgrade process. The name of this second microcontroller is the Firmware Upgrade Manager (FWUM). The FWUM can handle two Firmware code that are stored in two external SEPROM memories. If a failure occurs during firmware upgrade, the FWUM will automatically rollback to the redundant IPMC firmware image.

2.16.1 Sensor Data Record (SDR)

Every sensor on the baseboard is associated with a Sensor Data Record (SDR). Sensor Data Records contain information about the sensors identification such as sensor type, sensor name, sensor unit. SDR also contain the configuration of a specific sensor such as threshold/hystheresis, event generation capabilities that specifies sensor behaviour. Some field of the sensor SDR are configurable through IPMI v1.5 command and are set to built-in initial value. Finally one field wich is the sensor owner must reflect the baseboard addresses that allow the ShMc to identify the owner of the SDR when it is scaned from the satellite management controller and saved within the ShMc SDR repository.

The AT8001 management controller is set up as a satellite management controller (SMC). It does support sensor devices, and use the IPMI dynamic sensor population feature of IPMI v1.5 to merge the hot swaped AMC sensor with the AT8001 sensors population. The usual way the ShMc is informed about an AMC insertion is through the AMC carrier Hot Swap sensor, however to remain compliant to IPMI v1.5, the IPMC update the sensor population change indicator timestamp accessible through the Get Device SDR Info command. All SDRs can be queried using Device SDR commands to the firmware. Baseboard sensors that have been implemented are listed below.

2.16.2 Hardware Sensors

Sensor Name	Voltage/Signals Monitored	Scanning Enabled under Power State	Health LED (Green to Red)
Vcc 1.5v FRU0	+1.5 V	Power On	Exceeds critical threshold
Vcc 2.5v FRU0	+2.5 V	Power On	Exceeds critical threshold
Vcc 1.8v FRU0	+1.8 V	Power On	Exceeds critical threshold
Vcc Vtt FRU0	VTT DDR (+1.25 V)	Power On	Exceeds critical threshold
Vcc -48v FRU0	-48 V	Power On/Off	Exceeds critical threshold
Vcc 5v FRU0	+5 V	Power On	Exceeds critical threshold
Vcc 12v FRU0	+12 V	Power On	Exceeds critical threshold
Vcc Vcore FRU0	CPU Core Voltage	Power On	Exceeds critical threshold
Vcc 3.3v FRU0	+3.3 V	Power On	Exceeds critical threshold
Vcc 3.3vSus FRU0	+3.3 VSB	Power On/Off	Exceeds critical threshold
Icc 12v FRU0	Current +12 V Baseboard	Power On/Off	Exceeds critical threshold
Icc 12v FRU1	Current +12 V AMC	Power On/Off	Exceeds critical threshold
Icc 12v FRU2	Current +12 V AMC	Power On/Off	Exceeds critical threshold
Icc 5v FRU0	Current +5 V	Power On/Off	Exceeds critical threshold
Icc 3.3vSus FRU0	Current +3.3 VSB	Power On/Off	Exceeds critical threshold
Icc 1.8v FRU0	Current +1.8 V	Power On/Off	Exceeds critical threshold
Icc 1.5v FRU0	Current +1.5 V	Power On/Off	Exceeds critical threshold
Icc -48v FRU0	Current -48 V	Power On/Off	Exceeds critical threshold
Power FRU0	Power Baseboard	Power On/Off	Exceeds critical threshold
Power FRU1	Power AMC	Power On/Off	Exceeds critical threshold
Power FRU2	Power AMC	Power On/Off	Exceeds critical threshold
Temp BoardA Area	Board Temperature	Power On/Off	Exceeds critical threshold
Temp BoardB Area	Board Temperature	Power On/Off	Exceeds critical threshold
Temp CPU	CPU 0 Temperature	Power On/Off	Exceeds critical threshold
Temp MCH	MCH Temperature	Power On/Off	Exceeds critical threshold
Temp Vcore	Vcore Temperature	Power On/Off	Exceeds critical threshold
Temp PXH	PXH Temperature	Power On/Off	Exceeds critical threshold
Temp FC Area	Fibre Chanel Temperature	Power On/Off	
Temp 12vPS Area	12V supply Temperature	Power On/Off	
Processor	CPU 0 Presence	Power On/Off	No change
	CPU 0 IERR	Power On	No change
	CPU 0 Thermtrip	Power On	ThermTrip signal asserted
	CPU 0 ProcHot	Power On	ProcHot signal asserted
FRU0 Hot Swap	Baseboard HS State	Power On/Off	No change
FRU1 Hot Swap	AMC HS State	Power On/Off	No change
FRU2 Hot Swap	AMC HS State	Power On/Off	No change
IPMB0 Link Sensor	Operational state of IPMB-0	Power On/Off	No change
IPMBL Link Sensor	Operational state of IPMB-L	Power On/Off	No change

CPU Critical Interrupt	PCI SERR	Power On	No change
	PCI PERR	Power On	No change
System Firmware Progress		Power On	No change
Memory Error	ECC Multiple Bit error	Power On	No change
	ECC Single Bit error	Power On	No change
IPMI Watchdog	IPMC Watchdog Timer timeout	Power On/Off	No change
Boot Error	BIOS Main Flash	Power On	No change
	BIOS FRED Flash	Power On	No change
System Event	System Event	Power On	No change
ACPI State	Baseboard ACPI state	Power On/Off	No change
EventRcv ComLost	Communication lost with ShMc	Power On/Off	No change
IPMC Storage Err	SEEPROM error	Power On/Off	No change
Board Reset	Board Reset Source	Power On	No change

2.16.2.1 IPMB Link Sensor

The AT8001 provides two IPMB links to increase communication reliability to the shelf manager and other IPM devices on the IPMB bus. These IPMB links work together for increased throughput where both busses are actively used for communication at any point. A request might be received over IPMB Bus A, and the response is sent over IPMB Bus B. Any requests that time out are retried on the redundant IPMB bus. In the event of any link state changes, the event are written to the AT8001 SEL. IPMC monitors the bus for any link failure and isolates itself from the bus if it detects that it is causing errors on the bus. Events are sent to signify the failure of a bus or, conversely, the recovery of a bus.

2.16.2.2 FRU Hot Swap

The hot-swap event message conveys the current state of the FRU, the previous state, and a cause of the state change as can be determined by the IPMC. Refer to PICMG 3.0 Specifications for further details on the hot-swap state.

2.16.3 Field Replaceable Unit (FRU) Information

The FRU Information provides inventory data about the boards where the FRU Information Device is located. The part number or version number can be read through software.

FRU information in the AT8001 includes data describing the AT8001 board as per PICMG 3.0 specification requirements. Additional multirecords will be added for the BIOS to write CPU information, BIOS version number, and PMC information to FRU data correctly. This information is retrieved by the shelf manager (ShMC), enabling reporting of board-specific information through an out-of-band mechanism.

Following are the definitions for the multirecord implemented by the firmware as part of FRU data.

2.16.4 E-Keying

E-Keying has been defined in the PICMG 3.0 Specification to prevent board damage, prevent misoperation, and verify fabric compatibility. The FRU data contains the board point-to-point connectivity record as described in Section 3.7.2.3 of the PICMG 3.0 specification.

Upon management power-on, the firmware sets the Fibre Channel ports to front panel by default. When the board enters M3 power state, the shelf manager reads in the board point-to-point connectivity record from FRU and determines whether the board can enable the Fibre Channel ports to the back plane. Set/Get Port State IPMI commands defined by the PICMG 3.0 specification are used for either granting or rejecting the E-keys.

If user Fibre Channel selection is to the front, the firmware maintains the Fibre Channel ports to the front panel regardless of the shelf manager's granting or rejecting of E-keys for the board.

Additionnal E-Keying is prodived for connectivity between the AMC carrier and the AMC bays as described the in Section 3.9 and 3.7 of the AMC.0 RC.1.1 specification. The Set/Get AMC Port State IPMI commands defined by the AMC.0 specification are used for either granting or rejecting the E-keys.

2.16.5 IPMC Firmware Code

IPMC firmware code is organized into boot code and operational code, both of which are stored in a flash module. Upon an IPMC reset, the IPMC executes the boot code and performs the following:
1- Self test to verify the status of its hardware and memory.
2- Performs a checksum of the operational code.
3- Communicates with the Firmware Upgrade Manager (FWUM) in order to inform the IPMC watchdog that
the actual IPMC firmware is suitable for execution.

Upon successful verification of the operational code checksum, the firmware will jump to the operational code.

2.16.6 IPMC Firmware Upgrade Procedure

It is important to use compatible BIOS, IPMC, FWUM and FPGA versions. Since all these software and hardware solution are exchanging information, they must be in synch. Please always follow Kontron documentation for all your upgrade.
The recommended upgrade sequence must be : FPGA, FWUM, IPMC, BIOS.
You are able to read the actual version of FPGA, FWUM and IPMC using the tool IPMIFWU V3.4. The BIOS version is written at every boot during BIOS POST, you can also get it by entering BIOS Setup Menu. The BIOS Setup does also provide the IPMC firmware version, via the IPMI Menu.

IPMC Firmware upgrades can be done by using IPMITOOL. It has been desigh to upgrade through any IPMI interface without payload impact

2.16.7 FWUM Firmware Upgrade Procedure

It is important to use compatible BIOS, IPMC, FWUM and FPGA versions. Since all these software and hardware solution are exchanging information, they must be in synch. Please always follow Kontron documentation for all your upgrade.

The recommended upgrade sequence must be : FPGA, FWUM, IPMC, BIOS.
You are able to read the actual version of FPGA, FWUM and IPMC using the tool IPMIFWU V3.4. The BIOS version is written at every boot during BIOS POST, you can also get it by entering BIOS Setup Menu. The BIOS Setup does also provide the IPMC firmware version, via the IPMI Menu.

FWUM Firmware upgrade is done using IPMIFWU utility. This is a Linux utility developed by Kontron that use the serial port to exchange with the FirmWare Upgrade Manager (FWUM) in order to upgrade to FWUM or the IPMC firmware. Then this tool doesn't need the KCS driver to run (it doesn't use the IPMI interfaces).

Type the following to perform IPMC firmware upgrade

ipmifwu –p –f <FWUM_firmware_filename> -m <enter>

Please note that during FWUM firmware upgrade the IPMC is held in reset.

2.16.8 Updating AT8001 BIOS

The AMI Linux upgrade utility is used to upgrade the BIOS.
Please note that you'll have to reboot in order to take advantage of the new BIOS.

It is important to use compatible BIOS, IPMC, FWUM and FPGA versions. Since all these software and hardware solution are exchanging information, they must be in synch. Please always follow Kontron documentation for all your upgrade.
The recommended upgrade sequence must be: FPGA, FWUM, IPMC, BIOS.
You are able to read the actual version of FPGA, FWUM and IPMC using the tool IPMIFWU V3.4. The BIOS version is written at every boot during BIOS POST, you can also get it by entering BIOS Setup Menu. The BIOS Setup does also provide the IPMC firmware version, via the IPMI Menu.

Type the following:

afulnx2 /i<BIOS_BIN_File_Name> /pbnc <enter>
(no space between /I and the filename)

/pbnc is for

b - Program Boot Block
n - Program NVRAM
c - Destroy System CMOS

After the upgrade process is completed, reboot by typing

Ctrl-alt-del keys

During BIOS POST, enter BIOS Setup Menu by typing

Del key

In BIOS Setup Menu, make sure to select BIOS Optimal Default Settings by typing F9 key

2.16.9 OEM IPMI Commands

This section documents the OEM style IPMI commands implemented and supported on the AT8001.

Command Name	NetFunction	Command
Reset BIOS Flash Type	3A	01
Get Fibre Channel Port Selection	3A	02
Set Fibre Channel Port Selection	3A	03
Get HW Fibre Channel Port Selection	3A	04
Set Control State	3E	20
Get Control State	3E	21

2.16.9.1 Reset BIOS Flash Type

This command resets the processor and changes the BIOS bank select signal so that CPU boots off redundant BIOS bank.

	7	6	5	4	3	2	1	0
NetFn/LUN	NetFn = 3Ah (OEM Request)						RsLUN	
Command	Cmd = 01h							
Byte 1	BIOS checksum success/failure indication 00h Checksum success 01h Checksum failure							
Byte 1	Completion code							

2.16.9.2 Set Control State

This command sets the state of a control pin and overrides the control pin's auto state

	7	6	5	4	3	2	1	0
NetFn/LUN	NetFn = 3Eh (OEM Request)						RsLUN	
Command	Cmd = 20h							
Byte 1								
Byte 2	= Deassert, 1 = Assert, 3 = Reserved, FF = Don't change settings							
Byte 1	Completion code							

2.16.9.3 Get Control State

This command sets the state of a control pin. This command overrides the AUTO-state of the control pin.

	7	6	5	4	3	2	1	0
NetFn/LUN	NetFn = 3Eh (OEM Request)						RsLUN	
Command	Cmd = 20h							
Byte 1	Control number							
Byte 1	Completion code							
Byte 2	Control state, 0 = Deassert, 1 = Assert, 3 = Reserved, FF = Don't change settings							

2.16.9.4 Controls Identifier Table

This table lists the control identifiers that can be used with Set/Get Control State IPMI commands to query or set information on certain controls in the firmware.

Control Description	Control Number
FWH Hub (for BIOS bank information)0	0
FWH 0 Write Protect	1
FWH 1 Write Protect	2
FWH 0 Top Block Lock	3
FWH 1 Top Block Lock4	4

2.16.9.5 Hot-Swap Process

The AT8001 SBC has the ability to be hot-swapped in and out of a chassis. The onboard IPMC manages the SBC's power-up and power-down transitions. The list below illustrates this process for power down request.

1- Ejector latch is opened. HOT_SWAP_PB# assertion. IPMC firmware detects the assertion of this signal.
2- IPMC sends "Deactivation Request" message to SHMC. M state moves from M4-> M5.
3- Board moves from M5 -> M6 if the SHMC grants the request.
4- The IPMC's ACPI timer (3 minutes) starts if an ACPI-enable OS is loaded. Otherwise, it goes to Step 7 below. The IPMC asserts 20 ms pulse on SMC_PWRBTN#.
5- The Power Button Status register is set. It then asserts SCI# to the OS. If ACPI OS is enabled, SCI interrupt handler on the OS is called. Interrupt handler clears PWRBTN_STS bit. OS starts to perform a graceful shutdown.
6- The firmware deasserts payload power and sets the IPMI locked bit before it transitions from M6 to M1 state.



Note:
If the upper-level software moves the IPMC to M6, the same procedure is followed, starting with Step 4.

2.16.9.6 Hot-Swap LED

The AT8001 SBC supports a blue Hot Swap LED mounted on the front panel. The position of this LED depends on the board option and may be near the top handle or near the bottom handle. This LED indicates when it is safe to remove the SBC from the chassis. The on-board IPMC drives this LED to indicate the hot-swap state. The following states are possible:

LED state	Description
OFF	Board is in M4 state, normal state when board is in operation.
ON	Ready for hot swap.
Short blink	M5 state deactivation request
Long blink	M2 state Activation Request.

When the lower ejector handle is disengaged from the faceplate, the hot swap switch embedded in the PCB will assert a "HOT_SWAP_PB#" signal to the IPMC, and the IPMC will move from the M4 state to the M5 state. At the M5 state, the IPMC will ask the SHMC (or Shelf Manager) for permission

to move to the M6 state. The Hot Swap LED will indicate this state with a short blink. Once permission is received from the SHMC or higher-level software, the SBC will move to the M6 state.

The SHMC or higher level software can reject the request to move to the M6 state. If this occurs, the Hot Swap LED returns to a solid off condition, indicating that the SBC has returned to M4 state.

If the SBC reaches the M6 state, either through an extraction request through the lower ejector handle or a direct command from higher-level software and an ACPI-enabled OS is loaded on the SBC, the IPMC communicates to the OS that the module must discontinue operation in preparation for removal. The Hot Swap LED continues to flash during this preparation time, just like it does at the M5 state. When main board power is successfully removed from the SBC, the Hot Swap LED remains lit, indicating it is safe to remove the SBC from the chassis.

LED Status	Meaning
Off	Normal status
Blinking Blue	Preparing for removal/insertion: Long blink indicates activation is in progress, short blink when deactivation is in progress.
Solid Blue	Ready for hot swap

2.16.9.7 Ejector Mechanism

In addition to captive retaining screws, the AT8001 SBC has two ejector mechanisms to provide a positive cam action; this ensures the blade is properly seated. The bottom ejector handle also has a switch that is connected to the IPMC to determine if the board has been properly inserted.

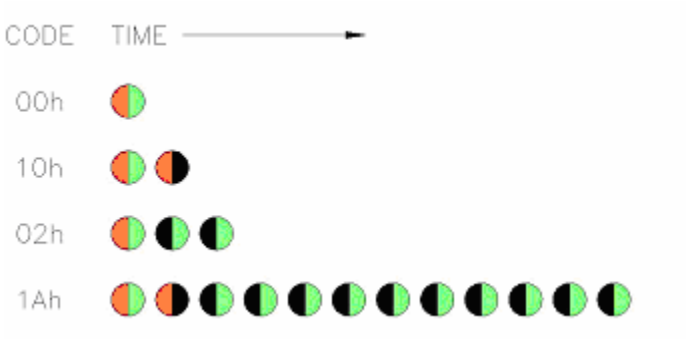
2.17 Debugging Features

2.17.1 POST Code Blinker / IDE Activity

The postcode blinker circuit uses a blinking sequence to display the current POST (Power On Self Test) code value on faceplate. This functionality is shared with the hard drive activity LED. This sequence restarts every time the POST codes value changes. Because POST codes changes all the time during a normal boot process, the blinker does not have enough time to complete its sequence and the debug LED blinks meaninglessly.
If the boot process succeeds, the POST code value has no interest and the BIOS will disable the post code blinker before the operating system launches.
If the boot sequence fails or the CPU hangs, the postcode blinker remains operational and repeats indefinitely the last postcode blink sequence defined below.

1. Blink simultaneously AMBER and GREEN one time: start of the sequence.
2. Blink AMBER "A" times while GREEN stays off. "A" range from 0 to 15.
3. Blink GREEN "G" times while AMBER stays off. "G" range from 0 to 15.
4. Repeat the sequence. (See step 1.)

"A" is the first (most significant) digit of the post code value in hexadecimal; while "G" is the second digit (i.e. post code value is AGh). Some examples are shown in the following figure.



2.17.2 Serial POST Codes

Kontron's serial POST Code display module (T2603) can be used with this board. The module is plugged on J13 or on the RTM RT8000 if available. It can display the BIOS POST codes (i.e. content of I/O locations 80-81h) or the IPMC POST codes depending on the presence of jumper JP7(1-2).

IPMC POST codes are only 8-bit and they are displayed with a "db" prefix (ex.: dbA4 for post A4h).

Also, a hardware status is displayed when the reset-switch is pressed. In this case, the code displayed has the meaning defined below.

T2603	Digit	Bit	Description	0123	4567	89AB	CDEF
	0 LSB	3	SKTOCC# (0 = CPU present)	0000	0000	1111	1111
		2	CPU_VTTEN (0 = wrong type of Xeon)	0000	1111	0000	1111
		1	BSEL1	0011	0011	0011	0011
		0	BSEL0	0101	0101	0101	0101
	1	3	JP7	0000	0000	1111	1111
		2	JP7	0000	1111	0000	1111
		1	SUSPEND#	0011	0011	0011	0011
		0	Vcore ok	0101	0101	0101	0101
	2	3	VTT (1.2V) ok	0000	0000	1111	1111
		2	1.5V ok	0000	1111	0000	1111
		1	1.8V ok	0011	0011	0011	0011
		0	2.5V ok	0101	0101	0101	0101
	3 MSB	3	3.3V ok	0000	0000	1111	1111
		2	5V ok	0000	1111	0000	1111
		1	12V ok	0011	0011	0011	0011
		0	3.3Vsus ok	0101	0101	0101	0101

Dependencies between supplies are as follow:

1. 12V, 5V and 1.8V start with no conditions
2. 3.3V starts when 1.8V is stable
3. 1.5V starts when 3.3V is stable
4. VTT starts when 12V and 1.5V are stable
5. 2.5V starts when 12V and 3.3V are stable
6. Vcore starts after a delay when 12V is stable

If the boot sequence fails or the CPU hangs, the postcode blinker remains operational and repeats indefinitely the last postcode blink sequence defined below.

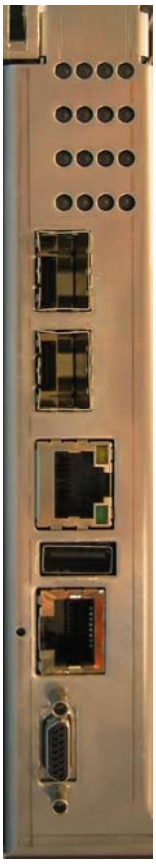
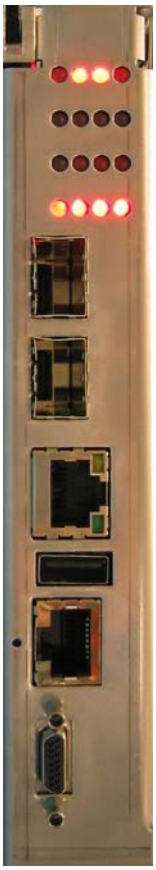
2.17.3 User LED 1 and 2

A status LED can be very useful for software development and for system level troubleshooting. Consult register 0x19A description for software usage (Appendix C). All the LEDs are available by IPMI has define in the PICMG specification 3.0

2.17.4 Lamp Test

The lamp test does the sequence shown below in the order 1-2-3-4-1-2-3- etc. Step 4 is not displayed when the regional bit is set for Europe (no red allowed). The lamp test can be initiated by software (IPMC) or just by pressing the reset pushbutton long enough.

LED arangement and face plate finish may vary depending on board configuration.

#1 No LEDs	#2 All green & blue LEDs	#3 All amber LEDs	#4 All red LEDs
			

2.17.5 IPMI controlled LED

The green Management LED represent when pulsing acommunication between Host Interface and IPMC
The green Management LED represent the IPMC heart beat when it blink slowly
The amber Management LED represent IPMC communication over IPMB-0 when pulsing

3. Installing the board

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3.5 Board Hot Swap and Installation 3-7

3.1 Setting Jumpers

3.1.1 Jumper Description

Description		
Clear CMOS	To clear the CMOS, power down the board, put the jumper in for a second and then remove it.	**JP2**
Console Redirection	To enable the Console Redirection Mode, put the jumper in.	**JP3**
Onboard Video	Use this jumper to disable the onboard video feature.	**JP4**
Video Position	Put a jumper in to route the video to the front connector.	**JP5**
Board Activation Override	When present, this jumper tells the IPMC to turn-on the board regardless of shelf manager authorisation. Typically used in a chassis wihtout a shelf manager (ShMC).	**JP6(1-2)**
AMC Activation Override	When present, this jumper tells the IPMC to turn-on the power of both AMCs regardless of shelf manager authorisation. Note that E-Keying is still used to control connection of AMC ports. The jumper needs to be present at power-up and is typically used in development (AMC with non-functionnal MMC (module management controller)).	**JP6(3-4)**
PostCode Source	The serial post-code display module will normally display the BIOS postcodes. When this jumper is present, IPMC postcodes are displayed instead. This is usefull for IPMC firmaware developpement and debugging.	**JP7(1-2)**
Always ON (IPMI override)	Put a jumper in to disable the IPMC and FWUM and turn-on the board.	**JP7(3-4)**
FPGA Configuration	User PROM. This PROM is field upgradable. This jumper should be present for normal use. Note that one, and only one, jumper must be present on JP8 (either 1-2 or 3-4).	**JP8(1-2)**
FPGA Configuration	Factory PROM. This is the safe configuration programmed in factory. This PROM cannot be updated in the field.	**JP8(3-4)**
PMC PCI M66EN	Put a jumper to restrict the conventional PCI speed of the PMC to 33MHz. Note that this does not affect the PCI-X speed.	**JP9(1-2)**
PMC PCI-X PCIXCAP	Put a jumper to disable PCI-X on the PMC and fall-back to conventional PCI mode.	**JP9(3-4)**
RESERVED	For manufacturing use. Do not put a jumper at this location for normal use.	**JP10**
ShMC Mode	When a jumper is present, the IPMC will act as a ShMC. The IPMC will answer at address 0x20 and provides 2.7K pull up on the IPMB bus. Note that proper software must run on the AT8001 in this mode for this to be usefull.	**JP11**
IDE 2,5" drive	Consult the Hard disk specification.	**JP12**

3.1.2 Setting Jumper & locations

JP1 - Spare Jumper	
• Spare Jumper	in

JP2 - Clear CMOS	
Clear CMOS	in
• Normal	out

JP3 - VT100 Mode	
Enabled	in
• Disabled	out

JP4 - Video	
Disable Video	in
• Normal	out

JP5 - Video Position	
• Front	in
Rear	out

JP6 - Overide Function	
ShMC Activation Override	1-2
Reserved	3-4

JP7(1-2) - Postcode	
Postcode to IPMC	in
• Postcode to BIOS	out

JP7(3-4) - IPMI Override	
Always On	in
• Normal Mode	out

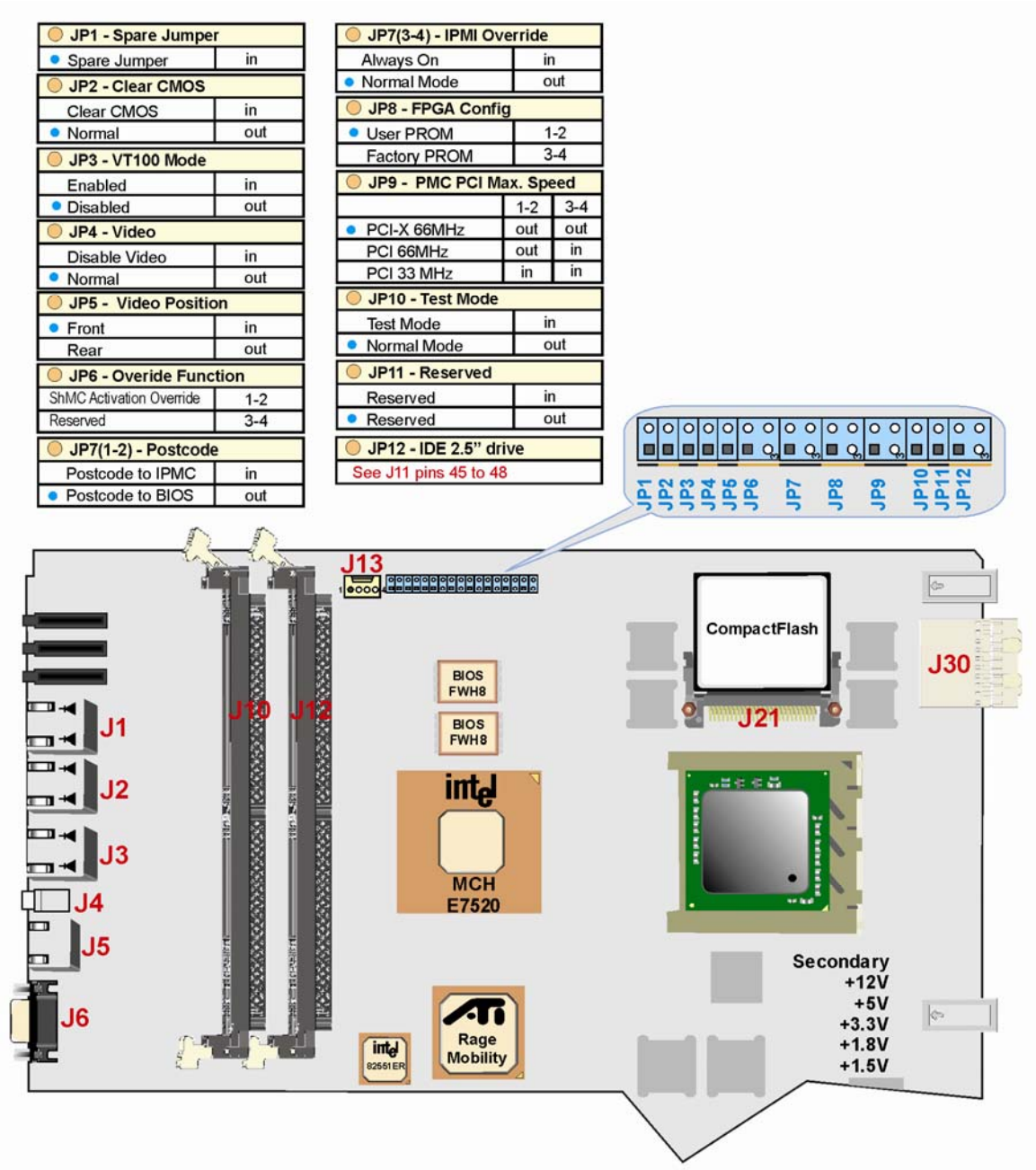
JP8 - FPGA Config	
• User PROM	1-2
Factory PROM	3-4

JP9 - PMC PCI Max. Speed		
	1-2	3-4
• PCI-X 66MHz	out	out
PCI 66MHz	out	in
PCI 33 MHz	in	in

JP10 - Test Mode	
Test Mode	in
• Normal Mode	out

JP11 - Reserved	
Reserved	in
• Reserved	out

JP12 - IDE 2.5" drive
See J11 pins 45 to 48



3.2 Processor

This product ships with the CPU installed and a thermal solution installed. Because the thermal solution is custom and the thermal interface is critical for passive cooling, Kontron does not guarantee thermal performance if the heat sink is removed and then reinstalled by the end user.

3.3 Memory

Only use validated memory with this product. Currently recommended configuration and part numbers are:

Manufacturer Part Number	Description	Company
M393T6450FG0-CCC	DIMM DDR2-400 512MB 64M*72 REG ECC	Samsung Semiconductor
MT18HTF12872Y-40EA1	DIMM DDR2-400 1GB 128M*72 REG ECC 1	Micron Technology, Inc.
MT18HTF12872Y-40EA2	DIMM DDR2-400 1GB 128M*72 REG ECC 1	Micron Technology, Inc.
M393T2950BG0-CCC	DIMM DDR2-400 1GB 128M*72 REG ECC 1	Samsung Semiconductor
M393T2950BZ0-CCC	DIMM DDR2-400 1GB 128M*72 REG ECC 1	Samsung Semiconductor
M393T5750BS0-CCC	DIMM DDR2-400 2GB 256M*72 REG ECC 1	Samsung Semiconductor
M393T5750BS0-D5C	DIMM DDR2-400 2GB 256M*72 REG ECC 1	Samsung Semiconductor
M393T5750BY0-CCC	DIMM DDR2-400 2GB 256M*72 REG ECC 1	Samsung Semiconductor
MT18HTF25672Y-40EA1	DIMM DDR2-400 2GB 256M*72 REG ECC 1	Micron Technology, Inc.

Memory should have the following characteristics:

- DDR2 400
- 1.8V only
- Single-sided or double-sided
- 1 layer of BGA on PCB side
- X4 or X8 configuration supported
- Serial Presence Detect (SPD) EEPROM
- 72-bit DIMMs only
- 1.45 inch maximum height

WARNING

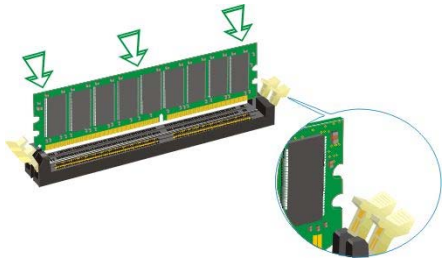
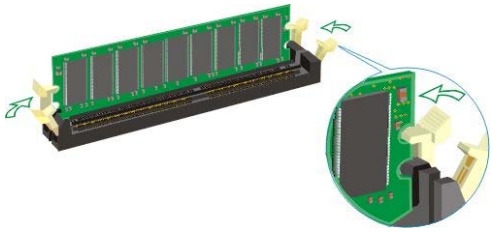
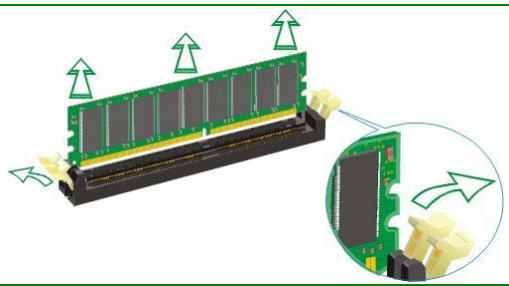


Because static electricity can cause damage to electronic devices, take the following precautions:

- Keep the board in its anti-static package, until you are ready to install memory.
- Wear a grounding wrist strap before removing the board from its package; this will discharge any static electricity that may have built up in your body.
- Handle the board by the faceplate or its edges.



3.3.1 Installing Memory

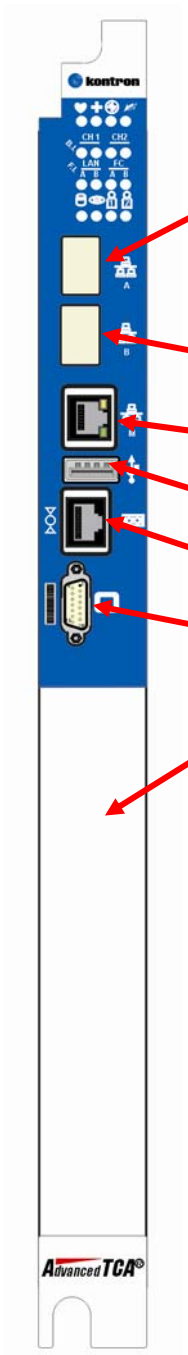
On an anti-static plane, place the board so that you are facing the memory sockets	
Insert the memory module into any available socket, aligning the notches on the module with the socket's key inserts.	
Push down the memory module until the retaining clips clip on each side.	
Repeat these steps to populate the other socket.	
To remove a memory module from a socket, push sideway the retaining clips on each side of the socket, to release the module. Pull out the memory from the socket.	

3.4 Onboard Interconnectivity

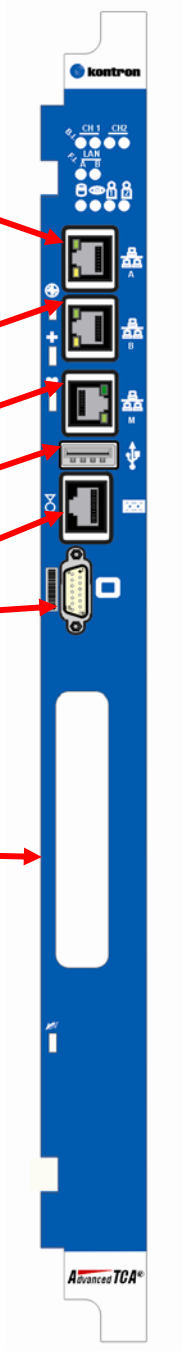
3.4.1 Onboard Connectors and Headers

Description	Connector	Comments
SFP Module 0	M1	Fibre channel or gigabit ethernet (Optional)
RJ45 Copper		gigabit ethernet (Optional)
SFP Module 1	M2	Fibre channel or gigabit ethernet (Optional)
RJ45 Copper		gigabit ethernet (Optional)
Ethernet Management	J3	RJ-45 connector with integrated speed and activity/link LED
USB 0	J4	Standard USB2.0 and USB1.1 port
Serial Port	J5	RJ-45 connector. See section XXX for pinout
VGA	J6	Micro-D15 need an adapter to transfer it to a regular DB15
Memory Sockets	J10,J12	240 pins standard memory socket DDRII-400
2.5" Hard Disk	J11	50 pins connector for use with IDE platform (Optional)
POST Code Connector	J13	Four pin connector for use with Kontron T2601 postcode module.
AMC B1	J18	Standard type B+ AMC connector (Optional)
AMC B2	J19	Standard type B+ AMC connector(Optional)
CompactFlash	J21	Type I connector with retainer
ATCA Base & Fabric Interface	J20,J23	Standard ATCA connector with 40 differential pairs
ATCA RTM Connector	J30	Standard ATCA connector with 40 differential pairs
Power	P10	Standard ATCA power connector
PCI Mezzanine	JN1-JN3	PMC connectors for 64-Bit PCI-X Mezzanine (Optional)

3.4.2 Front Plate Connectors and Indicators



Name	Description	Comments
J1	SFP Channel A	Small form factor pluggable module. Use an appropriate module depending on the data that will be routed to the SFP from the cross point switch. Kontron provides 2Gb module that will work for Fibre channel and gigabit Ethernet
J2	SFP Channel B	Same as above.
J3	Ethernet Management	10/100Mbit, standard RJ-45 connector.
J4	USB 0	4-Pin standard USB connector
J5	Serial Port	Standard 8-pin RJ-45 connector
J6	VGA	Micro DB-15. Use provided cable adapter to connect a monitor
	AMC B1 & AMC B2	Slot for full heigh half width AMC type B+. When no AMC used, a filler shall be installed.
	PMC & Hard Disk	The front plate supports a PMC cutout and a cap that also acts as an EMI shield when there is no PMC device installed.



3.5 Board Hot Swap and Installation

Because of the high-density pinout of the hard-metric connector, some precautions must be taken when connecting or disconnecting a board to/from a backplane:

1. Rail guides must be installed on the enclosure to slide the board to the backplane.
2. Do not force the board if there is mechanical resistance while inserting the board.
3. Screw the frontplate to the enclosure to firmly attach the board to its enclosure.
4. Use extractor handles to disconnect and extract the board from its enclosure.

WARNING



Always use a grounding wrist wrap before installing or removing the board from a chassis.



3.5.1 Installing the Card in the Chassis

To install a card in a chassis:

1. Remove the filler panel of the slot or see “Removing the Card” below.
2. Ensure the board is configured properly.
3. Carefully align the PCB edges in the bottom and top card guide.
4. Insert the board in the system until it makes contact with the backplane connectors.
5. Using both ejector handles, engage the board in the backplane connectors until both ejectors are locked.
6. Fasten screws at the top and bottom of the faceplate.

3.5.2 Removing the Board

If you would like to remove a card from your chassis please follow carefully these steps:

1. Unscrew the top and the bottom screw of the front panel.
2. Unlock the lower handle latch, depending on the software step, this may initiate a clean shutdown off the operating system.
3. Wait until the blue LED is fully ON, this mean that the hot swap sequence is ready for board removal.
4. Using both ejectors, disengage the board from the backplane.
5. Pull the board out of the chassis.

3.5.3 Installing a PMC Card

To install a PMC card:

1. Remove the front EMI cap.
2. Carefully push the PMC to mate the three connectors.
3. Screw the four screws at the bottom of the PMC to fix it to the board.
4. Power up the board and verify the PMC functionnality.

WARNING



- This feature is only available when you don't a have the AMC option
- You cannot have an AMC and a PMC at the same time



3.5.4 Installing an AMC

To install an AMC:

1. Remove the AMC filler panel.
2. Carefully engage the AMC into the card guide. Push the AMC until it fully mate with it's connector. Secure the AMC handle to the locking position..
3. In normal condition, the blue LED shall turn ON as soon as the AMC is fully inserted. It will turn OFF at the end of the hot swap sequence.

For AMC hot swap support to work, you must use an operating system with PCI Express hot swap support.

WARNING



- This feature is only available when you don't a have a PMC
- You cannot have an AMC and a PMC at the same time



3.5.5 Installing an hard disk

To install an hard disk:

1. Carefully connect the disk to the IDE connector.
2. Screw the four screws at the bottom of the board to fix it to the board.
3. Boot the AT8001 and make sure the drive is detected by the BIOS setup.

WARNING



- This feature is only available when you don't a have a AMC
- You cannot have an hard disk and a AMC at the same time



3.5.6 Installing a CompactFlash

This product supports all type I CompactFlash modules.

WARNING



Never install or remove the compact flash while the board is on.



To install the CompactFlash:

1. Insert the CompactFlash in place (J21).
2. Close the retention clip on it.

To remove the CompactFlash:

1. Open the retention clip.
2. Pull the CompactFlash module out.

4. Building an ATCA System

Contents

4.1 Building an ATCA System 4-1

4.1 Building an ATCA System

The basic components needed to build an ATCA system include:

1) Chassis (which includes backplane, power supply or power entry modules, fans)
2) Base interface switches and optionnality fabric interface switches
3) Shelf manager controllers (ShMC)
4) One or more AT8001 or other ATCA node boards
5) Possibly some rear transition modules

Consult Kontron's web site for available chassis, switches and node boards.

See your system's manual for more details.



4.1.1 Backplane

The AT8001 is compliant to ATCA 3.0R1.0 spec. It can be used in a Dual Star or a Full Mesh configuration.

4.1.2 Rear-Panel I/O

This feature is intended to extend the I/O capabilities of the AT8001 to the rear of the enclosure using a RTM I/O (RT8000).
The RTM I/O module gathers all the I/O signals of the CPU board and makes them easily accessible through standard headers and connectors located at the rear of enclosure. For more information about the RT8000 transition module, please consult our web site at: www.kontron.com

WARNING

Always use Kontron's RTM with your Kontron's front board or permanent damage could occur.

4.1.3 External Storage Devices

The AT8001 supports external storage device either through the fibre chanel interface (front SFP module or via a fabric interface switch) or through SATA connectors on the RTM. Note that SATA is only available on the RTM with some option of the AT8001.

4.1.4 Power Supply

The AT8001 expects two –48V feeds as per PICMG3.0R1.0. The AT8001 is fully working over a range of –39.5V to –72V as required by the specification.

4.1.5 Connector Keying

Mechanical keying in ATCA system exists for the main backplane and for RTM. Currently only one key is defined for ATCA front board: A1/K1 key value is 11.

RTM key is defined by front board manufacturer. Currently, Kontron use the A2/K2 value of 11 for it's front CPU board and matching RTM.

Specific connectivity either with the backplane or the RTM may vary and electronic keying (E-Keying) allow the IPMC (intelligent platform management controller) to prevent connection of incompatible components.

5. Software Setup

Contents

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5.2 Boot Utilities 5-24

5.3 Console Redirection (VT100 Mode) 5-25

5.4 Installing Drivers 5-28

5.5 MontaVista 5-29

5.1 AMI BIOS Setup Program

All relevant information for operating the board and connected peripherals is stored in the CMOS memory backed-up by a supercap or in the main BIOS flash. The later if the default configuration.

5.1.1 Accessing the BIOS Setup Utility

The system BIOS (Basic Input Output System) provides an interface between the operating system and the hardware of the AT8001 SBC. It uses the AMI Setup program, a setup utility in flash memory that is accessed by pressing the <DELETE> key at the appropriate time during system boot. This utility is used to set configuration data in CMOS RAM.

To run the AMI Setup program incorporated in the ROM BIOS:

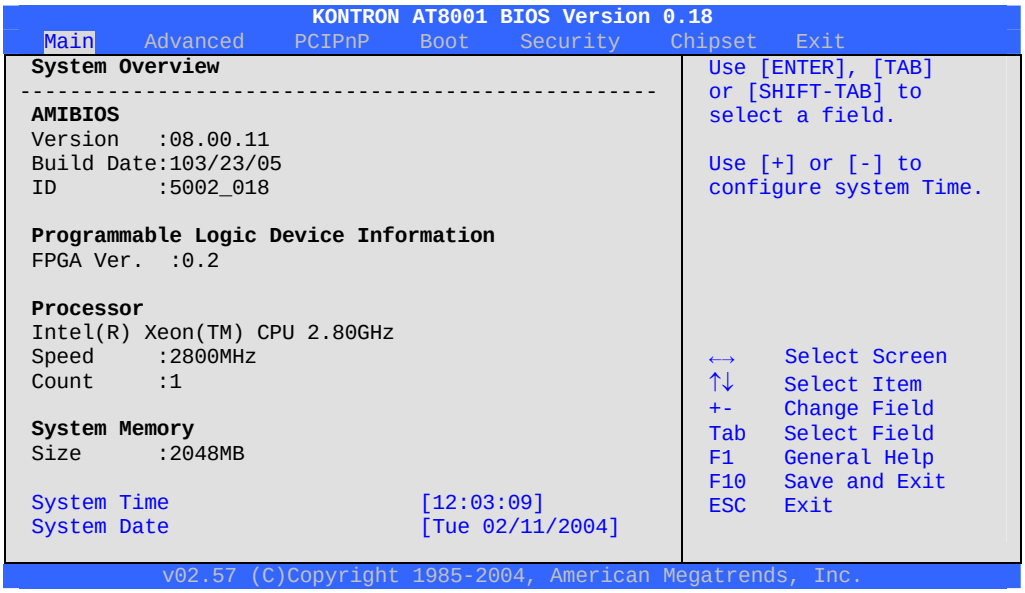
- Turn on or reboot the system.
- When you get the following messages, hit <DELETE> key (or F4 on Remote Keyboard) to enter SETUP.

AMIBIOS(C)2003 American Megatrends, Inc.
KONTRON AT8001 BIOS Version 0.18
CPU : Intel(R) Xeon(TM) CPU 2.80GHz
Speed : 2.80 GHz

Press DEL to run Setup (F4 on Remote Keyboard)
Press F11 for BBS POPUP (F3 on Remote Keyboard)

(C) American Megatrends, Inc.

The main menu of the AMI BIOS CMOS Setup Utility appears on the screen.



Setup Default values provide **optimum performance** settings for all devices and system features.



Note:

The CMOS setup option described in this section is based on **BIOS Version 0.18** The options and default settings may change in a new BIOS release.

CAUTION



These parameters have been provided to give control over the system. However, the values for these options should be changed only if the user has a full understanding of the timing relationships involved.



5.1.2 Menu Bar

The Menu Bar at the top of the window lists these selections:

Menu Selection	Description
Main	Use this menu for basic system configuration.
Advanced	Use this menu to set the Advanced Features available on your system.
PCIPnP	Use this menu to configure PCI and PnP features.
Boot	Use this menu to determine the booting device order.
Security	Use this menu to configure Security features.
Chipset	Use this menu to configure chipset features.
Exit	Use this menu to choose Exits option.

Use the left and right ← and → arrows keys to make a selection.

5.1.2.1 Legend Bar

Use the keys listed in the legend bar on the bottom to make your selections or exit the current menu. The chart on the following page describes the legend keys and their alternates.

Key	Function
<F1>	General Help windows (see 4.1.2.2).
<Esc>	Exit this menu.
← → arrow keys	Select a different menu.
<Home> or <End>	Move cursor to top or bottom of window.
<PgUp> or <PgDn>	Move cursor to top or bottom of window.
<->	Select the Previous Value for the field.
<+>	Select the Next Value for the field.
<F2> and <F3>	Change colors used in Setup.
<F7>	Disacard the changes for all menus.
<F8>	Load the Failsafe Default Configuration values for all menus.
<F9>	Load the Optimal Default Configuration values for all menus.
<F10>	Save and exit.
<Enter>	Execute Command, display possible value for this field or Select the sub-menu.

To select an item, use the arrow keys to move the cursor to the field you want. Then use the plus-and-minus value keys to select a value for that field. To save value commands in the Exit Menu, save the values displayed in all menus.

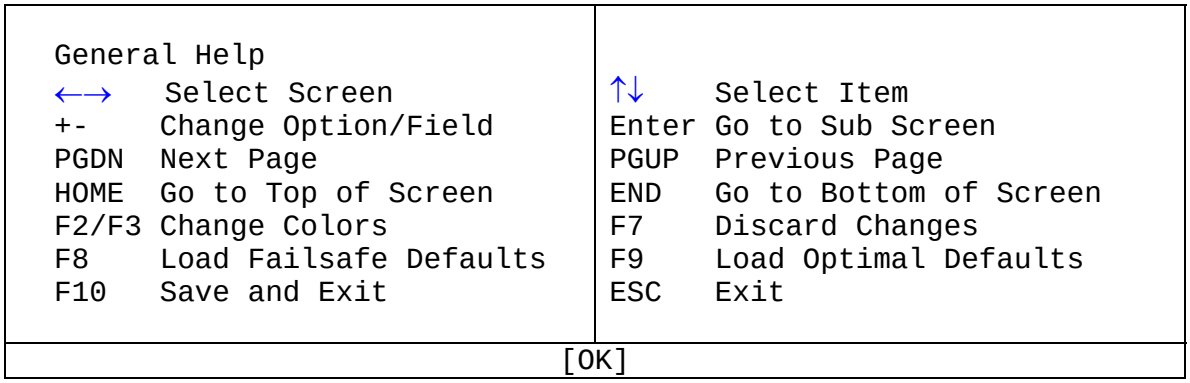
To display a submenu, use the arrow keys to move the cursor to the submenu you want. Then press <Enter>. A pointer ( ) marks all sub-menus.

5.1.2.2 *Field Help Window*

The help window on the right side of each menu displays the help text for the selected field. It updates as you move the cursor to each field.

5.1.2.3 *General Help Windows*

Pressing <F1>on any menu brings up the General Help window that describes the legend keys and their alternates:



5.1.2.4 Main Menu Selection

The scroll bar on the right of any windows indicates that there is more than one page of information in the windows. You can make the following selections on the Main Menu itself. Use submenus for other selections.

Feature	Options	Description
Version	Display only ex:	AMIBIOS Core version used with this BIOS.
Build Date	N/A	Build Date.
ID	N/A	OEM Identification code.
FPGA Ver.	N/A	Indicate the FPGA version (Programmable Logic)
Processor	N/A	Displays CPU Brand Name (show maximum CPU Speed available).
Speed	N/A	Displays current CPU Speed.
System Memory	N/A	Displays the amount of RAM memory detected during boot up.
System Time	HH:MM:SS	Set system time.
System Date	MM/DD/YYYY	Set system date.

5.1.2.5 Advanced Menu Selection

Feature	Options	Description
CPU Configuration	This is a Sub-Menu.	Configure CPU.
IDE Configuration	This is a Sub-Menu.	Configure the IDE device(s).
SuperIO Configuration	This is a Sub-Menu.	Configure SuperIO Chipset.
ACPI Configuration	This is a Sub-Menu.	Section for Advanced ACPI Configuration.
Event Log Configuration	This is a Sub-Menu.	Mark as read, Clear or View Event Log statistics.
MPS Configuration	This is a Sub-Menu.	Configure the Multi-Processor Table.
ATCA Channel Routing	This is a Sub-Menu.	Select the front panel or backplane (ATCA) Channel Connection. Warning! To switch the ports to backplane, you need E-key granting from shMC. If the ShMC rejects the E-key request, the port will remain at Front.
On-Board Device Configuration	This is a Sub-Menu.	Use this section to Enable/Disable special On-board Devices.
PCI Express Configuration	This is a Sub-Menu.	Configure PCI Express Support.
Remote Access Configuration	This is a Sub-Menu.	Configure Remote Access.
IPMI Configuration	This is a Sub-Menu.	IPMI configuration including server monitoring and event log.
USB Configuration	This is a Sub-Menu	Configure the USB Support.

5.1.2.5.1 CPU Configuration

Feature	Options	Description
Configure advanced CPU settings	Manufacturer Brand String Frequency FSB Speed Cache L1 Cache L2 Cache L3 Ratio Status Ration Actual Value	Displays only.
Ratio CMOS Setting	Varies. Values available are based on minimum/maximum ratios available.	Will display if CPU ratio is locked or unlocked and the minimum/maximum ratios available.
Max CPUID Value Limit	Disabled Enabled	This should be enabled order to boot legacy OSes that cannot support CPUs with extended CPUID functions.
CPU TM function	Disabled TM1	CPU Thermal Monitor mechanisms supported. TM2 only available if: 1.Freq.>3.6GHz FSB800 2.Freq.>2.8GHz FSB533
Execute Disable Bit	Disabled Enabled	When disabled, force the XD feature flag to always return 0.
Hardware Prefetcher	Disabled Enabled	This should be enabled in order to enable or disable the Hardware Prefetcher Disable Feature.
Adjacent Cache Line Prefetch	Disabled Enabled	This should be enabled in order to enable or disable the Adjacent Cache Line Prefetch Disable Feature.
Hyper-Threading technology	Disabled Enabled	Enabled for Windows XP and Linux 2.4.x (OS optimized for Hyper-Threading Technology).

5.1.2.5.2 IDE Configuration

Feature	Options	Description
IDE Configuration	Disabled P-ATA Only S-ATA Only P-ATA & S-ATA	Select IDE Mode. P-ATA Only: 4 P-ATA & 2 S-ATA S-ATA Only: 2 S-ATA P-ATA & S-ATA: 2 P-ATA & 2 S-ATA
S-ATA Running Enhanced Mode	Yes No	Set S-ATA Running Enhanced Mode.
P-ATA Channel Selection	Primary Secondary Both	Select P-ATA Channel
S-ATA Ports Definition	PO-3rd./P1-4th. Po-4th./P1-3rd.	Select S-ATA Ports
Primary IDE Master	This is a sub-menu	
Primary IDE Slave	This is a sub-menu	
Secondary IDE Master	This is a sub-menu	
Secondary IDE Slave	This is a sub-menu	
Third IDE Master	This is a sub-menu	
Fourth IDE Master	This is a sub-menu	
Hard Disk Write Protect	Disabled Enabled	Disabled/Enabled device write protection. This will be effective only if device is accessed through BIOS.
IDE Detect Time Out (sec)	0, 5, 10, 15, 20, 25, 30, 35	Select the time out value for detecting ATA/ATAPI device(s)

5.1.2.5.2.1 Primary IDE Master

Feature	Options	Description
Primary IDE Master	Device Vendor Size LBA Mode Block Mode PIO Mode Async DMA Ultra DMA S.M.A.R.T.	This is a list of modes and features supported by the drive, not how it is setup.
Type	Not installed Auto CD/DVD ARMD	Select the type of device connected to the system.
LBA/Large Mode	Disabled Auto	Disabled: Disables LBA Mode. Auto: Enables LBA Mode if the device supports it and the device is not already formatted with LBA Mode3 disabled
Block (Multi-Sector Transfer)	Disabled Auto	Disabled: the data transfer from and to the device occurs one sector at the time. Auto: the data transfer from and to the device occurs multiple sector at a time it the device supports it.
PIO Mode	Auto 0 1 2 3 4	Select PIO Mode.
DMA Mode	Auto SWDMA0 SWDMA1 SWDMA2 MWDMA0 MWDMA1 MWDMA2 UDMA0 UDMA1 UDMA2 UDMA3 UDMA4	Select DMA Mode. Auto: Auto detect SWDMAn: SingleWordDMAn MWDMAn: MultiWordDMAn UDMAn: UltraDMAn
S.M.A.R.T.	Auto Disabled Enabled	S.M.A.R.T. stands for Self-Monitoring, Analysis and Reporting Technology
32Bit Data Transfer	Disabled Enabled	Enable/Disabled 32-bit Data Transfer.

5.1.2.5.2.2 Primary IDE Slave

Feature	Options	Description
Primary IDE Slave	Device Vendor Size LBA Mode Block Mode PIO Mode Async DMA Ultra DMA S.M.A.R.T.	This is a list of modes and features supported by the drive, not how it is setup.
Type	Not installed Auto CD/DVD ARMD	Select the type of device connected to the system.
LBA/Large Mode	Disabled Auto	Disabled: Disables LBA Mode. Auto: Enables LBA Mode if the device supports it and the device is not already formatted with LBA Mode3 disabled
Block (Multi-Sector Transfer)	Disabled Auto	Disabled: the data transfer from and to the device occurs one sector at the time. Auto: the data transfer from and to the device occurs multiple sector at a time it the device supports it.
PIO Mode	Auto 0 1 2 3 4	Select PIO Mode.
DMA Mode	Auto SWDMA0 SWDMA1 SWDMA2 MWDMA0 MWDMA1 MWDMA2 UDMA0 UDMA1 UDMA2 UDMA3 UDMA4	Select DMA Mode. Auto: Auto detect SWDMAn: SingleWordDMAn MWDMAn: MultiWordDMAn UDMAn: UltraDMAn
S.M.A.R.T.	Auto Disabled Enabled	S.M.A.R.T. stands for Self-Monitoring, Analysis and Reporting Technology
32Bit Data Transfer	Disabled Enabled	Enable/Disabled 32-bit Data Transfer.

5.1.2.5.2.3 Secondary IDE Master

Feature	Options	Description
Secondary IDE Master	Device Vendor Size LBA Mode Block Mode PIO Mode Async DMA Ultra DMA S.M.A.R.T.	This is a list of modes and features supported by the drive, not how it is setup.
Type	Not installed Auto CD/DVD ARMD	Select the type of device connected to the system.
LBA/Large Mode	Disabled Auto	Disabled: Disables LBA Mode. Auto: Enables LBA Mode if the device supports it and the device is not already formatted with LBA Mode3 disabled
Block (Multi-Sector Transfer)	Disabled Auto	Disabled: the data transfer from and to the device occurs one sector at the time. Auto: the data transfer from and to the device occurs multiple sector at a time it the device supports it.
PIO Mode	Auto 0 1 2 3 4	Select PIO Mode.
DMA Mode	Auto SWDMA0 SWDMA1 SWDMA2 MWDMA0 MWDMA1 MWDMA2 UDMA0 UDMA1 UDMA2 UDMA3 UDMA4	Select DMA Mode. Auto: Auto detect SWDMAn: SingleWordDMAn MWDMAn: MultiWordDMAn UDMAn: UltraDMAn
S.M.A.R.T.	Auto Disabled Enabled	S.M.A.R.T. stands for Self-Monitoring, Analysis and Reporting Technology
32Bit Data Transfer	Disabled Enabled	Enable/Disabled 32-bit Data Transfer.

5.1.2.5.2.4 Secondary IDE Slave

Feature	Options	Description
Secondary IDE Slave	Device Vendor Size LBA Mode Block Mode PIO Mode Async DMA Ultra DMA S.M.A.R.T.	This is a list of modes and features supported by the drive, not how it is setup.
Type	Not installed Auto CD/DVD ARMD	Select the type of device connected to the system.
LBA/Large Mode	Disabled Auto	Disabled: Disables LBA Mode. Auto: Enables LBA Mode if the device supports it and the device is not already formatted with LBA Mode3 disabled
Block (Multi-Sector Transfer)	Disabled Auto	Disabled: the data transfer from and to the device occurs one sector at the time. Auto: the data transfer from and to the device occurs multiple sector at a time it the device supports it.
PIO Mode	Auto 0 1 2 3 4	Select PIO Mode.
DMA Mode	Auto SWDMA0 SWDMA1 SWDMA2 MWDMA0 MWDMA1 MWDMA2 UDMA0 UDMA1 UDMA2 UDMA3 UDMA4	Select DMA Mode. Auto: Auto detect SWDMAn: SingleWordDMAn MWDMAn: MultiWordDMAn UDMAn: UltraDMAn
S.M.A.R.T.	Auto Disabled Enabled	S.M.A.R.T. stands for Self-Monitoring, Analysis and Reporting Technology
32Bit Data Transfer	Disabled Enabled	Enable/Disabled 32-bit Data Transfer.

5.1.2.5.2.5 Third IDE Master

Feature	Options	Description
Third IDE Master	Device Vendor Size LBA Mode Block Mode PIO Mode Async DMA Ultra DMA S.M.A.R.T.	This is a list of modes and features supported by the drive, not how it is setup.
Type	Not installed Auto CD/DVD ARMD	Select the type of device connected to the system.
LBA/Large Mode	Disabled Auto	Disabled: Disables LBA Mode. Auto: Enables LBA Mode if the device supports it and the device is not already formatted with LBA Mode3 disabled
Block (Multi-Sector Transfer)	Disabled Auto	Disabled: the data transfer from and to the device occurs one sector at the time. Auto: the data transfer from and to the device occurs multiple sector at a time it the device supports it.
PIO Mode	Auto 0 1 2 3 4	Select PIO Mode.
DMA Mode	Auto SWDMA0 SWDMA1 SWDMA2 MWDMA0 MWDMA1 MWDMA2 UDMA0 UDMA1 UDMA2 UDMA3 UDMA4	Select DMA Mode. Auto: Auto detect SWDMAn: SingleWordDMAn MWDMAn: MultiWordDMAn UDMAn: UltraDMAn
S.M.A.R.T.	Auto Disabled Enabled	S.M.A.R.T. stands for Self-Monitoring, Analysis and Reporting Technology
32Bit Data Transfer	Disabled Enabled	Enable/Disabled 32-bit Data Transfer.

5.1.2.5.2.6 Fourth IDE Master

Feature	Options	Description
Fourth IDE Master	Device Vendor Size LBA Mode Block Mode PIO Mode Async DMA Ultra DMA S.M.A.R.T.	This is a list of modes and features supported by the drive, not how it is setup.
Type	Not installed Auto CD/DVD ARMD	Select the type of device connected to the system.
LBA/Large Mode	Disabled Auto	Disabled: Disables LBA Mode. Auto: Enables LBA Mode if the device supports it and the device is not already formatted with LBA Mode3 disabled
Block (Multi-Sector Transfer)	Disabled Auto	Disabled: the data transfer from and to the device occurs one sector at the time. Auto: the data transfer from and to the device occurs multiple sector at a time it the device supports it.
PIO Mode	Auto 0 1 2 3 4	Select PIO Mode.
DMA Mode	Auto SWDMA0 SWDMA1 SWDMA2 MWDMA0 MWDMA1 MWDMA2 UDMA0 UDMA1 UDMA2 UDMA3 UDMA4	Select DMA Mode. Auto: Auto detect SWDMAn: SingleWordDMAn MWDMAn: MultiWordDMAn UDMAn: UltraDMAn
S.M.A.R.T.	Auto Disabled Enabled	S.M.A.R.T. stands for Self-Monitoring, Analysis and Reporting Technology
32Bit Data Transfer	Disabled Enabled	Enable/Disabled 32-bit Data Transfer.

5.1.2.5.3 SuperIO Configuration

Feature	Options	Description
ICH SIO Serial Port1 Address	Disabled 3F8/IRQ4 2F8/IRQ3 3E8/IRQ4 2E8/IRQ3	Allows BIOS to select ICH Serial I/O Unit Serial Port 1 Base Addresses
ICH SIO Serial Port2 Address	Disabled 3F8/IRQ4 2F8/IRQ3 3E8/IRQ4 2E8/IRQ3	Allows BIOS to select ICH Serial I/O Unit Serial Port 2 Base Addresses
PLD POD Device	Disabled Enabled	Enable to use On-board LPT to program PLD using the On-board PLD POD Device.
Parallel Port Address	Disabled 378 278 3BC	Allow BIOS to Select Parallel Port Base Address.
Parallel Port Mode	Normal Bi-Directionnal ECP EPP ECP & EPP	Allows BIOS to Select Parallel Port Mode.
Parallel Port IRQ	IRQ5 IRQ7	Allow BIOS to Select Parallel Port IRQ

5.1.2.5.4 ACPI Configuration

Feature	Options	Description
Advanced ACPI Configuration	This is a Sub-Menu	Advanced ACPI Configuration settings Use this section to configure additional ACPI options.
Chipset ACPI Configuration	This is a Sub-Menu	Chipset ACPI related Configuration settings

5.1.2.5.4.1 Advanced ACPI Configuration

Feature	Options	Description
ACPI 2.0 Support	No Yes	Enable RSDP pointers to 64-bit Fixed System Description Tables.
ACPI APIC support	Disabled Enabled	Include ACPI APIC table pointer to RSDT pointer list.
AMI OEMB table	Disabled Enabled	Include OEMB table pointer to R(X)SDT pointer lists
Headless mode	Disabled Enabled	Enable / Disable Headless operation mode through ACPI.
Remote Access	Disabled Enabled	Select Remote Access type.
Terminal Type	ANSI VT100 VT-UTF8	Select the target terminal type.
Serial port number	ICH COM1 ICH COM2	Select Serial Port for console redirection. Make sure the selected port is enabled
Serial Port Mode	115200 8,n,1 57600 8,n,1 38400 8,n,1 19200 8,n,1 09600 8,n,1	Select Serial Port Settings.

5.1.2.5.4.2 Chipset ACPI Configuration

Feature	Options	Description
APIC ACPI SCI IRQ	Disabled Enabled	Enable/Disable APIC ACPI SCI IRQ.

5.1.2.5.5 Event Log Configuration

Feature	Options	Description
View Event Log		View all unread events
Mark all events as read		Mark all unread events as read.
Clear Event Log		Discard all events in the Event Log.
ECC Event Logging	Disabled Enabled	Enable or Disable ECC Event Logging
Hub Interface Event Logging	Disabled Enabled	Enable or Disable Hub Interface Event Logging
System Bus Event Logging	Disabled Enabled	Enable or Disable System Bus Event Logging
Memory Buffer Event Logging	Disabled Enabled	Enable or Disable Memory Buffer Event Logging
PCI Error Logging	Disabled Enabled	Enable or Disable PCI Error Logging
PCI Express Error Logging	Disabled Enabled	Enable or Disable PCI Express Advanced Error Logging.
Machine-Check Exception Action	Restart Execution Reboot System	Select what the BIOS Machine-Check Exception handler does when the program execution cannot be reliably restarted.

5.1.2.5.6 MPS Configuration

Feature	Options	Description
MPS Revision	1.1 1.4	Configures the Multiprocessor Specification (MPS) revision level. Some operating systems will require revision 1.1 for compatibility reasons.

5.1.2.5.7 ATCA Channel Routing (PICMG)

Feature	Options	Description
Actual Fabric LAN A Port State	Display Only	Display hardware actual state.
Fabric LAN A Port Setting	Disabled Front Panel A Fabric Ch1 Port 0	Select the front panel or backplane (ATCA) Channel connection. Warning! To switch the ports to backplane, you need E-key granting from ShMC. If the ShMC rejects the E-key request, the ports will remain at Front.
Actual Fabric LAN B port State	Display Only	Display hardware actual state.
Fabric LAN B Port Setting	Disabled Front Panel B Fabric Ch2 Port 0	Select the front panel or backplane (ATCA) Channel connection. Warning! To switch the ports to backplane, you need E-key granting from ShMC. If the ShMC rejects the E-key request, the ports will remain at Front.
Actual FC A Port State	Display Only	Display hardware actual state.
FC A Port Setting	Disabled Front Panel A Fabric Ch1 Port 3	Select the front panel or backplane (ATCA) Channel connection. Warning! To switch the ports to backplane, you need E-key granting from ShMC. If the ShMC rejects the E-key request, the ports will remain at Front.
Actual FC B Port State	Display Only	Display hardware actual state.
FC B Port Setting	Disabled Front Panel B Fabric Ch2 Port 3	Select the front panel or backplane (ATCA) Channel connection. Warning! To switch the ports to backplane, you need E-key granting from ShMC. If the ShMC rejects the E-key request, the ports will remain at Front.
Actual AMC B1 Port 0 State	Display Only	Display hardware actual state.
AMC B1 Port 0 Setting	Disabled Front Panel A Fabric Ch1 Port 0 Fabric Ch1 Port 1 Fabric Ch1 Port 3	Select the front panel or backplane (ATCA) Channel connection. Warning! To switch the ports to backplane, you need E-key granting from ShMC. If the ShMC rejects the E-key request, the ports will remain at Front.
Actual AMC B1 Port 1 State	Display Only	Display hardware actual state.
AMC B1 Port 1 Setting	Disabled Front Panel B Fabric Ch2 Port 0 Fabric Ch2 Port 1 Fabric Ch2 Port 3	Select the front panel or backplane (ATCA) Channel connection. Warning! To switch the ports to backplane, you need E-key granting from ShMC. If the ShMC rejects the E-key request, the ports will remain at Front.
Actual AMC B2 Port 0 State	Display Only	Display hardware actual state.
AMC B2 Port 0 Setting	Disabled Front Panel A Fabric Ch1 Port 0 Fabric Ch1 Port 1 Fabric Ch1 Port 3	Select the front panel or backplane (ATCA) Channel connection. Warning! To switch the ports to backplane, you need E-key granting from ShMC. If the ShMC rejects the E-key request, the ports will remain at Front.
Actual AMC B2 Port 1 State	Display Only	Display hardware actual state.
AMC B2 Port 1 Setting	Disabled Front Panel B Fabric Ch2 Port 0 Fabric Ch2 Port 1 Fabric Ch2 Port 3	Select the front panel or backplane (ATCA) Channel connection. Warning! To switch the ports to backplane, you need E-key granting from ShMC. If the ShMC rejects the E-key request, the ports will remain at Front.

5.1.2.5.8 On-Board Devices Configuration

Feature	Options	Description
On-board Fiber Channel	This is a title.	Configure On-board Fibre Channel Controller
Option ROM	Disabled Enabled	Initialize device expansion ROM.
On-Board Dual Ethernet 1	This is a title.	Configure On-board Dual-Ethernet 1 Controller
Option ROM Function A	Disabled Enabled	Initialize device expansion ROM. IBA GE Slot 0308 in Boot Menu. ATCA Base CH 1.
Option ROM Function B	Disabled Enabled	Initialize device expansion ROM. IBA GE Slot 0309 in Boot Menu. ATCA Base CH 2.
On-Board Dual Ethernet 2	This is a title.	Configure On-board Dual-Ethernet 2 Controller
Option ROM Function A	Disabled Enabled	Initialize device expansion ROM. IBA GE Slot 0310 in Boot Menu. ATCA Fabric Port 0.
Option ROM Function B	Disabled Enabled	Initialize device expansion ROM. IBA GE Slot 0311 in Boot Menu. ATCA Fabric Port 1.
LAN i82551er Routing	Follow VGA Front Rear	Set to Rear to use i82551er on RTM connector. Set Front to use connector on Front panel.

5.1.2.5.9 PCI Express Configuration

Feature	Options	Description
PCIe Jitter Tolerance	Disabled Enabled	Enable/Disable PCIe Jitter Tolerance.
PCIe Compliance mode	Disabled Enabled	Enable/Disable MCH entering PCI Express compliance mode.
PCI Express Port 4	Auto Disabled Enabled	Auto: Visible if Card Enable: Always visible Disable: Always Hide
Hot Plug Support – AMC B2	Disabled Enabled	Enabled: Set PCI Express Hot Plug capability. Disabled: Hot Plug is not available on this port.
PCI Express Port 6 – AMC B1	Auto Disabled Enabled	Auto: Visible if Card Enable: Always visible Disable: Always Hide
Hot Plug Support – AMC B1	Disabled Enabled	Enabled: Set PCI Express Hot Plug capability. Disabled: Hot Plug is not available on this port.

5.1.2.5.10 Remote Access Configuration

Feature	Options	Description
Console Redirection Jumper	Display only.	Display the hardware state of the Remote access jumper. The jumper can overwrite the CMOS setting to enable the console redirection.
Remote Access	Disabled Enabled	Select Remote Access Type
Serial Port number	ICH COM1 ICH COM2	Select Serial Port for console redirection Make sure the selected port is enabled
Serial Port Mode	115200 8,n,1 57600 8,n,1 38400 8,n,1 19200 8,n,1 09600 8,n,1	Select Serial Port settings.
Flow Control	None Hardware Software	Select Flow Control for console redirection.
Redirection After BIOS POST	Disabled Boot Loader Always	Disable: Turns off the redirection after POST Boot Loader: Redirection is active during POST ans during Boot Loader. Always: Redirection is always active. (Some OSs may not work if set to Always)
Terminal Type	ANSI VT100 VT-UTF8	Select the target terminal type
VT-UTF8 Combo Key Support	Disabled Enabled	Enable VT-UTF8 combination key Support for ANSI/VT100 terminals.

5.1.2.5.11 IPMI Configuration

Feature	Options	Description
Status of IPMC	Display only	Indicate the status of IPMI SMM KCS interface, this is not a self-test results.
IPMI Device and Firmware Information	This is a Sub-Menu	View IPMI Device and Firmware Information
FRU Board Information	This is a Sub-Menu	View FRU Board Information
KCS-SMS IRQ	IRQ10 IRQ11 Disabled	Select Management Controller IRQ for the System Management Software (SMS).
BIOS Watchdog Timer Action	No Action Reset System Power Cycle	Allows the IPMC to reset or power down the system if the BIOS/POST crashes or hags. Note: if this happens the IPMC will also switch to the other BIOS Flash image.
Disable BIOS Watchdog Timer		The IPMC will reset the system if you stay in the Setup for mopre than the allocated period of time (5 minutes). Use this feature to disable the Timer for this setup session only.
OS Load Watchdog Timer Action	Disabled Reset System Power Down Power Cycle	Allows the IPMC to reset or power down the system it the operating system crashes or hangs.
IPMC Watch Dog Time Out	5 min 1 min 10 Sec 30 Sec	Amount of time for IPMC to wait before assuming the system has crashed and needs to be reset.

5.1.2.5.11.1 IPMI Device and Firmware Information

Feature	Options	Description
Product ID	00005002 (example)	Displays only.
IPMI Version	1.5 (example)	Displays only.
Device ID	04 (example)	Displays only.
Device Revision	00 (example)	Displays only.
Firmware Revision	04.15 (example)	Displays only.
SDR Revision	08 (example)	Displays only.
FWUM Firmware Revision	01.03(example)	Display only.

5.1.2.5.11.2 FRU Board Information

Feature	Options	Description
Board Product name	AT8001 (example)	Displays only.
Board Serial Number	1000581102 (example)	Displays only.
Board Part number	AT8001######_1-000(example)	Displays only.
Product Name	AT8001 (example)	Displays only.
Product Part/Model	AT8001######_1-000 (example)	Displays only.
Product Version number	00(example)	Displays only.
Product Serial Number	1000581102 (example)	Display only.

5.1.2.5.12 USB Configuration

Feature	Options	Description
USB Function	Disabled 2 USB Ports All USB Ports	Enables USB Host controllers.
Legacy USB Support	Disabled Enabled Auto	Enables Support for legacy USB. Auto option disables legacy support if no USB device are connected
USB 2.0 Controller	Enabled Disabled	Enables the USB 2.0 controller
USB 2.0 Controller Mode	FullSpeed HiSpeed	Configure the USB 2.0 Controller in HiSpeed (480Mbps) or FullSpeed (12Mbps)
BIOS EHCI Hand-Off	Disabled Enabled	This is a workaround for OSes without EHCI hand-off support. The EHCI ownership change should claim by EHCI driver.
USB Mass Storage Device Configuration	This is a Sub-Menu	Configure the USB Mass Storage Class Devices.

5.1.2.5.12.1 USB Mass Storage Device Configuration

Feature	Options	Description
USB Mass Storage Reset Delay	10 Sec 20 sec 30 sec 40 Sec	Number of seconds POST waits for the USB mass storage device after start unit command.
Device #1-6		Mass Storage Device identification
Emulation Type (for each devices)	Auto Floppy Forced FDD Hard Disk CDROM	If Auto, USB devices less than 530MB will be emulated as Floppy and remaining as hard drive. Forced FDD option can be used to force a HDD formatted drive to boot as FDD (Ex. ZIP drive).

5.1.2.6 PCIPnP

Feature	Options	Description
Clear NVRAM	No Yes	Clear NVRAM during System.
PCI Latency Timer	32 64 93 128 160 192 22 248	Value in units of PCI clocks for PCI device latency timer register.
Allocate IRQ to PCI VGA	Yes No	Yes: Assings IRQ to PCI VGA card if card requests IRQ No: Does not assign IRQ to PCI VGA card even if card requests an IRQ.

5.1.2.7 Boot menu

Feature	Options	Description
Boot Setting Configuration	This is a sub-menu	Configure Settings during System Boot.
Boot Device Priority	This is a sub-menu	Specifies the Boot Device Priority sequence.
Hard Disk Drives	This is a sub-menu	Specifies the Boot Device Priority sequence from available Hard Drives.
Removable Drives	This is a sub-menu	Specifies the Boot Device Priority sequence from available Removable Drives.
CD/DVD Drives	This is a sub-menu	Specifies the Boot Device Priority sequence from available CD/DVD Drives.

5.1.2.7.1 Boot Settings Configuration

Feature	Options	Description
Quick Boot	Disabled Enabled	Allows BIOS to skip certain tests while booting. Ths system Configure Summary will be skipped. This will decrease the time needed to boot the system.
Quiet Boot	Disabled Enabled	Disabled: Display normal PORT messages. Enabled Disaplay OEM Logo instead of POST messages.
Add-On ROM Display Mode	Force BIOS Keep Current	Set display mode for Option ROM
Bootup Num-Lock	On Off	Select Power-on state for Num-Lock
PS/2 Mouse Support	Disabled Enabled Auto	Select support for PS/2 Mouse.
Wait For F1 If error	Disabled Enabled	Wait for F1 key to be pressed if error occurs
Hit DEL Message Display	Disabled Enabled	Display "Press DEL to run Setup" in POST.
Interrupt 19 Capture	Disabled Enabled	Allows option ROMs to trap interrupts 19. This is required by some PCI cards that provide a ROM based setup utility.
Retry Boot Sequence	Disabled Enabled	Enable this option to retry the Boot Sequence (infinite retries)
Save CMOS in FLASH	Disabled Enabled	Saving CMOS memory content into Flash Memory will prevent loosing CMOS options when Battery fails.

5.1.2.7.2 Boot Device Priority

Feature	Options	Description
1st Boot Device	Varies	Specifies the boot sequence from the available devices. A device enclosed in parenthesis has been disabled in the corresponding type menu.
Nth Boot Device	Varies	Number of entries will vary based on system configuration.

Note: The easiest way to select the desired priority is to select the 1st Boot Device, Hit Enter and choose a device from the options presented. Repeat this process for 2nd to Nth Boot Devices.

5.1.2.7.3 Hard Disk Drives

Feature	Options	Description
1st Drive	Varies	Specifies the boot sequence from the available devices.
Nth Drive	Varies	Number of entries will vary based on system configuration.

Note: The easiest way to select the desired priority is to select the 1st Drive, Hit Enter and choose a device from the options presented. Repeat this process for 2nd to Nth Drives.

5.1.2.7.4 Removable Drives

Feature	Options	Description
1st Drive	Varies	Specifies the boot sequence from the available devices.
Nth Drive	Varies	Number of entries will vary based on system configuration.

Note: The easiest way to select the desired priority is to select the 1st Drive, Hit Enter and choose a device from the options presented. Repeat this process for 2nd to Nth Drives.

5.1.2.7.5 CD/DVD Drives

Feature	Options	Description
1st Drive	Varies	Specifies the boot sequence from the available devices.
Nth Drive	Varies	Number of entries will vary based on system configuration.

Note: The easiest way to select the desired priority is to select the 1st Drive, Hit Enter and choose a device from the options presented. Repeat this process for 2nd to Nth Drives.

5.1.2.8 Security

Feature	Options	Description
Change Supervisor Password		Install or change the password.
Change User Password		Install or change the password.
Boot Sector Virus Protection	Disabled Enabled	Enable/Disable Boot Sector Virus Protection.

5.1.2.9 Chipset

Feature	Options	Description
NorthBridge Configuration	This is a sub-menu	Options for NB
Spread Spectrum Clocking Mode	Enabled Disabled	Allows BIOS to Set Clock Spread Spectrum for EMI Control

5.1.2.9.1 NorthBridge Configuration

Feature	Options	Description
Memory Remap Feature	Disabled Enabled	ENABLE: Allow remapping of overlapped PCI memory above the total physical memory. DISABLE: Do not allow remapping of memory.
Memory Mirroring/Sparing	Disabled Mirroring Sparing	Enable Memory RAS Feature: Mirroring or Sparing. Options available only if memory configuration supports Mirroring or Sparing.
DMA Controller	Disabled Enabled	Enable/Disable DMA Controller

5.1.2.10 Exit

Feature	Options	Description
Save Changes and Exit		Exit system dsetup after saving the changes. F10 key can be used for this operation.
Discard Changes and Exit		Exit system setup without saving any changes. ESC key can be used for this operation.
Discard Changes		Discard Changes done so far to nay of the setup questions. F7 key can be used for this operation.
Load Optimal Defaults		Load Optimals Default values for all the setup questions. F9 key can be used for this operation.
Load Failsafe Defaults		Load Failsafe Default values for all the setup questions. F8 key can be used for this operation.

5.2 Boot Utilities

AMI Boot Utilities are: Boot Menu POP-UP

Boot Menu POP-UP is a boot screen that displays a selection of boot devices from which you can boot your operating system.

5.2.1 Pressing <Del> (or <F4> from a Console Redirection terminal)

Pressing < Del > (or <F4> from a Console Redirection terminal) during POST enters Setup.

5.2.2 Pressing <F11> (or <F3> from a Console Redirection terminal)

Pressing <F11> (or <F3> from a Console Redirection terminal) displays the Boot Menu POP-UP with these options:

1. Load the operating system from a boot device of your choice.
2. Exit the Boot Menu POP-UP (with <ESC>) and load the operating system from the boot devices in the order specified in Setup.

5.2.3 BOOT Menu POP-UP

The BOOT Menu POP-UP expands your boot options by letting you choose your boot device, which could be a hard disk, floppy disk, CDROM, Flash Disk, SCSI or LAN. You can select your boot device in Setup, or you can choose a different device each time you boot during POST by selecting your boot device in t**he Boot device** <F11> (or <F3> from a Console Redirection terminal**)**.

5.3 Console Redirection (VT100 Mode)

The VT100 operating mode allows remote setup of the board. This configuration requires a remote terminal that must be connected to the board through a serial communication link.

5.3.1 Requirements

The terminal should emulate a VT100 or an ANSI terminal. Terminal emulation programs such as Telix©, HyperTherminal(Windows), minicom(Linux) or ProComm©(Windows) can also be used.

5.3.2 Setting Up and Configuring

To set up the VT100 mode:

1. Connect a monitor and a keyboard to your board and turn on the power.
2. Enter into the CMOS Setup program in the "Advanced" page, "Remote Acces Configuration" menu.
3. Select the VT100 mode and the appropriate COM port and save your setup.
4. Connect the communications cable.



Note:
If you do not require a full cable for your terminal, you can set up a partial cable by using only the TXD and RXD lines. To ignore control lines, loop them back as shown in VT100 Partial Setup cable diagram.

5. Configure your terminal to communicate using the same parameters as in CMOS Setup.



Bios Settings:
- Advanced → Remote Access Configuration

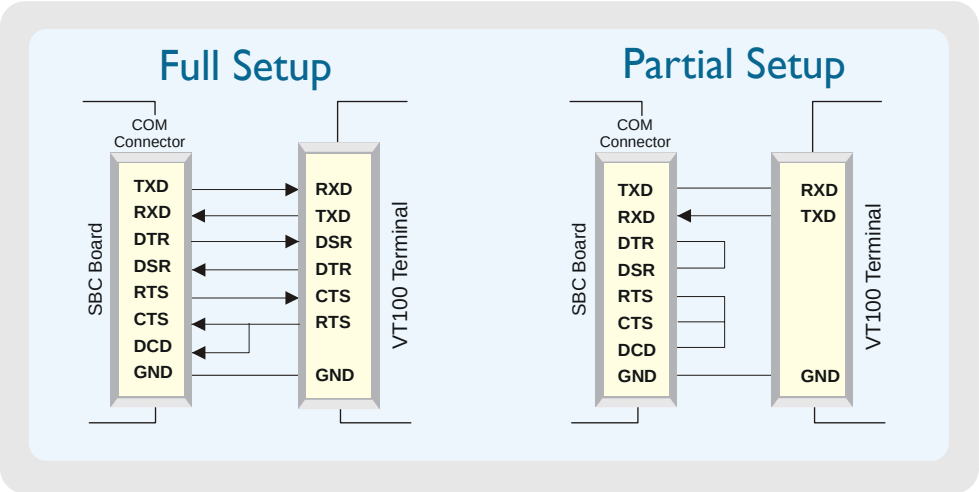
6. Install the Console Redirection jumper (will force VT100 enabled regardless of Setup option). Reboot the board.
7. Use the remote keyboard and display to set up the BIOS.
8. Save the setup, exit, and disconnect the remote computer from the board to operate in stand-alone configuration.

Console Redirection is done by refreshing the video address @ B8000h at the selected baud rate. This means that a low baud rate refreshes the screen slowly, but the CPU time is maximized for the applications. A high baud rate refreshes the screen rapidly, but the display frequently interrupts the serial port.

Console Redirection provided by AMI based BIOS can reset the target system using the sequence “Ctrl Shift –“.

5.3.3 Running Without a Terminal

The board can boot up without a screen or terminal attached. If the speed is set to Auto and no terminal is connected, the speed is set to 115,200 bauds.
You can run without a console by not enabling VT100 Mode and by disabling the onboard video.



Note:
Refer to “Serial Port 1 (J5)” section for connector location and pinout.

5.3.4 ANSI and VT100 Keystroke Mapping

Up	<ESC>[A
Down	<ESC>[B
Right	<ESC>[C
Left	<ESC>[D
Home	<ESC>[H
End	<ESC>[K
F1	<ESC>OP
F2	<ESC>OQ
F3	<ESC>OR
F4	<ESC>OT

5.3.5 VT-UTF8 Keystroke Mapping

The following “escape sequences” are defined in the “Conventions for Keys Not in VT100 Terminal Definition and ASCII Character Set” section of “Standardizing Out-of-Band Management Console Output and Terminal Emulation (VT-UTF8 and VT100+)”,available for download at microsoft.com.

F1 Key	<ESC>1
F2 Key	<ESC>2
F3 Key	<ESC>3
F4 Key	<ESC>4
F5 Key	<ESC>5
F6 Key	<ESC>6

F7 Key	<ESC>7
F8 Key	<ESC>8
F9 Key	<ESC>9
F10 Key	<ESC>0
F11 Key	<ESC>!
F12 Key	<ESC>@

Alt Modifier<ESC>^A	
Control Modifier	<ESC>^C
Home Key	<ESC>h
End Key	<ESC>k
Insert Key	<ESC>+
Delete Key	<ESC>-
Page Up Key	<ESC>?
Page Down Key	<ESC>/

These “escape sequences” are supported by VT-UTF8 compliant terminal connections, such as Windows Server 2003 Emergency Management Services (EMS).

AMIBIOS8 Serial Redirection supports these key sequences under two configurations:

- “Terminal Type” setup question is set to “VT-UTF8”
- “Terminal Type” setup question is set to “VT100” or “ANSI” and “VTUTF8 Combo Key Support” setup question is set to “Enabled”

5.4 Installing Drivers

5.4.1 Video Drivers

Various drivers are provided for different operating systems and software. To install a driver, refer to the Setup program located on the CD-ROM (provided with your board).

5.4.2 Fibre Channels

Various drivers are provided for different operating systems and software. To install a driver, use the Setup program located on the CD-ROM (provided with your board).

5.4.3 Ethernet Drivers

Various drivers are provided for different operating systems and software. To install a driver, use the Setup program located on the CD-ROM (provided with your board).

5.4.4 Other Drivers

For other operating system drivers and installation instructions or for more information, visit our Web site at www.kontron.com or our FTP site at ftp.kontron.ca/support/ or you may also contact Kontron's Technical Support department.

5.5 MontaVista

5.5.1 Introduction

This “how-to” explains the configuration and usage of the MontaVista CGE AT8001 LSP. The LSP include a custom kernel that support the AT8001 hardware, contain tools to update the BIOS, the IPMI firmware and access the IPMI controller. It does also include some useful scripts for hardware configuration.

5.5.2 Installation

Before installing the LSP, make sure that target x86_pentium4 and cross x86_pentium4 disks from MontaVista CGE 3.1 are installed. This is because the LSP do not include standard x86_pentium4 binary packages. See MontaVista CGE 3.1 user guide for installation process.

Installation has to be done in ROOT administrator only.

5.5.2.1 Automatic

Extract the LSP archive to a new directory:
gzip –dc {filename} | tar –xvf -

type *./setup.sh* in the directory where the LSP is extracted.

When prompted, enter the directory where MontaVista CGE 3.1 is installed
(Default: */opt/montavista*).

Wait until “INSTALLATION COMPLETED!” is displayed.

5.5.2.2 Manual

Extract the LSP archive to a new directory:
gzip –dc {filename} | tar –xvf -

Install the LSP:
mvl-rpm –ihv PATH_TO_LSP/cross-x86_pentium4-lsp-kotron_t5002-2.4.20_mvlcge31-041203.noarch.mvl

Install the Kontron Support Toolkit package:
mvl-rpm --target=x86_pentium4-linux –ihv PATH_TO_LSP/kst-0.1-041203.x86_pentium4.mvl

5.5.3 Configuration

Create a project using the LSP:

Open the Target Configuration Tool and click on the *New Project* button.

Enter your project name, project directory and your project summary.

Select Kontron T5002 x86 PC Target as your LSP.

Make sure *Use Custom Kernel* is selected.

Press the *Create* Button and now you should have all you need to build an image for the AT8001.

Adding Kontron Support Toolkit in your MontaVista CGE 3.1 image:

In the Target Configuration Tool select *View -> Package selector* from the menu (if the *View* menu is disabled, you need to create or open a configuration file by selecting *File -> New config... / Open config...*).

Select the *base* category, and if the installation was correctly done, there should be a new package named "kontron_toolkit" available in the package list.



Note:
The Kontron support toolkit package is subdivided in three categories. The base category (needed for the complete shutdown script), The IPMI category (needed for IPMI firmware update and IPMI accessibility) and BIOS (needed for updating the bios flash device).

5.5.4 Building the image

If you don't want to select package one by one, there is a file named *default.cfg* included with the LSP that is an example of configuration for the image. Just put it in the project directory and select it with *File -> Open Config...*

Select *File -> Build Target* to build the custom kernel and to generate *fsimage.tar* in your project directory that will include the kernel, the Kontron support toolkit and all selected packages.



WARNING
This image WILL NOT contain configurations for Kontron specific hardware. There is a file named "*conf.tar*" in the LSP archive that include configuration file for automatic drivers loading and support for the complete shutdown of the board.



5.5.5 Configuration Scripts

The LSP include *conf.tar* which is an archive of some scripts to configure at boot time, the Gigabit Ethernet port, Fiber channel (SCSI and LAN) and IPMI Controller.

What "*conf.tar*" contain:

/etc/init.d/halt	Modified halt scripts to add support for a complete board shutdown.
/etc/init.d/bootmisc.sh	Create two symbolic device links (for ipmifwu and ipmitool).
/etc/modules	Drivers initialization and configuration.

The *halt* script add direct access to ACPI in the shutdown process (with the help of *PORT* and *PCITWEAK* tools) to have support for a complete shutdown of the board.

To use these scripts, just extract this archive from the root directory of the generated MontaVista image.

Appendix

Contents

A - Memory & I/O Maps A-1

B - Kontron Extension Registers B-1

C – Connector Pinouts C-1

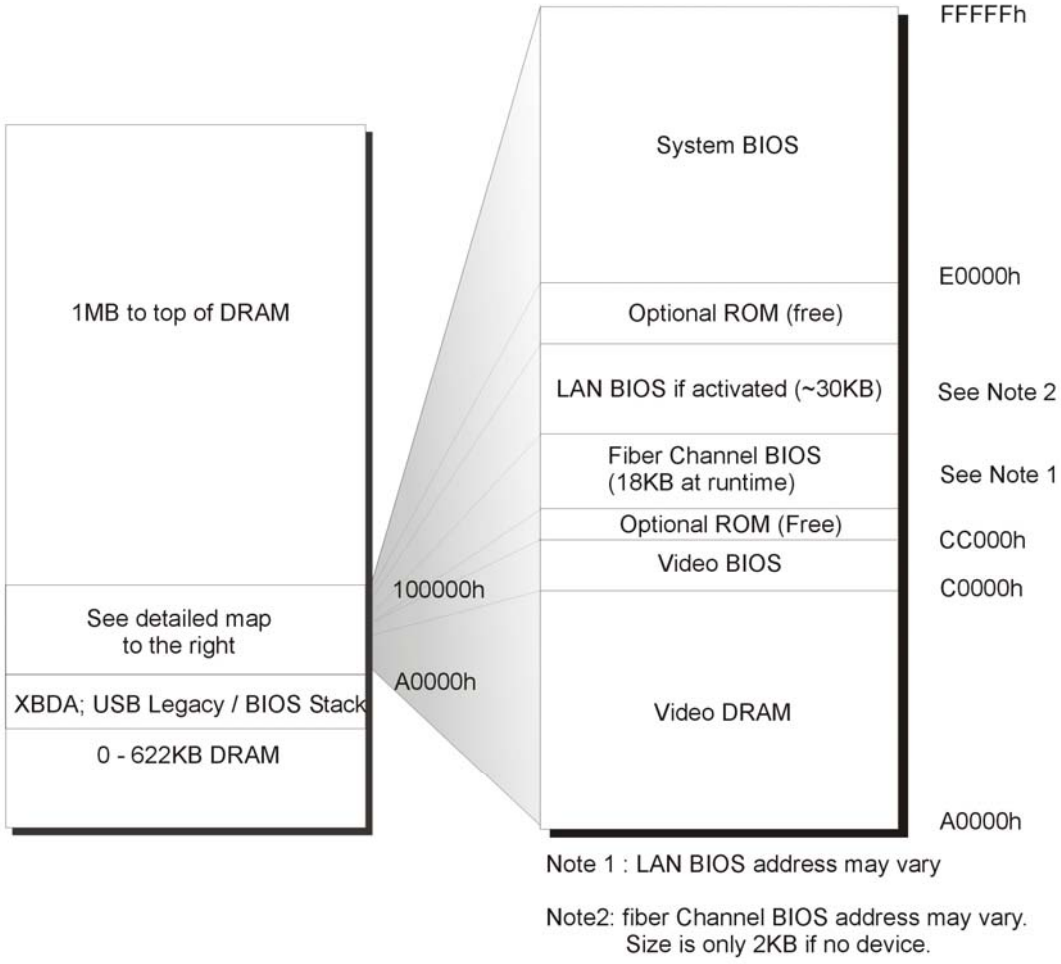
D – BIOS Setup Error Codes..... D-1

E – Software Update..... E-1

F – Getting Help F-1

A. Memory & I/O Maps

A.1 MEMORY MAPPING



Address	Function
00000-9B7FF	0-622 KB DRAM
9B800-9FFFF	622KB – 640 KB XBDA; USB Legacy / BIOS Stack
A0000-BFFFF	Video DRAM
C0000-CBFFF	Video BIOS
CC000-DBFFF	Optional ROM (Free) LAN BIOS around 30KB if activated, address may vary External Fiber Channel BIOS 18KB-64KB , address may vary
E0000-FFFFF	System BIOS
100000-PCI Memory	DRAM available

A.2 I/O MAPPING

Address	Optional Address	Function
000-01F		DMA Controller 1
020-03F		Interrupt Controller 1
040-05F		Timer
060-06F		Keyboard
070-07F		Real-time clock
080-09F		DMA Page Register
0A0-0BF		Interrupt Controller 2
0C0-0DF		DMA Controller 2
0F0-0F1, 0F8-0FF		Math Coprocessor
1F0-1F7, 3F6		Primary IDE
170-177, 376		Secondary IDE
3F0-3F7		Floppy Disk
3F8-3FF (COM1)	2F8-2FF (COM2)	Serial Port 1 (COM1 by default)
2F8-2FF (COM2)	3F8-3FF (COM1)	Serial Port 2 (COM2 by default)
400-9FF		Chipset Reserved
A00-A1F		Kontron Registers (on-board)
A20-A2F		Kontron Registers (RTM)
B00-0FFF		Chipset Reserved

A.3 PCI IDSEL and Device numbers

ID SEL#	BUS #	DEV #	V. ID	D. ID	Funct. #	Description	PCI Description
	0	0	8086h	3590h	0	E7520 – Memory Controller Hub	Bridge, host-bridge, multi-function
	0	1	8086h	3591h	0	E7520 – Memory Error Reporting	Bridge, host-bridge, multi-function
	0	1	8086h	3594h	0	E7520 – DMA Controller	System peripheral, non-specific, single-function
	0	2	8086h	3595h	0	E7520 – Host-to-PCI Express A Bridge (x8 or x4)	Bridge, PCI-to-PCI, single-function, type 1 header
	0	3	8086h	3596h	0	E7520 – Host-to-PCI Express A1 Bridge (x4 only)	Bridge, PCI-to-PCI, single-function, type 1 header
	0	4	8086h	3597h	0	E7520 – Host-to-PCI Express B Bridge (x8 or x4) – (Support Hot-Plug)	Bridge, PCI-to-PCI, single-function, type 1 header
	0	5	8086h	3598h	0	E7520 – Host-to-PCI Express B1 Bridge (x4 only)	Bridge, PCI-to-PCI, single-function, type 1 header
	0	6	8086h	3599h	0	E7520 – Host-to-PCI Express C Bridge (x8 or x4) – (Support Hot-Plug)	Bridge, PCI-to-PCI, single-function, type 1 header
	0	7	8086h	359Ah	0	E7520 – Host-to-PCI Express C1 Bridge (x4 only)	Bridge, PCI-to-PCI, single-function, type 1 header
	0	7	8086h	359Bh	0	E7520 – Extended Configuration Registers	???
	0	28	8086h	25Aeh	0	i6300ESB ICH – HUB Interface to PCI-X Bridge	
	0	29	8086h	25A9h	0	i6300ESB ICH – USB UHCI Controller #1	
	0	29	8086h	25Aah	1	i6300ESB ICH – USB UHCI Controller #2	
	0	29	8086h	25Abh	4	i6300ESB ICH – Watchdog Controller	
	0	29	8086h	25Ach	5	i6300ESB ICH – IOAPIC bus B	
	0	29	8086h	25Adh	7	i6300ESB ICH – USB EHCI Controller	
	0	30	8086h	25A1h	0	i6300ESB ICH – HUB Interface to PCI Bridge	
	0	31	8086h	25A2h	0	i6300ESB ICH – LPC Interface	
	0	31	8086h	25A1h	1	i6300ESB ICH – IDE Controller	
	0	31	8086h	25A3h	2	i6300ESB ICH – Serial-ATA Controller	
	0	31	8086h	25A4h	3	i6300ESB ICH – SMBus Controller	
AD16	1	0	1002h	4C52h	0	ATI Mobility	
AD17	1	1	8086h	1229h	0	i82551er	

	2	0	8086h	0329h	0	i6700PXH – PCI-Express to PCI Bridge (P2P-A)
	2	0	8086h	0326h	1	i6700PXH – I/OxAPIC-A
	2	0	8086h	032Ah	2	i6700PXH – PCI-Express to PCI Bridge (P2P-B)
	2	0	8086h	0327h	3	i6700PXH – I/OxAPIC-B
AD17	3	1	8086h	1079h	0	I82546GB
AD17	3	1	8086h	1079h	1	I82546GB
AD18	3	2	8086h	1079h	0	I82546GB
AD18	3	2	8086h	1079h	1	I82546GB
AD17	4	1	1000h	0626h	0	LSIF929X
AD17	4	1	1000h	0626h	1	LSIF929X
AD17	5 *	1	----	----	----	PMC
?	6 *	0	?	?	?	AMC – B1
?	7 *	0	?	?	?	AMC – B0

B. Kontron Extension Registers

B.1 FPGA/CPLD REGISTERS DEFINITION

Unused bits are reserved. To insure compatibility with other product and upgrades to this product, do not modify unused bits. Bits marked NU are not used on this board. Writing to such bit does nothing and reading is undefined, either 0 or 1 may be returned.

Legend:

Symbol		Signification
U	=	Unchanged (stay unchanged after reset)
X	=	Not Defined (bit not used on this board)
NU	=	Not Used

B.2 OVERVIEW

FPGA/CPLD registers

Address	Content
80h	*POST code*
81h	*Extended POST code (16-bit write only)*
A00h	*FPGA version*
A01h	*Debug LED control*
A02h	*FWUM control (for manufacturing / update use)*
A03h	*Reserved*
A04h	*Development Features (for development only)*
A05-A07h	*Reserved*
A08h	**TelcoClock option register 0: configuration*
A09h	**TelcoClock option register 1: configuration*
A0Ah	**TelcoClock option register 2: configuration & status*
A0Bh	**TelcoClock option register 3: configuration*
A0Ch	**TelcoClock option register 4: reset and test modes*
A0Dh	**TelcoClock option register 5: PLD version*
A0Eh	**TelcoClock option register 6: Alarms*
A0Fh	**TelcoClock option register 7: Interrupt number*
A10-A1Fh	*Reserved*

* Those registers depend on a manufacturing option..

B.3 0080H: POSTCODES

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0x080	READ	Postcode							
	WRITE	Postcode							
	Reset	00h							

Postcode — Postcodes are captured in this register as they are written.

B.4 0081H: EXTENDED POSTCODES

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0x081	READ	Postcode							
	WRITE	Postcode							
	Reset	00h							

Postcode — Postcodes are captured in this register as they are written. Be carefull that postcodes are not always 16-bit and the high byte in register 81h could be unrelated to the content of register 80h. Also, only 16-bit write to I/O 80h will write to I/O 81h. An 8-bit write to I/O 81h is ignored.

B.5 0A00H: FPGA VERSION

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0xA00	READ	Reserved				Version			
	WRITE	Reserved				*NU*	*NU*	*NU*	*NU*
	Reset	Reserved				Version			

Version — FPGA programmable logic version.

B.6 0A01H: DEBUG LED

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0xA01	READ	MfgFlag	RJ45	EnHD	EnPost	EnClk	Green0	Anber0	Red0
	WRITE	MfgFlag	RJ45	EnHD	EnPost	EnClk	Green0	Anber0	Red0
	Reset	0/NA	1	0	1	0	0	0	0

EnHD — Setting this bit will use led Amber0 to display hard disk activity (PATA & SATA)

EnPost — Enable usage of the debug LED to display the last post code of the boot. The BIOS clear this bit prior to operating system lauch.

EnClk — Enable TelcoClock monitoring on debug LED. Make sure EnHD and EnPost are cleared. When green: both clocks are present. When amber: only one clock is present. When red, no clock are present or the TelcoClock PLD is not initialized. This is a debug mode.

Reg0/ Amber0/ Green0 — Debug LED 0. Can be use as a debug LED or to display post code (default during boot) or hard disk activity (default following boot) or as an end-user status/debug LED.

RJ45 — This bit tels the FPGA wich LEDs should reflect LAN activity; RJ45 LEDs or grouped LEDs. The BIOS should set this bit as soon as possible to reflect the configuration of the fabric LAN. 0: if the LAN goes to the fabric or 1 if the LAN goes to the front-plate RJ45s.

MfgFlag — A memory element used by the BIOS and test software in manufacturing.
Note that this bit is cleared on a power-up but is not affected by a reset

About the debug LED: The idea is that the LED will light amber/green when in reset (this is hardware). As soon as the FPGA is programmed, the LED lights amber and is enabled for post-code display (see bellow). If the BIOS fail, it is possible to read the post-code. If the BIOS succeed, it will disable the post-code and enable HD activity on the green LED. If needed, the application software can then disable hard disk activity reporting and directly control the bi-color LED for status reporting.

How to read the 8-bit post-code:

- Both color: start of post sequence
- Amber blink: This is the high nibble. 0 to 15 blinks represent hexadecimal 0 to F.
- Green blink: This is the low nibble. 0 to 15 blinks represent hexadecimal 0 to F.

B.7 0A02H: FWUM

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0xA02	READ	*NU*	*NU*	Status	DoProg	RollBack	UART	MODE	RESET
	WRITE	*NU*	*NU*	*NU*	DoProg	RollBack	UART	MODE	RESET
	Reset	*X*	*X*	*X*	0	0	0	1	0

RESET	FWUM reset. This power-up state of this bit will be 0 under normal operating conditions. When the manufacturing jig is present or jumper0 (force-on) is present, the power-up state will be '1' (FWUM in reset).
MODE	FWUM mode pin.
UART	Set this bit to connect UART1 to the FWUM for programmation.
RollBack	Set to 1 for manual rollback (in conjunction with DoProg) Leave to 0 for normal operation
DoProg	Set to 1 then to 0 to start programming the IpmC with the new code.
Status	1 : FWUM Ready 0 : FWUM Busy

B.8 0A04H: DEVELOPMENT FEATURES

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0xA04	READ	MinorVersion				*NU*	PCB	SSC1	SSC0
	WRITE	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*	SSC1	SSC0
	Reset	MinorVersion				*X*	PCB	1	1

MinorVersion	Minor version that doesn't impact the IPMC. For in-house minor version tracking.
SSC0	Special Serial Connection bit 0
SSC1	Special Serial Connection bit 1
PCB	PCB Version. Should be "1" for production stable boards.

Those bits define special connections between serial devices that are meaningless to the end user. They are development and/or manufacturing facilities. Leave those bits in their default state for end-user operation.

SSC[1:0]	Effect
11	Normal operation (no development tricks).
01	Float FW_RXD pin. Use this to program the FWUM with the POD.
10	Connect FW_RXD and FW_TXD to RJ45 RS232 port
00	Connect B1 (IPMC uart 1) to ICH UART1

B.9 0A08H: TELCLOCK0 (TELECOM CLOCK OPTION)

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0xA08	READ	HWMODE	HO_LOS	MS2	MS1	REFALIGN	FCS	E3DS3	E3DS3OC3
	WRITE	HWMODE	HO_LOS	MS2	MS1	REFALIGN	FCS	E3DS3	E3DS3OC3
	Reset	0	0	0	0	0	0	0	0

HWMODE — Enable automatic switching by hardware.

HO_LOS — Switch criteria in HW mode.

When set, use PLL holdover detection as the switch criteria.

When cleared, use loss of clock (internal to PLD) as the switch criteria.

MS2/MS1 — PLL Mode selection:

MS[2..1] = 00: normal operation

MS[2..1] = 01: holdover mode

MS[2..1] = 10: free-run mode

MS[2..1] = 11: reserved

REFALIGN — Reference clock phase alignment. Changing this bit from 0 to 1 starts the alignement.

FCS — Filter characteristic s of the PLL.

0: 12Hz filter without phase slope limitation

1: 6Hz filter with phase slope limited to 41ns per 1.326ms.

E3DS3/ E3DS3OC3 — These bits select the transmission clock frequency, when TXREFx_SEL[2..0]=111 in register TelClock3.
E3DS3OC3 = 0, E3DS3 = 1: 8.592MHz
E3DS3OC3 = 0, E3DS3 = 0: 11.184MHz
E3DS3OC3 = 1, E3DS3 = 1: 34.368MHz
E3DS3OC3 = 1, E3DS3 = 0: 44.736MHz

B.10 0A09H: TELCLOCK1 (TELECOM CLOCK OPTION)

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0xA09	READ	RSV1	RSV0	SELCLK3B	SELCLK3A	REFSEL	8K_16M	SEL_REFFRQ	SEL_RDNCLK
	WRITE	*NU*	*NU*	SELCLK3B	SELCLK3A	*NU*	8K_16M	SEL_REFFRQ	SEL_RDNCLK
	Reset	*X*	*X*	0	0	X	0	0	0

SELCLK3B — Select clock to send to backplane CLK3B:
0=from first AMC (AMC B1, CLKC), 1=from second AMC (AMC B2, CLKC).

SELCLK3A — Select clock to send to backplane CLK3A
0=from first AMC (AMC B1, CLKC), 1=from second AMC (AMC B2, CLKC).

8K_16M — This bit is valid only when the transmission clock is selected by setting TXREFx_SEL[2..0]=101 in TelClock3 register. Setting this bit select the transmission clock frequency as 16.384 MHz, while clearing it select 8.0kHz.

SEL_REFFRQ — Select reference frequency (8k or 19.44M): 0 = 8kHz, 1=19.44MHz.
This bit controls the multiplexer that feeds clocks to the PLL.
0: PLL input clocks = CLK1A & CLK1B (8kHz per ATCA spec)
1: PLL input clocks = CLK2A & CLK2B (19.44MHz per ATCA spec)

SEL_RDNCLK — Setting this bit selects the secondary redundant reference clock, while clearing it selects the primary redundant reference clock. This bit is for a software (manual) switching.
Also known as "SEL" in Siemens code and in some part of the documentation.

REFSEL	Show the reference that is currently selected. 0: Primary reference 1: Secondary reference
RSV1/ RSV0	Reserved.

B.11 0A0AH: TELCLOCK2 (TELECOM CLOCK OPTION)

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0xA0A	READ	PRI_LOS	SEC_LOS	HOLDOVER	UNLOCK	*NU*	DRVCLKA1	*NU*	DRVCLKA0
	WRITE	*NU*	*NU*	*NU*	*NU*	*NU*	DRVCLKA1	*NU*	DRVCLKA0
	Reset	X	X	X	X	X	0	X	0

PRI_LOS	Loss of primary reference clock detected. This bit is high when the primary clock at the input of the PLL (i.e. after PLD mux) is loss.
SEC_LOS	Loss of secondary reference clock detected. This bit is high when the primary clock at the input of the PLL (i.e. after PLD mux) is loss.
HOLDOVER	Hold over detected by the PLL.
UNLOCK	Unlock detected by the PLL.
DRVCLKA1	Drive transmission clock CLKA for AMC-B2 This bit is forced to 0 when AMC-B2 is absent or unpowered.
DRVCLKA0	Drive transmission clock CLKA for AMC-B1 This bit is forced to 0 when AMC-B2 is absent or unpowered.

B.12 0A0BH: TELCLOCK3 (TELECOM CLOCK OPTION)

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0xA0B	READ	DRVCLK3B	DRVCLK3A	TXREF1_SEL[2..0]				TXREF0_SEL[2..0]	
	WRITE	DRVCLK3B	DRVCLK3A	TXREF1_SEL[2..0]				TXREF0_SEL[2..0]	
	Reset	0	0	000				000	

DRVCLK3B — Enable MLVDS buffer to drive CLK3B to the backplane
This bit is forced to 0 until the IPMC authorizes it.

DRVCLK3A — Enable MLVDS buffer to drive CLK3A to the backplane
This bit is forced to 0 until the IPMC authorizes it.

TXREF1_SEL[2..0] — Transmission reference clock for AMC-B2 selection (see table below).

TXREF0_SEL[2..0] — Transmission reference clock for AMC-B1 selection (see table below).

The transmission frequency is selected according to the following table.

TXREFx_SEL[2..0]	Transmission Clock Frequency
000	1.544 MHz (for T1/J1)
001	2.048 MHz (for E1)
010	4.096 MHz (for E1)
011	6.312 MHz (for J2)
100	8.192 MHz (for E1)
101	8 kHz/16.384 MHz* (for E1/T1/J1/J2)
110	19.44 MHz (for OC3, 12/STM-1, 4)
111	34.368/44.736MHz**(for E3/T3) or 8.592/11.184MHz

* 8kHz or 16 MHz can be selected by bit 8K_16M in TelClock1 register.

** One frequency can be selected by bits E3DS3 and E3DS3OC3 in TelClock0 register.

B.13 0A0CH: TELCLOCK4 (TELECOM CLOCK OPTION)

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0xA0C	READ	*NU*	*NU*	*NU*	*NU*	*NU*	IRQTST	RESET	TEST
	WRITE	*NU*	*NU*	*NU*	*NU*	*NU*	IRQTST	RESET	TEST
	Reset	*X*	*X*	*X*	*X*	*X*	0	1	0

IRQTST — Interrupt test. The state of this bit is ored with the real interrupt. This bit is for software testing. Ignore in normal operation. A "1" assert the interrupt request.

TEST — Ignore IPMC & shelf manager authorization.

Use this bit for testing only. In normal operation, leave this bit to 0 otherwise the AT8001 will not be compliant with the ATCA specification.

RESET — Hardware reset of the PLL.

B.14 0A0DH: TELCLOCK5 (TELECOM CLOCK OPTION)

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0xA0D	READ	PCB				Version			
	WRITE	*NU*				*NU*			
	Reset	PCB				Version			

PCB — Set to 1. Indicate that the compilation switch was properly set in the source code and that the PLD is compiled for PCB revision 1. Prior "non-test" version of this PLD had this bit cleared. Should be "1" for production boards.

VERSION — PLD code version.

Note that a value of:

PCB&Version = FF: indicate a test PLD to make a clock generator

PCB&Version = FE: indicate a test PLD used during manufacturing tests

B.15 0AOEH: TELCLOCK6 (TELECOM CLOCK OPTION)

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0xA0E	READ	UNLOCK10	UNLOCK01	HLDOVR10	HLDOVR01	SEC10	SEC01	PRI10	PRI01
	WRITE	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*
	Reset	X	X	X	X	X	X	X	X

PRI01	Bit PRI_LOS in register TelClock2 switched from 0 to 1.
PRI10	Bit PRI_LOS in register TelClock2 switched from 1 to 0.
SEC01	Bit SEC_LOS in register TelClock2 switched from 0 to 1.
SEC10	Bit SEC_LOS in register TelClock2 switched from 1 to 0.
HLDOVR01	Bit HOLDOVER in register TelClock2 switched from 0 to 1.
HLDOVR10	Bit HOLDOVER in register TelClock2 switched from 1 to 0.
UNLOCK01	Bit UNLOCK in register TelClock2 switched from 0 to 1.
UNLOCK10	Bit UNLOCK in register TelClock2 switched from 1 to 0.

This register reports changes since the last time it was read. A legacy ISA interrupt will be generated when any of those bits are set. The actual interrupt used is assigned by the BIOS at boot time and can be read from register TelClock7.

The action of reading this register will clear all bits that were '1' prior to the reading. Bits that turned to '1' during of after the reading will not be affected.

B.16 0AOFH: TELCLOCK7 (TELECOM CLOCK OPTION)

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0xA0F	READ	*NU*	*NU*	*NU*	*NU*	Interrupt Number			
	WRITE	*NU*	*NU*	*NU*	*NU*	Interrupt Number			
	Reset	X	X	X	X	0101b			

The content of this register is the number of the legacy ISA interrupt used for events (see register TelClock6). It is initialized at boot time by the BIOS.

The interrupt is acknowledged by a read of TelClock6 register. Always perform a read to this register before enabling the interrupt in the chipset to get rid of any pending interrupt.

Note that a value of 2 will hook the interrupt to an SMI.

C. Connector Pinouts

C.1 CONNECTORS AND HEADERS SUMMARY

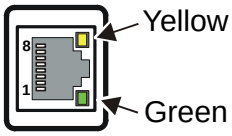
Connector	Description
M1	Fiber Channel 0 / RJ45 Connector
M2	Fiber Channel 1 / RJ45 Connector
J3	Ethernet Management
J4	USB 0
J5	Serial Port (RJ-45)
J6	VGA
J11	2.5" Hard Disk connector
J13	POST Code Connector
J21	CompactFlash
J23	ATCA Base & Fabric Interface
J30	ATCA RTM Connector
P10	ATCA Power
JN1	PMC Connector
JN2	PMC Connector
JN3	PMC Connector

C.2 FIBER CHANNEL (J1 & J2)

Signal	Pin		Pin	Signal
VEET_1	1		11	VEER_3
TX_FAULT	2		12	RD-
TX_DIS	3		13	RD+
MODDEF2	4		14	VEER_4
MODDEF1	5		15	VCCR
MODEFF0	6		16	VCCT
R_SEL	7		17	VEET_2
LOS	8		18	TD+
VEER1	9		19	TD-
VEER2	10		20	VEET_3
cGND_1	21		22	cGND_2
cGND_3	23		24	cGND_4
cGND_5	25		26	cGND_6
cGND_7	27		28	cGND_8
cGND_9	29		30	cGND_10
cGND_11	31			

C.3 ETHERNET MANAGEMENT (J3)

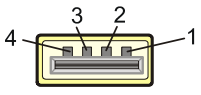
Signal	
TX+	1
TX-	2
RX+	3
N.C.	4
N.C.	5
RX-	6
N.C.	7
N.C.	8



Note
These two LEDs might be reversed.

C.4 USB (LOCATED ON FACEPLATE) (J4)

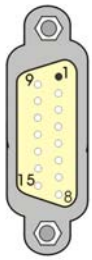
Signal	Pin
VCC	1
DATA-	2
DATA+	3
GND	4



C.5 SERIAL PORT 1 - RS-232 (J5)

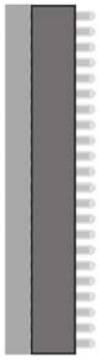
Signal	Pin		Pin	Signal
RTS	1		6	GND
DTR	2		7	RXD
TXD	3		8	DSR
GND	4		9	CTS

C.6 VIDEO (SVGA) (J6)

Signal	Pin		Pin	Signal
RED	1		9	N.C.
GREEN	2		10	GND
BLUE	3		11	N.C.
N.C.	4		12	SDATA
GND	5		13	HSYNC
GND	6		14	VSYNC
GND	7		15	SCLCK
GND	8			

C.7 2.5" IDE HARD DISK (J11)

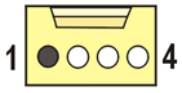
Signal	Pin		Pin	Signal
OPT_A	45		46	OPT_B
OPT_C	47		48	OPT_D
N.C.	49		50	N.C.
RESET#	1		2	GND
DD7	3		4	DD8
DD6	5		6	DD9
DD5	7		8	DD10
DD4	9		10	DD11
DD3	11		12	DD12
DD2	13		14	DD13
DD1	15		16	DD14
DD0	17		18	DD15
GND	19		20	KEY
DMARQ	21		22	GND
DIOW#	23		24	GND
DIOR#	25		26	GND
IORDY	27		28	CSEL#
DMASK#	29		30	GND
INTRQ	31		32	RSV
DA1	33		34	PDIAG#
DA0	35		36	DA2
CS0#	37		38	CS1#
DASP#	39		40	GND
VCC	41		42	VCC
GND	43		44	RSV



Active Low Signal

C.8 POST CODE (J13)

Signal	Pin
VCC3	1
DATA	2
CLOCK	3
GND	4

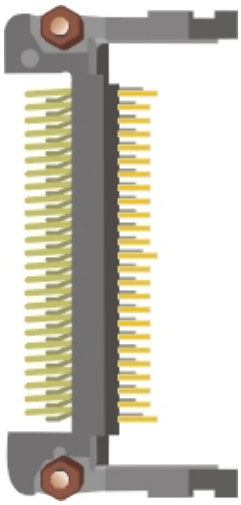


C.9 AMC B1 & AMC B2 (J18 & J19)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
B1	GND	B43	GND	B86	GND	B129	TxD15-(N.C.)
B2	12V	B44	RxD4+	B87	TxD8-	B130	TxD15+(N.C.)
B3	PS1#	B45	RxD4-	B88	TxD8+	B131	GND
B4	MP_3V3	B46	GND	B89	GND	B132	RxD15-(N.C.)
B5	GA0	B47	TxD4+	B90	RxD8-	B133	RxD15+(N.C.)
B6	RSV	B48	TxD4-	B91	RxD8+	B134	GND
B7	GND	B49	GND	B92	GND	B135	TxD16-(N.C.)
B8	RSV	B50	RxD5+	B93	TxD9-	B136	TxD16+(N.C.)
B9	12V	B51	RxD5-	B94	TxD9+	B137	GND
B10	GND	B52	GND	B95	GND	B138	RxD16-(N.C.)
B11	RxD0+	B53	TxD5+	B96	RxD9-	B139	RxD16+(N.C.)
B12	RxD0-	B54	TxD5-	B97	RxD9+	B140	GND
B13	GND	B55	GND	B98	GND	B141	TxD17-(N.C.)
B14	TxD0+	B56	IPMB-L-SCL	B99	TxD10-	B142	TxD17+(N.C.)
B15	TxD0-	B57	12V	B100	TxD10+	B143	GND
B16	GND	B58	GND	B101	GND	B144	RxD17-(N.C.)
B17	GA1	B59	RxD6+	B102	RxD10-	B145	RxD17+(N.C.)
B18	12V	B60	RxD6-	B103	RxD10+	B146	GND
B19	GND	B61	GND	B104	GND	B147	TxD18-(N.C.)
B20	RxD1+	B62	TxD6+	B105	TxD11-	B148	TxD18+(N.C.)
B21	RxD1-	B63	TxD6-	B106	TxD11+	B149	GND
B22	GND	B64	ND	B107	GND	B150	RxD18-(N.C.)
B23	TxD1+	B65	RxD7+	B108	RxD11-	B151	RxD18+(N.C.)
B24	TxD1-	B66	RxD7-	B109	RxD11+	B152	GND
B25	GND	B67	GND	B110	GND	B153	TxD19-(N.C.)
B26	GA2	B68	TxD7+	B111	TxD12-	B154	TxD19+(N.C.)
B27	12V	B69	TxD7-	B112	TxD12+	B155	GND
B28	GND	B70	GND	B113	GND	B156	RxD19-(N.C.)
B29	RxD2+	B71	IPMB_SDA	B114	RxD12-	B157	RxD19+(N.C.)
B30	RxD2-	B72	12V	B115	RxD12+	B158	GND
B31	GND	B73	GND	B116	GND	B159	TxD20-(N.C.)
B32	TxD2+	B74	CLK1+	B117	TxD13-(N.C.)	B160	TxD20+(N.C.)
B33	TxD2-	B75	CLK1-	B118	TxD13+(N.C.)	B161	GND
B34	GND	B76	GND	B119	GND	B162	RxD20-(N.C.)
B35	RxD3+(N.C.)	B77	CLK2+	B120	RxD13-(N.C.)	B163	RxD20+(N.C.)
B36	RxD3-(N.C.)	B78	CLK2-	B121	RxD13+(N.C.)	B164	GND
B37	GND	B79	GND	B122	GND	B165	TCLK(N.U.)
B38	TxD3+(N.C.)	B80	CLK3+	B123	TxD14-(N.C.)	B166	TMS(N.U.)
B39	TxD3-(N.C.)	B81	CLK3-	B124	TxD14+(N.C.)	B167	TRST#(N.U.)
B40	GND	B82	GND	B125	GND	B168	TDO(N.U.)
B41	ENABLE#	B83	PS0#(GND)	B126	RxD14-(N.C.)	B169	TDI(N.U.)
B42	12V	B84	12V	B127	RxD14+(N.C.)	B170	GND
		B85	GND	B128	GND		

C.10 COMPACTFLASH™ (J21)

Signal	Pin		Pin	Signal
GND	1		2	DD3
DD4	3		4	DD5
DD6	5		6	DD7
CS0#	7		8	GND
GND	9		10	GND
GND	11		12	GND
VCC3	13		14	GND
GND	15		16	GND
GND	17		18	DA2
DA1	19		20	DA0
DD0	21		22	DD1
DD2	23		24	N.C.
N.C.	25		26	N.C.
DD11	27		28	DD12
DD13	29		30	DD14
DD15	31		32	CS1#
N.C.	33		34	DIOR#
DIOW#	35		36	WE#(3.3V)
INTRq	37		38	VCC3
CSEL#(GND)	39		40	N.C.
RESET#	41		42	IORDY
DMARQ	43		44	DMACK#
DASP#	45		46	PDIAG#
DD8	47		48	DD9
DD10	49		50	GND



Active Low Signal

C.11 TELCO CLOCK (J20)

Pin	ROW A	ROW B	ROW C	ROW D	ROW E	ROW F
1	CLK1A+	CLK1A	CLK1B+	CLK1B	CLK2A+	CLK2A
2	Tx4(UP)+(N.C.)	Tx4(UP) -(N.C.)	Rx4(UP)+(N.C.)	Rx4(UP) - (N.C.)	CLK3A+	CLK3A
3	Tx2(UP)+(N.C.)	Tx2(UP) - (N.C.)	Rx2(UP)+(N.C.)	Rx2(UP) - (N.C.)	Tx3(UP)+(N.C.)	Tx3(UP) - (N.C.)
4	Tx0(UP)+(N.C.)	Tx0(UP) - (N.C.)	Rx0(UP)+(N.C.)	Rx0(UP) - (N.C.)	Tx1(UP)+(N.C.)	Tx1(UP) - (N.C.)
5	Tx2[15]+(N.C.)	Tx2[15] - (N.C.)	Rx2[15]+(N.C.)	Rx2[15] - (N.C.)	Tx3[15]+(N.C.)	Tx3[15] - (N.C.)
6	Tx0[15]+(N.C.)	Tx0[15] - (N.C.)	Rx0[15]+(N.C.)	Rx0[15] - (N.C.)	Tx1[15]+(N.C.)	Tx1[15] - (N.C.)
7	Tx2[14]+(N.C.)	Tx2[14] - (N.C.)	Rx2[14]+(N.C.)	Rx2[14] - (N.C.)	Tx3[14]+(N.C.)	Tx3[14] - (N.C.)
8	Tx0[14]+(N.C.)	Tx0[14] - (N.C.)	Rx0[14]+(N.C.)	Rx0[14] - (N.C.)	Tx1[14]+(N.C.)	Tx1[14] - (N.C.)
9	Tx2[13]+(N.C.)	Tx2[13] - (N.C.)	Rx2[13]+(N.C.)	Rx2[13] - (N.C.)	Tx3[13]+(N.C.)	Tx3[13] - (N.C.)
10	Tx0[13]+(N.C.)	Tx0[13] - (N.C.)	Rx0[13]+(N.C.)	Rx0[13] - (N.C.)	Tx1[13]+(N.C.)	Tx1[13] - (N.C.)
Pin	**ROW G**	**ROW H**	**ROW AB**	**ROW CD**	**ROW EF**	**ROW GH**
1	CLK2B+	CLK2B	GND	GND	GND	GND
2	CLK3B+	CLK3B	GND	GND	GND	GND
3	Rx3(UP)+(N.C.)	Rx3(UP) - (N.C.)	GND	GND	GND	GND
4	Rx3(UP)+(N.C.)	Rx3(UP) - (N.C.)	GND	GND	GND	GND
5	Rx3[15]+(N.C.)	Rx3[15] - (N.C.)	GND	GND	GND	GND
6	Rx1[15]+(N.C.)	Rx1[15] - (N.C.)	GND	GND	GND	GND
7	Rx3[14]+(N.C.)	Rx3[14] - (N.C.)	GND	GND	GND	GND
8	Rx1[14]+(N.C.)	Rx1[14] - (N.C.)	GND	GND	GND	GND
9	Rx3[13]+(N.C.)	Rx3[13] - (N.C.)	GND	GND	GND	GND
10	Rx1[13]+(N.C.)	Rx1[13] - (N.C.)	GND	GND	GND	GND

C.12 ATCA I/O (J23) ATCA 3.1

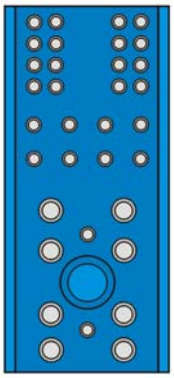
Pin	ROW A	ROW B	ROW C	ROW D	ROW E	ROW F
1	Tx2[2]+(N.C.)	Tx2[2]-(N.C.)	Rx2[2]+(N.U.)	Rx2[2]-(N.U.)	Tx3[2]-	Tx3[2]-
2	Tx0[2]+	Tx0[2]-	Rx0[2]+	Rx0[2]-	Tx1[2]+	Tx1[2]-
3	Tx2[1]+(N.C.)	Tx2[1]-(N.C.)	Rx2[1]+(N.U.)	Rx2[1]-(N.U.)	Tx3[1]+	Tx3[1]-
4	Tx0[1]+	Tx0[1]-	Rx0[1]+	Rx0[1]-	Tx1[1]+	Tx1[1]-
5	BI_DA1+	BI_DA1-	BI_DB1+	BI_DB1-	BI_DC1+	BI_DC1-
6	BI_DA2+	BI_DA2-	BI_DB2+	BI_DB2-	BI_DC2+	BI_DC2-
7	RSV	RSV	RSV	RSV	RSV	RSV
8	RSV	RSV	RSV	RSV	RSV	RSV
9	RSV	RSV	RSV	RSV	RSV	RSV
10	RSV	RSV	RSV	RSV	RSV	RSV
Pin	**ROW G**	**ROW H**	**ROW AB**	**ROW CD**	**ROW EF**	**ROW GH**
1	Rx3[2]+	Rx3[2]-	GND	GND	GND	GND
2	Rx1[2]+	Rx1[2]-	GND	GND	GND	GND
3	Rx3[1]+	Rx3[1]-	GND	GND	GND	GND
4	Rx1[1]+	Rx1[1]-	GND	GND	GND	GND
5	BI_DD1+	BI_DD1-	GND	GND	GND	GND
6	BI_DD2+	BI_DD2-	GND	GND	GND	GND
7	RSV	RSV	GND	GND	GND	GND
8	RSV	RSV	GND	GND	GND	GND
9	RSV	RSV	GND	GND	GND	GND
10	RSV	RSV	GND	GND	GND	GND

C.13 RTM Connector (J30)

Pin	ROW A	ROW B	ROW C	ROW D	ROW E	ROW F
1	USB1_VCC(N.C.)	USB0_VCC	PS2_CLK	PS2_DAT	LAN_DA-	LAN_DA+
2	BRD_RESET#	TEST_SPKR#	KBD_CLK	KBD_DAT	LAN_DB-	LAN_DB+
3	+5V	3.3V_SUS	SMB_SCL	SMB_SDA	LAN_DC- (N.C.)	LAN_DC+ (N.C.)
4	JTAG_CFG(N.C.)	TEST_ON#	POST_CLK	POST_DAT	LAN_DD- (N.C.)	LAN_DC- (N.C.)
5	JTAG_TDO	TEST_JIG#	LPC_CLK	LPC_HINIT#	LAN_SPD	LAN_ACT/L#
6	JTAG_TDI	3.3V	LPC_FRAME#	LPC_RESET#	LAN_CT (GND)	+12V
7	JTAG_TCK	TEST_FWH	LPC_AD2	LCP_AD3	VGA_SCL	VGA_SDA
8	JTAG_TMS	JTAG_TRST#(N.C.)	LPC_AD0	LPC_AD1	VGA_BLUE	SMB_ALERT#
9	SP0_RI	SP0_DTR	SP0_CTS	SP0_TX#	VGA_GREEN	VGA_VSYNC
10	SP0_RTS	SP0_RX#	SP0_DSR	SP0_DCD	VGA_RED	VGA_HSYNC
Pin	**ROW G**	**ROW H**	**ROW AB**	**ROW CD**	**ROW EF**	**ROW GH**
1	SATA0_RX- (N.C.)	SATA0_RX+(N.C.)	GND	GND	GND	GND
2	SATA0_TX- (N.C.)	SATA0_TX+(N.C.)	GND	GND	GND	GND
3	SATA1_RX- (N.C.)	SATA1_RX+(N.C.)	GND	GND	GND	GND
4	SATA1_TX- (N.C.)	SATA1_TX+(N.C.)	GND	GND	GND	GND
5	SATA2_RX- (N.C.)	SATA2_RX+(N.C.)	GND	GND	GND	GND
6	SATA2_TX- (N.C.)	SATA2_TX+(N.C.)	GND	GND	GND	GND
7	SATA3_RX- (N.C.)	SATA3_RX+(N.C.)	GND	GND	GND	GND
8	SATA3_TX- (N.C.)	SATA3_TX+(N.C.)	GND	GND	GND	GND
9	USB0_D	USB0_D+	GND	GND	GND	GND
10	USB1_D- (N.C.)	USB1_D+(N.C.)	GND	GND	GND	GND

Active Low Signal

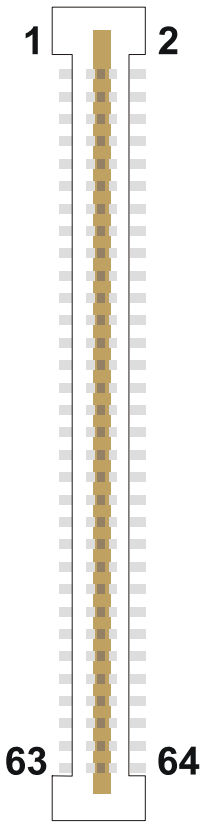
C.14 POWER (P10)

Signal	Pin		Pin	Signal
N.P.	1		2	N.P.
N.P.	3		4	N.P.
HA0	5		6	HA1
HA2	7		8	HA3
HA4	9		10	HA5
HA6	11		12	HA7/P
IPMBA_SCL	13		14	SDA_A
SCL_B	15		16	SDA_B
N.C.	17		18	N.C.
N.C.	19		20	N.C.
N.C.	21		22	N.C.
N.C.	23		24	N.C.
SHELF_GND	25		26	LOGIC_GND
ENABLE_B	27		28	VRTN_A
VRTN_B	29		30	EARLY_A
EARLY_B	31		32	ENABLE_A
-48V_A	33		34	-48V_B

Active Low Signal

C.15 JN1 – PMC (JN1)

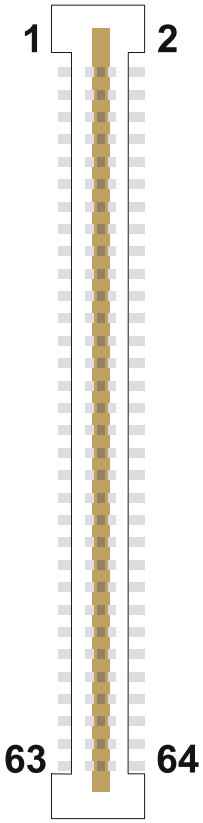
Signal	Pin		Pin	Signal
TCK(N.C.)	1		2	-12V
GND	3		4	INTA#
INTB#	5		6	INTC#
BUSMODE1#	7		8	5V
INTD#	9		10	PCI-RSV
GND	11		12	3V3_AUX (N.C.)
CLK	13		14	GND
GND	15		16	GNT#
REQ#	17		18	5V
VIO	19		20	AD31
AD28	21		22	AD27
AD25	23		24	GND
GND	25		26	C/BE#3
AD22	27		28	AD21
AD19	29		30	5V
VIO	31		32	AD17
FRAME#	33		34	GND
GND	35		36	IRDY#
DEVSEL#	37		38	5V
PCIXCAP	39		40	LOCK#
PCI-RSV	41		42	PCI-RSV
PAR	43		44	GND
VIO	45		46	AD15
AD12	47		48	AD11
AD9	49		50	5V
GND	51		52	C/CBE0#
AD6	53		54	AD5
AD4	55		56	GND
VIO	57		58	AD3
AD2	59		60	AD1
AD0	61		62	5V
GND	63		64	REQ64#



Active Low Signal

C.16 JN2 – PMC (JN2)

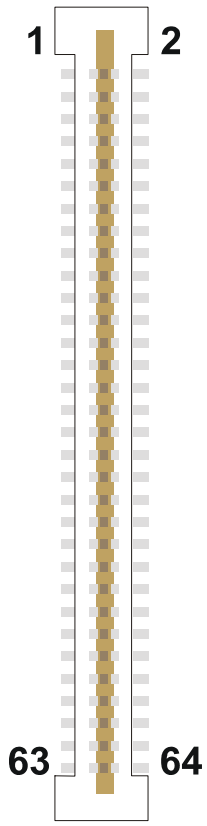
Signal	Pin		Pin	Signal
+12V	1		2	TRST#(GND)
TMS(N.U.)	3		4	TDO(N.U.)
TDI(N.U.)	5		6	GND
GND	7		8	PCI-RSV
PCI-RSV	9		10	PCI-RSV
BUSMODE2#	11		12	3V3
RST#	13		14	BUSMODE3#
3V3	15		16	BUSMODE4#
PME#(N.U.)	17		18	GND
AD30	19		20	AD29
GND	21		22	AD26
AD24	23		24	3V3
IDSEL	25		26	AD23
3V3	27		28	AD20
AD18	29		30	GND
AD16	31		32	C/BE2#
GND	33		34	PMC-RSV
TRDY#	35		36	3V3
GND	37		38	STOP#
PERR#	39		40	GND
3V3	41		42	SERR#
C/BE1#	43		44	GND
AD14	45		46	AD13
M66EN	47		48	AD10
AD8	49		50	3V3
AD7	51		52	PMC-RSV
3V3	53		54	PMC-RSV
PMC-RSV	55		56	GND
PMC-RSV	57		58	PMC-RSV
GND	59		60	PMC-RSV
ACK64#	61		62	3V3
GND	63		64	PMC-RSV



Active Low Signal

C.17 JN3 – PMC (JN3)

Signal	Pin		Pin	Signal
PMC-RSV	1		2	GND
GND	3		4	C/BE7#
C/BE6#	5		6	C/BE5#
C/BE4#	7		8	GND
VIO	9		10	PAR64
AD63	11		12	AD62
AD61	13		14	GND
GND	15		16	AD60
AD59	17		18	AD58
AD57	19		20	GND
VIO	21		22	AD56
AD55	23		24	AD54
AD53	25		26	GND
GND	27		28	AD52
AD51	29		30	AD50
AD49	31		32	GND
GND	33		34	AD48
AD47	35		36	AD46
AD45	37		38	GND
VIO	39		40	AD44
AD43	41		42	AD42
AD41	43		44	GND
GND	45		46	AD40
AD39	47		48	AD38
AD37	49		50	GND
GND	51		52	AD36
AD35	53		54	AD34
AD33	55		56	GND
VIO	57		58	AD32
PMC-RSV	59		60	PMC-RSV
PMC-RSV	61		62	GND
GND	63		64	PMC-RSV



Active Low Signal

D. BIOS Setup Error Codes

D.1 Bootblock Initialization Code Checkpoints

The Bootblock initialization code sets up the chipset, memory and other components before system memory is available. The following table describes the type of checkpoints that may occur during the bootblock initialization portion of the BIOS:

Checkpoint	Description
Before D1	Early chipset initialization is done. Early super I/O initialization is done including RTC and keyboard controller. NMI is disabled.
D1	Perform keyboard controller BAT test. Check if waking up from power management suspend state. Save power-on CPUID value in scratch CMOS.
D0	Go to flat mode with 4GB limit and GA20 enabled. Verify the bootblock checksum.
D2	Disable CACHE before memory detection. Execute full memory sizing module. Verify that flat mode is enabled.
D3	If memory sizing module not executed, start memory refresh and do memory sizing in Bootblock code. Do additional chipset initialization. Re-enable CACHE. Verify that flat mode is enabled.
D4	Test base 512KB memory. Adjust policies and cache first 8MB. Set stack.
D5	Bootblock code is copied from ROM to lower system memory and control is given to it. BIOS now executes out of RAM.
D6	Both key sequence and OEM specific method is checked to determine if BIOS recovery is forced. Main BIOS checksum is tested. If BIOS recovery is necessary, control flows to checkpoint E0. See *Bootblock Recovery Code Checkpoints* section of document for more information.
D7	Restore CPUID value back into register. The Bootblock-Runtime interface module is moved to system memory and control is given to it. Determine whether to execute serial flash.
D8	The Runtime module is uncompressed into memory. CPUID information is stored in memory.
D9	Store the Uncompressed pointer for future use in PMM. Copying Main BIOS into memory. Leaves all RAM below 1MB Read-Write including E000 and F000 shadow areas but closing SMRAM.
DA	Restore CPUID value back into register. Give control to BIOS POST (ExecutePOSTKernel). See *POST Code Checkpoints* section of document for more information.
E1-E8 EC-EE	OEM memory detection/configuration error. This range is reserved for chipset vendors & system manufacturers. The error associated with this value may be different from one platform to the next. Refer to memory initialization ERROR CODE D.5

D.2 POST Code Checkpoints

The POST code checkpoints are the largest set of checkpoints during the BIOS pre-boot process. The following table describes the type of checkpoints that may occur during the POST portion of the BIOS:

Checkpoint	Description
03	Disable NMI, Parity, video for EGA, and DMA controllers. Initialize BIOS, POST, Runtime data area. Also initialize BIOS modules on POST entry and GPNV area. Initialized CMOS as mentioned in the Kernel Variable "wCMOSFlags."
04	Check CMOS diagnostic byte to determine if battery power is OK and CMOS checksum is OK. Verify CMOS checksum manually by reading storage area. If the CMOS checksum is bad, update CMOS with power-on default values and clear passwords. Initialize status register A. Initializes data variables that are based on CMOS setup questions. Initializes both the 8259 compatible PICs in the system
05	Initializes the interrupt controlling hardware (generally PIC) and interrupt vector table.
06	Do R/W test to CH-2 count reg. Initialize CH-0 as system timer. Install the POSTINT1Ch handler. Enable IRQ-0 in PIC for system timer interrupt. Traps INT1Ch vector to "POSTINT1ChHandlerBlock."
08	Initializes the CPU. The BAT test is being done on KBC. Program the keyboard controller command byte is being done after Auto detection of KB/MS using AMI KB-5.
C0	Early CPU Init Start -- Disable Cache - Init Local APIC
C1	Set up boot strap processor Information
C2	Set up boot strap processor for POST
C5	Enumerate and set up application processors
C6	Re-enable cache for boot strap processor
C7	Early CPU Init Exit
0A	Initializes the 8042 compatible Key Board Controller.
0B	Detects the presence of PS/2 mouse.
0C	Detects the presence of Keyboard in KBC port.
0E	Testing and initialization of different Input Devices. Also, update the Kernel Variables. Traps the INT09h vector, so that the POST INT09h handler gets control for IRQ1. Uncompress all available language, BIOS logo, and Silent logo modules.
13	Early POST initialization of chipset registers.
24	Uncompress and initialize any platform specific BIOS modules.
30	Initialize System Management Interrupt.
2A	Initializes different devices through DIM. See *DIM Code Checkpoints* section of document for more information.
2C	Initializes different devices. Detects and initializes the video adapter installed in the system that have optional ROMs.
2E	Initializes all the output devices.
31	Allocate memory for ADM module and uncompress it. Give control to ADM module for initialization. Initialize language and font modules for ADM. Activate ADM module.
33	Initializes the silent boot module. Set the window for displaying text information.
37	Displaying sign-on message, CPU information, setup key message, and any OEM specific information.
38	Initializes different devices through DIM. See *DIM Code Checkpoints* section of document for more information.

39	Initializes DMAC-1 & DMAC-2.
3A	Initialize RTC date/time.
3B	Test for total memory installed in the system. Also, Check for DEL or ESC keys to limit memory test. Display total memory in the system.
3C	Mid POST initialization of chipset registers.
40	Detect different devices (Parallel ports, serial ports, and coprocessor in CPU, ... etc.) successfully installed in the system and update the BDA, EBDA...etc.
50	Programming the memory hole or any kind of implementation that needs an adjustment in system RAM size if needed.
52	Updates CMOS memory size from memory found in memory test. Allocates memory for Extended BIOS Data Area from base memory.
60	Initializes NUM-LOCK status and programs the KBD typematic rate.
75	Initialize Int-13 and prepare for IPL detection.
78	Initializes IPL devices controlled by BIOS and option ROMs.
7A	Initializes remaining option ROMs.
7C	Generate and write contents of ESCD in NVRam.
84	Log errors encountered during POST.
85	Display errors to the user and gets the user response for error.
87	Execute BIOS setup if needed / requested.
8C	Late POST initialization of chipset registers.
8D	Build ACPI tables (if ACPI is supported)
8E	Program the peripheral parameters. Enable/Disable NMI as selected
90	Late POST initialization of system management interrupt.
A0	Check boot password if installed.
A1	Clean-up work needed before booting to OS.
A2	Takes care of runtime image preparation for different BIOS modules. Fill the free area in F000h segment with 0FFh. Initializes the Microsoft IRQ Routing Table. Prepares the runtime language module. Disables the system configuration display if needed.
A4	Initialize runtime language module.
A7	Displays the system configuration screen if enabled. Initialize the CPU's before boot, which includes the programming of the MTRR's.
A8	Prepare CPU for OS boot including final MTRR values.
A9	Wait for user input at config display if needed.
AA	Uninstall POST INT1Ch vector and INT09h vector. Deinitializes the ADM module.
AB	Prepare BBS for Int 19 boot.
AC	End of POST initialization of chipset registers.
B1	Save system context for ACPI.
00	Passes control to OS Loader (typically INT19h).
61-70	OEM POST Error. This range is reserved for chipset vendors & system manufacturers. The error associated with this value may be different from one platform to the next.
DD-DE	OEM PCI init debug POST code during DIMM init, See *DIM Code Checkpoints* section of document for more information.

D.3 DIM Code Checkpoints

The Device Initialization Manager (DIM) gets control at various times during BIOS POST to initialize different system busses. The following table describes the main checkpoints where the DIM module is accessed:

Checkpoint	Description
2A	Initialize different buses and perform the following functions: Reset, Detect, and Disable (function 0); Static Device Initialization (function 1); Boot Output Device Initialization (function 2). Function 0 disables all device nodes, PCI devices, and PnP ISA cards. It also assigns PCI bus numbers. Function 1 initializes all static devices that include manual configured onboard peripherals, memory and I/O decode windows in PCI-PCI bridges, and noncompliant PCI devices. Static resources are also reserved. Function 2 searches for and initializes any PnP, PCI, or AGP video devices.
38	Initialize different buses and perform the following functions: Boot Input Device Initialization (function 3); IPL Device Initialization (function 4); General Device Initialization (function 5). Function 3 searches for and configures PCI input devices and detects if system has standard keyboard controller. Function 4 searches for and configures all PnP and PCI boot devices. Function 5 CONFIGURES all onboard peripherals that are set to an automatic configuration and configures all remaining PnP and PCI devices.
DD-DE	OEM PCI init debug POST code during DIMM init. DEh during BUS number assignment and DDh during ressource allocation, Hight byte is the BUS number.

While control is in the different functions, additional checkpoints are output to port 80h as a word value to identify the routines under execution. The low byte value indicates the main POST Code Checkpoint. The high byte is divided into two nibbles and contains two fields. The details of the high byte of these checkpoints are as follows:

HIGH BYTE XY

The upper nibble 'X' indicates the function number that is being executed. 'X' can be from 0 to 7.

0 = func#0, disable all devices on the BUS concerned.

1 = func#1, static devices initialization on the BUS concerned.

2 = func#2, output device initialization on the BUS concerned.

3 = func#3, input device initialization on the BUS concerned.

4 = func#4, IPL device initialization on the BUS concerned.

5 = func#5, general device initialization on the BUS concerned.

6 = func#6, error reporting for the BUS concerned.

7 = func#7, add-on ROM initialization for all BUSes.

8 = func#8, BBS ROM initialization for all BUSes.

The lower nibble 'Y' indicates the BUS on which the different routines are being executed. 'Y' can be from 0 to 5.

0 = Generic DIM (Device Initialization Manager).

1 = On-board System devices.

2 = ISA devices.

3 = EISA devices.

4 = ISA PnP devices.

5 = PCI devices.

D.4 ACPI Runtime Checkpoints

ACPI checkpoints are displayed when an ACPI capable operating system either enters or leaves a sleep state. The following table describes the type of checkpoints that may occur during ACPI sleep or wake events:

Checkpoint	Description
AC	First ASL check point. Indicates the system is running in ACPI mode.
AA	System is running in APIC mode.
01, 02, 03, 04, 05	Entering sleep state S1, S2, S3, S4, or S5.
10, 20, 30, 40, 50	Waking from sleep state S1, S2, S3, S4, or S5.

D.5 Memory initialization ERROR Code.

Checkpoint	Description
E1h	Memory Error - No memory installed.
E2h	Memory Error – Memory type mismatch.
E3h	Memory Error – Unsupported DIMM type.
E4h	Memory Error – Channel mismatch.
EAh	Memory Error – Memory timing error
EEh	Memory Error – Memory unsupported size.
EFh	Memory Error – Memory population order.
F1h	Memory Error – DIMM configuration error.
F3h	Memory Error – Error code for unsuccessful Memory Test.
F4h	Memory Error – Error code for unsuccessful ECC and Memory Initialization
F5h	Memory Error – Receive enable is busted so halt here

D.6 Beep Codes

The following table describes the beep codes that are used by AMIBIOS:

Number of Beeps	Description
1	Memory refresh timer error.
2	Parity error
3	Main memory read / write test error.
4	Motherboard timer not operational

5	Processor error
6	Keyboard controller BAT test error.
7	General exception error.
8	Display memory error.
9	ROM checksum error
10	CMOS shutdown register read/write error
11	Cache memory bad

D.6.1 Troubleshooting BIOS Beep Codes

Number of Beeps	Troubleshooting Action
1, 2 or 3	Reseat the memory, or replace with known good modules.
4-7, 9-11	Fatal error indicating a serious problem with the system. Consult your system manufacturer. Before declaring the motherboard beyond all hope, eliminate the possibility of interference by a malfunctioning add-in card. Remove all expansion cards cards except the video adapter. • If the beep codes are generated even when all other expansion cards are absent, the motherboard has a serious problem. Consult your system manufacturer. • If the beep codes are not generated when all other expansion cards are absent, one of the add-in cards is causing the malfunction. Insert the cards back into the system one at a time until the problem happens again. This will reveal the malfunctioning add-in card.
8	If the system video adapter is an add-in card, replace or reseat the video adapter. If the video adapter is an integrated part of the system board, the board may be faulty.

E. Software Update

E.1 Flash BIOS Update Procedure

The Flash BIOS update procedure is detailed in a ReadMe file included with the Flash BIOS package as well as the update utility. This package can be downloaded from our website www.kontron.com or from our FTP site ftp://ftp.kontron.ca/Support

E.2 IPMC Firmware Update Procedure

The IPMC Firmware update procedure is detailed in a ReadMe file included with the IPMC Firmware package as well as the update utility. This package can be downloaded from our website www.kontron.com or from our FTP site ftp://ftp.kontron.ca/Support

F. Getting Help

At Kontron, we take great pride in our customers' successes. We believe in providing full support at all stages of your product development.

If at any time you encounter difficulties with your application or with any of our products, or if you simply need guidance on system setups and capabilities, contact our Technical Support at:

CANADIAN HEADQUARTERS
Tel. (450) 437-5682
Fax: (450) 437-8053

If you have any questions about Kontron, our products, or services, visit our Web site at:
www.kontron.com

You also can contact us by E-mail at: support@ca.kontron.com

Or at the following address:

Kontron Canada, Inc.
616 Curé Boivin
Boisbriand, Québec
J7G 2A7 Canada

RETURNING DEFECTIVE MERCHANDISE

Before returning any merchandise please do one of the following if your product malfunctions:

- Call

    1. Call our **Technical Support** department in Canada at **(450) 437-5682**. Make sure you have the following on hand: **our Invoice #,** your **Purchase Order #,** and the **Serial Number** of the defective unit.

    2. Provide the serial number found on the back of the unit and explain the nature of your problem to a service technician.

    3. The technician will instruct you on the return procedure if the problem cannot be solved over the telephone.

    4. Make sure you receive an **RMA #** from **our Technical Support** before returning any merchandise.

- Fax

    1. Make a copy of the request form on the following page.

    2. Fill it out.

    3. Fax it to us at: (450) 437-0304

- E-mail

    1. Send us an e-mail at: RMA@ca.kontron.com. In the e-mail, you must include your name, your company name, your address, your city, your postal/zip code, your phone number, and your e-mail. You must also include the **serial number** of the defective product and **a description of the problem.**

When returning a unit.

i) In the box, you have to include the name and telephone number of a person whom we can contact for further explanations if necessary when returning goods. **Where applicable, always include all duty papers and invoice(s) associated with the item(s) in question.**

ii) Ensure that the unit is properly packed. Pack it in a rigid cardboard box.

iii) Clearly write or mark the RMA number on the outside of the package you are returning.

iv) Ship prepaid. We take care of insuring incoming units.

Kontron Canada Inc.
616 Curé Boivin
Boisbriand, Québec
J7G 2A7 Canada



Return to Manufacturer Authorization Request

Contact Name:	_____		
Company Name:	_____		
Street Address:	_____		
City:	_____	Province/State:	_____
Country:	_____	Postal/Zip Code:	_____
Phone Number:	_____	Extension:	_____
Fax Number:	_____	E-Mail:	_____

Serial Number	Failure or Problem Description	P.O. # (if not under warranty)

Kontron Canada, Inc., 616 Curé Boivin, Boisbriand, Québec, Canada, J7G 2A7

Fax this form to Kontron's Technical Support department in Canada at (450) 437-0304