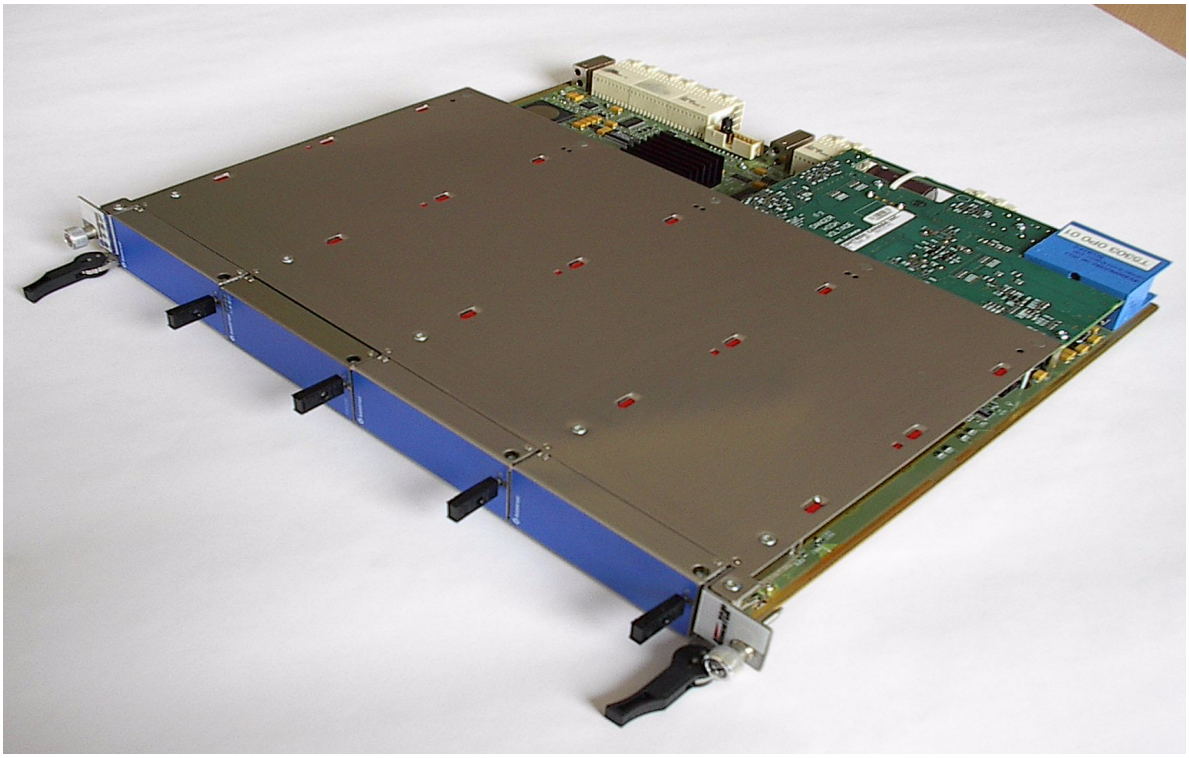
AT8400 USER GUIDE

AdvancedTCA

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Final disposition of this product after its service life must be accomplished in accordance with applicable country, state, or local laws or regulations.

Explanation of Symbols



CE Conformity

This symbol indicates that the product described in this manual is in compliance with all applied CE standards. Please refer also to the section “Applied Standards” in this manual.



Caution, Electric Shock!

This symbol and title warn of hazards due to electrical shocks (> 60V) when touching products or parts of them. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your material.

Please refer also to the section “High Voltage Safety Instructions” on the following page.



Warning, ESD Sensitive Device!

This symbol and title inform that electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Please read also the section “Special Handling and Unpacking Instructions” on the following page.



Warning!

This symbol and title emphasize points which, if not fully understood and taken into consideration by the reader, may endanger your health and/or result in damage to your material.



Note...

This symbol and title emphasize aspects the reader should read through carefully for his or her own advantage.

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Your new Kontron product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new Kontron product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions



Warning!

All operations on this device must be carried out by sufficiently skilled personnel only.



Caution, Electric Shock!

High voltages are present inside the chassis when the unit's power cord is plugged into an electrical outlet. Turn off system power, turn off the power supply, and then disconnect the power cord from its source before removing the chassis cover. Turning off the system power switch does not remove power to components.

Special Handling and Unpacking Instructions



ESD Sensitive Device!

Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing mezzanines, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory back-up, ensure that the board is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the board.

General Instructions on Usage

In order to maintain Kontron's product warranty, this product must not be altered or modified in any way. Changes or modifications to the device, which are not explicitly approved by Kontron AG and described in this manual or received from Kontron's Technical Support as a special handling instruction, will void your warranty.

This device should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This applies also to the operational temperature range of the specific board version, which must not be exceeded. If batteries are present their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, please follow only the instructions supplied by the present manual.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the board please re-pack it as nearly as possible in the manner in which it was delivered.

Special care is necessary when handling or unpacking the product. Please, consult the special handling and unpacking instruction on the previous page of this manual.

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If the customer's eligibility for warranty has not been voided, in the event of any claim, he may return the product at the earliest possible convenience to the original place of purchase, together with a copy of the original document of purchase, a full description of the application the product is used on and a description of the defect. Pack the product in such a way as to ensure safe transportation (see our safety instructions).

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Chapter 1

Introduction

1. Introduction

The Board described in this manual is designed for the Advanced Telecom Computing Architecture (AdvancedTCA® or ATCA) defined by the *PCI Industrial Computer Manufacturers Group (PICMG)*. The main advantages of AdvancedTCA include high throughput, multi-protocol support, high-power capability, hot swappability, high scalability and integrated system management. For further information regarding the AdvancedTCA standards and their use, please consult the complete AdvancedTCA specification or visit the *PICMG* web site.

1.1 Product Overview

The Kontron AT8400 is a PICMG 3.0 and 3.1 Option 2 compliant Carrier Board for Advanced TCA shelves, designed according to the RoHS directive. It is a 4-slot PICMG AMC.0 compliant Conventional Carrier with partial PCB cutaway in the AMC area. A Gigabit Ethernet Switch provides connection to the base and extension fabric interface.

1.1.1 AT8400 Features

The board is composed of the following building blocks:

- Gigabit Ethernet Switch
- PCI Express Infrastructure
- SAS/SATA Infrastructure
- Ethernet Switch Controller and Memory
- Synchronous Clock Distribution
- Up to four AMC bays
- RTM Connector (Zone 3)
- IPMI
- Power Supply Mezzanine incl. Hold Over Circuit

1.1.1.1 Ethernet Switch

- Broadcom BCM56305: 20 Port Gigabit Layer-2/3 Switch
- PCI 32b/66MHz Management IF
- Line rate switching for all packet sizes and conditions
- Supports 2 Base Channels 10/100/1000Base-T via external Copper PHY
- Supports 2 Fabric Channels with 4 1000Base-BX each via internal SERDES
- Supports 2 AMC GbE interfaces per AMC slot
- Supports 2 SGMII interfaces to the RTM
- Broadcom BCM5466R PHY for Base Interface and RTM connections

1.1.1.2 PCI Express Infrastructure

- PLX Technology PEX8532 32-Lane PCI Express Switch
- Supports 8 PCI Express Lanes to AMC B2 and B4
- Supports 4 PCI Express Lanes to AMC B1 and B3
- Supports 4 PCI Express Lanes to Update Channel
- Supports 4 PCI Express Lanes to SAS Controller

1.1.1.3 SAS/SATA Infrastructure

- LSI Logic LSISAS1064E 3.0 Gbit/s Serial Attached SCSI Controller
- LSI Logic LSISASx12 3.0 Gbit/s Serial Attached SCSI Expander
- SAS controller connected to PCI Express switch via 4 PCI Express Lanes
- SAS Expander connected to SAS Controller via 4 SAS Lanes
- SAS Expander connects to each AMC slot via 1 SAS Lane. 4 SAS lanes can be used via RTM
- AMC B1 and B3 as well as B2 and B4 are directly interconnected via SATA SAS connection. Onboard SAS/SATA port selectors are used to configure either direct AMC interconnect or SAS Expander connection

1.1.1.4 Ethernet Switch Controller and System Memory

- Socketless PowerPC IBM PPC405GP 133 MHz
- Used for switch provisioning and diagnostics
- 128 MBytes of SDRAM memory, 133 MHz
- 32 MBytes of Flash memory
- Management connection to Switch Controller (CLI, SNMP) via RS232 and Fast Ethernet via RTM

1.1.1.5 Synchronous Clock and PCI Express Clock Distribution

- Zarlink ZL30410 Multi-service Line Card PLL
- MLVDS Buffer
- CPLD for clock distribution and control
- PCI Express compliant clock source with optional Spread Spectrum Clock
- Switchable PCI Express clock sourc to all AMCs and to adjacent board via Update Channel 4

1.1.1.6 IPMI

- PICMG 3.0 / IPMI 1.5 compliant
- Additional Firmware Update Manager (FUM) for field upgrades, rollbacks and watchdog functions
- Renesas R8C/13 µController
- Serial EEPROM for FRU storage (serial ID)

1.1.1.7 AMC Bays

- Up to four AMC bays (see section 1.1.6)
- Partial PCB cutaway in the AMC area
- B+ connectors
- AMC.1 Type 4E2S (x4 PCI Express) on AMC B1 and B3
- AMC.1 Type 8E2S (x8 PCI Express) support on AMC B2 and B4
- Telecom clocks and/or PCI Express clock support

1.1.1.8 RTM Connector

- Support for 8 RTM lanes from each AMC
- FE and RS232 (RJ45) management ports
- 4x SAS / SATA connections
- 2x GbE
- 12V and 3V3 sus Supply Voltage connections
- I²C support
- JTAG and production I/O support

1.1.1.9 Power Supply Mezzanine

- Isolated 48V to 12V Standard Quarterbrick intermediate bus converter
- Hot swap support
- Hold Over Circuit using high voltage capacitor and charge pump
- Isolated management power supply
- 48V power Supply 'ORing' circuit
- Supplies point of load regulators for secondary supply voltages (derived from 12V intermediate rail) on base board

1.1.2 General compliances

The AT8400 is conform to the following specifications:

- PICMG 3.0 Advanced Telecommunications Computing Architecture (ATCA)
- PICMG 3.1 Ethernet/Fibre Channel for AdvancedTCA Systems
- AMC.0 Advance Mezzanine Card Base Specification
- AMC.1 PCI Express and Advanced Switching
- AMC.2 AMC Gigabit Ethernet
- AMC.3 AMC Storage
- IPMI v1.5 Intelligent Platform Management Interface Specification
- PCI Express 1.0a

1.1.3 Optional Accessories

1.1.3.1 AMC

Up to four standard full height single width or up to two full height double width AMC bays for standard or custom AMCs are implemented.

AMC slots can be equipped with a:

- Processor-AMC, e.g. acting as the system controller (saving one ATCA slot)
- HDD-AMC as mass storage device for the Processor-AMC
- SETS-AMC providing network synchronisation for telecom applications
- Dual 10 GbE Uplink AMC to enable multi-shelf AdvancedTCA systems

Because of AMC slot storage interconnects and for thermal reasons, the preferred PrAMC slots are B1 and B2 and the preferred HDD-AMC slots are B3 and B4.

1.1.3.2 RTM

An RTM is required for GbE switch out-of-band management access via Fast Ethernet or RS232 serial. Two GbE uplinks and an external 4x SAS connector are also provided. Kontron offers the RTM8400 to suit these requirements. For further information on the RTM8400, refer to section 3.2 of this document.

1.1.4 Hot Swap Capability

The board supports Full Hot Swap capability is required by PICMG 3.0 R1.0. It can be removed from or installed in the system while it is on (without powering-down the system). Please refer to the PICMG 3.0 R1.0 specification for additional details.

1.1.5 Board Options

The Kontron AT8400 is available with different AMC slot configurations:

Table 1-1: AMC Slot Options

Option	AMC Slot Configuration
A	4 x single width slots
B	2 x double width slots
C	2 x single width slots and 1 x double width slot on B1/B2
D	2 x single width slots and 1 x double width slot on B3/B4

1.2 Technical Specification

Table 1-2: AT8400 Main Specifications

	AT8400	SPECIFICATIONS

Processor and Memory	PowerPC IBM PPC 405 GP 133MHz	• IBM PowerPC® 405 32-bit RISC processor core operating at 133MHz with 16KB I- and D-caches
		• PC-133 synchronus DRAM (SDRAM) interface
		  • 40-bit interface serves 32 bits of data plus 8 check bits for ECC applications
		• 4KB on-chip memory (OCM)
		• DMA support for external peripherals, internal UART and memory
		  • Scatter-gather chaining supported
		  • Four channels
		• PCI Revision 2.2 compliant interface (32-bit, up to 66MHz)
		• Ethernet 10/100Mbps (full-duplex) support with media independent interface (MII)
		• Two serial ports (16550 compatible UART)
		• Internal processor local Bus (PLB) runs at SDRAM interface frequency
		• IEEE 1149.1 (JTAG) boundary scan

Ethernet	Broadcom 56305	• 20 10/100/1000 Mbps Ethernet ports
		• Fifth generation of StrataSwitch and StrataXGS product line
		• Line-rate switching for all packet sizes and conditions
		• On-chip data packet memory and table memory
		• Advanced Fast Filter Processor (FFP) ContentAware classification
		• Advanced security features in hardware
		• Port-trunking and mirroring supported across stack
		• Advanced packet flow control:
		  • Head-of-line-blocking prevention
		  • Back pressure support
		• QoS queues per port with hierarchical minimum/maximum shaping per class of Service (CoS) per queue per port
		• Standard compliant 802.1ad provider bridging
		• IEEE 1149.1 (JTAG) boundary scan

	Broadcom 5466R	• Advanced power management Line-side and MAC-side loopback • Ethernet@WireSpeed • Cable plant diagnostics that detects cable plant impairments • Automatic detection and correction of wiring pair swaps, pair skew, and pair polarity • Robust CESD tolerance and low EMI emissions • Support for jumbo packets up to 10 KB in size • IEEE 1149.1 (JTAG) boundary scan

Table 1-2: AT8400 Main Specifications (Continued)

	AT8400	SPECIFICATIONS
Interfaces	Backplane (Zone 2)	• Fabric channels 1 and 2: 4 x GbE (1000BASE-BX) • Base channels 1 and 2: 1 x GbE (1000BASE-T) • Synchronization Clock: 2 x CLK 1/2/3 (A/B) • Update channels 0 to 3: x4 PCIe • Update channel 4: 100 MHz PCIe Clock
	RTM (Zone 3)	• 8 generic RTM channels from each AMC Slot • 4 SAS/SATA/FC interfaces for mass storage • 2 GbE interfaces to front board switch • Serial port for PPC management • Fast Ethernet for PPC management • I2C IPMI connection

Table 1-2: AT8400 Main Specifications (Continued)

	AT8400	SPECIFICATIONS
General	Mechanical	• 8U form factor mechanically compliant to PICMG 3.0 and AMC.0 • Single slot (6HP) • Up to four standard full height/single width AMC slots • or up to two full height/double width AMC slots • 280 mm x 322 mm (11.024“ x 12.677“) • 150 mm cut away in AMC area • Weight: 1.825 kg
	Power Requirements	• Typical: 40W • Maximum (4 AMCs and RTM): 212W • AMCs may consume up to 161W • Operating Voltage: -38 to -72 VDC
	Temperature	Designed to meet or exceed the following (Characteristics with AMCs): • Air Flow: 30 CFM min • Operating: 0°C to +55°C (32°F to 131°F) • Non-operating: -40°C to +70°C (-40°F to 158°F)
	Humidity	Designed to meet or exceed the following: • Bellcore GR63, Section 4.1 • Operating: 15%-90% (non-condensing) at 55°C (131°F) • Non-Operating: 5%-95% (non-condensing) at 40°C (104°F)
	Altitude	Designed to meet or exceed the following: • Operating: 4000 m (13123 ft) • Non-operating: 15000 m (49212 ft)
	Vibration	Designed to meet or exceed the following: • Bellcore GR-63, Section 4.4 • Operating: 1.0G, 5-500Hz each axis • Non-operating: 0.5G, 5-50Hz, 3.0G, 50-500Hz each axis
	Shock	Designed to meet or exceed the following: • DIN/IEC 60068-2-27 • Bellcore GR-63, Section 4.3 • 30G, half-sine 11ms, each axis
	Safety	Designed to meet or exceed the following: • UL 60950, 3rd edition • EN 60950 • LVD 73/23/EEC • Denan Law

Table 1-2: AT8400 Main Specifications (Continued)

	AT8400	SPECIFICATIONS
General	EMC	Designed to meet or exceed the following: • FCC 47 CFR Part 15, Subpart B • EN55022, EN55024 • EN 300 386
	Reliability	• MTBF: > 167,000 hours @ 40°C/104°F (Telcordia SR-332, Issue 1)
HW Monitoring	LEDs	ATCA LEDs: • 4 LEDs ("Ready for Hot Swap", "Out of Service", "Healthy", "Heart Beat")
	Board Management	• based on IPMI 1.5 • FRU Management • Sensors (Voltage, Current, Temperature, Fuse) • Status and Alerting • Hot Swap Management for Base Board and AMC • Electronic Keying of Base and Fabric Interfaces and AMC ports • Local SEL

1.3 Software Support

The following table contains information related to software supported by the AT8400.

Table 1-3: AT8400 Software Specification

	SPECIFICATIONS
General	• Reliable field upgrades for all software components • Dual boot images with roll-back capability • Management via SNMP and Command Line Interface • System access via TELNET, SSH and serial line • Hot-Swap support (IPMI) • Hot-Plug support for AMC modules (IPMI)
Ethernet/Bridging	• Static link aggregation (IEEE 802.3ad) on uplink ports and dedicated fabric channels • Classic and rapid spanning tree algorithms shall be supported (IEEE 802.1D, IEEE 802.1w) • Quality Of Service on all ports (IEEE 802.1p) • Full Duplex operation and flow control on all ports (IEEE 802.3x) • Static MAC filtering • Port Authentication (IEEE 802.1X) • Auto negotiation of speeds and operational mode on all external GE interfaces as well as on all base fabric interfaces • Layer 2 multicast services using GARP/GMRP (IEEE 802.1p) • VLAN support including VLAN tagging (IEEE 802.3ac), dynamic VLAN registration with GARP/GVRP (IEEE 802.1Q) and Protocol based VLANs (IEEE 802.1v) • Double VLAN tagging • Port Mirroring
Applications	• NTP client for retrieving accurate time and date information • DHCP server • Onboard event management • Test and trace facilities • POST (power on self tests) diagnostics • Standards based SNMP implementation supporting SNMP v1, v2 and v3 for monitoring and management purposes • IPMI based management of the onboard AMC slots (AMC.*) • Persistent storage of configuration across restarts • Support for retrieving and installing multiple configurations

Table 1-3: AT8400 Software Specification (Continued)

	SPECIFICATIONS

Supported MIBS	• Switching Package MIBs
	  • RFC 1213 - MIB-II
	  • RFC 1493 - Bridge MIB
	  • RFC 1643 - Ethernet-like -MIB
	  • RFC 2233 - The Interfaces Group MIB using SMI v2
	  • RFC 2618 - RADIUS Authentication Client MIB
	  • RFC 2674 - VLAN & Ethernet Priority MIB
	  • RFC 2819 - RMON Groups 1,2,3 & 9
	  • RFC 3291 - Textual Conventions for Internet Network Addresses
	  • IANA-ifType-MIB
	  • IEEE 802.1X MIB (IEEE8021-PAE-MIB)
	  • IEEE 802.3AD MIB (IEEE8021-AD-MIB)
	• QoS Package MIB
	  • RFC 3289 - DIFFSERV-MIB & DIFFSERV-DCSP-TC MIBs
	• FASTPATH Enterprise MIB
	  • Support for all managed objects not contained in standards based MIBs.

Bootloader	u-boot Version 1.1.2 • POST • multi image support • loadable bootimage via network (bootp/tftp) • reliable field upgradable • H/W protected • KCS interface to IPMC • serial console support
Operating System	• MontaVista Linux Professional Edition 3.1

Chapter 2

Installation

2. Installation

The AT8400 has been designed for easy installation. However, the following standard precautions, installation procedures, and general information must be observed to ensure proper installation and to preclude damage to the board, other system components, or injury to personnel.

2.1 Safety Requirements

The following safety precautions must be observed when installing or operating the AT8400. *Kontron* assumes no responsibility for any damage resulting from failure to comply with these requirements.



Warning!

Due care should be exercised when handling the board due to the fact that the heat sink can get very hot. Do not touch the heat sink when installing or removing the board.

In addition, the board should not be placed on any surface or in any form of storage container until such time as the board and heat sink have cooled down to room temperature.



Note ...

Certain ATCA boards require bus master and/or rear I/O capability. If you are in doubt whether such features are required for the board you intend to install, please check your specific board and/or system documentation to make sure that your system is provided with an appropriate free slot in which to insert the board.



ESD Equipment!

This ATCA board contains electrostatically sensitive devices. Please observe the necessary precautions to avoid damage to your board:

- Discharge your clothing before touching the assembly. Tools must be discharged before use.
- When unpacking a static-sensitive component from its shipping carton, do not remove the component's antistatic packing material until you are ready to install the component in a computer. Just before unwrapping the antistatic packaging, be sure you are at an ESD workstation or grounded. This will discharge any static electricity that may have built up in your body.
- When transporting a sensitive component, first place it in an antistatic container or packaging.
- Handle all sensitive components at an ESD workstation. If possible, use antistatic floor pads and workbench pads.
- Handle components and boards with care. Do not touch the components or contacts on a board. Hold a board by its edges or by its metal mounting bracket.
- Do not handle or store system boards near strong electrostatic, electromagnetic, magnetic, or radioactive fields.

2.2 AT8400 Initial Installation Procedures

The following procedures are applicable only for the initial installation of the AT8400 in a system. Procedures for standard removal and hot swap operations are found in their respective chapters.

To perform an initial installation of the AT8400 in a system proceed as follows:

1. Ensure that the safety requirements indicated in section 2.1. are observed.



Warning!

Failure to comply with the instruction below may cause damage to the board or result in improper system operation.

2. Ensure that the board is properly configured for operation in accordance with application requirements before installing. For information regarding the configuration of the AT8400 refer to Chapter 4.



Warning!

Care must be taken when applying the procedures below to ensure that neither the AT8400 nor other system boards are physically damaged by the application of these procedures.

3. To install the AT8400 perform the following:

   a. Carefully insert the board into the slot designated by the application requirements for the board until it makes contact with the backplane connectors.



Warning!

DO NOT push the board into the backplane connectors. Use the ejector handles to seat the board into the backplane connectors.

   b. Using the ejector handle, engage the board with the backplane. When the ejector handle is locked, the board is engaged.
   c. Fasten the front panel retaining screws.
   d. Connect all external interfacing cables to the board as required.
   e. Ensure that the board and all required interfacing cables are properly secured.

4. The AT8400 is now ready for operation.
5. For out-of-band management, GbE and SAS/SATA access, install the RTM8400 (see below).

2.3 Standard Removal Procedures

To remove the board proceed as follows:

1. Ensure that the safety requirements indicated in section 2.1. are observed.



Warning!

Care must be taken when applying the procedures below to ensure that neither the AT8400 nor system boards are physically damaged by the application of these procedures.

2. Unscrew the front panel retaining screws.
3. Push in and hold the ejector handles in a horizontal position to release the hot swap switch. The blue LED starts blinking.
4. Wait until the blue LED is fully ON, this mean that the hot swap sequence is ready for board removal.
5. Disengage the board from the backplane by using both board ejection handles.
6. After disengaging the board from the backplane, pull the board out of the slot.

2.4 AMC Installation

To install an AMC proceed as follows:

1. Remove the AMC filler panel.
2. Carefully engage the AMC into the card guide. Push the AMC until it fully mates with its connector. Secure the AMC handle to the locking position.
3. In normal condition, the blue LED shall turn ON as soon as the AMC is fully inserted. It will turn OFF at the end of the hot swap sequence.

2.5 RTM Installation

To install the Kontron RTM8400 proceed as follows:

1. Remove the RTM filler panel.
2. Carefully insert the board into the RTM slot corresponding to the front board slot of the AT8400 until it makes contact with the front board connectors.
3. Connect all external interfacing cables to the RTM as required.
4. Ensure that the RTM and all required interfacing cables are properly secured.

The features of the RTM8400 are described in detail in Chapter 3, section 3.2.

2.6 Software Installation

The AT8400 comes as a pre-installed system with all necessary OS, Filesystem, drivers and applications factory-installed with default configurations.

Updating the Software with new Operating System or applications or new versions is provided by a dedicated update mechanism, which is described in Chapter 4.

2.7 Quick Start

This section gives instructions for (initially) accessing the CLI (Command Line Interface) of the AT8400 using either in-band access via the base interface or the out-of-band management interfaces (Serial Console or the Fast Ethernet) of an appropriate RTM. The CLI is required for configuring the GbE switch, as well as the PCIe and SAS subsystem infrastructure. Some basic settings for PCIe and SAS port assignment are also described.

2.7.1 In-Band CLI Access

The GbE switch on the AT8400 is pre-configured with a management VLAN. This VLAN is accessible over the base fabric interface. Telnet accesses to port 23 of this VLAN connect to the CLI. The VLAN is configured for DHCP and retrieves its IP address automatically when a DHCP server is found in the network. The procedure to obtain the issued IP from the DHCP server is beyond the scope of this document.

The management VLAN is configured with VLAN ID 1. The following Ethernet ports are members of the management VLAN ID 1 by default:

- Interface 0/3 connected to base interface switch in ATCA logical slot 1
- Interface 0/9, 0/11, 0/13, 0/15 connected to AMC bay B4, B3, B2, B1 on channel 0

Thus connectivity to the management VLAN ID 1 is by default possible through the base interface switch in ATCA chassis logical slot 1.

For more information on the management VLAN and how to assign a fixed IP address, refer to the *“AT8400 CLI Reference Manual“*.

2.7.2 Out-of-band CLI Access

The CLI can also be accessed via serial console or Fast Ethernet with an appropriate RTM. The RTM needs to provide the serial and Fast Ethernet ports of the AT8400 front board. The serial console is ready to use offhand without further configuration.

To connect to the CLI via the Fast Ethernet serviceport on the RTM, a telnet session must be established to the IP address of this interface, port 23.

It is necessary to assign an IP address statically to the serviceport. Because the required configuration steps are done in the CLI, an initial access using the serial console or in-band connectivity via the base interface (see 2.7.1) is required. The procedure for assigning an IP address to the serviceport is described in the following. User input is printed in bold letters.

1. Connect to serial port on the RTM.

   Port settings are:
   - 9600 bps
   - 8 bit, no parity, 1 stop bit (8N1)
   - no flow control

2. Ensure that the board is powered up.

3. Wait for boot process to complete, i.e. until the console selection menu appears.

```
b - connect Base Fabric console
r - reset system
```

4. Type ’b’ to connect to the Base Fabric console.

```
Connected to Base Fabric console
Press ^X or ^V to get to  menu again
Base Fabric switching application release BETA 1.04 starting

(Unit 1)>

User:
```

5. Log in as admin and enter privileged mode by typing ’enable’ (no passwords required by default).

```
User:admin
Password:
(Ethernet Fabric) >enable
Password:

(Ethernet Fabric) #
```

6. Set IP address and netmask. (see below for an example IP address setting)

```
(Ethernet Fabric) #serviceport ip 192.168.50.107 255.255.255.0
```

   The FE management interface is available from now on.

7. Save configuration by copying it to the flash, confirm by typing ’y’

```
(Ethernet Fabric) #copy system:running-config nvram:startup-config

This operation may take a few minutes.
Management interfaces will not be available during this time.

Are you sure you want to save? (y/n) y

Configuration Saved!

(Ethernet Fabric) #
```

To access the CLI via Fast Ethernet management port, open a telnet connection to the configured IP address, port 23.

For additional information on the system configuration, refer to the “*AT8400 CLI Reference Manual*“.

2.7.3 PCIe Configuration

Default configuration is:

- Upstream port (root complex) at PCI Express switch PEX port 8 (AMC B2)
- No Non-transparent bridge port defined

To change the upstream port (and NT-bridge port), use the following CLI command in priviledged mode:

```
set board pcie upstream <port>
```

or

```
set board pcie upstream <port> nt-bridge <port>
```

Where `<port>` can be `amcb1`, `amcb2`, `amcb3`, `amcb4` or `update`.

After changing the upstream/NT port, the PCIe subsystem requires a reset. This can be done by deactivating and activating the AT8400 carrier.

For an overview of the current configuration, use the CLI boardinfo command:

```
(Ethernet Fabric) #show boardinfo pcie
PCIE port    Setting          Hot-Plug
==========  ================ ========

amcb1        downstream       disabled
amcb2        upstream         disabled
amcb3        downstream       disabled
amcb4        downstream       disabled
update       non-transparent  disabled

Clock setting: SSC
```

For additional information on the system configuration, refer to the "*AT8400 CLI Reference Manual*".

2.7.4 SAS Configuration

The LSISAS1064E SAS controller has firmware version 1.11.00 (Initiator/Target configuration) pre-installed. An alternative version (1.10.00) provides integrated RAID support.

The SASx12A edge expander has appropriate configuration data pre-installed. In this default configuration, all AMC bays are connected to the SAS Expander (SAS Connect).

To establish a storage connection between AMC bays 1 and 3 instead (Direct AMC Connect), use the following command:

```
set board storage connect amcb3 amcb1
```

To reset the configuration to the default settings for bays 1 and 3, use the following command:

```
set board storage connect amcb3 sas
```

To establish a storage connection between AMC bays 2 and 4, use the following command:

```
set board storage connect amcb4 amcb2
```

To reset the configuration to the default settings for bays 2 and 4, use the following command:

```
set board storage connect amcb4 sas
```

For an overview of the current configuration, use the CLI boardinfo command:

```
(Ethernet Fabric) #show boardinfo storage
Device: amcb3   connected to storage device: sas
Device: amcb4   connected to storage device: amcb2
```

For additional information on the system configuration, refer to the "*AT8400 CLI Reference Manual"* and application note #0005 (AT8400-AN-#0005-SAS-INFRASTRUCTURE.pdf).

2.7.5 AM4001 Installation

For information on AM4001 operation and SW installation, refer to the AM4001 User Manual. The LSISAS1064E SAS controller requires SAS Linux driver version 3.02.62-1 or higher.

Chapter 3

Hardware Description

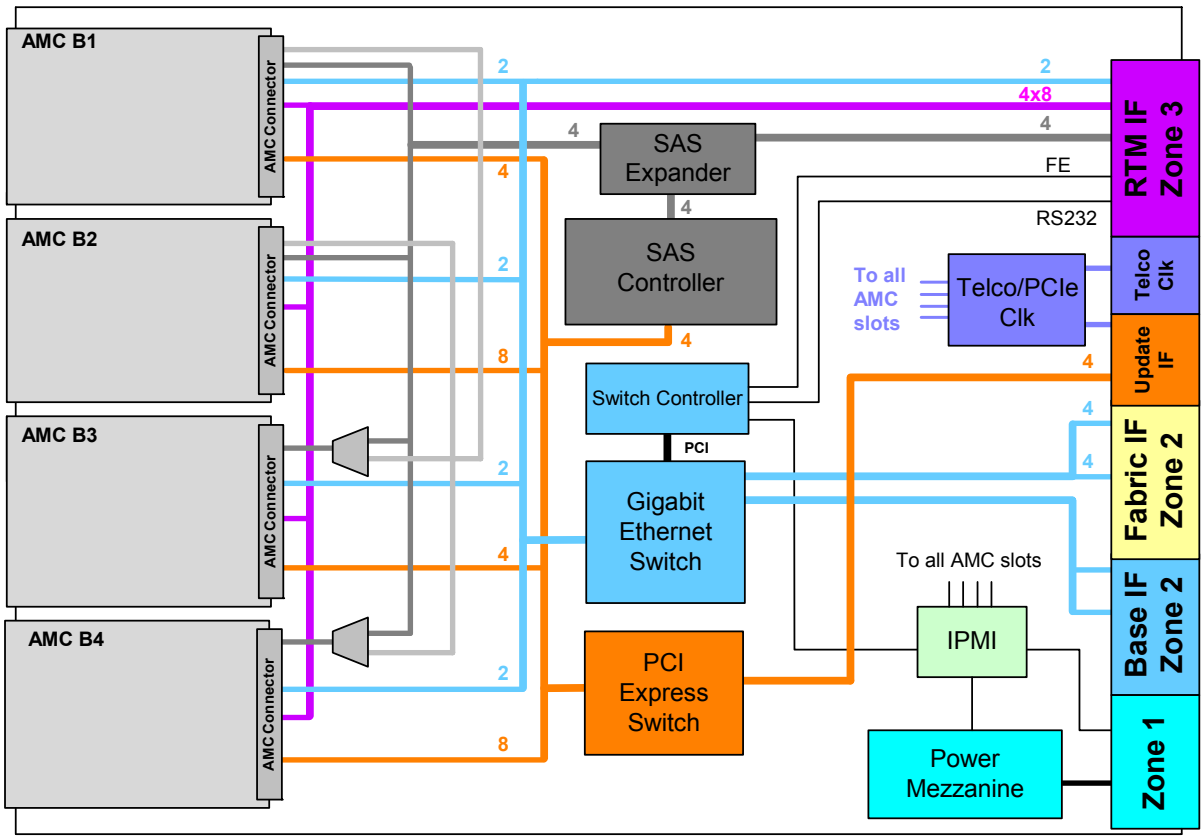
3. Hardware Description

This chapter describes the board specific items of the AdvancedTCA AMC Carrier Board AT8400 consisting of the main assembly with the Power Mezzanine Module. Also described is the RTM8400 used for management access and I/O extension.

3.1 Base Board

The base board is a PICMG 3.0 and 3.1 Option 2 compliant Carrier Board for AdvancedTCA shelves offering up to four AMC bays.

Figure 3-1: Functional Block Diagram Base Board



The main building blocks of the base board are:

- Ethernet Switch
- PCI Express Infrastructure
- SAS/SATA Infrastructure
- Ethernet Switch Controller and Memory
- Synchronous Clock Distribution
- AMC Bays
- IPMI
- RTM Interface
- Power Supply

3.1.1 Ethernet Switch

The main parts of the Ethernet Switch building block is a Broadcom BCM56305 20 port Gigabit Layer-2/3 Switch and a Broadcom BCM5466R QUAD 10/100/1000BASE-T PHY for the base and extension fabric interface, AMC and RTM Uplink connectivity. The BCM56305 is managed via the 32bit/33MHz PCI interface.

A BCM 5466R performs PHY functions for the 10/100/1000BASE-T ports of the RTM (GE1 and GE2) and the two base interface links.

The ports of the BCM56305 are assigned as follows:

Table 3-1: GbE Switch Port Assignment

CLI ID	Connection
0/1	RTM GE1
0/2	RTM GE2
0/3	Base Channel 1
0/4	Base Channel 2
0/5	Fabric Channel 2, Port 3
0/6	Fabric Channel 2, Port 2
0/7	Fabric Channel 2, Port 1
0/8	Fabric Channel 2, Port 0
0/9	AMC B4 Channel 0
0/10	AMC B4 Channel 1
0/11	AMC B3 Channel 0
0/12	AMC B3 Channel 1
0/13	AMC B2 Channel 0
0/14	AMC B2 Channel1
0/15	AMC B1 Channel 0
0/16	AMC B1 Channel 1

Table 3-1: GbE Switch Port Assignment (Continued)

CLI ID	Connection
0/17	Fabric Channel 1, Port 3
0/18	Fabric Channel 1, Port 2
0/19	Fabric Channel 1, Port 1
0/20	Fabric Channel 1, Port 0

3.1.2 PCI Express Infrastructure

The PCI Express Infrastructure consists of the PEX8532 PCI Express Switch with 32 lanes and up to 8 ports. It conforms to revision 1.0a of the PCI Express Base Specification. The generic switch settings are controlled from the IPMC via the CPLD.

Port numbering is according the PEX8532 numbering scheme.

Table 3-2: PEX8532 Lane Port Assignment

Port	Lane	Connection
0	0 to 7	AMC B4, Channel 4 to 11
1	8 to 11	AMC B3, Channel 4 to 7
2	12 to 15	ATCA Update Channel
8	16 to 23	AMC B2, Channel 4 to 11
9	24 to 27	AMC B1, Channel 4 to 7
10	28 to 31	SAS Controller

The default upstream port (root complex) is port 8 (AMC B2).

The PEX8532 reads the strapping signal pins to determine the selection of the system mode, the upstream port selected, and the lane configuration of all of the ports. The mode and lane configuration are fixed, the upstream port and the transparent bridge port are predefined by the IPMC via the CPLD. Any change in the strapping settings requires a reset of the PEX8532.

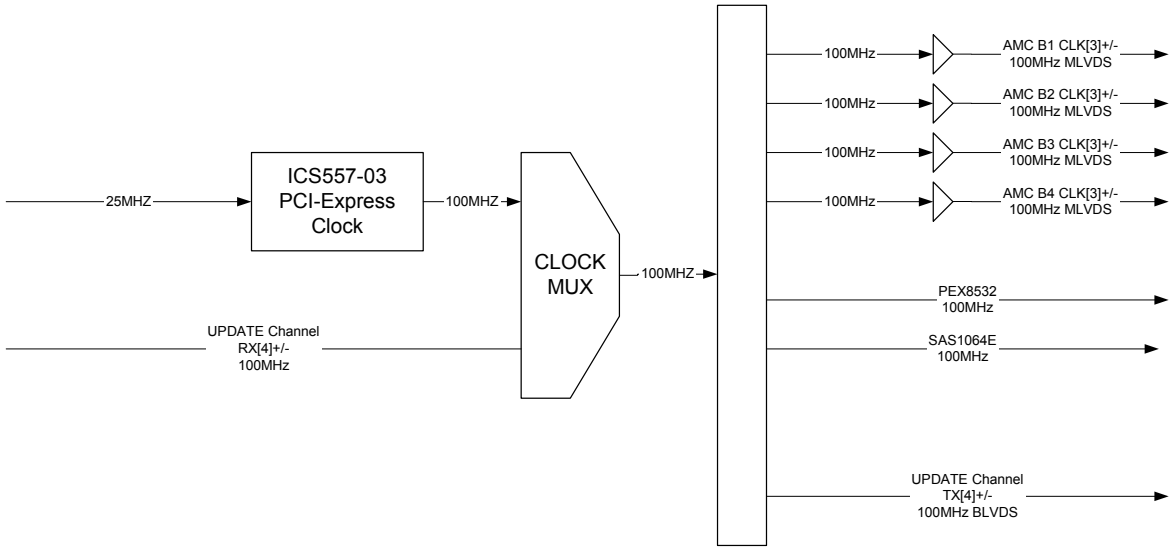
A serial EEPROM is attached to the PEX8532 for optional startup configuration data. It is not used by default.

The IPMC controls the Hot Swap controller of each PCI Express port. This allows orderly insertion and extraction of PCI Express AMCs from the running system without adversely affecting the system.

The PCI Express Clock distribution generates 100MHz according the PCI Express Base Specification 1.0a or distributes 100MHz received from Zone 2 Update Channel 4.

The modes and clock distribution are controlled by the IPMC.

Figure 3-2: PCI Express Clock Distribution Block Diagram



For details on how to configure the PCI Express Clock Distribution, refer to the CLI Reference Manual.

3.1.3 SAS/SATA Infrastructure

The major components of the SAS/SATA infrastructure are the LSI SAS1064E PCI Express to 4-Port Serial Attached SCSI Controller and the LSI SASx12A 3.0 Gbit/s Serial Attached SCSI Expander. Two 3.0 Gbit/s port selectors configure the AMC Bays' storage connections.

3.1.3.1 SAS Controller

The LSISAS1064E is a four-port 3.0Gbit/s SAS/SATA controller that is compliant with Fusion-MPT TM architecture, provides a four lane PCI Express interface, and supports the Integrated RAID TM solution. Each SAS/SATA lane supports 3.0Gbit/s and 1.5Gbit/s data rate transfer.

The LSISAS1064E is controlled via the PEX8532 PCI Express switch from the root complex. The four SAS/SATA lanes are connected to the LSISASx12A Expander.

The controller has a 32-bit external memory bus with 2MB Flash ROM and 32KB NVSRAM attached. The Flash ROM stores firmware configuration information, persistent data information and the PCI configuration data. The NVSRAM stores write journaling information when Integrated Mirroring (IM) is activated in an Integrated Raid implementation.

The LSISAS1064E die temperature is monitored by an integrated temperature sensor.

3.1.3.2 SAS Expander

The LSISASx12A is a 12-port Serial Attached SCSI (SAS) expander that supports 3.0 Gbit/s and 1.5 Gbit/s SAS and SATA data rate transfers.

The boot record for the LSISASx12A is stored in a serial EEPROM.

The LSISASx12A die temperature is monitored by an internal temperature sensor.

3.1.3.3 AMC Storage Connections

Two port selectors are used to configure either a storage connection between the AMC slots and the SAS Expander (SAS Connect) or between pairs of AMC slots (Direct AMC Connect). This is required to enable direct connections between AMCs with a SATA host and a SATA target. The first selector is used to enable direct SATA connection between AMC B1 and AMC B3 and the second one is used to enable direct SATA connection between AMC B2 and AMC B4. Both port selectors are controlled by the IPMC and can be configured independently from each other.

The table below shows the port assignment of the SAS Expander devices.

Table 3-3: SAS Expander Port Assignment

Channel	Connection
0	AMC B3 Channel 2*
1	AMC B4 Channel 2*
2	SAS Controller Port 0
3	SAS Controller Port 1
4	SAS Controller Port 2
5	SAS Controller Port 3
6	RTM, STOR3
7	RTM, STOR2
8	RTM, STOR1
9	RTM, STOR0
10	AMC B1 Channel 2
11	AMC B2 Channel 2

* Configured for SAS Connect

Depending on whether the port selectors are configured for SAS Connect or Direct AMC Connect, the SAS/SATA channels of the four AMC bays are interconnected as follows:

Table 3-4: AMC Storage Interconnect

AMC Channel	SAS Connect	Direct AMC Connect
B1 Channel 2	SAS Expander Port 10	SAS Expander Port 10
B1 Channel 3	-	B3 Channel 2
B2 Channel 2	SAS Expander Port 11	SAS Expander Port 11
B2 Channel 3	-	B4 Channel 2
B3 Channel 2	SAS Expander Port 0	B1 Channel 3
B3 Channel 3	-	-
B4 Channel 2	SAS Expander Port 1	B2 Channel 3
B4 Channel 3	-	-

For more information on how to configure the AMC Storage connections, refer to the CLI Reference Manual.

3.1.4 Ethernet Switch Controller and Memory

A PowerPC PPC405GP-133MHz 32 bit RISC processor with 16KB D-cache, 128MB SDRAM and 32MB Flash memory manages the Ethernet switch via 32bit / 66MHZ PCI local bus. The CPU is accessible with UART or 10/100BASE-T Ethernet from the RTM or in-band via the GbE switch.

3.1.4.1 PCI Interface

The PCI interface is a 32bit/66MHz system to control the on-board Broadcom BCM56305 base interface switch. The internal PCI arbiter of the PowerPC 405 GP is used.

The switch is located at virtual PCI slot 1, IDSEL 0.

3.1.4.2 Fast Ethernet Management Interface

The internal Fast Ethernet MAC of the PowerPC 405 GP is used as a management interface. Additionally a Fast Ethernet PHY transceiver and a RJ45 Connector with integrated magnetics and two LED's, located on the RTM, are used to complete the network interface.

The PHY is controlled via the MDIO interface of the PowerPC 405 GP. The MDIO address is set to 0. The default setting of the PHY is to operate in auto-negotiation enabled mode, 10/100, Full or Half duplex.

The Fast Ethernet Management Interface uses the following pins of the ATCA Zone 3 connector:

Table 3-5: Fast Ethernet Pins on RTM Connector

J30 Pin	Function
E1	MNG_LAN_DA-
F2	MNG_LAN_DA+
F1	MNG_LAN_DB-
F2	MNG_LAN_DB+

3.1.4.3 RS232 Management Interface

One RS232 interface (UART0) of the PowerPC 405 GP is connected to the RTM connector, the other one (UART1) is used as programming interface for IPMI.

The RS232 Management Interface uses the following pins of the ATCA Zone 3 connector:

Table 3-6: RS232 Pins on RTM Connector

J30 Pin	Function
A9	RI
A10	RTS
B9	DTR
B10	RXD
C9	CTS
C10	DSR
D9	TXD
D10	CD

3.1.4.4 SDRAM

Five 256 Mbit devices, soldered directly onto the PCB, provide 128 MByte of SDRAM plus 32 MByte for ECC.

The SDRAM interface of the PPC is 32 bit wide and operated at 133 MHz.

3.1.4.5 Flash ROM

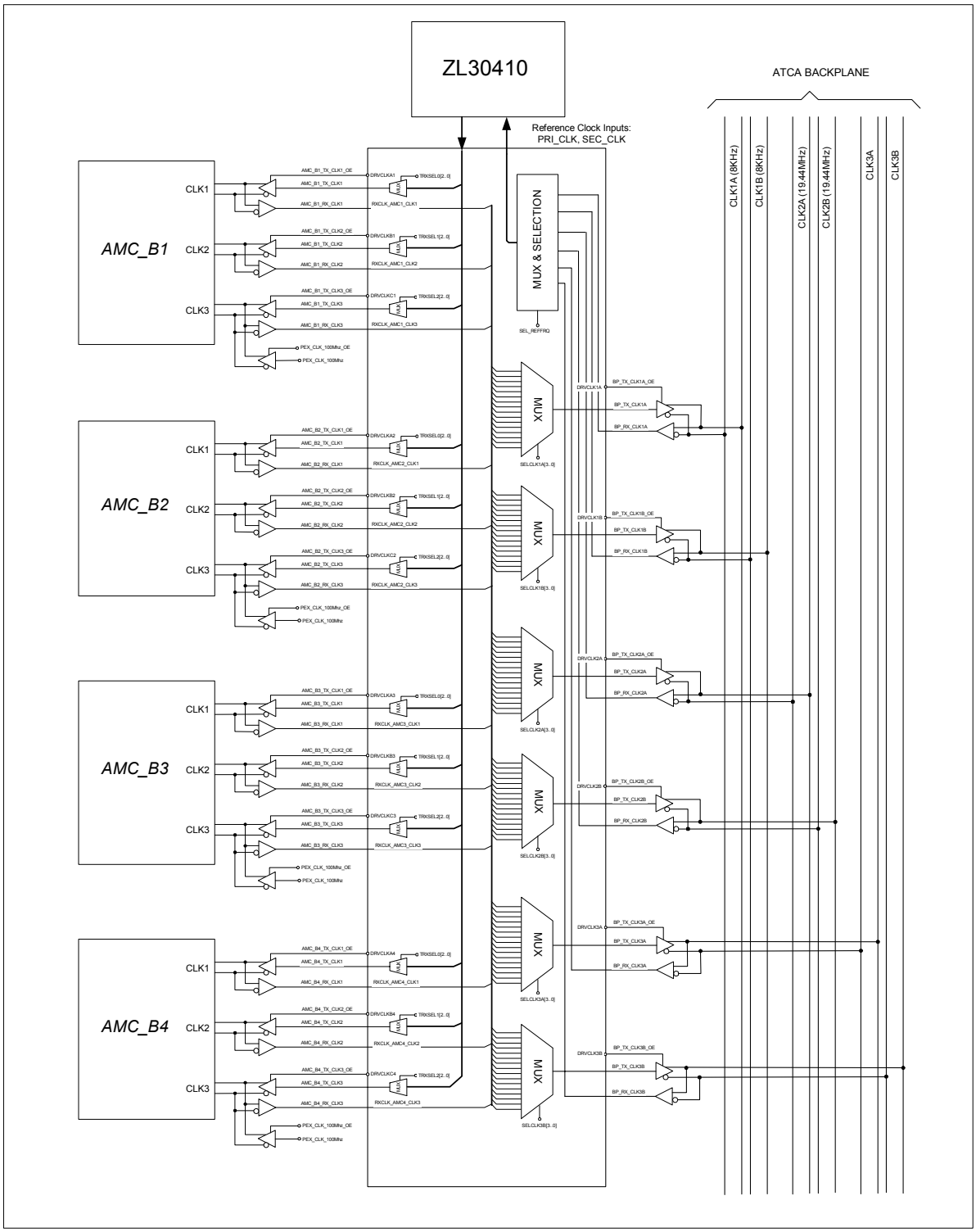
The CPU uses a 32 Mbyte Flash Memory device. Sector width is 128 Kbyte. The Flash ROM is connected to the lower 16 bit of the 32 bit peripheral data bus. The sectors containing the bootloader code are write protected, which can be disabled by setting jumper FWPD.

3.1.5 Synchronous Clock Distribution

The Clock CPLD is the global Clock distribution device on the carrier board. In conjunction with the Zarlink ZL30410 protection switch, the CPLD distributes all necessary Telecom clocks to or from the AMCs and the Backplane.

The following block diagram shows all possibilities to distribute any clock.

Figure 3-3: Block Diagram Synchronous Clock Distribution



It is generally possible to distribute all clocks in both directions. I.e. all clock signals received from the Zarlink protection switch can be driven by the CPLD to all AMC modules. It is also possible to route any clock from any AMC module to the ATCA backplane. Any ATCA backplane clock can be used as the Zarlink reference clock input. All four AMC CLK3 signals can also be driven by the PCI Express 100 MHz reference clock.

For more information on how to configure the clock distribution, refer to the AT8400 CLI Reference.

3.1.6 AMC Bays

Up to four full height and single width or up to two full height double width AMC bays for standard or custom AMCs are implemented with B+ AMC connectors, depending on the board option.

Table 3-7: AMC Slot Types

Board option	B1	B2	B3	B4
A	Single width AMC.1 Type 4E2S2	Single width AMC.1 Type 8E2S2	Single width AMC.1 Type 4E2S1	Single width AMC.1 Type 8E2S1
B	-	Double width AMC.1 Type 8E2S2	-	Double width AMC.1 Type 8E2S1
C	-	Double width AMC.1 Type 8E2S2	Single width AMC.1 Type 4E2S1	Single width AMC.1 Type 8E2S1
D	Single width AMC.1 Type 4E2S2	Single width AMC.1 Type 8E2S2	-	Double width AMC.1 Type 8E2S1

Both Telecom clocks and PCI Express clock are supported on each AMC Bay.

Because of the AMC slot storage interconnects (see section 3.1.3.3) and for thermal reasons, the preferred Processor AMC slots are B1 and B2 and the preferred HDD-AMC slots are B3 and B4. The PCI Express root complex is attached to port B2 by default.

Following AMC Geographic Addresses are implemeted:

Table 3-8: AMC Bay Address

AMC Bay ID	GA[2..0]	IPMB-L Address
B1	UGU	7Ah
B2	UUG	7Ch
B3	UUP	7Eh
B4	UPU	80h

The state of each GA signal is represented by G (grounded), U (unconnected) or P (pulled up to management power)

Table 3-9: AMC B1 Channel Assignment

Channel	Region	Connection
0	GbE	GbE Switch 0/15
1	GbE	GbE Switch 0/16
2	SAS/SATA	SAS Expander Port 10
3	SAS/SATA	-* AMC B3 Channel 2**
4	Fabric	PCI Express Switch Port 9, Lane 0
5	Fabric	PCI Express Switch Port 9, Lane 1
6	Fabric	PCI Express Switch Port 9, Lane 2
7	Fabric	PCI Express Switch Port 9, Lane 3
8	Fabric	-
9	Fabric	-
10	Fabric	-
11	Fabric	-
12	-	-
13	Extended	RTM, AMC_B1_P13
14	Extended	RTM, AMC_B1_P14
15	Extended	RTM, AMC_B1_P15
16	Extended	RTM, AMC_B1_P16
17	Extended	RTM, AMC_B1_P17
18	Extended	RTM, AMC_B1_P18
19	Extended	RTM, AMC_B1_P19
20	Extended	RTM, AMC_B1_P20

* Configured for SAS Connect

** Configured for Direct AMC Connect

Table 3-10: AMC B2 Channel Assignment

Channel	Region	Connection
0	GbE	GbE Switch 0/13
1	GbE	GbE Switch 0/14
2	SAS/SATA	SAS Expander Port 11
3	SAS/SATA	-* AMC B4 Channel 2**
4	Fabric	PCI Express Switch Port 8, Lane 0
5	Fabric	PCI Express Switch Port 8, Lane 1
6	Fabric	PCI Express Switch Port 8, Lane 2
7	Fabric	PCI Express Switch Port 8, Lane 3
8	Fabric	PCI Express Switch Port 8, Lane 4
9	Fabric	PCI Express Switch Port 8, Lane 5
10	Fabric	PCI Express Switch Port 8, Lane 6
11	Fabric	PCI Express Switch Port 8, Lane 7
12	-	-
13	Extended	RTM, AMC_B2_P13

Table 3-10: AMC B2 Channel Assignment (Continued)

Channel	Region	Connection
14	Extended	RTM, AMC_B2_P14
15	Extended	RTM, AMC_B2_P15
16	Extended	RTM, AMC_B2_P16
17	Extended	RTM, AMC_B2_P17
18	Extended	RTM, AMC_B2_P18
19	Extended	RTM, AMC_B2_P19
20	Extended	RTM, AMC_B2_P20

* Configured for SAS Connect

** Configured for Direct AMC Connect

Table 3-11: AMC B3 Channel Assignment

Channel	Region	Connection
0	GbE	GbE Switch 0/11
1	GbE	GbE Switch 0/12
2	SAS/SATA	SAS Expander Port 0* AMC B1 Channel 3**
3	SAS/SATA	-
4	Fabric	PCI Express Switch Port 1, Lane 0
5	Fabric	PCI Express Switch Port 1, Lane 1
6	Fabric	PCI Express Switch Port 1, Lane 2
7	Fabric	PCI Express Switch Port 1, Lane 3
8	Fabric	-
9	Fabric	-
10	Fabric	-
11	Fabric	-
12	-	-
13	Extended	RTM, AMC_B3_P13
14	Extended	RTM, AMC_B3_P14
15	Extended	RTM, AMC_B3_P15
16	Extended	RTM, AMC_B3_P16
17	Extended	RTM, AMC_B3_P17
18	Extended	RTM, AMC_B3_P18
19	Extended	RTM, AMC_B3_P19
20	Extended	RTM, AMC_B3_P20

* Configured for SAS Connect

** Configured for Direct AMC Connect

Table 3-12: AMC B4 Channel Assignment

Channel	Region	Connection
0	GbE	GbE Switch 0/9
1	GbE	GbE Switch 0/10
2	SAS/SATA	SAS Expander Port 1* AMC B2 Channel 3**
3	SAS/SATA	-
4	Fabric	PCI Express Switch Port 0, Lane 0
5	Fabric	PCI Express Switch Port 0, Lane 1
6	Fabric	PCI Express Switch Port 0, Lane 2
7	Fabric	PCI Express Switch Port 0, Lane 3
8	Fabric	PCI Express Switch Port 0, Lane 4
9	Fabric	PCI Express Switch Port 0, Lane 5
10	Fabric	PCI Express Switch Port 0, Lane 6
11	Fabric	PCI Express Switch Port 0, Lane 7
12	-	-
13	Extended	RTM, AMC_B4_P13
14	Extended	RTM, AMC_B4_P14
15	Extended	RTM, AMC_B4_P15
16	Extended	RTM, AMC_B4_P16
17	Extended	RTM, AMC_B4_P17
18	Extended	RTM, AMC_B4_P18
19	Extended	RTM, AMC_B4_P19
20	Extended	RTM, AMC_B4_P20

* Configured for SAS Connect

** Configured for Direct AMC Connect

AMC GbE Channels

Channels 0 and 1 of each AMC are connected to the Ethernet Switch. The Ethernet Switch supports 1000BASE-BX Gigabit Ethernet.

AMC SAS/SATA

Channels 2 and 3 of the AMC slots are reserved for SAS. All four AMC are connected to the SAS Expander. Additionally, a direct SATA interconnect between B1 and B3 is configurable, as well as between B2 and B4 (see section 3.1.3.3).

AMC PCI Express

Bays B1 and B3 implement a x4 PCIe connection on channels 4 to 7. B2 and B4 implement a x8 connection (channels 4 to 11). All slots are directly connected to the PCI Express switch.

Interconnects to RTM

Each AMC Bay has eight generic interconnects to the RTM Zone 3 (channels 13 to 20).

3.1.7 IPMI

The AT8400 supports an intelligent hardware management system based on the Intelligent Platform Management Interface (IPMI) Specification 1.5. The hardware management system provides the ability to manage the power, cooling and interconnect needs of intelligent devices, to monitor events and to log events to a central repository.

The main building blocks of the IPMI architecture of the AT8400 are:

- IPMC Intelligent Platform Management Controller
- FUM Firmware Update Manager
- CPLD Complex Programmable Logical Device

For further details please refer PICMG 3.0 standard Rev. 2.0.

3.1.7.1 IPMC

The IPM controller is a 16-bit microcontroller for IPMI applications with 512 Kbyte Flash and 40 Kbyte SRAM. It is compliant to IPMI version 1.5 specification. The microcontroller provides I²C interfaces to have access to the dedicated ShMCs, the AMCs, the RTM and the on board peripheral devices such as SEEPROM, temperature sensors and others. The microcontroller also provides three serial interfaces that are connected to the CPLD.

An LPC interface using the KCS protocol for communication between IPMC and PPC is implemented by the CPLD. IPMC operation is supervised by the FUM.

3.1.7.2 FUM

The Firmware Update Manager (FUM) is a microcontroller with 16 Kbyte data flash ROM and 1Kbyte RAM.

The FUM is responsible for field upgrades, rollbacks and watchdog functions of the IPM controller. Four SPI compatible memory devices are connected to the FUM which build up two IPMI firmware banks with 512 Kbyte each. One bank contains a copy of the current IPMC code. The other bank can be written without affecting IPMC operation. Once the bank is updated, the FUM writes its content into the IPMC. IPMC control signals are all buffered in the CPLD so that board operation is not affected during update. In the case of a fault during the update process, the FUM can configure the IPMC with the old firmware that is kept in the other bank. The FUM is also the watchdog timer for the IPMC. There are several control signals to supervise the IPM controller.

3.1.7.3 CPLDs

The Clock CPLD implements the Synchronous Clock Distribution (see section 3.1.5) and the Control CPLD is part of the board management. They are responsible for connecting the PPC to the IPMC and FUM and for handling the serial interfaces of PPC, IPMC and FUM to the RS232 connector on the front panel. The host interface between PowerPC and CPLD, realized by PPC's External Bus Interface (EBC), is used as CPLD-Register-Interface and as communication interface to IPM controller. The EBC is configured as a demultiplexed 8 Bit Address/Data interface. For accesses to the IPMC Controller, an EBC to LPC (Low Pin Count)-Bridge is included as protocol interface. The LPC interface is for communication between IPMC and PPC over KCS protocol.

The CPLD controls the LEDs for the whole board via shift registers. It handles the signals to monitor the AMCs and the RTM and handles the signals for the line drivers for the synchronization clocks.

An internal multiplexer controls the serial interfaces from the PPC, the FUM and the IPMC. It is possible to connect each device to the other or to the RS232 connector on the RTM.

3.1.8 RTM Interface

Management and I/O interfaces from the Base Board are routed to Zone 3 where a connector mates with the RTM. This allows Base Boards to be quickly and reliably serviced without the issues associated with disconnecting and reconnecting multiple cable assemblies. The RTM connection is compliant to the PICMG 3.0 standard.

For the connection between the AT8400 and the RTM, three connectors with 40 differential pairs are used (J30, J31 and J32).

Each AMC Bay has eight generic interconnects to the RTM Zone 3. Four SAS/SATA interfaces for mass storage are implemented. There is a JTAG connection for CPLD update or Boundary Scan-Test. An I²C IPMI interface is implemented for board management. The PPC405GP management interfaces (Fast Ethernet and RS232) are also connected to the RTM. Two GbE ports allow connection to the GbE switch.

For more information on the RTM8400, refer to section 3.2.

The Zone 3 connectors have the following pin assignments.

Table 3-13: J30 Assignment

J30	ROW A	AB	ROW B	ROW C	CD	ROW D
1	N.C.	GND	N.C.	N.C.	GND	N.C.
2	PROD_IO0	GND	PROD_IO1	N.C.	GND	N.C.
3	12V	GND	3V3_SUS	SMB_SCL	GND	SMB_SDA
4	PROD_IO2	GND	PLD_DOUT	PLD_CLOCK	GND	PLD_DIN
5	JTAG_TDO	GND	TEST_JIG#	N.C.	GND	PROD_IO3
6	JTAG_TDI	GND	12V	N.C.	GND	N.C.
7	JTAG_TCK	GND	PROD_IO4	N.C.	GND	N.C.
8	JTAG_TMS	GND	JTAG_TRST#	N.C.	GND	N.C.
9	SP_RI	GND	SP_DTR	SP_CTS	GND	SP_TX#
10	SP_RTS	GND	SP_RX#	SP_DSR	GND	SP_DCD
J30	**ROW E**	**EF**	**ROW F**	**ROW G**	**GH**	**ROW H**
1	MNG_LAN_DA-	GND	MNG_LAN_DA+	STOR0_RX-	GND	STOR0_RX+
2	MNG_LAN_DB-	GND	MNG_LAN_DB+	STOR0_TX-	GND	STOR0_TX+
3	N.C.	GND	N.C.	STOR1_RX-	GND	STOR1_RX+
4	N.C.	GND	N.C.	STOR1_TX-	GND	STOR1_TX+
5	N.C.	GND	GLAN_AB_CT	STOR2_RX-	GND	STOR2_RX+
6	MNG_LAN_CT	GND	12V	STOR2_TX-	GND	STOR2_TX+
7	N.C.	GND	N.C.	STOR3_RX-	GND	STOR3_RX+
8	N.C.	GND	SMB_ALRT#	STOR3_TX-	GND	STOR3_TX+
9	N.C.	GND	N.C.	N.C.	GND	N.C.
10	N.C.	GND	N.C.	N.C.	GND	N.C.

Table 3-14: J31 Assignment

J31	ROW A	AB	ROW B	ROW C	CD	ROW D
1	RTM_GE1_DA+	GND	RTM_GE1_DA-	RTM_GE1_DB+	GND	RTM_GE1_DB-
2	RTM_GE2_DA+	GND	RTM_GE2_DA-	RTM_GE2_DB+	GND	RTM_GE2_DB-
3	N.C.	GND	N.C.	N.C.	GND	N.C.
4	N.C.	GND	N.C.	N.C.	GND	N.C.
5	AMC_B1_P13_TX+	GND	AMC_B1_P13_TX-	AMC_B1_P13_RX+	GND	AMC_B1_P13_RX-
6	AMC_B1_P15_TX+	GND	AMC_B1_P15_TX-	AMC_B1_P15_RX+	GND	AMC_B1_P15_RX-
7	AMC_B1_P17_TX+	GND	AMC_B1_P17_TX-	AMC_B1_P17_RX+	GND	AMC_B1_P17_RX-
8	AMC_B1_P19_TX+	GND	AMC_B1_P19_TX-	AMC_B1_P19_RX+	GND	AMC_B1_P19_RX-
9	AMC_B2_P17_TX+	GND	AMC_B2_P17_TX-	AMC_B2_P17_RX+	GND	AMC_B2_P17_RX-
10	AMC_B2_P19_TX+	GND	AMC_B2_P19_TX-	AMC_B2_P19_RX+	GND	AMC_B2_P19_RX-
J31	**ROW E**	**EF**	**ROW F**	**ROW G**	**GH**	**ROW H**
1	RTM_GE1_DC+	GND	RTM_GE1_DC-	RTM_GE1_DD+	GND	RTM_GE1_DD-
2	RTM_GE2_DC+	GND	RTM_GE2_DC-	RTM_GE2_DD+	GND	RTM_GE2_DD-
3	N.C.	GND	N.C.	N.C.	GND	N.C.
4	N.C.	GND	N.C.	N.C.	GND	N.C.
5	AMC_B1_P14_TX+	GND	AMC_B1_P14_TX-	AMC_B1_P14_RX+	GND	AMC_B1_P14_RX-
6	AMC_B1_P16_TX+	GND	AMC_B1_P16_TX-	AMC_B1_P16_RX+	GND	AMC_B1_P16_RX-
7	AMC_B1_P18_TX+	GND	AMC_B1_P18_TX-	AMC_B1_P18_RX+	GND	AMC_B1_P18_RX-
8	AMC_B1_P20_TX+	GND	AMC_B1_P20_TX-	AMC_B1_P20_RX+	GND	AMC_B1_P20_RX-
9	AMC_B2_P18_TX+	GND	AMC_B2_P18_TX-	AMC_B2_P18_RX+	GND	AMC_B2_P18_RX-
10	AMC_B2_P20_TX+	GND	AMC_B2_P20_TX-	AMC_B2_P20_RX+	GND	AMC_B2_P20_RX-

Table 3-15: J32 Assignment

J32	ROW A	AB	ROW B	ROW C	CD	ROW D
1	AMC_B2_P13_TX+	GND	AMC_B2_P13_TX-	AMC_B2_P13_RX+	GND	AMC_B2_P13_RX-
2	AMC_B2_P15_TX+	GND	AMC_B2_P15_TX-	AMC_B2_P15_RX+	GND	AMC_B2_P15_RX-
3	AMC_B3_P13_TX+	GND	AMC_B3_P13_TX-	AMC_B3_P13_RX+	GND	AMC_B3_P13_RX-
4	AMC_B3_P15_TX+	GND	AMC_B3_P15_TX-	AMC_B3_P15_RX+	GND	AMC_B3_P15_RX-
5	AMC_B3_P17_TX+	GND	AMC_B3_P17_TX-	AMC_B3_P17_RX+	GND	AMC_B3_P17_RX-
6	AMC_B3_P19_TX+	GND	AMC_B3_P19_TX-	AMC_B3_P19_RX+	GND	AMC_B3_P19_RX-
7	AMC_B4_P13_TX+	GND	AMC_B4_P13_TX-	AMC_B4_P13_RX+	GND	AMC_B4_P13_RX-
8	AMC_B4_P15_TX+	GND	AMC_B4_P15_TX-	AMC_B4_P15_RX+	GND	AMC_B4_P15_RX-
9	AMC_B4_P17_TX+	GND	AMC_B4_P17_TX-	AMC_B4_P17_RX+	GND	AMC_B4_P17_RX-
10	AMC_B4_P19_TX+	GND	AMC_B4_P19_TX-	AMC_B4_P19_RX+	GND	AMC_B4_P19_RX-
J32	**ROW E**	**EF**	**ROW F**	**ROW G**	**GH**	**ROW H**
1	AMC_B2_P14_TX+	GND	AMC_B2_P14_TX-	AMC_B2_P14_RX+	GND	AMC_B2_P14_RX-
2	AMC_B2_P16_TX+	GND	AMC_B2_P16_TX-	AMC_B2_P16_RX+	GND	AMC_B2_P16_RX-
3	AMC_B3_P14_TX+	GND	AMC_B3_P14_TX-	AMC_B3_P14_RX+	GND	AMC_B3_P14_RX-
4	AMC_B3_P16_TX+	GND	AMC_B3_P16_TX-	AMC_B3_P16_RX+	GND	AMC_B3_P16_RX-
5	AMC_B3_P18_TX+	GND	AMC_B3_P18_TX-	AMC_B3_P18_RX+	GND	AMC_B3_P18_RX-
6	AMC_B3_P20_TX+	GND	AMC_B3_P20_TX-	AMC_B3_P20_RX+	GND	AMC_B3_P20_RX-
7	AMC_B4_P14_TX+	GND	AMC_B4_P14_TX-	AMC_B4_P14_RX+	GND	AMC_B4_P14_RX-
8	AMC_B4_P16_TX+	GND	AMC_B4_P16_TX-	AMC_B4_P16_RX+	GND	AMC_B4_P16_RX-
9	AMC_B4_P18_TX+	GND	AMC_B4_P18_TX-	AMC_B4_P18_RX+	GND	AMC_B4_P18_RX-
10	AMC_B4_P20_TX+	GND	AMC_B4_P20_TX-	AMC_B4_P20_RX+	GND	AMC_B4_P20_RX-

Signals with TX in their name are driven by the front board, those with RX are driven by the RTM.

3.1.9 Power Supply

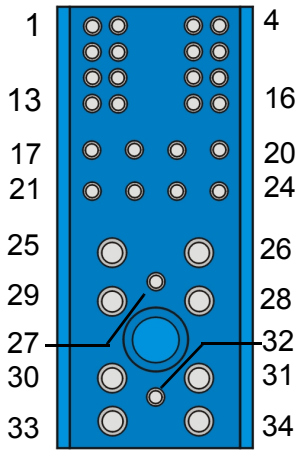
The power supply fulfils the PICMG3.0 requirements and has the following characteristics:

- Full operation at -38VDC to -72VDC
- No damage inflicted to board at 0VDC to -75VDC
- Typical payload power consumption (no RTM, no AMCs): 40W
- Maximum payload power consumption (no RTM, no AMCs): 51W
- Management power consumption (suspend power): 7W
- Additional AMC payload power consumption: 161W

3.1.9.1 Power Connector

The power connector supplies the board with two 48V redundant rails, digital ground and chassis ground. It also provides the redundant IPMB Shelf Manager connection.

Table 3-16: Power Connector (P10)

Signal	Pin		Pin	Signal
N.C.	1		2	N.C.
N.C.	3		4	N.C.
HA0	5		6	HA1
HA2	7		8	HA3
HA4	9		10	HA4
HA6	11		12	HA5
SCL_A	13		14	SDA_A
SCL_B	15		16	SDA_B
MT1_TIP(N.C.)	17		18	MT2_TIP(N.C.)
RING_A(N.C.)	19		20	RING_B(N.C.)
MT1_RING(N.C.)	21		22	MT2_RING(N.C.)
RRTN_A(N.C.)	23		24	RRTN_B(N.C.)
SHELF_GND	25		26	LOGIC_GND
ENABLE_B	27		28	VRTN_A
VRTN_B	29		30	EARLY_A
EARLY_B	31		32	ENABLE_A
-48V_A	33		34	-48V_B

3.1.9.2 Power Supply Mezzanine

The Filter, the Hot-Swap-Controller, the Hold Over circuit and the Quarter-Brick are situated on the Power Supply Mezzanine Module. The Power Supply Mezzanine is connected to the Carrier Board with the J4 connector.

Table 3-17: Pin Assignment Connector J4

Pin	Description	Pin	Description	Pin	Description	Pin	Description
1	V_12V_MODULE	12	GND	23	ENABLE_A	34	CGND_F
2	GND	13	V_12V_MODULE	24	I2C_SCL	35	RTN_B
3	V_12V_MODULE	14	GND	25	ENABLE_B	36	CGND_F
4	GND	15	V_3V3_SUS_MODULE	26	V_12V_EN#	37	V_-48V_A
5	V_12V_MODULE	16	GND	27	V_-48V_EARLY_OR	38	CGND_F
6	GND	17	V_3V3_SUS_MODULE	28	BLOW_FUSE#	39	V_-48V_A
7	V_12V_MODULE	18	GND	29	RTN_A	40	N.C.
8	GND	19	FEED_LOST#	30	CGND_F	41	V_-48V_B
9	V_12V_MODULE	20	GND	31	RTN_A	42	N.C.
10	GND	21	N.C.	32	CGND_F	43	V_-48V_B
11	V_12V_MODULE	22	I2C_SDA	33	RTN_B	44	N.C

3.1.9.3 Power Distribution

The 48 Volts are supplied by the backplane via two independent rails, primary (A) and secondary (B). The rails are mixed using power Schottky rectifiers. A 7A fuse protects each -48V line and a 10A fuse protects each RTN line. A hot swap controller enables the 48V power to the board.

On the mezzanine module, a quarter brick DC/DC converter transforms the 48 Volts to secondary 12 Volts for payload supply and 3.3 Volts for management supply.

Two further management voltages (5V and 1.8V) and six payload voltages (1.0V, 1.2V, 1.25V, 1.5V, 2.5V and 3.3V) are generated by point of load converters from the secondary voltages.

The management (or suspend) power is present once the board is connected to the backplane. It supplies the IPMI part which in turn controls the payload power. The various payload voltages are sequenced. The initial power up sequence is as follows (1ms delay between steps):

1. V_1V0
2. V_VCORE, V_1V5
3. V_3V3
4. V_2V5
5. V_1V25
6. V_1V2

The power down sequence is performed in reversed order with a 1ms delay.

3.1.9.4 Power Supply AMCs

Each AMC has its own power supply. The 12V payload power is generated by a hot swap controller and for the 3V3 management power a current limit switch is used. The maximum power dissipation for an AMC is 60W.

For further details please refer the AMC Specification.

3.1.9.5 Power Supply RTM

The RTM has its own power supply. The 12V payload power is generated by a hot swap controller and for the management power a current limit switch is used. The maximum power dissipation for an RTM is 10W.

For further details please refer the PICMG 3.0 standard.

3.1.9.6 Power Transients

The board provides continuous operation in the presence of transients shown in the following table of the PICMG 3.0 standard:

Table 3-18: Power Transients

Voltage	Duration	Comments	Protected by
- 200 Volts	5 µs	- 100 to - 200 Volts	Frame or Shelf
- 100 Volts	10 µs	- 75 to - 100 Volts	Board
- 75 Volts	10 ms	10 Volts per ms-Rise or Fall	Board
- 0 Volts	5 ms	50 Volts per ms-Fall 12.5 Volts per ms-Rise Assumes prior voltage is above -44 VDC for Shelves, -43 VDC for Boards	Board

In case of a 0V transient the board is able to keep the board alive for 5ms. The necessary energy is buffered in a capacitor.

3.1.9.7 Optional Chassis to Logic Ground Connection

According to NEBS requirement R9-14 of GR-1089-CORE issue 3, the AT8400 provides a connection between chassis and logic ground. It is made up of a screw that connects the PCB to the bottom sheet.

If chassis and logic ground shall be isolated, the screw with its washer can be removed. It is located near the jumper header J33 and is labelled "GND TO CHASSIS".

3.1.10 Jumpers

Six jumpers in the upper right corner allow debug settings (J33). The IPMI and PCIe E-Keying override jumpers enable bypassing communication with the ShMC for bench operation. The JTAG jumpers configure the boundary scan path. JTAG operation requires the use of the RTM8400.



Warning!

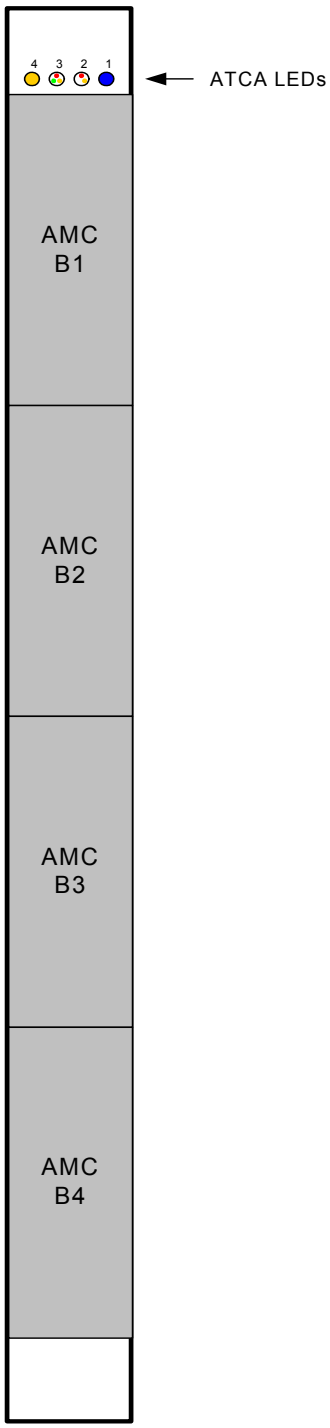
Operation with any of these jumpers set is not supported by the standard application software.

Table 3-19: Jumper Settings (• Default Setting)

FWPD - Flash Write Enable	
Write Enable	in
• Write Protect	out
IPMC0 - Front Board IPMI Override	
ShMC Bypass	in
• Normal Operation	out
IPMC1 - AMC IPMI Override	
ShMC Bypass	in
• Normal Operation	out
IPMC2 - PCIe E-Keying Override	
ShMC Bypass	in
• Normal Operation	out
JTAG_AMC - AMC JTAG Integration	
Included in JTAG Chain	in
• Excluded from JTAG Chain	out
JTAG_IPMC - IPMC JTAG	
Restrict JTAG to IPMC	in
• Normal JTAG Operation	out

3.1.11 Display Elements

Figure 3-4: Front Panel of AT8400



The four front panel ATCA LEDs display the status of the board's health.

Figure 3-5: Symbols Chart

	Heart Beat	ATCA LED3 (yellow)
	Healthy	ATCA LED2 (green)
	Out of Service	ATCA LED1 (red)
	Hot Swap	ATCA BLUE LED

Table 3-20: ATCA LEDs Signification

LED	Signification
ATCA LED3 (HB) (yellow)	User definable
ATCA LED2 (HY) (green)	On=Healthy (PPC/IPMC), Blink=Sensor out of range
ATCA LED1 (OOS) (red)	On=Out of Service (PPC/FUM) Blink=Firmware Update in Progress or Power denied
ATCA BLUE LED (H/S)	On=Ready for Hot Swap (IPMC) Blink=Hot Swap in Progress

3.2 RTM8400

The Rear Transition Module RTM8400 is designed for operation with the AT8400. The RTM8400 provides management access and extended I/O capabilities to the front board.

The RTM8400 has two connectors (P30 and P31), each with 40 differential pairs which contact the corresponding counterparts on the AT8400 (J30 and J31). The connector pinning can be found in section 3.1.8.

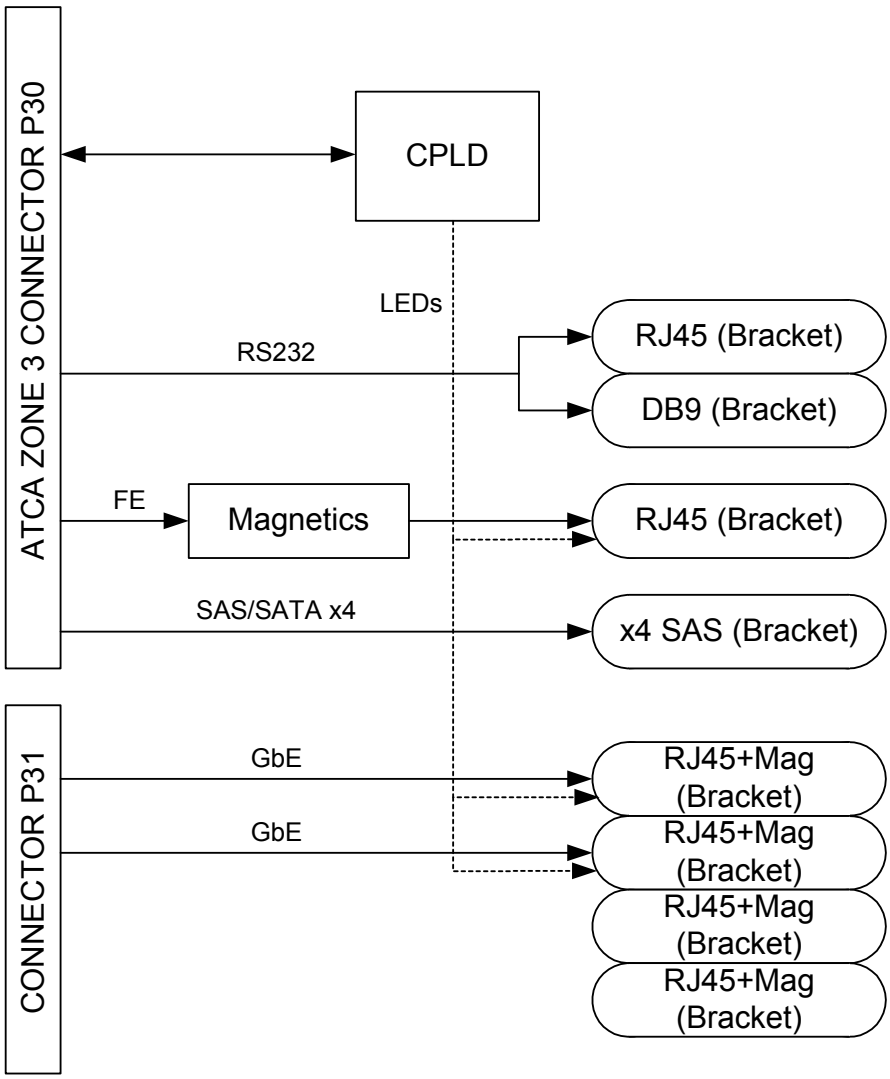
Following interfaces are offered by the RTM8400 for operation with the AT8400:

- RS232 management interface
- FE management interface
- Two GbE ports (connected to the front board GbE switch)
- Four SAS/SATA channels
- JTAG connectors

Maximum power dissipation of the RTM8400 is 2W. All active components are supplied by 3V3_SUS.

The following figure shows the features of the RTM.

Figure 3-6: RTM8400 Block Diagram



3.2.1 RS232 Management Interface

The RS232 is implemented as a RJ45 and as well a DB9 male connector in the faceplate. Console connection can be made using either interface.

Warning!

Do not connect to the RJ45 and the DB9 connector at the same time!

The connectors have the following pinning:

Table 3-21: Serial Port (DB9) Pin Assignment

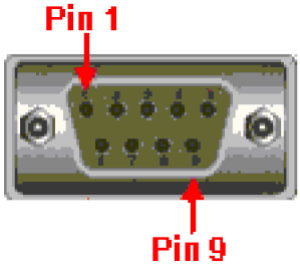
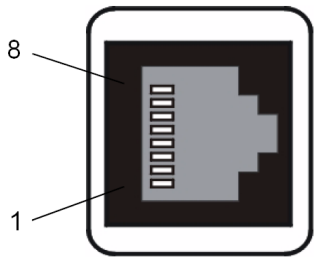
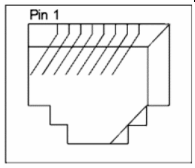
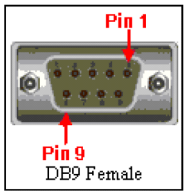
Pin Number	Signal	DB9 male
1	DCD	
2	RXD	
3	TXD	
4	DTR	
5	GND	
6	DSR	
7	RTS	
8	CTS	
9	RI	

Table 3-22: Serial Port (RJ45) Pin Assignment

Pin Number	Signal	
1	RTS	
2	DTR	
3	TXD	
4	GND	
5	GND	
6	RXD	
7	DSR	
8	CTS	

Connection to the RJ45 can be established with a straight through Ethernet cable and a RJ45 (female) to SubD (female) adapter if required. The adapter is described in the following table.

Table 3-23: Serial console terminal cable interface: RJ45 Female to DB9 Female

RJ45 Female	RJ45 Pin Number	Signal	Connected	Description	DB9 Pin Number	DB9 Female
 Front View	1	RTS	Y	Request To Send	8	 Front View
	2	DTR	Y	Data Terminal Ready	6	
	3	TXD	Y	Transmit	2	
	4	GND	N	Ground	-	
	5	GND	Y	Ground	5	
	6	RXD	Y	Receive	3	
	7	DSR	Y	Data Set Ready	4	
	8	CTS	N	Clear To Send	7	
	-	RI	N	Ring Indicator (Not used)	9	
	-	DCD	N	Carrier Detect (Not used)	1	

3.2.2 Fast Ethernet Management Interface

The Fast Ethernet port of the PowerPC 405 GP is used as a management interface. The external FE PHY device on the front board is connected to the RJ45 connector of the RTM.

The default setting of the AT8400's PHY is to operate in autonegotiation enabled mode, 10/100, Full or Half duplex. The two LEDs of the RJ 45 connector are controlled by the CPLD.

The connection is established with a straight through Ethernet cable.

Table 3-24: FE Port (RJ45) Pin Assignment

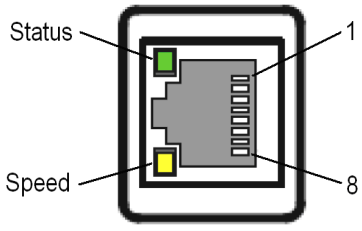
Pin Number	Signal	
1	TX+	
2	TX-	
3	RX+	
4	NC	
5	NC	
6	RX-	
7	NC	
8	NC	

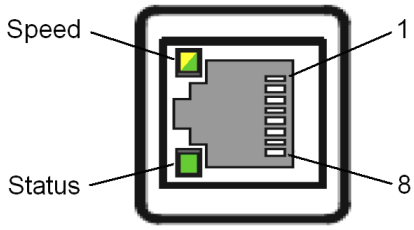
Table 3-25: Fast Ethernet Management (RJ45) LEDs Signification

Speed LED (Yellow)	
OFF	10BASE-T
ON	100BASE-TX
Status LED (Green)	
OFF	Link down
ON	Link up and no activity
BLINK	Link up and activity

3.2.3 GbE Ports

The GE1 and GE2 ports are connected to the front board's GbE switch. The GbE PHY device is placed on the front board, the magnetics are integrated into the x4 RJ45 connector. The connectors' pinning is set to MDI-X mode.

Table 3-26: GbE Pin Assignment

Pin Number	Signal	
1	BI_DB+	
2	BI_DB-	
3	BI_DA+	
4	BI_DD+	
5	BI_DD-	
6	BI_DA-	
7	BI_DC+	
8	BI_DC-	

The following table shows the assignment between connector position and switch port (CLI ID).

Table 3-27: GbE Assignment

Switch Port	Connector
0/1	GE1
0/2	GE2

The two lower RJ45 connectors of the 4-fold block are unused.

The LEDs are controlled by the CPLD: Link/ Activity (Green) and Speed (Green/Yellow).

Table 3-28: GbE LEDs Signification

Speed LED (Green/Yellow)	
GREEN	1000BASE-T
YELLOW	100BASE-TX
OFF	10BASE-T
Status LED (Green)	
OFF	Link down
ON	Link up and no activity
BLINK	Link up and activity

3.2.4 SAS/SATA Channels

An external 4x SAS/SATA connector provides access to the AT8400 SAS Expander device. The connector is a SFF-8470 fixed (receptacle) shielded connector with jack screws.

Table 3-29: External 4x SAS Connector Pin Assignment

Pin Number	Signal	Driven by
G1-G9	Ground	-
S1	STOR0_RX+	RTM
S2	STOR0_RX -	
S3	STOR1_RX +	
S4	STOR1_RX -	
S5	STOR2_RX+	
S6	STOR2_RX -	
S7	STOR3_RX +	
S8	STOR3_RX -	

Table 3-29: External 4x SAS Connector Pin Assignment (Continued)

Pin Number	Signal	Driven by
S9	STOR3_TX -	Front Board
S10	STOR3_TX +	
S11	STOR2_TX -	
S12	STOR2_TX +	
S13	STOR1_TX -	
S14	STOR1_TX +	
S15	STOR0_TX -	
S16	STOR0_TX +	
Housing	Chassis Ground	-

Table 3-30: Assignment of connector channels and expander ports

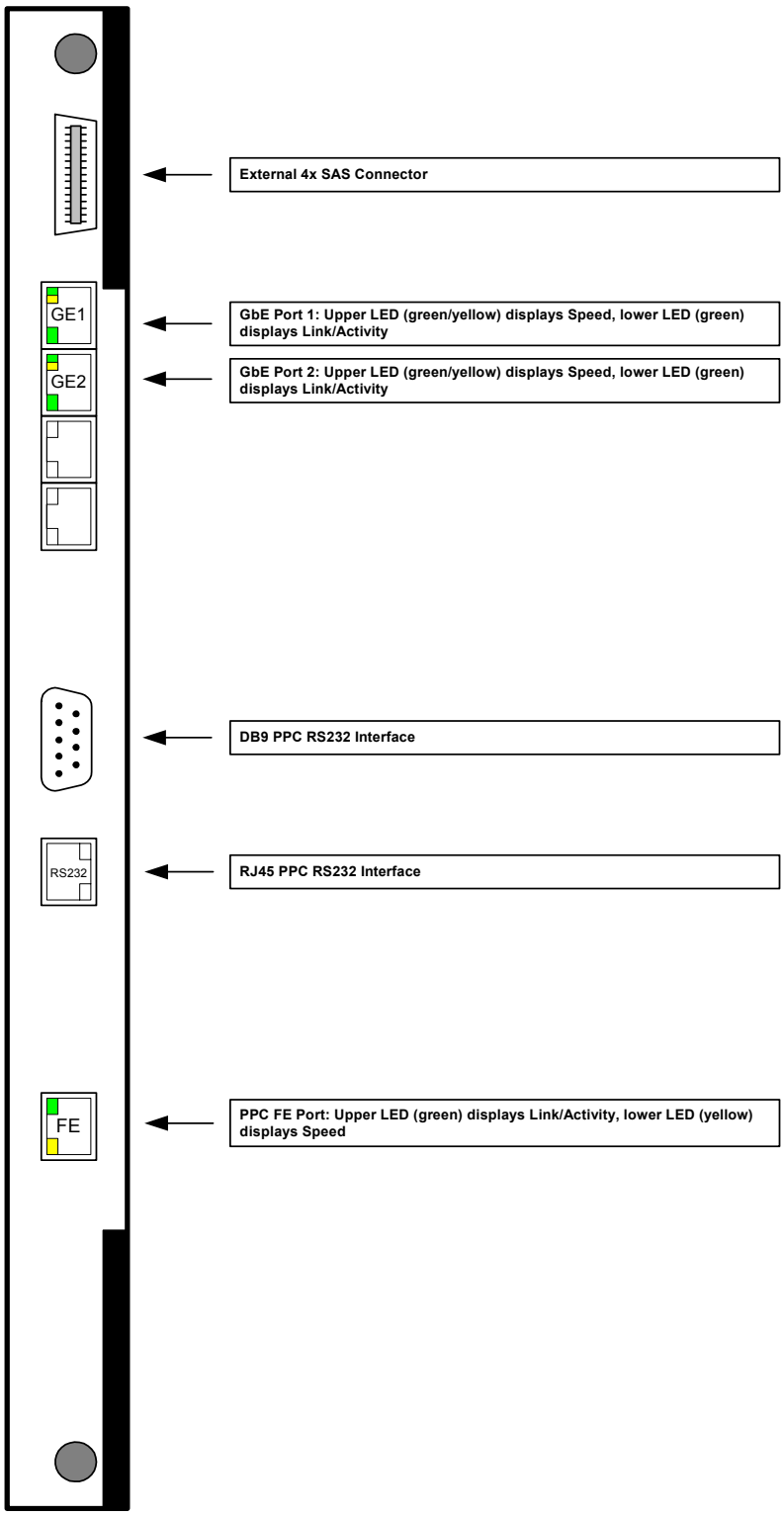
SAS Expander port number	Connector Channel
9	STOR0
8	STOR1
7	STOR2
6	STOR3

3.2.5 Jumpers and JTAG Connectors

Five jumpers configure debug settings for JTAG operation in conjunction with the four headers on the PCB top side. Details are described in the application note "AT840x-AN-#0012-JTAG with RTM8400.pdf".

3.2.6 Display Elements

Figure 3-7: Front Panel of the RTM8400



Chapter 4

Software Description

4. Software Description

Software on the AT8400 includes the following parts:

- Bootloader
- OS (rootFS, kernel)
- Application SW
- IPMI FW

The Software accomplishes operation of the switching hardware and is therefore also referenced as firmware. It is preinstalled on the system and can only be updated by a dedicated update procedure. This manual only describes bootloader, its self tests and IMPI Firmware and introduces the update procedure.

For additional information of system configuration using CLI commands refer to documentation "*AT8400 CLI Command Reference*".

Information about diagnostics and troubleshooting can be found in "*AT8400 Diagnostics Manual*".

4.1 Supported RFCs

The Software supports the following standards and RFCs.

4.1.1 Management

- RFC 826 - ARP
- RFC 854 - Telnet
- RFC 855 - Telnet Option
- RFC 1155 - SMI v1
- RFC 1157 - SNMP
- RFC 1212 - Concise MIB Definitions
- RFC 1867 - HTML/2.0 Forms w/ file upload extensions
- RFC 1901 - Community based SNMP v2
- RFC 2068 - HTTP/1.1 protocol as updated by draft-ietf-http-v11-spec-rev-03
- RFC 2246 - The TLS Protocol, Version 1.0
- RFC 2271 - SNMP Framework MIB
- RFC 2295 - Transparent Content Negotiation
- RFC 2296 - Remote Variant Selection; RSVA/1.0 State Management "cookies"
- RFC 2346 - AES Ciphersuites for Transport Layer Security
- RFC 2576 - Coexistence between SNMP v1,v2 & v3
- RFC 2578 - SMI v2

- RFC 2579 - Textual Conventions for SMI v2
- RFC 2580 - Conformance statements for SMI v2
- RFC 2818 - HTTP over TLS
- RFC 3410 - (Informational): Introduction and Applicability Statements for Internet Standard Management Framework (December 2002)
- RFC 3411 - An Architecture for Describing SNMP Management Frameworks (December 2002)
- RFC 3412 - Message Processing and Dispatching (December 2002)
- RFC 3413 - SNMP Applications (December 2002)
- RFC 3414 - User-based Security Model (December 2002)
- RFC 3415 - View-based Access Control Model (December 2002)
- RFC 3416 - Version 2 of SNMP Protocol Operations (December 2002)
- RFC 3417 - Transport Mappings (December 2002)
- RFC 3418 - Management Information Base (MIB) for the Simple Network Management Protocol (SNMP) (December 2002).
- RFC 3635 Definition of Managed Objects for Ethernet-like Interface Types
- HTML 4.0 Specification - December, 1997
- Java & Java Script 1.3
- SSL 3.0 & TLS 1.0
- SSH 1.5 & 2.0
- Draft-ietf-secsh-transport-16 - SSH Transport Layer Protocol
- Draft-ietf-secsh-userauth-17 - SSH Authentication Protocol
- Draft-ietf-secsh-connect-17 - SSH Connection Protocol
- Draft-ietf-secsh-architecture-14 - SSH Protocol Architecture
- Draft-ietf-secsh-publickeyfile-03 - SECSH Public Key File Format
- Draft-ietf-secsh-dh-group-exchange-04 - Diffie-Hellman Group exchange for the SSH Transport Layer Protocol
- Configurable Management VLAN ID
- Industry Standard CLI

4.1.2 Switching

- IEEE 802.3ac - VLAN Tagging
- IEEE 802.3ad - Link Aggregation with Static LAG and LACP support
- IEEE 802.1S - Multiple Spanning Tree
- IEEE 802.1W - Rapid Spanning Tree
- IEEE 802.1D - Spanning Tree

- GARP
- GVRP - Dynamic VLAN Registration
- GMRP - Dynamic L2 Multicast Registration
- IEEE 802.1Q - Virtual LANs with Port Based VLANs
- IEEE 802.1v - Protocol based VLANs
- IEEE 802.1p - Ethernet Priority with User Provisioning & Mapping
- IEEE 802.1X - Port Authentication
- IEEE 802.3x - Flow Control
- IGMP Snooping
- Port Mirroring
- Broadcast Storm Recovery
- Static MAC Filtering
- Double VLAN / vMAN Tagging
- Jumbo Frames
- IPv6 Classification APIs
- XMODEM
- RFC 768 - UDP
- RFC 783 - TFTP
- RFC 791 - IP
- RFC 792 - ICMP
- RFC 793 - TCP
- RFC 951 - BOOTP
- RFC 1321 - Message Digest Algorithm (MD5)
- RFC 1534 - Interoperation between BOOTP and DHCP
- RFC 2030 - Simple Network Time Protocol (SNTP) Version 4 for IPv4, IPv6 and OSI
- RFC 2131 - DHCP Client
- RFC 2131 - DHCP Server
- RFC 2132 - DHCP Options and BOOTP Vendor Extensions
- RFC 2865 - RADIUS Client
- RFC 2866 - RADIUS Accounting
- RFC 2868 - RADIUS Attributes for Tunnel Protocol Support
- RFC 2869 - RADIUS Extensions
- rfc2869bis - RADIUS support for EAP
- RFC 3176 - InMon Corporation's sFlow: A Method for Monitoring Traffic in Switched and Routed Networks

- RFC 3396 - Encoding Long Option in the Dynamic Host Configuration Protocol (DHCPv4)
- RFC 3580 - 802.1X RADIUS Usage Guidelines
- Draft-ietf-magma-snoop-11.txt - Considerations for IGMP and MLD Snooping Switches

4.1.3 QoS

- Bandwidth Policing (Min and Max; per port/per VLAN)
- Committed Information Rate (CIR)
- Maximum Burst Rate (MBR)
- Per Port (Interface)
- Per VLAN
- Filtering (L3/L4 Access Lists)
- IP Classification - 6 Tuple Classification
- RFC 2474 - DiffServ Definition
- RFC 2475 - DiffServ Architecture
- RFC 2597 - Assured Forwarding PHB
- RFC 3246 - An Expedited Forwarding PHB
- RFC 3260 - New Terminology and Clarifications for DiffServ

4.2 Supported MIBs

The Software supports the following MIBs.

4.2.1 Enterprise MIB

- Support for all managed objects not contained in standards based MIBs.

4.2.2 Switching Package MIBs

- RFC 1213 - MIB-II
- RFC 1493 - Bridge MIB
- RFC 1643 - Ethernet-like -MIB
- RFC 2233 - The Interfaces Group MIB using SMI v2
- RFC 2618 - RADIUS Authentication Client MIB
- RFC 2620 - RADIUS Accounting MIB
- RFC 2674 - VLAN & Ethernet Priority MIB
- RFC 2819 - RMON Groups 1,2,3 & 9
- RFC 2863 – Interfaces Group MIB

- RFC 3291 - Textual Conventions for Internet Network Addresses
- IANA-ifType-MIB
- IEEE 802.1X MIB (IEEE8021-PAE-MIB)
- IEEE 802.3AD MIB (IEEE8021-AD-MIB)

4.2.3 QoS Package MIB

- RFC 3289 - DIFFSERV-MIB & DIFFSERV-DCSP-TC MIBs

4.3 Bootloader

On the AT8400 Carrier board, the bootloader ‘u-boot‘ (universal bootloader) is used. The bootloader initializes the main components of the board like CPU, SDRAM, serial lines etc. for operation. After this, kernel and application are started from flash.

4.3.1 Power on self Test

4.3.1.1 Test Routines

Upon power on or system reset, the bootloader performs a set of Power On Self Tests (POST) to check the integrity of specific components. Components where a POST is available are:

- SDRAM
- PPC405 serial line
- PPC405 I2C
- PPC405 FE

In the case that a POST fails, a POST error code is written into the postcode high byte register of the onboard CPLD. The boot process is not stopped as there are good chances the board can boot even in case of POST errors. The postcode high byte register is also accessible by the IPMC which can report error codes to a separate management instance. Thus more comprehensive diagnostic tests could be started.

The following table shows a list of available POST routines including POST error codes.

Table 4-1: POST routines and error codes

Device	Test	POST Error Code
SDRAM	Data bus - walking 1 test	PCW_DLINE
SDRAM	Address bus - walking 1 test	PCW_ALINE
SDRAM	Memory - read/write test	PCW_MEM
PPC405 UART	Serial loopback teststring	PCW_SERIAL
PPC405 I2C	Bus scan for devices from I2C_ADDR_LIST	PCW_I2C
PPC405 FE	Phy access	PCW_ETH1
PPC405 FE	Phy loopback test using special Ethernet test frame	PCW_ETH2
KCS	KCS READY signal test	KCSCTL

4.3.1.2 Boot Steps

In addition to the Power On Self Tests described above, the bootloader logs the board startup sequence in the postcode low byte register. A postcode value is written each time a step in the start sequence has been completed successfully. The postcode stored is also accessible by the IPMC. In the case that an error occurs during execution of a step, the boot sequence is stopped because a fatal error has occurred with great likelihood. In this case, a management instance can read the last postcode written via the IPMC and thus determine where the fatal error has occurred.

A list of defined postcodes is shown in the table below.

Table 4-2: POST Boot Steps

POST Step Code	Value	Boot Step
PC_INIT	0x00	Initial PC, EBC has been set up
PC_BINIT	0x01	Board early init (interrupt settings)
PC_CLOCKS	0x02	Get system clocks
PC_TIMEB	0x03	Init timebase
PC_ENVINIT	0x04	Init environment
PC_BAUD	0x05	Init baudrate
PC_SERIAL	0x06	Init UART
PC_CPU	0x07	Check CPU
PC_PHY	0x08	Setup PHY
PC_I2C	0x09	Init I2C
PC_INITRAM	0x0A	Init SDRAM controller and SDRAM
PC_TESTRAM	0x0B	Test SDRAM
PC_INITSEQ	0x0F	Board init sequence completed
PC_INITBOARD	0x10	Board init ok, stack set up ok, board info struct set up
PC_RELOC	0x11	Relocation completed
PC_TRAP	0x18	Setup trap handler
PC_FLASH	0x19	Flash OK
PC_CPU2	0x1A	Init higher level parts of CPU
PC_RELOCENV	0x1B	Relocation of environment Ok
PC_BDINFO	0x1C	Fill missing fields of bdinfo
PC_PCI	0x1D	PCI configuration done
PC_DEVICES	0x1E	Device init done
PC_JUMPTABLE	0x1F	Jumptable init done
PC_CONSOLE	0x20	Console init done
PC_MAIN	0x2F	Enter main loop
PC_START_OS	0x3F	Pass control to OS, leave bootloader

4.4 IPMI Firmware

The PPC communicates with the Intelligent Management Controller (IPMC) using the Keyboard Controller Style (KCS) interface. The bootloader is able to communicate with the IPMC, e.g. for POST error logging purposes and fault resilient purposes.

The memory subsystem of the IPMC consists of an integrated flash memory to hold the IPMC operation code and integrated RAM for data. The field replaceable unit (FRU) inventory information is stored in the nonvolatile memory on an EEPROM connected via a local I2C interface to the IPMC microcontroller. It is possible to store up to 4 KBytes within the FRU inventory information. Communication over IPMB bus to the ShMC ensures that 'post-mortem' logging information is available even if the main processor becomes disabled.

The IPMC provides six I2C bus connections. Two are used as the redundant IPMB bus connections to the backplane, one is used for IPMB-L bus with AMC modules, one for the connection to a managed RTM, one for the Base Board and Mezzanine Sensors and one is for local EEPROM storage.

If an IPMB bus fault or IPMC failure occurs, IPMB isolators are used to switch and isolate the backplane/system IPMB bus from the faulted Carrier Board. If possible, the IPMC activates the redundant IPMB bus to re-establish system management communication to report the fault.

The onboard DC voltage, current, and temperature sensors are monitored by the IPMC microcontroller continuously. The IPMC will log an event into the ShMC's System Event Log (SEL) if any of the thresholds are exceeded.

To increase the reliability of the AT8400 management subsystem, an external watchdog supervisor for the IPMC is implemented. The IPMC strobes the external watchdog at two-second intervals to ensure continuity of operation of the board's management subsystem. If the IPMC ceases to strobe the watchdog supervisor for more than six seconds, the watchdog isolates the IPMC from the IPMBs and resets the IPMC. The watchdog supervisor does not reset the payload power and the restart of the IPMC will not affect the payload and will restore the previous Hot Swap state and power level negociated with the ShMC. The external watchdog supervisor is not configurable and must not be confused with the IPMI v1.5 watchdog timer commands.

This external watchdog of the IPMC is implemented in a second microcontroller. This Firmware Upgrade Manager (FUM) is responsible for monitoring the IPMC and for managing the IPMC fail safe firmware upgrade process. The FUM keeps two IPMC Firmware code images in two external SEEPROM memories. If a failure occurs during firmware upgrade, the FUM will automatically rollback to the last known working IPMC firmware image.

4.4.1 Sensor Data Record (SDR)

Every sensor on the Base Board is associated with a Sensor Data Record (SDR). Sensor Data Records contain information about the sensor's identification such as sensor type, sensor name, sensor unit. SDR also contain the configuration of a specific sensor such as threshold/hystheresis and event generation capabilities that specifies sensor behaviour. Some field of the sensor SDR are configurable through IPMI v1.5 commands and are set to built-in initial value.

The AT8400 management controller supports sensor devices and uses the IPMI dynamic sensor population feature of IPMI v1.5 to merge the AMC hot swap sensor with the AT8400 sensors population. AMC hot swap events indicated by this sensor are passed to the ShMC. Additionally, the IPMC updates the sensor population change indicator timestamp accessible

through the Get Device SDR Info command to remain compliant to IPMI v1.5.

All SDRs can be queried using Device SDR commands. Base Board sensors that have been implemented are listed below.

Table 4-3: AT8400 sensors

IPMI Sensor Name	Unit	Health LED/Sensor
IpmC Reboot	discrete	no change
IPMI Watchdog	discrete	no change
IPMC Storage Err	discrete	no change
SEL State	discrete	no change
FRU0 Reconfig	discrete	no change
EventRcv ComLost	discrete	no change
IPMI Info-1	discrete	no change
IPMI Info-2	discrete	no change
IPMB0 Link State	discrete	no change
FRU0 IPMBL State	discrete	no change
FRU1 IPMBL State	discrete	no change
FRU2 IPMBL State	discrete	no change
FRU3 IPMBL State	discrete	no change
FRU4 IPMBL State	discrete	no change
FRU0 FRU Agent	discrete	no change
FRU1 FRU Agent	discrete	no change
FRU2 FRU Agent	discrete	no change
FRU3 FRU Agent	discrete	no change
FRU4 FRU Agent	discrete	no change
FRU0 Hot Swap	discrete	no change
FRU1 Hot Swap	discrete	no change
FRU2 Hot Swap	discrete	no change
FRU3 HotSwap	discrete	no change
FRU4 HotSwap	discrete	no change
Firmware Upg Mng	discrete	no change
Health Error	discrete	no change
Temp Air Inlet	degrees C	Exceeds critical threshold
Temp Air Outlet	degrees C	Exceeds critical threshold
Temp SAS Contr.	degrees C	Exceeds critical threshold
Temp SAS Expan.	degrees C	Exceeds critical threshold
Icc CPU Core	Amps	Exceeds critical threshold
Vcc CPU Core 2V5	Volts	Exceeds critical threshold

Table 4-3: AT8400 sensors (continued)

IPMI Sensor Name	Unit	Health LED/Sensor
Icc 12V FRU0	Amps	Exceeds critical threshold
Vcc 12V FRU0	Volts	Exceeds critical threshold
Icc 12v FRU1	Amps	Exceeds critical threshold
Vcc 12v FRU1	Volts	Exceeds critical threshold
Icc 12v FRU2	Amps	Exceeds critical threshold
Vcc 12v FRU2	Volts	Exceeds critical threshold
Icc 12v FRU3	Amps	Exceeds critical threshold
Vcc 12v FRU3	Volts	Exceeds critical threshold
Icc 12v FRU4	Amps	Exceeds critical threshold
Vcc 12v FRU4	Volts	Exceeds critical threshold
Icc 3.3vSus FRU0	Amps	Exceeds critical threshold
Icc 3.3v FRU0	Amps	Exceeds critical threshold
Vcc 3.3v FRU0	Volts	Exceeds critical threshold
Icc 2.5v FRU0	Amps	Exceeds critical threshold
Vcc 2.5v FRU0	Volts	Exceeds critical threshold
Vcc 1.5v FRU0	Volts	Exceeds critical threshold
Icc 1.25v FRU0	Amps	Exceeds critical threshold
Vcc 1.25v FRU0	Volts	Exceeds critical threshold
Icc 1.2v FRU0	Amps	Exceeds critical threshold
Vcc 1.2v FRU0	Volts	Exceeds critical threshold
Icc 1.0v FRU0	Amps	Exceeds critical threshold
Vcc 1.0v FRU0	Volts	Exceeds critical threshold
Power FRU1	Watts	no change
Power FRU2	Watts	no change
Power FRU3	Watts	no change
Power FRU4	Watts	no change
FRU1 Mp Over Icc	discrete	no change
FRU1 Over Icc	discrete	no change
FRU1 Sensor Err	discrete	no change
FRU2 Mp Over Icc	discrete	no change
FRU2 Over Icc	discrete	no change
FRU2 Sensor Err	discrete	no change
FRU3 Mp Over Icc	discrete	no change
FRU3 Over Icc	discrete	no change
FRU3 Sensor Err	discrete	no change
FRU4 Mp Over Icc	discrete	no change

Table 4-3: AT8400 sensors (continued)

IPMI Sensor Name	Unit	Health LED/Sensor
FRU4 Over Icc	discrete	no change
FRU4 Sensor Err	discrete	no change
-48V FUSES	discrete	no change
CPU Status	discrete	no change
FRU1 PCIe Lane	discrete	no change
FRU2 PCIe Lane	discrete	no change
FRU3 PCIe Lane	discrete	no change
FRU4 PCIe Lane	discrete	no change
UPDC PCIe Lane	discrete	no change
PCIe BIST	discrete	no change
SAS Exp. Fault	discrete	no change
Board Reset	discrete	no change
POST Value	discrete	no change
FRU0 Pwr Denied	discrete	no change
FRU1 Pwr Denied	discrete	no change
FRU2 Pwr Denied	discrete	no change
FRU3 Pwr Denied	discrete	no change
FRU4 Pwr Denied	discrete	no change
Handle Switch	discrete	no change
Ver change	discrete	no change

4.4.1.1 IPMB Link Sensor

The AT8400 provides two IPMB links to increase communication reliability to the shelf manager and other IPM devices on the IPMB. These IPMB links work together for increased throughput where both busses are actively used for communication at any time. A request might be received over IPMB Bus A, and the response is sent over IPMB Bus B. Any requests that time out are retried on the redundant IPMB bus. In the event of any link state change, the events are written to the AT8400 SEL. The IPMC monitors the bus for any link failure and isolates itself from the bus if it detects that it is causing errors on the bus. Events are sent to signify the failure of a bus or, conversely, the recovery of a bus.

4.4.1.2 FRU Hot Swap

The hot swap event message conveys the current state of the FRU, the previous state, and a cause of the state change as can be determined by the IPMC. Refer to PICMG 3.0 Specifications for further details on the hot swap state.

4.4.1.3 CPU Status

The CPU Status is set if the PPC experiences a machine check error.

4.4.1.4 POSTCODE

The IPMC has access to the POSTCODE registers in the CPLD. Refer to section 4.3.1.2 (Boot Steps)

4.4.1.5 Health Error

The Health Error is asserted if one of the sensors in Table 4-3: (AT8400 sensors) matches the Health LED/Sensor condition.

4.4.2 Field Replaceable Unit (FRU) Information

This FRU information contains the IPMI defined Board and Product Information areas that hold the part number and serial number of the board and the Multirecord Information Area that contains the PICMG defined Point to Point Information records.

The Internal Use Area is preallocated to 384 bytes and is free for customer use.

This FRU information responds to FRU ID #0, which is the ID for the IPMC.

4.4.3 E-Keying

E-Keying has been defined in the PICMG 3.0 Specification to prevent board damage, prevent misoperation, and verify fabric compatibility. The FRU data contains the board point-to-point connectivity record as described in Section 3.7.2.3 of the PICMG 3.0 specification.

When the board enters M3 power state, the shelf manager reads in the board point-to-point connectivity record from FRU and determines whether the board can enable the Gigabit Ethernet ports to the back plane. Set/Get Port State IPMI commands defined by the PICMG 3.0 specification are used for either granting or rejecting the E-keys.

Additional E-Keying is prodived for connectivity between the AMC carrier and the AMC bays as described the in Section 3.9 and 3.7 of the AMC.0 RC.1.1 specification. The Set/Get AMC Port State IPMI commands defined by the AMC.0 specification are used for either granting or rejecting the E-keys.

4.4.4 IPMC Firmware Code

IPMC firmware code is organized into boot code and operational code, both of which are stored in a flash module. Upon an IPMC reset, the IPMC executes the boot code and performs the following:

1. Self test to verify the status of its hardware and memory.
2. Calculates a checksum of the operational code.
3. Communicates with the Firmware Upgrade Manager (FUM) in order to inform the IPMC watchdog that the current IPMC firmware is suitable for execution.

Upon successful verification of the operational code checksum, the firmware will jump to the operational code.

4.4.5 LEDs

For LED positions on the front panel, refer to Chapter 3, section 3.1.11., Display Elements.

4.4.5.1 Hot Swap LED (Blue LED)

The AT8400 Carrier Board supports a blue Hot Swap LED mounted on the front panel. This LED indicates when it is safe to remove the Carrier from the chassis. The on-board IPMC drives this LED to indicate the hot swap state. The following states are possible:

Table 4-4: LED state

LED state	Description
OFF	Board is in M4 state, normal state when board is in operation.
ON	Ready for hot swap
Short blink	Board is in M5 state. Deactivation in progress
Long blink	Activation in progress.

4.4.5.2 Out-Of-Service (OOS) LED (ATCA LED1)

Red LED

Table 4-5: OOS LED state

LED state	Description
ON	1) The bootup handshake between FUM and IPMC is not finished or failed 2) The firmware update is in progress and the new IPMC firmware image is copied to the FUM 3) power denied from ShMgr
Blinking	The FUM is programming the IPMC due to a firmware update or a rollback
OFF	The IPMC is operational

4.4.5.3 Health LED (ATCA LED2)

Green LED

Table 4-6: Health LED state

LED state	Description
ON	None of the health sensors is asserted
Blinking	At least one health sensor is asserted

4.4.5.4 Customer Definable LED (ATCA LED 3)

This is an amber LED which can be used by a customer application. This LED can be controlled by PICMG 3.0 defined LED commands.

4.4.6 Hot Swap Process

The AT8400 Carrier Board has the ability to be hot-swapped in and out of a chassis. The on-board IPMC manages the power-up and power-down transitions.

In addition to captive retaining screws, the AT8400 Carrier Board has two ejector mechanisms to provide a positive cam action; this ensures the blade is properly seated. The bottom ejector handle also has a switch that is connected to the IPMC to determine if the board has been properly inserted.

When the lower ejector handle is disengaged from the faceplate, the hot swap switch will assert a signal to the IPMC, and the IPMC will move from the M4 state to the M5 state. At the M5 state, the IPMC will ask the ShMC for permission to move to the M6 state. The Hot Swap LED will indicate this state with a short blink. Once permission is received from the ShMC or higher-level software, the board will move to the M6 state. The ShMC or higher level software can reject the request to move to the M6 state. If this occurs, the Hot Swap LED returns to a solid off condition, indicating that the Carrier Board has returned to M4 state.

If the Carrier Board reaches the M6 state, either through an extraction request through the lower ejector handle or a direct command from higher-level software. The Hot Swap LED continues to flash during this preparation time, just like it does in M5 state. When payload power is successfully turned off, the Hot Swap LED remains lit, indicating it is safe to remove the AT8400 from the chassis.

4.5 Firmware Administration

A running AT8400 system requires – after the bootloader has passed control to the kernel – the kernel itself, the root file system, the FASTPATH switching application and a configuration file for the base switch. Kernel, applications and RootFS are aggregated into an initrd-image. These software components, together with the IPMC image, make up the AT8400 firmware.

The flash holding the AT8400 software is divided into seven partitions. There are partitions to store two bootloader and two software images. Two partitions are reserved for the (redundant) bootloader environment and one partition is used to hold up to 99 configuration setting files. The software partitions hold a combined kernel and initrd image as well the application software which is part of the initrd. The partition scheme of the flash is shown below:

Table 4-7: FLASH Partition Scheme (32MB)

Partition	Size	MTD	Partition name
U-Boot Loader primary image	256KB	6	u-boot_P
U-Boot Loader secondary image, updatable	256KB	5	u-boot_S
U-Boot primary environment	256KB	4	u-boot_envA
U-Boot secondary environment	256KB	3	u-boot_envB
Software image secondary partition	14MB	2	image_B
Software image primary partition	14MB	1	image_A
JFFS2 Configuration File Partition	3MB	0	config

The firmware update procedure is designed to provide a failsafe capability to update IPMC, software and configuration settings separately. Each combination of these components can be used as a startup configuration, though they must be compatible to each other. Please always follow Kontron documentation for all your upgrades. Software versions provided with an official release are known to work together.

In the following, the CLI commands to setup, change and activate startup configuration and the CLI commands necessary to perform firmware upgrades are described. The CLI commands described below are executed in the privileged mode of the CLI hierarchy, which is entered by executing the ‘enable’ command. Please refer to the “*AT8400 CLI Command Reference*“ for more information regarding the CLI commands and the way to use them.

4.5.1 Startup Configurations

A startup configuration is a combination of an initrd and a configuration file for the base switch. The IPMC image is not part of the configuration and is updated separately. Several configurations (up to 99) can be defined but only one is active at a time. To display the currently available startup configurations, the CLI command ‘show’ is used.

```
(AT8400 Base Fabric) #show startupconfig startup

ACT NR INITRD       CONFIG
--- -- ------------ ------------
    01 A ALPHA 6.01 01 standard
 *  02 A ALPHA 6.01 02 config

(AT8400 Base Fabric) #
```

In this example, three startup configurations are available. Startup configuration 02 is the currently active configuration which is indicated by the '*' in the first column. This configuration consists of:.

- INITRD ALPHA 6.02 which is located in Software partition A.
- Base fabric configuration file which is stored in slot 02 of the configuration partition.

The user can define other startup configurations and combine images and configuration files as needed. To set up a new startup configuration, it is necessary to change into the CLI's configuration mode using the 'configure' command. In this mode, the 'startupslot' command is used as shown in the following example:

```
(AT8400 Base Fabric) (Config)#startupslot 3 config 2 initrd A

Successfully set startup slot 3
You may mark it active now and reboot to use the new configuration.

(AT8400 Base Fabric) (Config)#exit

(AT8400 Base Fabric) #show startupconfig startup

ACT NR INITRD       CONFIG
--- -- ------------ ------------
    01 A ALPHA 6.01 01 standard
 *  02 A ALPHA 6.01 02 config
    03 A ALPHA 6.01 02 config

(AT8400 Base Fabric) #
```

A new startup configuration has been added to the list combining the software images given in the previous command.



Warning!

It is not recommended to combine images from different releases.

The startup configuration created before can be deleted by entering exactly the same command string preceeded by 'no':

```
(AT8400 Base Fabric) (Config)#no startupslot 3 config 2 initrd A
```

The 'show' command can also be used to display available versions of initrd. The syntax is:

```
show startupconfig initrd
```

The configuration mode is also used to activate one of the available startup configurations. The syntax is:

```
startupslot 3 activate [once]
```

This command would activate the startup configuration 3 upon next system reset. The optional parameter ‘once’ would start configuration 3 only once after the next system reset and start the previously active configuration 2 on following resets. This is used to implement the failsafe upgrade procedure described below.

4.5.2 Updating Firmware

The firmware - except bootloader and IPMC image - is updated using the CLI. To get a reliable and failsafe update procedure, the following precautions must be fulfilled:

- Two independent partitions, one holds system A initrd and one holds system B initrd. The active system is either system A or system B. See the flash partition scheme shown above for more detail.
- One Time Boot capability: After having updated the inactive kernel and root file system, the new system has to be started by rebooting the board. In case of the update having installed an inoperable system which would cause the board to hang when booting, the next board reset will restart the previous known good version of the system. This is achieved by programming the bootloader environment appropriately.
- Redundant bootloader environment sectors: When the system is updated, the bootloader environment must be changed to be able to start the updated version. The bootloader environment sector is stored twice in flash, one active version and one backup version in case the active version is deleted during update due to power loss or similar errors. In this case, the redundant environment would cause the bootloader to start the previous known good version of the system.

A software update of the AT8400 Carrier Board is done by performing the following steps:

1. Download initrd image into the appropriate slot of the flash memory. Ensure that the currently active images are not overwritten.
2. Select a configuration for base switch for the new software release. This can be done by choosing the factory default or by storing the running system configuration into flash.
3. Create a startup configuration by combining the slots with the update images and the configuration slots for base and fabric switch.
4. Activate the selected startup configuration for One Time Boot.
5. Restart the board.
6. Activate the new startup configuration permanently

A software release for the AT8400 consists of one software package, initrd. The package is a tar archive containing an image of the software and a MD5 checksum file for consistency check. The name of the package file is arbitrary but the file names in the archive must not be altered.

When performing a firmware update, the software packages are loaded from a remote TFTP server in the first step. To load a software package via TFTP into a specified slot, the CLI command ‘download’ is used:

```
(AT8400 Base Fabric) #download initrd tftp://192.168.50.5/system.pkg B
```

```
Downloading image, this may take a while...
Successfully transferred initrd image tftp://192.168.50.5/initrd.pkg to slot 2
You may mark it active now and reboot to use the new initrd image.

(AT8400 Base Fabric) #
```

This downloads the specified initrd package file via TFTP and writes the image into the partition of the specified slot (B). The CRC32 checksum of the image is checked while writing it into flash. It is important **not** to overwrite the slots containing the currently active software, otherwise the One Time Boot mechanism does not make sense. In case of an error the partition will be deleted and the old image will be used to reboot the system

After the software image has been downloaded into flash, the configuration slot for the base switch must be selected. In case that no appropriate configuration for the base switch is available, the factory default configuration should be used for the startup configuration of the new software release. Alternatively, the running configuration settings of base switch can be stored on flash using the following CLI command:

```
(AT8400 Base Fabric) #copy system:running-config nvram:startup-config

This operation may take a few minutes.
Management interfaces will not be available during this time.

Are you sure you want to save? (y/n) y

Configuration Saved!

(AT8400 Base Fabric) #
```

Finally, a startup configuration containing the slots of the new software release and the configuration slots must be selected or a new startup configuration must be created as described above. After this step has been completed, the startup configuration is activated only for the next boot and the board is rebooted. This is done with the ‘startupslot’ CLI command in the configure mode:

```
(AT8400 Base Fabric) (Config)#startupslot 3 activate once
```

This command enables the startup configuration 3 only for the next system restart. In the case that the board hangs due to a corrupted software image, this will be detected and the board is automatically rebooted with the previous known good startup configuration. This way, a failsafe upgrade of the AT8400 software is possible.

To restart the board with the new startup configuration, the CLI command ‘reload’ is used:

```
(AT8400 Base Fabric) (Config)#reload
```

If the new startup configuration is considered functional after the reboot, it must be activated permanently, or else the one that is still active will be used again:

```
(AT8400 Base Fabric) (Config)#startupslot 3 activate
```

4.5.3 Updating IPMI

Updating the IPMI firmware is different from updating the other software parts as updating is done directly when invoking the download command. In case that the update procedure fails or the update image is corrupted, the IPMC will be able to restart all the same by means of its rollback functionality. The IPMI software package file is stored in the result/ppc405/firmware path of the release directory tree. To update the IPMI firmware, the CLI command ‘download’ is used:

```
AT8400 Base Fabric) #download ipmifw tftp://192.168.50.5/ipmi.pkg

Flashing a new IPMI firmware will disable the IPMI Controller for some minutes.
Are you sure to update the IPMI firmware? (y/n)y
...
(AT8400 Base Fabric) #
```

Appendix A

Getting Help

A. Getting Help

If, at any time, you encounter difficulties with your application or with any of our products, or if you simply need guidance on system setups and capabilities, contact our Technical Support at:

North America	EMEA
Tel.: (450) 437-5682	Tel.: +49 (0) 8341 803 333
Fax: (450) 437-8053	Fax: +49 (0) 8341 803 339

If you have any questions about Kontron, our products, or services, visit our Web site at: www.kontron.com

You also can contact us by E-mail at:

North America: support@ca.kontron.com

EMEA: support-kom@kontron.com

Or at the following address:

North America	EMEA
Kontron Canada, Inc.	Kontron Modular Computers GmbH
616 Curé Boivin	Sudetenstrasse 7
Boisbriand, Québec	87600 Kaufbeuren
J7G 2A7 Canada	Germany

RETURNING DEFECTIVE MERCHANDISE

Before returning any merchandise please do one of the following:

- **Call**

1. Call our Technical Support department in North America at (450) 437-5682 or in EMEA at +49 (0) 8341 803 333. Make sure you have the following on hand: our Invoice #, your Purchase Order # and the Serial Number of the defective unit.
2. Provide the serial number found on the back of the unit and explain the nature of your problem to a service technician.
3. The technician will instruct you on the return procedure if the problem cannot be solved over the telephone.
4. Make sure you receive an RMA # from our Technical Support before returning any merchandise.

- **Fax**

1. Make a copy of the request form on the following page.
2. Fill it out.
3. Fax it to us at: North America (450) 437-0304, EMEA +49 (0) 8341 803 339

- **E-mail**

1. Send us an e-mail at: RMA@ca.kontron.com in North America and at: orderprocessing@kontron-modular.com in EMEA. In the e-mail, you must include your name, your company name, your address, your city, your postal/zip code, your phone number, and your e-mail. You must also include the serial number of the defective product and a description of the problem.

WHEN RETURNING A UNIT

- In the box, you must include the name and telephone number of a person, in case further explanations are required. **Where applicable, always include all duty papers and invoice(s) associated with the item(s) in question.**
- Ensure that the unit is properly packed. Pack it in a rigid cardboard box.
- Clearly write or mark the RMA number on the outside of the package you are returning.
- Ship prepaid. We take care of insuring incoming units.

North America	EMEA
Kontron Canada, Inc.	Kontron Modular Computers GmbH
616 Curé Boivin	Sudetenstrasse 7
Boisbriand, Québec	87600 Kaufbeuren
J7G 2A7 Canada	Germany



Return to Manufacturer Authorization Request

Contact Name:	_____		
Company Name:	_____		
Street Address:	_____		
City:	_____	Province/State:	_____
Country:	_____	Postal/Zip Code:	_____
Phone Number:	_____	Extension:	_____
Fax Number:	_____	E-Mail:	_____

Serial Number	Failure or Problem Description	P.O. # (if not under warranty)

Fax this form to Kontron's Technical Support department

in North America at (450) 437-0304

or in EMEA at +49 (0)8341 803 339