kontron

AT8904M USER GUIDE

AdvancedTCA

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Imprint

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Explanation of Symbols



CE Conformity

This symbol indicates that the product described in this manual is in compliance with all applied CE standards. Please refer also to the section “Applied Standards” in this manual.



Caution, Electric Shock!

This symbol and title warn of hazards due to electrical shocks (> 60V) when touching products or parts of them. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your material.

Please refer also to the section “High Voltage Safety Instructions” on the following page.



Warning, ESD Sensitive Device!

This symbol and title inform that electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Please read also the section “Special Handling and Unpacking Instructions” on the following page.



Warning!

This symbol and title emphasize points which, if not fully understood and taken into consideration by the reader, may endanger your health and/or result in damage to your material.



Note...

This symbol and title emphasize aspects the reader should read through carefully for his or her own advantage.

For Your Safety

Your new Kontron product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new Kontron product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions



Warning!

All operations on this device must be carried out by sufficiently skilled personnel only.



Caution, Electric Shock!

High voltages are present inside the chassis when the unit's power cord is plugged into an electrical outlet. Turn off system power, turn off the power supply, and then disconnect the power cord from its source before removing the chassis cover. Turning off the system power switch does not remove power to components.

Special Handling and Unpacking Instructions



ESD Sensitive Device!

Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing mezzanines, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory back-up, ensure that the board is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the board.

General Instructions on Usage

In order to maintain Kontron's product warranty, this product must not be altered or modified in any way. Changes or modifications to the device, which are not explicitly approved by Kontron AG and described in this manual or received from Kontron's Technical Support as a special handling instruction, will void your warranty.

This device should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This applies also to the operational temperature range of the specific board version, which must not be exceeded. If batteries are present their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, please follow only the instructions supplied by the present manual.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the board please re-pack it as nearly as possible in the manner in which it was delivered.

Special care is necessary when handling or unpacking the product. Please, consult the special handling and unpacking instruction on the previous page of this manual.

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Kontron AG grants the original purchaser of Kontron's products a ***TWO YEAR LIMITED HARDWARE WARRANTY*** as described in the following. However, no other warranties that may be granted or implied by anyone on behalf of Kontron are valid unless the consumer has the express written consent of Kontron AG.

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If the customer's eligibility for warranty has not been voided, in the event of any claim, he may return the product at the earliest possible convenience to the original place of purchase, together with a copy of the original document of purchase, a full description of the application the product is used on and a description of the defect. Pack the product in such a way as to ensure safe transportation (see our safety instructions).

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Chapter 1

Introduction

1. Introduction

The AT8904M Board described in this manual is designed for the Advanced Telecom Computing Architecture (AdvancedTCA® or ATCA) defined by the *PCI Industrial Computer Manufacturers Group (PICMG)*. The main advantages of AdvancedTCA include high throughput, multi-protocol support, high-power capability, hot swappability, high scalability and integrated system management. For further information regarding the AdvancedTCA standards and their use, please consult the complete AdvancedTCA specification or visit the *PICMG* web site.

1.1 Product Overview

The Kontron AT8904M is a PICMG 3.0 and 3.1 compliant Hub Board for AdvancedTCA shelves, designed according to the RoHS directive. Suitable for dual-star and full-mesh in 14 and 16 slot systems, it also provides 2 mid-size AMC slots for customization. This unique versatile design allows cost-optimised tailoring to the requirements of the application.

The Base Interface switch provides Gigabit Ethernet services on Base Channels 2-16 and Fast Ethernet to the Shelf Managers. The Fabric Interface switch provides 10 Gigabit Ethernet links to all 15 Fabric Channels and both AMCs.

AMC slots can be equipped with

- Processor-AMC, e.g. acting as the system controller (saving one ATCA slot)
- Storage-AMC as mass storage device for the Processor-AMC
- Master Clock Generator AMC providing network synchronisation for telecom applications
- Dual 10GbE Fabric Inter-Link-AMC to enable multi-shelf AdvancedTCA systems

Performance

The AT8904M employs leading-edge switching technology providing full wire-speed throughput at all load conditions. A powerful control processor runs higher layer protocols based on the market leading LVL7 software suite.

Flexibility

The Fabric Interface is realized as a mezzanine on the base board. Therefore the AT8904M can easily be adapted to customer requirements without re-engineering the whole board, thus minimising time-to-market. Options include using Ethernet, Ethernet + Fibre Channel, PCI-Express or Advanced Switching on the Fabric Interface.

Management

The AT8904M is managed either in-band or out of band via 10/100 Ethernet or RS232 management ports. The comprehensive set of supported protocols rounds out the feature set of Kontrons' second generation AdvancedTCA Hub Board.

1.1.1 AT8904M Features

PICMG 3.0 compliant Hub Board

- Supports Base Interface (GbE)
- Supports Fabric Interface (10GbE)
- For 14 and 16 slot shelves
- 2 mid-size AMC slots for customization
- Uplinks for Base and Fabric Interface
- Comprehensive protocol support
- Full Hot-Swap capabilities
- Full Redundancy support

Base Interface (PICMG 3.0)

- Non-blocking layer 2/3 switching/routing
- 4x10/100/1000BASE-T uplinks on front panel
- 2xGbE connection to AMC slot B1
- 1xGbE connection to AMC slot B2

Fabric Interface (PICMG 3.1)

- Non-blocking layer 2 switching with VLANs
- 10GbE connection to redundant Hub Board
- 10GbE connections to payload slots 2-15
- 1x10/100/1000BASE-T uplink on front panel
- Dual 10GbE connection to each AMC slot

Management and Protocols

- Management via SNMP, TELNET, CLI
  - In-band
  - Out of band via Ethernet or RS232
- IPMI version 1.5
- Ethernet/Bridging protocols include
  - Link aggregation (802.3ad)
  - VLANs (802.1Q)
  - Spanning tree (802.1D, 802.1w)
  - QoS (802.1p)
  - Flow control (802.3x)
  - GVRP, GMRP

- Routing protocols include
  - OSPFv2
  - RIPv2
  - VRRP
  - DiffServ
  - ARP

1.1.2 General compliances

The AT8904M conforms to the following specifications:

- PICMG 3.0 AdvancedTCA Base Specification, Revision 2.0
- PICMG 3.1 Gigabit Ethernet for AdvancedTCA Systems, Revision 1.0
- AMC.0 AMC Base Specification, Revision 2.0
- AMC.2 AMC Gigabit Ethernet / 10 Gigabit XAUI Ethernet
- AMC.3 AMC Storage
- IPMI v1.5 Intelligent Platform Management Interface Specification

1.1.3 Optional Accessories

1.1.3.1 AMC

Two standard mid-size single width AMC bays for standard or custom AMCs are implemented.

AMC slots can be equipped with a

- Processor-AMC, e.g. acting as the system controller (saving one ATCA slot)
- HDD-AMC as mass storage device for the Processor-AMC
- Master Clock Generator AMC providing network synchronisation for telecom applications
- AM4310 Dual 10GbE Uplink AMC to enable multi-shelf AdvancedTCA systems (see chapter 3.3)

1.1.3.2 RTM

RTM is optional. For further information on RTM, please refer to chapter 3.1.7.

1.1.4 Hot Swap Capability

The board supports Full Hot Swap capability as required by PICMG 3.0 R2.0. It can be removed from or installed in the system while it is on (without powering-down the system). Please refer to the PICMG 3.0 R2.0 specification for additional details.

1.1.5 Board Options

The Kontron ATCA Hub family is available with different Fabric Mezzanine options. Mid-size and Full-size AMCs are supported.

Table 1-1: Fabric Interface Options

Product	AMC Size	Fabric Interface
AT8901M	Mid-size	none
AT8902M	Mid-size	Gigabit Ethernet
AT8904M	Mid-size	10 Gigabit Ethernet
AT8901	Full-size	none
AT8902	Full-size	Gigabit Ethernet

The AT8904M base board and the Gigabit Ethernet fabric mezzanine are described in Chapter 3.

1.2 Technical Specification

Table 1-2: AT8904M Main Specifications

	AT8904M	SPECIFICATIONS

Processor and Memory	PowerPC IBM PPC 405 GPr 400MHz	• IBM PowerPC® 405 32-bit RISC processor core operating up to 400MHz with 16KB I- and D-caches
		• PC-133 synchronus DRAM (SDRAM) interface
		  • 40-bit interface serves 32 bits of data plus 8 check bits for ECC applications
		• 4KB on-chip memory (OCM)
		• DMA support for external peripherals, internal UART and memory
		  • Scatter-gather chaining supported
		  • Four channels
		• PCI Revision 2.2 compliant interface (32-bit, up to 66MHz)
		• Ethernet 10/100Mbps (full-duplex) support with media independent interface (MII)
		• Two serial ports (16550 compatible UART)
		• Internal processor local Bus (PLB) runs at SDRAM interface frequency
		• IEEE 1149.1 (JTAG) boundary scan

Table 1-2: AT8904M Main Specifications (Continued)

	AT8904M	SPECIFICATIONS

Ethernet	Broadcom 5650x/5630x GbE Switch	• 24 10/100/1000 Mbps Ethernet ports
		• Fifth generation of StrataSwitch and StrataXGS product line
		• Line-rate switching for all packet sizes and conditions
		• On-chip data packet memory and table memory
		• IPv6 routing and tunneling
		• Advanced Fast Filter Processor (FFP) Content Aware classification
		• Advanced security features in hardware
		• Port-trunking and mirroring supported across stack
		• Advanced packet flow control:
		  • Head-of-line-blocking prevention
		  • Back pressure support
		• Eight QoS queues per port with hierarchical minimum/maximum shaping per Class of Service (CoS) per queue per port
		• Standard compliant 802.1ad provider bridging
		• IEEE 1149.1 (JTAG) boundary scan

	Broadcom BCM 56800	• 20 10-GbE/1-GbE ports
		• Based on StrataXGS architecture
		• 200-Gbps switching capacity at line rate
		• Support for eight classes of service (CoS) per port
		• Port trunking and remote mirroring support
		• Advanced packet flow control
		  • Head of line blocking prevention
		  • Full-duplex flow control (802.3x)
		• Supports IEEE 802.1p, TOS/DiffServ, rate limiting, policing, priority tagging, and remapping
		• Extended security and ACL filtering
		• Full IPv6 routing support
		• IEEE 1149.1 (JATAG) boundary scan

Table 1-2: AT8904M Main Specifications (Continued)

	AT8904M	SPECIFICATIONS
Interfaces	Backplane (Zone 2)	• Fabric channels 1-15: 10GbE (XAUI) • Base channel 1: 2 x Ethernet to ShMCs (10/100BASE-T) • Base channels 2-16: 1 x GbE (1000BASE-T) • CLK 1/2/3 (A/B) • Update channels: 2 x GbE (1000BASE-BX)
	RTM (Zone 3)	• 8 generic RTM channels from AMC Slot B1, 4 from B2 • SAS/SATA/FC interface for mass storage from each AMC Slot • I2C IPMI connection
	Front panel	• Serial port for management of PPC • Fast Ethernet for management of PPC • 4 RJ45 10/100/1000BASE-T Base Interface Uplinks • 1 RJ45 10/100/1000BASE-T Fabric Interface Uplink

Table 1-2: AT8904M Main Specifications (Continued)

	AT8904M	SPECIFICATIONS
General	Mechanical	• 8U form factor mechanically compliant to PICMG 3.0 • Single Slot (6HP) • 2 standard mid-size/single width AMC Slots • 280 mm x 322 mm (11.024“ x 12.677“) • Weight: 2.25 (4.96 lbs)
	Power Requirements	• Typical: 67W • Maximum (with 2 AMCs and RTM): 175W • AMCs may consume up to 65W • Operating Voltage: -38 to -72VDC
	Temperature	Designed to meet or exceed the following (Characteristics with AMC): • Air Flow: 30 CFM min • Operating: 0°C to +55°C (32°F to 131°F) • Non-operating: -40°C to +70°C (-40°F to 158°F)
	Humidity	Designed to meet or exceed the following: • Bellcore GR63, Section 4.1 • Operating: 15%-90% (non-condensing) at 55°C (131°F) • Non-Operating: 5%-95% (non-condensing) at 40°C (104°F)
	Altitude	Designed to meet or exceed the following: • Operating: 4000 m (13123 ft) • Non-Operating: 15000m (49212 ft)
	Vibration	Designed to meet or exceed the following: • Bellcore GR-63, Section 4.4 • Operating: 1.0G, 5-500Hz each axis • Non-operating: 0.5G, 5-50Hz; 3.0G, 50-500Hz each axis
	Shock	Designed to meet or exceed the following: • DIN/IEC 60068-2-27 • Bellcore GR-63, Section 4.3 • 30G, half-sine 11ms, each axis

Table 1-2: AT8904M Main Specifications (Continued)

	AT8904M	SPECIFICATIONS
General	Safety	Designed to meet or exceed the following: • UL 60950, 3rd edition • EN 60950 • LVD 73/23/EEC • Denan Law
	EMC	Designed to meet or exceed the following: • FCC 47 CFR Part 15, Subpart B • EN55022, EN55024 • EN 300 386
	Reliability	• MTBF: > 144,300 hours @ 40°C / 104°F (Telcordia SR-332, Issue 1)

HW Monitoring	LEDs	• ATCA LEDs:
		  • 4 LEDs ("Ready for Hot Swap", "Out of Service", "Healthy", "Heart Beat")
		• Ethernet:
		  • Shielded RJ-45 connectors with integrated LED's
		• Fabric/Base Ports :
		  • 4x/4x Shielded RJ-45 connectors with integrated LED's
		• User LEDs:
		  • 4 LEDs ("Base Status", "Base Selected", "Fabric Status", "Fabric Selected")
		• Switch LEDs:
		  • 16 LEDs (activity and link status for base or fabric channels, respectively)
		• Display switch:
		  • switches between fabric or base switch port status display

	Board Management	• Based on IPMI 1.5 • FRU Management • Sensors (Voltage, Current, Temperature, Fuse) • Status and Alerting • Hot Swap • Electronic Keying of Base and Fabric Interfaces

Table 1-3: AM4310 Main Specifications

	AM4310	SPECIFICATIONS
Ethernet	Broadcom 8704 10GbE PHY	• 4-Lane XAUI Interface (3.125 Gbps) • XFP Interface • Loss of signal detection • Standard compliant 802.3ae • IEEE 1149.1 (JTAG) boundary scan
Interfaces	XAUI Interface (AMC Connector)	• Fabric Fabric channels 1-5: 2 x GbE (1000BASE-BX) • Fabric channels 6-15: 1 x GbE (1000BASE-BX) • channels 4-11: 2 x 10GbE • Fabric channel 12: XG management interface (MDIO)
	Front panel	• 2 XFP cages
General	Mechanical	• Standard full height/single width AMC compliant to PICMG 3.0 • 73.6 mm x 180.7 mm (2.898“ x 7.114“)
	Power Requirements	• 65Maximum: 24W175 • Operating Voltage: 3.0 to 3.6V Management, 10 to 14V Payload
	Temperature	Designed to meet or exceed the following: • Air Flow: 30 CFM min • Operating: 0°C to +55°C (32°F to 131°F) • Non-operating: -40°C to +70°C (-40°F to 158°F)
	Humidity	Designed to meet or exceed the following: • Bellcore GR63, Section 4.1 • Operating: 15%-90% (non-condensing) at 55°C (131°F) • Non-Operating: 5%-95% (non-condensing) at 40°C (104°F)
	Altitude	Designed to meet or exceed the following: • Operating: 4000 m (13123 ft)) • Non-Operating: 15000m (49212 ft)
	Vibration	Designed to meet or exceed the following: • Bellcore GR-63, Section 4.4 • Operating: 1.0G, 5-500Hz each axis • Non-operating: 0.5G, 5-50Hz; 3.0G, 50-500Hz each axis
	Shock	Designed to meet or exceed the following: • DIN/IEC 60068-2-27 • Bellcore GR-63, Section 4.3 • 30G, half-sine 11ms, each axis

Table 1-3: AM4310 Main Specifications (Continued)

	AM4310	SPECIFICATIONS
General	Safety	Designed to meet or exceed the following: • UL 60950, 3rd edition • EN 60950 • LVD 73/23/EEC • Denan Law
	EMC	Designed to meet or exceed the following: • FCC 47 CFR Part 15, Subpart B • EN55022, EN55024 • EN 300 386
	Reliability	• MTBF: > 650,000 hours @ 40°C / 104°F (Telcordia SR-332, Issue 1)

HW Monitoring	LEDs	• ATCA LEDs:
		  • 3 LEDs ("Ready for Hot Swap", "Out of Service", "Healthy")
		• XFP LEDs:
		  • 2 LEDS (Link for each XFP)

	Board Management	• Based on IPMI 1.5 • FRU Management • Sensors (Voltage, Temperature) • Status and Alerting • Hot Swap and Fabric

1.3 Software Support

The following table contains information related to software supported by the AT8904M.

Table 1-4: AT8904M Software Specification

AT8904M	SPECIFICATIONS
General	• Reliable field upgrades for all software components • Dual boot images with roll-back capability • Management via SNMP and Command Line Interface • System access via TELNET, SSH and serial line • Hot-Swap support • Hot-Plug support for AMC modules • Redundancy support for base and extension fabric switches • IP router on the base fabric • Support for managing the optional MCG and XAUI uplink AMC modules • Modular software architecture to enable project specific customization
Ethernet/Bridging (Base and extension fabric switches)	• Static link aggregation (IEEE 802.3ad) on any port combination • Classic and rapid spanning tree algorithms supported (IEEE 802.1D, IEEE 802.1w) • Quality Of Service on all ports (IEEE 802.1p) • Full Duplex operation and flow control on all ports (IEEE 802.3x) • Static MAC filtering • Port Authentication (IEEE 802.1X) • Auto negotiation of speeds and operational mode on all external GbE interfaces as well as on all base fabric interfaces • Layer 2 multicast services using GARP/GMRP (IEEE 802.1p) • VLAN support including VLAN tagging (IEEE 802.3ac), dynamic VLAN registration with GARP/GVRP (IEEE 802.1Q) and Protocol based VLANs (IEEE 802.1v) • Double VLAN tagging • Port Mirroring
IP Routing	• Redundancy of routing functionality using a second switch hub board • IPv4 Forwarding on all base channels and connected uplink ports • Quality of service according to the DiffServ standards • ARP for all routable interfaces • ICMP for all routable interfaces • OSPF routing protocol version 2 • RIP routing protocol version 2 • VRRP (virtual router redundancy protocol) for transparent fail over of default routers • IGMP snooping

Table 1-4: AT8904M Software Specification (Continued)

AT8904M	SPECIFICATIONS
QoS	• CoS (Class of Service) • DifffServ (Differentiated Services) • ACL (Access Control List)
Applications	• NTP client for retrieving accurate time and date information • DHCP server • Onboard event management • Test and trace facilities • POST (power on self tests) diagnostics • Standards based SNMP implementation supporting SNMP v1, v2 and v3 for monitoring and management purposes • IPMI based management of the onboard AMC slots (AMC.*) • Persistent storage of configuration across restarts • Support for retrieving and installing multiple configurations • Support for hot-plugging of the hub board as well as AMCs

Supported MIBS	• Switching Package MIBs
	  • RFC 1213 - MIB-II
	  • RFC 1493 - Bridge MIB
	  • RFC 1643 - Ethernet-like -MIB
	  • RFC 2233 - The Interfaces Group MIB using SMI v2
	  • RFC 2618 - RADIUS Authentication Client MIB
	  • RFC 2620 - RADIUS Accounting MIB
	  • RFC 2674 - VLAN & Ethernet Priority MIB
	  • RFC 2819 - RMON Groups 1,2,3 & 9
	  • RFC 3291 - Textual Conventions for Internet Network Addresses
	  • IANA-ifType-MIB
	  • IEEE 802.1X MIB (IEEE8021-PAE-MIB)
	  • IEEE 802.3AD MIB (IEEE8021-AD-MIB)
	• Routing Package MIBs
	  • IANA-Address-Family-Numbers-MIB
	  • RFC 1724 - RIP v2 MIB Extension
	  • RFC 1850 - OSPF MIB
	  • RFC 2787 - VRRP MIB
	• QoS Package MIB
	  • RFC 3289 - DIFFSERV-MIB & DIFFSERV-DCSP-TC MIBs
	• FASTPATH Enterprise MIB
	  • Support for all managed objects not contained in standards based MIBs.

Table 1-4: AT8904M Software Specification (Continued)

AT8904M	SPECIFICATIONS
Bootloader	u-boot Version 1.1.2 • POST • multi image support • loadable bootimage via network (bootp/tftp) • reliable field upgradable • H/W protected • KCS interface to IPMC • serial console support
Operating System	• MontaVista Linux Professional Edition 3.1

Chapter 2

Installation

2. Installation

The AT8904M has been designed for easy installation. However, the following standard precautions, installation procedures, and general information must be observed to ensure proper installation and to preclude damage to the board, other system components, or injury to personnel.

2.1 Safety Requirements

The following safety precautions must be observed when installing or operating the AT8904M. Kontron assumes no responsibility for any damage resulting from failure to comply with these requirements.



Warning!

Due care should be exercised when handling the board due to the fact that the heat sink can get very hot. Do not touch the heat sink when installing or removing the board.

In addition, the board should not be placed on any surface or in any form of storage container until such time as the board and heat sink have cooled down to room temperature.



Note ...

Certain ATCA boards require bus master and/or rear I/O capability. If you are in doubt whether such features are required for the board you intend to install, please check your specific board and/or system documentation to make sure that your system is provided with an appropriate free slot in which to insert the board.



ESD Equipment!

This ATCA board contains electrostatically sensitive devices. Please observe the necessary precautions to avoid damage to your board:

- Discharge your clothing before touching the assembly. Tools must be discharged before use.
- When unpacking a static-sensitive component from its shipping carton, do not remove the component's antistatic packing material until you are ready to install the component in a computer. Just before unwrapping the antistatic packaging, be sure you are at an ESD workstation or grounded. This will discharge any static electricity that may have built up in your body.
- When transporting a sensitive component, first place it in an antistatic container or packaging.
- Handle all sensitive components at an ESD workstation. If possible, use antistatic floor pads and workbench pads.
- Handle components and boards with care. Don't touch the components or contacts on a board. Hold a board by its edges or by its metal mounting bracket.
- Do not handle or store system boards near strong electrostatic, electromagnetic, magnetic, or radioactive fields.

2.2 AT8904M Initial Installation Procedures

The following procedures are applicable only for the initial installation of the AT8904M in a system. Procedures for standard removal and hot swap operations are found in their respective chapters.

To perform an initial installation of the AT8904M in a system proceed as follows:

1. Ensure that the safety requirements indicated in section 2.1. are observed.



Warning!

Failure to comply with the instruction below may cause damage to the board or result in improper system operation.

2. Ensure that the board is properly configured for operation in accordance with application requirements before installing. For information regarding the configuration of the AT8904M refer to Chapter 4. For the installation of AT8904M specific peripheral devices and rear I/O devices refer to the appropriate chapters.



Warning!

Care must be taken when applying the procedures below to ensure that neither the AT8904M nor other system boards are physically damaged by the application of these procedures.

3. To install the AT8904M perform the following:
    1. Carefully insert the board into the slot designated by the application requirements for the board until it makes contact with the backplane connectors.



Warning!

DO NOT push the board into the backplane connectors. Use the ejector handles to seat the board into the backplane connectors.

    2. Using the ejector handle, engage the board with the backplane. When the ejector handle is locked, the board is engaged.
    3. Fasten the front panel retaining screws.
    4. Connect all external interfacing cables to the board as required.
    5. Ensure that the board and all required interfacing cables are properly secured.

4. The AT8904M is now ready for operation.

2.3 Standard Removal Procedures

To remove the board proceed as follows:

1. Ensure that the safety requirements indicated in section 2.1. are observed.



Warning!

Care must be taken when applying the procedures below to ensure that neither the AT8904M nor system boards are physically damaged by the application of these procedures.

2. Disconnect any interfacing cables that may be connected to the board.
3. Unscrew the front panel retaining screws.
4. Wait until the blue LED is fully ON, this mean that the hot swap sequence is ready for board removal.
5. Disengage the board from the backplane by using both board ejection handles
6. After disengaging the board from the backplane, pull the board out of the slot.

2.4 AMC Installation

To install an AMC proceed as follows:

1. Remove the AMC filler panel.
2. Carefully engage the AMC into the card guide. Push the AMC until it fully mate with its connector. Secure the AMC handle to the locking position.
3. In normal condition, the blue LED shall turn ON as soon as the AMC is fully inserted. It will turn OFF at the end of the hot swap sequence.

2.5 Software Installation

The AT8904M comes as a pre-installed system with all necessary OS, Filesystem, drivers and applications factory-installed with default configurations.

Updating the Software with new Operating System or applications or new versions is provided by a dedicated update mechanism, which is described in Chapter 4.

2.6 CLI Quick Start

This section gives instructions for (initially) accessing the CLI (Command Line Interface) of the AT8904M Base Fabric using either the Serial Console or the Fast Ethernet management interface (serviceport) on the front plate.

Serial Console CLI can be accessed directly with the appropriate cabling. A console menu allows to enter the Base Fabric console or to perform a system reset. Fast Ethernet access is done by establishing a telnet connection (see below).

In order to use the Fast Ethernet management port for CLI telnet access, an IP address must be assigned. This implies that at least the first CLI access has to be done by Serial Console in order to configure the serviceport IP settings. The corresponding procedure is described in the following. User input is printed in bold letters.

1. Connect to serial port on AT8904M front plate using the adapter described in Chapter 3, section 3.1.

   Port settings are:
   - 9600 bps
   - 8 bit, no parity, 1 stop bit (8N1)
   - no flow control

2. Ensure that the board is powered up.
3. Wait for boot process to complete, i.e. until the console selection menu appears.

```
b - connect Base Fabric console
r - reset system
```

4. Type " b" to connect to the Base Fabric console.

```
Connected to Base Fabric console
Press ^X or ^V to get to menu again
Base fabric switching application Release BETA 6.09 starting

(Unit 1)>

User:
```

5. Log in as admin and enter privileged mode (no passwords required by default).

```
User:admin
Password:
(Base Fabric) >enable
Password:

(Base Fabric) #
```

6. Set IP address and netmask (see below for an example IP address setting).

```
(Base Fabric) #serviceport ip 192.168.168.42 255.255.255.0

(Base Fabric) #
```

   The FE management interface is available as from now.

7. Save configuration by copying it to the flash, confirm by typing “y“.

```
(Base Fabric) #copy system:running-config nvram:startup-config

This operation may take a few minutes.
Management interfaces will not be available during this time.

Are you sure you want to save? (y/n) y

Configuration Saved!

(Base Fabric) #
```

To access the CLI via Fast Ethernet management port, open a telnet connection to the configured IP address, port 23.

For additional information on the system configuration, refer to documentation “*AT8901/02/04M CLI Reference Manual*“.

Chapter 3

Hardware Description

3. Hardware Description

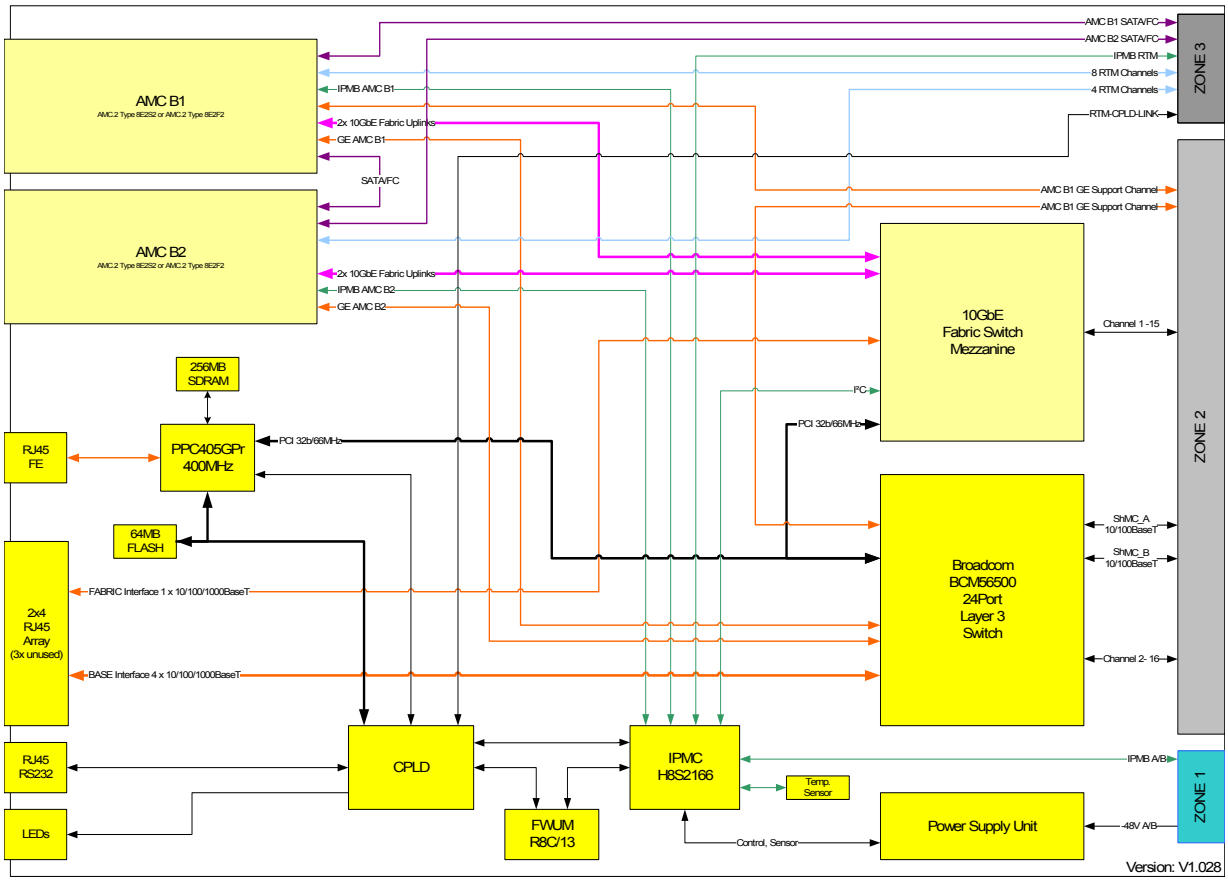
This chapter describes the board specific items of the conventional carrier AdvancedTCA Hub Board AT8904M consisting of the base board and the fabric mezzanine module.

Also described is the AM4310 10GbE Uplink AMC which is available as an optional accessory.

3.1 Base Board

The AT8904M is a PICMG 3.0 and 3.1 compliant Hub Board for AdvancedTCA shelves. It provides a base interface and a 10GbE fabric interface (with the mezzanine), suitable for dual-star and full-mesh configurations in 14 and 16 slot systems. It also provides two mid-size AMC slots for customization.

Figure 3-1: Functional Block Diagram Base Board



The main building blocks of the base board are:

- CPU and Memory
- Base Switch
- Fabric Switch Interface
- AMC Bays
- IPMI
- Synchronization clock
- RTM Interface
- Power Supply

3.1.1 CPU and Memory

The CPU is an IBM PowerPC 405 GPr 400MHz 32-bit RISC processor with 16KB D-cache.

PCI Interface

The PCI interface is a 32bit/66MHz system to control the on-board Broadcom BCM56500 base interface switch and the optional fabric mezzanine module. The internal PCI arbiter of the PowerPC 405 GPr is used.

The virtual PCI slots are ordered in the following way:

Table 3-1: PCI Slots

PCI-Slot	IDSEL	Device
1	0	Base Interface Switch: Broadcom BCM56500
2	1	Fabric Mezzanine Module

Fast Ethernet Management Interface

The internal Fast Ethernet MAC of the PowerPC 405 GPr is used as a management interface. Additionally, a Fast Ethernet PHY transceiver and a RJ45 Connector with integrated magnetics and two LED's, located on the front panel, are used to complete the network interface.

The PHY is controlled via the MDIO interface of the PowerPC 405 GPr. The MDIO address is set to 0. The default setting of the PHY is to operate in auto-negotiation enabled mode, 10/100, Full or Half duplex.

The PHY drives the two LEDs of the RJ 45 Connector, buffered by the CPLD.

The connection is established with a straight through Ethernet cable.

The RJ45 connector has the following pin assignment:

Table 3-2: Fast Ethernet Management (RJ45) Pin Assignment

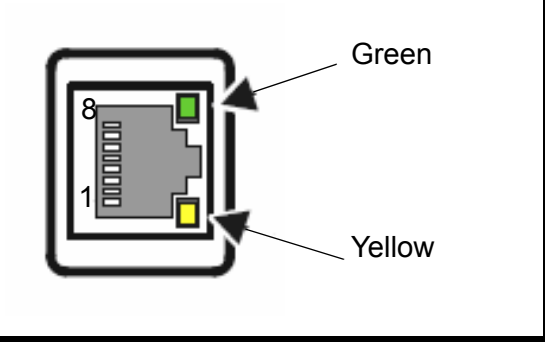
Signal	Pin	
TX+	1	
TX-	2	
RX+	3	
N.C.	4	
N.C.	5	
RX-	6	
N.C.	7	
N.C.	8	

Table 3-3: Fast Ethernet Management (RJ45) LEDs Signification

Speed LED (yellow)		
	OFF	10BASE-T
	ON	100BASE-TX
Status LED (green)		
	OFF	Link Down
	ON	Link Up and no activity
	BLINK	Link up and activity

SDRAM

Five 512Mbit devices, soldered directly onto the PCB, provide 256 Mbyte of SDRAM plus 64 Mbyte for ECC.

The SDRAM interface of the PPC is 32 bit wide and operated at 133 MHz.

Flash

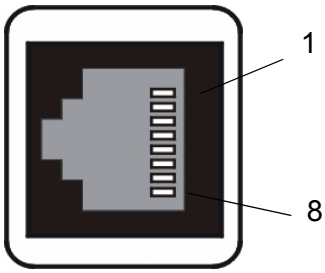
The CPU has two 32 Mbyte Flash Memory devices, which result in 64 Mbyte total Flash memory space. The sector width is 64 Kbyte.

The Flashes are connected to the 32 bit peripheral data bus. The PowerPC 405 GPr accesses the Flashes with CS0#. The sector containing the bootloader code is write protected. The protection can be disabled by setting jumper FWPD.

RS232 Management Interface

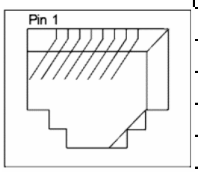
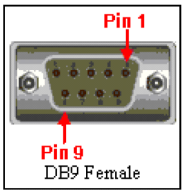
One RS232 interface (UART0) of the PowerPC 405 GPr is connected to the front panel RJ45 connector, the other one (UART1) is used as programming interface for IPMI.

Table 3-4: Serial Port (RJ45) Pin Assignment

Signal	Pin	
RTS	1	
DTR	2	
TXD	3	
GND	4	
GND	5	
RXD	6	
DSR	7	
CTS	8	

External connection is established with a straight through Ethernet cable and a RJ45 (female) to SubD (female) adapter if required. The adapter is described in the following table.

Table 3-5: Serial console terminal cable interface: RJ45 Female to DB9 Female

RJ45 Female	RJ45 Pin Number	Signal	Connected	Description	DB9 Pin Number	DB9 Female
 Front View	1	RTS	Y	Request To Send	8	 Front View
	2	DTR	Y	Data Terminal Ready	6	
	3	TXD	Y	Transmit	2	
	4	GND	N	Ground	-	
	5	GND	Y	Ground	5	
	6	RXD	Y	Receive	3	
	7	DSR	Y	Data Set Ready	4	
	8	CTS	N	Clear To Send	7	
	-	RI	N	Ring Indicator (Not used)	9	
	-	CD	N	Carrier Detect (Not used)	1	

3.1.2 Base Switch

The base switch is a Broadcom BCM56500 24 port GbE multilayer switch that can operate in 10/100/1000 Mbps. It integrates advanced Layer 3 switching features for IPv4 and IPv6 routing. includes enhanced QoS support and jumbo packet line rate switching.

The PPC controls the switch over a 32bit/66MHz PCI Interface.

Base Interface (Zone 2)

The board supports 15+2 ATCA backplane channels. The board can operate in a dual star and full mesh configuration. The switch is connected to the backplane via four 10/100/1000BASE-T quad PHYs and eight 10/100/1000BASE-T dual magnetics. The pin assignment for the Zone 2 connectors is compliant to the PICMG 3.0 standard. GbE channels 0/20 and 0/24 of the switch are the 100BASE-TX ShMC base channels (ShMC cross-connects).

Table 3-6: Base Interface Port Mapping

CLI ID	Channel	LED
0/1	Uplink 1	-
0/2	Uplink 2	-
0/3	Uplink 3	-
0/4	Uplink 4	-
0/5	16	16
0/6	15	15
0/7	14	14
0/8	13	13
0/9	12	12
0/10	11	11
0/11	10	10
0/12	9	9
0/13	8	8
0/14	7	7
0/15	6	6
0/16	5	5
0/17	4	4
0/18	3	3
0/19	2	2
0/20	SMCA	1
0/21	Local AMC B1, channel 0	-
0/22	Remote AMC B1, channel 1	-
0/23	Local AMC B2, channel 0	-
0/24	SMCB	1

Base Interface Uplink

The Hub Board supports four base interface uplinks to the front panel. The switch is connected to the RJ45 connectors with integrated status LEDs on the front panel via a 10/100/1000BASE-T quad PHY and two 10/100/1000BASE-T dual magnetics. GbE channels 0/1 to 0/4 of the switch map to uplink channels 1 to 4.

Table 3-7: Base Uplink (J39/J38) Pin Assignment

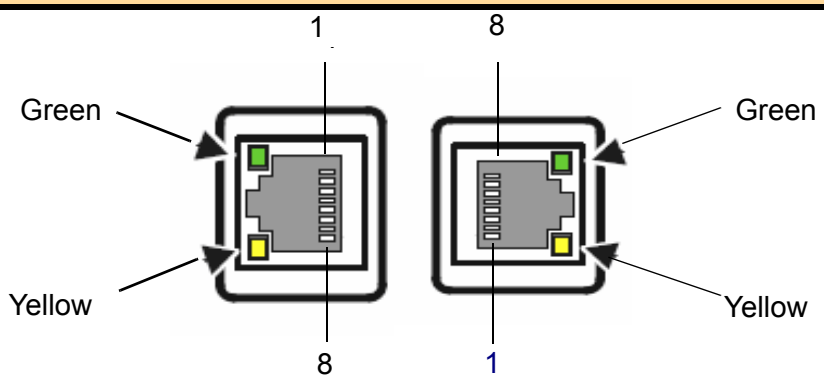
Signal	Pin	
DB+	1	
DB-	2	
DA+	3	
DD+	4	
DD-	5	
DA-	6	
DC+	7	
DC-	8	

Table 3-8: Base Uplink (J39/J38) LEDs Signification

Speed LED (yellow)		
	OFF	10BASE-T
	BLINK	100BASE-TX
	ON	1000BASE-T
Status LED (green)		
	OFF	Link Down
	ON	Link Up and no activity
	BLINK	Link Up and activity

ShMC Cross-connection

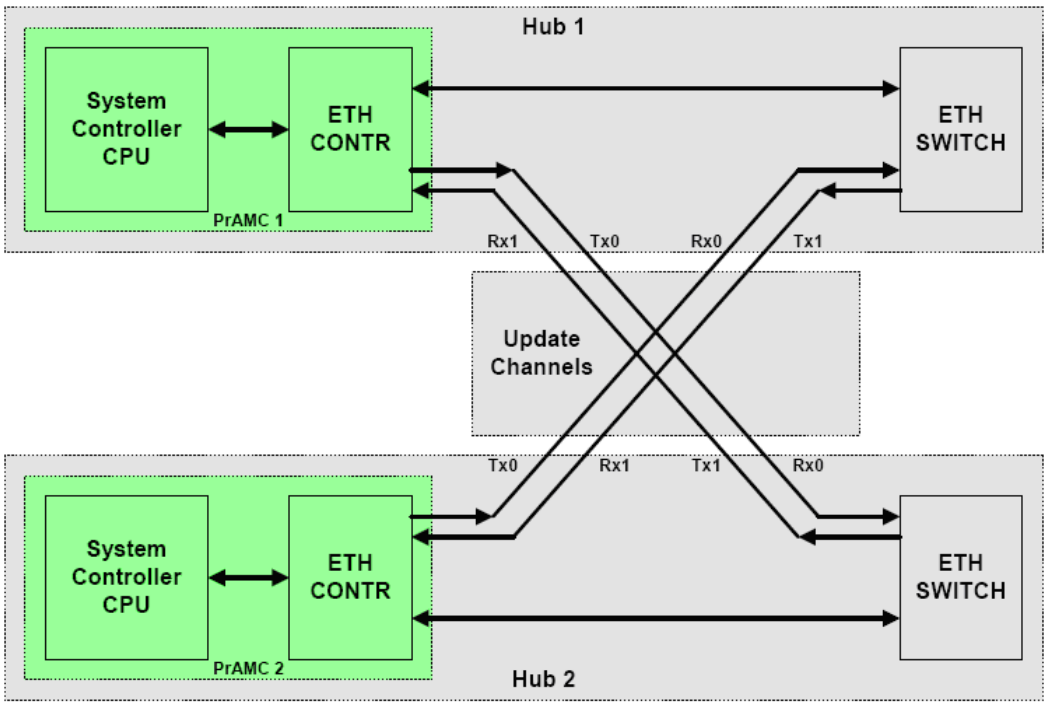
The Hub Board provides two dedicated 10/100BASE-T connections to the shelf managers according to PICMG 3.0 rev. 2 (redundancy shelf manager cross-connection). Port 0/20 is connected to SMCA, 0/24 to SMCB.

AMC GbE Support Channels

Each AMC bay has one GbE connection to the base interface switch (AMC channel 0). On channel 1, AMC bay B1 has an additional link to the backplane update channel, thereby providing a cross-connect to the base switch of the neighbouring, redundant Hub Board.

In applications with a PrAMC used as a system controller in the ATCA Hub Board, the system controller redundancy ensures that a fault in the base switch of one Hub Board does not cut the connection to the redundant Hub Board (see block diagram below). The connection between AMC B1 and the backplane update channel is buffered to allow E-Keying control by the IPMC. However, E-Keying of the connection from the base switch to the update channel does not include disabling the LVDS transmitter lines.

Figure 3-2: Block Diagram AMC GbE Cross-connect via update channels



The block diagram shows one solution for the AMC GbE support channels with a PrAMC as System Controller.

3.1.3 Fabric Switch Interface

The main board provides connection for the mezzanine board allowing various technologies for the backplane fabric interface and AMC fabric interfaces.

The 10GbE option of the AT8904M provided by the mezzanine is described in section 3.2.

The connection interface to the mezzanine consists of three 220 pin high speed connectors.

3.1.4 AMC Bays

Two AMC bays for standard or custom AMCs mid-size and single width are implemented with B+ connectors, which are compliant to the AMC.0 R1.0 specification.

Following AMC Geographic Addresses are implemented:

Table 3-9: AMC Bay Address

AMC	AMC Bay ID	GA [2..0]	IPMB-L Address
1	B1	UGU	7Ah
2	B2	UUG	7Ch

The state of each GA signal is represented by G (grounded), U (unconnected) or P (pulled up to management power).

Table 3-10: AMC B1 Channel Assignment

Channel	Region	Connection
0	GbE	Local Base Switch 0/21
1	GbE	Remote Base Switch 0/22
2	SATA/FC	AMC B2, channel 2
3	SATA/FC	RTM, STOR0
4	Fabric	10GbE Uplink 0/27[0]
5	Fabric	10GbE Uplink 0/27[1]
6	Fabric	10GbE Uplink 0/27[2]
7	Fabric	10GbE Uplink 0/27[3]
8	Fabric	10GbE Uplink 0/28[0]
9	Fabric	10GbE Uplink 0/28[1]
10	Fabric	10GbE Uplink 0/28[2]
11	Fabric	10GbE Uplink 0/28[3]
12	Extended	-
13	Extended	RTM, AMC_B1_P13
14	Extended	RTM, AMC_B1_P14
15	Extended	RTM, AMC_B1_P15
17	Extended	RTM, AMC_B1_P17

Table 3-10: AMC B1 Channel Assignment (Continued)

Channel	Region	Connection
18	Extended	RTM, AMC_B1_P18
19	Extended	RTM, AMC_B1_P19
20	Extended	RTM, AMC_B1_P20
TCLKA	Clock	From backplane CLK3A
TCLKB	Clock	To backplane CLK2A or CLK2B
TCLKC	Clock	From backplane CLK3B
TCLKD	Clock	To backplane CLK1A or CLK1B
FCLKA	Clock	Fabric mezzanine reference clock

Table 3-11: AMC B2 Channel Assignment

Channel	Region	Connection
0	GbE	Local Base Switch 0/23
1	GbE	-
2	SATA/FC	AMC B1, channel 2
3	SATA/FC	RTM, STOR1
4	Fabric	10GbE Uplink 0/25[0]
5	Fabric	10GbE Uplink 0/25[1]
6	Fabric	10GbE Uplink 0/25[2]
7	Fabric	10GbE Uplink 0/25[3]
8	Fabric	10GbE Uplink 0/26[0]
9	Fabric	10GbE Uplink 0/26[1]
10	Fabric	10GbE Uplink 0/26[2]
11	Fabric	10GbE Uplink 0/26[3]
12	Extended	-
13	Extended	-
14	Extended	-
15	Extended	-
17	Extended	RTM, AMC_B2_P17
18	Extended	RTM, AMC_B2_P18
19	Extended	RTM, AMC_B2_P19
20	Extended	RTM, AMC_B2_P20
TCLKA	Clock	From backplane CLK3A
TCLKB	Clock	To backplane CLK2A or CLK2B
TCLKC	Clock	From backplane CLK3B

Table 3-11: AMC B2 Channel Assignment (Continued)

Channel	Region	Connection
TCLKD	Clock	To backplane CLK1A or CLK1B
FCLKA	Clock	Fabric mezzanine reference clock

Interconnects to RTM

AMC Bay B1 has eight generic interconnects to the RTM Zone 3 (channels 13 to 20), B2 has four interconnects (channels 17 to 20). The second SATA/FC port of each AMC Bay (channel 3) is also connected to the RTM.

For further details, please refer to section 3.1.7., RTM Interface.

AMC GbE Support Channels

The first GbE port of each AMC Bay (channel 0) is connected to the base switch, the second one (channel 1) of AMC Bay 1 is also connected to the neighbouring Hub Board via Zone 2 Update Channel.

See also section 3.1.2.

AMC SATA/FC Channels

The first SATA port (channel 2) connects both AMC Bays together. A possible application is a PrAMC in one Bay and a storage AMC in the other. The second SATA port (channel 3) of each AMC Bay is connected to the RTM.

AMC 10GbE Support Channels

Each AMC Bay has two 10GbE/XAUI connections to the fabric mezzanine interface (channels 4 to 11), see also chapters 3.2.1 and 3.3.

Example Configurations

- **PrAMC and storage AMC**
  The preferred PrAMC (e.g. Kontron AM4002) slot is B1, the storage AMC (e.g. Kontron AM4500 SATA AMC) should be placed in B2. This ensures optimal airflow and cooling as well as the possibility to make use of the GbE support channel feature connecting the PrAMC to the base switch of the neighbouring AT8904M.
- **Master Clock Generator (MCG) AMC**
  A MCG AMC providing backplane clocks CLK1A/B and CLK2A/B can be placed in any of the two AMC slots. However, in combination with a PrAMC, the preferred slot is B2.

- **AM4310**
  The 10GbE Uplink AMC AM4310 connects two XAUI interfaces to the fabric switch. On the AT8904M, both AMC slots provide two XAUI interfaces (see chapter 3.2.1).
  If only one AM4310 will be used, the preferred slot is B2. This allows additional use of a PrAMC or MCG AMC in B1.

  For more information on the AM4310, refer to chapter 3.3.

3.1.5 IPMI

The Hub Board supports an intelligent hardware management system, based on the Intelligent Platform Management Interface (IPMI) Specification 1.5. The hardware management system provides the ability to manage the power, cooling and interconnect needs of intelligent devices, to monitor events and to log events to a central repository.

The main building blocks of the IPMI architecture of the AT8904M are:

- IPMC Intelligent Platform Management Controller
- FUM Firmware Update Manager
- CPLD Complex Programmable Logical Device

For further details please refer PICMG 3.0 standard Rev. 2.0.

IPMC

The IPM controller is a 16-bit microcontroller for IPMI applications and it is compliant to IPMI version 1.5 specification. The microcontroller has large on chip memory of 512 Kbyte Flash and 40 Kbyte SRAM. The microcontroller provides six I2C interfaces to have access to the dedicated ShMCs, the AMCs, the fabric mezzanine module, the RTM and the on board peripheral devices such as SEEPROM and temperature sensor. The microcontroller also provides three serial interfaces that are connected to the CPLD.

An LPC interface using the KCS protocol for communication between IPMC and PPC is implemented. IPMC operation is supervised by the FUM.

FUM

The Firmware Update Manager (FUM) is a microcontroller with embedded 16 Kbyte data flash ROM and 1 Kbyte RAM.

The FUM is responsible for field upgrades, rollbacks and watchdog functions of the IPM controller. Four SPI compatible memory devices are connected to the FUM which build up two IPMI firmware banks with 512 Kbyte each. One bank contains a copy of the current IPMC code. The other bank can be written without affecting IPMC operation. Once the bank is updated, the FUM writes its content into the IPMC. IPMC control signals are all buffered in the CPLD so that board operation is not affected during update. In the case of a fault during the update process, the FUM can configure the IPMC with the old firmware that is kept in the other bank. The FUM is also the watchdog timer for the IPMC. There are several control signals to supervise the IPM controller.

CPLD

The CPLD is responsible for connecting the PPC to the IPMC and FUM and for handling the serial interfaces of PPC, IPMC and FUM to the RS232 connector on the front panel. The host interface between PowerPC and CPLD, realized by PPC's External Bus Interface (EBC), is used as CPLD-Register-Interface and as communication interface to IPM controller. The EBC is configured as a demultiplexed 8 Bit Address/Data interface. For accesses to the IPMC Controller, an EBC to LPC (Low Pin Count)-Bridge is included as protocol interface. The LPC interface is for communication between IPMC and PPC over KCS protocol. An additional LPC-IF is connected to the Fabric mezzanine.

The CPLD controls the LEDs for the whole board via shift registers. It handles the signals to monitor the AMCs, fabric mezzanine module and the RTM and handles the signals for the line drivers for the synchronization clocks and the AMC GbE support channels.

An internal multiplexer controls the serial interfaces from the PPC, the FUM and the IPMC. It is possible to connect each device to the other or to the RS232 connector on the front panel.

3.1.6 Synchronization Clock

The Synchronization Clock Interface provides four differential pairs per AMC for clock distribution from the AMCs to the Hub Board and vice versa to enable applications that require the exchange of synchronous timing information among modules and consequently multiple boards in a shelf. This allows modules to source clock(s) to the system in the case where it provides a network interface function, or conversely to receive timing information from another carrier board or module within the system. The four synchronization clock signals are TCLKA, TCLKB, TCLKC and TCLKD, each supported by a differential pair. TCLKB and TCLKD are driven by the AMCs to the backplane and TCLKA and TCLKC are driven from the backplane to the AMCs. AMC1 and 2 cannot transmit or receive simultaneously signals to or from the backplane. Either the CLK signals of AMC1 or the CLK signals of AMC2 are valid. The Hub Board cannot receive any synchronization clocks from other carrier boards, it is only used for distribution. The four differential clock signals are buffered by MLVDS differential line drivers that are controlled by the IPMC and CPLD respectively.

For further details please refer AMC specification AMC0.RC1.1.

3.1.7 RTM Interface

The use of an RTM is optional. I/O signals from the Base Board are routed to Zone 3 where a connector mates with the RTM. The RTM connection is compliant to the PICMG 3.0 standard.

For the connection between the Hub Board and the RTM two daughter card connectors with 40 differential pairs are used.

Each AMC Bay has eight (B1) or four (B2) pairs of generic interconnects to the RTM Zone 3 (AMC_B1_P13 to AMC_B1_P20 and AMC_B2_P17 to AMC_B2_P20). One SATA/FC interface for mass storage from each AMC Slot is implemented (STOR0 and STOR1). Also an I2C IPMI connection is implemented for an intelligent RTM.

The Zone 3 connector has the following pin assignment:

Table 3-12: J30 Pin Assignment

PIN	ROW A	ROW B	ROW C	ROW D	ROW E	ROW F	ROW G	ROW H
1	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	STOR0_ RX-	STOR0_ RX+
2	PROD_IO0	PROD_IO1	N.C.	N.C.	N.C.	N.C.	STOR0_ TX-	STOR0_ TX+
3	12V	3.3V_SUS	SMB_SCL	SMB_ SDA	N.C.	N.C.	STOR1_ RX-	STOR1_ RX+
4	PROD_IO2	PLD_DOUT	PLD_CLK	PLD_DIN	N.C.	N.C.	STOR1_ TX-	STOR1_ TX+
5	JTAG_TDO	TEST_JIG#	N.C.	PROD_IO 3	N.C.	N.C.	N.C.	N.C.
6	JTAG_TDI	12V	N.C.	N.C.	N.C.	12V	N.C.	N.C.
7	JTAG_TCK	PROD_IO4	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.
8	JTAG_TMS	JTAG_ TRST#	N.C.	N.C.	N.C.	SMB_ ALERT#	N.C.	N.C.
9	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.
10	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.

Active Low Signal

Table 3-13: J31 Pin Assignment

PIN	ROW A	ROW B	ROW C	ROW D	ROW E	ROW F	ROW G	ROW H
1	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.
2	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.
3	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.
4	N.C.	N.C.	N.C.	N.C.N.C.	N.C.	N.C.	N.C.	N.C.
5	AMC_B1_ P13_TX+	AMC_B1_ P13_TX-	AMC_B1_ P13_RX+	AMC_B1_ P13_RX-	AMC_B1_ P14_TX+	AMC_B1_ P14_TX-	AMC_B1_ P14_RX+	AMC_B1_ P14_RX-
6	AMC_B1_ P15_TX+	AMC_B1_ P15_TX-	AMC_B1_ P15_RX+	AMC_B1_ P15_RX-	N.C.	N.C.	N.C.	N.C.
7	AMC_B1_ P17_TX+	AMC_B1_ P17_TX-	AMC_B1_ P17_RX+	AMC_B1_ P17_RX-	AMC_B1_ P18_TX+	AMC_B1_ P18_TX-	AMC_B1_ P18_RX+	AMC_B1_ P18_RX-
8	AMC_B1_ P19_TX+	AMC_B1_ P19_TX-	AMC_B1_ P19_RX+	AMC_B1_ P 19_RX-	AMC_B1_ P20_TX+	AMC_B1_ P20_TX-	AMC_B1_ P20_RX+	AMC_B1_ P20_RX-
9	AMC_B2_ P 17_TX+	AMC_B2_ P17_TX-	AMC_B2_ P17_RX+	AMC_B2_ P17_RX-	AMC_B2_ P18_TX+	AMC_B2_ P18_TX-	AMC_B2_ P18_RX+	AMC_B2_ P18_RX-
10	AMC_B2_ P19_TX+	AMC_B2_ P19_TX-	AMC_B2_ P19_RX+	AMC_B2_ P19_RX-	AMC_B2_ P20_TX+	AMC_B2_ P20_TX-	AMC_B2_ P20_RX+	AMC_B2_ P20_RX-

Additional interfaces are implemented for communication to a PLD, JTAG connectivity and production purposes.

3.1.8 Power Supply

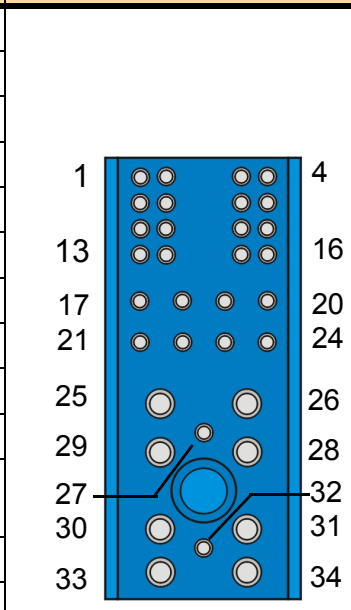
The power supply fulfills the PICMG 3.0 requirements and has the following characteristics:

- Full operation at -38VDC to -72VDC
- No damage inflicted to board at 0VDC to -75VDC
- Typical payload power consumption (no RTM, no AMCs): 67W
- Maximum payload power consumption (no RTM, no AMCs): 100W
- Management power consumption (suspend power): 7W
- Additional AMC payload power consumption: 65W

3.1.8.1 Power Connector

The power connector supplies the board with two 48V redundant rails, digital ground and chassis ground. It also provides the redundant IPMB Shelf Manager connection.

Table 3-14: Power Connector (P10)

Signal	Pin		Pin	Signal
N.C.	1		2	N.C.
N.C.	3		4	N.C.
HA0	5		6	HA1
HA2	7		8	HA3
HA4	9		10	HA4
HA6	11		12	HA5
SCL_A	13		14	SDA_A
SCL_B	15		16	SDA_B
MT1_TIP(N.C.)	17		18	MT2_TIP(N.C.)
RING_A(N.C.)	19		20	RING_B(N.C.)
MT1_RING(N.C.)	21		22	MT2_RING(N.C.)
RRTN_A(N.C.)	23		24	RRTN_B(N.C.)
SHELF_GND	25		26	LOGIC_GND
ENABLE_B	27		28	VRTN_A
VRTN_B	29		30	EARLY_A
EARLY_B	31		32	ENABLE_A
-48V_A	33		34	-48V_B

3.1.8.2 Power Distribution

The 48 Volts are supplied by the backplane via two independent rails, primary (A) and secondary (B). The rails are mixed using power Schottky rectifiers. A 7A fuse protects each -48V line and a 10A fuse protects each RTN line. A hot swap controller enables the 48V power to the board.

A quarter brick DC/DC converter transforms the 48 Volts to secondary 12 Volts, which are distributed on the board. The converter allows a maximum of 14A output current.

Two different management voltages (3.3V and 5V) and five payload voltages (3.3V, 2.5V, 1.8V, 1.25V and 1.2V) are generated by point of load converters. These are either switches or linear regulators.

The management (or suspend) power is present once the board is connected to the backplane. It supplies the IPMI part which in turn controls the payload power. The various payload voltages are sequenced. The initial power up sequence is as follows (20ms delay between steps):

1. 3.3V, 1.8V and fabric mezzanine
2. 2.5V, 1.25V and 1.2V

The Power Down Sequence is performed in reversed order with a 1ms delay.

3.1.8.3 Power Supply AMCs

Each AMC has its own power supply. The 12V payload power is generated by a hot swap controller and for the 3V3 management power a current limit switch is used. The maximum power dissipation for an AMC is 60W. Both AMCs together must not consume more than 65W.

For further details please refer the AMC Specification.

3.1.8.4 Power Supply RTM

The RTM has its own power supply. The 12V payload power is generated by a hot swap controller and for the management power a current limit switch is used. The maximum power dissipation for an RTM is 10W.

For further details please refer the PICMG 3.0 standard.

3.1.8.5 Power Transients

The board provides continuous operation in the presence of transients shown in the following table of the PICMG 3.0 standard:

Table 3-15: Power Transients

Voltage	Duration	Comments	Protected by
- 200 Volts	5 µs	- 100 to - 200 Volts	Frame or Shelf
- 100 Volts	10 µs	- 75 to - 100 Volts	Board
- 75 Volts	10 ms	10 Volts per ms-Rise or Fall	Board
- 0 Volts	5 ms	50 Volts per ms-Fall 12.5 Volts per ms-Rise Assumes prior voltage is above -44 VDC for Shelves, -43 VDC for Boards	Board

In case of a 0V transient the board is able to keep the board alive for 8ms. The necessary energy is buffered in a capacitor. The load time for the capacitor is 100s.

3.1.8.6 Optional Chassis to Logic Ground Connection

According to NEBS requirement R9-14 of GR-1089-CORE issue 3, the AT8904M provides a connection between chassis and logic ground. It is made up of a screw that connects the PCB to the bottom sheet.

If chassis and logic ground shall be isolated, the screw with its washer can be removed. It is located near the jumper header J11 and is labelled "GND TO CHASSIS".

3.1.9 Reset

The reset chain is based on seven elements. The first element in the chain is the voltage supply monitor, followed by the CPLD, FUM, IPMC, Payload voltage, PPC and Base Interface and finally the Fabric Interface.

The reset switch will perform a reset on the CPU when pressed for less than 1 second and a complete board reset (including IPMI) when pressed for more than 2 seconds.

3.1.10 Jumpers

Five jumpers in the upper right corner allow debug settings (J11). The IPMI override jumpers enable bypassing communication with the ShMC for bench operation. The JTAG jumpers configure the boundary scan path. JTAG operation requires the use of an RTM.



Warning!

Operation with any of these jumpers set is not supported by the standard application software.

Table 3-16: Jumper Settings (• Default Setting)

FWPD - Flash Write Enable	
Write Enable	in
• Write Protect	out
IPMC0 - Front Board IPMI Override	
ShMC Bypass	in
• Normal Operation	out
IPMC1 - AMC IPMI Override	
ShMC Bypass	in
• Normal Operation	out
JTAG_AMC - AMC JTAG Integration	
Included in JTAG Chain	in
• Excluded from JTAG Chain	out
JTAG_IPMC - IPMC JTAG	
Restrict JTAG to IPMC	in
• Normal JTAG Operation	out

3.1.11 Display Elements

Figure 3-3: AT8904M Front Panel

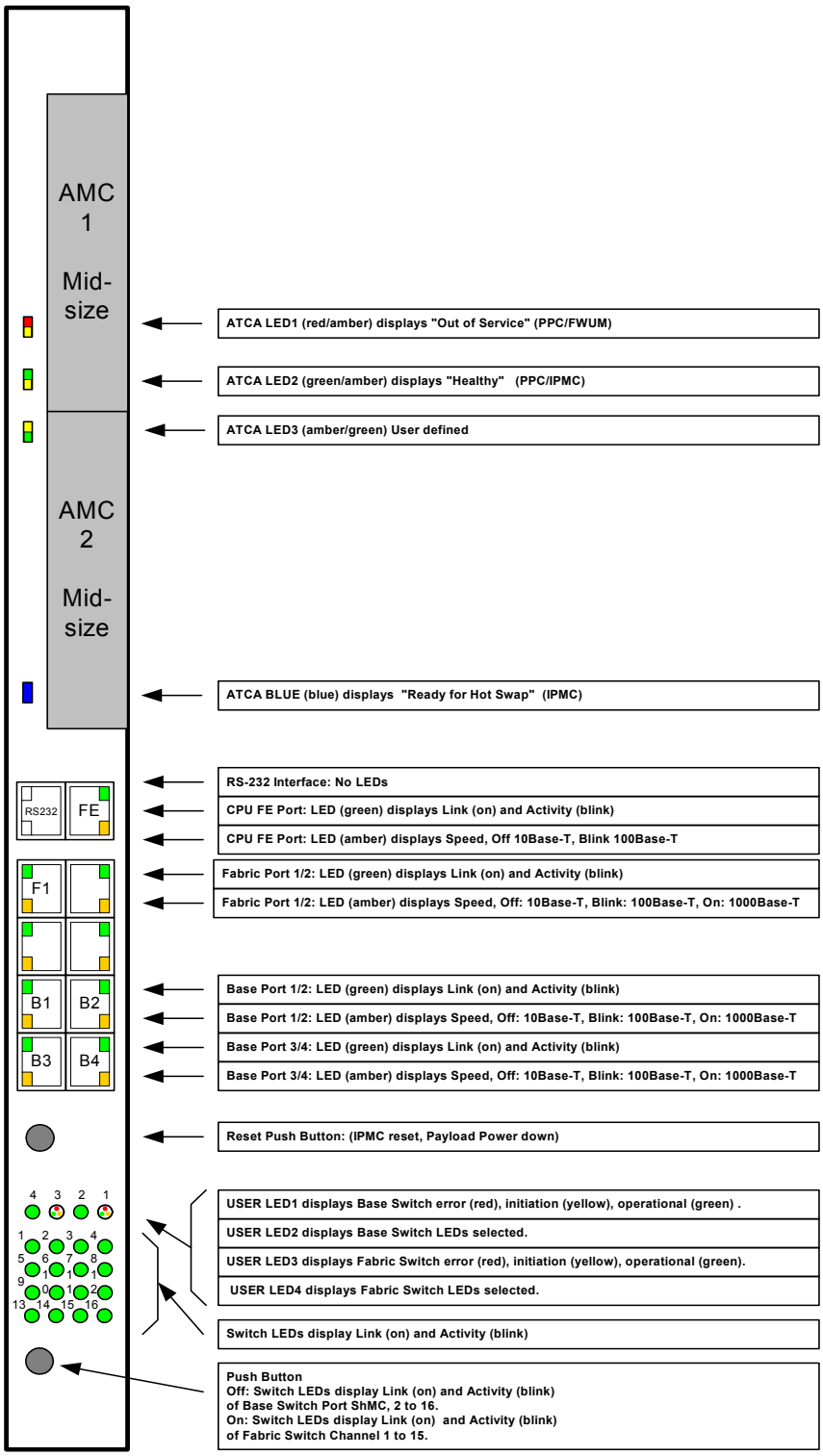


Table 3-17: ATCA LEDs Signification

LED	Signification
ATCA LED3 (HB) (amber/green)	User definable
ATCA LED2 (HY) (green/amber)	On=Healthy (PPC/IPMC), Blink=Sensor out of range
ATCA LED1 (OOS) (red/amber)	On=Out of Service (PPC/FUM) Blink=Firmware Update in Progress or Power denied
ATCA BLUE LED (H/S)	On=Ready for Hot Swap (IPMC) Blink=Hot Swap in Progress

Figure 3-4: Backplane Switch LEDs Signification

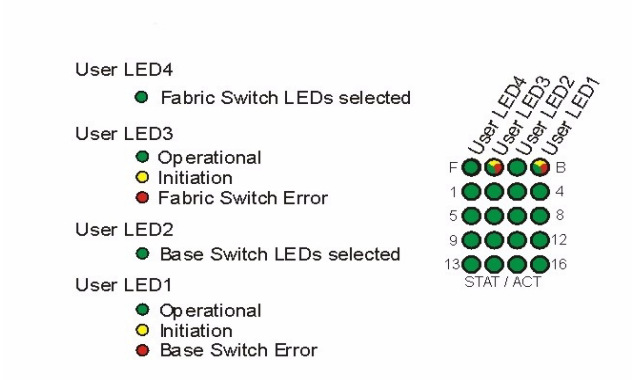


Table 3-18: Backplane Link LEDs Signification

STAT/ACT LEDs 1-16	
OFF	Link Down
ON	Link Up and no activity
BLINK	Link Up and activity

The four front panel ATCA LEDs (ATCA LEDs 1 to 3 and the Blue LED alongside the AMC slots) display the board's health and hotswap status (see table 3-17). Four User LEDs (see figure 3-4) and 16 STAT/ACT LEDs give status information for the base and fabric switches and their links.

The LED push button toggles between the display of the base interface's and the fabric interface's links. User LEDs 2 (base IF) and 4 (fabric IF) indicate which interface's links' status and activity are currently displayed by the 16 STAT/ACT LEDs.

The STAT/ACT LED number on the front plate indicates the logical ATCA slot (not the channel number) of the connection. LED 1 for the base interface is the combined status/activity LED for both ShMC links. If any of the two ShMC links is up, the LED is lit. If any of the links is active, the LED blinks. LED 1 is not used for the fabric interface.

For the 10 GbE fabric interface, the STAT/ACT LEDs do not display activity. They only indicate the link status by being lit when the link is established.

Each RJ45 displays the status of the link with the two integrated LEDs.

The reset switch will perform a reset on the CPU when pressed for less than 1 second and a complete board reset (including IPMI) when pressed for more than 2 seconds.

Switch LED Assignment

Table 3-19: Switch LED Assignment

Switch LED Number	Base Interface	Fabric Interface	Logical ATCA Slot
1	SMCA/B (Ch 1)	-	ShMC (s)
2	Ch 2	Ch 1	(other Hub)
3	Ch 3	Ch 2	3
4	Ch 4	Ch 3	4
5	Ch 5	Ch 4	5
6	Ch 6	Ch 5	6
7	Ch 7	Ch 6	7
8	Ch 8	Ch 7	8
9	Ch 9	Ch 8	9
10	Ch 10	Ch 9	10
11	Ch 11	Ch 10	11
12	Ch 12	Ch 11	12
13	Ch 13	Ch 12	13
14	Ch 14	Ch 13	14
15	Ch 15	Ch 14	15
16	Ch 16	Ch 15	16

3.2 Fabric Mezzanine

This section describes the board specific items of the fabric mezzanine module.

The mezzanine is a PICMG 3.1 compliant module for the AT8904M AdvancedTCA Hub Board from Kontron. It provides a fabric interface switch with twenty 10GbE ports.

The mezzanine module is supplied by the 3V3 management power and the 12V payload power. The module is controlled by the IPM controller via an I2C interface. The interface is connected to the JTAG chain for boundary scan test ability.

The board is compatible to the following standards:

- PICMG 3.0 AdvancedTCA Base Specification, Revision 2.0
- PICMG 3.1 Ethernet/Fibre Channel for AdvancedTCA Systems, Revision 1.0
- IPMI v1.5. Intelligent Platform Management Interface Specification

The main building blocks of the fabric mezzanine are:

- Fabric Switch
- IPMI
- Power Supply

3.2.1 Fabric Switch

The fabric switch is a Broadcom BCM56800 20 port 10 GbE multilayer switch. It integrates advanced Layer 3 switching features for IPv4 and IPv6 routing and includes enhanced QoS support and jumbo packet line rate switching.

The PPC controls the switch over a 32bit/66MHz PCI Interface.

Fabric Interface (Zone 2)

The Fabric Interface is comprised of 15 channels providing connectivity among up to 16 boards in a Full Mesh or Star configuration. The Fabric Interface can be used in a variety of ways by Boards and Backplanes to meet the needs of many applications defined by the PICMG 3.0 Revision 2.0 standard. The pin assignment for the Zone 2 connectors is compliant to the PICMG 3.0 standard.

Table 3-20: Fabric Interface Port Mapping

CLI ID	Channel	LED
0/1	AMC B2 Port 4-7	-
0/2	AMC B2 Port 8-11	-
0/3	FC1	2
0/4	FC2	3
0/5	FC3	4
0/6	FC4	5
0/7	FC5	6
0/8	FC10	11
0/9	FC9	10
0/10	FC8	9
0/11	FC7	8
0/12	FC6	7
0/13	FC15	16
0/14	FC14	15
0/15	FC13	14
0/16	FC12	13
0/17	FC11	12
0/18	AMC B1 Port 8-11	-
0/19	AMC B1 Port 4-7	-
0/20	Uplink Port 1	-

Fabric Interface Uplink

The mezzanine supports one fabric interface uplinks to the front panel of the Hub Board which is converted to 10/100/1000BASE-T. The switch is connected to the RJ45 connector with integrated status LEDs on the front panel via a media converter and magnetics. GbE channel 0/20 of the switch maps to uplink channel 1

The RJ45 connector has the following pin assignment:

Table 3-21: Fabric Uplink (J40/J41) Pin Assignment

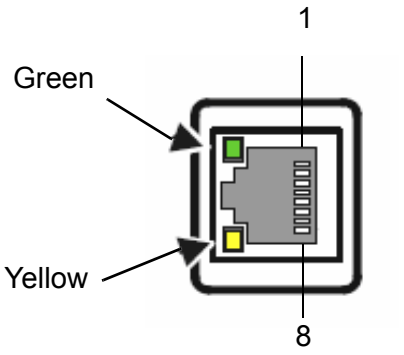
Signal	Pin	
DB+	1	
DB-	2	
DA+	3	
DD+	4	
DD-	5	
DA-	6	
DC+	7	
DC-	8	

Table 3-22: Fabric Uplink (J40/J41) LEDs Signification

Speed LED (yellow)		
	OFF	10BASE-T
	BLINK	100BASE-TX
	ON	1000BASE-T
Status LED (green)		
	OFF	Link Down
	ON	Link Up and no activity
	BLINK	Link Up and activity

10GbE Uplink to AMC Bays

The fabric mezzanine module provides four 10GbE connections to AMC B2 and AMC B1 of the Hub Board . Together with the AM4310 10GbE Uplink AMC, a high speed shelf interconnect is possible (see chapter 3.3).

3.2.2 IPMI

The Management is done by the IPMI controller of the Hub Board. The mezzanine is connected by an I2C interface the IPM controller on the base board. It provides an EEPROM with 64Kbyte RAM for module information. Voltage and temperature measurement is done by a 10-Bit digital temperature sensor with eight channels ADCs.

3.2.3 Power Supply

The power supply is designed according the PICMG 3.0 standard. The board power sequencing is done by the IPMI controller of the Hub Board.

The base board provides the 3V3_SUS management power supply for the mezzanine. The power is used to supply all management relevant parts.

12V payload power are also supplied by the base board. They are used to derive the 3V3, 2V5 and the 1V25 power supply for the mezzanine module payload.

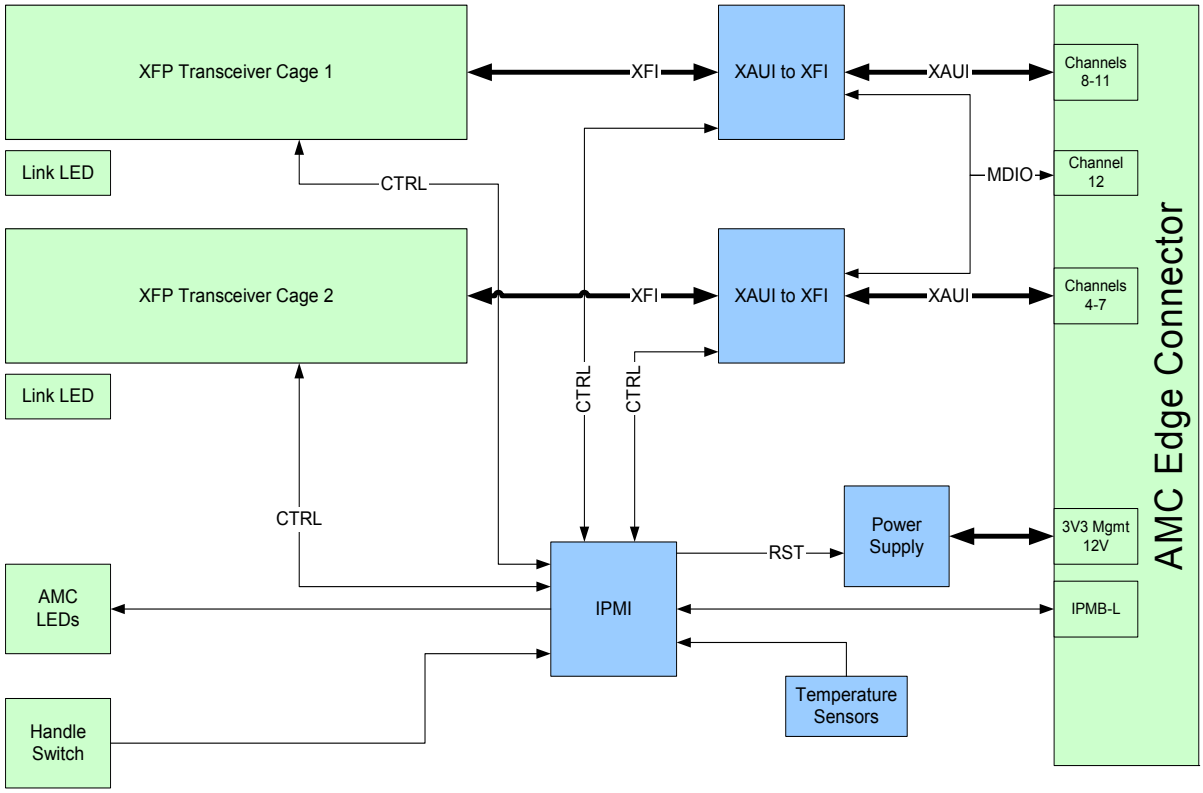
Maximum power consumption of the fabric mezzanine module is 35W.

3.3 AM4310

The AM4310 is a PICMG AMC.0 R1.0 ECN002 compliant Advanced Mezzanine Card module with two 10 Gigabit Ethernet ports. It is designed for operation with the AT8904M ATCA hub blade to equip it with up to four high speed chassis interlink ports.

The AM4310 adapts the two 10 GbE XAUI ports of the PICMG AMC.2 compliant edge connector to the XFP connectors on the front panel.

Figure 3-5: AM4310 Block Diagram



The main building blocks of the AM4310 are:

- XFP Ports
- XAUI to XFI Transceivers
- IPMI
- Power Supply

3.3.1 XFP Ports

The AMC module contains two 10 GbE XFP uplinks at the front panel. XFP modules are not provided with the AM4310 and have to be obtained separately. The XFP uplink ports are according to the SFF Committee, INF-80077i, rev. 4.0, 10 Gigabit Small Form Factor Pluggable Module (XFP). Modules with -5.0V are not supported. An application note with a list of XFP modules successfully operated in the AM4310 is available upon request.



Caution!

Do not look into the laser beam!
The XFP modules are fitted with a class 1 or 1M laser. To avoid possible exposure to hazardous levels of invisible laser radiation, do not exceed maximum ratings.



Warning!

The XFP cages have heatsinks which can dissipate 1.5W with no airflow. If the XFP module consumes more than 1.5W (up to 3.5W), the user has to ensure sufficient airflow to cool the XFP module. Otherwise, the modules may be damaged.

The XFP cages have the following pin assignment.

Table 3-23: XFP Connector Pin Assignment

Pin No	Signal	Description
1	GND	Module Ground
2	VEE5	Not connected
3	MOD_DE_SEL	Module De-select; When held low, allows module to respond to 2-wire serial interface
4	INTERRUPT#	Not connected
5	TX_DIS	Transmitter Disable; Turns off transmitter laser output
6	VCC5	+5V Power Supply
7	GND	Module Ground
8	VCC3	+3.3V Power Supply
9	VCC3	+3.3V Power Supply
10	SCL	I²C Serial Interface Clock
11	SDA	I²C Serial Interface Data Line

Table 3-23: XFP Connector Pin Assignment (Continued)

Pin No	Signal	Description
12	MOD_ABS	Indicates Module is not present. Grounded in the Module
13	MOD_NR	Module Not Ready; Indicating XFP Module Operational Fault
14	RX_LOS	Receiver Loss Of Signal Indicator
15	GND	Module Ground
16	GND	Ground
17	RD-	Transmitter Inverted Data Input
18	RD+	Transmitter Non-Inverted Data Input
19	GND	Ground
20	VCC2	+1.8V Power Supply
21	P_DOWN/RST	Power down: When high, requires the module to limit power consumption to 1.5W or below. I²C serial interface must be functional in the low power mode. Reset: The falling edge initiates a complete reset of the module including the I²C serial interface, equivalent to a power cycle.
22	VCC2	+1.8V Power Supply
23	GND	Ground
24	REFCLK+	Reference Clock Non-Inverted Input, AC coupled on the host board
25	REFCLK-	Reference Clock Inverted Input, AC coupled on the host board
26	GND	Module Ground
27	GND	Module Ground
28	TD-	Receiver Inverted Data Output
29	TD+	Receiver Non-Inverted Data Output
30	GND	Module Ground

3.3.2 XAUI to XFI Transceivers

The two XAUI to XFI transceivers have a 4-lane XAUI interface with 2.5MHz MDIO management interface. They incorporate a fully-integrated clock multiplication unit (CMU), clock and data recovery (CDR), SerDeses and limiting amplifiers. The transceiver operates in asynchronous clock mode which is provided by the elastic buffers. For configuration options of the transceivers, refer to the AT8902 CLI Reference Manual.

On the AMC edge connector, AMC channels 4 to 7 map to the XAUI port of the transceiver for XFP1 and AMC channels 8 to 11 to the transceiver XAUI port for XFP2. The user definable channel 12 contains the MDIO control connection between the fabric switch and the AMC's XAUI to XFI transceivers.

The AT8904M provides four 10GbE uplinks connected to the fabric switch. The following table shows the available connections.

Table 3-24: Fabric Interface 10GbE Port Mapping

CLI ID	10GbE Port in AMC slots
0/18	AMC B1 XFP1
0/19	AMC B1 XFP2
0/2	AMC B2 XFP1
0/1	AMC B2 XFP2

3.3.3 IPMI

The AM4310 supports an intelligent hardware management system based on the Intelligent Platform Management Interface (IPMI).

The main building blocks of the IPMI architecture are:

- MMC (Module Management Controller)
- FUM (Firmware Upgrade Manager)

MMC

The MMC interacts with the IPMC on the base board through the IPMB-L-interface. The controller provides the information about the AMC module, reports voltage levels and the temperature at three different spots on the PCB.

FUM

The FUM controls the MMC firmware update. Two EEPROM banks are connected to the FUM, one for the old firmware image and one for the new image. During an update, the new firmware image will be programmed in one of the two EEPROMs. This new image is then programmed into the MMC under control of the FUM. If the MMC does not start correctly with the new image, the previous image of the other EEPROM will be programmed in the MMC.

3.3.4 Power Supply

The module power supply consists of two parts, management power supply (3V3_SUS) and payload power supply (12V).

Management power supplies the Module Management Controller (MMC) as well as associated circuits like temperature sensors, FRU Data EEPROM, voltage and current measurement circuits and Firmware Update Manager with associated memory.

Payload power can only be switched on if management power is present and the module is safely inserted into the AMC slot (signal PS1# is active). Payload power is activated by the carrier board upon successful negotiation with the MMC.

The 12V payload power feeds local point of load DC/DC converters which provide the individual payload voltages.

The following table shows the maximum current of the AMC module with XFP modules populated (each consuming 3.5W).

Table 3-25: Power Consumption

Voltage	Maximum current
12V	2A
3V3 management	83mA

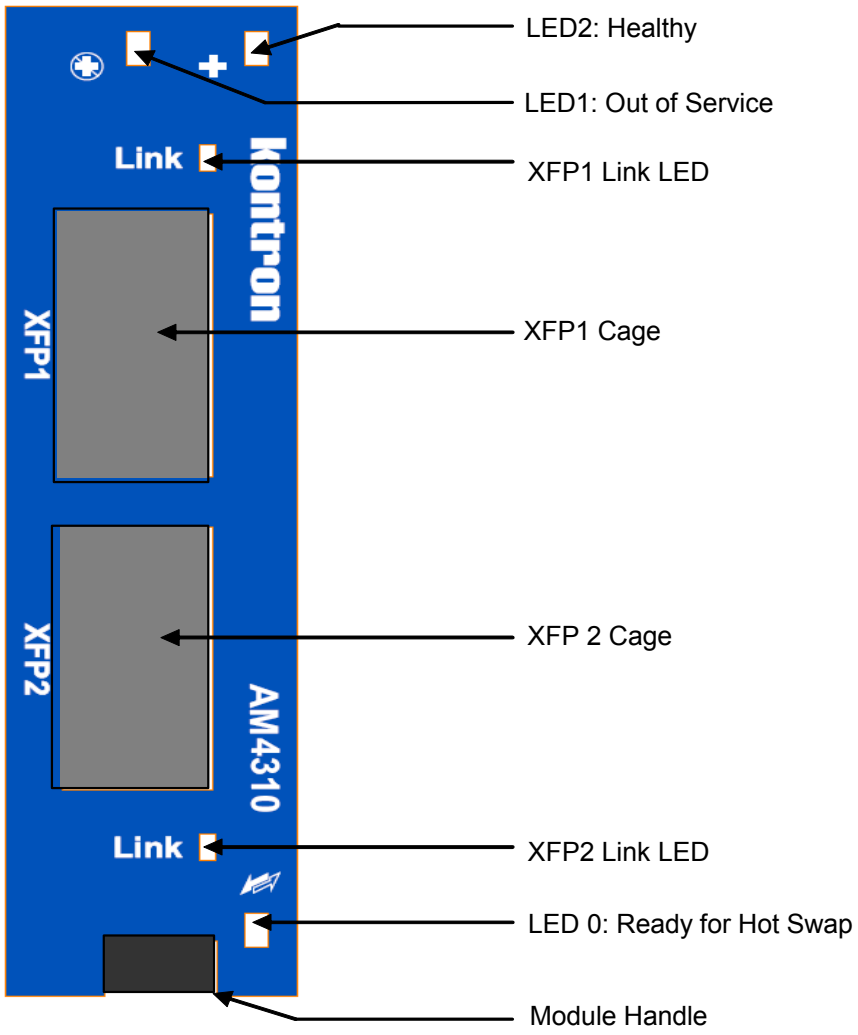
3.3.5 Reset

The reset logic is controlled by two voltage monitoring devices. Once the management power is stable and the AMC is enabled by the base board, the IPMI reset is released.

The reset-signals for the PHY devices are released by the MMC after the AMC is activated by the shelf manager and all payload voltages are ok.

3.3.6 Front Plate Elements

Figure 3-6: AM4310 Front Plate



The functionality of the ATCA LEDs is as indicated in the table below.

Table 3-26: ATCA LEDs Signification

LED	Colour	Functional Description
LED 0 Ready for Hot Swap	Blue	On when board is ready to be hot swapped. Short Blink during 'deactivation in progress'. Long Blink during 'activation in progress'.
LED 1 Out of Service	RED (Default)	On when MMC is not working or payload power not granted (controlled by FWUM). Blinking during F/W upgrade.
LED 2 Healthy	Green/ Amber	Green when MMC is active and all sensors are within limits. Amber when one or more sensors are out of inner limit.
XFP1 Link LED	Green	Data link established on XFP1
XFP2 Link LED	Green	Data link established on XFP2
Module Handle		To activate the AMC payload and for extracting the module.

Chapter 4

Software Description

4. Software Description

Software on the AT8904M includes the following parts:

- Bootloader
- OS (rootFS, kernel)
- Application SW
- IPMI FW

The Software accomplishes operation of the switching hardware and is therefore also referenced as firmware. It is preinstalled on the system and can only be updated by a dedicated update procedure. This manual only describes bootloader, its self tests and IMPI Firmware and introduces the update procedure.

For additional information of system configuration using CLI commands refer to documentation "*AT8901/02/04M CLI Reference Manua*l".

4.1 Supported RFCs

The Software supports the following standards and RFCs.

4.1.1 Management

- RFC 826 - ARP
- RFC 854 - Telnet
- RFC 855 - Telnet Option
- RFC 1155 - SMI v1
- RFC 1157 - SNMP
- RFC 1212 - Concise MIB Definitions
- RFC 1867 - HTML/2.0 Forms w/ file upload extensions
- RFC 1901 - Community based SNMP v2
- RFC 2068 - HTTP/1.1 protocol as updated by draft-ietf-http-v11-spec-rev-03
- RFC 2246 - The TLS Protocol, Version 1.0
- RFC 2271 - SNMP Framework MIB
- RFC 2295 - Transparent Content Negotiation
- RFC 2296 - Remote Variant Selection; RSVA/1.0 State Management "cookies"
- RFC 2346 - AES Ciphersuites for Transport Layer Security

- RFC 2576 - Coexistence between SNMP v1,v2 & v3
- RFC 2578 - SMI v2
- RFC 2579 - Textual Conventions for SMI v2
- RFC 2580 - Conformance statements for SMI v2
- RFC 2818 - HTTP over TLS
- RFC 3410 - (Informational): Introduction and Applicability Statements for Internet Standard Management Framework (December 2002)
- RFC 3411 - An Architecture for Describing SNMP Management Frameworks (December 2002)
- RFC 3412 - Message Processing and Dispatching (December 2002)
- RFC 3413 - SNMP Applications (December 2002)
- RFC 3414 - User-based Security Model (December 2002)
- RFC 3415 - View-based Access Control Model (December 2002)
- RFC 3416 - Version 2 of SNMP Protocol Operations (December 2002)
- RFC 3417 - Transport Mappings (December 2002)
- RFC 3418 - Management Information Base (MIB) for the Simple Network Management Protocol (SNMP) (December 2002).
- RFC 3635 Definition of Managed Objects for Ethernet-like Interface Types
- HTML 4.0 Specification - December, 1997
- Java & Java Script 1.3
- SSL 3.0 & TLS 1.0
- SSH 1.5 & 2.0
- Draft-ietf-secsh-transport-16 - SSH Transport Layer Protocol
- Draft-ietf-secsh-userauth-17 - SSH Authentication Protocol
- Draft-ietf-secsh-connect-17 - SSH Connection Protocol
- Draft-ietf-secsh-architecture-14 - SSH Protocol Architecture
- Draft-ietf-secsh-publickeyfile-03 - SECSH Public Key File Format
- Draft-ietf-secsh-dh-group-exchange-04 - Diffie-Hellman Group exchange for the SSH Transport Layer Protocol
- Configurable Management VLAN ID
- Industry Standard CLI

4.1.2 Switching

- IEEE 802.3ac - VLAN Tagging
- IEEE 802.3ad - Link Aggregation with Static LAG and LACP support
- IEEE 802.1S - Multiple Spanning Tree
- IEEE 802.1W - Rapid Spanning Tree
- IEEE 802.1D - Spanning Tree
- GARP
- GVRP - Dynamic VLAN Registration
- GMRP - Dynamic L2 Multicast Registration
- IEEE 802.1Q - Virtual LANs with Port Based VLANs
- IEEE 802.1v - Protocol based VLANs
- IEEE 802.1p - Ethernet Priority with User Provisioning & Mapping
- IEEE 802.1X - Port Authentication
- IEEE 802.3x - Flow Control
- IGMP Snooping
- Port Mirroring
- Broadcast Storm Recovery
- Static MAC Filtering
- Double VLAN / vMAN Tagging
- Jumbo Frames
- IPv6 Classification APIs
- XMODEM
- RFC 768 - UDP
- RFC 783 - TFTP
- RFC 791 - IP
- RFC 792 - ICMP
- RFC 793 - TCP
- RFC 951 - BOOTP
- RFC 1321 - Message Digest Algorithm (MD5)

- RFC 1534 - Interoperation between BOOTP and DHCP
- RFC 2030 - Simple Network Time Protocol (SNTP) Version 4 for IPv4, IPv6 and OSI
- RFC 2131 - DHCP Client
- RFC 2131 - DHCP Server
- RFC 2132 - DHCP Options and BOOTP Vendor Extensions
- RFC 2865 - RADIUS Client
- RFC 2866 - RADIUS Accounting
- RFC 2868 - RADIUS Attributes for Tunnel Protocol Support
- RFC 2869 - RADIUS Extensions
- rfc2869bis - RADIUS support for EAP
- RFC 3176 - InMon Corporation's sFlow: A Method for Monitoring Traffic in Switched and Routed Networks
- RFC 3396 - Encoding Long Option in the Dynamic Host Configuration Protocol (DHCPv4)
- RFC 3580 - 802.1X RADIUS Usage Guidelines
- Draft-ietf-magma-snoop-11.txt - Considerations for IGMP and MLD Snooping Switches

4.1.3 Routing

- Weighted Static Routes
- RFC 819 - Domain Naming Convention for Internet User Applications
- RFC 826 - Ethernet ARPRFC 894 - Transmission of IP Datagrams over Ethernet Networks
- RFC 896 - Congestion Control in IP/TCP Networks
- RFC 919 - Broadcasting Internet Datagrams
- RFC 922 - Broadcasting Internet Datagrams in the presence of subnets
- RFC 950 - Internet Standard Subnetting Procedure
- RFC 1027 - Using ARP to implement transparent subnet gateways
- RFC 1058 - RIP v1
- RFC 1256 - ICMP Router Discovery Messages
- RFC 1321 - Message Digest Algorithm (MD5)
- RFC 1519 - CIDR

- RFC 1723 - RIP v2
- RFC 1765 - OSPF Database Overflow
- RFC 1812 - Requirements for IP Version 4 Routers
- RFC 2328 - OSPF v2 w/ Equal Cost Multipath support
- RFC 3046 - DHCP/BootP Relay
- RFC 3101 - OSPF with NSSA support
- RFC 3768 - Virtual Router Redundancy Protocol (VRRP)
- Route Redistribution across RIP and OSPF
- VLAN Routing

4.1.4 QoS

- Bandwidth Policing (Min and Max; per port/per VLAN)
- Committed Information Rate (CIR)
- Maximum Burst Rate (MBR)
- Per Port (Interface)
- Per VLAN
- Filtering (L3/L4 Access Lists)
- IP Classification - 6 Tuple Classification
- RFC 2474 - DiffServ Definition
- RFC 2475 - DiffServ Architecture
- RFC 2597 - Assured Forwarding PHB
- RFC 3246 - An Expedited Forwarding PHB
- RFC 3260 - New Terminology and Clarifications for DiffServ

4.2 Supported MIBs

The Software supports the following MIBs.

4.2.1 Enterprise MIB

- Support for all managed objects not contained in standards based MIBs.

4.2.2 Switching Package MIBs

- RFC 1213 - MIB-II
- RFC 1493 - Bridge MIB
- RFC 1643 - Ethernet-like -MIB
- RFC 2233 - The Interfaces Group MIB using SMI v2
- RFC 2618 - RADIUS Authentication Client MIB
- RFC 2620 - RADIUS Accounting MIB
- RFC 2674 - VLAN & Ethernet Priority MIB
- RFC 2819 - RMON Groups 1,2,3 & 9
- RFC 2863 – Interfaces Group MIB
- RFC 3291 - Textual Conventions for Internet Network Addresses
- IANA-ifType-MIB
- IEEE 802.1X MIB (IEEE8021-PAE-MIB)
- IEEE 802.3AD MIB (IEEE8021-AD-MIB)

4.2.3 Routing Package MIBs

- Draft-ietf-ipv6-rfc2096-update-07.txt - IP Forwarding Table MIB
- IANA-Address-Family-Numbers-MIB
- RFC 1724 - RIP v2 MIB Extension
- RFC 1850 - OSPF MIB
- RFC 2787 - VRRP MIB

4.2.4 QoS Package MIB

- RFC 3289 - DIFFSERV-MIB & DIFFSERV-DCSP-TC MIBs

4.3 Bootloader

On the AT8904M Hub Board, the bootloader ‘u-boot‘ (universal bootloader) is used. The bootloader initializes the main components of the board like CPU, SDRAM, serial lines etc. for operation. After this, kernel and application are started from flash.

4.3.1 Power On Self Test

4.3.1.1 Test Routines

Upon power on or system reset, the bootloader performs a set of Power On Self Tests (POST) to check the integrity of specific components. Components where a POST is available are:

- SDRAM
- PPC405 serial line
- PPC405 I2C
- PPC405 FE

In the case that a POST fails, a POST error code is written into the postcode high byte register of the onboard CPLD. The boot process is not stopped as there are good chances the board can boot even in case of POST errors. The postcode high byte register is also accessible by the IPMC which can report error codes to a separate management instance. Thus more comprehensive diagnostic tests could be started.

The following table shows a list of available POST routines including POST error codes.

Table 4-1: POST routines and error codes

Device	Test	POST Error Code
SDRAM	Data bus - walking 1 test	PCW_DLINE
SDRAM	Address bus - walking 1 test	PCW_ALINE
SDRAM	Memory - read/write test	PCW_MEM
PPC405 UART	Serial loopback teststring	PCW_SERIAL
PPC405 I2C	Bus scan for devices from I2C_ADDR_LIST	PCW_I2C
PPC405 FE	Phy access	PCW_ETH1
PPC405 FE	Phy loopback test using special Ethernet test frame	PCW_ETH2
KCS	KCS READY signal test	KCSCTL

4.3.1.2 Boot Steps

In addition to the Power On Self Tests described above, the bootloader logs the board startup sequence in the postcode low byte register. A postcode value is written each time a step in the start sequence has been completed successfully. The postcode stored is also accessible by the IPMC. In the case that an error occurs during execution of a step, the boot sequence is stopped because a fatal error has occurred with great likelihood. In this case, a management instance can read the last postcode written via the IPMC and thus determine where the fatal error has occurred.

A list of defined postcodes is shown in the table below.

Table 4-2: POST Boot Steps

POST Step Code	Value	Boot Step
PC_INIT	0x00	Initial PC, EBC has been set up
PC_BINIT	0x01	Board early init (interrupt settings)
PC_CLOCKS	0x02	Get system clocks
PC_TIMEB	0x03	Init timebase
PC_ENVINIT	0x04	Init environment
PC_BAUD	0x05	Init baudrate
PC_SERIAL	0x06	Init UART
PC_CPU	0x07	Check CPU
PC_PHY	0x08	Setup PHY
PC_I2C	0x09	Init I2C
PC_INITRAM	0x0A	Init SDRAM controller and SDRAM
PC_TESTRAM	0x0B	Test SDRAM
PC_INITSEQ	0x0F	Board init sequence completed
PC_INITBOARD	0x10	Board init ok, stack set up ok, board info struct set up
PC_RELOC	0x11	Relocation completed
PC_TRAP	0x18	Setup trap handler
PC_FLASH	0x19	Flash OK
PC_CPU2	0x1A	Init higher level parts of CPU
PC_RELOCENV	0x1B	Relocation of environment Ok
PC_BDINFO	0x1C	Fill missing fields of bdinfo
PC_PCI	0x1D	PCI configuration done
PC_DEVICES	0x1E	Device init done
PC_JUMPTABLE	0x1F	Jumptable init done
PC_CONSOLE	0x20	Console init done
PC_MAIN	0x2F	Enter main loop
PC_START_OS	0x3F	Pass control to OS, leave bootloader

4.4 IPMI Firmware

The PPC communicates with the Intelligent Platform Management Controller (IPMC) using the Keyboard Controller Style (KCS) interface. The bootloader is able to communicate with the IPMC, e.g. for POST error logging purposes and fault resilient purposes.

The memory subsystem of the IPMC consists of an integrated flash memory to hold the IPMC operation code and integrated RAM for data. The field replaceable unit (FRU) inventory information is stored in the nonvolatile memory on an EEPROM connected via a local I2C interface to the IPMC microcontroller. It is possible to store up to 4 Kbytes within the FRU inventory information. Communication over IPMB bus to the ShMC ensures that 'post-mortem' logging information is available even if the main processor becomes disabled.

The IPMC provides six I2C bus connections. Two are used as the redundant IPMB bus connections to the backplane, one is used for IPMB-L bus with AMC modules, one for the connection to a managed RTM, one for the Base Board and Mezzanine Sensors and one is for local EEPROM storage.

If an IPMB bus fault or IPMC failure occurs, IPMB isolators are used to switch and isolate the backplane/system IPMB bus from the faulted Hub Board. If possible, the IPMC activates the redundant IPMB bus to re-establish system management communication to report the fault.

The onboard DC voltage, current, and temperature sensors are monitored by the IPMC microcontroller continuously. The IPMC will log an event into the ShMC's System Event Log (SEL) if any of the thresholds are exceeded.

To increase the reliability of the Hub board management subsystem, an external watchdog supervisor for the IPMC is implemented. The IPMC strobes the external watchdog at two-second intervals to ensure continuity of operation of the board's management subsystem. If the IPMC ceases to strobe the watchdog supervisor for more than six seconds, the watchdog isolates the IPMC from the IPMBs and resets the IPMC. The watchdog supervisor does not reset the payload power and the restart of the IPMC will not affect the payload and will restore the previous Hot Swap state and power level negociated with the ShMC. The external watchdog supervisor is not configurable and must not be confused with the IPMI v1.5 watchdog timer commands.

This external watchdog of the IPMC is implemented in a second microcontroller. This Firmware Upgrade Manager (FUM) is responsible for monitoring the IPMC and for managing the IPMC fail safe firmware upgrade process. The FUM keeps two IPMC Firmware code images in two external SEEPROM memories. If a failure occurs during firmware upgrade, the FUM will automatically rollback to the last known working IPMC firmware image.

4.4.1 Sensor Data Record (SDR)

Every sensor on the Base Board is associated with a Sensor Data Record (SDR). Sensor Data Records contain information about the sensor's identification such as sensor type, sensor name, sensor unit. SDR also contain the configuration of a specific sensor such as threshold/hystheresis and event generation capabilities that specifies sensor behaviour. Some field of the sensor SDR are configurable through IPMI v1.5 commands and are set to built-in initial value. The AT8904M management controller supports sensor devices and uses the IPMI dynamic sensor population feature of IPMI v1.5 to merge the AMC hot swap sensor with the AT8904M sensors population. AMC hot swap events indicated by this sensor are passed to the ShMC. Additionally, the IPMC updates the sensor population change indicator timestamp accessible through the Get Device SDR Info command to remain compliant to IPMI v1.5.

All SDRs can be queried using Device SDR commands. Base Board sensors that have been implemented are listed below.

Table 4-3: AT8904M sensors

IPMI Sensor Name	Unit	Scanning Enabled Under Power State	Health LED/Sensor
IpmC Reboot	discrete	On/Off	No change
IPMI Watchdog	discrete	On/Off	No change
SEL State	discrete	On/Off	No change
IPMB0 Link State	discrete	On/Off	No change
FRU0 IPMBL State	discrete	On/Off	No change
FRU1 IPMBL State	discrete	On/Off	No change
FRU2 IPMBL State	discrete	On/Off	No change
IPMI Info-1	discrete	On/Off	No change
IPMI Info-2	discrete	On/Off	No change
FRU0 Reconfig	discrete	On/Off	No change
FRU0 FRU Agent	discrete	On/Off	No change
FRU1 FRU Agent	discrete	On/Off	No change
FRU2 FRU Agent	discrete	On/Off	No change
EventRcv ComLost	discrete	On/Off	No change
FRU0 Hot Swap	discrete	On/Off	No change
FRU1 Hot Swap	discrete	On/Off	No change
FRU2 Hot Swap	discrete	On/Off	No change
IPMC Storage Err	discrete	On/Off	No change
Temp Base Area	degrees C	On/Off	Exceeds critical threshold
Icc 12v FRU0	Amps	On	Exceeds critical threshold
Vcc 12v FRU0	Volts	On	Exceeds critical threshold
Icc 12v FRU1	Amps	On	Exceeds critical threshold
Icc 12v FRU2	Amps	On	Exceeds critical threshold

Table 4-3: AT8904M sensors (continued)

IPMI Sensor Name	Unit	Scanning Enabled Under Power State	Health LED/Sensor
Icc 3.3vSus FRU0	Amps	On/Off	Exceeds critical threshold
Vcc 3.3vSus FRU0	Volts	On/Off	Exceeds critical threshold
Icc 3.3v FRU0	Amps	On	Exceeds critical threshold
Vcc 3.3v FRU0	Volts	On	Exceeds critical threshold
Icc 2.5v FRU0	Amps	On	Exceeds critical threshold
Vcc 2.5v FRU0	Volts	On	Exceeds critical threshold
Icc 1.8v FRU0	Amps	On	Exceeds critical threshold
Vcc 1.8v FRU0	Volts	On	Exceeds critical threshold
Icc 1.25v FRU0	Amps	On	Exceeds critical threshold
Vcc 1.25v FRU0	Volts	On	Exceeds critical threshold
Icc 1.2v FRU0	Amps	On	Exceeds critical threshold
Vcc 1.2v FRU0	Volts	On	Exceeds critical threshold
-48V A FUSE	discrete	On/Off	No change
-48V B FUSE	discrete	On/Off	No change
-48V A RTN FUSE	discrete	On/Off	No change
-48V B RTN FUSE	discrete	On/Off	No change
CPU Status	discrete	On	No change
Post Code	discrete	On	No change
Power FRU1	Watts	On	No change
Power FRU2	Watts	On	No change
Firmware Upg Mng	discrete	On/Off	No change
Board Reset	discrete	On	No change
Boot Cycle Fault	discrete	On/Off	No change
Health Error	discrete	On/Off	No change
FRU1 Mp Over Icc	discrete	On/Off	No change
FRU1 Over Icc	discrete	On/Off	No change
FRU1 Sensor Err	discrete	On/Off	No change
FRU2 Mp Over Icc	discrete	On/Off	No change
FRU2 Over Icc	discrete	On/Off	No change
FRU2 Sensor Err	discrete	On/Off	No change
Mezz. Presence	discrete	On/Off	No change
FRU0 Pwr Denied	discrete	On/Off	No change
FRU1 Pwr Denied	discrete	On/Off	No change
FRU2 Pwr Denied	discrete	On/Off	No change
Handle Switch	discrete	On/Off	No change

Table 4-3: AT8904M sensors (continued)

IPMI Sensor Name	Unit	Scanning Enabled Under Power State	Health LED/Sensor
Ver change	discrete	On/Off	No change

Table 4-4: Additional AT8904M sensors (Mezzanine)

IPMI Sensor Name	Unit	Scanning Enabled Under Power State	Health LED/Sensor
Temp Mezz. Area	degrees C	On	Exceeds critical threshold
Vcc 1.25v Mezz.	Volts	On	Exceeds critical threshold
Vcc 2.5v Mezz.	Volts	On	Exceeds critical threshold
Vcc 3.3v Mezz.	Volts	On	Exceeds critical threshold
Vcc 12v Mezz.	Volts	On	Exceeds critical threshold

4.4.1.1 IPMB Link Sensor

The AT8904M provides two IPMB links to increase communication reliability to the shelf manager and other IPM devices on the IPMB. These IPMB links work together for increased throughput where both busses are actively used for communication at any time. A request might be received over IPMB Bus A, and the response is sent over IPMB Bus B. Any requests that time out are retried on the redundant IPMB bus. In the event of any link state change, the events are written to the AT8904M SEL. The IPMC monitors the bus for any link failure and isolates itself from the bus if it detects that it is causing errors on the bus. Events are sent to signal the failure of a bus or, conversely, the recovery of a bus.

4.4.1.2 FRU Hot Swap

The hot swap event message conveys the current state of the FRU, the previous state, and a cause of the state change as can be determined by the IPMC. Refer to PICMG 3.0 Specifications for further details on the hot swap state.

4.4.1.3 Fabric Presence Sensor

The FPS indicates if an optional Extension Fabric Mezzanine is present.

4.4.1.4 CPU Status

The CPU Status is set if the PPC experiences a machine check error.

4.4.1.5 POSTCODE

The IPMC has access to the POSTCODE registers in the CPLD. Refer to chapter 4.3.1.2 (Boot Steps).

4.4.1.6 Health Error

The Health Error is asserted if one of the sensors in Table 4-3: (AT8904M sensors) *and* Table 4-4: (Additional AT8904M sensors (Mezzanine)) matches the Health LED/Sensor condition.

4.4.2 Field Replaceable Unit (FRU) Information

4.4.2.1 Base Board FRU Information

This FRU information contains the IPMI defined Board and Product Information areas that hold the part number and serial number of the board and the Multirecord Information Area that contains the PICMG defined Point to Point Information records.

The Internal Use Area is preallocated to 384 bytes and is free for customer use.

This FRU information responds to FRU ID #0, which is the ID for the IPMC.

4.4.2.2 Mezzanine FRU Information

The FRU information of any optional Mezzanine Extension responds to FRU ID #3 and is manged by the IPMC. This FRU information contains the IPMI defined Board and Product Information Areas and contains the part number and serial number of the mezzanine.

4.4.3 E-Keying

E-Keying has been defined in the PICMG 3.0 Specification to prevent board damage, prevent misoperation, and verify fabric compatibility. The FRU data contains the board point-to-point connectivity record as described in Section 3.7.2.3 of the PICMG 3.0 specification.

When the board enters M3 power state, the shelf manager reads in the board point-to-point connectivity record from FRU and determines whether the board can enable the Gigabit Ethernet ports to the back plane. Set/Get Port State IPMI commands defined by the PICMG 3.0 specification are used for either granting or rejecting the E-keys.

Additional E-Keying is prodived for connectivity between the AMC carrier and the AMC bays as described the in Section 3.9 and 3.7 of the AMC.0 RC.1.1 specification. The Set/Get AMC Port State IPMI commands defined by the AMC.0 specification are used for either granting or rejecting the E-keys.

4.4.4 IPMC Firmware Code

IPMC firmware code is organized into boot code and operational code, both of which are stored in a flash module. Upon an IPMC reset, the IPMC executes the boot code and performs the following:

1. Self test to verify the status of its hardware and memory.
2. Calculates a checksum of the operational code.
3. Communicates with the Firmware Upgrade Manager (FUM) in order to inform the IPMC watchdog that the current IPMC firmware is suitable for execution.

Upon successful verification of the operational code checksum, the firmware will jump to the operational code.

4.4.5 LEDs

For LED positions on the front plate refer to Chapter 3, section 3.1.11., Display Elements.

4.4.5.1 Hot Swap LED (Blue LED)

The AT8904M Hub Board supports a blue Hot Swap LED mounted on the front panel. This LED indicates when it is safe to remove the Hub from the chassis. The on-board IPMC drives this LED to indicate the hot swap state. The following states are possible:

Table 4-5: LED state

LED state	Description
OFF	Board is in M4 state, normal state when board is in operation.
ON	Ready for hot swap
Short blink	Board is in M5 state. Deactivation in progress
Long blink	Activation in progress.

4.4.5.2 Out-Of-Service (OOS) LED (ATCA LED1)

The AT8904M supports a red Out of Service LED mounted on the front panel. The position of this LED is near the top handle besides the blue Hot Swap led. The on-board FWUM or the IPMC can drive this LED to indicate the service state of the IPMC. The OEM application can also drive this LED using the PICMG LED control APIs. The following states are possible:

Table 4-6: OOS LED state

LED state	Description
ON	Out of service condition, the IPMC is hold in reset
OFF	Normal/Idle board is in service, unless blue led is on
Blink (50/50)	The FUM is programming the IPMC due to a firmware update or a rollback
Short blink	Power denied condition detected: Payload has been left in M3 state for more than 30 secs or SetPowerLevel ‘0‘ has been received while in M2 or M3 state

Other application defined LED usage may be implemented.

The AT8904M AMC.0 carrier also implements the OOS LED “Short blink” mode for its AdvancedMC mates on detection of “power denied” conditions.

LED state	Description
Short blink	Power denied condition detected: AMC current draw requirements exceed carrier power budget or SetPowerLevel ‘0‘ has been received while in M2 or M3 state

As per AMC.0, if the AMC current draw requirements exceed AMC.0 carrier power budget, the AT8904M will keep the AMC in M1 state with the blue Hot Swap LED in the ON state.

4.4.5.3 Health LED (ATCA LED2)

Green LED

Table 4-7: Health LED state

LED state	Description
ON	None of the health sensors is asserted
Blinking	At least one health sensor is asserted

4.4.5.4 Customer Definable LED (ATCA LED 3)

This is an amber LED which can be used by a customer application. This LED can be controlled by PICMG 3.0 defined LED commands.

4.4.6 Hot Swap Process

The AT8904M Hub Board has the ability to be hot-swapped in and out of a chassis. The on-board IPMC manages the power-up and power-down transitions.

In addition to captive retaining screws, the Hub Board has two ejector mechanisms to provide a positive cam action; this ensures the blade is properly seated. The bottom ejector handle also has a switch that is connected to the IPMC to determine if the board has been properly inserted.

When the lower ejector handle is disengaged from the faceplate, the hot swap switch will assert a signal to the IPMC, and the IPMC will move from the M4 state to the M5 state. At the M5 state, the IPMC will ask the ShMC for permission to move to the M6 state. The Hot Swap LED will indicate this state with a short blink. Once permission is received from the ShMC or higher-level software, the board will move to the M6 state.

The ShMC or higher level software can reject the request to move to the M6 state. If this occurs, the Hot Swap LED returns to a solid off condition, indicating that the Hub Board has returned to M4 state.

If the Hub Board reaches the M6 state, either through an extraction request through the lower ejector handle or a direct command from higher-level software. The Hot Swap LED continues to flash during this preparation time, just like it does in M5 state. When payload power is successfully turned off, the Hot Swap LED remains lit, indicating it is safe to remove the Hub board from the chassis.

4.5 Firmware Administration

A running AT8904M system requires – after the bootloader has passed control to the kernel – the kernel itself, the root file system (initrd), the FASTPATH switching application and a configuration file for base and fabric switch. These software components, together with the IPMC image, make up the AT8904M firmware.

The flash holding the software is divided into twelve partitions. There are partitions to store two bootloader, three kernel and three initrd images. Two partitions are reserved for the bootloader environments, one partition is used to hold up to nine images of the switching application (depending on the size of the images) and one partition is used to hold up to 99 configuration setting files. The partition scheme of the flash is shown below:

Table 4-8: FLASH Partition Scheme (64MB)

Partition	Size	MTD
U-Boot Loader primary image (write protected)	256KB	11
U-Boot Loader secondary image, updatable (optional)	256KB	10
U-Boot primary environment	256KB	9
U-Boot secondary environment	256KB	8
Kernel factory image (KERNEL F)	2MB	7
Kernel primary image (KERNEL A)	2MB	6
Kernel secondary image (KERNEL B)	2MB	5
Initrd factory default (INITRD F)	7MB	4
Initrd primary image (INITRD A)	7MB	3
Initrd secondary image (INITRD B)	7MB	2
JFFS Configuration File Partition CONFIGURATION text file F CONFIGURATION text file 01 CONFIGURATION text file ... CONFIGURATION text file 99 CONFIGSLOTS file containing multiple kernel/initrd/application/configuration combination for selection through CLI	4MB	1
JFFS Application Archive Partition APPLICATION tgz archive F APPLICATION tgz archive 01 APPLICATION tgz archive ... APPLICATION tgz archive N	32MB	0

The kernel and initrd partitions labelled with ‘F’ contain factory default images which are known to work properly on the AT8904M. The factory default images cannot be updated using the CLI commands described below.

The firmware update procedure is designed to provide a failsafe capability to update IPMC, kernel, initrd, application and configuration settings separately. Each combination of these components can be used as a startup configuration, though they must be compatible to each other. Please always follow Kontron documentation for all your upgrades. Software versions provided with an official release are known to work together.

In the following, the CLI commands to setup, change and activate startup configuration and the CLI commands necessary to perform firmware upgrades are described. The CLI commands described below are executed in the privileged mode of the CLI hierarchy, which is entered by executing the 'enable' command. Please refer to the "*AT8901/02/04M CLI Reference Manual*" for more information regarding the CLI commands and the way to use them.

4.5.1 Startup Configurations

A startup configuration is a combination of a kernel, initrd, application image and configuration files for base and fabric switch. The IPMC image is not part of the configuration and is updated separately. Several configurations (up to 99) can be defined but only one is active at a time. To display the currently available startup configurations, the CLI command 'show' is used.

```
(Base Fabric) #show startupconfig startup
ACT NR KERNEL       SYSTEM       APPLICATION   BASE-CONFIG     EXT-CONFIG
--- -- ------------ ------------ ------------- --------------- ---------------
     F F BETA 6.09  F BETA 6.09  F  BETA 6.09  F  factory      F  factory
*A  01 A BETA 6.09  A BETA 6.09  02 BETA 6.09  01 standard     01 standard

(Base Fabric) #
```

In this example, two startup configurations are available. Startup configuration 01 is the currently active configuration which is indicated by the '*' in the first column. This configuration consists of:

- Kernel BETA 6.09 which is located in kernel partition A
- Initrd BETA 6.09 which is located in initrd partition A.
- Application BETA 6.09 which is stored in slot 02 of the application partition.
- Base and fabric configuration files which are stored in slot 01 of the configuration partition.

The user can define other startup configurations and combine images and configuration files as needed. To set up a new startup configuration, it is necessary to change into the CLI's configuration mode using the 'configure' command. In this mode, the 'startupslot' command is used as shown in the following example:

```
(Base Fabric) (Config)#startupslot 3 config 1 application 2 initrd F kernel F

Successfully set startup slot 3
You may mark it active now and reboot to use the new configuration.

(Base Fabric) (Config)#exit

(Base Fabric) #
```

```
(Base Fabric) #show startupconfig startup
ACT NR KERNEL       SYSTEM       APPLICATION   BASE-CONFIG     EXT-CONFIG
--- -- ------------ ------------ ------------- --------------- ---------------
     F F BETA 6.09  F BETA 6.09  F  BETA 6.09  F  factory      F  factory
*A  01 A BETA 6.09  A BETA 6.09  02 BETA 6.09  01 standard     01 standard
    03 F BETA 6.09  F BETA 6.09  02 BETA 6.09  01 standard     01 standard
```

A new startup configuration has been added to the list combining the software images given in the previous command.



Warning!

It is not recommended to combine images from different releases.

The startup configuration created before can be deleted by entering exactly the same command string preceeded by ‘no’:

```
(Base Fabric) (Config)#no startupslot 3 config 1 application 2 initrd F kernel F
```

The ‘show’ command can also be used to display available versions of kernel, initrd, applications and configurations or all of them. The syntax is:

```
show startupconfig startup|kernel|initrd|application|config|all
```

The configuration mode is also used to activate one of the available startup configurations. The syntax is:

```
startupslot 3 activate [once]
```

This command would activate the startup configuration 3 upon next system reset. The optional parameter ‘once’ would start configuration 3 only once after the next system reset and start the previously active configuration 1 on following resets. This is used to implement the failsafe upgrade procedure described below.

4.5.2 Updating Firmware

The firmware - except bootloader and IPMC image - is updated using the CLI. To get a reliable and failsafe update procedure, the following precautions must be fulfilled:

- Three independent partitions each for kernel and root file system where one holds the factory default system, one holds system A kernel and root file system and one holds system B kernel and root file system. The active system is either system A or system B, the factory default serves as a backup in case an upgrade of either system A or B fails. See the flash partition scheme shown above for more detail.

- One Time Boot capability: After having updated the inactive kernel and root file system, the new system has to be started by rebooting the board. In the case that the update has installed an inoperable system which would cause the board to hang when booting, the next board reset must restart the previous known good version of kernel and root file system. This is achieved by programming the bootloader environment appropriately.
- Redundant bootloader environment sectors: When the system is updated, the bootloader environment must be changed to be able to start the updated version. The bootloader environment sector is stored twice in flash, one active version and one backup version in case the active version is deleted during update due to power loss or similar errors. In this case, the redundant environment would cause the bootloader to start the previous known good version of kernel and root file system.

A software update of the Hub Board is done by performing the following steps:

1. Download kernel, initrd and application images into the appropriate slots of the flash memory. Ensure that the currently active images are not overwritten.
2. Select a configuration for base and fabric switch for the new software release. This can be done by choosing the factory default or by storing the running system configuration into flash.
3. Create a startup configuration by combining the slots with the update images and the configuration slots for base and fabric switch.
4. Activate the selected startup configuration for One Time Boot.
5. Restart the board.
6. Activate the new startup configuration permanently

A software release for the AT8904M consists of three software packages for kernel, initrd and application software. The packages are tar archives containing an image of the software and a MD5 checksum file for consistency check. The name of the package file is arbitrary but the file names in the archive must not be altered.

When performing a firmware update, the software packages are loaded from a remote TFTP server in the first step. This is done by means of the frontpanel FE port of the Hub board. To load a software package via TFTP into a specified slot, the CLI command ‘download’ is used:

```
(Base Fabric) #download kernel tftp://192.168.50.5/kernel.pkg B

Downloading image, this may take a while...
Successfully transferred kernel image tftp://192.168.50.5/kernel.pkg to slot 2
You may mark it active now and reboot to use the new kernel image.

(Base Fabric) #
```

This downloads the specified kernel package file via TFTP and writes the kernel image into the kernel partition of the specified slot (B). The MD5 checksum of the kernel image is checked before writing it into flash. The same procedure can be done with initrd and application packages. It is important not to overwrite the slots containing the currently active software, otherwise the One Time Boot mechanism does not make sense.

After the software images have been downloaded into flash, the configuration slots for base and fabric switch must be selected. In case that no appropriate configuration for base and/or fabric switch are available, the factory default configuration for base and fabric switch should be used for the startup configuration of the new software release. Alternatively, the running configuration settings of base and fabric switch can be stored on flash using the following CLI command:

```
(Base Fabric) #copy system:running-config nvram:startup-config slot 3

This operation may take a few minutes.
Management interfaces will not be available during this time.

Are you sure you want to save? (y/n) y

Configuration Saved!

(Base Fabric) #
```

Instead of storing the configuration for ‘both’ base and fabric switch, ‘base-only’ or ‘ext-only’ might be given as parameters.

Finally, a startup configuration containing the slots of the new software release and the configuration slots must be selected or a new startup configuration must be created as described above. After this step has been completed, the startup configuration is activated only for the next boot and the board is rebooted. This is done with the ‘startupslot’ CLI command in the configure mode:

```
(Base Fabric) (Config)#startupslot 3 activate once
```

This command enables the startup configuration 3 only for the next system restart. In the case that the board hangs due to a corrupted software image, this will be detected and the board is automatically rebooted with the previous known good startup configuration. This way, a failsafe upgrade of the AT8904M software is possible.

To restart the board with the new startup configuration, the CLI command ‘reload’ is used:

```
(Base Fabric) (Config)#reload
```

If the new startup configuration is considered functional after the reboot, it must be activated permanently, or else the one that is still active will be used again:

```
(Base Fabric) (Config)#startupslot 3 activate
```

4.5.3 Updating IPMI

Updating the IPMI firmware is different from updating the other software parts as updating is done directly when invoking the download command. In the case that the update procedure fails or the update image is corrupted, the IPMC will be able to restart all the same by means of its rollback functionality. The IPMI software package file is stored in the result/ppc405/firmware path of the release directory tree. To update the IPMI firmware, the CLI command ‘download’ is used:

```
(Base Fabric) #download ipmifw tftp://192.168.50.5/ipmi.pkg

Flashing a new IPMI firmware will disable the IPMI Controller for some minutes.
Are you sure to update the IPMI firmware? (y/n)y
...
(Base Fabric) #
```

Appendix A

Getting Help

A. Getting Help

If, at any time, you encounter difficulties with your application or with any of our products, or if you simply need guidance on system setups and capabilities, contact our Technical Support at:

North America	EMEA
Tel.: (450) 437-5682	Tel.: +49 (0) 8341 803 333
Fax: (450) 437-8053	Fax: +49 (0) 8341 803 339

If you have any questions about Kontron, our products, or services, visit our Web site at: www.kontron.com

You also can contact us by E-mail at:

North America: support@ca.kontron.com

EMEA: support-kom@kontron.com

Or at the following address:

North America	EMEA
Kontron Canada, Inc.	Kontron Modular Computers GmbH
616 Curé Boivin	Sudetenstrasse 7
Boisbriand, Québec	87600 Kaufbeuren
J7G 2A7 Canada	Germany

RETURNING DEFECTIVE MERCHANDISE

Before returning any merchandise please do one of the following:

- **Call**

1. Call our Technical Support department in North America at (450) 437-5682 or in EMEA at +49 (0) 8341 803 333. Make sure you have the following on hand: our Invoice #, your Purchase Order # and the Serial Number of the defective unit.
2. Provide the serial number found on the back of the unit and explain the nature of your problem to a service technician.
3. The technician will instruct you on the return procedure if the problem cannot be solved over the telephone.
4. Make sure you receive an RMA # from our Technical Support before returning any merchandise.

- **Fax**

1. Make a copy of the request form on the following page.
2. Fill it out.
3. Fax it to us at: North America (450) 437-0304, EMEA +49 (0) 8341 803 339

- **E-mail**

1. Send us an e-mail at: RMA@ca.kontron.com in North America or at: orderprocessing@kontron-modular.com in EMEA. In the e-mail, you must include your name, your company name, your address, your city, your postal/zip code, your phone number, and your e-mail. You must also include the serial number of the defective product and a description of the problem.

WHEN RETURNING A UNIT

- In the box, you must include the name and telephone number of a person, in case further explanations are required. **Where applicable, always include all duty papers and invoice(s) associated with the item(s) in question.**
- Ensure that the unit is properly packed. Pack it in a rigid cardboard box.
- Clearly write or mark the RMA number on the outside of the package you are returning.
- Ship prepaid. We take care of insuring incoming units.

North America	EMEA
Kontron Canada, Inc.	Kontron Modular Computers GmbH
616 Curé Boivin	Sudetenstrasse 7
Boisbriand, Québec	87600 Kaufbeuren
J7G 2A7 Canada	Germany



Return to Manufacturer Authorization Request

Contact Name:	_____		
Company Name:	_____		
Street Address:	_____		
City:	_____	Province/State:	_____
Country:	_____	Postal/Zip Code:	_____
Phone Number:	_____	Extension:	_____
Fax Number:	_____	E-Mail:	_____

Serial Number	Failure or Problem Description	P.O. # (if not under warranty)

Fax this form to Kontron's Technical Support department

in North America at (450) 437-0304 or

in EMEA at +49 (0)8341 803 339