» Kontron User's Guide «



COMe-cXLi2 Computer-on-Module (COM)

Document version 1.7

» Table of Contents «

1 User Information 1

1.1 About This Document 1

1.2 Copyright Notice 1

1.3 Trademarks 1

1.4 Standards 1

1.5 Warranty 2

1.6 Technical Support 2

2 Introduction 3

2.1 The COMe-cXLi2 COM 3

2.2 Naming Clarifications 3

2.3 Understanding the COM Functionality 4

2.4 COM Express® Documentation 4

2.5 COM Express® COM Benefits 5

3 Specifications 7

3.1 Functional Specification 7

3.2 Functional Block Diagram 10

3.3 Mechanical Specifications 10

3.4 Electrical Specifications 11

3.4.1 Supply Voltage 11

3.4.2 Supply Current (Windows XP SP3) 12

3.5 Environmental Specifications 12

3.6 MTBF 13

4 COM Connectors 14

4.1 Pin-Outs 15

4.1.1 Connector J1 – CPLD Debug 32

4.1.2 Connector J2 – SO DIMM DDR2 Soldered 32

4.1.3 Connector J3 - US15WPT JTAG Connector 32

4.1.4 Connector J4 - SDIO/MMC Socket 33
4.1.5 Connector J5 - FAN 33
4.2 Signal Descriptions 33
4.2.1 PCI Express Interface 33
4.2.2 USB Interface 33
4.2.3 SATA Interface 35
4.2.4 Audio Interface 35
4.2.5 Serial IRQ 36
4.2.6 Graphics Interface 36
4.2.7 Ethernet Interface 37
4.2.8 LPC Bus Interface 38
4.2.9 Power Control Interface 40
4.2.10 Miscellaneous Circuits 42

5 Special Features 44

5.1 Hyper-Threading 44
5.2 Enhanced Speedstep Technology 44
5.3 SDCard Interface (SDIO) 44
5.4 Watchdog 46
5.5 General Purpose Input and Output (GPIO) 46
5.6 Fast I^2C 47
5.7 ACPI Suspend Modes and Resume Events 48

6 Design Consideration 49

6.1 Thermal Management 49
6.2 Heat-Spreader Dimensions 49
6.3 Onboard Fan Connector 49
6.3.1 BIOS Settings for Fan Control 51
6.3.2 Fan Connector Electrical Characteristics 52

7 System Resources 53

7.1 Interrupt Request (IRQ) Lines 53
7.2 Memory Area 55
7.3 I/O Address Map 55
7.4 Peripheral Component Interconnect (PCI) Devices 57

7.5 System Management Bus (SMBus) 58
7.6 K-Station / JIDA32 Resources 59

8 BIOS Operation 60

8.1 The COMe-cXLi2 COM has AMI® BIOS installed on the onboard8-Mbit firmware hub. Determining the BIOS Version 60
8.2 Setup Guide 60
8.2.1 Start AMI® BIOS Setup Utility 60
8.3 BIOS Setup 63
8.3.1 Main Menu 63
8.3.2 Advanced Settings Menu 64
8.3.3 Advanced PCI/PnP Settings 82
8.3.4 Boot Settings 83
8.3.5 Security Settings 85
8.3.6 GPIO Configuration 86
8.3.7 MPS Configuration 87
8.3.8 USB Mass Storage Device Configuration 88
8.3.9 Boot Device Priority 89
8.3.10 Advanced Chipset Configuration 90
8.3.11 North Bridge Chipset Configuration 91
8.3.12 JILI Display Configuration 92
8.3.13 South Bridge Chipset Configuration 93
8.3.14 Exit Options 94
8.4 Appendix A: JIDA Standard 94
8.5 JIDA Information 95

9 Appendix B: Architecture Information 96

9.1 Buses 96
9.1.1 ISA, Standard PS/2 – Connectors 96
9.1.2 PCI/104 96
9.2 General PC Architecture 96
9.3 Ports 97
9.3.1 RS-232 Serial 97
9.3.2 Serial ATA 97
9.3.3 USB 97
9.4 Programming 98

10 Appendix C: Document Revision History 99

1 User Information

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Kontron is certified to ISO 9000 standards.

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This Kontron product is warranted against defects in material and workmanship for the warranty period from the date of shipment. During the warranty period, Kontron will at its discretion decide to repair or replace defective products.

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Please consult our website at http://www.kontron.com/support for the latest product documentation, utilities, drivers and support contacts. Consult our customer section for the latest BIOS downloads, Product Change Notifications and additional tools and software. You can also always contact your board supplier for technical support.

2 Introduction

2.1 The COMe-cXLi2 COM

The Kontron COMe-cXLi2 Computer-on-Module (COM) extends the COM Express® specification to include a small module form factor (95 x 95 mm) with the commonly used COM Express® Type 2 connector for use in extreme environmental conditions. Each component operates within the E2 industrial temperature range of -40 to +85°C and meets the tolerances required for high reliability with respect to shock and vibration resistance. This design enables the development of energy-saving devices based on the Intel® Atom™ processor Z5xx T Series and the Intel® System Controller Hub with the secure development path of an established, future-proof industry standard.

The Kontron COMe-cXLi2 module offers LVDS as well as more sophisticated graphics support with SDVO. Using the PCI Express* pin-out, SDVO delivers additional video signals for DVI monitor outputs, SDTV and HDTV television outputs, and TV tuner inputs to greatly simplify system graphics design. These special features make this 95 x 95 mm Computer-on-Module ideal for small, mobile, extremely energy-efficient multimedia devices as well as mobile test and measurement applications such as those used in government/military and transportation applications. Other standard features of the COMe-cXLi2 COMs include: Gigabit Ethernet, Serial ATA, single-channel LVDS, and USB 2.0 support.

All modules in the Kontron COM Express® compact family are compatible with the COM Express® standard (Pin-out Type 2) and thus ensure easy interchangeability as well as design scalability and future migration paths. The COMe-cXLi2 COM is a complete PC with standard interfaces such as USB and additional options like sound capabilities, a flat panel interface, and Ethernet.

2.2 Naming Clarifications

COM Express® defines a Computer-On-Module, or COM, with all the components necessary for a bootable host computer, packaged as a super-component. The interfaces provide a smooth transition path from legacy parallel interfaces to Low Voltage Differential Signaling (LVDS) interfaces including the PCI bus, parallel ATA (PATA), PCI Express*, and Serial ATA (SATA).

» Kontron COM Express® basic form factor modules are 125mm x 95mm and follow the Type 2 and Type 6 pin-out definitions.

» Kontron COM Express® compact form factor modules are 95mm x 95mm and follow the Type 2 and 6 pin-out definitions.

» Kontron COM Express® mini form factor modules are 55mm x 84mm and follow the Type 1 and 10 pin-out definitions.

2.3 Understanding the COM Functionality

All Kontron COM Express® basic and compact form factor modules contain two connectors, each with two rows. The primary connector rows are Row A and Row B. The secondary connector rows are Row C and Row D. The primary connector (Row A and Row B) features the following legacy-free functionality:

» Gigabit Ethernet LAN

» Serial ATA (SATA)

» 8xUSB 2.0

» LVDS18/24/26/48-bit

» Intel® High Definition Audio (HAD)

» LPC (Low Pin Count) Bus

» PCI Express*

» SDIO

» I^2C

The secondary connector (Row C and Row D) supports the following buses and I/O:

» PCI Express (available for versions where the PCIe-to-PCI bridge is not implemented)

» PCI

» IDE (optional)

» SDV0

NOTE: For a full description of the COM Express Type 2 pin-out, refer to the PICMG website or documentation.

2.4 COM Express® Documentation

This product manual serves as one of three principal references for this COM Express® module design. It documents the specifications and features of the COMe-cXLi2 COM. The other two references, which are available from your Kontron support representative or from PICMG®, include:

» The COM Express® Specification, which defines the COM Express® module form factor, pin-out, and signals. This document can be obtained by filling out the order form on the PIGMG website.

» The PICMG COM Express® Design Guide, which serves as a general guide for baseboard design, with a focus on maximum flexibility to accommodate a wide range of COM Express® modules. This guide is on the PICMG website at http://www.picmg.com .

2.5 COM Express® COM Benefits

Compact form factor COM Express modules are very compact (95 x 95 mm), highly integrated computers. All Kontron COM Express® compact modules feature a standardized form factor and a standardized connector layout for a specified set of signals. Each Kontron COM Express® compact module is based on the Connector Type 2 pin-out of the COM Express® specification. This standardization allows designers to create a single-system baseboard that can accept present and future Kontron COM Express® compact module modules.

Kontron COM Express® compact module modules include common personal computer (PC) peripheral functions such as:

» Graphics

» USB ports

» Ethernet

» Audio

» IDE, PATA, and SATA

Baseboard designers can optimize exactly how each of these functions is implemented physically for the intended application. Designers can place connectors precisely where they are needed on a baseboard that is designed for an optimal fit in the system packaging.

A peripheral PCI bus can be implemented directly on the baseboard rather than on mechanically unwieldy expansion cards. The ability to build a system on a single baseboard using the computer as one plug-in super-component simplifies packaging, eliminates cabling, and significantly reduces system-level total cost of ownership.

A single baseboard design can use a range of COM Express modules. This flexibility enables product differentiation at various price/performance points, and the design of future-proof systems with a built-in upgrade path. The modularity of a COM Express solution also ensures against obsolescence as computer technology evolves. A properly designed COM Express baseboard can work with several successive generations of COM Express modules.

A COM Express baseboard design has many of the advantages of a custom, computer-board design, but delivers better obsolescence protection, greatly reduced engineering effort, and faster time to market.

3 Specifications

3.1 Functional Specification

Processor: Intel® Atom™ Z5xx Series

» CPU:	45nm Z520-XL 1.33 GHz/533 MHz (extended temperature version)
» Cores:	1 (with HTT)
» Bus Speed:	533 MHz
» Bus/Core Ratio:	11 / 12
» Cache:	L1 cache 24KB data/32 KB instruction L2 cache 512 KB, 8-way
» Features:	Hyper-Threading Technology (HTT) Intel® Virtualization Technology Execute Disable Bit Enhanced Intel® Speedstep Technology Core Sleep States: C0, C1E, C2E, C3, C4E, Intel Deep Power Down State C6
» Instruction Set:	32-bit
» Package:	22mm x 22mm
» Thermal Spec:	40°C to +85°C

NOTE: Intel Deep Power Down State C6 may not be available in the first early field test (EFT) samples.

Chipset: Intel® System Controller Hub US15WPT

» Speed:	533 MHz FSB
» Memory:	On-board DDR2 industrial temperature range (8x1GB – 8x2GB)
» USB:	8 x USB 2.0 with one USB client supported
» Audio:	Intel® High Definition Audio (24 bit / 96 kHz)
» Video:	Single channel 24-bit LVDs, single SDVD channel, no VGA support
» PCI Express:	1x PCIe x 1 lane In standard versions of the COMe-cXLi2, one PCIe lane is used by GbE, and the second is used by the PCIe-to-PCI bridge. When PCIe-to-PCI Bridge is removed, only 1x PCIe is available as the other is still used by GbE. Because of the routing decisions for the GbE, only one PCIe lane is ever available for use even if the GbE is depopulated.

» TDP: 2.3W

» Package: 37.5mm x 37.5mm

Integrated Graphics: Intel® Graphics Media Accelerator 500(Intel® GMA 500)

» Graphics Memory: Up to 352 MBytes with Intel® Embedded Graphics Driver (IEGD), up to 256 MBytes with GMA

» Features: HDTV/HD capable

Video decode acceleration supporting MPEG 2/4/H.260

DirectX®9.0c

OpenGL 2.0

Display Interfaces

» CRT: VGA is not supported from the US15WPT System Controller Hub

» Flat Panel: Single Channel LVDS 18/24bit (JUMPtec Intelligent LVDS interface – JILI), resolution up to 1366 x 768 (WXGA), no dithering

» Digital Display: SDVO, shares pins with PEG interface on COM Express connector rows C-D with resolution up to FullHD 1920x1080.

Storage

» SATA: 1x Serial ATA (SATA) supporting up to 1.5 Gbit/sec transfer rate (PATA-to-SATA bridge)

» SATA Features: Boot, NCQ, Staggered Spinup, Port Multiplier

» PATA 1x Parallel ATA (PATA)

Onboard Devices:

» Ethernet: Intel® 82574 10/100/1000 GbE MAC (industrial temperature version), Intel® 82574 PHY (Max TDP 0.727W) uses one PCIe lane

» Ethernet Features: WakeOnLAN, PXE Lanboot, Time Sync Protocol Indicator, Jumbo Frames

» TPM: Infineon™ SLB9635TT1 Trusted Platform Module 1.2, onboard

» Watchdog: Kontron PIC microcontroller (interfaces to chipset over a watchdog-specific I^2C interface)

» PCIe Switch: 0, or 1 PCIe links
See details in section 4.2.1

» Power Management: L0-L3, Device Power Management D0-D3hot)

Additional Interfaces:

» LPC: Yes, to COM Express A-B connector

» SMBus: Yes

» I^2C: fast I^2C (from US15WPT system controller hub)

» GPIO: 8 GPIO, 4 GPI and 4 GPO

» SDIO: 1x onboard microSD/MMC card socket (US15WPT SDIO port #0)
1x SDIO port shared with GPIO signals (US15WPT SDIO port #1)
SD Card Specification 1.1
SDIO boot supported
Power Management & Misc

» JIDA: Yes, JIDA EEPROM
JIDA BIOS support
JILI BIOS support
JIDA16 and JIDA32 BIOS support
AMI Core 8 BIOS

» K-Station: Yes

» Bootlogo: Yes

» MARS: Yes, Charger & Manager Support

» HWM: Temperature Monitoring for CPU and Board Temperature (onboard W83L786 HWM)
HWM for external Winbond ADT7476ARQZ

» Passive Cooling: Passive and Critical Trip Point

» ACPI: ACPI 1.0 / 2.0 / 3.0

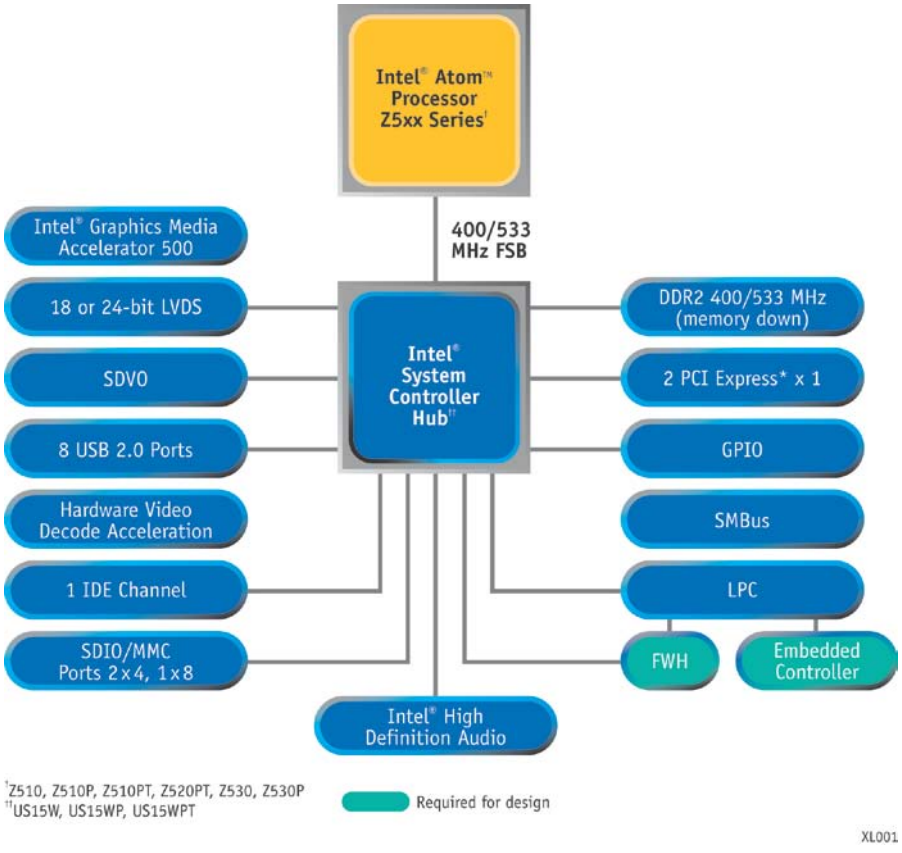
» S-States: S0, S3, S4, S5

» Input Voltage: Single supply support with wide range input
Allows 5V only design (such as ETX) or 12V only design (COM Express)

3.2 Functional Block Diagram

Figure 1 is t he COMe-cXLi2 COM block diagram

Figure 1: COMe-cXLi2 COM Block Diagram



As noted previously, the COMe-cXLi2 has only up to 1 PCIe lane abailable when the PCIe to PCI switch is not in use and the second lane is always routed for GigE LAN.

3.3 Mechanical Specifications

Module Dimensions

» 95 mm x 95 mm ±0.2 mm (3.47 in. x 3.47 in)

Height on Top

» Approximately 3.5 mm maximum (without the PCB)

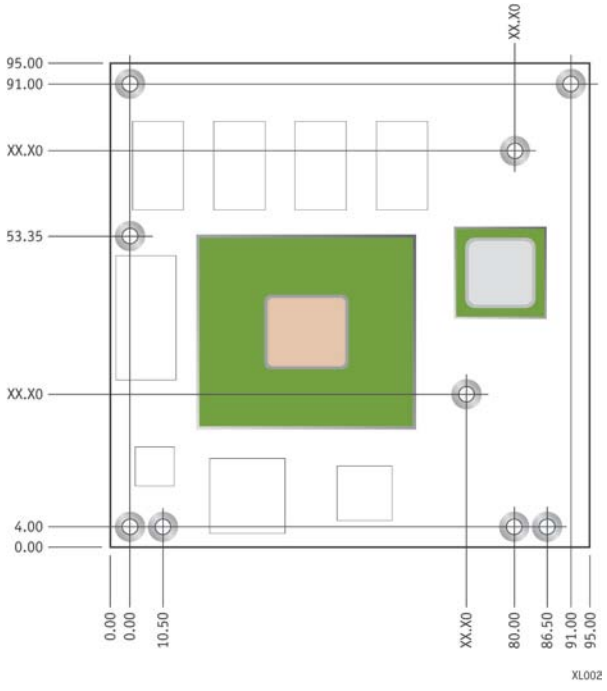
» Height varies depending on whether the optional cooling solution (either a passive heatsink or a heat spreader plate) is installed

Height on Bottom

» Approximately 4.06 mm maximum (without the PCB)

Figure 2 is the COMe-cXLi2 COM mechanical drawing

Figure 2: COMe-cXLi2 COM Mechanical Drawing



All dimensions are shown in millimeters. The COM Express® specification says that these holes should be ± 0.25mm [±0.010"], unless otherwise noted. The tolerances for placement of the COM Express connector with respect to the peg holes (dimensions [16.50, 6.00]) should be ± 0.10mm [±0.004"]. The 220-pin connector is mounted on the back of the PCB and is seen "through" the board in this view. The 4 mounting holes shown in the drawing use 6mm diameter pads and 2.7mm plated holes for use with 2.5mm hardware. The pads are tied to the PCB ground plane. Gray circles represent the mechanical mounting holes. Black circles represent the mounting holes required by the PICMG COM Express® standard.

3.4 Electrical Specifications

3.4.1Supply Voltage

» 5 V to 18 V DC in single supply mode (AT)

Power Supply Risetime

» The input voltages rise from ≤10% of nominal to within the regulation ranges within 0.1ms to 20ms.

Supply Voltage Ripple

» Maximum 100 mV peak to peak 0-20MHz

3.4.2Supply Current (Windows XP SP3)

The testing performed to capture the supply current data used tested modules mounted on a Kontron evaluation board with a mouse and keyboard connected. The power consumption tests were executed in Windows XP (with SP3) using a tool to stress the CPU at 100 % load. The power measurement values were captured after 15 minutes of full load or a stable CPU core temperature of 90°C. To ensure a stable die temperature, a corresponding heatsink was used to hold the temperature under the critical trip point. All boards were equipped with a 1024-MB DDR SDRAM. The modules were tested using the maximum CPU frequency. For more detailed information, refer to the "Power Consumption" diagrams on the EMD Customer section of the Kontron website.

Table 1: Atom Z520 1.3GHz - 36006-1000-13-1

	Power Consumption in [W]
Windows Desktop (idle)	4.2
TAT at maximum power configuration	6.3
S3 with Wake-on-LAN disabled	0.037
S5 with Wake-on-LAN disabled	0.19

Note: It is difficult to test for all possible applications on the market. There may be an application that draws more power from the CPU than the values measured in the table above. Take this into consideration if you are at the limit of the thermal specification, in which case you should consider improving your thermal solution.

3.5 Environmental Specifications

Temperature

Operating: (with Kontron heat-spreader plate assembly):

» Ambient temperature: -40 to +85°C

» Maximum heat spreader-plate temperature: -40 to +85°C(*)

» Non-operating: -40 to +85°C

Note: *The maximum operating temperature with the heat spreader plate installed is the maximum measurable temperature on any spot on the heat spreader surface. You must maintain the temperature according to the specification above.

Operating (without Kontron heat-spreader plate assembly):

» Maximum operating temperature: -40°C to +85°C

» Non operating: -40°C to +85°C

Note: **The maximum operating temperature is the maximum measurable temperature on any spot on the module surface. You must maintain the temperature according to the specification above.

Humidity

» Operating: 10% to 90% (non condensing)

» Non operating: 5% to 95% (non condensing)

3.6 MTBF

144628 hours

4 COM Connectors

The pin-outs for Kontron COM Express® compact module interface connectors X1A and X1B are documented for convenient reference. See the PICMG COM Express® Specification on the PICMG website and COM Express® Design Guide on the Kontron website for detailed, design-level information.

Figure 3: Connector Locations

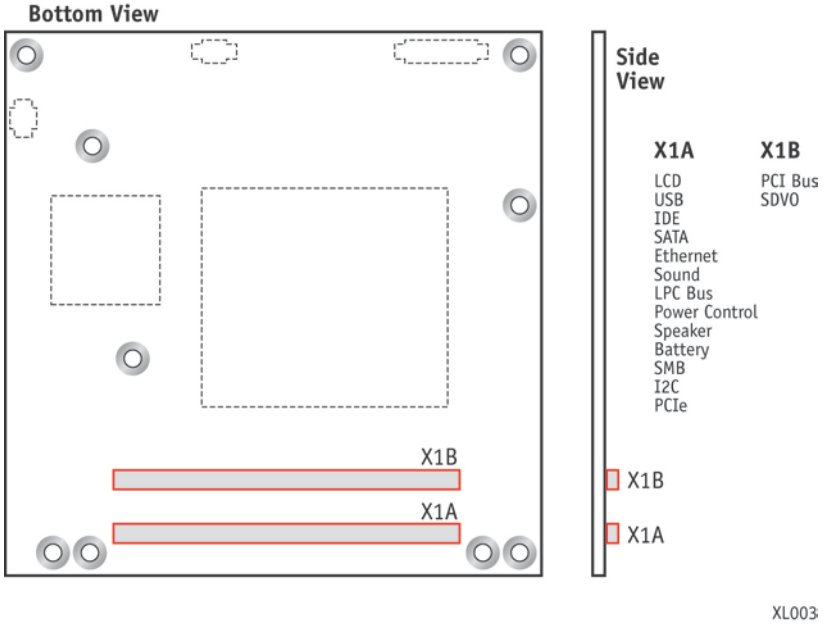


Table2: General Signal Description

Type	Description
I/O-3,3	Bi-directional 3,3 V IO-Signal
I/O-5T	Bi-dir. 3,3V I/O (5V Tolerance)
I/O-5	Bi-directional 5V I/O-Signal
I-3,3	3.3V Input
I/OD	Bi-directional Input/Output Open Drain
I-5T	3.3V Input (5V Tolerance)
OA	Output Analog
OD	Output Open Drain
O-1,8	1.8V Output
O-3,3	3.3V Output
O-5	5V Output
DP-I/O	Differential Pair Input/Output
DP-I	Differential Pair Input
DP-O	Differential Pair Output
PU	Pull-Up Resistor
PD	Pull-Down Resistor

Type	Description
PWR	Power Connection
nc	Not connected, Signal not available

Note: To protect external power lines of peripheral devices, make sure that the wires have the right diameter to withstand the maximum available current and the enclosure of the peripheral device fulfils the fire-protection requirements in IEC/EN60950

4.1 Pin-Outs

Table 3: Connector X1A - Row A

Pin	Signal	Description	Type	Termination	Comment
A1	GND_1	Power Ground	PWR	-	-
A2	GBE0_MDI3-	Ethernet Receive Data-	DP-I	Intel 82574IT	-
A3	GBE0_MDI3+	Ethernet Receive Data+	DP-I	Intel 82574IT	-
A4	GBE0_LINK100#	Ethernet Speed LED 100Mbps	O-3.3	Intel 82574IT	-
A5	GBE0_LINK1000#	Ethernet Speed LED 1000Mbps	O-3.3	Intel 82574IT	-
A6	GBE0_MDI2-	Ethernet Receive Data-	DP-I	Intel 82574IT	-
A7	GBE0_MDI2+	Ethernet Receive Data+	DP-I	Intel 82574IT	-
A8	GBE0_LINK#	LAN Link LED	OD	Intel 82574IT	-
A9	GBE0_MDI1-	Ethernet Receive Data-	DP-I	Intel 82574IT	-
A10	GBE0_MDI1+	Ethernet Receive Data+	DP-I	Intel 82574IT	-
A11	GND_2	Power Ground	PWR	-	-
A12	GBE0_MDI0-	Ethernet Transmit Data-	DP-O	Intel 82574IT	-
A13	GBE0_MDI0+	Ethernet Transmit Data+	DP-O	Intel 82574IT	-
A14	GBE0_CTREF	LAN Reference Voltage	O-1.8	is on a power rail controlled	-
A15	SUS_S3#	Indicates Suspend to RAM state	O-3.3	CPLD I/O	CPLD I/O
A16	SATA0_TX+	SATA 0 Transmit Data+	DP-O	Marvell 88SA8052A1	-

Pin	Signal	Description	Type	Termination	Comment
A17	SATA0_TX-	SATA 0 Transmit Data-	DP-O	Marvell 88SA8052A1	-
A18	SUS_S4#	Indicates Suspend to Disk state	O-3.3	CPLD I/O	CPLD I/O
A19	SATA0_RX+	SATA 0 Receive Data+	DP-I	Marvell 88SA8052A1	-
A20	SATA0_RX-	SATA 0 Receive Data-	DP-I	Marvell 88SA8052A1	-
A21	GND_3	Power Ground	PWR		-
A22	SATA2_TX+	Not connected	nc		not supported
A23	SATA2_TX-	Not connected	nc		not supported
A24	SUS_S5#	Indicates Soft Off state	O-3.3	CPLD I/O	CPLD I/O
A25	SATA2_RX+	Not connected	nc		not supported
A26	SATA2_RX-	Not connected	nc		not supported
A27	BATLOW#	Indicates low external battery	I-3.3	-	CPLD I/O
A28	ATA_ACT#	SATA, IDE, SD Activity Indicator	O-3.3	Buffered Output	-
A29	AC_SYNC	HD Audio Sync	O-3.3	PD 22k in US15W	-
A30	AC_RST#	HD Audio Reset	O-3.3	PD 22k in US15W	-
A31	GND_4	Power Ground	PWR	-	-
A32	AC_BITCLK	HD Audio Clock	O-3.3	PD 22k in US15W	24MHz
A33	AC_SDOUT	HD Audio Data	O-3.3	PD 22k in US15W	-
A34	BIOS_DISABLE#	Disable Module BIOS. Enables boot from a BIOS on Baseboard	I-3.3	PU 10k 3.3V	fir external LPC FWH
A35	THRMTRIP#	CPU thermal shutdown indicator	O-3.3	PU 2k 3.3V	-
A36	USB3-	USB Data- Port #3	DP-I/O	PD 15k in US15W	-
A37	USB3+	USB Data+ Port #3	DP-I/O	PD 15k in US15W	-
A38	USB_2_3_OC#	USB Overcurrent Pair 2 / 3	I-3.3	PU 10k 3.3V	-
A39	USB6-	USB Data- Port #6	DP-I/O	PD 15k in US15W	-
A40	USB6+	USB Data+ Port #6	DP-I/O	PD 15k in US15W	-
A41	GND_5	Power Ground	PWR	-	-

Pin	Signal	Description	Type	Termination	Comment
A42	USB4-	USB Data- Port #4	DP-I/O	PD 15k in US15W	-
A43	USB4+	USB Data+ Port #4	DP-I/O	PD 15k in US15W	-
A44	USB_4_5_OC#	USB Overcurrent Pair 4 / 5	I-3.3	PU 10k 3.3V	-
A45	USB0-	USB Data- Port #0	DP-I/O	PD 15k in US15W	-
A46	USB0+	USB Data+ Port #0	DP-I/O	PD 15k in US15W	-
A47	VCC_RTC	RTC Power Supply +3V	PWR	-	-
A48	EXCD0_PERST#	PCIe Express Card 0 Reset	O-3.3	3.3V CMOS IO in US15W	-
A49	EXCD0_CPPE#	PCIe Express Card 0 Request	I-3.3	3.3V CMOS IO in US15W	-
A50	LPC_SERIRQ	LPC Serial Interrupt Request	IO-3.3	PU 8k2 3.3V	-
A51	GND_6	Power Ground	PWR	-	-
A52	PCIE_TX5+	Not connected	nc	-	not supported
A53	PCIE_TX5-	Not connected	nc	-	not supported
A54	SDIO_D0 GPI0	SDIO#0 Data0 General Purpose Input 0	I/O-3.3 I-3.3	PU 75k in US15W PU 10k 3.3V	Bus Switch PI5C3390
A55	PCIE_TX4+	Not connected	nc	-	Not Supported
A56	PCIE_TX4-	Not connected	nc	-	Not Supported
A57	GND_7	Power Ground	PWR	-	-
A58	PCIE_TX3+	Not connected	nc	-	Not Supported
A59	PCIE_TX3-	Not connected	nc	-	Not Supported
A60	GND_8	Power Ground	PWR	-	-
A61	PCIE_TX2+	Not connected	nc	-	Not Supported
A62	PCIE_TX2-	Not connected	nc	-	Not Supported
A63	SDIO_D1 GPI1	SDIO#0 Data1 General Purpose Input 1	I/O-3.3 I-3.3	PU 75k in US15W PU 10k 3.3V	Bus Switch PI5C3390
A64	PCIE_TX1+	Not connected	nc	-	Not Supported
A65	PCIE_TX1-	Not connected	nc	-	Not Supported
A66	GND_9	Power Ground	PWR	-	-
A67	SDIO_D2	SDIO#0 Data2	I/O-	PU 75k in	Bus Switch

Pin	Signal	Description	Type	Termination	Comment
	GPI2	General Purpose Input 2	3.3 I-3.3	US15W PU 10k 3.3V	PI5C3390
A68	PCIE_TX0+	PCIe lane #0 Transmit+	DP-O	PU 50R inUS15W	-
A69	PCIE_TX0-	PCIe lane #0 Transmit-	DP-O	PU 50R inUS15W	-
A70	GND_10	Power Ground	PWR	-	-
A71	LVDS_A0+	LVDS Channel A (positive)	DP-O	PU 50R inUS15W	-
A72	LVDS_A0-	LVDS Channel A (negative)	DP-O	PU 50R inUS15W	-
A73	LVDS_A1+	LVDS Channel A (positive)	DP-O	PU 50R inUS15W	-
A74	LVDS_A1-	LVDS Channel A (negative)	DP-O	PU 50R inUS15W	-
A75	LVDS_A2+	LVDS Channel A (positive)	DP-O	PU 50R inUS15W	-
A76	LVDS_A2-	LVDS Channel A (negative)	DP-O	PU 50R inUS15W	-
A77	LVDS_VDD_EN	LVDS Panel Power Control	O-3.3	PD 100k	
A78	LVDS_A3+	LVDS Channel A (positive)	DP-O	PU 50R inUS15W	-
A79	LVDS_A3-	LVDS Channel A (negative)	DP-O	PU 50R inUS15W	-
A80	GND_11	Power Ground	PWR	-	-
A81	LVDS_A_CK+	LVDS Channel A Clock+	DP-O	PU 50R inUS15W	-
A82	LVDS_A_CK-	LVDS Channel A Clock-	DP-O	PU 50R inUS15W	-
A83	LVDS_I2C_CK	LVDS I2C Clock (DDC)	IO-3.3	PU 10k 3.3V	-
A84	LVDS_I2C_DAT	LVDS I2C Data (DDC)	IO-3.3	PU 10k 3.3V	
A85	SDIO_D3 GPI3	SDIO# Data3 General Purpose Input 3	I/O-3.3 I-3.3	PU 75k in US15W PU 10k 3.3V	Bus Switch PI5C3390
A86	KBD_RST#	Keyboard Reset	I-3.3	PU 10k 3.3V	-
A87	KBD_A20GATE	A20 gate	I-3.3	PU 10k 3.3V	-
A88	PCIE0_CK_REF	PCIe Clock (positive)	DP-O	-	100MHz

Pin	Signal	Description	Type	Termination	Comment
	+				
A89	PCIE0_CK_REF -	PCIe Clock (negative)	DP-O	-	100MHz
A90	GND_12	Power Ground	PWR	-	-
A91	RSVD1	Reserved	nc	-	-
A92	RSVD2	Reserved	nc	-	-
A93	SDIO_Clk GPO0	SDIO#0 Clock General Purpose Output 0	O-3.3 O-3.3	PU 75k in US15W PD 1k	Bus Switch PI5C3390
A94	RSVD3	Reserved	nc	-	-
A95	RSVD4	Reserved	nc	-	-
A96	GND_13	Power Ground	PWR	-	-
A97	VCC_12V_1	12V VCC	PWR	-	-
A98	VCC_12V_2	12V VCC	PWR	-	-
A99	VCC_12V_3	12V VCC	PWR	-	-
A100	GND_14	Power Ground	PWR	-	-
A101	VCC_12V_4	12V VCC	PWR	-	-
A102	VCC_12V_5	12V VCC	PWR	-	-
A103	VCC_12V_6	12V VCC	PWR	-	-
A104	VCC_12V_7	12V VCC	PWR	-	-
A105	VCC_12V_8	12V VCC	PWR	-	-
A106	VCC_12V_9	12V VCC	PWR	-	-
A107	VCC_12V_10	12V VCC	PWR	-	-
A108	VCC_12V_11	12V VCC	PWR	-	-
A109	VCC_12V_12	12V VCC	PWR	-	-
A110	GND_15	Power Ground	PWR	-	-

Table4: Connector X1A - Row B

Pin	Signal	Description	Type	Termination	Comment
B1	GND_16	Power Ground	PWR	-	-
B2	GBE0_ACT#	Ethernet Activity LED	O-3.3	Buffered 3.3V Output	-

Pin	Signal	Description	Type	Termination	Comment
B3	LPC_FRAME#	LPC Frame Indicator	O-3.3	-	-
B4	LPC_AD0	LPC Address / Data Bus	IO-3.3	PU 20k in US15W	-
B5	LPC_AD1	LPC Address / Data Bus	IO-3.3	PU 20k in US15W	-
B6	LPC_AD2	LPC Address / Data Bus	IO-3.3	PU 20k in US15W	-
B7	LPC_AD3	LPC Address / Data Bus	IO-3.3	PU 20k in US15W	-
B8	LPC_DRQ0#	Not connected	nc	-	-
B9	LPC_DRQ1#	Not connected	nc	-	-
B10	LPC_CLK	LPC Clock	O-3.3	-	up to 33MHz
B11	GND_17	Power Ground	PWR	-	-
B12	PWRBTN#	Power Button Input	I-3.3	PU 100k 3.3V	Diode, serial 470
B13	SMB_CLK	SMBus Clock	O-3.3	PU 4k7 3.3V	-
B14	SMB_DAT	SMBus Data	IO-3.3	PU 4k7 3.3V	-
B15	SMB_ALERT#	SMBus Interrupt	IO-3.3	PU 10k 3.3V	Diode serial
B16	SATA1_TX+	Not connected	nc	-	Not Supported
B17	SATA1_TX-	Not connected	nc	-	Not Supported
B18	SUS_STAT#	Indicates imminent suspend operation; used to notify LPC devices.	O-3.3	-	CPLD I/O
B19	SATA1_RX+	Not connected	nc	-	Not Supported
B20	SATA1_RX-	Not connected	nc	-	Not Supported
B21	GND_18	Power Ground	PWR	-	-
B22	SATA3_TX+	Not connected	nc	-	not supported
B23	SATA3_TX-	Not connected	nc	-	not supported
B24	PWR_OK	Power OK from power supply	I-3.3	PU 100k up after diode	CPLD I/O
B25	SATA3_RX+	Not connected	nc	-	not supported
B26	SATA3_RX-	Not connected	nc	-	not supported
B27	WDT	Indicator for Watchdog	O-3.3	-	CPLD I/O

Pin	Signal	Description	Type	Termination	Comment
		Timeout			
B28	AC_SDIN2	Not connected	nc	-	not supported
B29	AC_SDIN1	Audio Codec Serial Data in 1	I-3.3	PD 22k in US15W	-
B30	AC_SDIN0	Audio Codec Serial Data in 0	I-3.3	PD 22k in US15W	-
B31	GND_19	Power Ground	PWR	-	-
B32	SPKR	Speaker Interface	O-3.3	-	-
B33	I2C_CK	General Purpose I2C Clock	IO-3.3	PU 2k2 3.3V	US15W
B34	I2C_DAT	General Purpose I2C Data	IO-3.3	PU 2k2 3.3V	US15W
B35	THRM#	Over Temperature Indicator	I-3.3	PU 10k	TC7SET08FU input
B36	USB2-	USB Data- Port #2 (USB Mode)	DP-I/O	PD 15k in US15W	-
B37	USB2+	USB Data+ Port #2 (USB Mode)	DP-I/O	PD 15k in US15W	-
B38	USB_6_7_OC#	USB Overcurrent Pair 6 / 7	I-3.3	PU 10k 3.3V	-
B39	USB7-	USB Data- Port #7 USB Data- Client (Client Mode)	DP-I/O DP-I/O	PD 15k in US15W PU 1k5 in US15W	- -
B40	USB7+	USB Data+ Port #7 USB Data+ Client (Client Mode)	DP-I/O DP-I/O	PD 15k in US15W PU 1k5 in US15W	- -
B41	GND_20	Power Ground	PWR	-	-
B42	USB5-	USB Data- Port #5	DP-I/O	PD 15k in US15W	-
B43	USB5+	USB Data+ Port #5	DP-I/O	PD 15k in US15W	-
B44	USB_0_1_OC#	USB Overcurrent Pair 0 /1	I-3.3	PU 10k 3.3V	-
B45	USB1-	USB Data- Port #1	DP-I/O	PD 15k in US15W	-
B46	USB1+	USB Data+ Port #1	DP-I/O	PD 15k in US15W	-
B47	EXCD1_PERST#	PCIe Express Card 1 Reset	O-3.3	-	-
B48	EXCD1_CPPE#	PCIe Express Card 1 Request	I-3.3	PU 8k2 3.3V	-
B49	SYS_RESET#	Reset button input	I-3.3	PU 100k 3.3V	CPLD I/O

Pin	Signal	Description	Type	Termination	Comment
				after diode and 470R Serial	
B50	CB_RESET#	Carrier Board Reset	O-3.3	-	CPLD I/O
B51	GND_21	Power Ground	PWR	-	-
B52	PCIE_RX5+	Not connected	nc	-	Not Supported
B53	PCIE_RX5-	Not connected	nc	-	Not Supported
B54	SDIO_CMD GPO1	SDIO#0 Command General Purpose Output 1	I/O-3.3 O-3.3	PU 75k in US15W PD 1k	Bus Switch PI5C3390
B55	PCIE_RX4+	Not connected	nc	-	Not Supported
B56	PCIE_RX4-	Not connected	nc	-	Not Supported
B57	SDIO_WP GPO2	SDIO#0 WriteProtection General Purpose Output 2	I-3.3 O-3.3	PU 75k in US15W PD 1k	Bus Switch PI5C3390
B58	PCIE_RX3+	Not connected	nc	-	Not Supported
B59	PCIE_RX3-	Not connected	nc	-	Not Supported
B60	GND_22	Power Ground	PWR	-	-
B61	PCIE_RX2+	Not connected	nc	-	Not Supported
B62	PCIE_RX2-	Not connected	nc	-	Not Supported
B63	SDIO_CD# GPO3	SDIO#0 CardDetect General Purpose Output 3	I-3.3 O-3.3	PU 75k in US15W PD 1k	Bus Switch PI5C3390
B64	PCIE_RX1+	Not connected	nc		Not Supported
B65	PCIE_RX1-	Not connected	nc		Not Supported
B66	WAKE0#	PCI Express Wake Event	I-3.3	PU 10k 3.3V	CPLD I/O
B67	WAKE1#	General Purpose Wake Event	I-3.3	PU 10k 3.3V	CPLD I/O
B68	PCIE_RX0+	PCIe lane #0 Receive+	DP-I	PD 50R inUS15W	-
B69	PCIE_RX0-	PCIe lane #0 Receive-	DP-I	PD 50R inUS15W	-
B70	GND_23	Power Ground	PWR	-	-
B71	LVDS_B0+	Serial DVO Red+	DP-O	PU 50R in US15W	Configuration option

Pin	Signal	Description	Type	Termination	Comment
B72	LVDS_B0-	Serial DVO Red-	DP-O	PU 50R in US15W	Configuration option
B73	LVDS_B1+	Serial DVO Green+	DP-O	PU 50R in US15W	Configuration option
B74	LVDS_B1-	Serial DVO Green-	DP-O	PU 50R in US15W	Configuration option
B75	LVDS_B2+	Serial DVO Blue+	DP-O	PU 50R in US15W	Configuration option
B76	LVDS_B2-	Serial DVO Blue-	DP-O	PU 50R in US15W	Configuration option
B77	LVDS_B3+	Serial DVO+	DP-O	PD 50R in US15W	Configuration option
B78	LVDS_B3-	Serial DVO-	DP-O	PD 50R in US15W	Configuration option
B79	LVDS_BKLT_EN	Backlight Enable	O-3.3	PD 100k	-
B80	GND_24	Power Ground	PWR	-	-
B81	LVDS_B_CK+	Serial DVO CLK+	nc	PU 50R in US15W	Configuration option
B82	LVDS_B_CK-	Serial DVO CLK-	nc	PU 50R in US15W	Configuration option
B83	LVDS_BKLT_CTRL	Backlight Brightness Control	O-3.3	-	-
B84	VCC_5V_SBY	+5V Standby	PWR	-	-
B85	VCC_5V_SBY	+5V Standby	PWR	-	-
B86	VCC_5V_SBY	+5V Standby	PWR	-	-
B87	VCC_5V_SBY	+5V Standby	PWR	-	-
B88	RSVD5	Reserved	-	-	-
B89	VGA_RED	Not connected	nc	-	not supported
B90	GND_25	Power Ground	PWR	-	-
B91	VGA_GRN	Serial Digital Video TV-OUT Sync CLK	DP-I	-	Configuration option
B92	VGA_BLU	Serial Digital Video TV-OUT Sync CLK	DP-I	-	Configuration option
B93	VGA_HSYNC	Serial Digital Video Field Stall	DP-I	-	Configuration option
B94	VGA_VSYNC	Serial Digital Video Field Stall	DP-I	-	Configuration option
B95	VGA_I2C_CK	Serial DVO Control Clock	I/OD	-	Configuration option
B96	VGA_I2C_DAT	Serial DVO Control Data	I/OD	-	Configuration option
B97	TV_DAC_A	Not connected	nc	-	not supported
B98	TV_DAC_B	Not connected	nc	-	not

Pin	Signal	Description	Type	Termination	Comment
					supported
B99	TV_DAC_C	Not connected	nc	-	not supported
B100	GND_26	Power Ground	PWR	-	-
B101	VCC_12V_13	12V VCC	PWR	-	-
B102	VCC_12V_14	12V VCC	PWR	-	-
B103	VCC_12V_15	12V VCC	PWR	-	-
B104	VCC_12V_16	12V VCC	PWR	-	-
B105	VCC_12V_17	12V VCC	PWR	-	-
B106	VCC_12V_18	12V VCC	PWR	-	-
B107	VCC_12V_19	12V VCC	PWR	-	-
B108	VCC_12V_20	12V VCC	PWR	-	-
B109	VCC_12V_21	12V VCC	PWR	-	-
B110	GND_27	Power Ground	PWR		

Note: The termination resistors in this table are already mounted on the COM Express® module. Refer to the PICMG COM Express® Design Guide for information about additional termination resistors.

Table 5: Connector X1B - Row C

Pin	Signal	Description	Type	Termination	Comment
C1	GND	Power Ground	PWR	-	-
C2	IDE_D7	IDE Data Bus	I/O-5T	-	-
C3	IDE_D6	IDE Data Bus	I/O-5T	-	-
C4	IDE_D3	IDE Data Bus	I/O-5T	-	-
C5	IDE_D15	IDE Data Bus	I/O-5T	-	-
C6	IDE_D8	IDE Data Bus	I/O-5T	-	-
C7	IDE_D9	IDE Data Bus	I/O-5T	-	-
C8	IDE_D2	IDE Data Bus	I/O-5T	-	-
C9	IDE_D13	IDE Data Bus	I/O-5T	-	-
C10	IDE_D1	IDE Data Bus	I/O-5T	-	-
C11	GND	Power Ground	PWR	-	-
C12	IDE_D14	IDE Data Bus	I/O-5T	-	-
C13	IDE_IORDY	IDE I/O Ready	I/O-	PU 10k 3.3V	-

Pin	Signal	Description	Type	Termination	Comment
			5T	(S0)	
C14	IDE_IOR#	IDE I/O Read	I/O-3,3	-	-
C15	PCI_PME#	PCI Power Management Event	I/O-3,3	PU 10k 3.3V (A)	Serial diode, CPLD
C16	PCI_GNT2#	PCI Bus Grant 2	O-3,3		PCI Bridge
C17	PCI_REQ2#	PCI Bus Request 2	I-5T	PU 8k2 5V (S0)	PCI Bridge
C18	PCI_GNT1#	PCI Bus Grant 1	O-3,3		PCI Bridge
C19	PCI_REQ1#	PCI Bus Request 1	I-5T	PU 8k2 5V (S0)	PCI Bridge
C20	PCI_GNT0#	PCI Bus Grant 0	O-3,3		PCI Bridge
C21	GND	Power Ground	PWR	-	-
C22	PCI_REQ0#	PCI Bus Request 0	I-5T	PU 8k2 5V (S0)	PCI Bridge
C23	PCI_RST#	PCI Bus Reset	O-3,3	-	PCI Bridge
C24	PCI_AD0	PCI Address & Data Bus line	I/O-5T	-	PCI Bridge
C25	PCI_AD2	PCI Address & Data Bus line	I/O-5T	-	PCI Bridge
C26	PCI_AD4	PCI Address & Data Bus line	I/O-5T	-	PCI Bridge
C27	PCI_AD6	PCI Address & Data Bus line	I/O-5T	-	PCI Bridge
C28	PCI_AD8	PCI Address & Data Bus line	I/O-5T	-	PCI Bridge
C29	PCI_AD10	PCI Address & Data Bus line	I/O-5T	-	PCI Bridge
C30	PCI_AD12	PCI Address & Data Bus line	I/O-5T	-	PCI Bridge
C31	GND	Power Ground	PWR	-	-
C32	PCI_AD14	PCI Address & Data Bus line	I/O-5T	-	PCI Bridge
C33	PCI_C/BE1#	PCI Bus Command and Byte enables 1	I/O-5T	-	PCI Bridge
C34	PCI_PERR#	PCI Bus Grant Error	I/O-5T	PU 8k2 5V (S0)	PCI Bridge
C35	PCI_LOCK#	PCI Bus Lock	I/O-5T	PU 8k2 5V (S0)	PCI Bridge
C36	PCI_DEVSEL#	PCI Bus Device Select	I/O-5T	PU 8k2 5V (S0)	PCI Bridge
C37	PCI_IRDY#	PCI Bus Initiator Ready	I/O-5T	PU 8k2 5V (S0)	PCI Bridge
C38	PCI_C/BE2#	PCI Bus Command and	I/O-	-	PCI Bridge

Pin	Signal	Description	Type	Termination	Comment
		Byte enables 2	5T		
C39	PCI_AD17	PCI Address & Data Bus line	I/O-5T	-	PCI Bridge
C40	PCI_AD19	PCI Address & Data Bus line	I/O-5T	-	PCI Bridge
C41	GND	Power Ground	PWR	-	-
C42	PCI_AD21	PCI Address & Data Bus line	I/O-5T	-	PCI Bridge
C43	PCI_AD23	PCI Address & Data Bus line	I/O-5T	-	PCI Bridge
C44	PCI_C/BE3#	PCI Bus Command and Byte enables 3	I/O-5T	-	PCI Bridge
C45	PCI_AD25	PCI Address & Data Bus line	I/O-5T	-	PCI Bridge
C46	PCI_AD27	PCI Address & Data Bus line	I/O-5T	-	PCI Bridge
C47	PCI_AD29	PCI Address & Data Bus line	I/O-5T	-	PCI Bridge
C48	PCI_AD31	PCI Address & Data Bus line	I/O-5T	-	PCI Bridge
C49	PCI_IRQA#	PCI Bus Interrupt Request A	I-5T	PU 8k2 5V (S0)	PCI Bridge
C50	PCI_IRQB#	PCI Bus Interrupt Request B	I-5T	PU 8k2 5V (S0)	PCI Bridge
C51	GND	Power Ground	PWR	-	-
C52	PEG_RX0+	Serial Digital Video TV-OUT Sync CLK	DP-I	-	Configuration option
C53	PEG_RX0-	Serial Digital Video TV-OUT Sync CLK	DP-I	-	Configuration option
C54	TYPE0#	Not connected for type 2 module	nc	-	-
C55	PEG_RX1+	Serial DVO+	DP-O	PD 50R in US15W	Configuration option
C56	PEG_RX1-	Serial DVO-	DP-O	PD 50R in US15W	Configuration option
C57	TYPE1#	Not connected for type 2 module	nc	-	-
C58	PEG_RX2+	Serial Digital Video Field Stall+	DP-I	-	Configuration option
C59	PEG_RX2-	Serial Digital Video Field Stall-	DP-I	-	Configuration option
C60	GND	Power Ground	PWR	-	-
C61	PEG_RX3+	Not connected	nc	-	-
C62	PEG_RX3-	Not connected	nc	-	-

Pin	Signal	Description	Type	Termination	Comment
C63	RSVD	Not connected	nc	-	-
C64	RSVD	Not connected	nc	-	-
C65	PEG_RX4+	Not connected	nc	-	-
C66	PEG_RX4-	Not connected	nc	-	-
C67	RSVD	Not connected	nc	-	-
C68	PEG_RX5+	Not connected	nc	-	-
C69	PEG_RX5-	Not connected	nc	-	-
C70	GND	Power Ground	PWR	-	-
C71	PEG_RX6+	Not connected	nc	-	-
C72	PEG_RX6-	Not connected	nc	-	-
C73	SDVO_DATA	SDVO_CTRLDATA	I/O-3,3	-	-
C74	PEG_RX7+	Not connected	nc	-	-
C75	PEG_RX7-	Not connected	nc	-	-
C76	GND	Power Ground	PWR	-	-
C77	RSVD	Not connected	nc	-	-
C78	PEG_RX8+	Not connected	nc	-	-
C79	PEG_RX8-	Not connected	nc	-	-
C80	GND	Power Ground	PWR	-	-
C81	PEG_RX9+	Not connected	nc	-	-
C82	PEG_RX9-	Not connected	nc	-	-
C83	RSVD	Not connected	nc	-	-
C84	GND	Power Ground	PWR	-	-
C85	PEG_RX10+	Not connected	nc	-	-
C86	PEG_RX10-	Not connected	nc	-	-
C87	GND	Power Ground	PWR	-	-
C88	PEG_RX11+	Not connected	nc	-	-
C89	PEG_RX11-	Not connected	nc	-	-
C90	GND	Power Ground	PWR	-	-
C91	PEG_RX12+	Not connected	nc	-	-
C92	PEG_RX12-	Not connected	nc	-	-
C93	GND	Power Ground	PWR	-	-
C94	PEG_RX13+	Not connected	nc	-	-
C95	PEG_RX13-	Not connected	nc	-	-
C96	GND	Power Ground	PWR	-	-
C97	RSVD	Not connected	nc	-	-
C98	PEG_RX14+	Not connected	nc	-	-
C99	PEG_RX14-	Not connected	nc	-	-

Pin	Signal	Description	Type	Termination	Comment
C100	GND	Power Ground	PWR	-	-
C101	PEG_RX15+	Not connected	nc	-	-
C102	PEG_RX15-	Not connected	nc	-	-
C103	GND	Power Ground	PWR	-	-
C104	VCC_12V	12V VCC	PWR	-	-
C105	VCC_12V	12V VCC	PWR	-	-
C106	VCC_12V	12V VCC	PWR	-	-
C107	VCC_12V	12V VCC	PWR	-	-
C108	VCC_12V	12V VCC	PWR	-	-
C109	VCC_12V	12V VCC	PWR	-	-
C110	GND	Power Ground	PWR	-	-

Note: The termination resistors in this table are already mounted on the COM Express® board. Refer to the PICMG COM Express® Design Guide for information about additional termination resistors.

Table6: Connector X1B - Row D

Pin	Signal	Description	Type	Termination	Comment
D1	GND	Power Ground	PWR	-	-
D2	IDE_D5	IDE Data Bus	I/O-5T	-	-
D3	IDE_D10	IDE Data Bus	I/O-5T	-	-
D4	IDE_D11	IDE Data Bus	I/O-5T	-	-
D5	IDE_D12	IDE Data Bus	I/O-5T	-	-
D6	IDE_D4	IDE Data Bus	I/O-5T	-	-
D7	IDE_D0	IDE Data Bus	I/O-5T	-	-
D8	IDE_REQ	IDE Data Bus	I/O-5T	-	-
D9	IDE_IOW#	IDE IO Write	O-3,3	-	-
D10	IDE_ACK#	IDE DMA Acknowledge	O-3,3	-	-
D11	GND	Power Ground	PWR	-	-
D12	IDE_IRQ	IDE Interrupt Request	I-5T	PD 10k 3V3	-
D13	IDE_A0	IDE Address Bus	O-3,3	-	-
D14	IDE_A1	IDE Address Bus	O-3,3	-	-
D15	IDE_A2	IDE Address Bus	O-3,3	-	-
D16	IDE_CS1#	IDE Chip Select Channel 0	O-3,3	-	-
D17	IDE_CS3#	IDE Chip Select	O-3,3	-	-

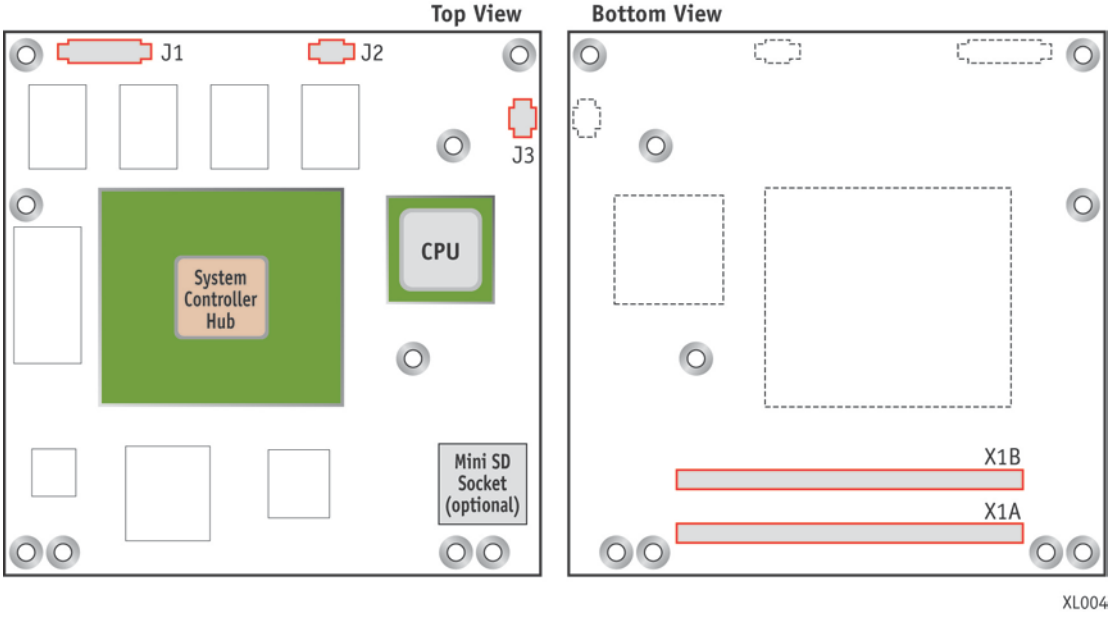
Pin	Signal	Description	Type	Termination	Comment
		Channel 1			
D18	IDE_RESET#	IDE Hard Drive Reset	O-3,3	-	CPLD
D19	PCI_GNT3#	PCI Bus Grant 3	O-3,3		PCI Bridge
D20	PCI_REQ3#	PCI Bus Request 0	I-5T	PU 8k2 5V (S0)	PCI Bridge
D21	GND	Power Ground	PWR	-	-
D22	PCI_AD1	PCI Address & Data Bus line	I/O-5T	-	PCI Bridge
D23	PCI_AD3	PCI Address & Data Bus line	I/O-5T	-	PCI Bridge
D24	PCI_AD5	PCI Address & Data Bus line	I/O-5T	-	PCI Bridge
D25	PCI_AD7	PCI Address & Data Bus line	I/O-5T	-	PCI Bridge
D26	PCI_C/BE0#	PCI Bus Command and Byte enables 0	I/O-5T	-	PCI Bridge
D27	PCI_AD9	PCI Address & Data Bus line	I/O-5T	-	PCI Bridge
D28	PCI_AD11	PCI Address & Data Bus line	I/O-5T	-	PCI Bridge
D29	PCI_AD13	PCI Address & Data Bus line	I/O-5T	-	PCI Bridge
D30	PCI_AD15	PCI Address & Data Bus line	I/O-5T	-	PCI Bridge
D31	GND	Power Ground	PWR	-	-
D32	PCI_PAR	PCI Bus Parity	I/O-5T	-	PCI Bridge
D33	PCI_SERR#	PCI Bus System Error	I/O-5T	PU 8k2 5V (S0)	PCI Bridge
D34	PCI_STOP#	PCI Bus Stop	I/O-5T	PU 8k2 5V (S0)	PCI Bridge
D35	PCI_TRDY#	PCI Bus Target Ready	I/O-5T	PU 8k2 5V (S0)	PCI Bridge
D36	PCI_FRAME#	PCI Bus Cycle Frame	I/O-5T	PU 8k2 5V (S0)	PCI Bridge
D37	PCI_AD16	PCI Address & Data Bus line	I/O-5T	-	PCI Bridge
D38	PCI_AD18	PCI Address & Data Bus line	I/O-5T	-	PCI Bridge
D39	PCI_AD20	PCI Address & Data Bus line	I/O-5T	-	PCI Bridge
D40	PCI_AD22	PCI Address & Data Bus line	I/O-5T	-	PCI Bridge
D41	GND	Power Ground	PWR	-	-
D42	PCI_AD24	PCI Address & Data Bus	I/O-	-	PCI Bridge

Pin	Signal	Description	Type	Termination	Comment
		line	5T		
D43	PCI_AD26	PCI Address & Data Bus line	I/O-5T	-	PCI Bridge
D44	PCI_AD28	PCI Address & Data Bus line	I/O-5T	-	PCI Bridge
D45	PCI_AD30	PCI Address & Data Bus line	I/O-5T	-	PCI Bridge
D46	PCI_IRQC#	PCI Bus Interrupt Request C	I-5T	PU 8k2 5V (S0)	PCI Bridge
D47	PCI_IRQD#	PCI Bus Interrupt Request D	I-5T	PU 8k2 5V (S0)	PCI Bridge
D48	PCI_CLKRUN#	PCI Clock Run	O-3,3	PU 8k2 3.3V (S0)	
D49	PCI_M66EN	PCI_M66EN	I-5T	PU 8k2 5V (S0)	PCI Bridge
D50	PCI_CLK	CLK_PCI_33M_EXT | PCI Clock 33MHz	O-3,3	-	PCI Bridge
D51	GND	Power Ground	PWR	-	-
D52	PEG_TX0+	Serial DVO Red+	DP-O	PU 50R in US15W	Configuration option
D53	PEG_TX0-	Serial DVO Red-	DP-O	PU 50R in US15W	Configuration option
D54	PEG_LANE_RV#	Not connected	nc	-	-
D55	PEG_TX1+	Serial DVO Green+	DP-O	PU 50R in US15W	Configuration option
D56	PEG_TX1-	Serial DVO Green-	DP-O	PU 50R in US15W	Configuration option
D57	TYPE2#	Not connected for type 2 module	nc	-	-
D58	PEG_TX2+	Serial DVO Blue+	DP-O	PU 50R in US15W	Configuration option
D59	PEG_TX2-	Serial DVO Blue-	DP-O	PU 50R in US15W	Configuration option
D60	GND	Power Ground	PWR	-	-
D61	PEG_TX3+	SDVOB_CLK_P	DP-O	-	-
D62	PEG_TX3-	SDVOB_CLK_N	DP-O	-	-
D63	RSVD	-	nc	-	
D64	RSVD	-	nc	-	
D65	PEG_TX4+	Not connected	nc	-	-
D66	PEG_TX4-	Not connected	nc	-	-
D67	GND	Power Ground	PWR	-	-
D68	PEG_TX5+	Not connected	nc	-	-
D69	PEG_TX5-	Not connected	nc	-	-
D70	GND	Power Ground	PWR	-	-
D71	PEG_TX6+	Not connected	nc	-	-

Pin	Signal	Description	Type	Termination	Comment
D72	PEG_TX6-	Not connected	nc	-	-
D73	SDVO_CLK	SDVO_CTRLCLK	IO-3,3	-	-
D74	PEG_TX7+	Not connected	nc	-	Configuration option
D75	PEG_TX7-	Not connected	nc	-	-
D76	GND	Power Ground	PWR	-	-
D77	IDE_CBLID	IDE_CBLID# | IDE cable type detect	I/0-3,3	PU 10k 3V3	-
D78	PEG_TX8+	Not connected	nc	-	-
D79	PEG_TX8-	Not connected c	nc	-	-
D80	GND	Power Ground	PWR	-	-
D81	PEG_TX9+	Not connected	nc	-	-
D82	PEG_TX9-	Not connected	nc	-	-
D83	RSVD	Not connected	nc	-	-
D84	GND	Power Ground	PWR	-	-
D85	PEG_TX10+	Not connected	nc	-	-
D86	PEG_TX10-	Not connected	nc	-	-
D87	GND	Power Ground	PWR	-	-
D88	PEG_TX11+	Not connected	nc	-	-
D89	PEG_TX11-	Not connected	nc	-	-
D90	GND	Power Ground	PWR	-	-
D91	PEG_TX12+	Not connected	nc	-	-
D92	PEG_TX12-	Not connected	nc	-	-
D93	GND	Power Ground	PWR	-	-
D94	PEG_TX13+	Not connected	nc	-	-
D95	PEG_TX13-	Not connected	nc	-	-
D96	GND	Power Ground	PWR	-	-
D97	PEG_ENABLE#	Not connected	nc	-	-
D98	PEG_TX14+	Not connected	nc	-	-
D99	PEG_TX14-	Not connected	nc	-	-
D100	GND	Power Ground	PWR	-	-
D101	PEG_TX15+	Not connected	nc	-	-
D102	PEG_TX15-	Not connected	nc	-	-
D103	GND	Power Ground	PWR	-	-
D104	VCC_12V	12V VCC	PWR	-	-
D105	VCC_12V	12V VCC	PWR	-	-
D106	VCC_12V	12V VCC	PWR	-	-
D107	VCC_12V	12V VCC	PWR	-	-
D108	VCC_12V	12V VCC	PWR	-	-
D109	VCC_12V	12V VCC	PWR	-	-
D110	GND	Power Ground	PWR	-	-

Note: The termination resistors in this table are already mounted on the COM Express® board. Refer to the PICMG COM Express® Design Guide for information about additional termination resistors.

Figure 4: Onboard Connectors



4.1.1Connector J1 – CPLD Debug

The onboard 12-pin connector J1 is for accessing the CPLD.

WARNING: The debug port is for internal use only. Do not connect any devices.

4.1.2Connector J2 – SO DIMM DDR2 Soldered

There is up to 2 GBytes of DDR2 memory supplied on board.

4.1.3Connector J3 - US15WPT JTAG Connector

This is the US15WPT debug connector

WARNING: The debug port is for internal use only. Do not connect any devices.

4.1.4Connector J4 - SDIO/MMC Socket

The onboard SDIO socket J4 provides the SDIO port #0 from US15SCH. See Section 5.3, "SDCard Interface (SDIO)" for more detailed information.

4.1.5Connector J5 - FAN

This is the 3-pin FAN connector for a 5V fan. J5 can be configured in the BIOS setup. See Section 6.3, "Onboard Fan Connector"for more detailed information.

NOTE: Although there is a fan connector on the module, active cooling is not needed for the module to function fully in the -40C to +85C extreme temperature range

4.2 Signal Descriptions

4.2.1PCI Express Interface

The PCI Express* x1 lane is a fast connection interface for many different system devices, such as network controllers, I/O controllers or express card devices. The implementation of this subsystem complies with the COM Express® Specification. Refer to the PICMG COM Express® Design Guide for additional implementation information.

The COMe-cXLi2 COM supports 1 PCI Express x1 lanes. See Table 7 for detailed configuration information.

Table 7: PCI Express Configuration

Source 1	Optional	Standard	Target
Intel US15WPT PCIe #2	-	Intel 82574IT LAN GB	Intel 82574IT LAN GB
Intel US15WPT PCIe #1	COMe PCIe Lane #0		

Only 1x PCIe x1 is available for use.

Notes: 1) The PCI Express lanes can only be used in an x1 configuration. An x4 lane configuration is not possible.
2) PCI Express HotPlug functionality is not supported from the US15WPT SCH.

4.2.2USB Interface

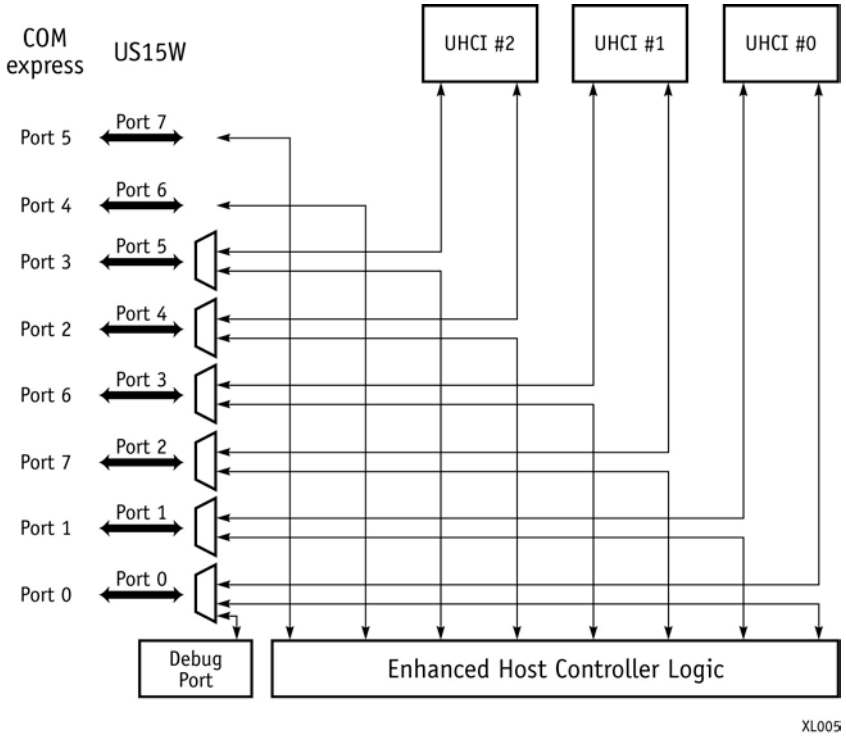
The USB interface comes with three USB controllers (six USB ports). Table 8 shows the USB configuration for the COMe-cXLi2 module.

Table 8: USB Configuration

COMexpress™ Port	SCH US15W Port	Description
USB0	USB0	USB 2.0 compliant ports
USB1	USB1	
USB2	USB4	
USB3	USB5	
USB4	USB6	Not USB 2.0 compliant, no UHCI controller (no USB 1.1 / USB 2.0 only)
USB5	USB7	
USB6	USB3	USB 2.0 compliant port
USB7	USB2	USB Client or USB 2.0 compliant port (configurable in BIOS Setup)

Figure 5 shows the internal USB mapping from the US15WPT system controller hub.

Figure 5: USB Mapping



NOTE: Additional USB connections can be added using external USB hubs.

USB Client Port

The USB interface also supports one USB client port (USB port 7) that can be activated in the BIOS setup. If the client function is disabled in the BIOS this port acts as a standard USB port.

NOTES: 1) USB power lines cannot be connected to the USB client port.
2) Special USB client and host driver software is needed to implement the USB client function. When this driver software is installed, the client port appears as a mass storage device and NDIS Network device or as an NDIS Network device only in the operating system device manager. Please refer to the customer section of the Kontron download page for the COMe-cXLi2 at http://emdcustomersection.kontron.com/ to obtain the driver

Configuration

The USB controllers are PCI bus devices. The BIOS allocates the required system resources during configuration of the PCI bus.

4.2.3SATA Interface

Configuration

The COMe-cXLi2 uses a PATA to SATA bridge for the SATA interface, thus no driver install is required. The SATA controller is a PCIe bus device. The BIOS allocates the required system resources during the PCIe device configuration.

4.2.4Audio Interface

The Intel® System Controller Hub US15WPT supports Intel® High Definition Audio (HDA). This HD audio configuration supports up to four audio streams (with up to 16 channels each), 32-bit sample depth, and sample rates up to 192 KHz.

With this configuration you can implement hardware CODECs on your baseboard for 7.1/5.1 audio systems and SDIF output. The pins for the HD audio are defined in Section 4.1.2.

WARNING: Only baseboards with an HD audio CODEC are supported. AC97 CODECs are not compatible with the US15WPT SCH.

Configuration

The audio controller is a PCI bus device. The BIOS allocates the required system resources during configuration of the PCI device.

4.2.5Serial IRQ

The serial IRQ pin offers a standardized interface to link interrupt request lines to a single wire.

Configuration

The serial IRQ machine is in "Continuous Mode".

4.2.6Graphics Interface

The COMe-cXLi2 uses the Intel® Graphics Media Accelerator 500 (Intel® GMA 500) with a 200MHz GPU clock that is integrated in the Intel® System Controller Hub (US15WPT).This configuration delivers shader-based technologies and high-performance 2D, 3D, and video capabilities. The GMA 500 graphics engine supports a variety of LCD panels with single clock, color depths of 18/24 bit, and resolutions up to WXGA (1366x768). The maximum supported pixel clock on the system controller hub is 112 MHz.

Hardware video decode acceleration relieves the decode burden from the processor and reduces the power consumption of the system. Full hardware decode acceleration of H.264, MPEG2, VC1 and WMV9 eliminates the need for software CODEC as well as offloading the CPU.

The Intel® GMA 500uses the onboard RAM for graphics memory. The pre-allocated memory is defined through BIOS settings.

Possible settings are:

» 1MB

» 4MB

» 8MB

The total amount of graphics memory in the operating system depends on the size of system memory and the driver settings used. The graphics media accelerator (GMA) driver uses DVMT to manage the allocation of system memory according to the needs of the applications that are running. The Intel® Embedded Graphics Driver (IEGD) allocates the maximum graphics memory depending on system memory and driver settings.

Physical Memory on COMe-cXLi2 COM	Pre-allocated Memory in BIOS Setup	Maximum Graphics Memory with GMA Driver	Maximum Graphics Memory with IEGD
512MB	1MB	127MB	352MB
512MB	4MB	126MB	352MB
512MB	8MB	125MB	352MB
1024MB	1MB	255MB	352MB

1024MB	4MB	254MB	352MB
1024MB	8MB	253MB	352MB

Note : When using 1 MByte of pre-allocated memory, operating systems without active GMA or IEGD may have problems displaying a screen (e.g. during a Windows XP installation).

VGA

The COMe-cXLi2 graphics subsystem integrated in the Intel® System Controller Hub US15W does not support VGA output.

LVDS Flat Panel Interface (JILI)

The user interface for flat panels is the JUMPtec* Intelligent LVDS Interface (JILI). The implementation of this subsystem complies with the COM Express® specification. For additional implementation information, refer to the *PICMG COM Express® Design Guide* on the PIGMG website.

SDVO Interface

The COMe-cXLi2 Serial Digital Video Output (SDVO) port is integrated on the US15WPT system controller hub. The SDVO port has the following features:

» Shares pins with the PEG interface

» One SDVO port

» Drives a variety of SDVO devices (e.g., TV-Out Encoders, TMDS and LVDS transmitters)

The implementation of this subsystem complies with the COM Express® specification. For additional implementation information, refer to the *PICMG COM Express® Design Guide* on the PICMG website.

4.2.7Ethernet Interface

The Ethernet interface on the COMe-cXLi2 COM is the industrial temperature version of the Intel® 82574 Gigabit Ethernet Controller. The GbE controller is connected to the PCI Express Switch port #1. The controller supports a 10/100/1000 Base-T interface and it auto-negotiates the use of 10 Mbit/sec, 100 Mbit/sec or 1Gbit/sec connections.

The network interface operates at its lowest power (<1W) when GbE is fully active. The interface supports functions such as WOL (WakeOnLAN) and PXE (Preboot eXecution Environment) boot.

For cable lengths and terminations on your baseboard, refer to the PICMG *COM Express® Design Guide* on the PICMG website.

Configuration

The Ethernet controller is a PCI Express bus device. The BIOS allocates the required system resources during the configuration of the PCIe device.

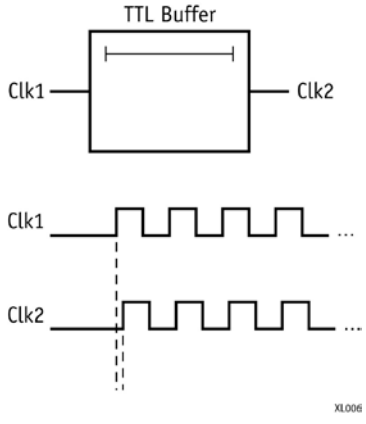
4.2.8 LPC Bus Interface

The Low Pin Count (LPC) interface signals are connected to the LPC bus bridge, which is located on the US15WPT system controller hub. The LPC low-speed interface can be used for peripheral circuits. For example, it can be used as an external super I/O controller to combine legacy-device support into a single IC. The implementation of this subsystem complies with the COM Express® specification. For additional implementation information, refer to the *PICMG COM Express® Design Guide* on the PICMG website.

The LPC bus does not support DMA (Direct Memory Access) and therefore imposes limitations for ISA bus and standard I/Os (SIOs) like floppy or LPT interface implementations.

WARNING: When more than one device is connected to the LPC bus, a clock buffer is required. Because of the power management of the LPC bus, you must use great care with clock buffers that require synchronization as they could prevent the board from booting up.

Figure 6: Standard Clock Buffer



NOTE: When using a standard clock buffer on the baseboard, be aware that the generated delay must be considered for the length matching of the layout.

Clock Buffer Reference Schematic

The schematic in Figure 7 shows an implementation example for the clock buffer.

Figure 7: LPC Clock Buffer

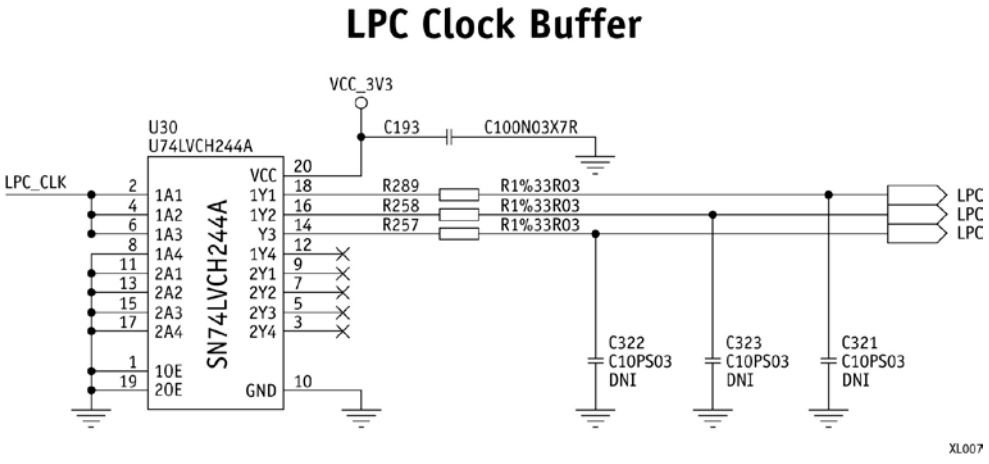


Table 9: LPC Addresses

Address (HEX)	Device
0000 - 00FF	IBM PC compatible devices (IRQ-Controller, Keyboard, RTC etc.)
002E-002F	Optional: Super I/O W83627
004e - 004f	TPM
01F0 - 01F7	Fixed Disk
03C0 - 03CF	VGA/EGA compatible registers
03F6	Fixed Disk
0400 - 043F	SMBus
0480 - 04BF	GPIO SCH
04D0 - 04D1	IRQ Configuration
08F0 - 08FF	Optional
0900 - 091F	Power Management
0A80 - 0A83	Reserved
0CF8 - 0CFF	PCI Configuration
D880 - D887	PCI LAN Controller *
E080 - E09F	PCI USB Controller *
E480 - E49F	PCI USB Controller *
E880 - E887	PCI VGA Controller *
EF00 - EF1F	PCI USB Controller*
FFA0 – FFAF	PCI IDE Controller *

* = not fixed, configured by the BIOS automatically and may be different in other system configurations.

Table 10: Device Addresses

Address (HEX)	Device
00000000 - 0009FFFF	DOS- (Real mode-) memory
000A0000 - 000BFFFF	Display memory
000C0000 - 000CBFFF	VGA Bios
000CC000 - 000DFFFF	Other Option ROM
000E0000 - 000EFFFF	System BIOS extended space
000F0000 - 000FFFFF	System BIOS base segment
00100000 - 7FFFFFFF	System Memory
80000000 - FFF00000	PCI Memory, other extensions
CFDDC000 - CFFFFFFF	PCI LAN Controller
D0000000 - DFFFFFFF	PCI VGA Controller / Audio Controller / USB Controller
FEC00000 - FEC00040	APIC Configuration
FED00000 - FED003FF	Event Timer
FED10000 - dynamic	Audio Controller
FED40000 - FED4BFFF	LPC Configuration
F0000000 - F0003FFF	RCRB (Root Complex)
FFC00000 - FFF00000	Reserved
FFF00000 - FFFFFFFF	Firmware Hub
FFF80000 - FFFFFFFF	Mapping space for BIOS ROM

For further details, please refer to the Intel "System Controller Hub External Design Specification (EDS)", "I/O Address Space" chapter on the Intel website at http://www.intel.com.

4.2.9Power Control Interface

Power Good (PWR_OK)

The COMe-cXLi2 COM provides an external input for a power-good signal (pin B24). The implementation of this subsystem complies with the COM Express®

Specification. PWR_OK is internally pulled up to 3.3V and must be high-level to power on the module.

Power Button (PWRBTN#)

The power button (pin B12) is available through the module connector as defined in the pin-out list. To start the module using the power button the PWRBTN# signal must be at least 50ms (50ms ≤ t < 4sec) at low-level power.

By pressing the power button for at least four seconds, the module can be put into the power-off mode.

Reset Button (SYS_RESET#)

The reset button (pin B49) is available through the module connector as defined in the pin-out list. The module stays in reset as long as SYS_RESET# is grounded.

Power Supply

The COMe-cXLi2 COM has a wide range of power inputs, from 5V to 18V DC. The supply voltage is applied through 42 pins (VCC) on the module connector.

The module does not support ATX mode. The COMe-cXLi module will auto power on whenever +5V_Standby or +12V is present without pressing the power on button.

Single Supply Mode

Single Supply Mode:

In single supply mode the module starts automatically when VCC power is connected and Power Good input is open or at high-level (internal PU to 3.3V). PS_ON# is not used in single supply mode.

To power on the module from the S5 state, press the power button or reconnect VCC.

Table 11: Single Supply Mode

State	PWRBTN#	PWR_OK	V5_StdBy	VCC
G3	X	x	x	0
G3 -> S0	High	open / high	x	connecting VCC
S5	high	open / high	x	VCC

S5 -> S0	PWRBTN Event	open / high	x	reconnecting VCC

NOTES: 1) Columns marked "x" are not relevant for the specified power state.
2) All ground pins have to be tied to the ground plane of the carrier board.

4.2.10 Miscellaneous Circuits

Speaker

The implementation of this subsystem complies with the COM Express® Specification. For additional implementation information, refer to the PICMG COM Express® Design Guide.

Battery

The implementation of this subsystem complies with the COM Express® specification. For additional implementation information, refer to the *PICMG COM Express® Design Guide* on the PICMG website.

In compliance with the EN60950 standard, there are at least two current-limiting devices (resistor and diode) between the battery and the consuming component.

I^2C Bus

The CPLD implementation connects LPC to the I^2C controller to allow higher speed I^2C transactions than in previous I/O implementations.

For additional information, refer to the *PICMG COM Express® Design Guide* on the PICMG website and I^2C application notes and JIDA specifications, which are available on the Kontron website at http://emdcustomersection.kontron.com/.

See the Chapter 8, "BIOS Operation" for supported I^2C features.

SMBus

System Management Bus (SMB) signals are connected to the SMBus controller, which is located on the US15WPT system controller hub. The SMBus is a 2-wire bi-directional bus (clock and serial data) used for system management tasks

such as reading parameters from a memory card or reading temperatures and voltages of system components.

The SMBus uses the same signaling scheme as the I^2C bus.

PCI Bus

The US15WPT system controller hub does not support PCI.

IDE Port

The IDE host adapter on the US15WPT system controller hub supports UDMA-33/66/100 operation. The implementation of this subsystem complies with the COM Express® Specification. For additional implementation information, refer to the *PICMG COM Express® Design Guide* on the PICMG website.

5 Special Features

5.1 Hyper-Threading

Hyper-Threading (officially termed Hyper-Threading Technology or HTT) is an Intel-proprietary technology used to improve parallelization of computations performed on PCs. Hyper-threading works by duplicating certain sections of the processor—those that store the architectural state -- but not duplicating the main execution resources. A hyper-threading equipped processor can appear to be two "logical" processors to the host operating system, thus allowing the operating system to schedule two threads or processes simultaneously. Hyper Threading Technology support always depends on the operating system.

5.2 Enhanced Speedstep Technology

The Intel® Atom Processor Z520 supports the Intel® Enhanced SpeedStep™ technology, which automatically switches the processor between maximum performance mode and battery-optimized mode, depending on the needs of the application being run. Speedstep technology lets you optimize the system performance to match application requirements. When powered by a battery or running in idle mode, the processor drops to lower frequencies (by changing the CPU ratios) and voltage to conserving battery life while maintaining a high level of performance. The frequency is set back to high automatically, allowing you to customize performance.

Note: To use Enhanced SpeedStep™ technology, you need an operating system that supports it.

Disabling Speedstep in the BIOS enables manual control of CPU performance. You can set the CPU performance state in the BIOS setup or use third-party software to control CPU performance states.

5.3 SDCard Interface (SDIO)

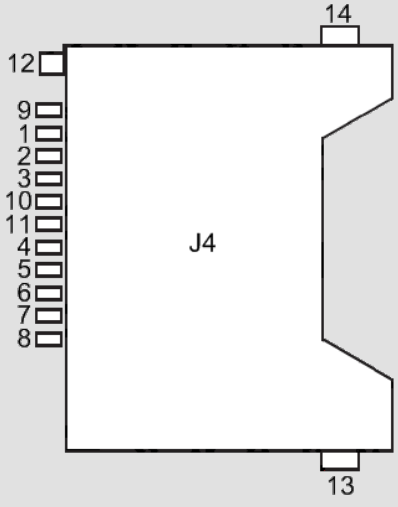
SD card is a standard for removable memory storage. It is designed and licensed by the SD Card Association (http://sdcard.org). The card form factor, electrical interface, and protocol are all part of the SD Card specification. The US15WPT system controller hub supports up to three SDIO interfaces. On the COMe-cXLi2 COM the first interface, SDIO#0, is used for the onboard microSD Card socket. The second port, SDIO#1, provides the SD card interface and shares pins with the GPIO signals to the baseboard. SDIO#3 is not used and is deactivated.

NOTE: The integrated SDIO 1.1 / MMC 4.1 controller on the US15WPT only supports byte-address mode for SDIO storage cards up to 2GB. Sector-addressing and SDHC are not supported.

» MMC 4.1 supports transfer rates up to 48 MHz and bus widths of 1, 4, or 8 bits

» SDIO 1.1 supports transfer rates up to 24 MHz and bus widths of 1 or 4 bits.

Figure 8: Onboard microSD/MMC Socket J4



1	DAT2 – Data Line 2
2	CD/DATA3
3	CMD – Command Line
4	VDD - Supply Voltage - 3.3V
5	CLK - Clock
6	VSS2 - Supply Voltage - GND
7	DAT0 - Data Line 0
8	DAT1 - Data Line 1
9	GND - Lever
10	Detect Switch
11	Not connected
12	Detect
13	Ground 0
14	Ground 1

Table 12. SDIO/GPIO on the COM Express® Connector

General Purpose Input/Output (GPIO)	SD Interface (SDIO) Signals
GPI0	SLOT0_DATA0
GPI1	SLOT0_DATA1
GPI2	SLOT0_DATA2
GPI3	SLOT0_DATA3
GPO0	SLOT0_CLK
GPO1	SLOT0_CMD
GPO2	SLOT0_WP
GPO3	SLOT0_CD#

NOTES: 1) The SLOT0-CMD line needs a pull-up resistor that varies depending on the length of the electrical paths (typically from 10k Ohm

to 100k Ohm).
2) The maximum length for SDIO signals on the baseboard is 80mm
3) SDIO boot is supported on baseboards that conform to the maximum length
specification for SDIO (80mm).

5.4 Watchdog

This feature is implemented within an I^2C Watchdog and offers a single-stage watchdog. You can configure the Watchdog Timer (WDTimer) using the JIDA32 Library API (Refer to Appendix: JIDA Standard), or through the BIOS setup, or directly through register settings. The application software should strobe the WDTrigger to prevent a timeout. The WDTrigger resets and restarts the system after a timeout to provide a way to recover from program crashes or lockups.

The Watchdog can be enabled through:

» BIOS Setup (with BIOS NOW1R113 or newer)

» JIDA32 or K-Station

» Direct programming over register settings

The Watchdog can be triggered through

» JIDA32 or K-Station

» Direct programming (i.e., writing data into one register of the CPLD)

For information about programming this feature, see the JIDA32/K-Station driver packet in the Kontron Customer section or contact your local sales support representative to get an application note about low level programming.

5.5 General Purpose Input and Output (GPIO)

The COMe-cXLi2 COM provides eight GPIOs that can be accessed through the module connector described in the Pin-out Lists, Section 0. The GPIO interface is shared with SDIO signals and can be enabled in BIOS setup for either GPIO or SDIO.

Note: GPIO cannot drive applications faster than 2msec. Data transfer rates up to 1 kHz maximum are recommended.

Table 13: GPIO COM Express Pin-Outs

Bit of GPIO Port0	Function	COM Express Pin
0	GPI0	A54

1	GPI1	A63
2	GPI2	A67
3	GPI3	A85
4	GPO0	A93
5	GPO1	B54
6	GPO2	B57
7	GPO3	B63

5.6 Fast I²C

The COMe-cXLi2 COM integrates two configurable I²C buses. The external I²C provided via the US15WPT SCH GPIOs on COM Express® connector pin B33/B34 and the JILI (LVDS) I²C from US15WPT SCH is available on COM Express® connector pin A83/A84. The I²C interface offers full multimaster and clock stretching support.

Table 14: JIDA/external I²C speed

Setup	ATOM™ Z520	
Extra high	not supported	
Very high	150 kHz	
High	80 kHz	
Medium	40 kHz	60 kHz
Slow	11 kHz	16 kHz
Very slow	1.5 kHz	2 kHz
Ultra slow	0.8 kHz	1 kHz

JILI I²C Speed

Setup	ATOM™ Z520	
Extra high	not supported	
Very high	90 kHz	
High	36 kHz	
Medium	18 kHz	
Slow	2.8 kHz	
Very slow	1.0 kHz	
Ultra slow	not supported	

5.7 ACPI Suspend Modes and Resume Events

The COMe-cXLi2 COM only supports the S3 state (=Save to RAM). S4 (=Save to Disk) is not supported by the BIOS (S4_BIOS) but S4_OS is supported by the following operating systems:

» Windows XP

» Windows Vista

» Windows 7

Events that Resume the System from S3

» USB keyboard (1)

» USB mouse (1)

» Power button

» WakeOnLan (2)

Events that Resume the System from S4/S5

» Power button

» WakeOnLan

NOTES: 1) The OS must support wake-up via USB devices and the baseboard must power the USB port with StandBy-Voltage
2) WakeOnLan must be enabled in the driver options

6 Design Consideration

6.1 Thermal Management

A heat-spreader plate (36006-0000-99-0) assembly is available from Kontron Embedded Modules for the COMe-cXLi2 COM. The heat-spreader plate on top of this assembly is NOT a heat sink. It works as a COM Express®-standard thermal interface to be used with a heat sink or other cooling device.

External cooling must be provided to maintain the heat-spreader plate at proper operating temperatures. Under worst-case conditions, the cooling mechanism must maintain an ambient air and heat-spreader plate temperature of 85° C or less.

The aluminum slugs and thermal pads on the underside of the heat-spreader assembly implement thermal interfaces between the heat-spreader plate and the major heat-generating components on the COMe-cXLi2. About 80 percent of the power dissipated within the module is conducted to the heat-spreader plate and can be removed by the cooling solution.

Kontron also has defined a passive heatsink (36006-0000-99-0C01) that can be used in place of the heat spreader plate to provide additional cooling. You can use many thermal-management solutions with the heat-spreader plates, including active and passive approaches. The optimum cooling solution varies, depending on the COM Express® application and environmental conditions and the module is fully functional at the full -40C to +85C temperature even without the heat spreader plate or the passive heatsink. Drawings for both the heat spreader plate and the passive heatsink are available on request. Also, see the *PICMG COM Express® Design Guide* on the PICMG website for further information about thermal management.

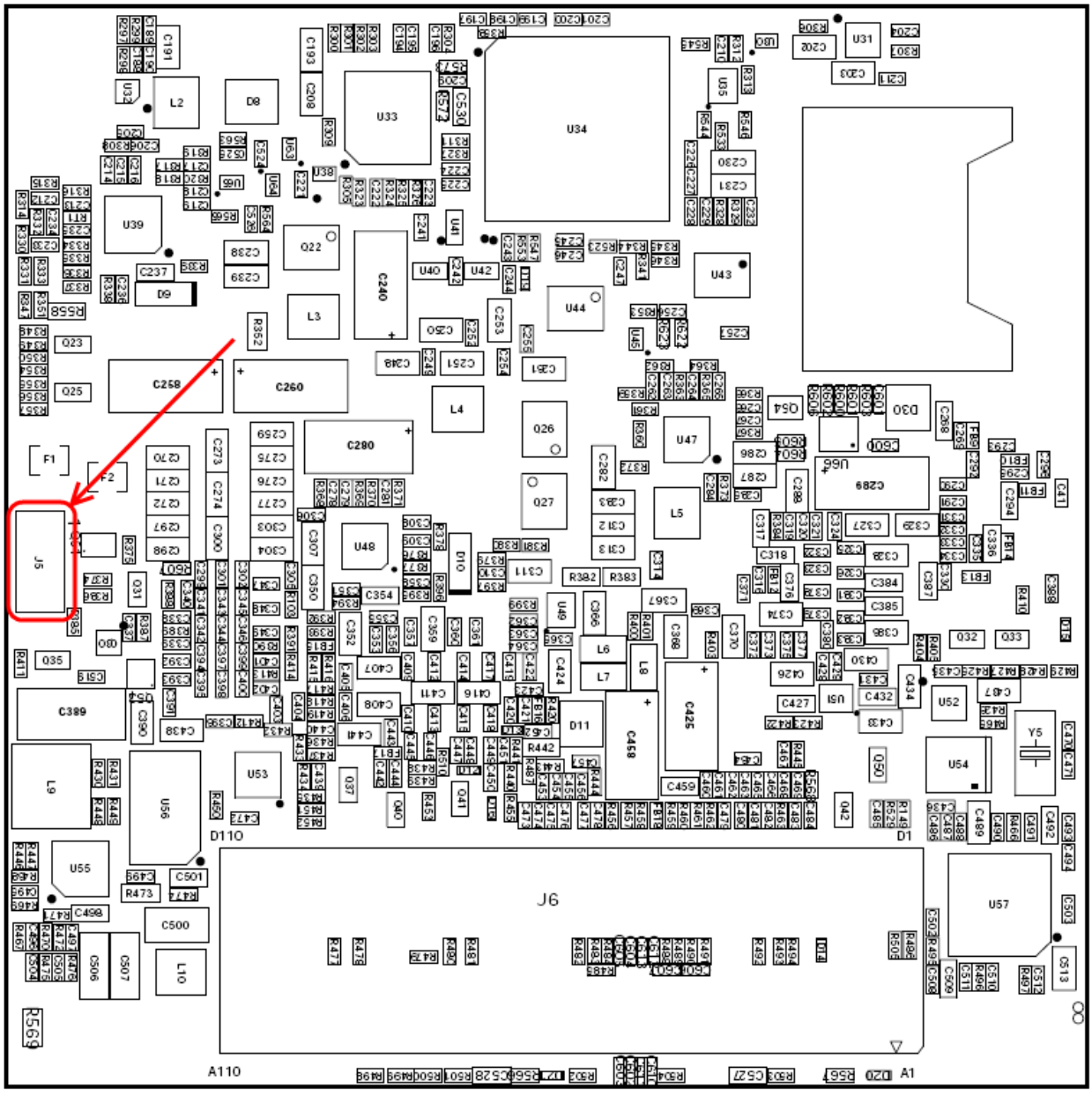
6.2 Heat-Spreader Dimensions

Documentation for the COMe-cXLi2 COM cooling solutions is provided at http://emdcustomersection.kontron.com.

6.3 Onboard Fan Connector

This section describes how to connect an optional fan to the connector located directly on the COMe-cXLi2 COM. With certain BIOS-settings it is possible to control the fan depending on the active trip point temperature. The fan switches on/off depending on the adjusted Active Trip Point temperature. In order for this feature to function properly an ACPI compliant OS is necessary.

Figure 9: Fan Connector Location and Pin-Out

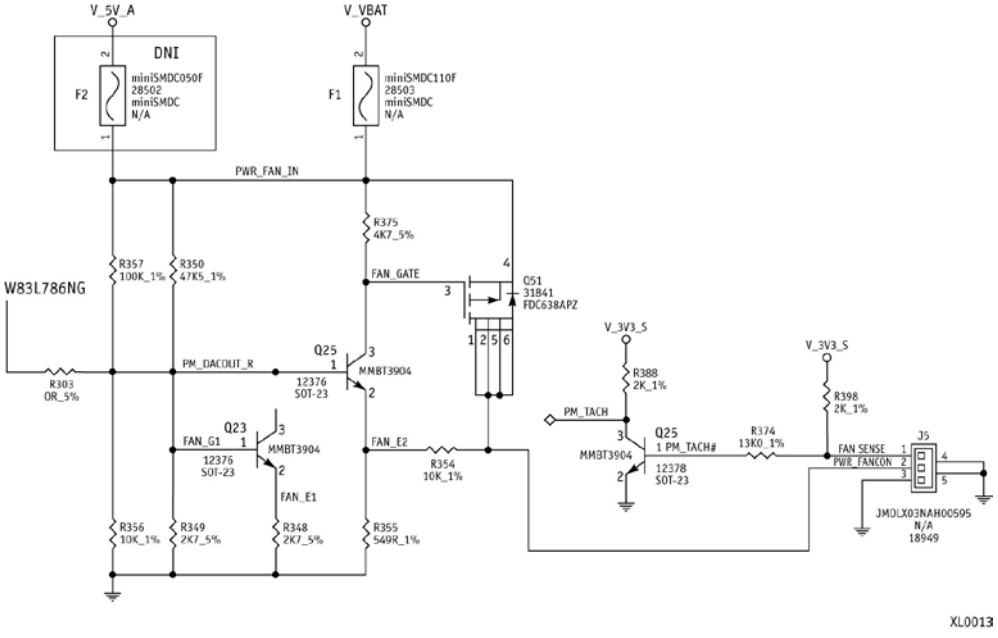


The onboard fan connector (J3) is on the left bottom side of the PCB. The connection details are covered in the Figure 10 schematic.

Table 15. Fan Connector (J3) Pin-Out

Pin	Description
1	Sense
2	Power (12V)
3	GND

Figure 10: Fan Connector Schematic



Connector J3 specifications and Kontron part numbers for the components are:

» Part number: (Molex) J8: 53261-0371

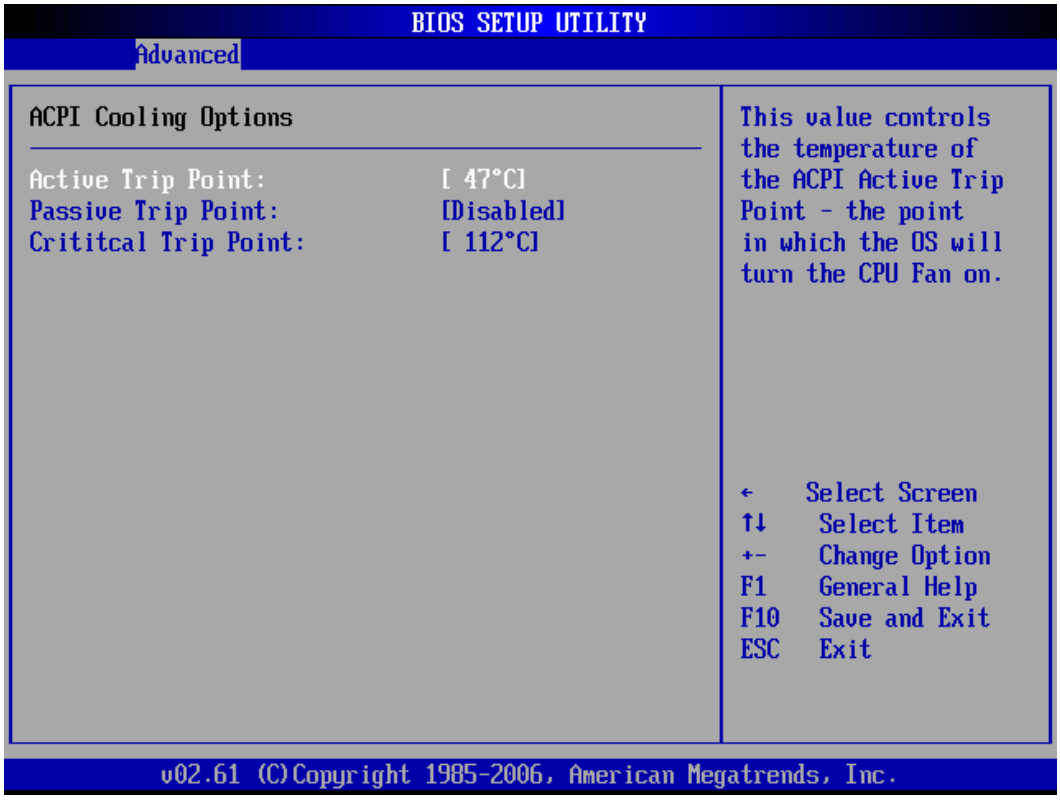
» Mates with: 51021-0300

» Crimp terminals: 50079-8100

6.3.1BIOS Settings for Fan Control

In the BIOS setup you can specify the active cooling trip point. Use Advanced Settings - > ACPI Settings -> ACPI Cooling Options in the BIOS setup utility to do this. For more information, see Chapter 8.3, "BIOS Setup".

Figure 11: Fan Control BIOS Settings



The active cooling trip point is the ACPI temperature that triggers switching the fan on or off.

6.3.2Fan Connector Electrical Characteristics

» VCC in FANCON: VCC of board, limited to 12V max

» Imax: 0.40 A

NOTE: The VCC_in_FANCON output is not short circuit proof. You may need to ensure that the circuit is protected externally by a fuse on the backplane, for example.

7 System Resources

7.1 Interrupt Request (IRQ) Lines

Table 16: 8259 PIC Mode

IRQ #	Used For	Available	Comment
0	Timer0	No	
1	Keyboard	No	
2	Cascade	No	
3	External SIO - COM2	Yes (No)	Note (1)
4	External SIO - COM1	Yes (No)	Note (1)
5	PCI	for PCI	Dynamic (BIOS default)
6	External SIO	Yes (No)	Note (1)
7	External SIO - LPT1	Yes (No)	Note (1)
8	RTC	No	
9	ACPI	No	Note (2)
10	PCI	for PCI	Dynamic (BIOS default)
11	PCI	for PCI	Dynamic (BIOS default)
12	PS/2 Mouse	Yes (No)	Note (1)
13	FPU	No	
14	Primary IDE	No	Note (1)
15	PCI	for PCI	Dynamic (BIOS default)

NOTES: 1) If the "Used For" device is disabled in setup, the interrupt is available for other devices.
2) Not available if ACPI is used

Table 17: APIC Mode

IRQ #	Used For	Available	Comment
0	Timer0	No	
1	Keyboard	No	
2	Cascade	No	
3	External SIO - COM2	Yes (No)	Note (1)
4	External SIO - COM1	Yes (No)	Note (1)
5	PCI	for PCI	Dynamic (BIOS default)
6	External SIO	Yes (No)	Note (1)
7	External SIO - LPT1	Yes (No)	Note (1)
8	RTC	No	
9	ACPI	No	Note (2)
10	PCI	for PCI	Dynamic (BIOS default)
11	PCI	for PCI	Dynamic (BIOS default)
12	PS/2 Mouse	Yes (No)	Note (1)
13	FPU	No	
14	Primary IDE	No	Note (1)
15	PCI	for PCI	Dynamic (BIOS default)
16	PIRQ [A]	No	PCI IRQ line 1 + US15W graphics + SDcard + PCIe- Switch + HDAudio + SATA Bridge + USB client (if enabled) (3)
17	PIRQ [B]	No	PCI IRQ line 2 + SDcard + PCIe- Switch, Note (3)
18	PIRQ [C]	No	PCI IRQ line 3 + LAN Controller + PCIe- Switch, Note (3)
19	PIRQ [D]	No	PCI IRQ line 4 + PCIe- Switch + PCIe2PCI-Bridge, Note (3)
20	PIRQ [E]	No	USB UHCI Controller #1, Note (3)
21	PIRQ [F]	No	USB UHCI Controller #2, Note (3)
22	PIRQ [G]	No	USB UHCI Controller #3, Note (3)
23	PIRQ [H]	No	USB UHCI Controller #4, Note (3)

NOTES: 1) If the "Used For" device is disabled in setup, the interrupt is available for other devices.
2) Not available if ACPI is used
3) ACPI OS decides on the particular IRQ usage

7.2 Memory Area

The first 640 KBytes of DRAM are used as main memory. With DOS, you can address 1 MB of memory directly. Memory area above 1 MB (high memory, extended memory) is accessed under DOS via special drivers such as HIMEM.SYS and EMM386.EXE, which are part of the operating system. Please refer to the operating system documentation or special textbooks for information about HIMEM.SYS and EMM386.EXE.

Other operating systems (Linux or Windows versions) allow you to address the full memory area directly.

Upper Memory	Used for	Available	Comment
A0000h – BFFFFh	VGA Memory	No	Mainly used by graphic controller
C0000h – CFFFFh	VGA BIOS	No	Used by onboard VGA ROM
D0000h – DFFFFh		Yes	Free for shadow RAM in standard configurations.
E0000h – FFFFFh	System BIOS	No	Fixed

7.3 I/O Address Map

The I/O-port addresses of the COMe-cXLi2 COM are functionally identical to those of a standard PC/AT system. All addresses not mentioned in Table 1 should be available. We recommend that you do not use I/O addresses below 0100h for additional hardware for compatibility reasons, even if available.

Table 18: I/O Address Assignments

I/O Address	Used for	Available	Comment
0000 - 001F	System Resources	No	Fixed
0020 - 003F	Interrupt Controller 1	No	Fixed
002E - 002F	WB 83627	No	Fixed if WB83627HG is in system
0040 - 005F	Timer, Counter	No	Fixed
004E - 004F	TPM	No	Fixed if TPM is in system
0060 - 006F	Keyboard Controller	No	Fixed
0070 - 007F	RTC and CMOS Registers	No	Fixed
0080	BIOS Postcode	No	Fixed

I/O Address	Used for	Available	Comment
0081 - 008F	DMA Page Register	No	Fixed
00A0 - 00BF	Interrupt Controller 2	No	Fixed
00C0 - 00DF	DMA Controller 2	No	Fixed
00E0 - 00EF	System Control	No	Fixed
00F0 - 00FF	Math Coprocessor	No	Fixed
0170 – 0177 0376	Fixed Disk	No	Available if IDE port 1 is disabled
01F0 - 01F7 03F6	Fixed Disk	No	Available if IDE port 1 is disabled
0290-0295	WB83627 HWM	No	Fixed if WB83627HG is in system
03B0 - 03DF	VGA	No	Fixed
0400 - 043F	SMBus	No	Fixed
0480 - 04BF	GPIO	No	Fixed
04D0 - 04D1	PIC Extension	No	Fixed
0900 - 091F	Power Management	No	Fixed
09C0 - 09FF	GPE	No	Fixed
0A05 – 0A06	WB83627HG Hardware Monitor	No	Fixed if WB83627HG is in system
0A80 – 0A81	CPLD	No	in Future versions
C000 - CFFF	PCIe-to-PCI Bridge	No	Dynamic (BIOS default address)
0CF8 - 0CFF	PCI Configuration	No	Fixed
D000 - DFFF	PCIe-to-PCI bridge	No	Dynamic (BIOS default address)
D880 - D88F	SATA Controller	No	Dynamic (BIOS default address)
E080 - E09F	PCI USB Controller	No	Dynamic (BIOS default address)
E480 - E49F	PCI USB Controller	No	Dynamic (BIOS default address)
E880 - E887	VGA	No	Dynamic (BIOS default address)
EF00 - EF1F	PCI USB Controller	No	Dynamic (BIOS default address)
FFA0 - FFAF	PCI IDE Controller	No	Dynamic (BIOS default address)

7.4 Peripheral Component Interconnect (PCI) Devices

All devices follow the Peripheral Component Interconnect 2.3 (PCI 2.3) and the PCI Express Base 1.0a specifications. The BIOS and OS control memory and I/O resources. Please see the PCI 2.3 specification for details.

Table 19: PCI Device IRQs

PCI Device	PCI IRQ	Interface	Comment
Host Bridge / Memory Controller	None		Integrated in chipset
Graphics / Video Controller	INTA		Integrated in chipset
USB Client Controller	INTA		Integrated in chipset
HD Audio Controller	INTA		Integrated in chipset
PCI Express Port (Bridge)	INTA		Integrated in chipset
PCI Express Port (Bridge)	INTB		Integrated in chipset
UHCI USB Controller 1	INTE		Integrated in chipset
UHCI USB Controller 2	INTF		Integrated in chipset
UHCI USB Controller 3	INTG		Integrated in chipset
EHCI USB Controller	INTH		Integrated in chipset
SDIO/MMC Controller 1	INTA		Integrated in chipset
SDIO/MMC Controller 2	INTB		Integrated in chipset
ISA Bridge / LPC Controller	None		Integrated in chipset
IDE Controller	None		Integrated in chipset
Network Controller SATA	INTC INTA	PCI Express PCI Express	External i82574 External SIL3132

Table 20: External I^2C Bus #1

I^2C Address	Used For	Available	Comment	JIDA Bus Nr.
A0h	JIDA-EEPROM	No	EEPROM for	0

			CMOS Data	
A2h	JIDA-EEPROM	No	EEPROM for CMOS Data	0

Table 21: External I²C Bus #2

I²C Address	Used For	Available	Comment	JIDA Bus Nr.
B0h	Watchdog	NO	external WD PIC	2

Table 22: JILI I²C Bus

I²C Address	Used For	Available	Comment	JIDA Bus Nr.
A0h	JILI-EEPROM	No	EEPROM for JILI Data	4

7.5 System Management Bus (SMBus)

Table 23: SMBus Address Assignments

Address	Device	Notes	JIDA Bus Nr.
12h	SMART_CHARGER	Not to be used with any SMBus device except a charger	1
14h	SMART_SELECTOR	Not to be used with any SMBus device except a selector	1
16h	SMART_BATTERY	Not to be used with any SMBus device except a battery	1
5Ch	Winbond W83L786NG HWM	Do not use under an circumstances	1
A0h	SPD EEPROM on DDR2 memory	Do not use under an circumstances	1
D2h / DCh	Clock Gen CK610/ICS9DB403	Do not use under an circumstances	1
E6h	PCA9538 Digital I/O (GPIO)	Do not use under an circumstances	1

7.6 K-Station / JIDA32 Resources

Table 24: I²C

BUS	Function
I2C 0	Internal / JIDA I2C #1
I2C 1	SM-Bus
I2C 2	Internal / JIDA I2C #2 (for slow devices)
I2C 3	SDVO I2C
I2C 4	JILI I2C

Table 25: Storage

Device	Function
EEPROM 0	JIDA EEPROM Area1 with 32 Bytes (free to use)
EEPROM 1	JIDA EEPROM Area 2 with 33 Bytes (reserved)

Table 26: GPIO

Port	Function
IO-Port 0	GPIO Port, Bit 0-3: Input, Bit 4-7: Output

Table 27: Hardware Monitor

Sensor	Function
Temp 0	CPU ACPI Temperature (measured with Winbond W839786 HWM)
Temp 1	Module Temperature (internal IC temperature of onboard Winbond W839786 HWM)
FAN 0	Module CPU fan sensor (measured with Winbond W839786 HWM)
Voltage 0	Winbond 839786 Voltage Sensor 0: CoreA
Voltage 1	Winbond 839786 Voltage Sensor 1: VRAM
Voltage 2	Winbond 839786 Voltage Sensor 2: +3.3V

8 BIOS Operation

8.1 The COMe-cXLi2 COM has AMI® BIOS installed on the onboard8-Mbit firmware hub. Determining the BIOS Version

To determine the AMI® BIOS version, press the Pause key on your keyboard immediately, as soon as you see the following text display in the upper left corner of your screen:

» AMIBIOS © 2006 American Megatrends, Inc.

» BIOS Date: 06/16/08 10:52:49 Ver: 08.00.14

» Kontron® BIOS Version < UXP1RXXX>

» © Copyright 2002-2008 Kontron

8.2 Setup Guide

The AMIBIOS Setup Utility changes system behavior by modifying the BIOS configuration. The setup program uses a number of menus to make changes and turn features on or off.

Note: Selecting incorrect values may cause system boot failure. Load setup default values to recover by pressing <F9>.

8.2.1Start AMI® BIOS Setup Utility

To start the AMI® BIOS setup utility, press <DEL> when the following string appears during boot-up:

Press <DEL> to enter Setup

The Info menu then appears.

The Setup Screen has several sections:

Setup Screen	Location	Function
Menu Bar	Top	Lists and selects all top level menus.
Legend Bar	Right side Bottom	Lists setup navigation keys.
Item Specific Help Window	Right side Top	Help for selected item.
Menu Window	Left Center	Selection fields for current menu.

Menu Bar

The menu bar at the top of the window lists different menus. Use the ← or → key to make a selection.

Legend Bar

Use the keys listed on the bottom of the legend bar to make your selections or exit the current menu. The table below describes the legend keys and their alternates.

Key	Function
<F1> or <Alt-H>	General Help window.
<Esc>	Exit menu.
← or → Arrow key	Select a menu.
↑ or ↓ Arrow key	Select fields in current menu.
<Home> or <End>	Move cursor to top or bottom of current window.
<PgUp> or <PgDn>	Move cursor to next or previous page.
<F9>	Load the default configuration values for this menu.
<F10>	Save and exit.
<Enter>	Execute command or select submenu.
<Alt-R>	Refresh screen.

Selecting an Item

Use the ↑ or ↓ key to move the cursor to the field you want. Then use the + and – keys to select a value for that field. The Save Value commands in the Exit menu save the values displayed in all the menus.

Displaying Submenus

Use the ← or → key to move the cursor to the submenu you want and then press <Enter>. A pointer (▸) marks all submenus.

Item Specific Help Window

The Help window on the right side of each menu displays the Help text for the selected item. It updates as you move the cursor through each field.

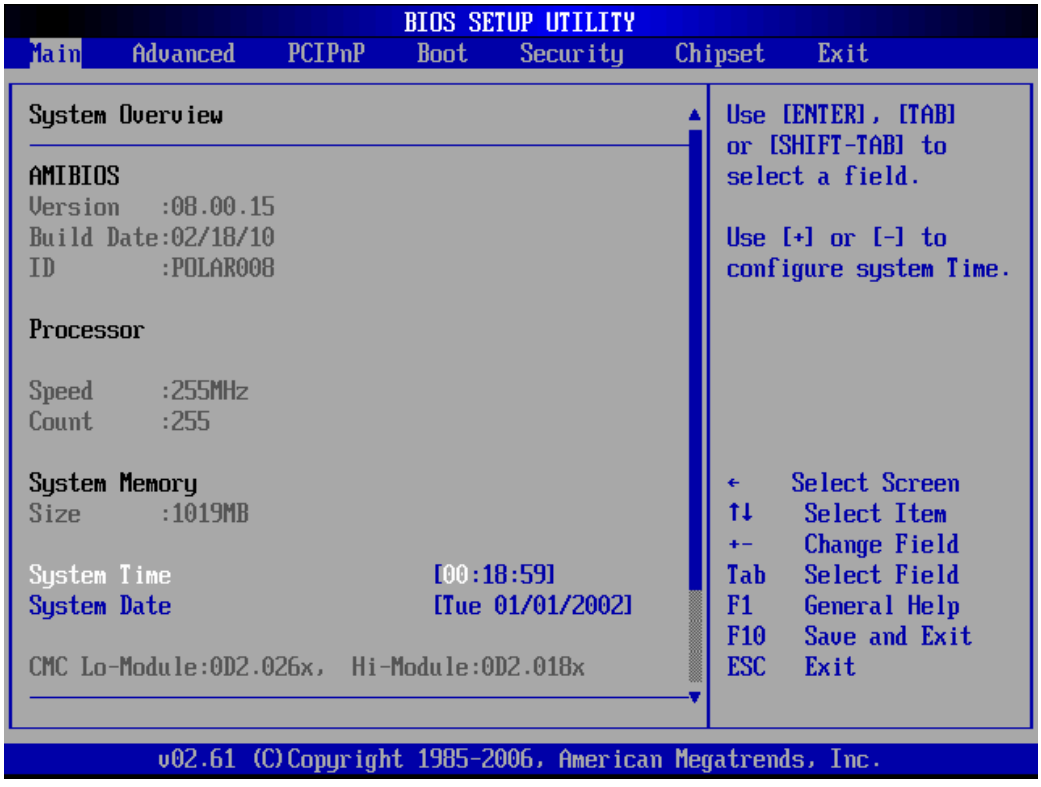
General Help Window

Pressing <F1> or <Alt-F1> on a menu brings up the General Help window that describes the legend keys and their alternates. Press <Esc> to exit the General Help window.

8.3 BIOS Setup

NOTE:	Default Settings are in bold

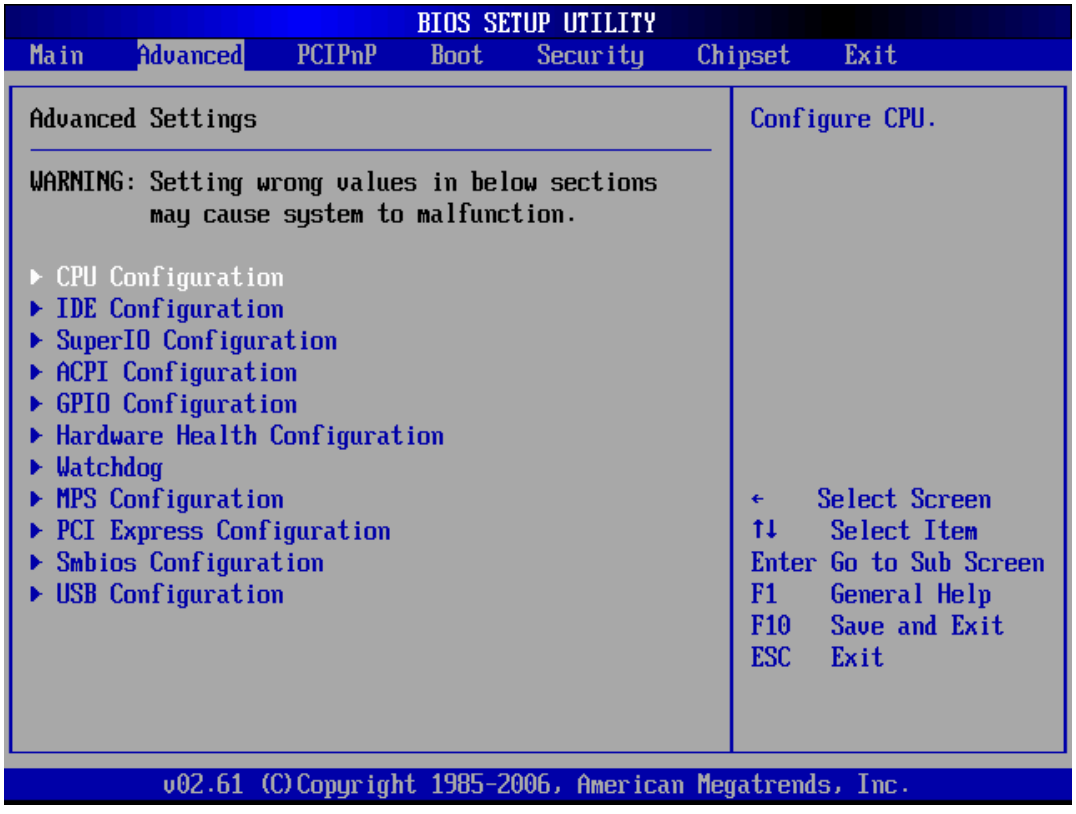
8.3.1Main Menu



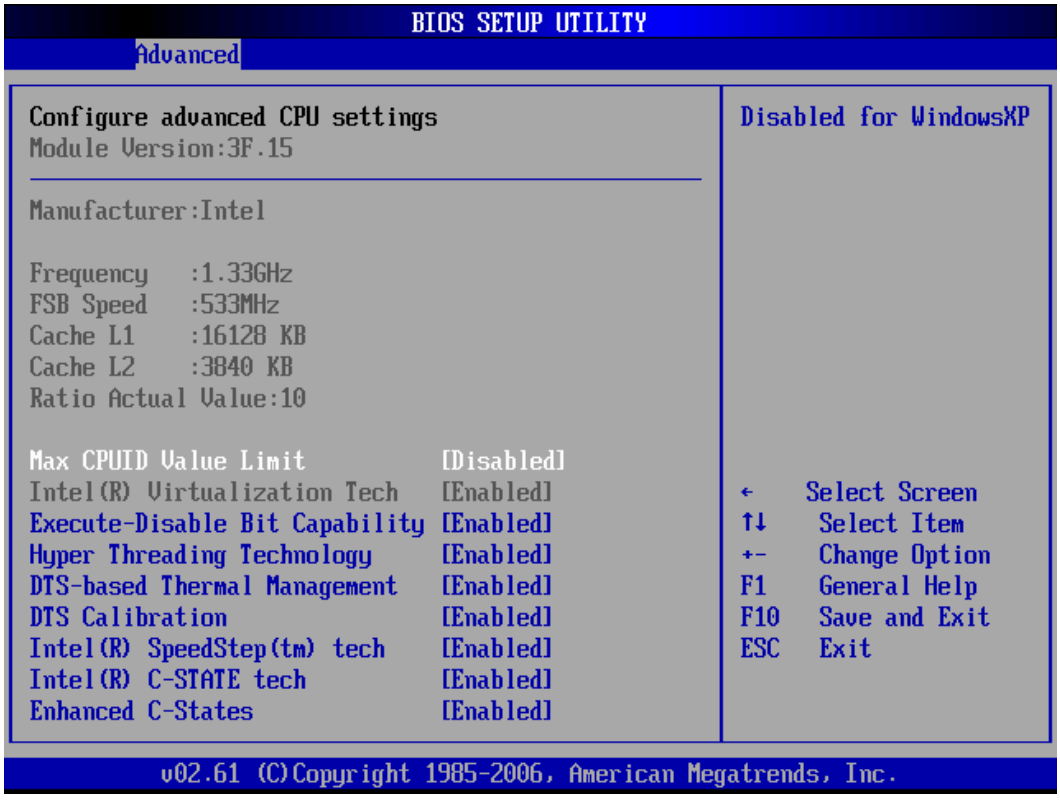
Note: The screen shot provided above shows the preliminary BIOS ID (POLAR008). The production BIOS ID is UXP1Rxxx.

Feature	Option	Description
System Time	[hh:mm:ss]	<Tab>, <Shift-Tab>, or <Enter> selects field
System Date	[mm-dd-yyyy]	<Tab>, <Shift-Tab>, or <Enter> selects field

8.3.2Advanced Settings Menu



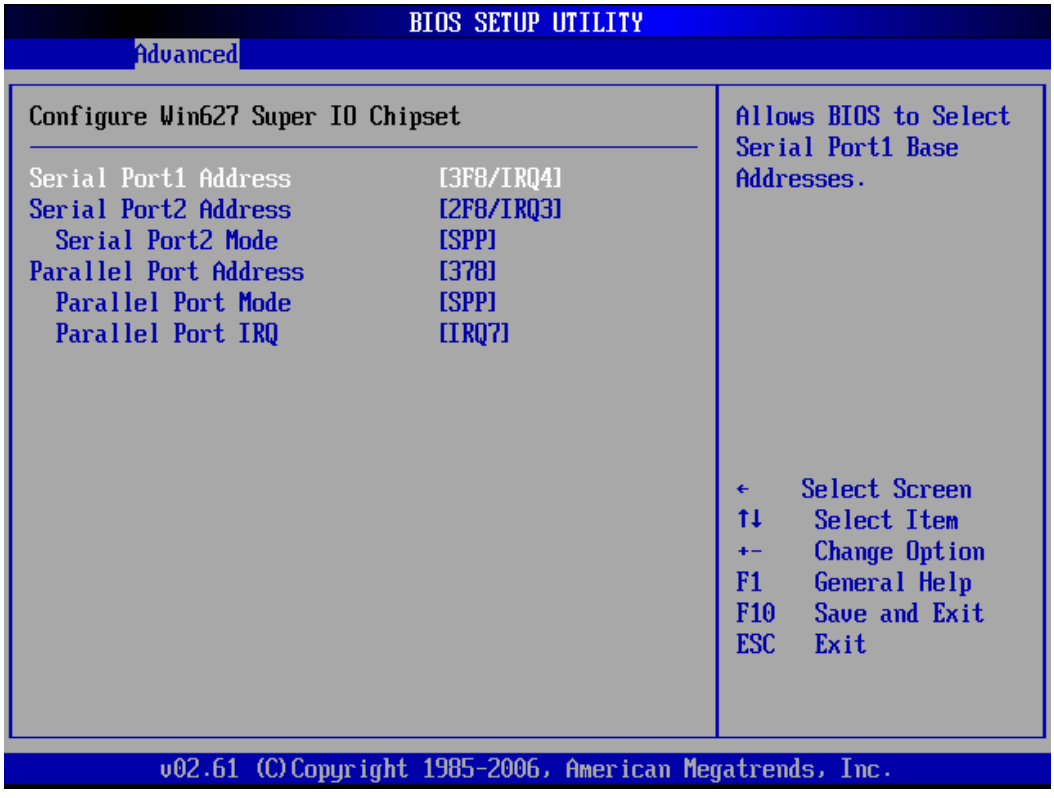
Advanced CPU Settings Configuration



Feature	Option	Description
Max CPUID Value Limit	**Disabled** Enabled	Disabled for WindowsXP
CPU TM Functionality	**Disabled** Enabled	Enables or disables both TM1 and TM2 simultaneously.
CPU Performance	Low Middle **High**	Sets the CPU ratio for Z510 / Z530 CPU Low: 600MHz / 800MHz Middle: 800MHz / 1200MHz High: 1100MHz / 1600MHz Note: Speedstep is disabled if CPU P-State is fixed to low or middle
Execute-Disable Bit Capability	**Enabled** Disabled	When disabled, force the XD feature flag to always return 0
Hyper Threading Technology	**Enabled** Disabled	Enables or Disables Intel® Hyper Threading Technology
Intel® SpeedStep™	**Enabled** Disabled	Enables and Disables the SpeedStep power management feature
Intel® C-State tech	**Enabled** Disabled	Enables and Disables the C - States. If enabled, the CPU is set to C2 - C6 state in idle mode

Feature	Option	Description
Enhanced C-STATE	**Enabled** Disabled	CPU idle is set to enhanced C-states

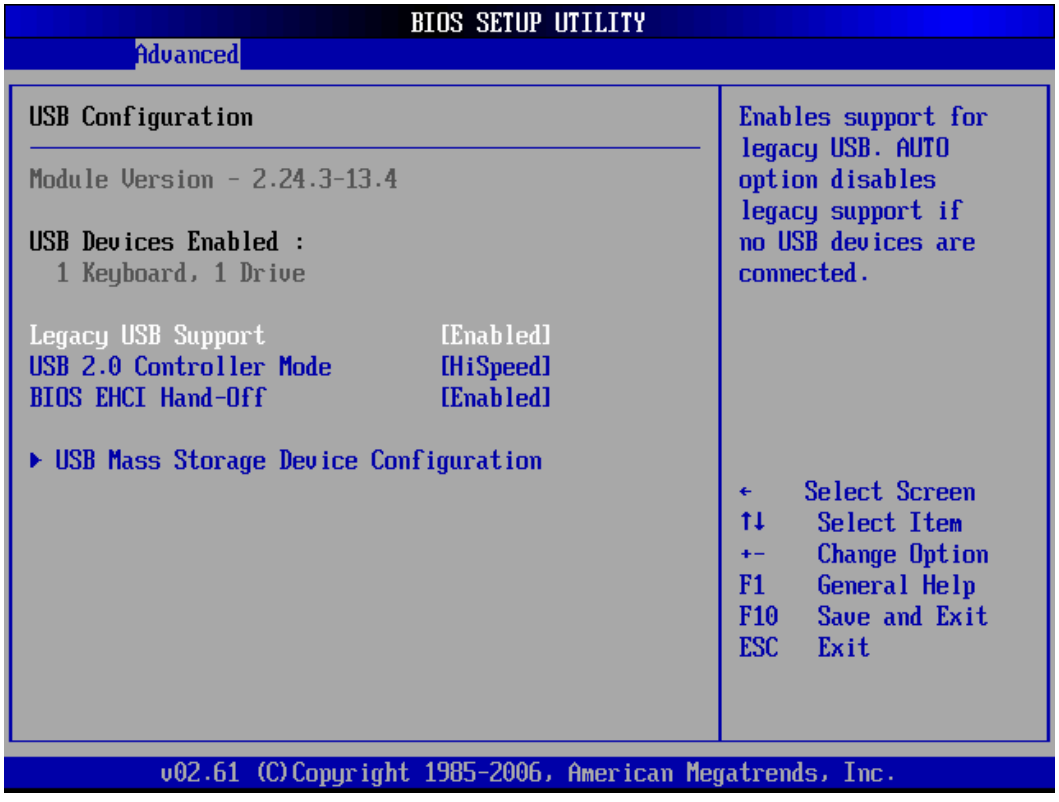
Legacy Devices – LPC I/O Configuration



Feature	Option	Description
Serial Port1 Address	Disabled **3F8/IRQ4** 3E8/IRQ4 2E8/IRQ3	Selects the serial Port 1 base address
Serial Port2 Address	Disabled **2F8/IRQ3** 3E8/IRQ4 2E8/IRQ3	Selects the serial Port 2 base address
Serial Port2 Mode	**Normal** IrDA ASK IR	Selects the mode for serial Port2
Parallel Port Address	Disabled **378** 278 3BC	Selects the parallel Port base address
Parallel Port	**Normal**	Selects the parallel Port mode

Feature	Option	Description
Mode	Bi-Directional ECP EPP ECP & EPP	
Parallel Port IRQ	IRQ5 **IRQ7**	Selects the parallel Port IRQ

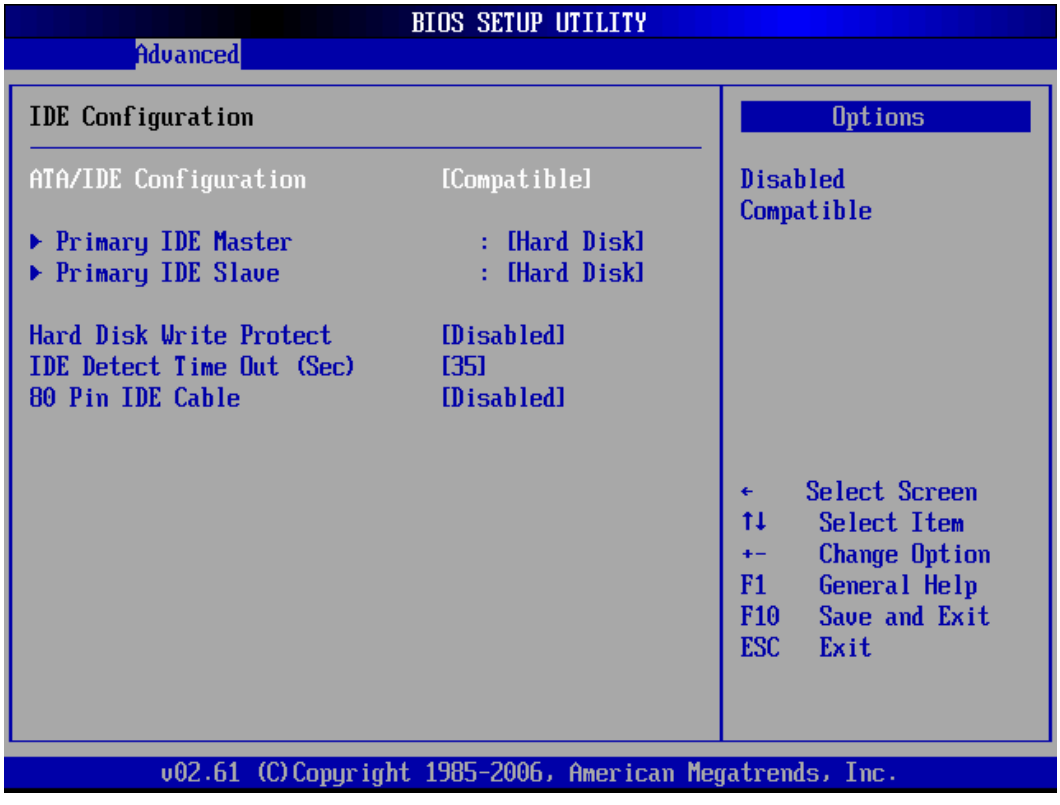
Devices Configuration - USB Configuration



Feature	Option	Description
USB Functions	Disabled 2 Ports 4 Ports **6 Ports**	Defines the number of USB UHCI ports (USB 1.1). EHCI ONLY is automatically added
USB 2.0 Controller	**Enabled** Disabled	Controls EHCI (USB 2.0) functionality for all the UHCI ports set to active state
USB Client Controller	Enabled **Disabled**	This enables the USB client functionality on COM Express USB Port #7
Legacy USB Support	Disabled **Enabled**	Enables support for legacy USB. AUTO option disables legacy

Feature	Option	Description
	Auto	support if no USB devices are connected
USB Keyboard Legacy Support	**Enabled** Disabled	Enables legacy support for USB keyboard
USB Mouse Legacy Support	**Enabled** Disabled	Enables legacy support for USB mouse
USB Storage Device Support	**Enabled** Disabled	Enables support for USB mass storage devices
USB 2.0 Controller Mode	FullSpeed **HiSpeed**	Configures the USB 2.0 controller in HiSpeed (480Mbps) or FullSpeed (12Mbps)
BIOS EHCI Hand-Off	Disabled **Enabled**	This is a workaround for an OS without EHCI hand-off support. The EHCI ownership change should claim by the EHCI driver

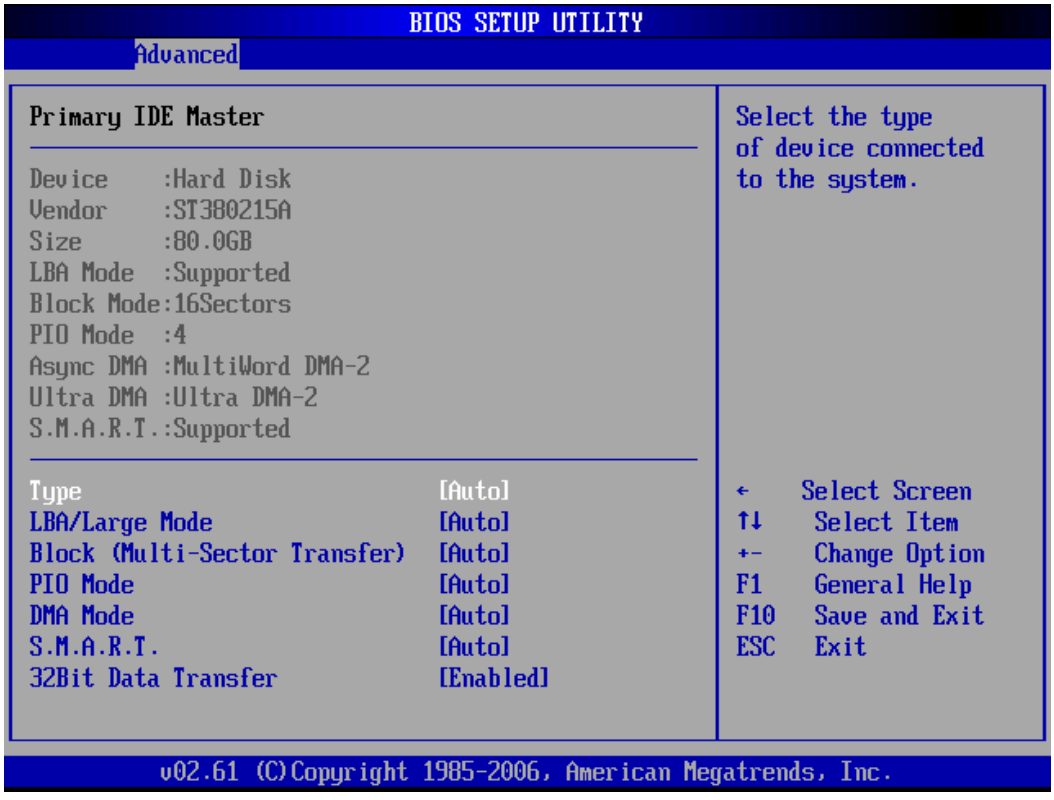
Devices Configuration - IDE Configuration



Feature	Option	Description
ATA/IDE Configuration	Disabled **Enabled**	Enables or disables the IDE interface of US15W SCH.
▸ Primary IDE Master	Submenu	While entering setup, BIOS auto detects the presence of IDE

Feature	Option	Description
		devices. This displays the status of auto-detection of IDE Devices
▸Primary IDE Slave	Submenu	While entering setup, BIOS auto detects the presence of IDE devices. This displays the status of auto-detection of IDE Devices
Hard Disk Write Protect	**Disabled** Enabled	Allows the write protection of Hard Disk devices. Only valid if the device is accessed through the BIOS
IDE Detect Time Out (Sec.)	0, 5, 10, 15 20, 25, 30, 35	Selects the time out value for the detection of ATA/ ATAPI devices

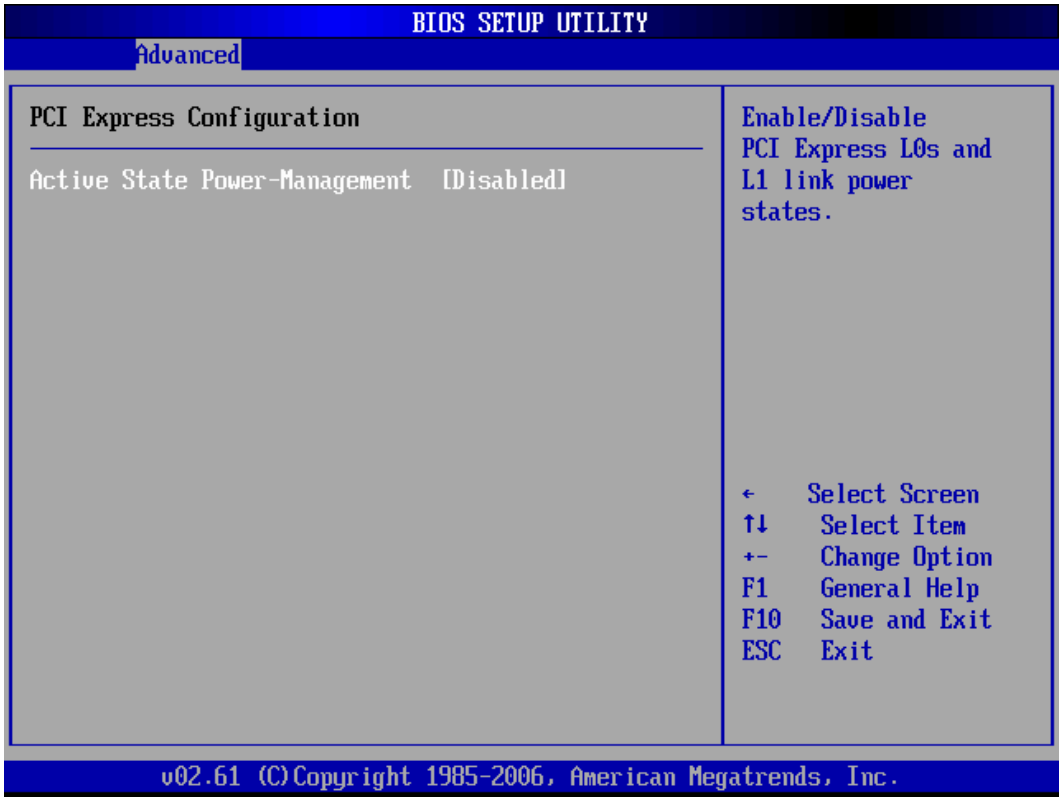
Devices Configuration - IDE Configuration - IDE Master/Slave Submenu



Feature	Option	Description
Type	Not Installed **Auto** CD/DVD ARMD	Selects the type of the IDE Devices connected to the system

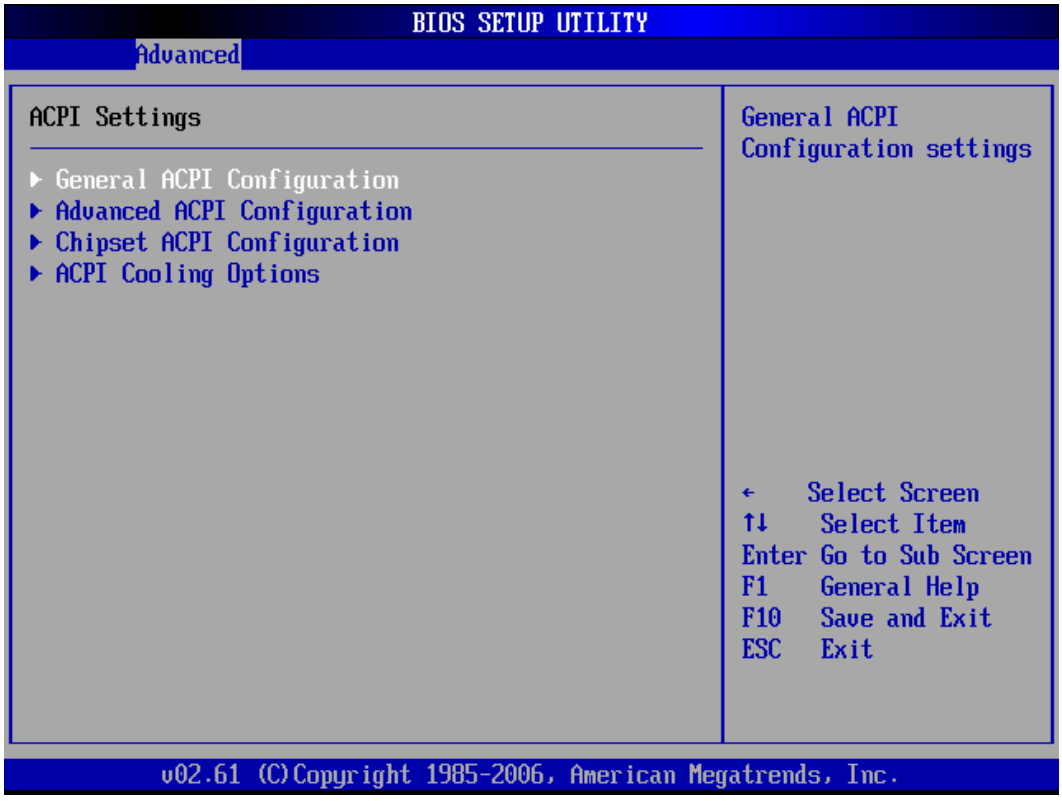
Feature	Option	Description
LBA/Large Mode	Disabled **Auto**	Disables the LBA mode or enables it, when a device supports it
Block (Multi-Sector Transfer)	Disabled **Auto**	Disabled: The data transfer from and to the device occurs one sector at a time Auto: The data transfer from and to the device occurs multiple sectors at a time if the device supports it
PIO Mode	**Auto** 0 1 2 3 4	(Auto) Configures the PIO Mode
DMA Mode	**Auto** SWDMAn MWDMAn UDMAn	SWDMA: Single Word DMA MWDMA: Multi Word DMA UDMA: Ultra DMA
S.M.A.R.T.	**Auto** Enabled Disabled	Disables, Enables or automatically enables the S.M.A.R.T feature (Self-Monitoring, Analysis and Reporting Technology)
32Bit Data Transfer	**Enabled** Disabled	Disables and Enables the 32Bit Data Transfer Mode

Devices Configuration - PCI Express Configuration



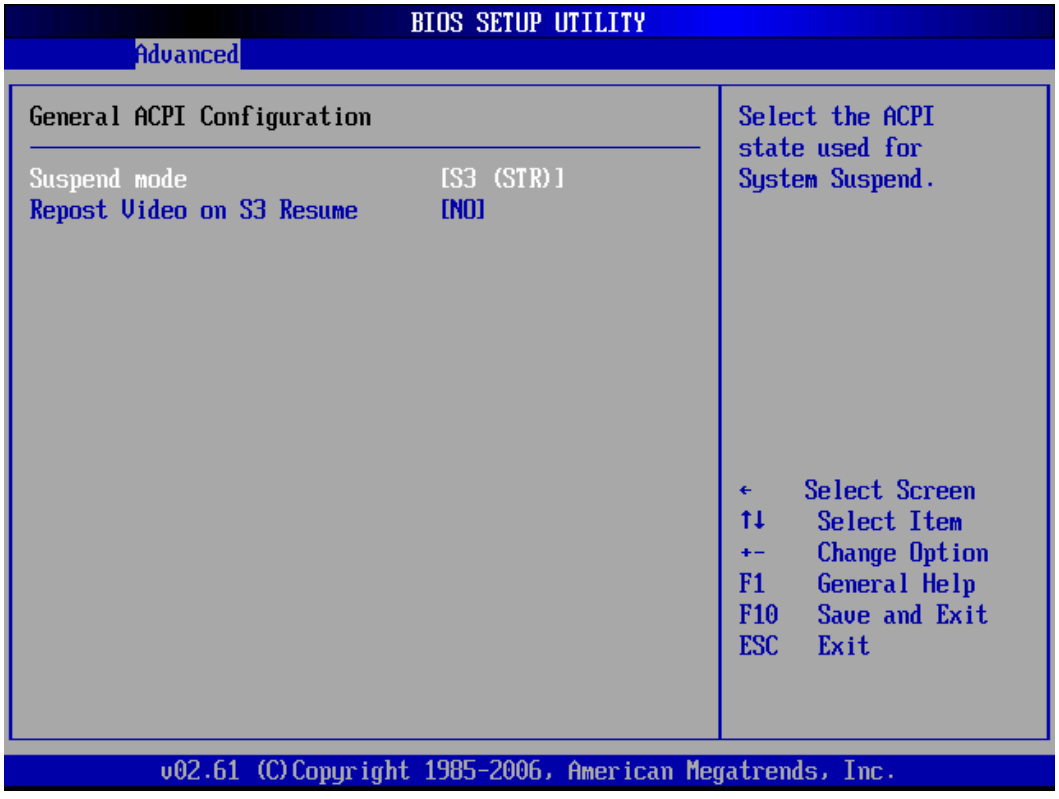
Feature	Option	Description
PCIe Port 0	**Auto** Enabled Disabled	Enables or disables PCIe Port 0 Note: This Port is used for onboard PCIe Switch
PCIe Port 1	**Auto** Enabled Disabled	Enables or disables PCIe Port 1
Active State Power-Management	Enabled **Disabled**	Enable/Disable PCI Express L0s and L1 link power states

ACPI Configuration



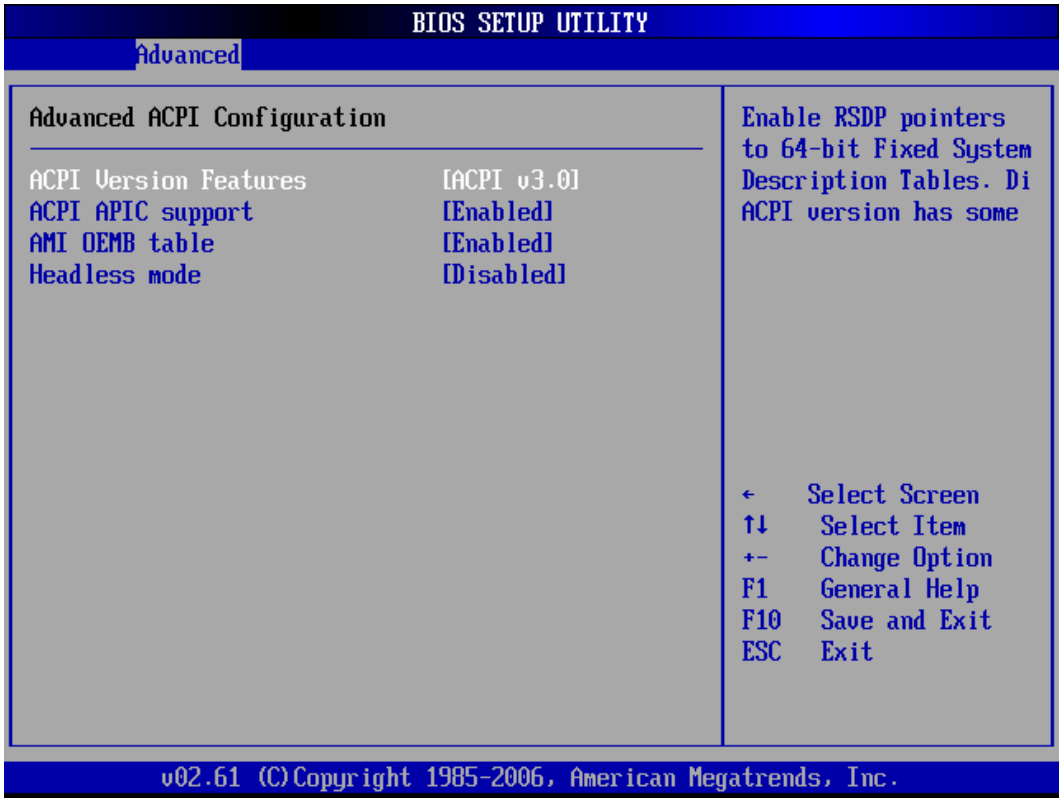
Feature	Option	Description
▸General ACPI Configuration	Submenu	
▸Advanced ACPI Configuration	Submenu	
▸Chipset ACPI Configuration	Submenu	
▸ACPI Cooling Options	Submenu	

ACPI Configuration - General ACPI Configuration



Feature	Option	Description
Repost Video on S3 Resume	**No** Yes	Determines whether to invoke VGA BIOS post on S3/STR resume

ACPI Configuration - Advanced ACPI Configuration



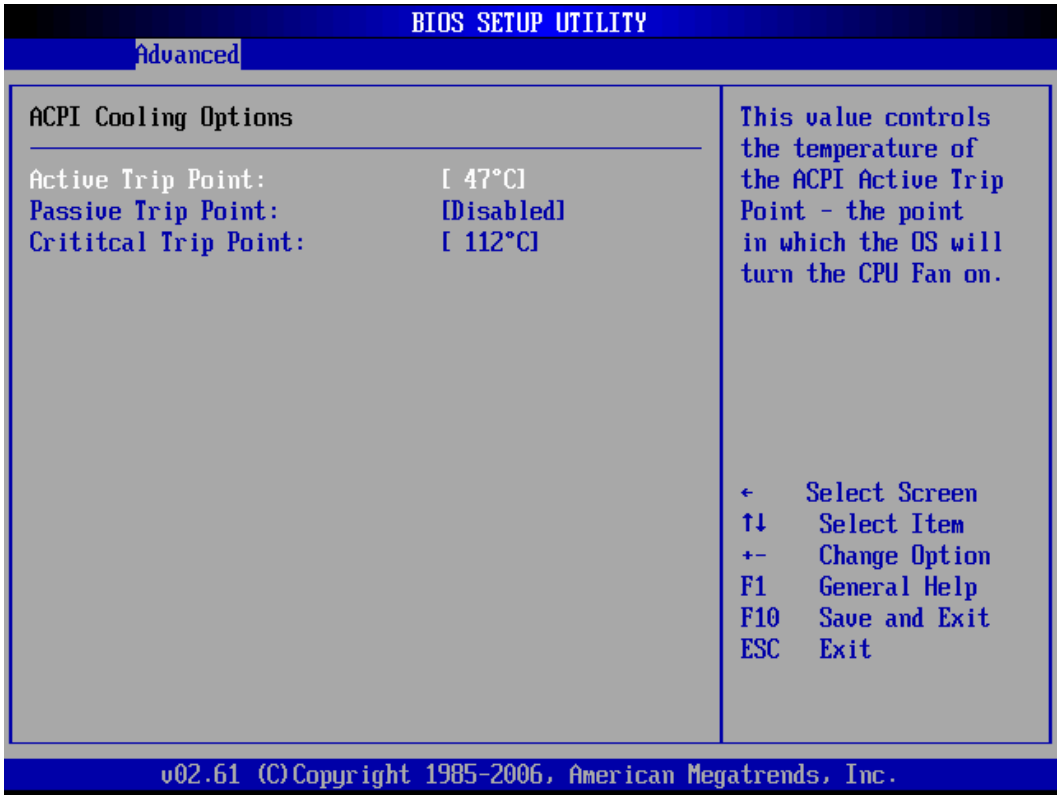
Feature	Option	Description
ACPI Version	ACPI 1.0 **ACPI 2.0** ACPI 3.0	Selects the desired ACPI specification (OS depending)
ACPI APIC Support	Disabled **Enabled**	Include ACPI APIC table pointer to RSDT pointer list. APIC supports more IRQs and faster interrupt handling
AMI OEMB Table	Disabled **Enabled**	Includes the AMI OEMB table pointer. The OEMB table is used to fill in POST data in AML code during ACPI OS operations. This option should only be disabled if ACPI 1.0 is used
Headless Mode	**Disabled** Enabled	Indicates support for headless operation, which means without keyboard, mouse and/or monitor. The OS must support the headless mode

ACPI Configuration - Chipset ACPI Configuration



Feature	Option	Description
USB Device Wakeup From S3/S4	**Disabled** Enabled	Enable/Disable USB Device Wakeup From S3/S4

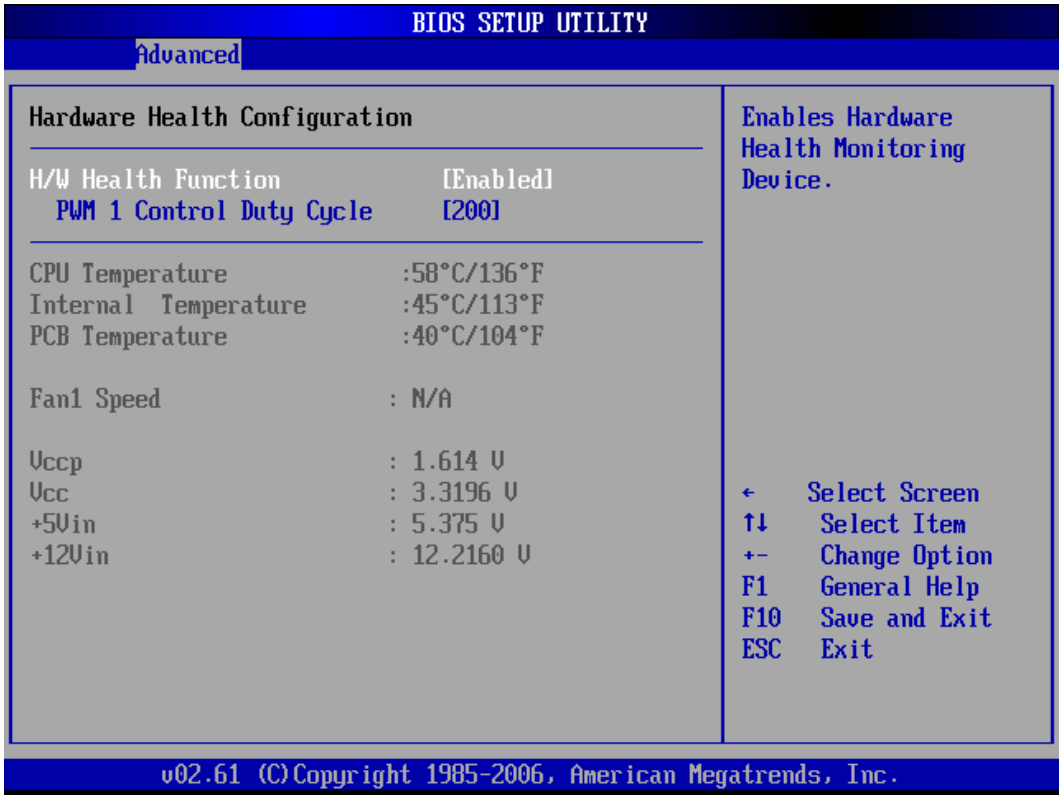
ACPI Configuration - ACPI Cooling Options



Feature	Option	Description
Passive Trip Point	**Disabled** 40°C 45°C 50°C 55°C 60°C 65°C 70°C 75°C 80°C 85°C 90°C 95°C 100°C 105°C 110°C	This value controls the temperature of the ACPI Passive Trip Point - the point in which the OS will begin throttling the CPU.
S4 Thermal Shutdown	40°C 45°C 50°C 55°C 60°C 65°C	This value controls the temperature at which the system will shutdown to a S4 state (if S4 was enabled before)

Feature	Option	Description
	70°C 75°C **80°C** 85°C 90°C 95°C 100°C 105°C 110°C	
Critical Trip Point	40°C 45°C 50°C 55°C 60°C 65°C 70°C 75°C 80°C 85°C 90°C 95°C **100°C** 105°C 110°C	This value controls the temperature of the ACPI Critical Trip Point - the point in which the OS will shut the system off.

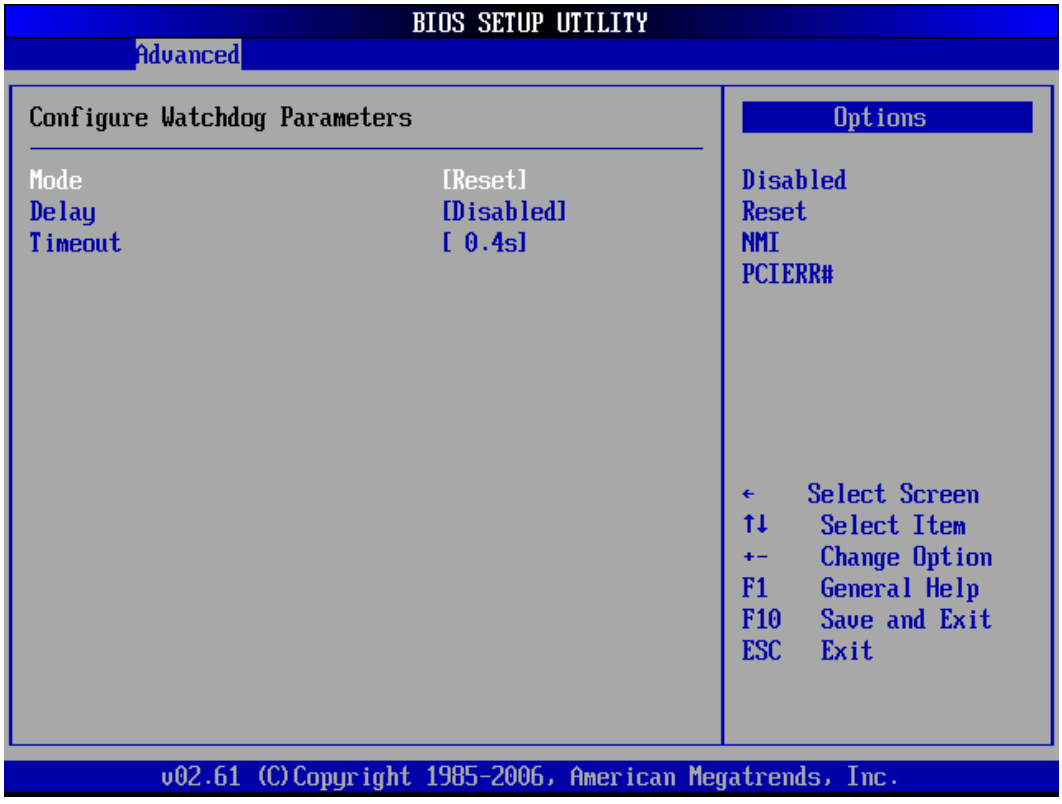
Module Hardware Health Function Configuration



Feature	Option	Description
Module H/W Health Function	**Enabled** Disabled	Enables Hardware Health Monitoring Device on module
CPU FAN Ticks Per Revolution	**1** 2 4 8	Set 'Ticks per rev' according to number of impulses sent by this type of fan during one full revolution
CPU Fan Divisor	1 2 4 **8** 16 32 64 128	Adjust Fan Divisor to allow for best display when the rotation is at the edges of the range. If the value gets out of range the fan would be displayed non-working although still running. Divisor 1: 8800 rpm Divisor 2: 4400 rpm Divisor 4: 2200 rpm Divisor 8: 1100 rpm Divisor 16: 550 rpm Divisor 32: 275 rpm

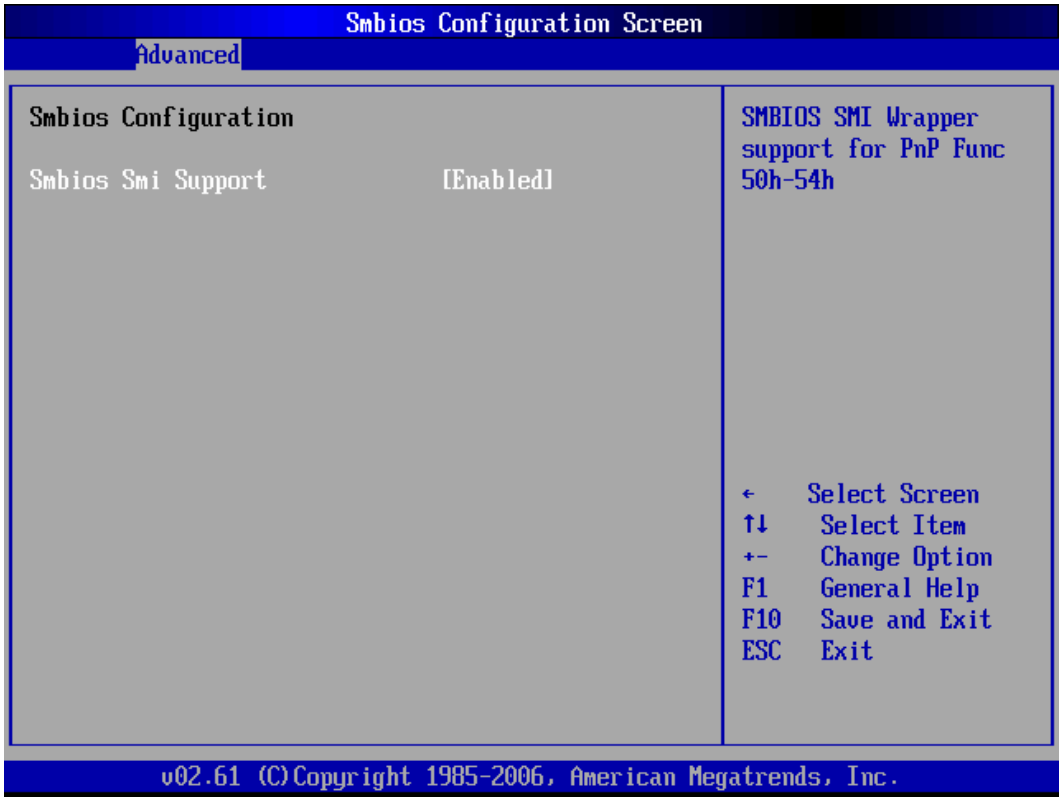
Feature	Option	Description
		Divisor 64: 137 rpm Divisor 128: 68 rpm
CPU Fan Control Mode	Manual Mode **Thermal Mode** SMARTFAN TM II	Specify different modes to control the fan
CPU Fan Output Level	15	PWM/DC Output Level 0: fan output is always logical low or at min voltage 15: fan output is always logical high or at max voltage xx: fan output logic output level is (xx/16*100%)
Target Temperature	045	Temperature value where the fan starts to work Min = 0, Max = 127
Tolerance Value	01	Tolerance Value Min = 0, Max = 15

Miscellaneous – Watchdog Parameters



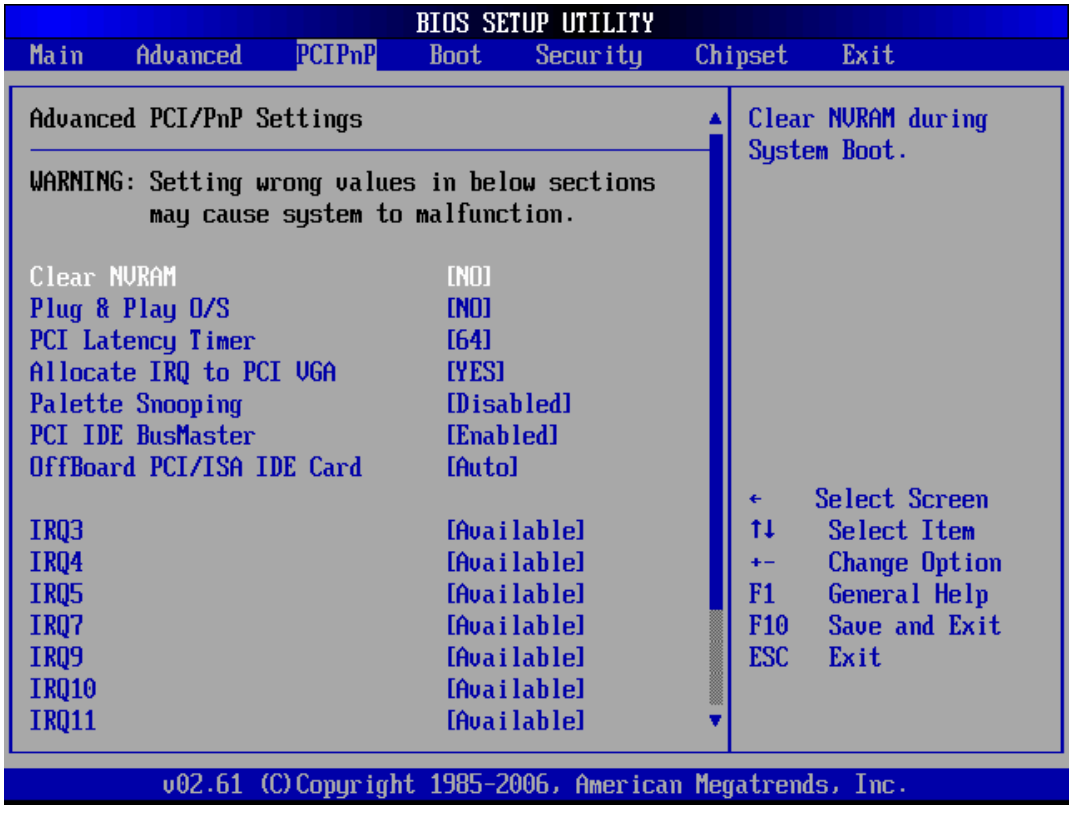
Feature	Option	Description
Watchdog Mode	**Disabled** Reset NMI	Enables / disables Watchdog
Delay	**Disabled** 1s 5s 10s 30s 1:00m 5:00m 10:00m 30:00m	Set the delay before the Watchdog gets active
Timeout	0.4s 1s 5s **10s** 30s 1:00m 5:00m 10:00m	Set the timeout for Watchdog Reset mode

SMBIOS Configuration



Feature	Option	Description
Smbios Smi Support	**Enabled** Disabled	SMBIOS SMI Wrapper support for PnP Func 50h-54h

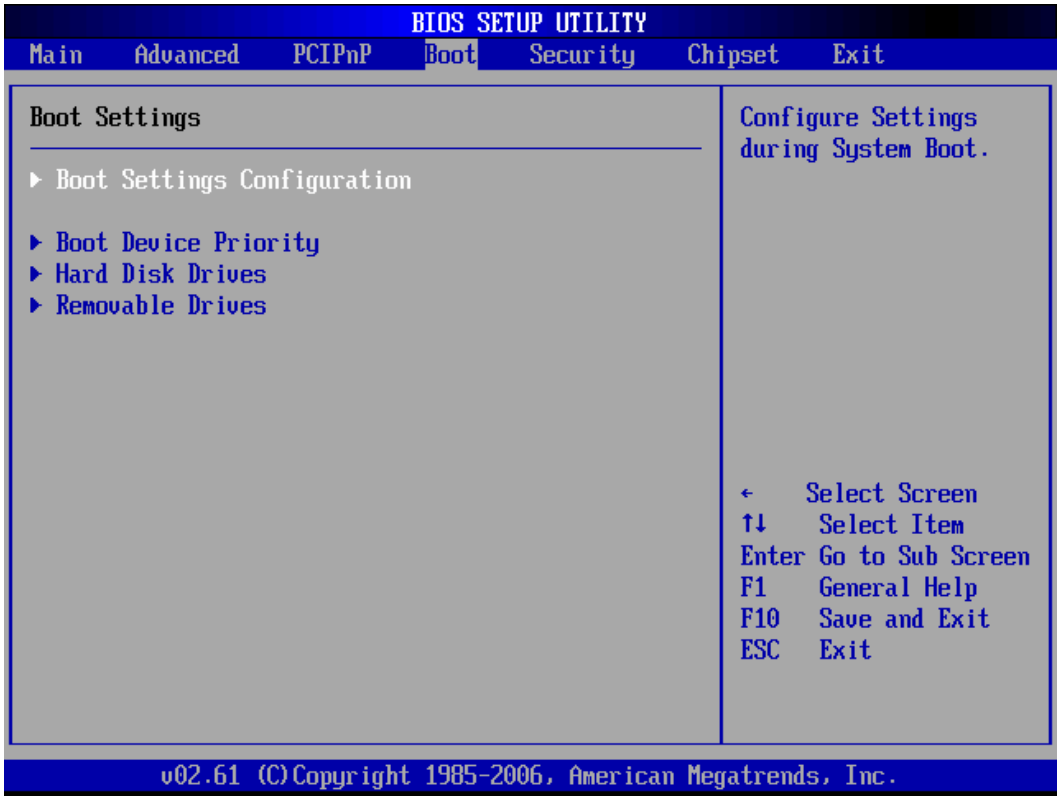
8.3.3Advanced PCI/PnP Settings



Feature	Option	Description
Clear NVRAM	**No** Yes	Clear NVRAM (None Volatile RAM) during system boot
Plug & Play O/S	**No** Yes	No: lets the BIOS configure all the devices in the system Yes: lets the OS configure PnP devices not required for boot if your system has a Plug and Play OS
PCI Latency Timer	32 **64** 96 128 160 192 224 248	Set this value to allow the Master Latency Timer to be adjusted. This option sets the latency of most PCI devices
PCI IDE Bus master	Disabled **Enabled**	If enabled improves the performance of the IDE interface for some operating systems (e.g. DOS)
IRQ3 IRQ4	**Available** Reserved	Reserved means that this interrupt is a legacy IRQ (not

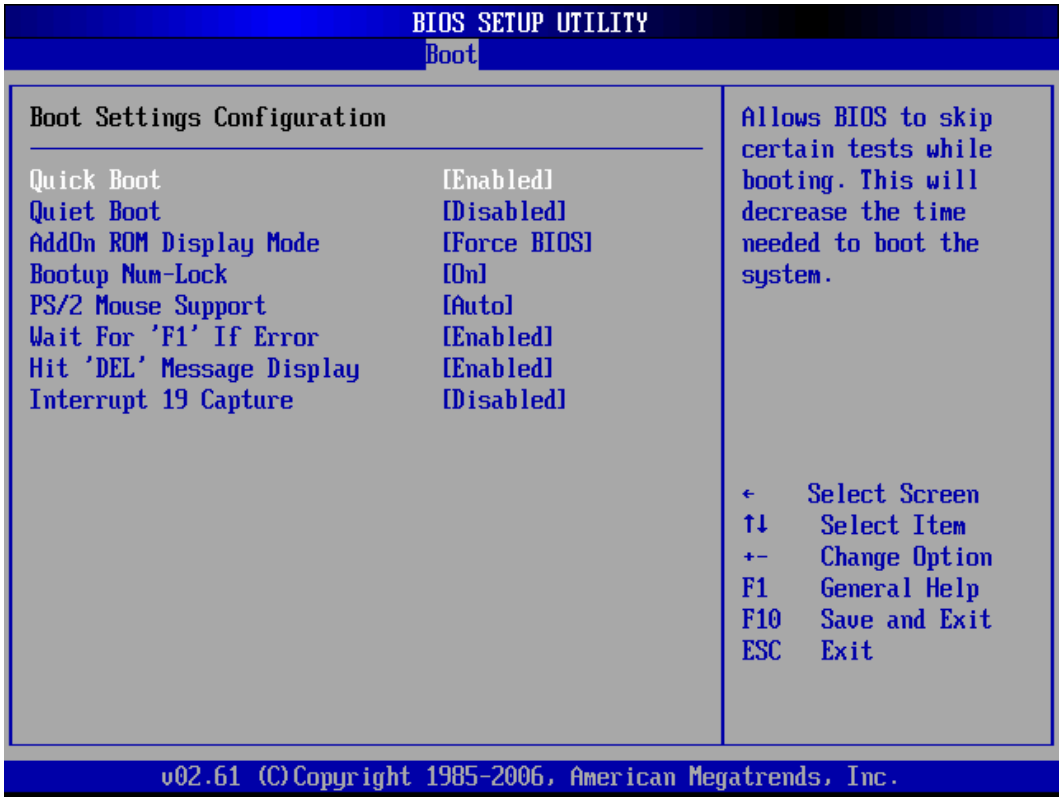
Feature	Option	Description
IRQ5 IRQ7 IRQ9 IRQ10 IRQ11 IRQ15		shared). Available defines that this interrupt can be used as a PCI IRQ
Reserved Memory Size	**Disabled** Enabled	Size of memory block to reserve for legacy ISA devices

8.3.4Boot Settings



Feature	Option	Description
Boot Settings Configuration	Submenu	Defines some special boot settings
1st Boot Device	Submenu	Specifies the 1st boot device
2nd Boot Device	Submenu	Specifies the 2nd boot device
3rd Boot Device	Submenu	Specifies the 3rd boot device

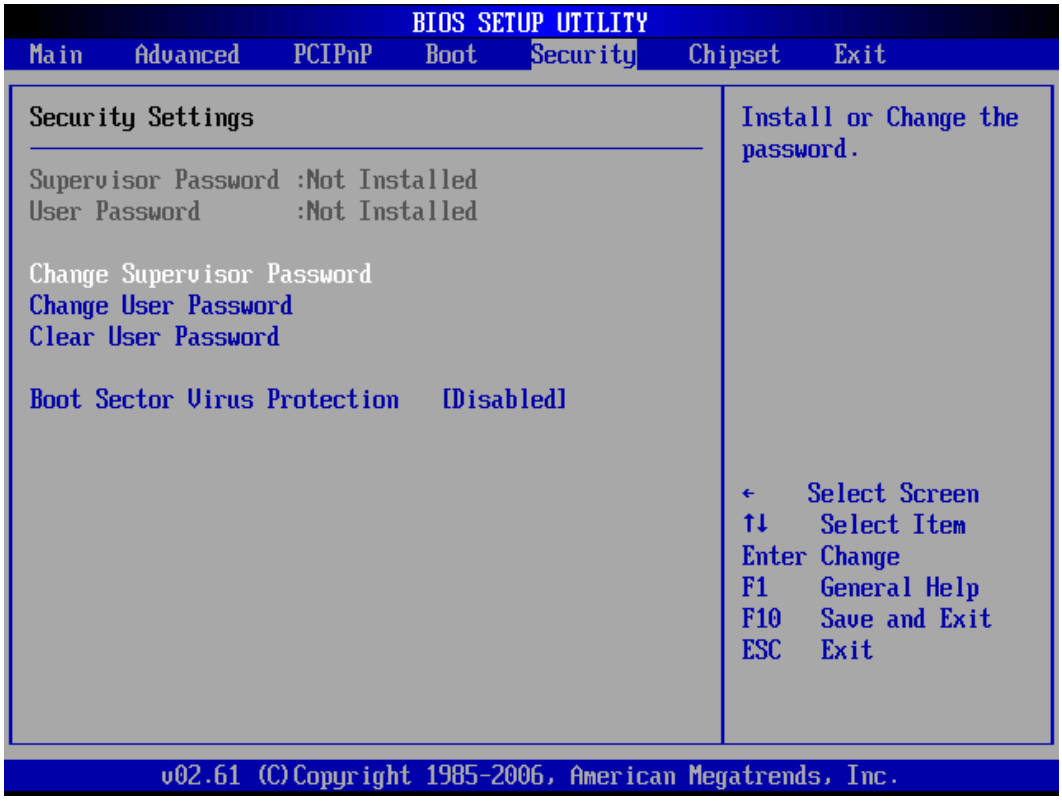
Boot Settings Configuration



Feature	Option	Description
Quick Boot	Disabled **Enabled**	Allows BIOS to skip certain tests while booting. This will decrease the time needed to boot the system
Quiet Boot	**Disabled** Enabled	If disabled the BIOS generates the normal messages, otherwise an OEM logo can be displayed
AddOn ROM Display Mode	**Force BIOS** Keep Current	Keep Current keeps the current display mode. Force BIOS switches to BIOS mode before an AddOn ROM is called
Bootup Num-Lock	Off **On**	Select power-on state for Numlock
PS/2 Mouse Support	Disabled Enabled **Auto**	If disabled or no PS/2 mouse is found (Auto) the BIOS frees up IRQ12
Wait For F1 If Error	Disabled **Enabled**	Enabled allows the BIOS to wait for any error. If an error is detected, pressing <F1> will enter the setup

Feature	Option	Description
		and the BIOS settings can be adjusting to fix the problem
'Press DEL' Message Display	Disabled **Enabled**	Enabled allows the BIOS to display the message Press DEL to run Setup after memory initialization. Disabled suppresses this message
Interrupt 19h Capture	**Disabled** Enabled	If enabled AddOn ROMs can be trapped interrupt 19h (Boot IRQ). This option would make sense when using network boot (PXE ROM)

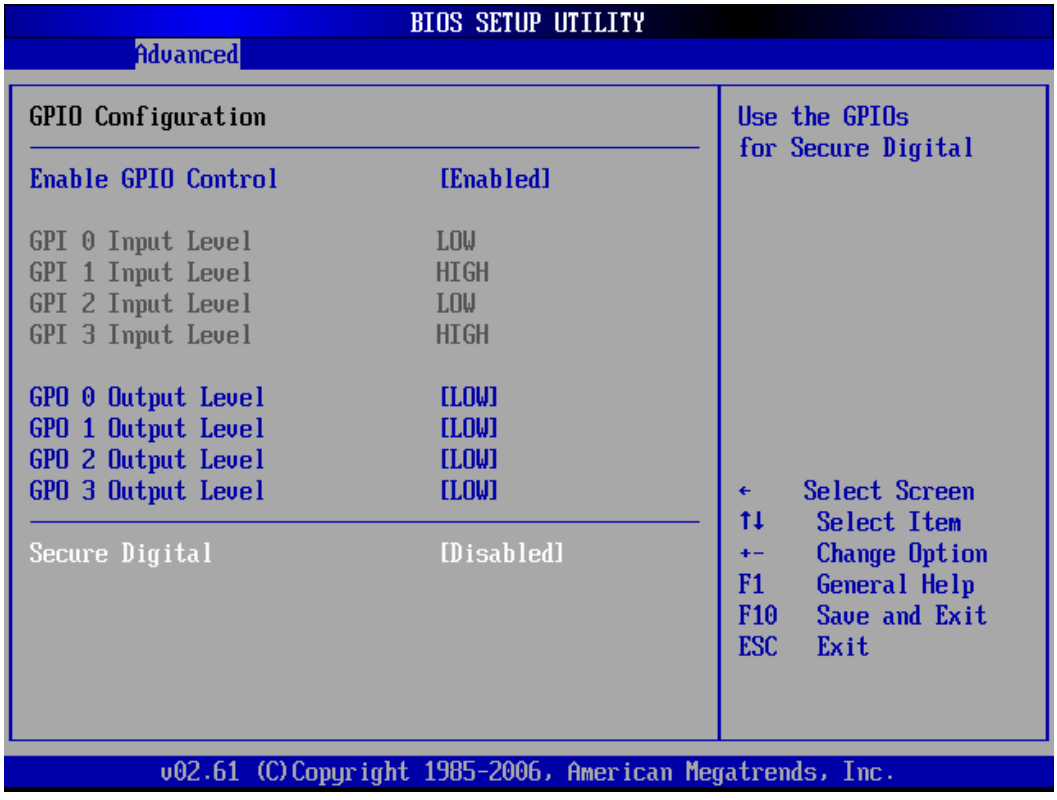
8.3.5Security Settings



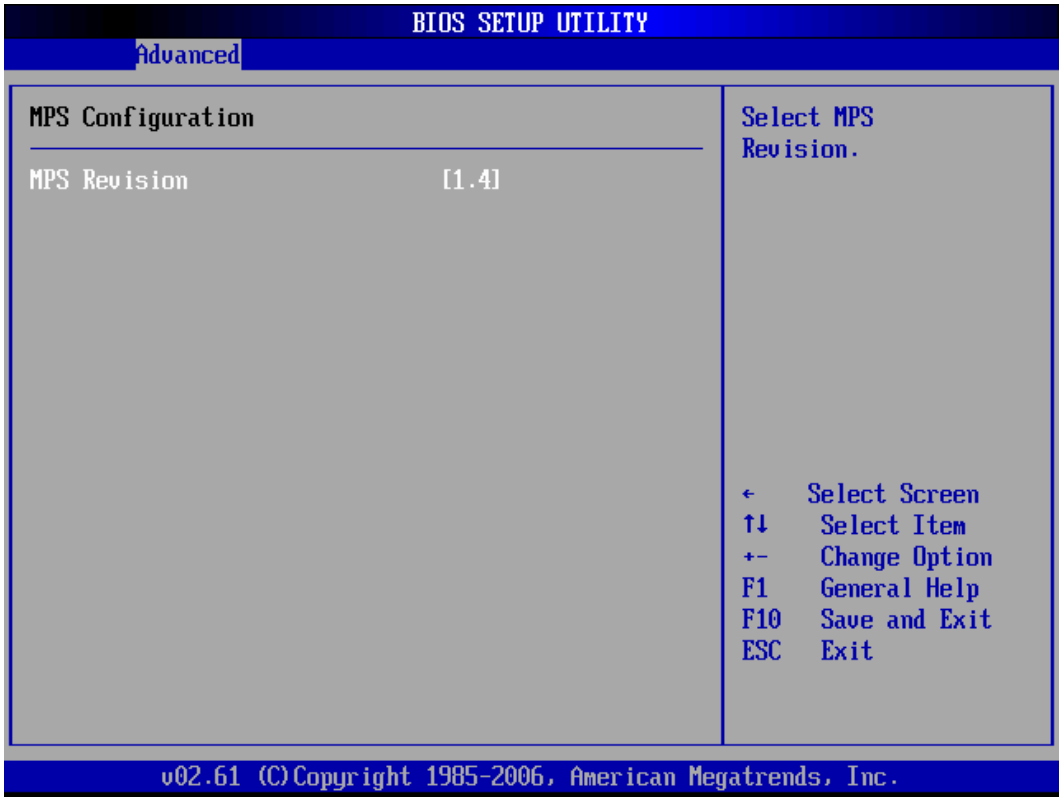
Feature	Option	Description
Change Supervisor Password		Select this option and press Enter to change the supervisor password
Change User Password		Select this option and press Enter to change the user

		password
Boot Sector Virus Protection	**Disabled** Enabled	If a program or a virus accesses the boot sector a warning appears if the option is enabled
▸ Trusted Computing	Submenu	

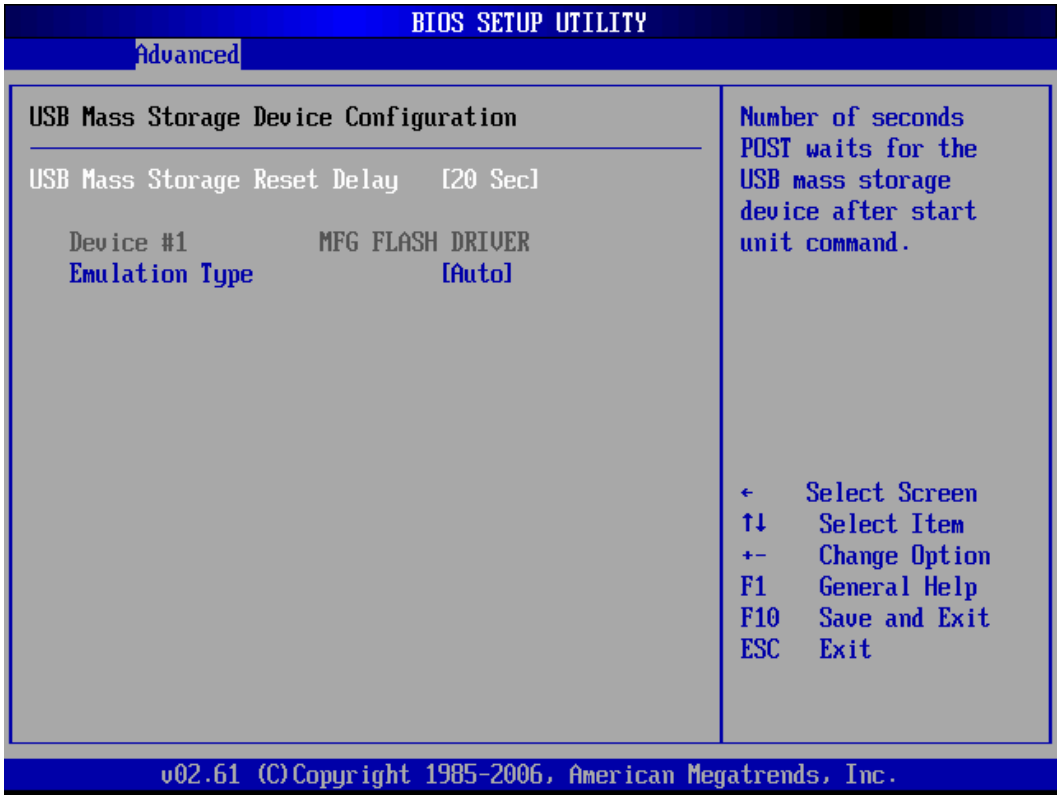
8.3.6 GPIO Configuration



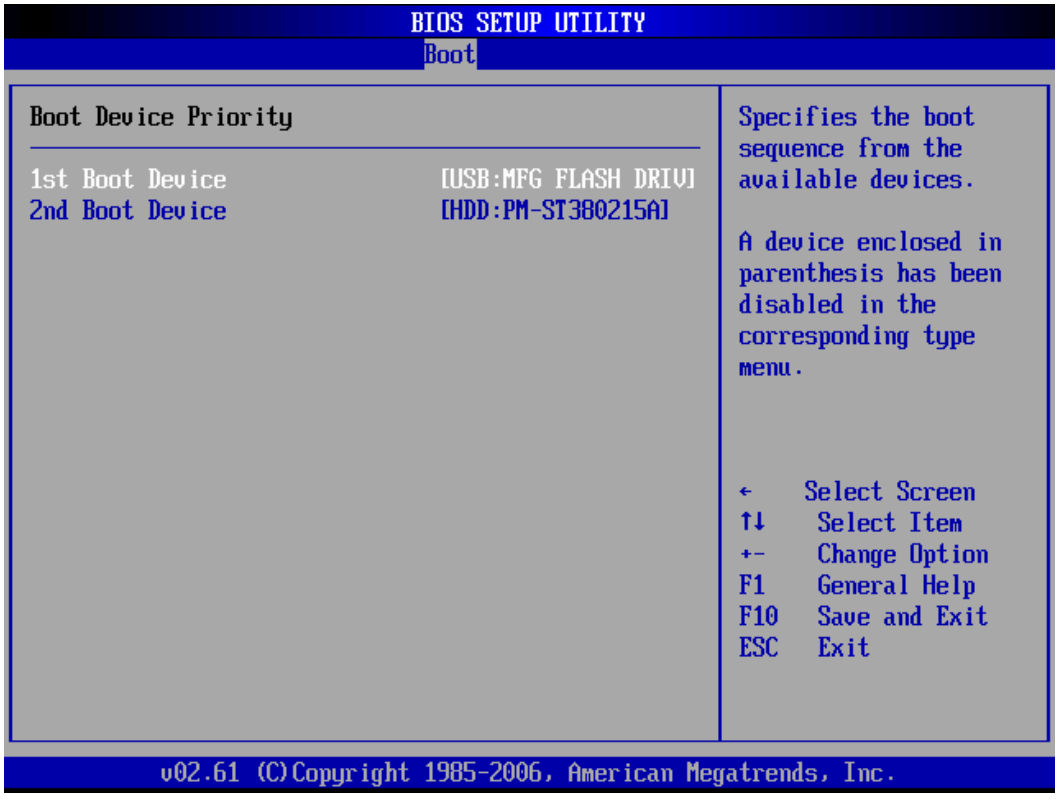
8.3.7MPS Configuration



8.3.8USB Mass Storage Device Configuration



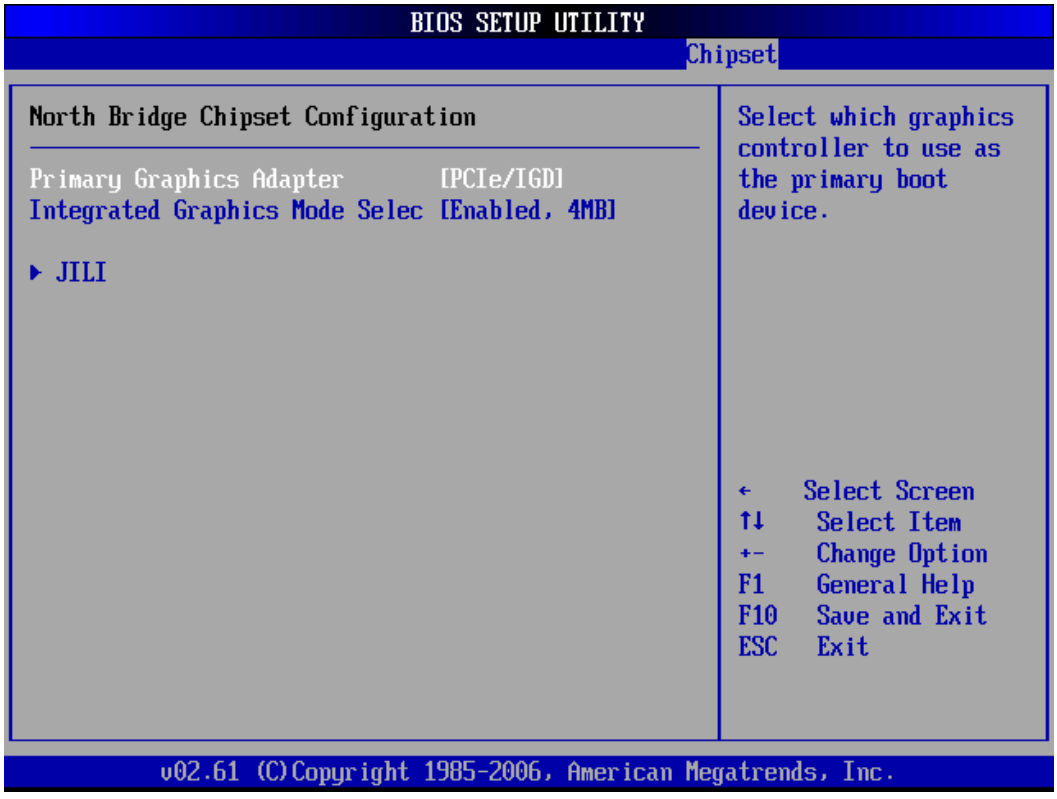
8.3.9Boot Device Priority



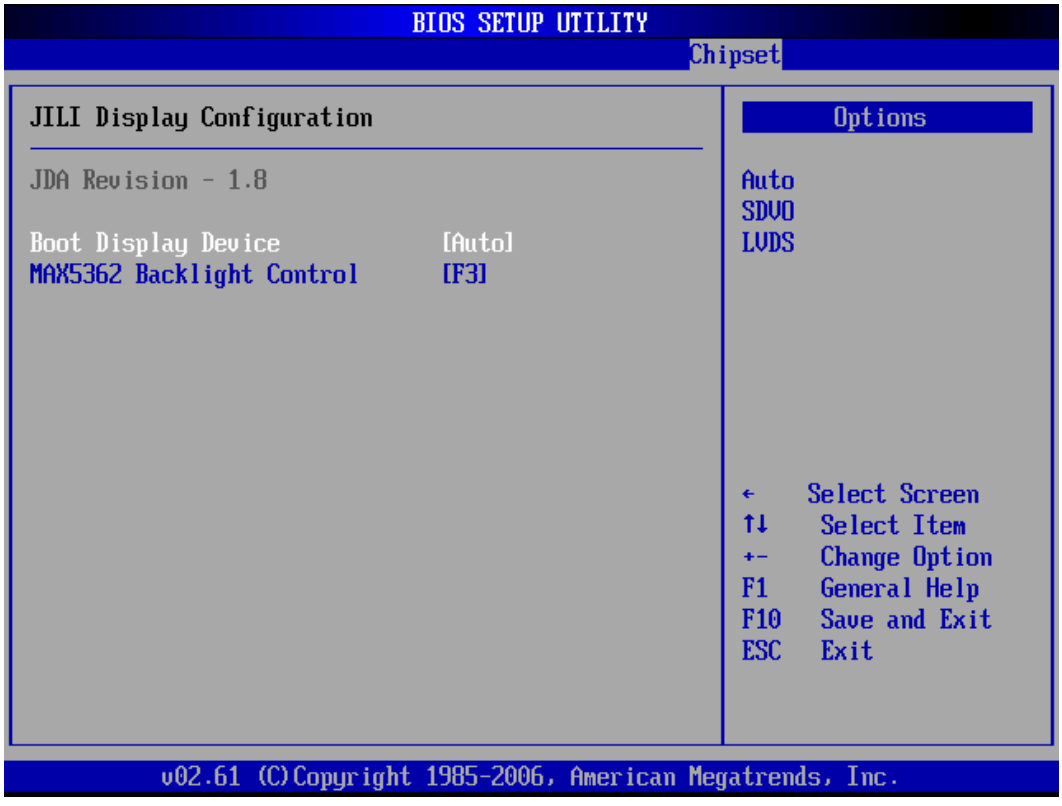
8.3.10 Advanced Chipset Configuration



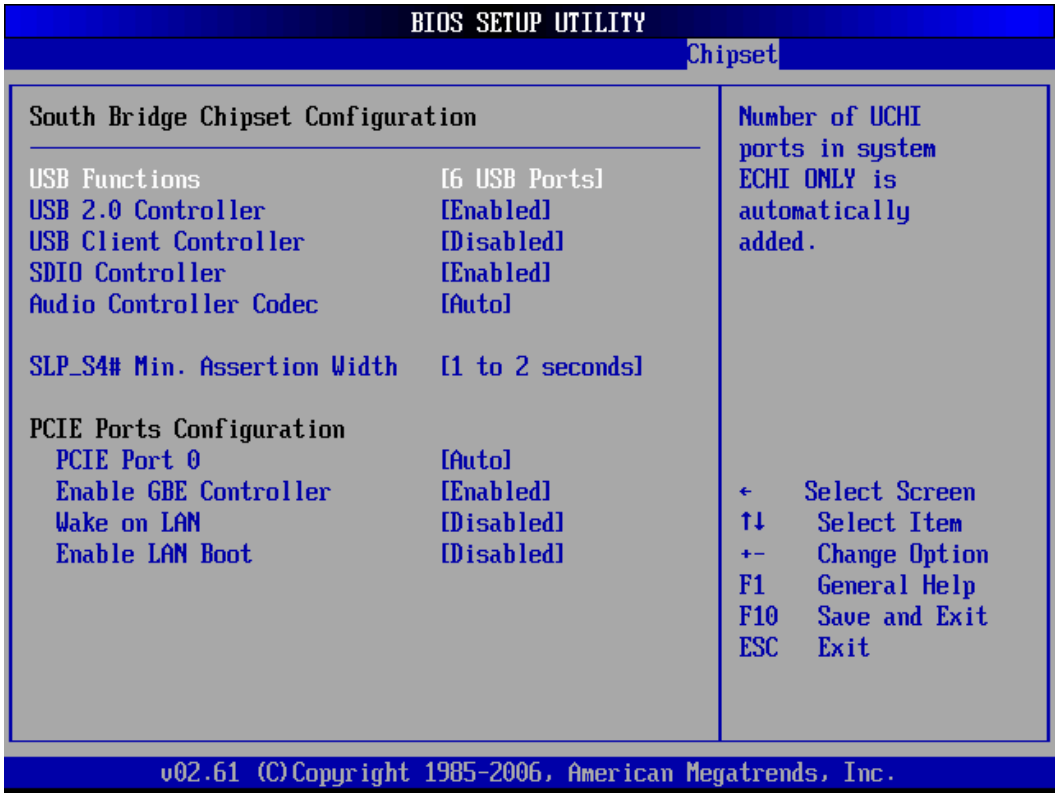
8.3.11 North Bridge Chipset Configuration



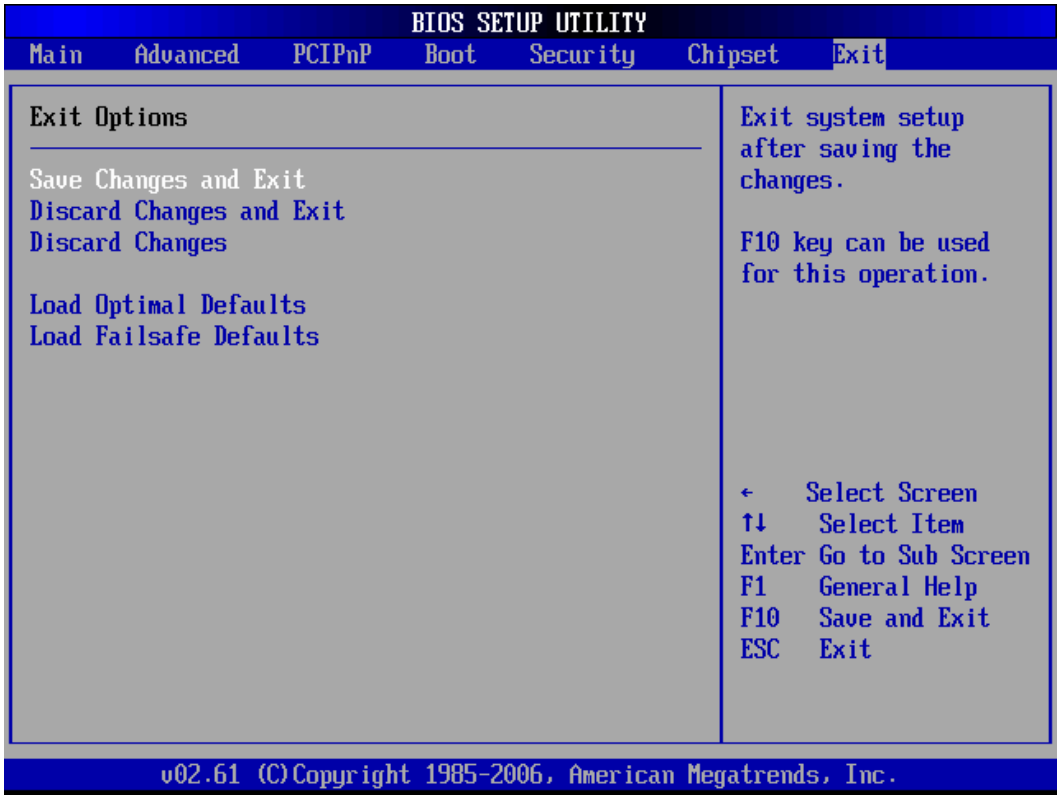
8.3.12 JILI Display Configuration



8.3.13 South Bridge Chipset Configuration



8.3.14 Exit Options



Feature	Description
Save To RTC/EEPROM and Exit	Saving system setup to RTC and EEPROM and exit setup. F10 key can be used for this operation
Save As Custom Defaults To RTC/Flash and Exit	Saving system setup as custom defaults to RTC and Flash and exit setup. F11 key can be used for this operation
Discard Changes and Exit	Exit system setup without saving any changes. ESC key can be used for this operation
Discard Changes	Discards changes done so far to any of the setup questions. F7 key can be used for this operation
Load Manufacturing Defaults	Load manufacturing default values for all the setup questions. F9 key can be used for this operation

8.4 Appendix A: JIDA Standard

Every board with an on-board BIOS extension supports the following function calls, which supply information about the board. Jumptec Intelligent Device

Architecture (JIDA) functions are called via Interrupt 15h. Functions include:

» AH=Eah

» AL=function number

» DX=4648h (security word)

» CL=board number (starting with 1)

The interrupt returns a CL□0 if a board with the number specified in CL does not exist. CL will equal 0 if the board number exists. In this case, the content of DX determines if the operation was successful. DX=6B6Fh indicates success; other values indicate an error.

8.5 JIDA Information

To obtain information about boards that follow the JIDA standard, use the following procedure.

» Call Get BIOS ID with CL=1. The name of the first device installed will be returned. If you see the result Board exists (CL=0), increment CL, and call Get BIOS ID again.

» Repeat until you see Board not present (CL□0). You now know the names of all boards within your system that follow the JIDA standard.

» You can find out more information about a specific board by calling the appropriate inquiry function with the board's number in CL.

NOTE: Association between board and board number may change because of configuration changes. Do not rely on any association between board and board number. Always use the procedure described above to determine the association between board and board number.

Refer to the JIDA manual in the jidai1xx.zip folder, which is available from the Kontron Web site, for further information on implementing and using JIDA calls with C sample code.

9 Appendix B: Architecture Information

The following sources of information can help you better understand PC architecture.

9.1 Buses

9.1.1ISA, Standard PS/2 – Connectors

» AT Bus Design: Eight and Sixteen-Bit ISA, E-ISA and EISA Design, Edward Solari, Annabooks, 1990, ISBN 0-929392-08-6

» AT IBM Technical Reference Vol. 1&2, 1985

» ISA & EISA Theory and Operation, Edward Solari, Annabooks, 1992, ISBN 0929392159

» ISA Bus Specifications and Application Notes, Jan. 30, 1990, Intel

» ISA System Architecture, Third Edition, Tom Shanley and Don Anderson, Addison-Wesley Publishing Company, 1995, ISBN 0-201-40996-8

» Personal Computer Bus Standard P996, Draft D2.00, Jan. 18, 1990, IEEE Inc

» Technical Reference Guide, Extended Industry Standard Architecture Expansion Bus, Compaq 1989

9.1.2PCI/104

» Embedded PC 104 Consortium

» The consortium provides information about PC/104 and PC/104-Plus technology. You can search for information about the consortium on the Web.

» PCI SIG

» The PCI-SIG provides a forum for its ~900 member companies, who develop PCI products based on the specifications that are created by the PCI-SIG. You can search for information about the SIG on the Web.

» PCI & PCI-X Hardware and Software Architecture & Design, Fifth Edition, Edward Solari and George Willse, Annabooks, 2001, ISBN 0-929392-63-9.

» PCI System Architecture, Tom Shanley and Don Anderson, Addison-Wesley, 2000, ISBN 0-201-30974-2.

9.2 General PC Architecture

» Embedded PCs, Markt&Technik GmbH, ISBN 3-8272-5314-4 (German)

» Hardware Bible, Winn L. Rosch, SAMS, 1997, 0-672-30954-8

» Interfacing to the IBM Personal Computer, Second Edition, Lewis C. Eggebrecht, SAMS, 1990, ISBN 0-672-22722-3

» The Indispensable PC Hardware Book, Hans-Peter Messmer, Addison-Wesley, 1994, ISBN 0-201-62424-9

» The PC Handbook: For Engineers, Programmers, and Other Serious PC Users, Sixth Edition, John P. Choisser and John O. Foster, Annabooks, 1997, ISBN 0-929392-36-1

9.3 Ports

9.3.1RS-232 Serial

» EIA-232-E standard

» The EIA-232-E standard specifies the interface between (for example) a modem and a computer so that they can exchange data. The computer can then send data to the modem, which then sends the data over a telephone line. The data that the modem receives from the telephone line can then be sent to the computer. You can search for information about the standard on the Web.

» RS-232 Made Easy: Connecting Computers, Printers, Terminals, and Modems, Martin D. Seyer, Prentice Hall, 1991, ISBN 0-13-749854-3

» National Semiconductor: The Interface Data Book includes application notes. Type "232" as search criteria to obtain a list of application notes. You can search for information about the data book on National Semiconductor's Web site.

9.3.2Serial ATA

Serial AT Attachment (ATA) Working Group: This X3T10 standard defines an integrated bus interface between disk drives and host processors. It provides a common point of attachment for systems manufacturers and the system. You can search for information about the working group on the Web. We recommend you also search the Web for information on 4.2 I/O cable, if you use hard disks in a DMA3 or PIO4 mode.

9.3.3USB

USB Specification

USB Implementers Forum, Inc. is a non-profit corporation founded by the group of companies that developed the Universal Serial Bus specification. The USB-IF was formed to provide a support organization and forum for the advancement and adoption of Universal Serial Bus technology. You can search for information about the standard on the Web.

9.4 Programming

» C Programmer's Guide to Serial Communications, Second Edition, Joe Campbell, SAMS, 1987, ISBN 0-672-22584-0

» Programmer's Guide to the EGA, VGA, and Super VGA Cards, Third Edition, Richard Ferraro, Addison-Wesley, 1990, ISBN 0-201-57025-4

» The Programmer's PC Sourcebook, Second Edition, Thom Hogan, Microsoft Press, 1991, ISBN 1-55615-321-X

» Undocumented PC, A Programmer's Guide to I/O, CPUs, and Fixed Memory Areas, Frank van Gilluwe, Second Edition, Addison-Wesley, 1997, ISBN 0-201-47950-8

10 Appendix C: Document Revision History

Revision	Date	Edited by	Changes
0.1	5-Nov-09	CAV	Initial creation of manual
0.5	12-Jan-10	LdJ	First review draft
0.6	4-Mar-10	LdJ	Second review draft with review input and new figures
0.8	11-Mar-10	LdJ	Updated with additional changes to pin-outs, part numbers
0.9	30-Apr-10	CAV	Update to Table 7
1.0	21-July-10	CAV	Update information regarding PCIe lanes and various other updates.
1.1	19-Aug-10	CAV	Updated MTBF and Electrical Specification
1.2	1-Dec-2010	CAV	Update to PCIe lanes info in on page 9
1.3	20-Dec-2010	CAV	Removed RAID function and PEX references throughout the document as they are not supported by the design
1.4	8-Apr-2011	CAV	Update to info in Section 4.2.3
1.5	9-Dec-2011	CAV	Updated necessary voltage information in sections 3.4.1 and 4.2.9 to reflect 5V-18V
1.6	27-Feb-2012	CAV	Updated product name to be COMe-cXLi2 and removed "BOOT USB HDD First" from BIOS section
1.7	31-May-2012	CAV	Correction to remove reference to ATX mode support. Add info that module will auto power on whenever +5V_Standby or +12V is present, without waiting for power button press

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