Modular Computers ®

CP301

3U CompactPCI
Pentium III-based CPU Board

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The product described in this manual is in compliance with all applied CE standards.

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Revision History

Revision History			
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Rev. Index	**Brief Description of Changes**	**Board Index**	**Date of Issue**
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02	General manual revision and update including addition of Rear I/O module chapter	00	Nov.00

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Explanation of Symbols



CE Conformity

This symbol indicates that the product described in this manual is in compliance with all applied CE standards. Please see also the section “Applied Standards” in this manual.



Caution!

This symbol and title warn you of hazards due to electrical shocks (> 60 V) when touching products or parts of them. Failure to observe the necessary precautions as described and/or prescribed by the law may result in damage to your product and/or endanger your life/health.

Please see also the section “High Voltage Safety Instructions”.



ESD-Sensitive Device!

This symbol and title highlight the fact that electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Please read also the section “Special Handling and Unpacking Instructions” on the following pageof this manual.



Attention!

This symbol and title emphasize aspects which, if not understood and taken into consideration by the reader, may result in hazards to health and/or material damage.



Note:

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This symbol and title accompany information highlighting positive aspects of a *PEP* product and/or procedure.



Troubleshooting

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For your safety

Your new *PEP* product has been developed and carefully tested in order to provide all the features necessary to ensure full compliance with all electrical safety requirements. It has also been designed for a long fault-free life. However, the life expectancy of your product will be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interests of your own safety and of the correct operation of your new *PEP* product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions



Warning!

All operations on this device must be carried out by sufficiently skilled personnel.



Caution!

The power supply must always be disconnected before installation, repair and maintenance operations are carried out on this product. Failure to comply with this basic precaution will subject the operator to serious electrical shock hazards. Always unplug the power cable before such operations.
Before installing your new *PEP* product into a system always ensure that your mains power is switched off. This applies also to the installation of piggybacks.

Special Handling and Unpacking Instructions



ESD Sensitive Device!

Electronic boards and their components are sensitive to static electricity. Care must therefore be exercised at all times during handling and inspection of the board, in order to ensure product integrity.

- Do not handle this product while it is outside its protective enclosure while it is not used for operational purposes, unless it is otherwise protected.
- Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where safe work stations are not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.
- It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the board is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or tracks on the board.

General Instructions on Usage

- In order to maintain *PEP's* product warranty, this product must not be altered or modified in any way. Changes or modifications to the device, which are not explicitly approved by *PEP Modular Computers* and described in this manual or received from *PEP* Technical Support as a special handling instruction, will void your warranty.
- This device should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This applies also to the operational temperature range of the specific board version, which must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.
- In performing all necessary installation and application operations, please, follow only the instructions supplied by the present manual.
- Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the board please re-pack it as nearly as possible in the manner in which it was delivered.
- Special care is necessary when handling or unpacking the product. Please consult the special handling and unpacking instructions on the previous page of this manual.

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Chapter 1

Introduction

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1. Introduction

1.1 Introduction to CompactPCI

The *PEP Modular Computers* CompactPCI product described in this chapter operates with the PCI bus architecture to support additional I/O and memory-mapped devices as required by various industrial applications. For detailed information concerning the CompactPCI standard, please consult the complete Peripheral Component Interconnect (PCI) and CompactPCI Specifications. For further information regarding these standards and their use, visit the homepage of the *PCI Industrial Computer Manufacturers Group (PICMG)*.

Many system-relevant CompactPCI features that are specific to *PEP Modular Computers* CompactPCI systems may be found described in the *PEP* CompactPCI System Manual. Due to its size, this manual cannot be downloaded via the internet. Please refer to the section “Related Publications” at the end of this chapter for the relevant ordering information.

The CompactPCI System Manual includes the following information:

- Common information that is applicable to all system components, such as safety information, warranty conditions, standard connector pinouts etc.
- All necessary information to combine *PEP Modular Computers* racks, boards, backplanes, power supply units and peripheral devices in a customized CompactPCI system, as well as configuration examples.
- Data on rack dimensions and configurations as well as information on mechanical and electrical rack characteristics.
- Information on the distinctive features of *PEP Modular Computers* CompactPCI boards, such as functionality, hotswap capability. In addition, an overview is given for all existing *PEP Modular Computers* CompactPCI boards with links to the relating datasheets.
- Generic information on the *PEP Modular Computers* CompactPCI backplanes, such as the slot assignment, PCB form factor, distinctive features, clocks, power supply connectors and signalling environment, as well as an overview of the *PEP Modular Computers* CompactPCI standard backplane family.
- Generic information on the *PEP Modular Computers* CompactPCI power supply units, such as the input/output characteristics, redundant operation and distinctive features, as well as an overview of the *PEP Modular Computers* CompactPCI standard power supply unit family.

1.2 *PEP* Single-height CPU Boards

Socket 7 Family

The CP312 is a highly integrated 32bit/33 MHz CompactPCI single-board computer that is designed around the Pentium® family from Intel® and AMD®'s K6™ microprocessors. The VGA interface is integrated within the Chipset. To achieve high CPU and memory performance the board includes 512 kB L2 Cache. DRAM is 32 MB or 64 MB (soldered) which together with the SODIMM provides up to 128 MB main memory.

Mobile Pentium®III Family

The CP302 is a high performance 64-bit/33 MHz CompactPCI system controller board designed to utilize the Intel®, Mobile Pentium®III Coppermine™ microprocessors and future processors. This board is based on the Intel®, 440BX AGP sets and can support CPU speeds of 400 MHz through 700 MHz and host bus speeds up to 100 MHz.

The CP301 is a system controller which is identical to the CP302 in every respect except that it has a diifferent layout and a new 4HP front panel interface. The CP301 supports two COM ports and one Fast Ethernet connector on the 4HP interface. The keyboard, USB and VGA connectors are not available on the 4HP product.

The CP302PM is a non-system controller which is identical to the CP302 apart from having a different PCI/PCI (non-transparent) bridge at J1/J2. This makes possible the addition of further CP302PM's together with a system controller CPU on one CompactPCI bus, i.e. multiprocessing.

1.3 CP301 Product Overview

The CP301 is a highly integrated single-board computer designed around the Intel® Mobile Pentium® III family of microprocessors. The board has been designed to find an optimum equilibrium between performance and power dissipation and supports clock speed of 700 MHz - and higher as available.

Optionally, the CP301 can be equipped with a 69030 VGA chip with 4 MB SDRAM memory. Speed of operation is assured by means of the onboard 66 MHz AGP interface. High resolution is provided with the video controller supporting pixel resolutions of up to 1600 x 1200 or up to 16.7 M colors. The board also features a 10BASE-T/100BASE-TX Fast Ethernet based on the Intel®, 82559 Fast Ethernet PCI Bus Controller.

Designed for stability and packaged in a rugged format, the board fits into all applications situated in industrial environments. The low power consumption of the board is further assured through the use of 3.3 V and 1.5V I/O technology.

The board is compatible with the Microsoft Windows NT® operating system. However, the performance of CompactPCI can be tailored to suit real-time applications and operating systems such as Linux®, QNX® or VxWorks® which are instrumental to the success of CompactPCI in these market sectors.

1.4 CP301 Board Introduction

The CP301 is a CompactPCI Mobile Pentium®III Coppermine™ based single-board computer specifically designed for use in highly integrated platforms with solid mechanical interfacing for a wide range of industrial environment applications.

Some of the CP301's outstanding features are:

- compliance with CompactPCI Interface 2.0 R3.0
- independent CompactPCI interface
- suitable for all Intel® Mobile Pentium®III Coppermine™ processors in the 495-pin BGA2 package
- up to 256 MB SDRAM main memory, 128 MB soldered with ECC and 128 MB via SODIMM
- 256 kB FLASH for BIOS
- Flash Disk up to 288 MB
- optional onboard high performance AGP VGA controller (rear I/O only)
- one EIDE interface, two with Rear I/O version
- one Fast Ethernet device: 10BaseT & 100BaseTX
- integrated Hardware monitor
- optional rear I/O

The CP301 includes the following commonly used peripheral devices:

- floppy disk interface
- keyboard/USB interface (both optional via rear I/O)
- two serial ports(ESD protected and EMI compliant)
- counter/timers
- watchdog timer
- real-time clock

1.5 CP301 Main Specifications

Table 1-1: CP301 Main Specifications

CP301	Specifications
CPU	Intel® Mobile Pentium®III Coppermine™ processor up to 700 MHz with 256 kB L2 on-die cache in 495 BGA2 packaging
Memory	100 MHz system memory bus 256 kB L2 on-die full speed processor cache 64 MB up to 128 MB SDRAM via one SODIMM socket running at 100 MHz 64 up to 128 MB SDRAM soldered with ECC running at 100 MHz 512 kB Flash (or optional SRAM with 256 kB or 512 kB) Optional DiskOnChip™ module up to 288 MB 2x256 Byte EEPROM for storing CMOS data when operating without battery and 2 x 256 byte EEPROM for user purposes
Super I/O	The FDC37C672 from SMSC is an ISA Plug and Play compatible I/O device that provides the following functions: - Two 16C550 compatible UARTs with 16 bytes FIFO - PS/2 keyboard and mouse interface (optional on rear I/O) - Floppy disk controller up to 2.88 MB
Chipset	Intel® 82440BX PCI/AGP controller - GTL processer interface - Integrated DRAM controller - AGP and PCI interface Intel® 82371EB PCI/ISA EIDE Xcelerator (PIIX4E) - Multifunction PCI to ISA bridge - Enhanced DMA controller - Interrupt controller based on two 82C59's - Timer based on 82C84 - Real-time clock - Power management logic - Supports two USB interfaces (optional on rear I/O) - Supports two EIDE interfaces
Fast Ethernet Interface	Controller: Intel® 82559 Fast Ethernet Controller Data Rate: 10 & 100 MBit/s Ethernet: Full 802.2 & 802.3 IEEE compliance supporting 10Base-T and 100Base-TX Cabling: Category 5 two-pair cabling
Software Support	Award BIOS with Preboot Agent contained within 256 kB of Flash memory. The BIOS parameters are saved in the EEPROM. The CP301 is able to operate without disks, keyboard and video operating systems: Linux®, QNX®, VxWorks®, Windows NT® etc. MS-DOS®, Windows 95®, 98®, Windows 2000®
CompactPCI Bus Interface	Compatible with CompactPCI Specification V 2.0, Rev. 3.0 64-bit/33 MHz master interface 3.3V/5.0V compatible

Table continued on following page

Table 1-1: CP301 Main Specifications

CP301	Specifications
Rear I/O	When the rear I/O is enabled the CompactPCI interface is configured for 32-bit/33 MHz The 32-bit CompactPCI bus has rear I/O capability. The following interfaces are routed to the rear I/O connector J2: COM1 and COM2, PS/2 mouse and keyboard, 2xUSB's, Ethernet and secondary EIDE port.
General	Dimensions: 100 mm x 160 mm Operating temp.: 0°C to +60°C E1 (optional): -25°C to +75°C E2 (optional): -40°C to +85°C Storage temp.: -55°C to +85°C Operating humidity: 0% to 95% non-condensing Weight: CP301 4HP without heatsink: 200g CP301 4HP with heatsink: 278g
Front Panel Interfaces	COM1: 8-pin RJ45 (RS232) COM2: 9-pin D-sub (RS232) Ethernet: one RJ45 connector LED's: ACT, SPEED: Ethernet status LED: TH: Overtemperature status Reset button, guarded
Onboard interfaces	One EIDE interface supporting Ultra/DMA for 2 hard disks or CD-ROM on 40-pin 2.54mm connectors One floppy disk interface (up to 2.88 MB) PCI extension connection
Thermal Management / System Monitoring	Watchdog: software configurable watchdog generates IRQ, NMI or hardware reset Hardware monitor: LM81 monitoring temperature, fan speed and all onboard voltages Temperature monitor: MAX 1617 monitoring the CPU on-die and board temperature
Hotswap-Compatible	The CP301 supports the addition or removal of other boards whilst in a powered-up state. Individual clocks for each slot and Enum signal handling are in compliance with the PCIMG 2.1 Hotswap Specification.
Common Features	DC power monitors (3.3V and 5V) Battery socket and 3.0V lithium battery for RTC: VARTA Type CR2025 PANASONIC BR2020

1.6 Power Consumption and Temperature Range

The CP301 board is based on the Intel® Mobile Pentium®III processor. Intel® has developed mobile processors to meet the specific needs of mobile PC's. As such, they operate at lower voltages than their desktop counterparts, are significantly smaller in size, consume less power and dissipate less heat. The design is optimized for low power consumption applications.

The goal of this description is to provide a method to calculate the power consumption for the CP301 base board and for additional configurations. The processor dissipates the majority of the thermal power.

The power consumption table lists the voltage and current specifications for the CP301 board and the CP301 accessories. The values are measured with a 8 slot passive CompactPCI backplane and two power supplies, one for the CPU and the other one for the harddisk. During the measurement the power consumption of the backplane can be ignored. The operating systems was DOS 6.22 without power management and Windows NT 4.0 with power management. The measured values varied, because the power depended on the processor activity. All Mobile Pentium®III processors are powered with 1.35V core voltage (low power version).

These values were measured at the DOS prompt and without the keyboard.

Table 1-2: Power Consumption Table with DOS Running (without keyboard)

Power	5V	3.3V	Total
400 MHz 32 or 64 MB Memory (128 Mbit chips) without VGA	5.2W	5.3W	10.5W
400 MHz 64 or 128 MB Memory with VGA	5,3W	6.5W	11.8W
500 MHz 64 or 128 MB Memory with VGA	5.9W	6.5W	12.4W
700 MHz 64 or 128 MB Memory with VGA	*TBD*	*TBD*	*TBD*

Table 1-3: Power Consumption Table with Windows NT 4.0 Running (no application started and without keyboard)

Power	5V	3.3V	Total
400 MHz 32 or 64 MB Memory (128 Mbit chips) without VGA	1.2W	4.7W	5.9W
400 MHz 64 or 128 MB Memory with VGA	1.2W	5.9W	7.1W
500 MHz 64 or 128 MB Memory without VGA	1.4W	5.9W	7.3W
700 MHz 64 or 128 MB Memory without VGA	*TBD*	*TBD*	*TBD*

The 400 MHz version without VGA is not a standard version. For more information please contact *PEP*.

Table 1-4: Power Consumption Table for CP301 Accessories

Module	Power 5V	Power 3.3V
Keyboard	100 mW	--
64 MB SODIMM module	--	500 mW
128 MB SODIMM module	--	500 mW
DiskOnChip™ 16 MB	100 mW	--
DiskOnChip™ 144 MB	100 mW	--

1.6.1 Temperature Range

The CP302 family are the first CompactPCI boards capable of operating over the extended temperature range from -40°C up to + 85°C. All onboard components are specially selected for the higher temperature range. For the higher temperatures the desktop processors are not suitable, because the power consumption is higher and the allowable case temperature is lower. The only suitable processor is the Intel® Mobile Pentium®III processor family. These processors are produced with the new 0.18-micron process which have lower power consumption and support higher case temperatures (100°C).

1.6.1.1 Temperature Range and Air Flow

These values have been measured with typical applications under DOS and Windows NT 4.0. In worst case situations the values and the temperature range must be reduced accordingly. For all situations the maximum case temperature of the Mobile Pentium III processor must be below 100°C. This temperature value can be measured with the onboard remote temperature sensor. In instances of overtemperature the hardware monitor will reduce the processor clock to lower the generated power.

Table 1-5: Typical Temperature Range and Required Air Flow

Heat Sink Version	Range	400 MHz	500 MHz	700 MHz
4HP	0°C - 60°C	0 m/s	0 m/s	0 m/s
	-25°C - 75°C	0 m/s	0 m/s	*TBD* m/s
	-40°C - 85°C	0.6 m/s	1.0 m/s	*TBD* m/s
8HP	0°C - 60°C	0 m/s	0 m/s	0 m/s
	-25°C - 75°C	0 m/s	0 m/s	*TBD* m/s
	-40°C - 85°C	0 m/s	0.6 m/s	*TBD* m/s

0 m/s air flow means standard convection cooling with the board in an upright position. An airflow of 1 m/s is a typical value for a standard *PEP* ASM 4 rack (3U CompactPCI rack with 1U cooling fans). For other racks or housings the available airflow will be different. The maximum ambient temperature must be recalculated and / or measured for such environments. For the calculation of the maximum ambient temperature the processor case temperature must never exceed 100°C. The maximum heatsink temperature depends on the physical characteristics of the heatsink and thermal connection to the processor. To ensure that the heatsink temperature does not exceed its limits an airflow may be needed for a given ambient temperature. Heatsink temperature is measured at the top of the heatsink base, closest to the processor.

Important Warning concerning overheating follows on next page.

Important:

It is the responsibility of the end user to ensure that the processor case temperate never exceeds 100° Celsius in order to protect the board against overheating. Permanent overheating can damage the board.

If the temperature on the processor die is greater than 100°C the maximum ambient temperature must be reduced or an external airflow must be provided by means of an additional fan.

1.7 Software Support

Real-time operating systems such as QNX®, VxWorks®, and others are supported. The standard PC features supported by the BIOS also allow for PC operating systems such as Linux®, MS-DOS®, Windows 9X®, Windows 2000®, Windows NT 4.0® (Embedded).

1.8 Applied Standards

1.8.1 CE Compliance

The *PEP Modular Computers'* CompactPCI systems comply with the requirements of the following CE-relevant standards:

- Emission EN50081-1
- Immission EN50082-2
- Electrical Safety EN60950

1.8.2 Mechanical Compliance

- Mechanical Dimensions IEEE 1101.10

1.8.3 Environmental Tests

- Vibration/Broad-Band Random Vibration IEC68-2-6 IEC68-2-64 (3U boards)
- Permanent Shock IEC68-2-29
- Single Shock IEC68-2-27

1.9 Related Publications

1.9.1 CompactPCI Systems/Boards

- CompactPCI Specification, V. 2.0, Rev. 3.0

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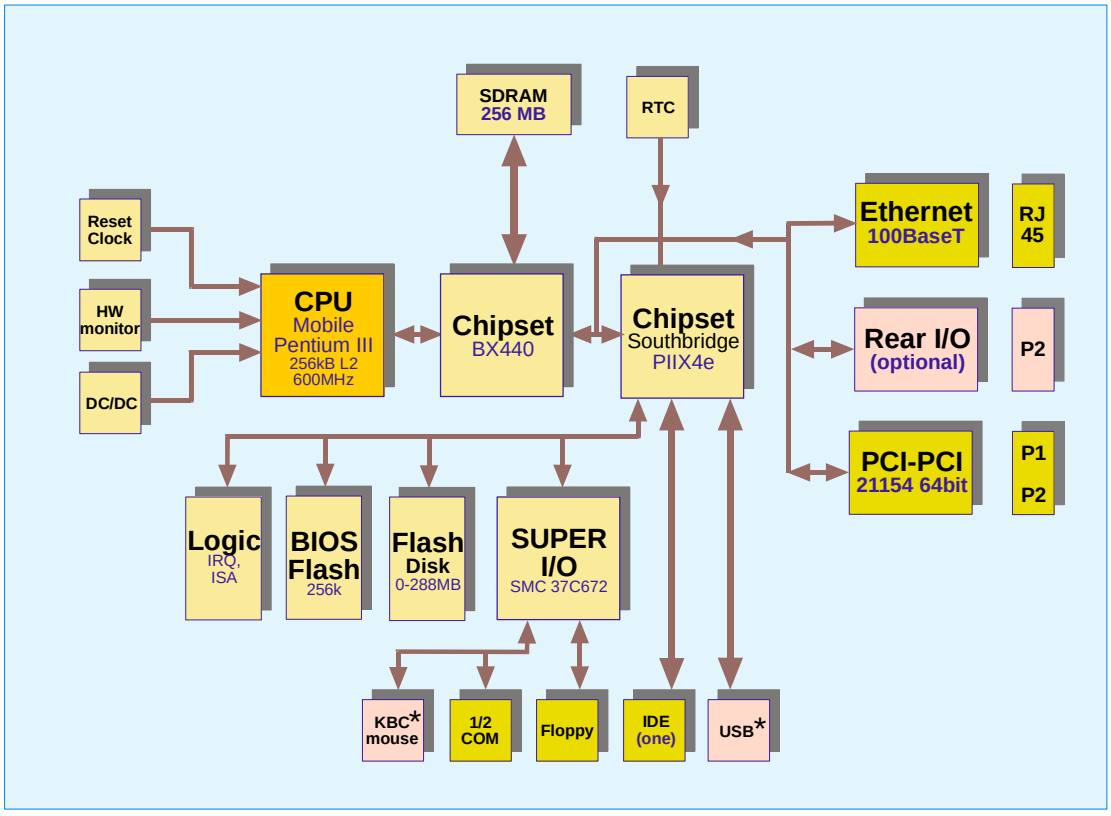
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2. Functional Description and Configuration

2.1 Functional Block Diagram

Figure 2-1: CP301 Functional Block Diagram

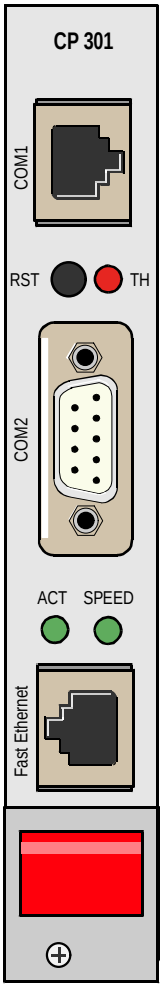


Key

The pink boxes signify features/functionality associated with the optional Rear I/O module, these optional features are additionally highlighted with an asterisk*

2.2 Front Panel

Figure 2-2: CP301 Front Panel



The front panel includes one LED placed under the serial interface connector (“Board LED”) and two LED’s placed over the Ethernet connector (“Ethernet LED”). The functions of the LED’s are as follows:

Board LED:

- TH (red) = Temperature alarm; if ON, an overtemperature has occurred. The CPU clock speed is reduced automatically.

Ethernet LED’s:

- ACT (green) = if ON link is active and transmission is in progress via the Ethernet link.
- SPEED (green) = if ON transmission speed is 100 MBit/s.

2.3 Board Layouts

Figure 2-3: CP301 Board Layout (Front Side)

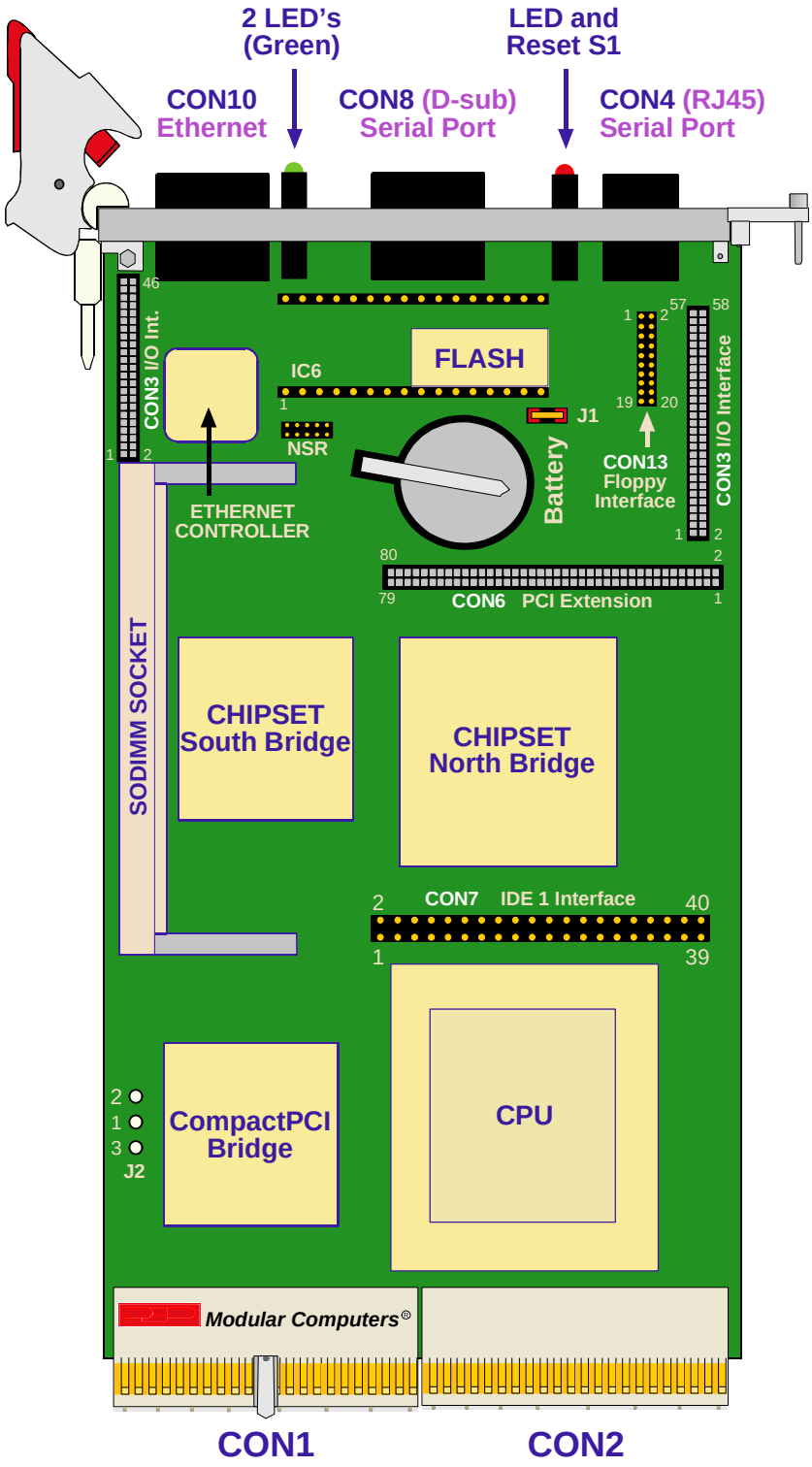
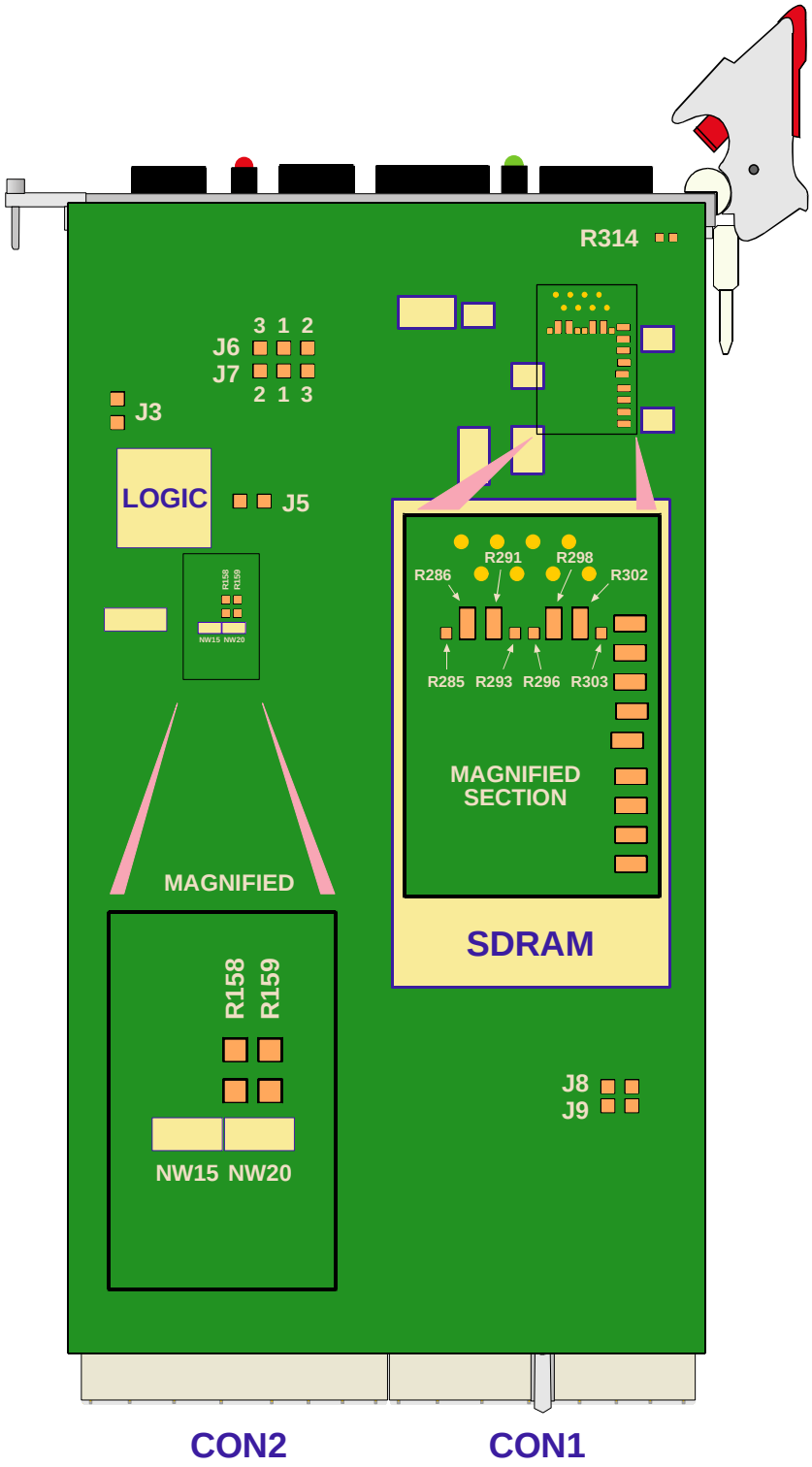


Figure 2-4: CP301 Board Layout (Reverse Side)



2.4 Main Features

The following descriptions highlight the main features of the principal functional blocks of the CP301.

2.4.1 CPU

The CP301 supports the Intel® Mobile Pentium®III Coppermine™ processor family up to 700 MHz with 256 kB L2 on-die cache in a 495-pin BGA2 package. The processor speed is automatically selected. The onboard voltage regulator is automatically programmed by the processor's VID pins to provide the required voltage. All supported onboard memory can be cached.

2.4.2 Memory

The CP301 has two locations for installing memory; up to 128 MB may be soldered with ECC and a further 128 MB may be added by means of the onboard SODIMM socket. The board supports a maximum of 256 MB. All installed memory will be automatically detected, so there is no need to set any jumpers. All PC/100 compliant SDRAM on 144-pin gold SODIMM's are supported by the CP301 board.

Table 2-1: Memory Options Utilizing SODIMM Sockets

Onboard	SODIMM	ECC Support
64MB	--	Enabled
64MB	64 MB	Not supported
64MB	128 MB	Not supported
128MB	--	Enabled
128MB	64 MB	Not supported
128MB	128 MB	Not supported

All memory components and SODIMM's used with this board must comply with the following PC SDRAM specifications:

- PC SDRAM Specification PC100
- PC Serial Presence Detect Specification

2.4.3 Interrupts

Two enhanced 8259-style interrupt controllers provide a total of fifteen interrupt inputs with features which include level and edge-triggered inputs, fixed and rotating priorities and individual input masking. Interrupt sources include: Counter/timers, serial I/O, RTC, keyboard/mouse, printer, floppy disk, EIDE interfaces and four interrupt sources on the CompactPCI backplane.

2.5 Peripherals

The following standard peripherals are available on the CP301 board:

- *Real-Time Clock*

  The real-time clock performs time-keeping functions and includes 256 bytes of general purpose battery-backed CMOS RAM. Features include an alarm function, programmable periodic interrupt and a 100-year calendar. All battery-backed CMOS RAM data remains stored in an additional EEPROM. This prevents data loss.

- *Counter/Timer*

  Three 8254-style counter/timers are included on the CP301 as defined for the PC/AT.

2.5.1 Watchdog Timer

A watchdog timer is provided, which forces an IRQ5, NMI or Reset condition (configurable in the watchdog register). The watchdog time can be programmed in 12 steps ranging from 125 msec up to 256 seconds. If the watchdog timer is enabled, it cannot be stopped.

2.5.2 Battery

The CP301 is provided with a 3.0V “coin cell” lithium battery for the RTC.

To replace the battery please proceed as follows:

- Turn off power
- Remove the battery
- Place the new battery in the socket.
- Make sure that you insert the battery the right way round. The plus pole must be on the top!

The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer. Suitable batteries include the VARTA CR2025 and PANASONIC BR2020

Important notes concerning the battery appear on the next page

Important

- Care must be taken to ensure that the battery is correctly replaced.
- The battery should be replaced only with an identical or equivalent type recommended by the manufacturer.
- Dispose of used batteries according to the manufacturer's instructions.
- The typical life expectancy of a 170 mAh battery (VARTA CR2025) is 4 - 5 years with an average on-time of 8 hours per working day at an operating temperature of 30°C. However, this typical value varies considerably because the life expectancy is dependent on the operating temperature and the standby time (shutdown time) of the system in which it operates.
  To ensure that the lifetime of the battery has not been exceeded it is recommended to exchange the battery after 3 - 4 years.

2.5.3 Reset

The CP301 is automatically reset by a precision voltage monitoring circuit that detects a drop in voltage below the acceptable operating limit of 4.725 V for the 5V line and below 3.0V for the 3.3V line, or in the event of a power failure of the DC/DC converter. Other reset sources include the watchdog timer and local push-button switch. The CP301 responds to any of these sources by initializing local peripherals and issuing the PCIRST* signal on the CompactPCI bus.

The CP301 has a variety of reset options:

- Front panel push button
- Watchdog
- Backplane reset (PRST input)
- Power control (5V, 3.3V and CPU core voltage)

2.5.4 SMBus Devices

The CP301 provides a System Management Bus (SMBus) for access to several system monitoring and configuration functions. The SMBus consists of a two-wire I2C bus interface. The following table describes the function and address of every onboard SMBus device.

Table 2-2: SMBus Device Addresses

Device	SMB Address
PIIX4 slave port	0001000Xb
Temperature sensor MAX1617	0011000Xb
Hardware Monitor LM81	0101100Xb
EEPROM	1010XXXXb

2.5.5 Thermal Management / System Monitoring

The LM81 can be used to monitor several critical hardware parameters of the system, including power supply voltages, fan speeds and temperatures; all of which are very important for the proper operation and stability of a high-end computer system. The LM81 provides an I2C™ serial bus interface.

The voltages of the onboard power supply (+12 V, -12V, +5V, +3.3V, +1.5V, Vcore) are supervised. The onboard hardware monitor is able to detect the CPU fan speed and an external fan speed in revolutions per minute (RPM). The presence of the fans is automatically detected.

The integrated MAX1617 temperature sensors monitor the CPU temperature to make sure that the system is operating at a safe temperature level. If the temperature is too high, the sensors automatically reduces the CPU clock frequency, depending on the mode chosen in the BIOS set.

2.5.6 Serial EEPROM

A serial EEPROM is provided, organised into 4 blocks with 256 bytes per block (24LC08). This EEPROM is connected to the I2C™ bus provided by the PIIX4E.

Table 2-3: EEPROM Address Map

Address	Function
1010000xb	SODIMM SPD
1010001xb	Onboard SPD
1010010xb	Not available
1010011xb	Not available
1010100xb	VxWorks parameter (24LC08)
1010101xb	Free for user purposes (24LC08)
1010110xb	Free for user purposes (24LC08)
1010111xb	CMOS backup (24LC08)

It is strongly recommended that users access only the two free EEPROM banks

2.5.7 Flash Memory

There are two Flash devices available as described below, one for the BIOS and one 32-pin socket for a flexible Flash configuration.

1. BIOS Flash

The CP301 uses a 256 kB flash memory to store BIOS firmware. It can be updated as new versions of the BIOS become available. You may easily upgrade your BIOS using the AWARD *awdflash* utility .

2. Socket Memory

Different flash module versions are available. In order to achieve flexibility with low cost the flash memory is not soldered, but connected via a special module from M-Systems (DiskOnChip™ 2000).

- Standard flash memory of up to 512 KB in a 32-pin DIL package
  - AMD29F010
  - AMD29F040
- Standard EEPROM memory in a 32-pin DIL package
  - AMD27C010
  - AMD27C020
- DiskOnChip™ flash memory:
  - 8 - 288 MB

For higher flash memory capacity it is recommended to use an ATA flash disk.

2.5.8 PCI- to-PCI Bridge

The Intel® 21154 bridge is a 64-bit 33 MHz PCI-to-PCI bridge device. It supports up to seven CompactPCI loads through a passive backplane.

The 21154 is a second generation PCI-to-PCI bridge and is fully compliant with the PCI Local Bus Specification Rev. 2.1. The 64-bit interface interoperates transparently with either 64-bit or 32-bit devices.

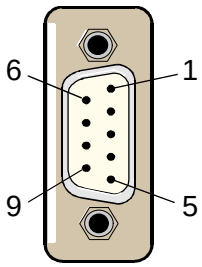
The PC-to-PCI bridge allows the primary and secondary PCI bus to operate concurrently. A master and target on the same PCI bus can communicate while the other PCI bus is busy.

2.6 Board Interfaces

2.6.1 Serial Ports

The CP301 has two serial ports; one, CON8, is a 9-pin D-sub, the other an 8-pin RJ45 connector.

Figure 2-5: D-sub 9-pin Male Connector



2.6.1.1 Serial Port Connector CON8 (D-sub) Pinout

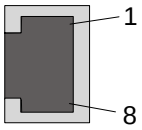
The serial port male connector CON8 allows the connection of RS232 devices to the CP301 board.

Table 2-4: Serial Port Connector CON8 (D-sub) Pinout

D-sub 9	Signal	Function	In/Out
1	DCD	Data carrier detect	In
2	RXD	Receive data	In
3	TXD	Transmit data	Out
4	DTR	Data terminal ready	Out
5	GND	Signal ground	--
6	DSR	Data send request	In
7	RTS	Request to send	Out
8	CTS	Clear to send	In
9	RI	Ring indicator	In

2.6.1.2 Serial Port Connector CON4 (RJ45) Pinout

Figure 2-6: RJ45 8-pin Connector



The serial port RJ45 connector CON4 allows the connection of RS232 devices to the CP301 board.

Table 2-5: Serial Port Connector CON4 (RJ45) Pinout

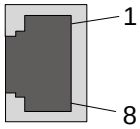
RJ45	Signal	Function	In/Out
1	DSR	Data send request	In
2	RTS	Request to send	Out
3	GND	Signal ground	--
4	TXD	Transmit data	Out
5	RXD	Receive data	In
6	DCD	Data carrier detect	In
7	CTS	Clear to send	In
8	DTR	Data terminal ready	Out

2.6.2 Fast Ethernet

The CP301 board includes a 10BASE-T/100BASE-TX network solution based on the Intel® 82559 Fast Ethernet PCI Bus Controller. The controller contains two receive and transmit FIFO buffers that prevent data overruns or underruns while waiting for access to the PCI bus.

Two LED's monitor network conditions. The Boot from LAN feature is supported, for details please refer to section 4.5, BIOS Features Setup, in chapter 4.

Figure 2-7: Ethernet/Fast Ethernet 8-pin Connector



The Ethernet connector is realized as an RJ45 twisted-pair connector. The interface provides automatic detection and switching between 10Base-T and 100Base-TX data transmission.

2.6.2.1 Ethernet RJ45 Connector CON10 Pinout

The CON10 supplies the 10Base-TX/100Base-TX interface to the Ethernet controller.

Table 2-6: Ethernet RJ45 Connector CON10 Pinout

RJ45	Signal	Function
1	TX+	Transmit +
2	TX-	Transmit -
3	RX+	Receive +
4	NC	--
5	NC	--
6	RX-	Receive -
7	NC	--
8	NC	--

2.6.3 Ethernet LED Status

Green: ACT: This LED monitors network connection and activity. The LED lights up when network packets are sent or received through the RJ45 port. When this LED is not lit it means that either the computer is not sending or receiving network data or that the cable connection is faulty.

Green: SPEED: This LED lights up to indicate a successful 100Base-TX connection. When not lit the connection is operating at 10Base-T.

2.6.4 Fan Power Supply

A fan for CPU cooling may be connected through the power connector J2.

Table 2-7: Fan Power Supply

J2	Function
1	GND
2	+5V or +12V Please see table 2-16 on page 2-30 for necessary jumper setting
3	Sense input

2.6.5 EIDE Interface

The two EIDE interfaces support PIO mode 4 with transfers up to 14 MB per second and Bus Master Ultra-DMA 33 transfer up to 33 MB per second. The EIDE controller can sustain a maximum transfer rate of 33 MB per second between the EIDE drive buffer and PCI.

There are two independent EIDE ports available (a primary onboard and a secondary on the Rear I/O). The primary EIDE interface is a 40-pin, 2-row male connector AT standard interface for an EIDE HardDisk.

Each EIDE interface provides support for two devices (one master and one slave). All HardDisks can be used in cylinder head sector (CHS) mode with the BIOS also supporting the logical block addressing (LBA) mode.

Important

Each EIDE interface supports a maximum of two devices connected in the master-slave mode. To configure the first as a master disk and the second as a slave disk, please refer to the HardDisk manufacturer's documentation.

EIDE connector pinout appears on the following page

2.6.5.1 EIDE Connector CON7

The following table sets out the pinout of the CON7 connector, giving the corresponding signal names. The maximum length of cable that may be used is 35 cm. The colored stripe on a ribbon cable (pin 1) from the EIDE1 port should face towards the SODIMM socket.

Table 2-8: Pinout of AT Standard Connector CON7

Pin	Signal	Function	In/Out
1	IDERESET	Reset HD	Out
2	GND	Ground signal	--
3	HD7	HD data 7	In/Out
4	HD8	HD data 8	In/Out
5	HD6	HD data 6	In/Out
6	HD9	HD data 9	In/Out
7	HD5	HD data 5	In/Out
8	HD10	HD data 10	In/Out
9	HD4	HD data 4	In/Out
10	HD11	HD data 11	In/Out
11	HD3	HD data 3	In/Out
12	HD12	HD data 12	In/Out
13	HD2	HD data 2	In/Out
14	HD13	HD data 13	In/Out
15	HD1	HD data 1	In/Out
16	HD14	HD data 14	In/Out
17	HD0	HD data 0	In/Out
18	HD15	HD data 15	In/Out
19	GND	Ground signal	--
20	N/C	--	--
21	IDEDRQ	DMA request	In
22	GND	Ground signal	--
23	IOW	I/O write	Out
24	GND	Ground signal	--

Table continued on following page

Table 2-8: Pinout of AT Standard Connector CON7

Pin	Signal	Function	In/Out
25	IOR	I/O read	Out
26	GND	Ground signal	--
27	IOCHRDY	I/O channel ready	In
28	GND	Ground signal	--
29	IDEDACKA	DMA Ack	Out
30	GND	Ground signal	--
31	IDEIRQ	Interrupt request	In
32	N/C	--	--
33	A1	Address 1	Out
34	N/C	--	--
35	A0	Address 0	Out
36	A2	Address 2	Out
37	HCS0	HD select 0	Out
38	HCS1	HD select 1	Out
39	LED	LED driving	In
40	GND	Ground signal	--

2.6.6 Floppy Drive Interface

The onboard floppy disk controller supports either 5.25 inch or 3.5 inch (1.44 or 2.88 MB) floppy disks. A 20-pin male connector provides the signals for an optional floppy-drive that can be installed by means of a special adapter.

2.6.6.1 Floppy Disk Connector CON13

Table 2-9: Floppy Disk Connector CON13 Pinout

Pin	Signal	Function	In/Out
1-4	GND	Ground signal	--
4	HDSEL	Head select	Out
6	DSKCH	Disk change	In
7	WP	Write protect	In
8	RDATA	Read data	In
9	WGAT	Write enable	Out
10	TRK0	Track 0 signal	In
11	STEP	Step pulse	Out
12	WDAT	Write data	Out
13	MTR1	Motor 1 enable	Out
14	DIR	Step direction	Out
15	DS1	Driver select 1	Out
16	DS0	Driver select 0	Out
17	INDEX	Index pulse	In
18	MTR0	Motor 0 enable	Out
19	DRVDEN1	Drive and media select	Out
20	DRVDEN0	Drive and media select	Out

Note:

The adapter must be mounted directly onto the floppy drive. There is therefore no necessity for an intermediate cable between the floppy drive and the adapter.

2.6.7 CompactPCI Bus Interface(s)

The complete CompactPCI connector configuration comprises two connectors named J1 and J2

Their function is as follows:

- J1/J2: 64-bit CompactPCI interface with PCI bus signals, arbitration, clock and power
- J2 has optional Rear I/O interface functionality.

The board is capable of driving up to seven CompactPCI slots, with individual arbitration and clock signals. In addition to standard CompactPCI system functionality, the CP301 also supports Hotswap capability which means that hotswappable boards can be removed from or installed in the system whilst it is running.

The CP301 is designed for CompactPCI bus architecture. The CompactPCI standard is electrically identical to the PCI local bus. However, these systems are enhanced to operate in rugged industrial environments and to support multiple slots.

CompactPCI connector pinouts appear on the following page.

2.6.7.1 Compact PCI Connectors CON1 and CON2 Pinouts

The CP301 is provided with two 2 mm x 2 mm pitch female CompactPCI bus connectors, J1 and J2.

Table 2-10: CompactPCI Bus Connector CON1 (J1) Pinout

Pin	Row A	Row B	Row C	Row D	Row E	Row F
25	5V	REQ64*	ENUM*	3.3V	5V	GND
24	AD[1]	5V	V(I/O)	AD[0]	ACK64*	GND
23	3.3V	AD[4]	AD[3]	5V	AD[2]	GND
22	AD[7]	GND	3.3V	AD[6]	AD[5]	GND
21	3.3V	AD[9]	AD[8]	M66EN*	C/BE[0]*	GND
20	AD[12]	GND	V(I/O)	AD[11]	AD[10]	GND
19	3.3V	AD[15]	AD[14]	GND	AD[13]	GND
18	SERR*	GND	3.3V	PAR	C/BE[1]*	GND
17	3.3V	RSV	RSV	GND	PERR*	GND
16	DEVSEL	GND	V(I/O)	STOP*	LOCK*	GND
15	3.3V	FRAME*	IRDY*	GND	TRDY*	GND
12-14	Key Area					
11	AD[18]	AD[17]	AD[16]	GND	C/BE[2]*	GND
10	AD[21]	GND	3.3V	AD[20]	AD[19]	GND
9	C/BE[3]*	IDSEL	AD[23]	GND	AD[22]	GND
8	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND
7	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND
6	REQ*	GND	3.3V	CLK	AD[31]	GND
5	BRSVP1A5	BRSVP1B5	RST*	GND	GNT*	GND
4	BRSVP1A4	GND	V(I/O)	INTP	INTS	GND
3	INTA*	INTB*	INTC*	5V	INTD*	GND
2	TCK	5V	TMS	TDO	TDI	GND
1	5V	-12V	TRST*	+12V	5V	GND

Table 2-11: 64-bit CompactPCI Bus Connector CON2 (J2) Pinout

Pin	Row Z	Row A	Row B	Row C	Row D	Row E	Row F
22	GND	GA4	GA3	GA2	GA1	GA0	GND
21	GND	CLK6	GND	RSV	RSV	RSV	GND
20	GND	CLK5	GND	RSV	GND	RSV	GND
19	GND	GND	GND	RSV	RSV	RSV	GND
18	GND	RSV	RSV	RSV	GND	RSV	GND
17	GND	RSV	GND	PRST#	REQ6#	GNT6#	GND
16	GND	RSV	RSV	DEG#	GND	RSV	GND
15	GND	RSV	GND	FAL#	REQ5#	GNT5#	GND
14	GND	AD[35]	AD[34]	AD[33]	GND	AD[32]	GND
13	GND	AD[38]	GND	V(I/O)	AD[37]	AD[36]	GND
12	GND	AD[42]	AD[41]	AD[40]	GND	AD[39]	GND
11	GND	AD[45]	GND	V(I/O)	AD[44]	AD[43]	GND
10	GND	AD[49]	AD[48]	AD[47]	GND	AD[46]	GND
9	GND	AD[52]	GND	V(I/O)	AD[51]	AD[50]	GND
8	GND	AD[56]	AD[55]	AD[54]	GND	AD[53]	GND
7	GND	AD[59]	GND	V(I/O)	AD[58]	AD[57]	GND
6	GND	AD[63]	AD[62]	AD[61]	GND	AD[60]	GND
5	GND	C/ BE[5]#]	GND	V(I/O)	C/ BE[4]#]	PAR64	GND
4	GND	V(I/O)	RSV	C/ BE[7]#]	GND	C/ BE[6]#]	GND
3	GND	CLK4	GND	GNT3#	REQ4#	GNT4#	GND
2	GND	CLK2	CLK3	SYSEN#	GNT2#	REQ3#	GND
1	GND	CLK1	GND	REQ1#	GNT1#	REQ2#	GND

2.6.8 Rear I/O Interface

The CP301 board provides optional rear I/O connectivity for peripherals for special compact systems. Some standard PC interfaces are implemented and assigned to the front panel and to the rear connector J2.

When the rear I/O module is used, the signals of some of the main board/front panel connectors are routed to the module interface. Thus the rear I/O module makes it much easier to remove the CPU in the rack as there is practically no cabling on the CPU board.

For this configuration two versions are available. One with 64-bit/33 MHz CompactPCI and reduced rear I/O functionality and one with 32-bit/33 MHz and some rear I/O peripherals.

For the system rear I/O feature a special backplane is necessary. The CP301 with rear I/O is compatible with all standard CompactPCI passive backplanes with rear I/O support on the system slot.

The CP301 rear I/O provides the following interfaces, all signals are available on J2 only when the board is ordered for rear I/O functionality:

32-bit CompactPCI and Rear I/O

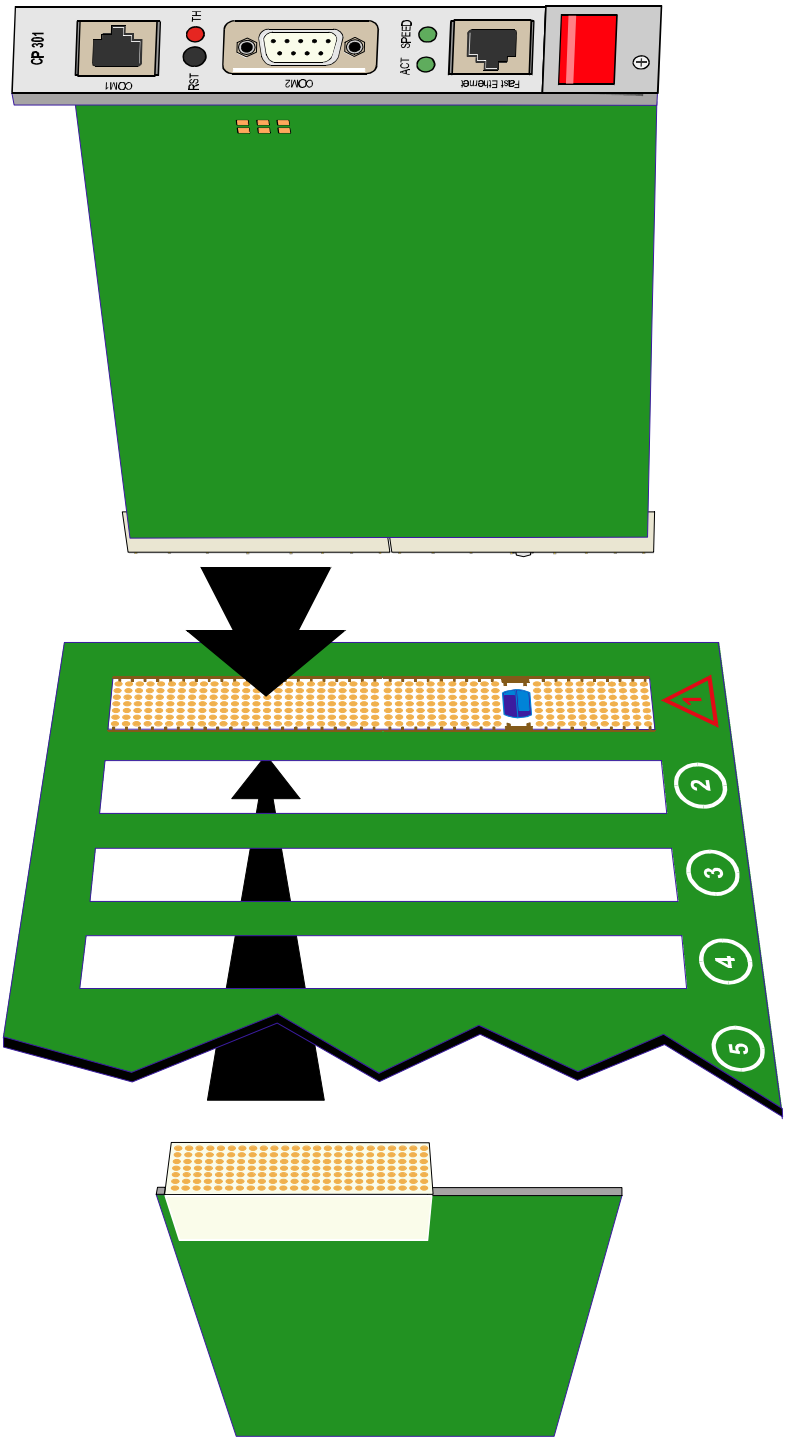
- 32-bit/33 MHz CompactPCI
- PS/2 keyboard
- PS/2 mouse
- Two USB ports
- Ethernet port without LED
- Two COM ports
- Second EIDE port
- Fan control input

The following ports may be used either for rear or front I/O, the combination of both rear and front is not possible.

- Ethernet port without LED
- Two COM ports
- Second EIDE port

2.6.8.1 Rear I/O Configuration Illustration

Figure 2-8: CP301 Rear I/O Configuration



2.6.8.2 Optional Rear I/O interface on Compact PCI Connector CON2

The CP301 conducts a wide range of I/O signals through the rear I/O connector J2.

Note:

If the rear I/O feature is selected the PCI interface is only 32-bit. For the 3U rear I/O a special backplane is necessary.

Table 2-12: Rear I/O CompactPCI Bus Connector CON2 (J2) Pinout

Pin	Z	A	B	C	D	E	F
22	GND	GA4	GA3	GA2	GA1	GA0	GND
21	GND	CLK6	GND	TDN 1)	RDN 1)	RDP 1)	GND
20	GND	CLK5	GND	TDP 1)	GND	VCC 1)	GND
19	GND	GND	GND	RSV 5)	RSV 5)	+3.3V 1)	GND
18	GND	KDAT 1)	UV0- 1)	UV1+ 1)	RSV 5)	+3.3V 1)	GND
17	GND	KCLK 1)	N/A 3)	PRST	REQ6	GNT6	GND
16	GND	PMDAT 1)	UV0+ 1)	DEG	GND	UV1- 1)	GND
15	GND	PMCLK 1)	N/A 3)	FAL	REQ5	GNT5	GND
14	GND	2RIN 2)	2DSR 2)	2RTS 2)	N/A 3)	2CTS 2)	GND
13	GND	2RXD 2)	FANSENSE (GND)	N/A 3)	2DTR 2)	2DCD 2)	GND
12	GND	1DSR 2)	1RTS 2)	1CTS 2)	N/A 3)	2TXD	GND
11	GND	1DTR 2)	GND	IDEDB9 (VIO) 4)	1DCD 2)	1RIN 2)	GND
10	GND	IDEDB8 4)	IDERST 4)	1TXD 2)	IDEDB10 (GND) 4)	1RXD 2)	GND
9	GND	IDEDB6 4)	IDEDB7 (GND) 4)	IDEDB4 (VIO) 4)	IDEDB5 4)	IDEDB11 4)	GND
8	GND	IDEDB3 4)	IDEDB12 4)	IDEDB2 4)	GND	IDEDB1	GND
7	GND	IDEDB14 4)	IDEDB0 (GND) 4)	IDEDB15 (VIO) 4)	IDEDRQB 4)	IDEIOWB	GND
6	GND	IDEIORB 4)	ICHRDYB 4)	IDACKB 4)	IDEDB13 (GND) 4)	IDEIRQB 4)	GND
5	GND	IDEAB1 4)	GND	IDAB0 (VIO) 4)	IDEAB2 4)	RSV 5)	GND
4	GND	VIO	VCC 1)	IDECSB0 4)	GND	IDECSB1 4)	GND
3	GND	CLK4	GND	GNT3	REQ4	GNT4	GND
2	GND	CLK2	CLK3	SSYSEN	GNT2	REQ3	GND
1	GND	CLK1	GND	REQ1	GNT1	REQ2	GND

Table legend follows on next page

Legend for table on preceding page**:**

1) Ethernet, SMBUS, Keyboard, Mouse, USB and Power (64-bit and rear I/O possible)

2) COM1, COM2 (only 32-bit and rear I/O)

3) These signals are not available on this board

4) EIDE Port (only 32-bit and rear I/O)

5) Reserved

The greyed table cells indicate the power grouping

2.6.8.3 Rear I/O Jumper Setting

Rear I/O interfaces are only available on Rear I/O versions of the board.

In order to implement the system Rear I/O feature, a system slot Rear I/O backplane is necessary. This backplane must comply with the CompactPCI Specification PICMG 2.0 R3.0, October 1999.

Warning:

If the board is ordered for 64-bit CompactPCI the Rear I/O feature is **not supported**. The Rear I/O jumpers and resistors must not be configured for Rear I/O. The setting of the Rear I/O jumpers and resistors **may result in damage to your board or system**.

Ethernet Interface

Ethernet signals are available on J2 when the board is ordered for Rear I/O configuration. To configure the Ethernet port for Rear I/O requires the installation of zero ohm resistors on the board to connect the signals to the J2 connector.

Note:

The combination of both front and Rear I/O is not supported.

VGA Interface

VGA signals are not available as standard when the board is ordered for Rear I/O configuration.

Serial Interface COM1 and COM2

Only one interface may be used (Rear I/O or front I/O). If the Rear I/O interface is enabled the drivers for the COM1 and COM2 port on the CP302 IDE2 module must be disabled.

Keyboard/Mouse Interface

All PS2 connectors are electrically identical. Due to this it is not possible to use a mouse at the front I/O and a second mouse at the Rear I/O port at the same time.

USB Interface

There are two independent USB interfaces available, one port is routed to the 4-pin front I/O connector. This port may also be used on the Rear I/O interface. The second port is only available on the Rear I/O connector.



Note:

The USB 1 port is electrically identical and not separated. Do not connect devices at both connectors (front I/O and Rear I/O) at the same time.

2.7 Jumper Description

2.7.1 External BIOS

It is possible to redirect the first CPU fetch from the onboard flash to the Flash socket. If jumper J1 is open, the board boots from the BIOS in the onboard flash memory. When J1 is closed, the board boots from the socket flash.

Table 2-13: External BIOS Setting

J1	Function	Comment
Closed	External Bios	Use this setting only if the onboard flash does not work.
Open	Internal Bios	Normal boot from the onboard BIOS

2.7.2 Memory Type Selection

This solder jumper selects the memory type to be installed on the flash socket IC6.

Table 2-14: Memory Type Selection

J6	J7	Memory type	Comment
1-2	1-2	SRAM with 256 kB or 512 kB	--
1-3	1-3	All DiskOnChip™, Flash and EPROM types up to 4 Mbit	Default

2.7.3 Flash Type Selection

This solder jumper selects the flash type to be installed on the flash socket IC6.

Table 2-15: Flash Type Selection

J3	Function	Comment
Closed	4 Mbit flash type	--
Open	2 Mbit flash type	Default

2.7.4 Fan Power Supply Selection

The voltage for the CPU cooling fan can be configured using jumpers J8 and J9

Table 2-16: Fan Power Supply Selection

J9	J8	Function
Closed	Open	+5V
Open	*Closed*	*+12V*

Default setting is shown in italics

2.7.5 PCI VI/O setting

The CP301 provides for either a 5V or 3.3V PCI signaling environment.

The BVI/O power jumpers on the board are used to power the buffers on the peripheral boards and the PMC interface. The BVI/O does not provide power to the CompactPCI interface. The CompactPCI VI/O must be configured via the backplane.

Table 2-17: PCI VI/O setting

Board VI/O setting	R158	R159
5V default	Open	Closed
3.3V	Closed	Open

2.7.6 Shorting Chassis GND (Shield) to Logic GND

The front panel including the front panel connectors are isolated to the logic ground. This zero Ohm resistor enables connection between the chassis GND and logic GND.

Table 2-18: Shorting Chassis GND (Shield) to Logic GND

R314	Function
Open	*Connectors are isolated to logic GND*
Short	Connectors are connected to logic GND and chassis GND

The default setting is indicated by italics.

2.7.7 Jumper Setting for Rear I/O

Rear I/O interfaces are only available on Rear I/O versions of the board.

In order to implement the system Rear I/O feature, a system slot Rear I/O backplane is necessary. This backplane must comply with the CompactPCI Specification PICMG 2.0 R3.0, October 1999.

Warning:

If the board is ordered for 64-bit CompactPCI the Rear I/O feature is **not supported**. The Rear I/O jumpers and resistors must not be configured for Rear I/O. The setting of the Rear I/O jumpers and resistors **may result in damage to your board or system**.

Ethernet Interface

Ethernet signals are available on J2 when the board is ordered for Rear I/O configuration. To configure the Ethernet port for Rear I/O requires the installation of zero ohm resistors on the board to connect the signals to the J2 connector.

Table 2-19: Ethernet Interface Configuration

Configuration	Ethernet Front I/O	Ethernet Rear I/O
R286, R291, R298, R302	Closed	Open
R285, R293, R296, R303	Open	Closed

Note:

The combination of both front and Rear I/O is not supported.

2.7.8 Reserved Jumpers

Jumper J5 is reserved for future configurations

2.8 Memory Map

The CP301 board uses the standard AT ISA memory map.

The following table displays the memory map for the first megabyte:

Table 2-20: Memory Map for the 1st Megabyte

Memory Range (Hex.)	Size	Function
0xE0000-0xFFFFF	**128k**	BIOS implemented in Flash EPROM Reset vector FFFF0h
0xD0000-0xDFFFF	**8k/64k**	Flash disk: min. 8 kB, max. 64 kB
0xC8000-0xCFFFF	**32k**	Free
0xC0000-0xC7FFF	**32k**	BIOS of the VGA card
0xA0000-0xBFFFF	**128k**	Normally used as video RAM as follows: CGA video: 0xB8000-0xBFFFF Monochrome video: 0xB0000-0xB7FFF EGA/VGA video: 0xA0000-0xAFFFF
0x00000-0x9FFFF	**640k**	DOS reserved memory space
0x00000-0x00501	--	BIOS data area and interrupt space

I/O Address Map appears on the following page

Table 2-21: I/O Address Map

Address Range (Hex.)	Device
000,00F	DMA controller #1
020,021	Interrupt controller #1
022,02F	Reserved
040,043	Timer
060,063	Keyboard interface
070,071	RTC port
080,08F	DMA page register
0A0,0A	Interrupt controller #2
0C0,0DF	DMA controller #2
0E0,0EF	Reserved
0F0,0FF	Math coprocessor
170,17F	Hard disk secondary
1F0,1FF	Hard disk primary
278,27F	Parallel port LPT2
280	Watchdog trigger
281	Onboard reset
282	Watchdog time
283	Rear I/O control
284	Interrupt routing
286	I/O status
288	Board version
289	Hardware index
28A	Jumper status
28B	Logic index
28C	PCI Interrupt routing
28E	Memory management
28F	Flash Socket Page
2E8,2EF	Serial port COM4
2F8,2FF	Serial port COM2
378,37F	Parallel printer port LPT1
3BC,3BF	Parallel printer port LPT3
3E8,3EF	Serial port COM3
3F0,3F7	Floppy Disk + Super-I/O #1 Com.
3F8,3FF	Serial port COM1

2.9 Special Registers Description

The following registers are special registers for the CP301 to watch the onboard hardware special features and the CompactPCI control signals.

Normally, only the system BIOS uses these registers, but they are documented here for application use as required. Take care when modifying the contents of these registers as the system BIOS may be relying on the state of the bits under its control.

2.9.1 Watchdog

The CP301 has one watchdog timer. This timer is provided with a programmable timeout ranging from 125 msec to 256 sec. Failure to retrigger the watchdog timer within a set time period results in a system reset, NMI or an interrupt. These can be configured via the register 0x284.

To enable the watchdog bit 4 of the register 0x282 must be set.

With a write access to the register 0x280 the watchdog is re-triggered. Once the watchdog is enabled, it must be continuously strobed within the terminal count period to avoid expiry of the Watchdog.

2.9.1.1 Watchdog Trigger

A write access triggers the watchdog.

The I/O location for the watchdog trigger is 0x280.

Watchdog Timer section appears on the following page

2.9.1.2 Watchdog Timer

The CP301 has one watchdog timer with a programmable timeout ranging from 125 msec. to 256 sec.

The I/O location for the watchdog configuration is 0x282.

Table 2-22: Watchdog Configuration

Bits	Type	Default	Function
7-5	R	0	Reserved
4	RW	1	1 = enable watchdog (read and write) 0 = disable watchdog (read only)
3-0	RW	0	The nominal timeout period is 20% longer than the minimum. 0 = 125 msec 1 = 250 msec 2 = 500 msec 3 = 1 sec 4 = 2 sec 5 = 4 sec 6 = 8 sec 7 = 16 sec 8 = 32 sec 9 = 64 sec 10 = 128 sec 11 = 256 sec 12-15 reserved

2.9.2 Reset Control Register

This register controls the reset signal for the Ethernet controller and the VGA-AGP interface. A low signal keeps the chips in the reset mode. The default configuration is high.

The I/O location for the reset control register is 0x281.

Table 2-23: Reset Control Register

Bits	Type	Default	Function
7-2	R	0	Reserved
1	RW	1	Reset VGA-AGP interface 1 = set reset signal high 0 = set reset signal low
0	RW	1	Reset the Ethernet chip 1 = set reset signal high 0 = set reset signal low

2.9.3 Rear I/O Configuration Register

This register is used by the CPU to control the signal path (front I/O or rear I/O) of the two COM ports. The default configuration is the front I/O interface.

The I/O location for the rear I/O register is 283h.

Table 2-24: Rear I/O Configuration Register

Bits	Type	Default	Function
7-1		0	Reserved
2	RW	0	COM 1 and COM 2 port interface 1 = rear I/O interface 0 = front I/O interface
0-1		0	Reserved

2.9.4 Interrupt Configuration Register

The interrupt configuration register holds a series of bits defining the interrupt routing for the watchdog, the power control derate signal and the CompactPCI enumeration signal. If the watchdog timer timesout, it can generate three independent hardware events: reset, NMI and IRQ5 interrupt.

The enumeration signal is generated by a hotswap compatible board after insertion and prior to removal. The system uses this interrupt signal to force software to configure the new board. The derate signal indicates that the power supply is beginning to derate its power output.

The I/O location for the interrupt configuration is 0x284.

Table 2-25: Onboard Interrupt Configuration

Bits	Type	Default	Function
7	--	0	Reserved
6	RW	1	Watchdog LED output 1 = enable red LED 0 = disable red LEDrb
5	--	0	Reserved
4	RW	0	CPCI enum signal IRQ5 routing 1 = enable IRQ5 0 = disable IRQ5
3	RW	0	CPCI derate signal IRQ5 routing 1 = enable IRQ5 0 = disable IRQ5
2	RW	0	Watchdog hardware reset 1 = enable reset 0 = disable reset
1	RW	0	Watchdog IRQ5 routing 1 = enable IRQ5 0 = disable IRQ5
0	RW	0	Watchdog NMI routing 1 = enable NMI 0 = disable NMI

2.9.5 I/O Status

This register describes the local and CompactPCI control signals. The watchdog status bit indicates the status of the watchdog timer. If the timer is not re-triggered within the previously set time period, the bit is set to “0”. The fail signal is an output of the power supply indicating a power supply failure. For the description of the derate and enumeration signals please see the interrupt routing register.

The I/O location for the I/O status is 0x286

Table 2-26: I/O-Status

Bits	Type	Default	Function
7	R	--	Watchdog status 0 = watchdog interrupt
6	R	--	Reserved
5	R	--	Reserved
4	R	--	Reserved
3	R	--	System slot identification 0 = System slot
2	R	--	System enumeration hot swap 0 = new board
1	R	--	Supply fail signal of CPCI (this signal is low active)
0	R	--	Derating signal of CPCI (this signal is low active)

2.9.6 Board ID

This register describes the hardware and the board index.

I/O location 0x288.

Table 2-27: Board ID

Bits	Type	Default	Function
7-0	R	0x32	Board version 0 = reserved 0x30 = CP302 Master version 0x31 = CP302 Slave version 0x32 = CP301 version 0x33 = CP301 customized version

The content of this register is unique for each *PEP* CompactPCI board.

2.9.7 Hardware Index

The hardware index will signal to the software when differences in the hardware require different handling by the software. It starts with the value 0 and will be incremented with each change in hardware as development continues.

I/O location 0x289

Table 2-28: Hardware Index

Bits	Type	Default	Function
7-0	R	--	Revision ID 0 = Index 0000

2.9.8 Jumper Status

This register can be used to read the onboard jumper configuration.

I/O location 0x28A

Table 2-29: Jumper Status

Bits	Type	Default	Function
7	R	1	Boot jumper J1 1 = onboard flash 0 = socket flash
6-3	R	--	Reserved
2	R	--	Rear I/O module status 1 = no rear I/O module plugged in 0 = rear I/O module plugged in
1	R	--	Reserved
0	R	--	Reserved

2.9.9 Logic Version

The logic version register may be used to identify the logic status of the board by software. It starts with the value 0 and will be incremented with each logic update.

I/O location 0x28B

Table 2-30: Logic Version

Bits	Type	Default	Function
7-0	R	--	Logic version 0 = Index 0000

2.9.10 PCI Interrupt Routing

This register is used by the CPU to control the PCI interrupt routing. Every interrupt line of the backplane can be enabled or disabled. The interrupt mask register bits enable the appropriate bits when low, and disable them when high. The default configuration is “all interrupts enabled”.

The I/O location for the PCI interrupt routing is 0x28C.

Table 2-31: PCI Interrupt Routing

Bits	Type	Default	Function
7-4	R	--	Reserved
3	RW	0	P1 INTD
2	RW	0	P1 INTC
1	RW	0	P1 INTB
0	RW	0	P1 INTA

2.9.11 Memory Management of Flash Socket

Flash devices which may be mounted in socket IC6 are accessed in paged mode, up to 512 kB are addressable in total. The page size depends on the setting of the Flash Socket Page Register; the Flash access is 8 pages with 64 kB, 16 pages with 32 kB or 64 pages with 8 kB.

The Memory Management Register should be used to select the individual pages.
The I/O location is 0x28E.

Table 2-32: Memory Management

Bits	Type	Default	Function 8 kB	Function 32 kB	Function 64 kB
7-6	R	--	Reserved	--	--
5	RW	0	Address A18	--	--
4	RW	0	Address A17	--	--
3	RW	0	Address A16	Address A18	--
2	RW	0	Address A15	Address A17	Address A18
1	RW	0	Address A14	Address A16	Address A17
0	RW	0	Address A13	Address A15	Address A16

2.9.12 Flash Socket Page

The Flash Socket Page register is used to select the page size to be addressed. The size can be programmed from 8 kB to 64 kB. The default value is 8 kB which results in the following address window: 0xDE000 - 0xDFFFF.

The I/O location of the flash window setup is 0x28F.

Table 2-33: Flash Socket Page

Bits	Type	Default	Addressable Range in
7-0	RW	0	2 = 64kB 0xD0000 - 0xDFFFF 1 = 32kB 0xD8000 - 0xDFFFF 0 = 8kB 0xDE000 - 0xDFFFF

Note:

The default value for DiskOnChip™ is 8 kB.

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Chapter 3

Installation

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3. Installation

3.1 Board Installation



Caution!

If your board type is not specifically qualified as hotswap capable, please switch off the CompactPCI system before installing the board in a free CompactPCI slot. Failure to do so could endanger your life/health and may damage your board or system.



Note:

Certain CompactPCI boards require bus master and/or rear I/O capability. If you are in doubt whether such features are required for the board you intend to install, please check your specific board and/or system documentation to make sure your system is provided with an appropriate free slot to insert the board.



ESD Equipment!

Your CompactPCI board contains electrostatically sensitive devices. Please observe the necessary precautions to avoid damage to your board:

- Discharge your clothing before touching the assembly. Tools must be discharged before use.
- Do not touch components, connector-pins or traces.
- If working at an anti-static workbench with professional discharging equipment, please do not omit to use it.

Chapters 2 and 4 of this manual describe the hardware and software setup of the CP301 controller board, its CPU and the following related devices:

- serial port COM1 and COM2
- floppy disk interface
- EIDE device interfaces
- Fast Ethernet



PEP Advantage

One or more of the above mentioned mass storage and I/O devices may be connected to your CP301 controller board. However, none of these devices have to be installed for the CP301 to function, as it is designed to be bootstrapped solely from the FLASH device.

3.1.1 Placement of the CP301

The *PEP* CompactPCI system configuration is characterized by the fact that its system slot (slot “1”) is on the right end of the backplane, thus allowing for physical CPU growth (heat-sink, cooling fan etc.) associated with higher-performance processors.



Important!

After having inserted your controller board, please make sure it has been fitted into the system slot.

3.1.2 EIDE Interfaces.

The CP301 board is provided with two EIDE interfaces, a primary onboard and a secondary on the Rear I/O.

The EIDE interfaces each allow installation of up to two devices (one master-slave pair). If installed, the devices are automatically recognized by the BIOS at system “power on”.



Important!

The primary EIDE interface supports a maximum of two devices connected in the master-slave mode. To configure the first as a master disk and the second as a slave disk please refer to the HardDisk manufacturer’s documentation.

Hard-Disk Installation

To install a hard disk, it is necessary to perform the following operations in the given order:

1. Install the hardware;
2. Initialize the software necessary to run the chosen operating system.



Attention!

The incorrect connection of power or data cables may damage your hard disk unit and/or CP301 board.

3.2 Software Installation

The installation of the Ethernet and all other on-board peripheral drivers is described in detail in the relevant Driver Kit files.

3.2.1 Using BIOS Setup on the CP301

The CP301 board is designed as a “headless system”. This means that normally it is used without an operator console.

For entering the BIOS Setup and other diagnostic purposes a terminal emulation software can be attached via a serial null modem cable to the CP301 board. This functionality is provided by the “Award Preboot Agent”, which is integrated into the CP301 BIOS.

Standard BIOS input and output routines are redirected which makes it possible to use all software including BIOS, BIOS Setup, typical bootstrap loaders and MS-DOS. In addition MS-DOS applications, which do NOT write directly to the VGA memory, will work with the Preboot Agent.

Either a terminal, terminal emulation software such as “Hyperterm”, or the ”Award Preboot Manager” software may be used as the system console.

Using the “Award Preboot Manager” adds the following functionality:

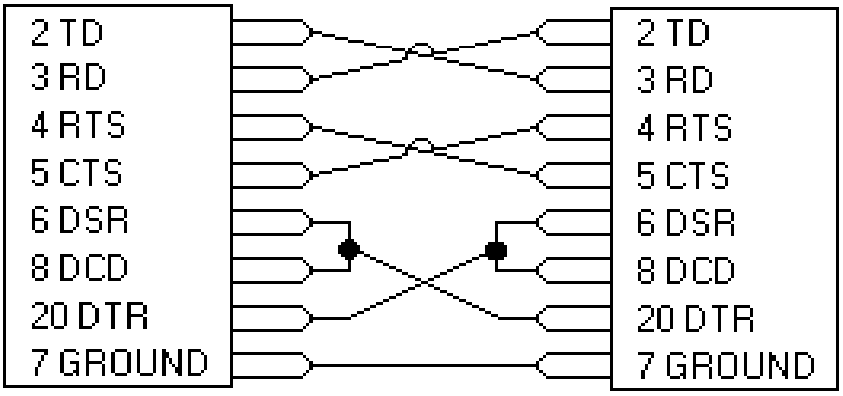
- support for modem handshake lines
- display of postcodes
- emulation of a virtual floppy drive (bootable)
- reboot command via serial line

The default configuration of the CP301 is as follows:

COM1: 19200 baud, 8 data bits, no parity, 1 stop bit, hardware handshake.

A serial null modem cable is required whereby the hardware handshake lines must be connected as in the following example.

Figure 3-1: Null Modem Cable Example



Alternatively to the above an external VGA card such as CP331 may be used to provide outputs to a CRT or LCD.

The Award Preboot Manager package includes online help and installation instructions and operates under Win9x and Windows NT.

The CP301 Rear I/O version provides the possibility to connect a keyboard.

Chapter 4

CMOS Setup

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4. CMOS Setup

This chapter describes the Award BIOS Setup program, EliteBIOS, version 4.51PG. The Setup program lets you modify basic system configuration settings.

4.1 Proprietary Notice

Unless otherwise noted, chapter 4 of this manual, which concerns the EliteBIOS setup program, as well as the information herein disclosed are proprietary to AWARD Software International, Inc. Any person or entity to whom this document is furnished or who otherwise has possession thereof, by acceptance agrees that it will not be copied or reproduced in whole or in part, nor used in any manner except to meet the purposes for which it was delivered.

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4.2 Introduction to Setup

This manual describes the Award BIOS Setup program. The Setup program lets you modify basic system configuration settings. The settings are then stored in a dedicated battery-backed memory, called CMOS RAM, that retains the information when the power is turned off.

A special feature of *PEP's* CompactPCI boards is that all Setup information is additionally saved in a non-volatile serial EEPROM. This feature provides the user with enhanced data security in comparison with a standard PC board, because setup data will not be lost should the battery fail.

The Award BIOS in your computer is a customized version of an industry-standard BIOS for IBM PC AT–compatible personal computers. It supports the Intel®x86 and compatible processors. The BIOS provides critical low-level support for the system central processing, memory, and I/O subsystems.

The Award BIOS has been customized by adding important, but nonstandard, features such as virus and password protection, power management, and detailed fine-tuning of the chipset controlling the system.

The rest of this manual is intended to guide you through the process of configuring your system using Setup.

Starting Setup

The Award BIOS is immediately activated when you first turn on the computer. The BIOS reads system configuration information in CMOS RAM and begins the process of checking out the system and configuring it through the Power-on Self Test (POST).

When these preliminaries are finished, the BIOS seeks an operating system on one of the data storage devices (hard drive, floppy drive, etc.). The BIOS launches the operating system and hands control of system operations to it.

During POST, you can start the Setup program in one of two ways:

- By pressing <Del> immediately after switching the system on, or
- By pressing the <Del> key or by simultaneously pressing <CTRL>, <ALT>, and <ESC> keys when the following message appears briefly at the bottom of the screen during POST:

Press DEL to enter SETUP

If the message disappears before you respond and you still wish to enter Setup, restart the system to try again by turning it OFF then ON or pressing the RESET button on the system case. You may also restart by simultaneously pressing <CTRL>, <ALT>, and <Delete> keys. If you do not press the keys at the correct time and the system does not boot, an error message appears and you are again asked to

Press F1 to continue, DEL to enter SETUP

Setup Keys

The following table describes how to navigate in Setup using the keyboard.

Table 4-1: Keyboard Commands

Up Arrow	Move to previous item
Down Arrow	Move to next item
Left Arrow	Move to the item to the left
Right Arrow	Move to the item to the right
Esc Key	Main Menu: Quit without saving changes into CMOS RAM. Status Page Setup Menu and Option Page Setup Menu: Exit current page and return to Main Menu
PgUp Key	Increase the numeric value or make changes
PgDn Key	Decrease the numeric value or make changes
+ Key	Increase the numeric value or make changes
- Key	Decrease the numeric value or make changes
F1 Key	General help, only for Status Page Setup Menu and Option Page Setup Menu
F2 Key Shift-F2	Change color from total of 16 colors. F2 to select color forward, Shift-F2 to select color backward
F3 Key	Calendar, only for Status Page Setup Menu
F4 Key	Reserved
F5 Key	Restore the previous CMOS value from CMOS, only for Option Page Setup Menu
F6 Key	Load the default CMOS RAM value from BIOS default table, only for Option Page Setup Menu
F7 Key	Load the default
F8 Key	Reserved
F9 Key	Reserved
F10 Key	Save all the CMOS changes, only for Main Menu

Getting Help

Press F1 and a small help window pops up that describes the appropriate keys to use and the possible selections for the highlighted item. To exit the Help Window press <Esc> or the F1 key again.

In Case of Problems

If, after making and saving system changes with Setup, you discover that your computer is no longer able to boot, the Award BIOS supports an override to the CMOS settings that resets your system to its default configuration.

You can invoke this override by immediately pressing <Insert> when you restart your computer. You can restart by either using the ON/OFF switch, the RESET button or by pressing <CTRL>, <ALT> and <Delete> at the same time.

The best advice is to only alter settings that you thoroughly understand. In particular, do not change settings in the Chipset screen without good reason. The Chipset defaults have been carefully chosen by *PEP Modular Computers* for optimum performance and reliability. Even a seemingly small change to the Chipset setup may result in the system becoming unstable.

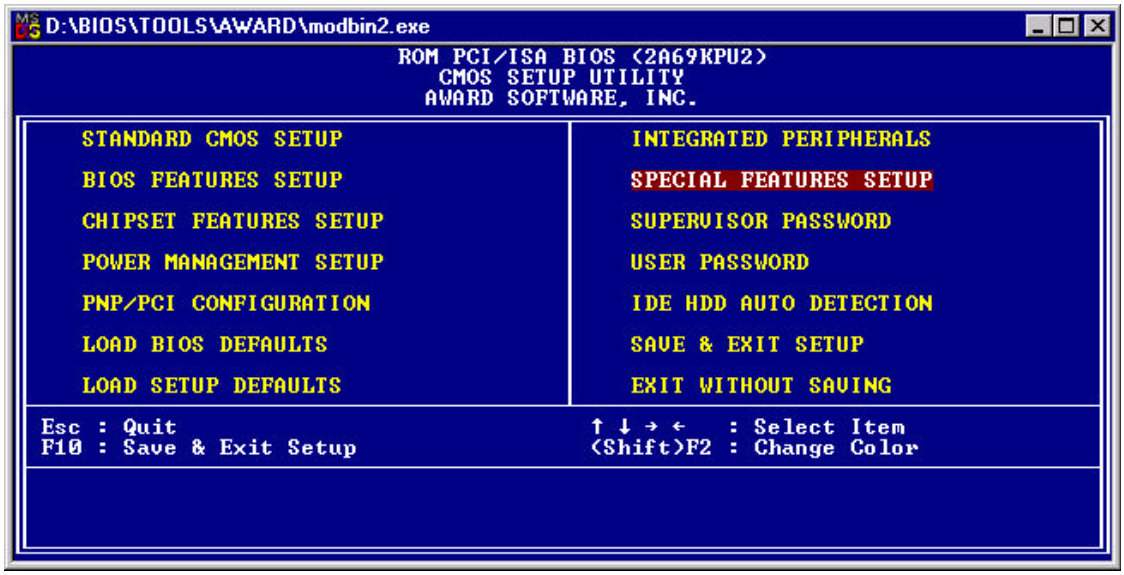
Setup Variations

Not all systems have the same Setup. While the basic look and function of the Setup program remains the same for all systems, the appearance of your Setup screens may differ from the screens shown here. Each system design and chipset combination require customized configurations. In addition, the final appearance of the Setup program depends on your system designer. Your system designer may decide that certain items should not be available for user configuration and remove them from the Setup program.

4.3 Main Setup Menu

When you enter the Award BIOS CMOS Setup Utility, a Main Menu, similar to the one shown below, appears on the screen. The Main Menu allows you to select from several Setup functions and two exit choices. Use the arrow keys to select items and press ↵ to accept and enter the sub-menu.

Figure 4-1: CMOS Setup Utility Main Menu — Screen Display



A brief description of each highlighted selection appears at the bottom of the screen.

Following is a brief summary of each Setup category.

Standard CMOS Setup

Options in the original PC AT-compatible BIOS.

BIOS Features Setup

Award enhanced BIOS options.

Chipset Features Setup

Options specific to your system chipset.

Power Management Setup

Advanced Power Management (APM) options.

PNP/PCI Configuration

PlugandPlay standard and PCI Local Bus configuration options.

Integrated Peripherals

I/O subsystems, that depend on the integrated peripherals controller in your system.

Special Features Setup

Items related to features of this board, which are not common to standard motherboard designs.

Supervisor/User Password

Change, set, or disable a password. In BIOS versions that allow separate user and supervisor passwords, only the supervisor password permits access to Setup. The user password generally allows only power-on access.

EIDE HDD Auto Detection

Automatically detect and configure EIDE hard disk parameters.

Load BIOS Defaults

BIOS defaults are factory settings for the most stable, minimal-performance system operations.

Load Setup Defaults

Setup defaults are factory settings for optimal-performance system operations.

Save & Exit Setup

Save settings in non-volatile CMOS RAM and exit Setup.

Exit Without Save

Abandon all changes and exit Setup.

4.4 Standard CMOS Setup

In the Standard CMOS menu you can set the system clock and calendar, record disk drive parameters and the video subsystem type, and select the type of errors that stop the BIOS POST.

Date

The BIOS determines the day of the week from the other date information. This field is for information only.

Press the → or ← key to move to the desired field (date, month, year). Press the “PgUp” or “PgDn” key to increment the setting, or type the desired value into the field.

Time

The time format is based on the 24-hour military-time clock. For example, 1 p.m. is 13:00:00. Press the → or ← key to move to the desired field. Press the PgUp or PgDn key to increment the setting, or type the desired value into the field.

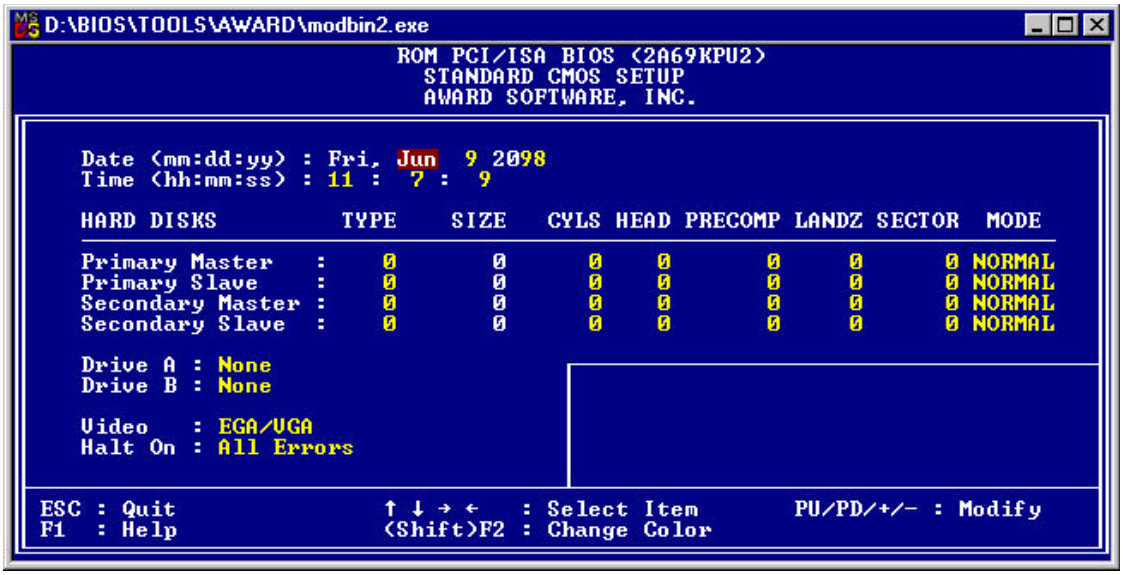
Hard Disks

The BIOS supports up to four EIDE drives. This section does not show information relating to other EIDE devices, such as a CD-ROM drive, or about other hard drive types, such as SCSI drives.

Important!

We recommend that you select the AUTO type for all drives.

Figure 4-2: Standard CMOS Setup Menu — Screen Display



The BIOS has the capability to automatically detect the specifications and optimal operating mode of almost all EIDE hard drives. When you select type AUTO for a hard drive, the BIOS detects its specifications during POST, every time the system boots.

If you do not want to select drive type AUTO, other methods of selecting the drive type are available as follows:

1. Match the specifications of your installed EIDE hard drive(s) with the pre-programmed values for drive types 1 through 45.
2. Select USER and enter values into each drive parameter field.
3. Use the EIDE HDD AUTO DECTECTION function in “Setup”.

The following table provides a brief explanation of drive specifications:

Table 4-2: Description of Drive Specifications

Spec.		Description
Type		The BIOS contains a table of pre-defined drive types. Each defined drive type has a specified number of cylinders, number of heads, write pre-compensation factor, landing zone, and number of sectors. Drives whose specifications do not accommodate any pre-defined type are classified as type USER.
Size		Disk drive capacity (approximate). Note that this size is usually slightly greater than the size of a formatted disk given by a disk-checking program.
Cyls.		Number of cylinders
Head		Number of heads
Precomp.		Write pre-compensation cylinder
Landz		Landing zone
Sector		Number of sectors
Mode	Auto	Auto: The BIOS automatically determines the optimal mode.
	Normal	The maximum number of cylinders, heads, and sectors supported are 1024, 16, and 63 respectively.
	Large	For drives that do not support LBA and have more than 1024 cylinders.
	LBA	During drive accesses, the EIDE controller transforms the data address described by sector, head, and cylinder number into a physical block address, significantly improving data transfer rates. For drives with greater than 1024 cylinders.

Drive A / Drive B

Selects the correct specifications for the diskette drive(s) installed in the computer.

Table 4-3: Diskette Drives

None	No diskette drive installed
360K, 5.25 in	5-1/4 inch PC-type standard drive; 360 kilobyte capacity
1.2M, 5.25 in	5-1/4 inch AT-type high-density drive; 1.2 megabyte capacity
720K, 3.5 in	3-1/2 inch double-sided drive; 720 kilobyte capacity
1.44M, 3.5 in	3-1/2 inch double-sided drive; 1.44 megabyte capacity
2.88M, 3.5 in	3-1/2 inch double-sided drive; 2.88 megabyte capacity

Video

Selects the type of primary video subsystem in your computer. The BIOS usually detects the correct video type automatically. The BIOS supports a secondary video subsystem, however, this is not selected in Setup.

Table 4-4: Primary Video Subsystem Selection

EGA/VGA	Enhanced Graphics Adapter/Video Graphics Array. For EGA, VGA, SEGA, SVGA or PGA monitor adapters.
CGA 40	Color Graphics Adapter, power-up in 40 column mode
CGA 80	Color Graphics Adapter, power-up in 80 column mode
MONO	Monochrome adapter, includes high resolution monochrome adapters

Halt On

During the power-on self-test (POST), the computer stops if the BIOS detects a hardware error. You can program the BIOS to ignore certain errors during POST and continue the boot-up process. The possible selections are listed in the following table.

Table 4-5: POST Specific Commands

Command	POST Action
No errors	POST does not stop for any errors.
All errors	If the BIOS detects any non-fatal error, POST stops and prompts you to take corrective action.
All, But Keyboard	POST does not stop for a keyboard error, but stops for all other errors.
All, But Diskette	POST does not stop for diskette drive errors, but stops for all other errors.
All, But Disk/Key	POST does not stop for a keyboard or disk error, but stops for all other errors.

Memory

You cannot change any values in the Memory fields; they are only for your information. The fields show the total installed random access memory (RAM) and amounts allocated to base memory, extended memory, and other (high) memory. RAM is counted in kilobytes (KB: approximately one thousand bytes) and megabytes (MB: approximately one million bytes).

RAM is the computer's working memory, where the computer stores programs and data currently being used, so they are accessible to the CPU. Modern personal computers may contain up to 64 MB, 128 MB, or more.

Base Memory

Typically 640 KB. Also called conventional memory. The DOS operating system and conventional applications use this area.

Extended Memory

Above the 1 MB boundary. Early IBM personal computers could not use memory above 1 MB, but current PCs and their software can use extended memory.

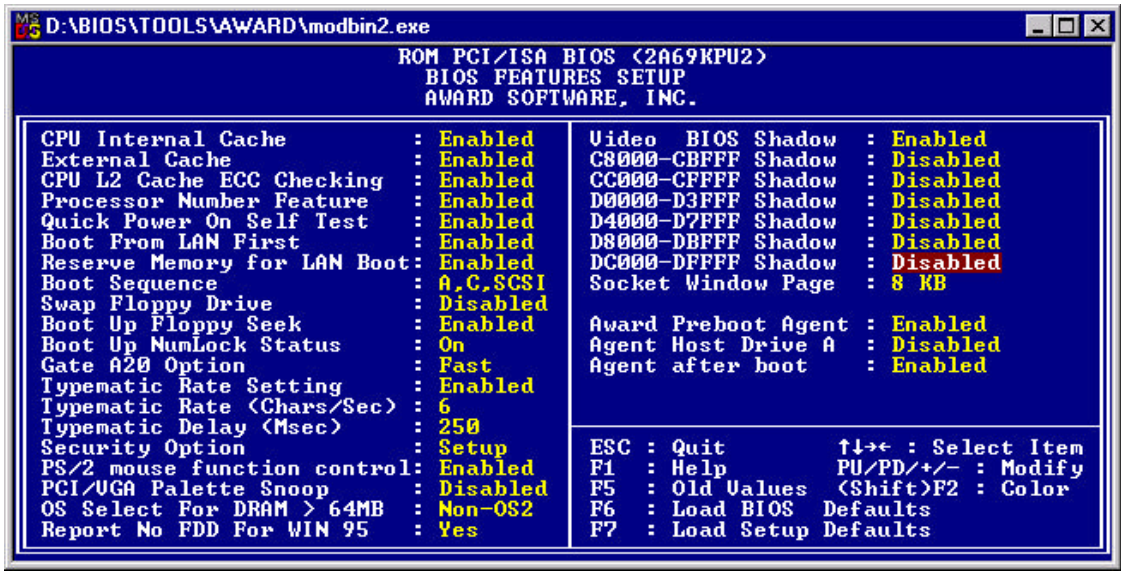
Other Memory

Between 640 KB and 1 MB; often called High Memory. DOS may load terminate-and-stay-resident (TSR) programs, such as device drivers, in this area, to free as much conventional memory as possible for applications. Lines in your CONFIG.SYS file that start with LOADHIGH load programs into high memory.

4.5 BIOS Features Setup

This screen contains industry-standard options additional to the core PC AT BIOS. This section describes all fields presented by Award Software in this screen. The example screen below may vary somewhat from the one in your Setup program; your system board designer may omit or modify some fields

Figure 4-3: BIOS Features Setup — Screen Display



CPU Internal Cache / External Cache

Cache memory is additional memory that is much faster than conventional DRAM (system memory). CPU's from 486-type on up contain internal cache memory, and most, but not all, modern PC's have additional (external) cache memory. When the CPU requests data, the system transfers the requested data from the main DRAM into cache memory, for even faster access by the CPU.

The External Cache field may not appear if your system does not have external cache memory.

CPU L2 Cache ECC Checking

When you select *Enabled*, memory checking is enabled when the external cache contains ECC SRAM's.

Quick Power-on Self Test

Select Enabled to reduce the amount of time required to run the power-on self-test (POST). A quick POST skips certain steps. We recommend that you normally disable quick POST. Better to find a problem during POST than lose data during your work.

Boot from LAN first

If Your BIOS if capable of Booting from LAN via DHCP/BOOTP – protocol (option), you can switch this option on/off here.

Boot Sequence

The original IBM PC's loaded the operating system from drive A (floppy disk), so IBM PC-compatible systems are designed to search for an operating system first on drive A, and then on drive C (hard disk). However, modern computers usually load the operating system from the hard drive, and may even load it from a CD-ROM drive. The BIOS now offers 10 different boot sequence options of three drives each. In addition to the traditional drives A and C, options include EIDE hard drives D, E and F; plus an SCSI hard drive and a CD -ROM drive.

Swap Floppy Drive

This field is effective only in systems with two floppy drives. Selecting Enabled assigns physical drive B to logical drive A, and physical drive A to logical drive B.

Boot Up Floppy Seek

When Enabled, the BIOS tests (seeks) floppy drives to determine whether they have 40 or 80 tracks. Only 360-KB floppy drives have 40 tracks; drives with 720 KB, 1.2 MB, and 1.44 MB capacity all have 80 tracks. Because very few modern PC's have 40-track floppy drives, we recommend that you set this field to Disabled to save time.

Boot Up Numlock Status

Toggle between On or Off to control the state of the NumLock key when the system boots. When toggled On, the numeric keypad generates numbers instead of controlling cursor operations.

Boot Up System Speed

Select High to boot at the default CPU speed; select Low to boot at the speed of the AT bus. Some add-in peripherals or old software (such as old games) may require a slow CPU speed. The default setting is High.

Gate A20 Option

Gate A20 refers to the way the system addresses memory above 1 MB (extended memory). When set to Fast, the system chipset controls Gate A20. When set to Normal, a pin in the keyboard controller controls Gate A20. Setting Gate A20 to Fast improves system speed, particularly with OS/2 and Windows.

Typematic Rate Setting

When Disabled, the following two items (Typematic Rate and Typematic Delay) are irrelevant. Keystrokes repeat at a rate determined by the keyboard controller in your system.

When Enabled, you can select a typematic rate and typematic delay.

Typematic Rate (Chars/Sec)

When the typematic rate setting is enabled, you can select a typematic rate (the rate at which a character repeats when you hold down a key) of 6, 8, 10, 12, 15, 20, 24 or 30 characters per second.

Typematic Delay (ms)

When the typematic rate setting is enabled, you can select a typematic delay (the delay before key strokes begin to repeat) of 250, 500, 750 or 1000 milliseconds.

Security Option

If you have set a password, select whether the password is required every time the System boots, or only when you enter Setup.

PS/2 Mouse Function Control

If your system has a PS/2 mouse port and you instal a serial pointing device, select *Disabled*.

PCI/VGA Palette Snoop

Your BIOS Setup may not contain this field. If the field is present, leave at Disabled.

OS Select for DRAM>64MB

Select OS2 only if you are running the OS/2 operating system with greater than 64 MB of RAM in your system.

Report No FDD for WIN 95

Select *Yes* to release IRQ6 when the system contains no floppy drive, for compatibility with Windows 95 logo certification. In the **Integrated Peripherals** screen, select *Disabled* for the **Onboard FDC Controller** field.

Shadow

Software that resides in a read-only memory (ROM) chip on a device is called *firmware*. The Award BIOS permits *shadowing* of firmware such as the system BIOS, video BIOS, and similar operating instructions that come with some expansion peripherals, such as, for example, a SCSI adaptor.

Shadowing copies firmware from ROM into system RAM, where the CPU can read it through the 16-bit or 32-bit DRAM bus. Firmware not shadowed must be read by the system through the 8-bit X-bus. Shadowing improves the performance of the system BIOS and similar ROM firmware for expansion peripherals, but it also reduces the amount of high memory (640 KB to 1 MB) available for loading device drivers, etc.

Enable shadowing into each section of memory separately. Many system designers hardwire shadowing of the system BIOS and eliminate a System BIOS Shadow option.

Video BIOS shadows into memory area C0000-C7FFF. The remaining areas shown on the BIOS Features Setup screen may be occupied by other expansion card firmware. If an expansion peripheral in your system contains ROM-based firmware, you need to know the address range the ROM occupies to shadow it into the correct area of RAM.

Socket Window Page

The CP301 is equipped with a 32-pin socket to take additional Flash-ROM. This Flash-ROM may be addressed by a paging mechanism. The size of one Flash page can be set at this point as follows:

Table 4-6: Setting Flash Page Size

Page Size	Address Space used by Socket Flash EPROM
8 KB	0xDE000 - 0xDFFFF
32 KB	0xD8000 - 0xDFFFF
64 KB	0xD0000 - 0xDFFFF

Award Preboot Agent

Agent software may be enabled and disabled. The default is Disabled.

Agent Port Address

Select which UART address Agent software should use. Note to have set a UART in the INTEGRATED PERIPHERALS page to one of the below allowed settings. Recommended is 03F8h, which means COM1 (03F8h / IRQ 4); “auto” must not be selected.

The Agent system must have a serial (RS-232C) peripheral subsystem, to support a null modem (direct) connection.

If the Agent and host connect, but a session is not established, check the Agent COM port settings which should read as follows:

3F8h - IRQ4
2F8h - IRQ3
3E8h - IRQ4
2E8h - IRQ3

Agent Host Drive A

When the administrative host is using the Preboot Manager application, the Agent can boot and run applications from host floppy drive A. INT13 calls intended for the Agent floppy drive A are redirected by the Agent extension to the host floppy drive A. All other INT13 calls are passed along to the original interrupt handler. The Manager application can receive the Agent drive A interrupt and interpret the commands. It then calls its own INT13 handler to read or write the requested sectors to host drive A. Both Manager and Agent serial version software use Xmodem protocol for all transfers.

The floppy drive redirection feature permits support personnel to remotely administer two vital tools on the Agent system:

- PC DIAG diagnostics package from Unicore Software (available through Award Software as part of the Manager application).
- AWDFLASH BIOS flash upgrade utility. (in batch mode, this means giving the parameters at the command line; e.g. awdflash <filename> /Sn/Py, DO NOT USE INTERACTIVE MODE!!!)

Select Enabled to enable this feature, default is Disabled.

Agent after Boot

In the "standard" Agent product, Agent software continues to function after the operating system loads. However, some non-DOS operating systems are not compatible with the Agent BIOS extension, so the Agent should disable when the OS loads. Selecting Disabled turns off the Agent software just as the BIOS transfers control to the operating system. Default is Disabled.

Award Baud Rate

The baud rate is preset to 19200 baud and cannot be changed. For this reason it does not appear in the setup menu.

Null-Modem Cable Pinout

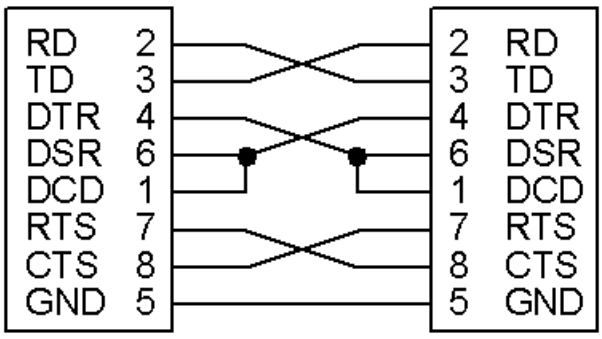


Figure 4-4: Null-Modem Cable Connection

A null-modem cable is a serial cable designed to connect two PC's. Each end has a 9-pin, female RS-232C connector. If you are creating your own 9-pin cable, connect the two ends through the cable as shown here.

Further Information

For further information please refer to the manual for the Award Preboot Agent™ 2.0 which accompanies the manual for the Award Preboot Manager™ 2.0.

4.6 Chipset Features Setup

This section describes features of the PIIX4 PCIset. If your system contains a different chipset, this section will bear little resemblance to what you see on your screen..

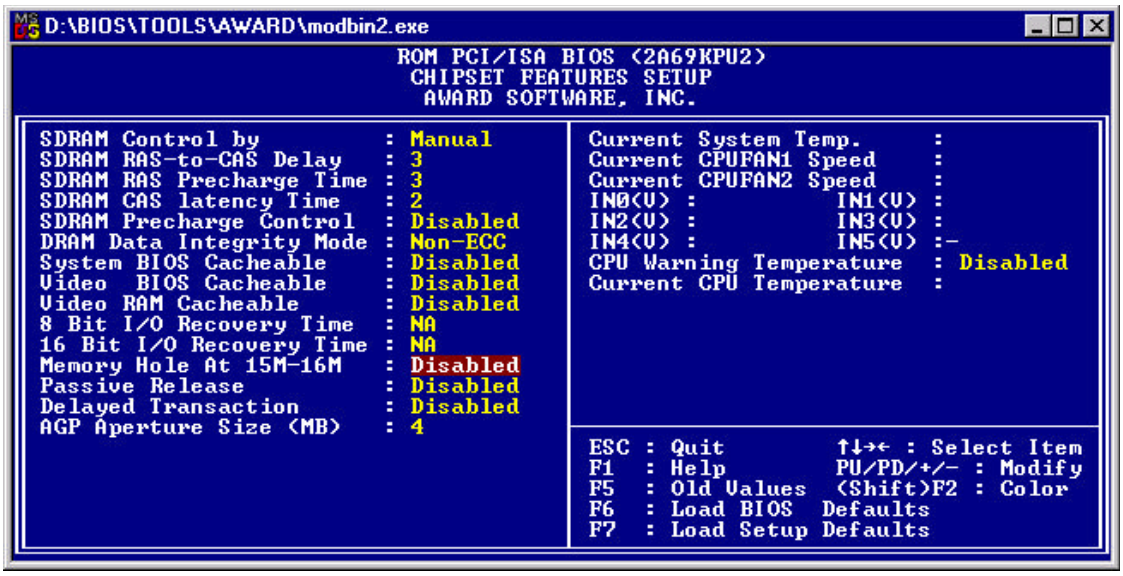
PEP Advantage

This section describes all the fields presented on this screen display. Please note that your system board designer may omit or modify some of the fields described in the following.

Advanced Options

The parameters in this screen are for system designers, service personnel, and technically competent users only. Do not reset these values unless you understand the consequences of your changes.

Figure 4-5: Chipset Features Setup — Screen Display.



SDRAM Control by Manual / Auto

Auto Configuration selects predetermined optimal values for chipset parameters. When *Disabled*, chipset parameters revert to setup information stored in the CMOS. Many fields in this screen are not available when Auto Configuration is *Enabled*.

SDRAM RAS To CAS Delay

Select the RAS to CAS delay time. See Refresh Cycle Time for information about the Auto Configuration of this value.

SDRAM RAS Precharge Time

The precharge time is the number of cycles it takes for the RAS to accumulate its charge before DRAM refresh. If insufficient time is allowed, refresh may be incomplete and the DRAM may fail to retain data.

SDRAM CAS Latency Time

When synchronous DRAM is installed, you can control the number of CLK's between the SDRAM's sample of a read command and the time when the controller samples read data from the SDRAM's. Do not reset this field from the default value specified by the system designer.

SDRAM Precharge Control

When *Enabled*, all CPU cycles to SDRAM result in an All Banks Precharge Command on the SDRAM interface.

DRAM Data Integrity Mode

Select *Non-ECC* or *ECC* (error-correcting code), according to the type of installed DRAM.

System BIOS Cacheable

Selecting *Enabled* allows caching of the system BIOS ROM at 0xF0000 to 0xFFFFF, resulting in better system performance. However, if any program writes to this memory area, a memory access error may result.

Video BIOS Cacheable

Selecting *Enabled* allows caching of the video BIOS ROM at 0xC0000 to 0xC7FFF, resulting in better video performance. However, if any program writes to this memory area, a memory access error may result.

Video RAM Cacheable

Selecting *Enabled* allows caching of the video memory (RAM) at 0xA0000 to 0xAFFFF, resulting in better video performance. However, if any program writes to this memory area, a memory access error may result.

8/16-bit I/O Recovery Time

The I/O recovery mechanism adds bus clock cycles between PCI-originated I/O cycles to the ISA bus. This delay takes place because the PCI bus is so much faster than the ISA bus.

These two fields let you add recovery time (in bus clock cycles) for 16-bit and 8-bit I/O.

Memory Hole at 15M-16M

You can reserve this area of system memory for ISA adaptor ROM. When this area is reserved, it cannot be cached. The user information for peripherals that need to use this area of system memory usually discusses their memory requirements.

Passive Release

When *Enabled*, CPU to PCI bus accesses are allowed during passive release. Otherwise, the arbiter only accepts another PCI master access to local DRAM.

Delayed Transaction

The chipset has an embedded 32-bit posted write buffer to support delay transactions cycles. Select *Enabled* to support compliance with PCI specification version 2.1.

AGP Aperture Size (MB)

Select the size of the Accelerated Graphics Port (AGP) aperture. The aperture is a portion of the PCI memory address range dedicated for graphics memory address space. Host cycles that hit the aperture range are forwarded to the AGP without any translation. See http://www.agpforum.org for AGP information.

CPU Warning Temperature

Select the combination of lower and upper limits for CPU temperature, if your computer contains an environmental monitoring system. If the CPU temperature extends beyond either limit, any warning mechanism programmed into your application is activated.

Current CPU Temperature

This field displays the *current* CPU temperature, if your computer contains an environmental monitoring system.

Current CPU Fan 1

Monitors the onboard Fan mounted on the CPU heat sink, if available.

Current CPU Fan 2

Monitors the Fan signal routed to the rear I/O connector.

Voltage Monitor

Displays all onboard voltages for diagnostic purposes.

Shutdown Temperature

Select the combination of lower and upper limits for the system shutdown temperature, if your computer contains an environmental monitoring system. If the temperature extends beyond either limit, the system shuts down.

Recommendation for optimizing performance:

With only 64/128 MB onboard SDRAM is installed, use the following settings:

SDRAM RAS-to-CAS Delay: 2

SDRAM RAS Precharge Time: 2

SDRAM CAS latency Time: 2

If additional RAM is installed in the SODIMM socket, automatic SDRAM Control is recommended.

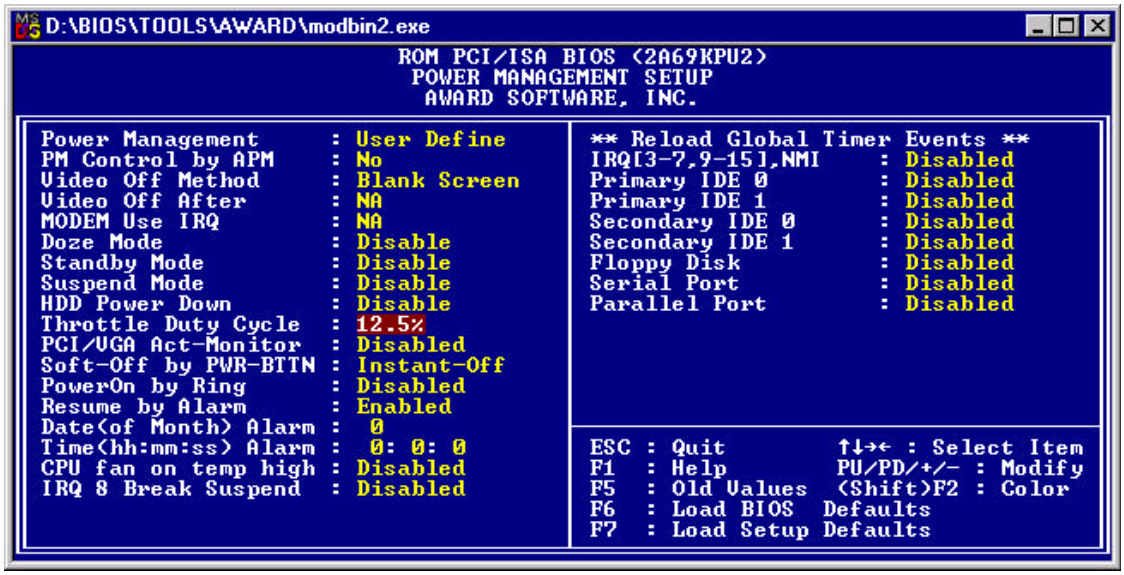
Field Shutdown Temperature: this does not exist for the CP301

4.7 Power Management

PEP Advantage

This section describes all fields presented on this screen display. Please note that your system board designer may omit or modify some of the fields described in the following.

Figure 4-6: Power Management Setup — Screen Display.



ACPI Function

Select *Enabled* only if your computer's operating system supports the Advanced Configuration and Power Interface (ACPI) specification. Currently, Windows 98®, Windows 2000® and Windows NT® support ACPI.

Power Management

This option allows you to select the type (or degree) of power saving for Doze, Standby, and Suspend modes. See the section *PM Timers* for a brief description of each mode.

The following table describes each power management mode:

Table 4-7: Power Management Modes

Mode	Description
Max. Saving	Maximum power savings. **Only Available for SL CPU's**. Inactivity period is 1 minute in each mode.
User Defined	Sets each mode individually. Select time-out periods in the *PM Timers* section, which follows.
Min. Saving	Minimum power savings. Inactivity period is 1 hour in each mode (except the hard drive).

PM Control by APM

If Advanced Power Management (APM) is installed in your system, selecting *Yes* gives improved power savings.

Video-Off Method

Determines the manner in which the monitor is blanked.

Table 4-8: Video-Off Commands

V/H SYNC+Blank	System switches off vertical and horizontal synchronization ports and writes blanks to the video buffer.
DPMS Support	Select this option if your monitor supports the Display Power Management Signaling (DPMS) standard of the Video Electronics Standards Association (VESA). Use the software supplied for your video subsystem to select video power management values.
Blank Screen	System writes blanks only to the video buffer.

Video-Off Option

This item determines the power management modes the monitor will enter before entering the Off-state as defined by the Video Off Method below. The Video Off Option moves from the low (doze) to the medium (standby) to high (suspend) power saving modes.

Modem Use IRQ

Name the interrupt request (IRQ) line assigned to the modem (if any) on your system. Activity by the selected IRQ always awakens the system.

4.8 PM Timers

The following modes are Green PC power saving functions. They are user-configurable only during User Defined Power Management mode.

Doze Mode

After the selected period of system inactivity (1 minute to 1 hour), the CPU clock runs at a slower speed while all other devices still operate at full speed.

Stand-By Mode

After the selected period of system inactivity (1 minute to 1 hour), the fixed disk drive and the video shut down while all other devices still operate at full speed.

Suspend Mode

After the selected period of system inactivity (1 minute to 1 hour), all devices except the CPU shut down.

HDD Power Down

After the selected period of drive inactivity (1 to 15 minutes), the hard disk drive powers down while all other devices remain active.

Throttle Duty Cycle

When the system enters Doze mode, the CPU clock runs only part of the time. You may select the percentage of the time that the clock runs.

Soft-Off by PWR-BTTN

When you select *Instant Off* or *Delay 4 Sec*., turning the system off with the on/off button places the system in a very low power usage state, either immediately or after 4 seconds, with only enough circuitry receiving power to detect power button activity or Resume by Ring activity.

Power-on by Ring

When *Enabled*, an input signal on the serial Ring Indicator (RI) line (in other words, an incoming call on the modem) awakens the system from a soft off state.

Resume by Alarm

When *Enabled*, you can set the date and time at which the RTC (real-time clock) alarm awakens the system from suspend mode.

Date (of Month) Alarm

Select a date in the month when you want the alarm to go off.

Time (hh:mm:ss) Alarm

Set the time at which you want the alarm to go off.

IRQ8 Break (Event From) Suspend

You can select *Enabled* or *Disabled* for monitoring of IRQ8 (the Real Time Clock) so that it does not awaken the system from Suspend mode.

Reload Global Timer Events

When Enabled, an event occurring on each of the devices listed below restarts the global timer for Standby mode:

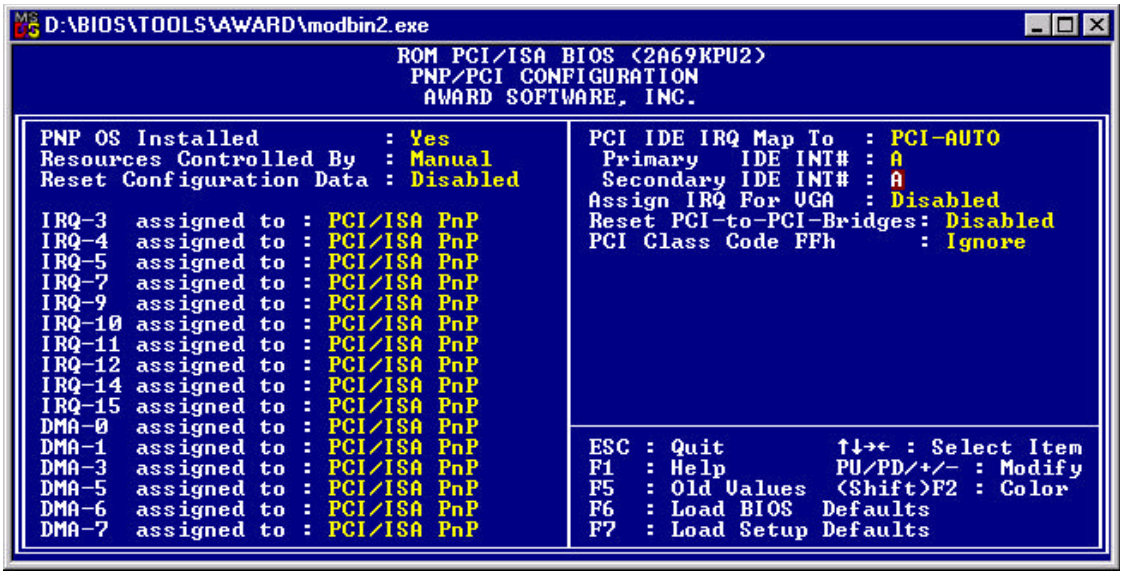
- IRQ§-7, 9-15, NM1,
- Primary EIDE 0,
- Primary EIDE 1,
- Secondary EIDE 0,
- Secondary EIDE 1,
- Floppy Disk,
- Serial Port,
- Parallel Port, and
- IRQ9 (IRQ2 Redir).

4.9 PNP/PCI Configuration

PEP Advantage

This section describes all the fields presented by this screen display. Please note that your system board designer may omit or modify some of the fields described in the following.

Figure 4-7: PNP/PCI Configuration — Screen Display



PNP OS Installed

Select “Yes” if the system operating environment is PlugandPlay aware (e.g. Win 95).

Resources Controlled by

The Award PlugandPlay BIOS can automatically configure all the boot and PlugandPlay-compatible devices. If you select *Auto*, all the interrupt request (IRQ) and DMA assignment fields disappear, as the BIOS automatically assigns them.

Reset Configuration Data

Normally this field is left *Disabled*. Select *Enabled* to reset Extended System Configuration Data (ESCD) when you exit Setup if you have installed a new add-on and the system re-configuration has caused such a serious conflict that the operating system cannot boot.

IRQ *n* Assigned to

When resources are controlled manually, assign each system interrupt as one of the following types, depending on the type of device using the interrupt.

Legacy ISA	Devices compliant with the original PC AT bus specification, requiring a specific interrupt (such as IRQ4 for serial port 1).
PCI/ISA PnP	Devices compliant with the PlugandPlay standard, whether designed for PCI or ISA bus architecture.

DMA *n* Assigned to

When resources are controlled manually, assign each system interrupt as one of the following types, depending on the type of device using the interrupt.

Legacy ISA	Devices compliant with the original PC AT bus specification, requiring a specific DMA channel
PCI/ISA PnP	Devices compliant with the PlugandPlay standard, whether designed for PCI or ISA bus architecture.

PCI EIDE IRQ Map to

This field lets you select PCI EIDE IRQ mapping or PC AT (ISA) interrupts. If your system does not have one or two PCI EIDE connectors on the system board, select values according to the type of EIDE interface(s) installed in your system (PCI or ISA). Standard ISA interrupts for EIDE channels are IRQ14 for primary and IRQ15 for secondary.

Primary/Secondary EIDE INT#

Each PCI peripheral connection is capable of activating up to four interrupts: *INT# A*, *INT# B*, *INT# C* and *INT# D*. By default, a PCI connection is assigned *INT# A*. Assigning *INT# B* has no meaning unless the peripheral device requires two interrupt services rather than just one. Because the PCI EIDE interface in the chipset has two channels, it requires two interrupt services. The primary and secondary EIDE INT# fields default to

values appropriate for two PCI EIDE channels, with the primary PCI EIDE channel having a lower interrupt than the secondary.

Reset PCI-to-PCI Bridges

The BIOS may reset the PCI-to-PCI Bridges in the system using a software reset mechanism. Especially in conjunction with Hotswap compatible boards, it should be disabled. Default is disabled.

PCI Class Code FFh:

Some PCI boards generate a class code 0FFh. Although this code does not conform with the PCI standard, boards of this kind are distributed by some vendors.

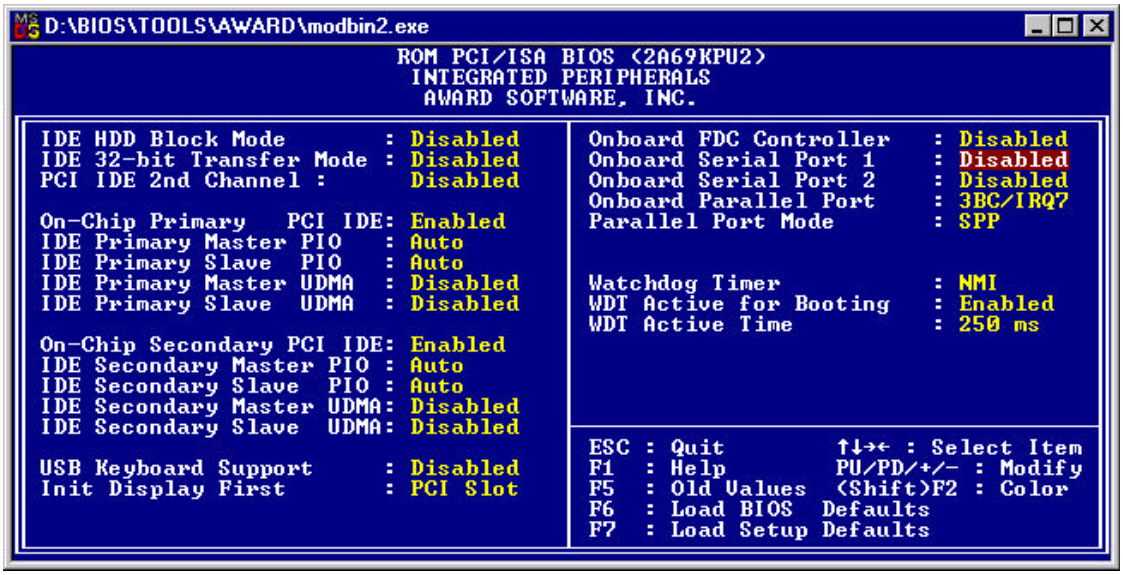
By setting this field to configure, these non-standard boards will be ignored
By setting this field to ignore, these non-standard boards will also be configured by the BIOS and made operable.

4.10 Integrated Peripherals

Important!

This section describes all the fields presented by Award Software in this screen display. Please note that your system board designer may omit or modify some fields.

Figure 4-8: Integrated Peripherals — Screen Display



PCI EIDE 2nd Channel

Used to enable the 2nd PCI EIDE interface

EIDE HDD Block Mode

Select *Enabled* only if your hard drives support block mode.

EIDE 32-bit Transfer Mode

Enables or disables 32-bit Data transfers.

On-Chip PCI EIDE (Primary/Secondary)

The Intel® 82C440BX chipset contains a PCI EIDE interface with support for two EIDE channels. Select *Enabled* to activate the primary and/or secondary EIDE interface. Select *Disabled* to deactivate this interface if you instal a primary and/or secondary add-in EIDE interface.

EIDE PIO Modes (Primary/Secondary Master/Slave)

The four EIDE PIO (Programmed Input/Output) fields let you set a PIO mode (0-4) for each of up to four EIDE devices that the internal PCI EIDE interface supports. Modes 0 through 4 provide successively increased performance. In *Auto* mode, the system automatically determines the best mode for each device.

EIDE Primary/Secondary Master/Slave UDMA

UDMA (Ultra DMA) is a DMA data transfer protocol that utilizes ATA commands and the ATA bus to allow DMA commands to transfer data at a maximum burst rate of 33 MB/s. When you select *Auto* in the four EIDE UDMA fields (for each of up to four EIDE devices that the internal PCI EIDE interface supports), the system automatically determines the optimal data transfer rate for each EIDE device.

USB Keyboard Support

Select *Enabled* if your system contains a Universal Serial Bus (USB) controller and you have a USB keyboard.

Init Display First

Initialize the AGP video display before initializing any other display device on the system. Thus the AGP display becomes the primary display.

Onboard FDC Controller

Select *Enabled* if your system has a floppy disk controller (FDC) installed on the system board and you wish to use it. If you install an add-on FDC or the system has no floppy drive, select *Disabled* in this field.

Onboard Serial Ports: 1, 2

Select a logical COM port address and corresponding interrupt for the first and second serial ports.

Onboard Parallel Port

Select a logical LPT port address and corresponding interrupt for the physical parallel port.

Parallel Port Mode

Select an operating mode for the onboard parallel port. Select *Normal* unless you are certain that both your hardware and software support one of the other available modes.

ECP Mode Use DMA

Select a DMA channel for the parallel port for use during ECP mode.

Watchdog Timer

Select the watchdog routing.

WDT Active for Booting

Select *Enable* if the watchdog timer requires to be started before the operating system is booted from the BIOS.

WDT Active Time

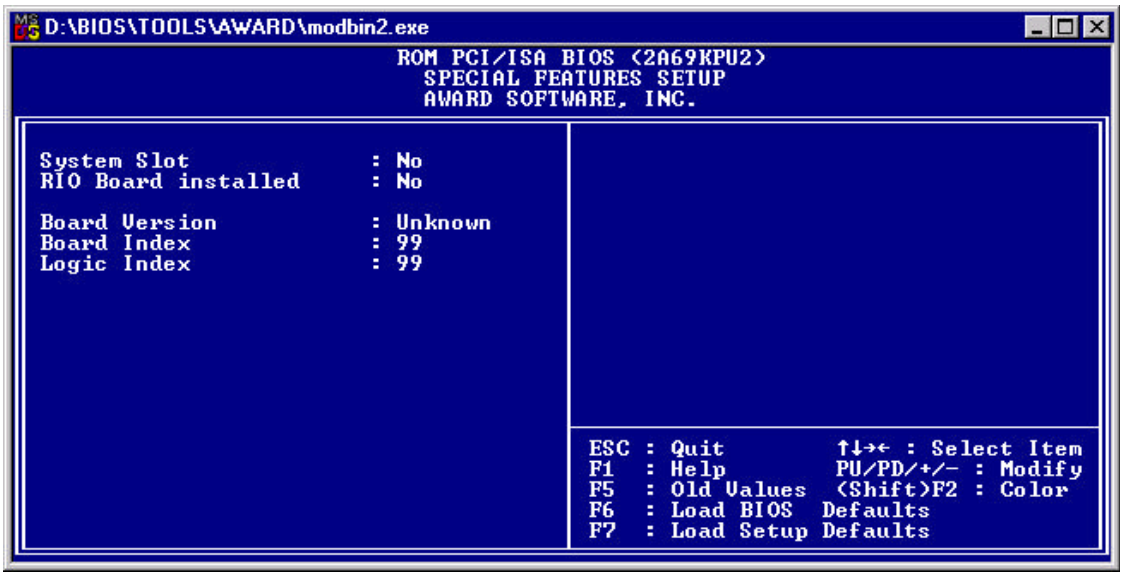
Select the time after which the action selected occurs, if the watchdog timer is not retriggered.

4.11 Special Setup Features

Important!

This section describes all the fields presented by Award Software in this screen display. Your system board designer may omit or modify some fields.

Figure 4-9: Special Features Setup — Screen Display



System Slot

This is a display only field. Yes indicates that this CPU is the system controller configuring the backplane and handling all interrupts relating to the backplane. No indicates that this CPU is a slave CPU.

Board Version

This is a display only field, which reflects the value of an onboard register. This must always correspond with the CPU on which the BIOS is installed.

Board Index

This is a display only field, which reflects the value of an onboard register. It shows the index of the hardware.

Logic Index

This is a display only field, which reflects the value of an onboard register. It shows the index of the onboard logic. When the Board Index is 00 this item is not displayed.

4.12 Password Setting

When you select this function, the following message appears at the center of the screen:

`Enter password:`

Type the password, up to eight characters in length, and press "↵". Typing a password clears any previously entered password from the CMOS memory.

After having pressed "↵" the message changes to:

`Confirm password:`

Type the password again and press "↵". To abort the process at any time, press "Esc".

In the "Security Option" item in the "BIOS Features Setup" screen, select `System` or `Setup`:

Table 4-9: Security Options

System	Enter a password each time the system boots and whenever you enter Setup.
Setup	Enter a password whenever you enter Setup.



Important!

To clear the password, simply press "↵" when asked to enter a password. Then the password function is disabled.

4.13 POST Messages

During the Power-on Self Test (POST), the BIOS displays a message whenever it detects a correctable error. Any error message is followed by this prompt:

```
Press “F1” to continue, “Ctrl-Alt-Esc” or “Del” to enter setup.
```

Following is a list of POST error messages for both the ISA and the EISA BIOS.

CMOS Battery Has Failed

The CMOS battery is no longer functional. It should be replaced.

CMOS Checksum Error

Checksum of CMOS is incorrect. This can indicate that the CMOS has become corrupted. This error may have been caused by a weak battery. Check the battery and replace it, if necessary.

Disk Boot Failure, Insert System Disk and Press Enter

No boot device was found. This could mean that either a boot drive was not detected or that the drive does not contain proper system boot files. Insert a system disk into Drive A: and press <Enter>. If you assumed the system would boot from the hard drive, make sure the controller is inserted correctly and all cables are properly attached. Also be sure the disk is formatted as a boot device. Then reboot the system.

Diskette Drives or Types Mismatch Error - Run Setup

Type of floppy-disk drive installed in the system is different from the CMOS definition. Run “Setup” to reconfigure the drive type correctly.

Display Switch is Set Incorrectly

Display switch on the motherboard can be set to either monochrome or color. This error message indicates that the switch has a setting other than that indicated in Setup. Determine which setting is correct, and then either turn off the system and change the jumper, or enter Setup and change the video selection.

Display Type Has Changed Since Last Boot

Since the last powering-down of the system, the display adapter has been changed. You must configure the system for the new display type.

EISA Configuration Checksum Error - Please Run EISA Configuration Utility

The EISA non-volatile RAM checksum is incorrect or cannot correctly read the EISA slot. This can indicate either the EISA non-volatile memory has become corrupted or the slot has been configured incorrectly. Ensure also that the card is installed firmly in the slot.

EISA Configuration Is Not Complete - Please Run EISA Configuration Utility

The slot configuration information stored in the EISA non-volatile memory is incomplete.



Note:

When either of the above EISA error messages appears, the system boots in ISA mode so that you can run the EISA Configuration Utility.

Error Encountered Initializing Hard-Drive

Hard drive cannot be initialized. Make sure that the adapter is installed correctly and that all cables are correctly and firmly attached. Ensure also that the correct hard drive type is selected in “Setup”.

Error Initializing Hard-Disk Controller

Cannot initialize controller. Make sure that the cord is correctly and firmly installed in the bus. Ensure also that the correct hard drive type is selected in Setup. Also check to see if any jumper needs to be set correctly on the hard drive.

Floppy-Disk Controller Error or No Controller Present

Cannot find or initialize the floppy drive controller. Make sure that the controller is installed correctly and firmly. If there are no floppy drives installed, ensure that the floppy-disk drive selection in “Setup” is set to NONE.

Invalid EISA Configuration - Please Run EISA Configuration Utility

The non-volatile memory containing EISA configuration information was programmed incorrectly or has become corrupted. Re-run EISA configuration utility to correctly program the memory.



Note:

When this error appears, the system boots in ISA mode so that you can run the EISA configuration utility.

Keyboard Error or No Keyboard Present

Cannot initialize the keyboard. Make sure that the keyboard is attached correctly and that no keys are being pressed during the boot process.

If you are deliberately configuring the system without a keyboard, set the “Error Halt” condition in “Setup” to HALT ON ALL, BUT KEYBOARD. This causes the BIOS to ignore the missing keyboard and continue the boot process.

Memory Address Error at ...

Indicates a memory address error at a specific location. You can use this location along with the memory map for your system to find and replace the bad memory chips.

Memory Parity Error at ...

Indicates a memory parity error at a specific location. You can use this location along with the memory map for your system to find and replace the bad memory chips.

Memory Size Has Changed Since Last Boot

Memory has been added or removed since the last boot. In EISA mode use the configuration utility to reconfigure the memory configuration. In ISA mode enter “Setup” and enter the new memory size into the memory fields.

Memory Verify Error at ...

Indicates an error verifying a value already written to memory. Use the location along with your system's memory map to locate the bad chip.

Offending Address not Found

This message is used in conjunction with the “I/O Channel Check” and “RAM Parity Error” messages whenever the segment that has caused the problem cannot be isolated.

Offending Segment

This message is used in conjunction with the “I/O Channel Check” and “RAM Parity Error” messages whenever the segment that has caused the problem has been isolated.

Press a Key to Reboot

This message appears at the bottom of the screen when an error occurs that requires you to reboot. Press any key to reboot the system.

Press “F1” to Disable NMI, “F2” to Reboot

When the BIOS detects a non-maskable interrupt condition during boot, you can disable the NMI and continue to boot, or you can reboot the system with the NMI enabled.

RAM Parity Error - Checking for Segment ...

Indicates a parity error in the random access memory.

Should Be Empty But EISA Board Found - Please Run EISA Configuration Utility

A valid board ID was found in a slot that was configured as having no board ID.

Note:

When this error appears, the system boots in ISA mode so that you can run the EISA configuration utility.

Should Have EISA Board but not Found - Please Run EISA Configuration Utility

The board installed is not responding to the ID request, or no board ID has been found in the indicated slot.



Note:

When this error appears, the system boots in ISA mode so that you can run the EISA configuration utility.

Slot not Empty

Indicates that a slot designated as empty by the EISA Configuration Utility actually contains a board.



Note:

When this error appears, the system boots in ISA mode so that you can run the EISA configuration utility.

System Halted, <CTRL-ALT-DEL> to Reboot ...

Indicates that the present boot attempt has been aborted and that the system must be rebooted. Press and hold down the “CTRL” and “ALT” keys and press “DEL”.

Wrong Board in Slot - Please Run EISA Configuration Utility

The board ID does not match the ID stored in the EISA non-volatile memory.



Note:

When this error appears, the system boots in ISA mode so that you can run the EISA configuration utility.

4.14 POST Codes

ISA and PCI POST codes are routed to port address 80H.

Table 4-10: Early POST Codes before System BIOS is Shadowed

POST Code	Action
Reset	RTC & KBC initialization
0CFh	Early CPU Detection
0C0h	Early Chipset initialization
0C1h	Memory presence test: detects memory modules and programs chipset accordingly
0C6h	L2 Cache sizing test
0C3h	Decompresses Bios
0C5h	Shadows Main Bios and jumps to POST

Table 4-11: Normal POST Codes after System BIOS is Shadowed

POST Code	Action
03h	Set 40h, 72h to 1234h if it was a warm boot
04h	Reserved
05h	SuperIO early programming Clear Screen Initializes KBC
06h	Tests whether F000-Segment read/writeable Detects flash type
07h	Tests CMOS access If supported: Test if overide key (Insert) pressed during reset
08h 0BEh	-- Programs chipset defaults
09h	Reads CPU ID Cache initialization if necessary If supported: Restores CMOS from flash backup if required
0Ah	Initializes interrupt vectors Copies CMOS to stack If supported: Checks for dual processor

Table continued on following page

Table 4-11: Normal POST Codes after System BIOS is Shadowed

POST Code	Action
0Bh	Detects Coprocessor Initializes Power Management chipset Updates CPU microcode if P6 CPU Reads existing ESCD Scans PCI devices and busses, assigns I/O and Memory to PCI devices Initializes Clock generator Initializes Hardware monitoring / temperature sensor
0Ch	Initializes keyboard buffer in BDA
0Dh 0BFh 0Dh	-- Program chipset Measures CPU core speed Initializes VGA video If VGA video not found: Checks for CGA If none found: Beepcode -..
0Eh	If CGA video found: Checks video memory If supported: Tries to init Award preboot agent If supported: Shows graphic logo, otherwise shows EPA logo If not full screen graphic logo, shows copyright message and CPU type and speed If ISA VGA video: Switches on ISA video ROM shadowing
0Fh	Tests DMA Channel 0
10h	Tests DMA Channel 1
11h	Tests DMA Page Registers
12h	--
13h	--
14h	Tests and init timer (8254)
15h	If not warm boot: tests MasterPIC mask register bits
16h	If not warm boot: tests SlavePIC mask register bits
17h	--
18h	Tests PIC's by use of timer. Restores timer
19h	--
1Ah	--
1Bh	--
1Ch	--
1Dh	--
1Eh	--

Table continued on following page

Table 4-11: Normal POST Codes after System BIOS is Shadowed

POST Code	Action
30h	Measures total memory size
31h	Initialize USB Tests all memory above 1MB, shows memory size
32h	Scans for ISA PnP devices, isolates and assigns CSN to ISA PnP devices Disables SuperIO COM/LPT ports Detects and records COM/LPT ports Programs Super IO according to setup and detects any other COM/LPT ports present in the system Programs Audio system Initializes chipset EIDE channels
33h	--
34h	--
35h	--
36h	--
37h	--
38h	--
39h	--
3Ah	--
3Bh	--
3Ch	Enables going to setup
3Dh	Installs PS/2 mouse if present If ACPI supported: checks for compressed ACPI table
3Eh	Attempts to enable L2 Cache
3Fh	--
40h	--
41h 0BFh	-- Programs chipset Chipset auto configuration if required SuperIO COM/LPT auto configuration if required Records system device nodes Assigns resources to ISA PnP devices Installs Floppy disk
42h	Installs EIDE hard disk and ATAPI drives
43h	Checks and initializes COM/LPT ports
44h	--

Table continued on following page

Table 4-11: Normal POST Codes after System BIOS is Shadowed

POST Code	Action
45h	Initializes coprocessor
46h	--
47h	Saves boot_sector_buffer
48h	--
49h	--
4Ah	--
4Bh	--
4Ch	--
4Dh	--
4Eh	Checks for USB keyboard Displays previously detected POST errors. If any, checks for "Halt on" condition setting and if necessary, waits for keys "F1" or "Del".
4Fh	Checks for password entry if necessary
50h	Saves CMOS values in stack back to CMOS
51h	Switches all ISA PnP devices into "Wait For Key" state
52h	USB final initialization Decompresses embedded PCI Option ROM's Assigns IRQ's to PCI devices Programs onboard SCSI if present and activated If ACPI supported: Decompresses and installs ACPI table Checks for and runs non-video option ROM's Switches on ISA option ROM shadowing Fetches and runs embedded SCSI Option ROM's Fetches and runs embedded ISA Option ROM's Disables unused shadow areas Releases lower 32KB of E000 Segment
53h	--
54h	--
55h	--
56h	--
57h	--
58h	--
59h	--
5Ah	--
5Bh	--

Table continued on following page

Table 4-11: Normal POST Codes after System BIOS is Shadowed

POST Code	Action
5Ch	--
5Dh	--
5Eh	--
5Fh	--
60h	Prepares EIDE/ATAPI/SCSI for boot
61h	Sets speed turbo/deturbo Final chipset initialization Final power management initialization Clears screen Shows system info
62h	Programs keyboard numlock/typerate
63h	Builds ESCD and saves ESCD in flash Checks for correct century in CMOS Setup timer tick in BDA Clears any pending keys in BDA Flushes cache Releases upper 32KB of E000 Segment if Award Preboot Agent not present and active
0FFh	Boot

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Appendix A

CP-RIO3-01 Rear I/O Module

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A. CP-RIO3-01 Rear I/O Module

A.1 Overview

The CP302 family (CP302, CP302-PM and CP301) provides optional Rear I/O connectivity for peripherals, a feature which may be particularly useful in specialised CompactPCI systems. Some standard PC interfaces are implemented and assigned to the front panel and to the rear connector J2.

When the Rear I/O module is used, the signals of some of the main board/front panel connectors are routed to the module interface. Thus the Rear I/O module makes it much easier to remove the CPU in the rack as there is practically no cabling on the CPU board.

For the system Rear I/O feature a special backplane is necessary. The CPU board with Rear I/O is compatible with all standard CompactPCI passive backplanes with Rear I/O support on the system slot.

The CP-RIO3-01 Rear I/O provides the following interfaces, all signals are available via jumper J2 .

32-bit CompactPCI and Rear I/O

- 32-bit/33 MHz CompactPCI
- PS/2 keyboard
- PS/2 mouse
- Two USB ports
- Ethernet port without LED
- Two COM ports
- VGA CRT interface
- Second EIDE port
- Fan control input

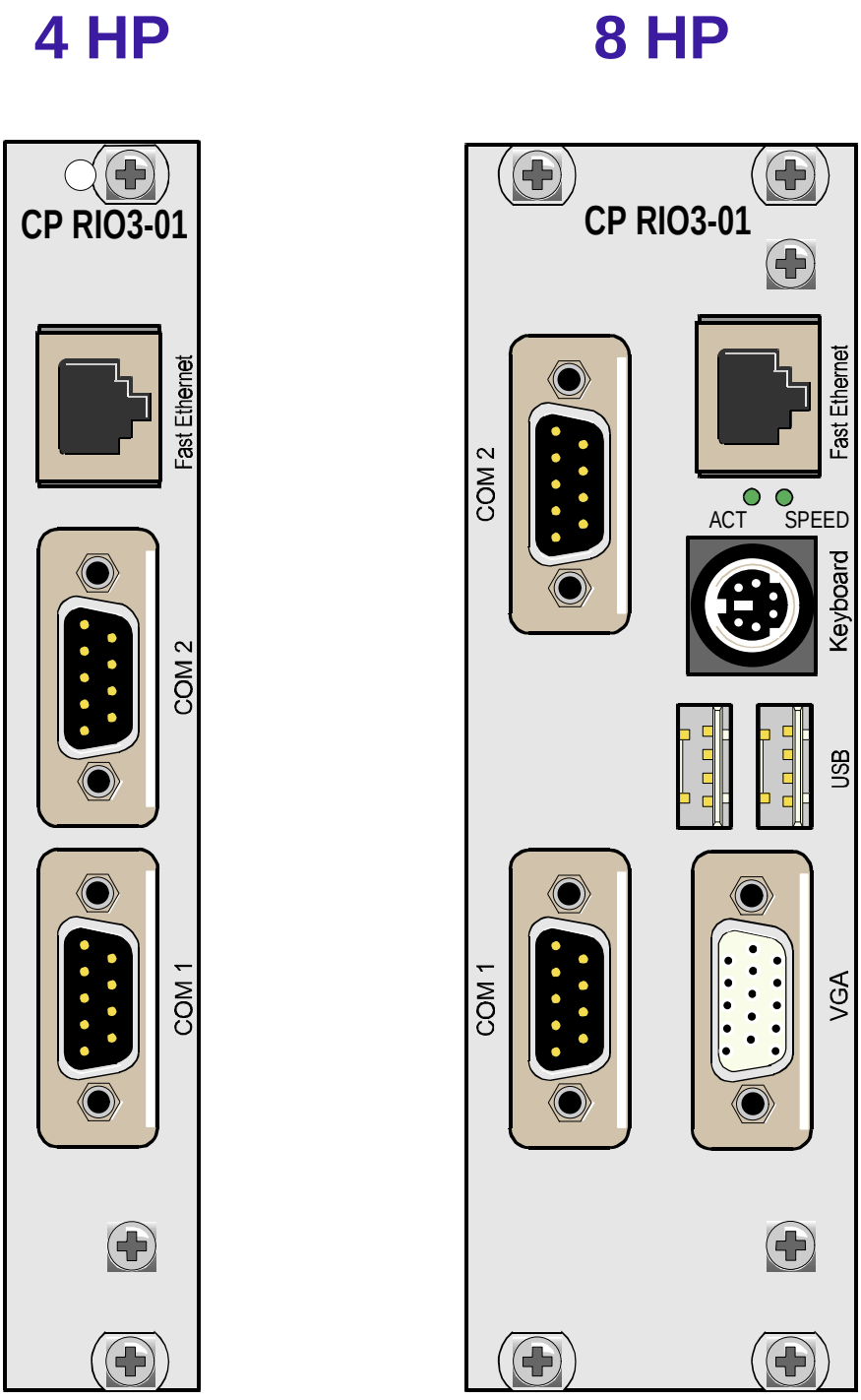
The following ports may be used either for rear or front I/O, the combination of both rear and front is not possible.

- Ethernet port without LED
- Two COM ports
- VGA CRT interface
- Second EIDE port

A.2 Front Panels

Note that the two green Ethernet LED's are not active on the CP-RIO3-01.

Figure A-1: CP-RIO3-01 Front Panels, 4HP and 8HP Versions



A.3 Board Layouts: 4HP and 8HP Versions

Figure A-2: CP-RIO3-01 4HP Version Board Layout

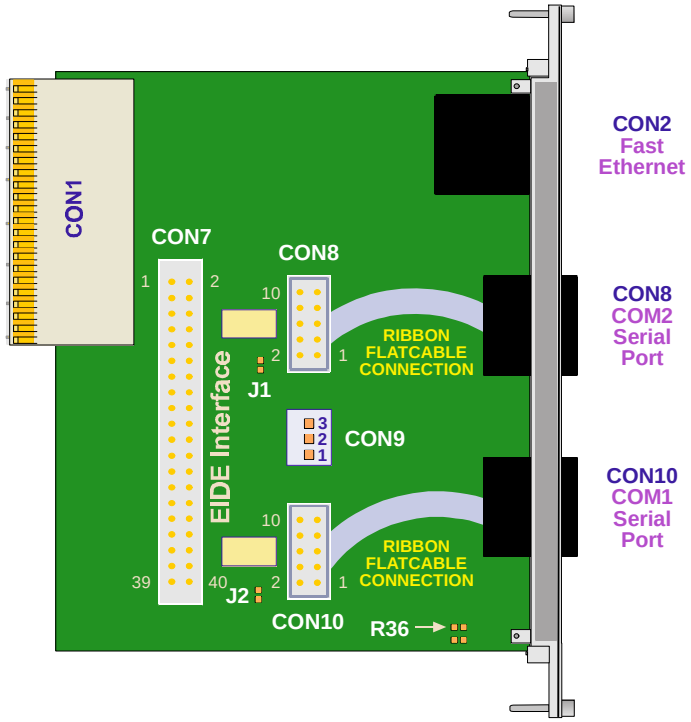
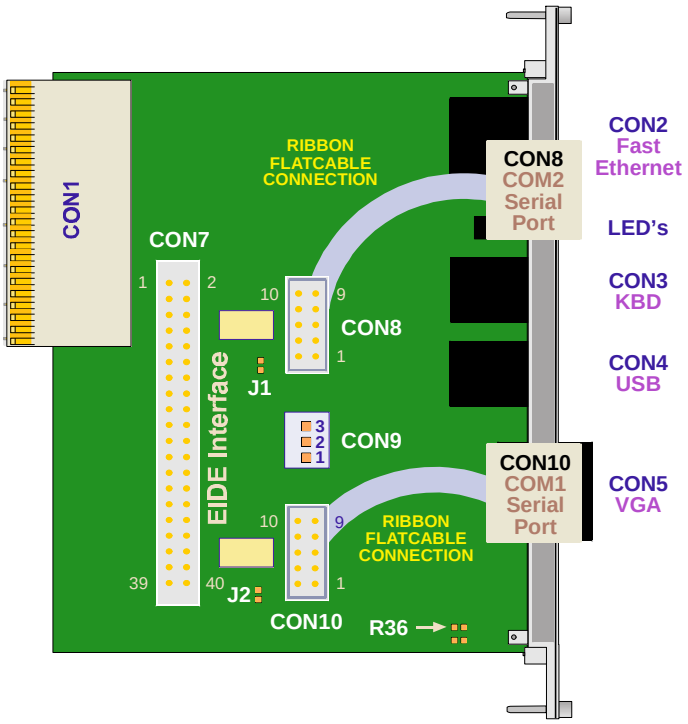


Figure A-3: CP-RIO3-01 8HP Version Board Layout



A.4 Module Interfaces

A.4.1 Keyboard/Mouse Interface

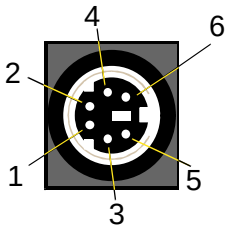


Figure A-4: Keyboard/Mouse Connector

The PC/AT standard keyboard/mouse connector is a PS/2-type 6-pin shielded mini-DIN connector. The keyboard power supply unit is protected by a 500 mA fuse. All signal lines are EMI-filtered.

A special adapter to connect a mouse device and/or a keyboard to the PS/2 connector ia available from *PEP*

A.4.1.1 Keyboard Connector CON3 Pinout

The CP-RIO3-01 (8HP version) has the AT keyboard connector implemented on a 6-pin Mini-Din connector.

A special adapter to connect a mouse device and/or keyboard to the PS/2 connector is available from *PEP*.

Table A-1: Keyboard Connector CON3 Pinout

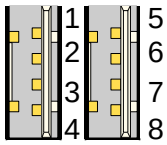
Pin	Name	Function	In/Out
1	KDATA	Keyboard data	In/Out
2	MDATA	Mouse data	In/Out
3	GND	Ground signal	--
4	VCC	VCC signal	--
5	KCLK	Keyboard clock	Out
6	MCLK	Mouse clock	Out

Note:

The keyboard power supply is protected with a fuse (500mA) and all the signal lines are EMI-filtered.

A.4.2 USB Interfaces

Figure A-5: USB Connector CON4



There are two identical USB interfaces on the CP-RIO3-01 module (8HP version) each with a maximum transfer rate of 12 Mbit provided for connecting USB devices. One USB peripheral may be connected to each port. To connect more than two USB devices an external hub is required.

A.4.2.1 USB Connector CON4 Pinout

Table A-2: USB Connector CON4 Pinout

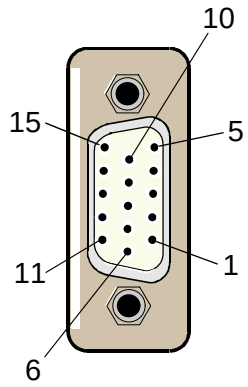
Pin	Name	Function	In/Out
1	VCC	VCC signal	--
2	UV0-	Differential USB-	--
3	UV0+	Differential USB+	--
4	GND	GND signal	--
5	VCC	VCC signal	--
6	UV0-	Differential USB-	--
7	UV0+	Differential USB+	--
8	GND	GND signal	--

Note:

The USB power supply feeding the two ports is protected by a 1.5 A fuse. All signal lines are EMI-filtered.

A.4.3 VGA Interface

Figure A-6: D-sub VGA Connector



A.4.3.1 VGA Connector CON5 Pinout

The 15-pin female connector CON5 is used to connect a VGA monitor to the CP-RIO3-01 (8HP version) board.

Table A-3: VGA Connector CON5 Pinout

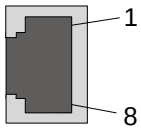
D-sub 15	Signal	Function	In/Out
1	Red	Red video signal output	Out
2	Green	Green video signal output	Out
3	Blue	Blue video signal output	Out
13	Hsync	Horizontal sync.	TTL out
14	Vsync	Vertical sync.	TTL out
12	Sdata	Not supported	In/Out
15	Sclk	Not supported	Out
9	VCC	Power +5V 200 mA no fuse protection	Out
5,6,7,8,10	GND	Signal ground	--
4,11	Free	--	--

Note:

The 75 Ohm termination resistors for the three VGA signals (red, green, blue) are located on the baseboard.

A.4.4 Fast Ethernet Interface

Figure A-7: Ethernet/Fast Ethernet Connector



The Ethernet connector is realized as an RJ45 twisted-pair connector. The interface provides automatic detection and switching between 10Base-T and 100Base-TX data transmission.

A.4.4.1 RJ45 Connector CON2 Pinout

CON2 supplies the 10Base-TX/100Base-TX interface to the Ethernet controller.

Table A-4: RJ45 Connector CON2 Pinout

RJ45	Signal	Function
1	TX+	Transmit +
2	TX-	Transmit -
3	RX+	Receive +
4	NC	--
5	NC	--
6	RX-	Receive -
7	NC	--
8	NC	--

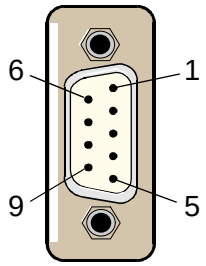
A.4.5 Ethernet LED Status

Important note:

The two green Ethernet LED's are not active on the CP-RIO3-01.

A.4.6 Serial Port Interfaces

Figure A-8: PC-compatible D-sub Serial Interface



A.4.6.1 Serial Port Connectors CON8 and CON10 Pinouts

The serial port male connectors CON2 and CON6 allow the connection of RS232 devices to the CP-RIO3-01 board.

Table A-5: Serial Port Connectors CON8 and CON10 Pinouts

DSUB 9	Signal	Function	In/Out
1	DCD	Data carrier detect	In
2	RXD	Receive data	In
3	TXD	Transmit data	Out
4	DTR	Data terminal ready	Out
5	GND	Signal ground	--
6	DSR	Data send request	In
7	RTS	Request to send	Out
8	CTS	Clear to send	In
9	RI	Ring indicator	In

Note:

To ensure the proper functioning of the Rear I/O serial interfaces, the drivers for COM1 and COM2 on the CP302 I/O module must be disabled.

A.4.7 Fan Control Interface (optional)

A fan for CPU cooling can be connected via the power connector CON9.

A4.7.1 Fan Control Connector CON9 Pinout

Table A-6: Fan Control Connector CON9 Pinout

Pin	Function
1	Ground
2	5V Fan Supply Voltage at a maximum current of 300 mA
3	Fansense

A.4.8 EIDE Interface

A.4.8.1 EIDE Connector EIDE2 (CON7) Pinout

The following table sets out the pin numbers of connector CON7 and sets out its corresponding signal names and functions.

Table A-7: Pinout of AT Standard Connector EIDE2

Pin	Signal	Function	In/Out
1	IDERESET	Reset HD	Out
2	GND	Ground signal	--
3	HD7	HD data 7	In/Out
4	HD8	HD data 8	In/Out
5	HD6	HD data 6	In/Out
6	HD9	HD data 9	In/Out
7	HD5	HD data 5	In/Out
8	HD10	HD data 10	In/Out
9	HD4	HD data 4	In/Out
10	HD11	HD data 11	In/Out
11	HD3	HD data 3	In/Out
12	HD12	HD data 12	In/Out
13	HD2	HD data 2	In/Out

Table continued on following page

Table A-7: Pinout of AT Standard Connector EIDE2

Pin	Signal	Function	In/Out
14	HD13	HD data 13	In/Out
15	HD1	HD data 1	In/Out
16	HD14	HD data 14	In/Out
17	HD0	HD data 0	In/Out
18	HD15	HD data 15	In/Out
19	GND	Ground signal	--
20	N/C	--	--
21	IDEDRQ	DMA request	In
22	GND	Ground signal	--
23	IOW	I/O write	Out
24	GND	Ground signal	--
25	IOR	I/O read	Out
26	GND	Ground signal	--
27	IOCHRDY	I/O channel ready	In
28	GND	Ground signal	--
29	IDEDACKA	DMA Ack	Out
30	GND	Ground signal	--
31	IDEIRQ	Interrupt request	In
32	N/C		--
33	A1	Address 1	Out
34	N/C	--	--
35	A0	Address 0	Out
36	A2	Address 2	Out
37	HCS0	HD select 0	Out
38	HCS1	HD select 1	Out
39	LED	LED driving	In
40	GND	Ground signal	--

A.4.9 Rear I/O interface on Compact PCI Connector CON1

The CP-RIO3-01 conducts a wide range of I/O signals through the Rear I/O connector J2.

Note:

If the Rear I/O feature is selected the PCI interface is only 32-bit. For the 3U Rear I/O a special backplane is necessary.

A.4.9.1 Compact PCI Connector CON1 Pinout

Table A-8: Rear I/O CompactPCI Bus Connector J2 (CON1) Pinout

Pin	Z	A	B	C	D	E	F
22	GND	GA4	GA3	GA2	GA1	GA0	GND
21	GND	CLK6	GND	TDN 1)	RDN 1)	RDP 1)	GND
20	GND	CLK5	GND	TDP 1)	GND	VCC 1)	GND
19	GND	GND	GND	RSV 5)	RSV 5)	+3.3V 1)	GND
18	GND	KDAT 1)	UV0- 1)	UV1+ 1)	Battery 6)	+3.3V 1)	GND
17	GND	KCLK 1)	ROUT (GND) 3)	PRST	REQ6	GNT6	GND
16	GND	PMDAT 1)	UV0+ 1)	DEG	GND	UV1- 1)	GND
15	GND	PMCLK 1)	GOUT (GND) 3)	FAL	REQ5	GNT5	GND
14	GND	2RIN 2)	2DSR 2)	2RTS 2)	VSYNC (GND) 3)	2CTS 2)	GND
13	GND	2RXD 2)	FANSENSE (GND)	BOUT (VIO) 3)	2DTR 2)	2DCD 2)	GND
12	GND	1DSR 2)	1RTS 2)	1CTS 2)	HSYNC (GND) 3)	2TXD	GND
11	GND	1DTR 2)	GND	IDEDB9 (VIO) 4)	1DCD 2)	1RIN 2)	GND
10	GND	IDEDB8 4)	IDERST 4)	1TXD 2)	IDEDB10 (GND) 4)	1RXD 2)	GND
9	GND	IDEDB6 4)	IDEDB7 (GND) 4)	IDEDB4 (VIO) 4)	IDEDB5 4)	IDEDB11 4)	GND
8	GND	IDEDB3 4)	IDEDB12 4)	IDEDB2 4)	GND	IDEDB1	GND
7	GND	IDEDB14 4)	IDEDB0 (GND) 4)	IDEDB15 (VIO) 4)	IDEDRQB 4)	IDEIOWB	GND
6	GND	IDEIORB 4)	ICHRDYB 4)	IDACKB 4)	IDEDB13 (GND) 4)	IDEIRQB 4)	GND
5	GND	IDEAB1 4)	GND	IDAB0 (VIO) 4)	IDEAB2 4)	LED 6)	GND
4	GND	VIO	VCC 1)	IDECSB0 4)	GND	IDECSB1 4)	GND
3	GND	CLK4	GND	GNT3	REQ4	GNT4	GND
2	GND	CLK2	CLK3	SSYSEN	GNT2	REQ3	GND
1	GND	CLK1	GND	REQ1	GNT1	REQ2	GND

Legend for table on preceding page**:**

1) Ethernet, SMBUS, Keyboard, Mouse, USB and Power (64-bit and Rear I/O possible)

2) COM1, COM2 (only 32-bit and Rear I/O)

3) VGA Signals (only 32-bit and Rear I/O)

4) EIDE Port (only 32-bit and Rear I/O)

5) Reserved

6) The battery and LED signals are active only on the CP301 and CP302-PM

The greyed table cells indicate the power grouping

A.5 Jumper Setting

A.5.1 COM Port Configuration

The two COM ports are configured using solder jumpers J1 and J2

A.5.1.1 COM1 Configuration

Table A-9: COM1 Configuration using Jumper J2

J2	Function
Open	*RS232 enabled*
Closed	RS232 disabled

The default setting is indicated by italics.

A.5.1.2 COM2 Configuration

Table A-10: COM2 Configuration using Jumper J1

J1	Function
Open	*RS232 enabled*
Closed	RS232 disabled

The default setting is indicated by italics.

A.5.2 Shorting Chassis GND (Shield) to Logic GND

The front panel including the front panel connectors are isolated to the logic ground. This zero Ohm resistor enables connection between the chassis GND and logic GND.

Table A-11: Shorting Chassis GND (Shield) to Logic GND

R36	Function
Open	*Connectors are isolated to logic GND*
Short	Connectors are connected to logic GND and chassis GND

The default setting is indicated by italics.