Modular Computers®

CP371

16 Channel CompactPCI
Analog Input Controller

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The product described in this manual is in compliance with all applied CE standards.

Revision History

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01	Initial Issue	00	Oct 2001
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Imprint

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This manual was realized by: **TPD/Engineering, PEP Modular Computers GmbH**.

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CE Conformity

This symbol indicates that the product described in this manual is in compliance with all applied CE standards. Please refer also to the section “Applied Standards” in this manual.



Caution, Electric Shock!

This symbol and title warn of hazards due to electrical shocks (> 60V) when touching products or parts of them. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your material.

Please refer also to the section “High Voltage Safety Instructions” on the following page.



Warning, ESD Sensitive Device!

This symbol and title inform that electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Please read also the section “Special Handling and Unpacking Instructions” on the following page.



Warning!

This symbol and title emphasize points which, if not fully understood and taken into consideration by the reader, may endanger your health and/or result in damage to your material.



Note...

This symbol and title emphasize aspects the reader should read through carefully for his or her own advantage.

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Your new *PEP* product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new *PEP* product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions



Warning!

All operations on this device must be carried out by sufficiently skilled personnel only.



Caution, Electric Shock!

Before installing your new PEP product into a system always ensure that your mains power is switched off. This applies also to the installation of piggybacks.

Serious electrical shock hazards can exist during all installation, repair and maintenance operations with this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing work.

Special Handling and Unpacking Instructions



ESD Sensitive Device!

Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory back-up, ensure that the board is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the board.

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General Instructions on Usage

In order to maintain PEP's product warranty, this product must not be altered or modified in any way. Changes or modifications to the device, which are not explicitly approved by *PEP Modular Computers* and described in this manual or received from PEP Technical Support as a special handling instruction, will void your warranty.

This device should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This applies also to the operational temperature range of the specific board version, which must not be exceeded. If batteries are present their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, please follow only the instructions supplied by the present manual.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the board please re-pack it as nearly as possible in the manner in which it was delivered.

Special care is necessary when handling or unpacking the product. Please, consult the special handling and unpacking instruction on the previous page of this manual.

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Chapter 0

Introduction

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1. Introduction

1.1 System Overview

The CompactPCI board described in this manual operates with the PCI bus architecture to support additional I/O and memory-mapped devices as required by various industrial applications. For detailed information concerning the CompactPCI standard, please consult the complete Peripheral Component Interconnect (PCI) and CompactPCI Specifications. For further information regarding these standards and their use, visit the homepage of the *PCI Industrial Computer Manufacturers Group (PICMG)*.

Many system relevant CompactPCI features that are specific to PEP Modular Computers CompactPCI systems may be found described in the PEP CompactPCI System Manual. Please refer to the section “Related Publications” at the end of this chapter for the relevant ordering information.

The CompactPCI System Manual includes the following information:

- Common information that is applicable to all system components, such as safety information, warranty conditions, standard connector pinouts etc.
- All the information necessary to combine PEP’s racks, boards, backplanes, power supply units and peripheral devices in a customized CompactPCI system, as well as configuration examples.
- Data on rack dimensions and configurations as well as information on mechanical and electrical rack characteristics.
- Information on the distinctive features of PEP CompactPCI boards, such as functionality, hot swap capability. In addition, an overview is given for all existing PEP CompactPCI boards with links to the relating data sheets.
- Generic information on the PEP CompactPCI backplanes, such as the slot assignment, PCB form factor, distinctive features, clocks, power supply connectors and signalling environment, as well as an overview of the PEP CompactPCI standard backplane family.
- Generic information on the PEP CompactPCI power supply units, such as the input/output characteristics, redundant operation and distinctive features, as well as an overview of the PEP CompactPCI standard power supply unit family.

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1.2 Product Overview

The CP371 Analog Input Controller is a part of a comprehensive concept to provide CompactPCI system integrators with a complete range of CompactPCI I/O products which include the functions of analog input, analog output, digital input, and digital output implemented as separate individual boards. This concept ensures a maximum degree of system design flexibility thus allowing efficient and effective usage of available resources.

The basic functions of this board are to provide interfacing to the application (process), perform analog to digital signal conversion, and to make the raw digitized data along with gain and offset correction data available for further processing. The major components involved in these processes are the front end (process side) signal conditioning, an analog to digital converter (ADC), and the Analog to Digital Conversion Process and Communications (ADC ProComm) controller which is realized in a field-programmable gate array (FPGA). The ADC ProComm Controller is designed to provide effective and efficient control of the analog to digital conversion process as well as interfacing to the CPCI System Controller.

The following table provides a quick overview of the CP371 board.

Table 1-1: CP371 Product Overview

CP371 FEATURES	DESCRIPTION
Analog Input Board	• CompactPCI: 3U, 4HP • 33 MHz system clock • 32-bit address and data bus • Designed for Plug and Play • Complies with the CPCI specification
Input Signals	• Voltages: Single-Ended (0 to 5V, 0 to 10V) and Differential (± 5V, ± 10V) • Current: 0 to 20 mA and 4 to 20 mA
Output Data	• Raw digitalized data (of analog input), 12-bit resolution • Gain correction data • Offset correction data
Monitor and Control	• Cluster active LED's • ADC ProComm controller • System Master driver software

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1.3 Board Overview

1.3.1 Board Introduction

The CP371 is a 16 channel (dual cluster, eight channels each) analog input board. The sources of the analog inputs presented to the board may either be a voltage or current generator. The board accepts either single-ended or differential voltages. Currents of up to 20 mA are converted to a single-ended voltage prior to further processing.

Input signal processing begins with the presentation of the signal to the front panel connector. Signal conditioning prior to analog to digital conversion includes: conversion of current signals to single-ended voltage signals; low-pass filtering and over voltage protection; differential to single-ended voltage conversion, input offsetting, and gain correction. After analog to digital conversion, the raw digitized analog data is transferred from the ADC to the ADC ProComm controller where calibrated gain and offset data are made available for further processing. The ADC ProComm controller is not only responsible for controlling data acquisition, it also controls the interface to the CompactPCI bus.

Input signal types and ranges are as follows:

- Voltages:
  - Single-ended:
    - 0 to 5 V
    - 0 to 10 V
  - Differential:
    - ± 5 V
    - ± 10 V
- Currents:
  - 0 to 20 mA
  - 4 to 20 mA

Output data are:

- Raw digitized analog input data
- Gain correction data
- Offset correction data

1.3.2 Board Specific Information

Specific board components involved in the analog to digital conversion and data handling process are:

- One front panel connector (62-pin, female, D-Sub type)
- Sixteen channels of input signal conditioning
- Two, 12-bit ADC's (one for each cluster of 8 channels each)
- Four optocouplers (serial data and control signals, two for each cluster)
- One FPGA (the ADC ProComm controller)
- One CompactPCI bus connector (J1, board to backplane, 132-pin, female, six row)
- One JTAG/ISP on board programming connector (10-pin, male, dual row)
- Two DC/DC converters (isolation)
- One EEPROM (Capability ROM)

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1.4 System Relevant Information

The following system relevant information is general in nature but should still be considered when developing applications using the CP371.

Table 1-2: System Relevant Information

SUBJECT	INFORMATION
System Configuration	The CP371 operates with a system clock frequency of 33 MHz. The number of CP371's which can be installed in any one system depends solely on the number of CPCI slots available.
Master/Slave Functionality	The CP371 functions only as a slave. As such it requires a system master for servicing.
System Controller	The CP371 cannot function as a system controller.
Analog Inputs	Analog inputs to the CP371 must conform to the inputs specifications set forth in this manual for the CP371. In most cases, some form of signal conditioning will be required on the process side prior to a signal being presented to the CP371.

1.4.1 System Configuration

When implementing applications, precautions must be taken to ensure that the input signals presented to the CP371 comply with the specifications set forth in this manual. For this reason it will be necessary for most applications to provide signal conditioning prior to presenting the analog input to the CP371. In addition, it is imperative that signal interference be kept to a minimum. Refer to chapters 4 and 5 for further information.

1.4.2 Driver Software

The CP371 is supplied with appropriate driver software which provides software interfacing to the system master.

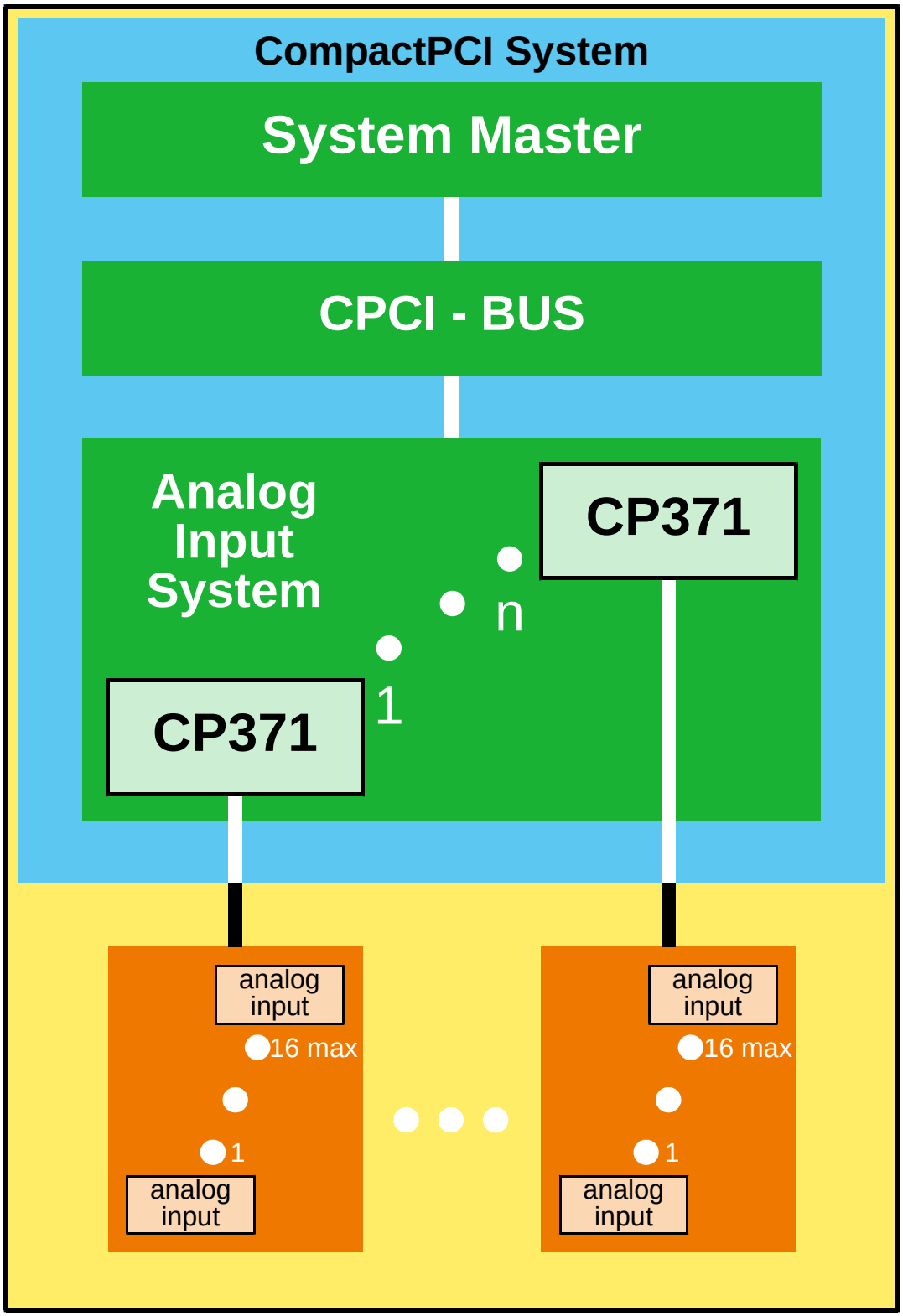
1.5 Board Diagrams

The following diagrams provide additional information concerning board functionality and component layout.

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1.5.1 System Level Interfacing

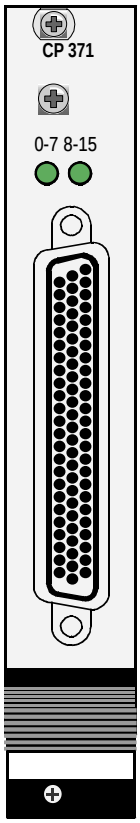
Figure 1-1: CP371 System Level Interfacing Diagram



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1.5.2 Front Panels

Figure 1-2: CP371 Front Panel



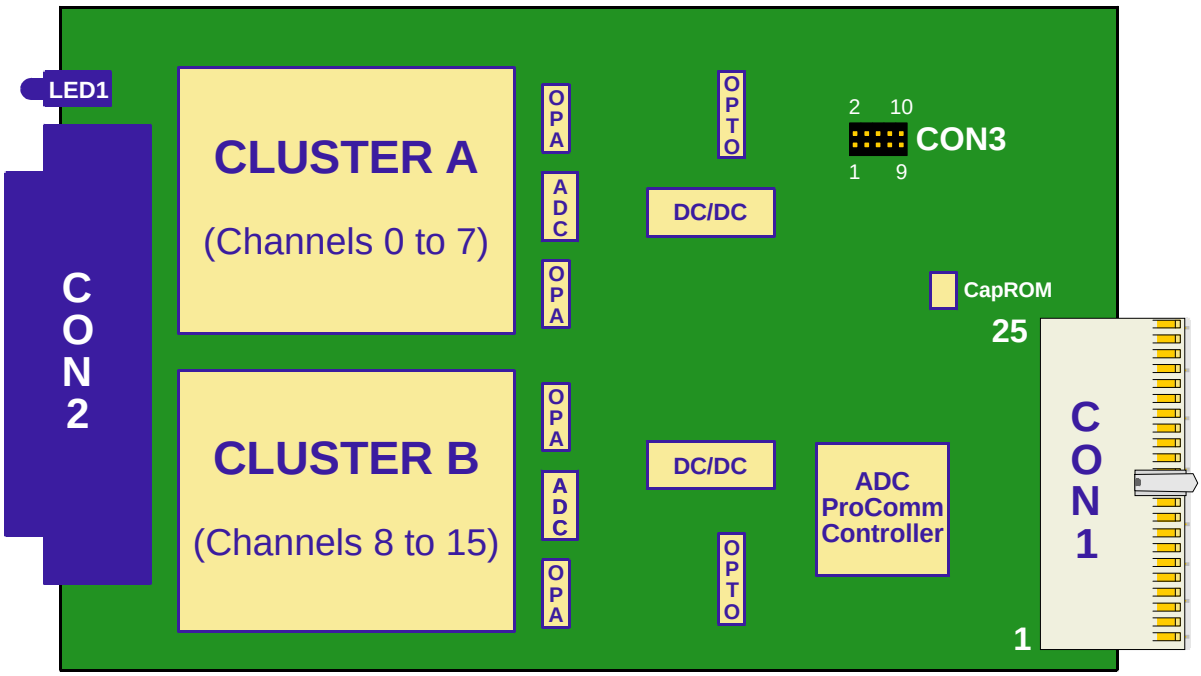
LEGEND:

0-7 when LED is active: cluster A is activated

8-15 when LED is active: cluster B is activated

1.5.3 Board Layout

Figure 1-3: CP371 Board (Front View)



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1.6 Technical Specifications

Table 1-3: CP371 Main Specifications

GROUP	TYPE	DESCRIPTION
ADC ProComm Controller and Related	FPGA Logic Device	Provides PCI interfacing and IO control logic
Peripheral Memory	CapROM	4 kBit (512 byte) EEPROM
External Interfaces	Analog Input	One, 62-pin, female, three row, D-sub connector Supports up to sixteen analog input channels
	CPCI Bus	One, 132-pin, female, six row connector (standard CPCI type connector for J1)
Internal Interfaces	JTAG/ISP	JTAG/ISP 10-pin SMD connector for programming and testing purposes
Indicators	Front Panel LED	Two, green LED's for indicating cluster operation status (enabled or disabled)
General	Mechanical	Conforms with IEEE 1101.1
	Power Requirements	Voltages: 3.3 V 5 V VCC
	Power Consumption	Voltages: 3.3 V = 0.132 W 5 V = 1.9 W
	Temperature Range	Operational: 0ºC to +70ºC Standard -40ºC to +85ºC E2 Storage: -55ºC to +125ºC
	Humidity	0% to 95% non-condensing
	Dimensions	100 mm x 160 mm single height Eurocard
	Board Weight	152 g (2 cluster configuration)
Software Driver Information (See note below)	PCI Header	Device ID: 0x5555 Vendor ID: 0x1556 Class Code: 0x118000 Subsystem Device ID: 0x00D0 Subsystem Vendor ID: 0x1518

Note...



The Device ID and Vendor ID refer to the chip manufacturer. In the Class Code value given, "11" relates to the data acquisition and signal processing controllers and "8000" relates to the Analog IO modules. Subsystem Device ID and Subsystem Vendor ID are defined by PEP.

In addition, the CP371 uses 64kB in PCI memory space, BAR0, is not prefetchable, and no interrupts are used.

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Table 1-4: CP371 Analog Input Specifications

TYPE	DESCRIPTION
Input Types / Ranges	VOLTAGES: Single-ended: 0 to 5 V 0 to 10 V Differential: ± 5 V ± 10 V CURRENTS: 0 to 20 mA 4 to 20 mA
Channels	Standard: 16 channels total (two clusters of 8 channels each) Optional: 8 channels total (one cluster of 8 channels)
Channel Connections	Sixteen pairs of dedicated connector pins for plus and minus; sixteen separate pins for configuring on board shunt resistors for current inputs; twelve ground pins distributed over the connector
Conversion	Continuous serial sampling of input channels, serial multiplexed output of the ADC; single measurement buffering for each channel in the ADC ProComm controller
Throughput Rate	13.9 kHz per channel
Resolution	12 bit
Accuracy	See table 1-5
Input Filter (edge frequency)	15 kHz for single-ended 20 kHz for differential
Input Protection	8 kV ESD
Over Voltage/Current Protection	Voltage: ± 24 V maximum Current: 30 mA maximum
Isolation	2 kV process to system
Input Impedance	Voltage: 450 k ohm Current: 250 ohm

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Table 1-5: CP371 Accuracy

	INPUT TYPE and RANGE	SIGNAL ACCURACY at 23°C ± % of FULL SCALE	ACCUMULATING DEVIATION % per K (S and E1 BOARDS	ACCUMULATING DEVIATION % per K (E2 BOARDS
BASIC ACCURACY	0 V – 5 V	< 0.0488	< 0.0006	< 0.0006
	0 V – 10 V	< 0.0244	< 0.0004	< 0.0004
	- 5 V – + 5 V	< 0.0244	< 0.0004	< 0.0004
	- 10 V – + 10 V	< 0.0244	< 0.0004	< 0.0004
	0 mA – 20 mA	< 0.0488	< 0.0006	< 0.0006
BASIC ACCURACY (statistically evaluaated)	0 V – 5 V	< 0.0244	< 0.0004	< 0.0004
	0 V – 10 V	< 0.0244	< 0.0004	< 0.0002
	- 5 V – + 5 V	< 0.0244	< 0.0004	< 0.0002
	- 10 V – + 10 V	< 0.0122	< 0.0002	< 0.0002
	0 mA – 20 mA	< 0.0244	< 0.0004	< 0.0004
PRODUCTION ACCURACY 1	VOLTAGE	< 0.15	< 0.001	< 0.001
	CURRENT	< 0.15	< 0.001	< 0.001
PRODUCTION ACCURACY 2	VOLTAGE	< 0.25	< 0.001	< 0.001
	CURRENT	< 0.25	< 0.001	< 0.001

Note:

PRODUCTION ACCURACY 1: calibration by PEP; single samples

PRODUCTION ACCURACY 2: best case calibration (not supported by PEP); mean average of samples (sample count > 100)

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1.7 Applied Standards

The *PEP Modular Computers'* CompactPCI systems comply with the requirements of the following standards:

Table 1-6: Applied Standards

	TYPE	STANDARD
CE	Emission	EN50081-1
	Immunity, Industrial Environment	EN50082-2
	Immunity, IT Equipment	EN55024
	Electrical Safety	EN60950
MECHANICAL	Mechanical Dimensions	IEEE 1101.1
ENVIRONMENTAL TESTS	Vibration, Sinusoidal	IEC68-2-6
	Random Vibration, Broadband	IEC68-2-64 (3U boards)
	Permanent Shock	IEC68-2-29
	Single Shock	IEC68-2-27

1.8 Related Publications

Table 1-7: Related Publications

	ISSUED BY	DOCUMENT
CompactPCI Systems	PICMG	CompactPCI Specification, V. 2.0, Rev. 3.0
	PEP Modular Computers	CompactPCI Systems Manual (ID 19953)

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Chapter 2

Functional Description

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2. Functional Description

The following chapters present more detailed, board level information about the CP371 analog input controller whereby the board components and their basic functionality are discussed in general.

2.1 General Information

The CP371 is comprised basically of the following:

- Signal conditioning
- Analog to digital converter
- ADC ProComm controller
  - Realized in an FPGA device
  - Controls analog data acquisition and provides interfacing to the CPCI bus
- System interfaces for:
  - Analog inputs
    - Two, 8 channel clusters: Cluster A, Cluster B
    - One, 62-pin, female, 3-pin row, D-sub connector (CON2)
  - CompactPCI bus
    - 132-pin, female, 6-pin row connector (CON1)
    - CompactPCI specification
  - Testing and program development (JTAG/ISP) connector (CON3)
- On board memory: Capability EEPROM (CapROM)
- Monitor and Control
  - Two each, green status LED's for cluster activation (channels 0-7 and 8-15)
  - Registers
- Software

2.1.1 Signal Conditioning

Analog input signal conditioning is comprised of two clusters (A and B) each of the following:

- Over-voltage and over-current protection
- Low-pass signal filtering
- Input conversion (differential and current) to single-ended
- Signal pre-conditioning (gain and offset) prior to presentation to the ADC

2.1.2 Analog to Digital Converter

For each cluster there is one, eight channel, 12-bit analog to digital converter (ADC) available. After a cluster is activated, sampling is done starting with the lowest numbered channel of the cluster until all channels have been sampled. This is repeated as long as required. Within the ADC, the sampled data is serialized and made available for further processing by the ADC Pro-Comm controller.

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2.1.3 ADC ProComm Controller

Within the CP371, the ADC ProComm controller is responsible for supervising and controlling the analog data acquisition process and providing communications with the CompactPCI system master. Applications address the CP371 through its software driver interface within the system master whereby the controller accepts requests from the driver, executes them accordingly, and supervises the analog to digital conversion process. Data from the ADC is processed through the ADC ProComm controller and then made available to the system master.

In addition to the raw digitized analog data, the ADC ProComm controller also has access to board calibration data for gain and offset error correction. This data is available to the application through the driver software.

2.1.4 System Interfaces

The CP371 provides interfacing capability for the following system elements:

- Analog input
- CompactPCI bus
- Test and program development: JTAG/ISP

Analog input interfacing is achieved via the CON2 connector. Interfacing to the CompactPCI bus is accomplished via the CON1 connector. Test and program development is supported by the CON3 connector.

2.1.5 Monitor and Control

Various monitor and control functions are available for the operation of the CP371. Two LED's are available for operator interaction. In addition, applications have access via the System Master driver software to board specific registers.

2.1.6 Software

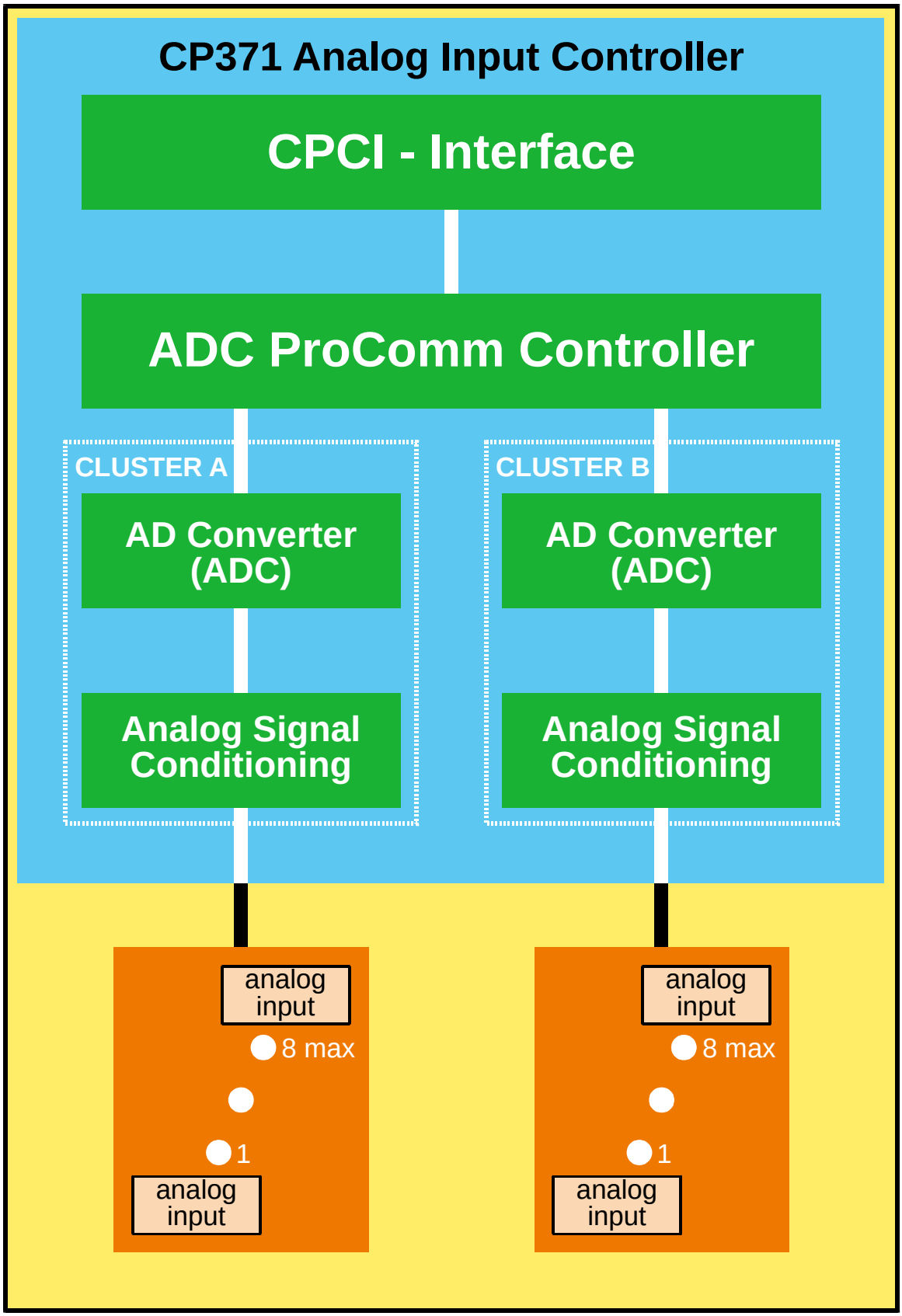
Driver software is available for the System Master application software.

2.2 Board-Level Interfacing Diagram

The following figure demonstrates the interfacing structure between the internal processing modules of the CP371 and other major CP371 system components. Where CP371 system elements have common interfacing they are grouped into a block. Interfacing common to only one element of a block is indicated with a direct connecting line. The interfacing lines are shown in white where they are on board and in black for board external interfacing.

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Figure 2-1: CP371 Board Level Interfacing



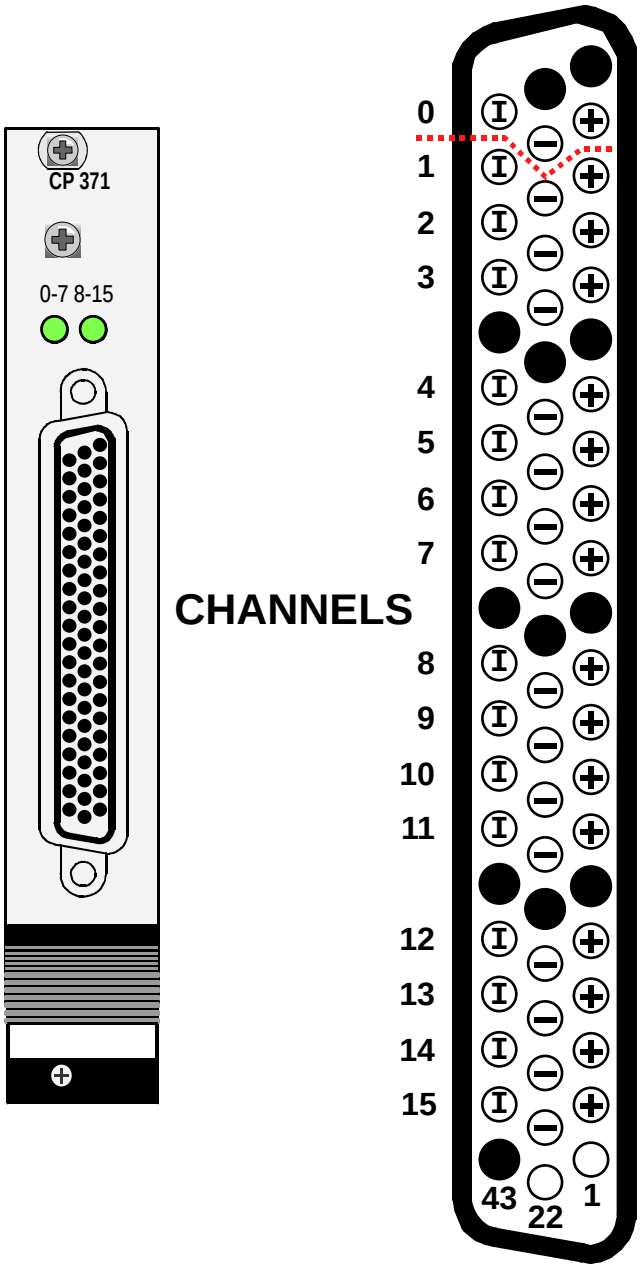
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2.3 System Interfaces

2.3.1 Analog Input Interface

The analog input interface is accomplished through the CON2 connector. The following figure and table indicate the pin layout and pinout of this connector.

Figure 2-2: Pin Layout of the Analog Input Interface Connector CON2



Pin Naming Convention:

- ● Ground (analog)
- \+ Plus
- \- Minus
- I I (current)
- O Pin not connected

Plus, minus, and I are names for these pins and **do not** indicate the polarity of the signal to be presented to the CP371.

LED's

0-7 Cluster A activated (Channels 0 to 7)

8-15 Cluster B activated (Channels 8 to 15)

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Table 2-1: Pinout of the Analog Input Interface Connector CON2

CHANNEL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
	1	NC	22	NC	43	AGND
15	2	AIN/I 15+	23	AIN15-	44	I15-
14	3	AIN/I 14+	24	AIN14-	45	I14-
13	4	AIN/I 13+	25	AIN13-	46	I13-
12	5	AIN/I 12+	26	AIN12-	47	I12-
	6	AGND	27	AGND	48	AGND
11	7	AIN/I 11+	28	AIN11-	49	I11-
10	8	AIN/I 10+	29	AIN10-	50	I10-
9	9	AIN/I 9+	30	AIN9-	51	I9-
8	10	AIN/I 8+	31	AIN8-	52	I8-
	11	AGND	32	AGND	53	AGND
7	12	AIN/I 7+	33	AIN7-	54	I7-
6	13	AIN/I 6+	34	AIN6-	55	I6-
5	14	AIN/I 5+	35	AIN5-	56	I5-
4	15	AIN/I 4+	36	AIN4-	57	I4-
	16	AGND	37	AGND	58	AGND
3	17	AIN/I 3+	38	AIN3-	59	I3-
2	18	AIN/I 2+	39	AIN2-	60	I2-
1	19	AIN/I 1+	40	AIN1-	61	I1-
0	20	AIN/I 0+	41	AIN0-	62	I0-
	21	AGND	42	AGND		

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2.3.2 CPCI Interface and Pinout

The CPCI interface is based on the specification PICMG 2.0 R 3.0, 10/1/99. The following figure and table indicate the pin layout and pinout of the CPCI connector, CON1 (J1).

Figure 2-3: CPCI Connector CON1 (J1)

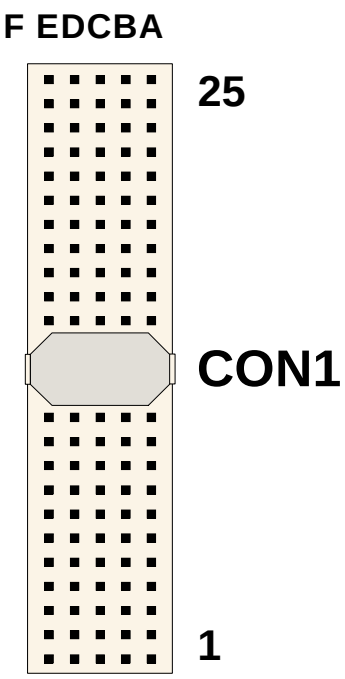


Table 2-2: CPCI Connector CON1 (J1)

PIN	PIN ROW					
	A	B	C	D	E	F
1	VCC	NC	NC	NC	VCC	GND
2	NC	VCC	NC	TDO	TDI	GND
3	INTA#	NC	NC	VCC	NC	GND
4	NC	GND	NC	NC	NC	GND
5	NC	NC	RST	GND	NC	GND
6	NC	GND	3,3V	CLK	AD[31]	GND
7	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND
8	AD[26]	GND	NC	AD[25]	AD[24]	GND
9	C/BE[3]	IDSEL	AD[23]	GND	AD[22]	GND
10	AD[21]	GND	3,3V	AD[20]	AD[19]	GND
11	AD[18]	AD[17]	AD[16]	GND	C/BE[2]	GND
12-14 Key Area						
15	3,3V	FRAME#	IRDY	GND	TRDY	GND
16	DEVSEL#	GND	NC	STOP	LOCK	GND
17	3,3V	NC	NC	GND	PERR	GND
18	SERR#	GND	3,3V	PAR	C/BE[1]	GND
19	3,3V	AD[15]	AD[14]	GND	AD[13]	GND
20	AD[12]	GND	NC	AD[11]	AD[10]	GND
21	3,3V	AD[9]	AD[8]	M66EN	C/BE[0]	GND
22	AD[7]	GND	3,3V	AD[6]	AD[5]	GND
23	3,3V	AD[4]	AD[3]	VCC	AD[2]	GND
24	AD[1]	VCC	NC	AD[0]	NC	GND
25	VCC	NC	NC	3,3V	VCC	GND

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2.3.3 Test and Program Development

2.3.3.1 JTAG/ISP Interface and Pinout

A JTAG/ISP interface is provided on the CP371 for the manufacturer's use (logic programming, JTAG test). This is a SAMTEC 10-pin, male, dual row connector (0.050" pin pitch).

Figure 2-4: JTAG Connector (CON3)

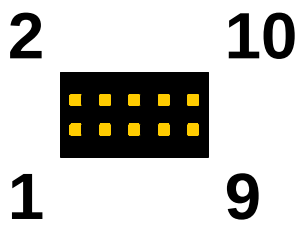


Table 2-3: JTAG Connector (CON3) Pinout

SIGNAL	PIN	PIN	SIGNAL
TCK	1	2	GND
TDO	3	4	VCC
TMS	5	6	NC
NC	7	8	N/C
TDI	9	10	GND

2.4 CapROM EEPROM

The CapROM is a 4 kBit (512 byte) EEPROM for storing gain and offset error correction data as well as providing the ability to store board control relevant information for allowing software configuration of the CP371.

2.5 Monitor and Control (M/C)

Monitor and Control functions are divided essentially into Pre-operation and Operation. Pre-operation M/C deals with board configuration and system requirements. Operation M/C covers direct operator interfaces.

2.5.1 Pre-Operation M/C

Pre-operation M/C is a direct function of the application and the system requirements. These requirements dictate the analog input configuration as well as the overall system integration. Analog input configuration is addressed in detail in chapters 4 and 5. These chapters provide detailed information concerning input signal conditioning and environmental aspects which re-

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late to the operation and performance of the CP371. Overall system integration and compliance with its requirements is beyond the scope of this manual.

2.5.2 Operation M/C

Operation M/C is a function of the CP371 driver software and the application. Direct interaction by the operator is limited to the function provided by the cluster activation LED's (0-7 for cluster A; 8-15 for cluster B). When lit, these LED's indicate that the corresponding cluster has been activated for operation.

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Chapter 3

Installation

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3. Installation

The CP371 has been designed for easy installation. However, the following standard precautions, installation procedures, and general information must be observed to ensure proper installation and to preclude damage to the board or injury to personnel.

3.1 Hardware Installation

The product described in this manual can be installed in any available 3U slot of a CompactPCI system except for the system master slot.

3.1.1 Safety Requirements

The board must be securely fastened to the chassis using the two front panel retaining screws located at the top and bottom of the board to ensure proper grounding and to avoid loosening caused by vibration or shock.

In addition the following electrical hazard precautions must be observed.



Caution, Electric Shock Hazard!

Ensure that the system main power is removed prior to installing or removing this board. Ensure that there are no other external voltages or signals being applied to this board or other boards within the system. Failure to comply with the above could endanger your life or health and may cause damage to this board or other system components including process-side signal conditioning equipment.



ESD Equipment!

This PEP board contains electrostatically sensitive devices. Please observe the following precautions to avoid damage to your board:

Discharge your clothing before touching the assembly. Tools must be discharged before use.

Do not touch any on board components, connector pins, or board conductive circuits.

If working at an anti-static workbench with professional discharging equipment, ensure compliance with its usage when handling this product.

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3.1.2 Installation Procedures

To install the board proceed as follows:

1. Ensure that the safety requirements indicated above are observed.



Warning!

Failure to comply with the instruction below may cause damage to the board or result in improper system operation. Please refer to chapters 4 and 5 for configuration information.

2. Ensure that the board is properly configured for operation before installing.



Note...

Care must be taken when applying the procedures below to ensure that when the board is inserted it is not damaged through contact with other boards in the system.

3. To install the board perform the following:
   1. Prior to installation of the board disengage the insertion/extraction handle by first unlocking the handle and pressing it down.
   2. Insert the board into an appropriate slot, and, using the insertion/extraction handle, ensure that it is properly seated in the backplane. (Front panel is flush with the rack front; the insertion/extraction handle is locked.)
4. Fasten the front panel retaining screws.



Warning!

Proper and safe operation of the CP371 Analog Input Controller depends on the correct configuration of input signals and signal conditioning. System integrators must ensure that all signals presented to the CP371 comply with the specifications set forth in this manual.

Failure to comply with the above may cause damage to the board or result in improper system operation. Please refer to chapters 4 and 5 for configuration information.

5. Connect external interfacing cables to the board as required.
6. Ensure that the interfacing cables are properly secured.

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3.1.3 Removal Procedures

To remove the board proceed as follows:

1. Ensure that the safety requirements indicated above are observed.



Warning!

Care must be taken when applying the procedures below to ensure that when the board is removed it is not damaged through contact with other boards in the system.

2. Disconnect any interfacing cables that may be connected to the board.
3. Loosen both of the front panel retaining screws.
4. To remove the board from the backplane perform the following:
    1. Unlock the insertion/extraction handle by pressing down on the grey locking mechanism in the middle of the handle. (This should be achievable with a minimum of force. If necessary lift the handle up slightly while pressing down on the grey locking mechanism.)
    2. Disengage the board from the backplane by pressing down on the insertion/extraction handle and pull the board out of the slot ensuring that the board does not make contact with adjacent boards. (If the handle does not move, it is not unlocked. Repeat the unlocking procedure above and try again. Do not use force!)

3.2 Software Installation

Installation of the CP371 driver software is a function of the application operating system. For further information refer to the appropriate software documentation.

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Chapter 4

Configuration

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4. Configuration

The following chapters provide information for configuring the CP371 board for operation.

4.1 Jumper Settings

The CP371 does not have any jumpers which require configuring.

4.2 Analog Input Signal Requirements.

In addition to the input signal types and their ranges which have been specified in chapter 1, system integrators must be aware of the need for certain types of input configuration requirements for the CP371. The following chapters describe each of the signal types with regards to their individual connection configuration requirements.

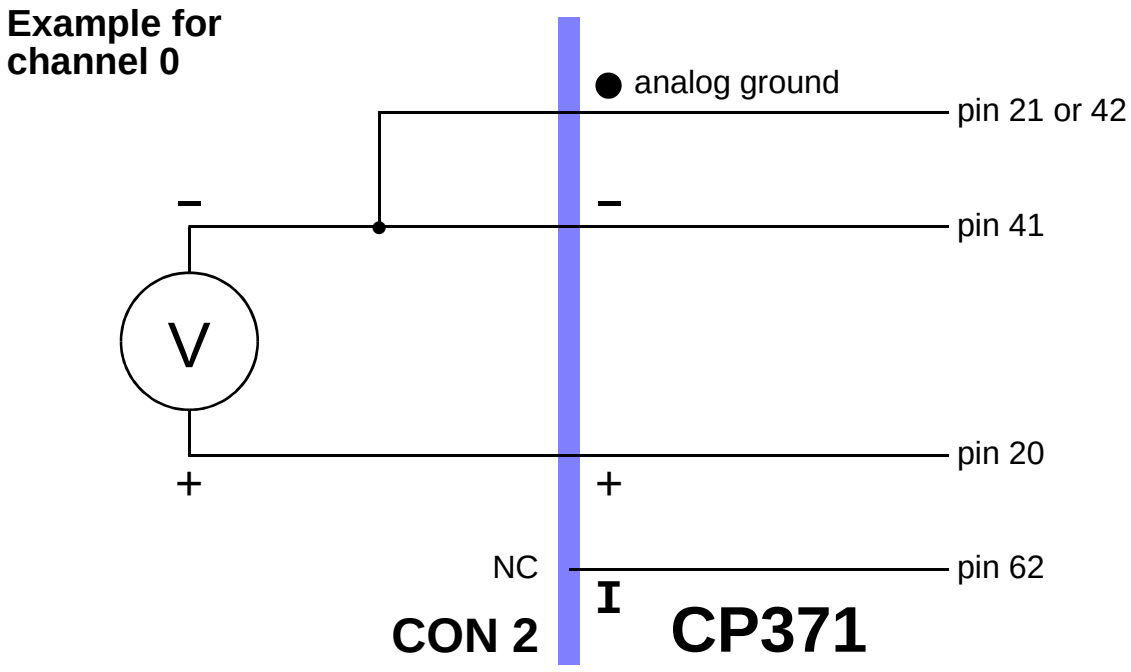
4.2.1 Channels

The CON2 connector of the CP371 is layed out so that for each input channel there are three input pins per channel available. This allows for each channel to be configured separately as required. As can be seen from Figure 2-2, each channel's respective pins are grouped together starting at the top of the connector with channel 0 (cluster A). The configuration of each channel is dependent of the type of signal being presented to the CP371. The following chapters address the basic requirements for each type of possible signal.

4.2.2 Single-ended Input Signals

Signals of this type are required to be connected: plus to plus; minus to minus. In addition the minus pole must be connected externally to the analog ground of the CON2 connector. Refer to the figure below for this type of connection.

Figure 4-1: Single-ended Input Configuration

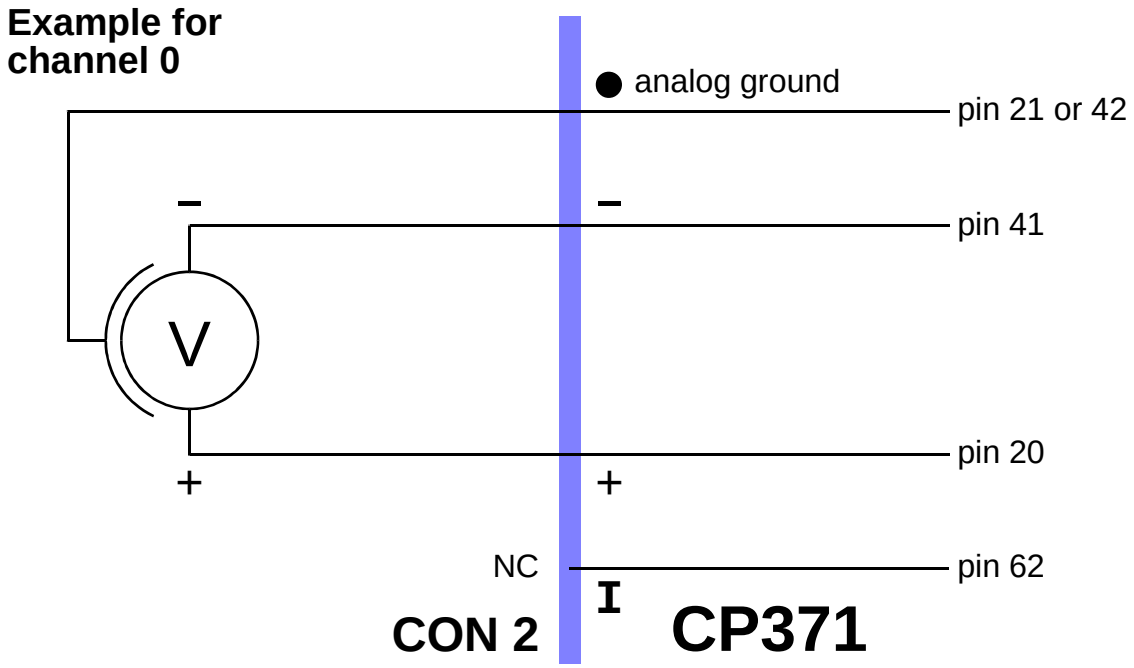


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4.2.3 Differential Input Signals

Signals of this type are required to have connections to plus and minus. Analog ground is a function of the input signal and is connected as required. Refer to the figure below for this type of connection.

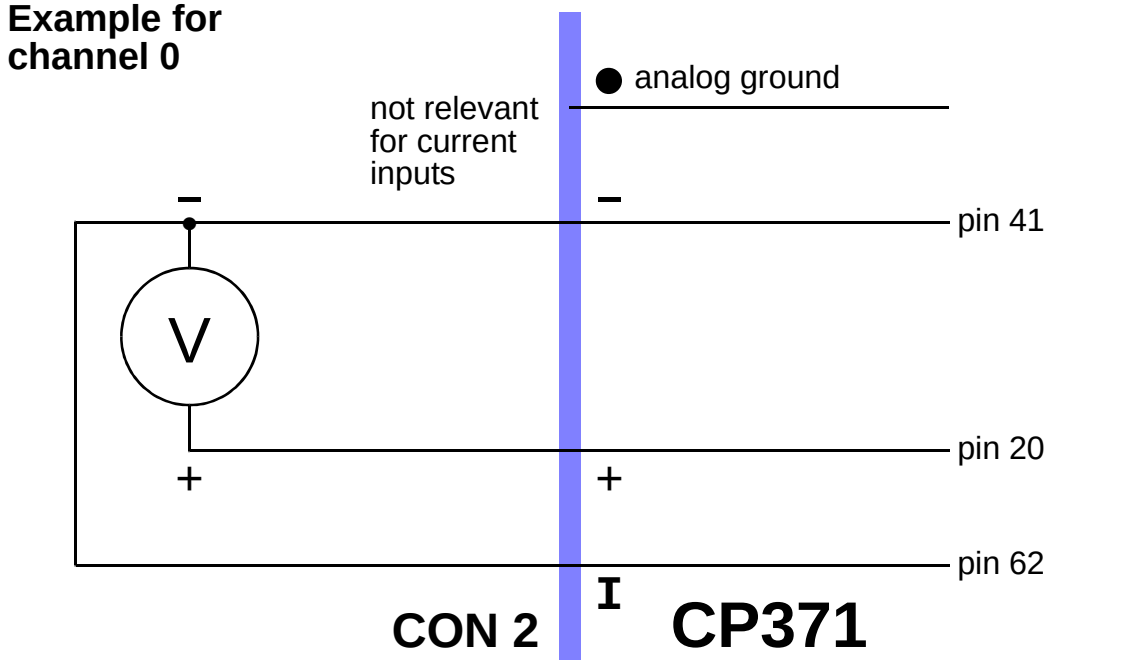
Figure 4-2: Differential Input Configuration



4.2.4 Current Input Signals

Signals of this type are required to be connected: plus to plus; minus to I. In addition the minus pole must be connected externally to minus of the CON2 connector. Refer to the figure below for this type of connection.

Figure 4-3: Current Input Configuration

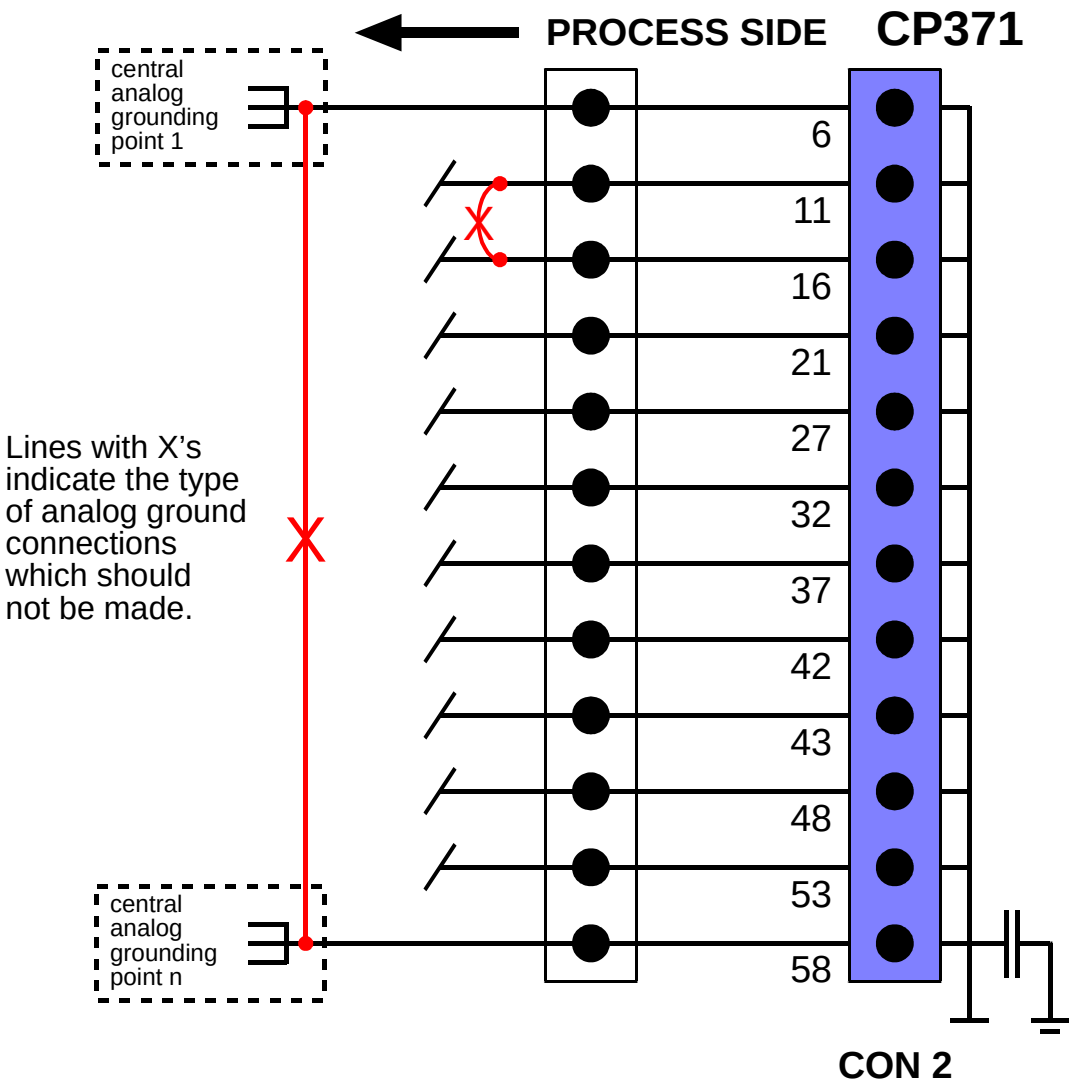


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4.2.5 Analog Ground Usage

Analog ground usage must be carefully considered in order to avoid ground loops or floating signals which can ultimately lead to the degradation of the system performance. The figure below indicates the nominal analog grounding situation, but is, of course, very much subject to the requirements of the application as a whole. What is important, however, is to ensure that ground loops do not get created in the course of the wiring up of the various system components. Additionally, it may be necessary to use heavier gauge wiring to avoid excessive loading of single wires.

Figure 4-4: Analog Grounding



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4.3 Programming Interface

4.3.1 Access Control Logic

All the resources of the CP371 are mapped within the 64KB PCI memory address space which itself is set in the PCI configuration register BAR0. The port size of all local or backend registers is 32-bit by default. The address map of the registers is as follows.

Table 4-1: Backend Register Address Map

BASE ADDRESS (BAR0)	SIZE	FUNCTION
+ 0x0000	4 kB	COMMON BOARD REGISTER
0x0800	32 bit	com_sta Hardware Status Register
0x0C00	32 bit	com_ctl Hardware Debug Register
+ 0x1000	4 kB	CAPABILITY ROM, SERIAL EEPROM
0x1000	32 bit	cmd_r Command Register
0x1400	32 bit	ctl_r Control Register
0x1800	32 bit	sta_r Status Regsiter
0x1C00	32 bit	dat_r Data Register
+ 0x2000	4 kB	ADC CLUSTER A
0x2400	32 bit	ctl_a, Cluster a Common Control Register
0x2C00	32 bit	dat_a_0 ADC Data channel # 0
0x2C04	32 bit	dat_a_1 ADC Data channel # 1
0x2C08	32 bit	dat_a_2 ADC Data channel # 2
0x2C0C	32 bit	dat_a_3 ADC Data channel # 3
0x2C10	32 bit	dat_a_4 ADC Data channel # 4
0x2C14	32 bit	dat_a_5 ADC Data channel # 5
0x2C18	32 bit	dat_a_6 ADC Data channel # 6
0x2C1C	32 bit	dat_a_7 ADC Data channel # 7

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Table 4-1: Backend Register Address Map

BASE ADDRESS (BAR0)	SIZE	FUNCTION
+ 0x3000	4 kB	ADC CLUSTER B
0x3400	32 bit	ctl_b, Cluster b Common Control Register
0x3C00	32 bit	dat_b_0 ADC Data channel # 0
0x3C04	32 bit	dat_b_1 ADC Data channel # 1
0x3C08	32 bit	dat_b_2 ADC Data channel # 2
0x3C0C	32 bit	dat_b_3 ADC Data channel # 3
0x3C10	32 bit	dat_b_4 ADC Data channel # 4
0x3C14	32 bit	dat_b_5 ADC Data channel # 5
0x3C18	32 bit	dat_b_6 ADC Data channel # 6
0x3C1C	32 bit	dat_b_7 ADC Data channel # 7
+ 0x4000	48 kB	reserved for additional clusters
0xFFFF		

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4.3.2 ADC Control Logic

This part of the IO Control Logic controls the communication with the ADC (MAX1270). The ADC integrates 8 channels per chip (2 clusters for a total of 16 channels) and has a serial bus interface operating at 2 MHz.

ADC operating mode is individually programmable for each channel, i.e. the polarity (unipolar/bipolar) and range (5/10/20V). After initialization of the corresponding ADC Control Registers an Enable Bit must be set to '1'.

The ADC Control Logic handles the cyclic setup of the necessary ADC control word including start bit, channel address, channel mode, and clock mode without any software intervention. The digitized data are automatically stored in dual-ported data registers. An arbiter avoids access conflicts between PCI access and ADC access to the same data register.

Table 4-2: ADC Common Control Register Bit Map

BITS	TYP.	DEF.	FUNCTION
31	R/W	0	Enable
30 - 16	R/W	00	reserved
15 - 14	R/W	00	RNG, BIP for ADC channel # 7
13 - 12	R/W	00	RNG, BIP for ADC channel # 6
11 - 10	R/W	00	RNG, BIP for ADC channel # 5
9 - 8	R/W	00	RNG, BIP for ADC channel # 4
7 - 6	R/W	00	RNG, BIP for ADC channel # 3
5 - 4	R/W	00	RNG, BIP for ADC channel # 2
3 - 2	R/W	00	RNG, BIP for ADC channel # 1
1 - 0	R/W	00	RNG, BIP for ADC channel # 0

Table 4-3: RNG, BIP Bits

RNG	BIP	INPUT RANGE
0	0	0 – 5 V
1	0	0 – 10 V
0	1	– 5 V
1	1	– 10 V

Table 4-4: ADC Data Registers Bit Map

BITS	TYPE	DEFAULT	FUNCTION
31 - 12	R	0	reserved
11 - 0	R	0	Data, 12 bit digit

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4.3.3 Programming the Board Capability ROM

Besides correction data for gain and offset errors other board specific capabilities can be stored in this dedicated onboard ROM. The purpose is that software will be able to configure itself, according to the hardware version (i.e. type, number of channels, insertion of components, input circuit, etc.).

The Board Capability ROM is implemented using a 4 KBit serial EEPROM of the type 93LC66 from Microchip.

The serial interface of the device has been realized in hardware resulting in a very simple register based programming interface with command, control, and data registers. All protocol and serial timing specifications are resolved by hardware.

Programming of the Board Capability ROM is undertaken as follows: The control word is written into the ROM Control Register including command opcode and internal address. Then optional data (in case of Write action) is written into the ROM Data Register. Command execution is started by setting the Startbit in the ROM Command Register. Then Ready/Busy must be polled in the ROM Status Register. After reaching Ready status, the next command can be set up and data (in case of Read action) can be fetched from the ROM Data Register.

Table 4-5: ROM Command Register Bit Map

BITS	TYPE	DEFAULT	FUNCTION
31	R/W	0	Startbit
30 - 0	R/W	00	reserved

Note: The Startbit will automatically be reset as soon as an action is completed.

Table 4-6: ROM Control Register Bit Map

BITS	TYPE	DEFAULT	FUNCTION
31 - 18	R/W	0	reserved
17 - 16	R/W	00	Opcode
15 - 9	R/W	00	reserved
8 - 0	R/W	00	internal address (A8..A0)

Note: The commands READ, EWEN (write enable) and WRITE are sufficient for all purposes.

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Table 4-7: Opcodes and Commands

OPCODE	A8 ... A0	COMMAND
00	11xxxxxxx	EWEN
10	xxxxxxxxx	READ
01	xxxxxxxxx	WRITE

Note: The EWEN (Erase and Write enable) command must be executed once before the first write.

Table 4-8: ROM Status Register Bit Map

BITS	TYPE	DEFAULT	FUNCTION
31	R/W	0	Busy
30 - 0	R/W	00	reserved

Note: As soon as the Startbit is set the Busy/Ready bit becomes active (Busy=1). It remains set as long as the command is executed and is reset when command execution is complete.

Table 4-9: ROM Data Register Bit Map

BITS	TYPE	DEFAULT	FUNCTION
31-8	R/W	0	reserved
7-0	R/W	0	Data (for data read and write commands)

4.3.4 Common Board Registers

These registers are for internal test and debug only. The Common Status Register contains Logic- Version and PCB- Version. The Common Control Register is a read/write register without any further functionality. Neither of these should be used by standard software.

Table 4-10: Hardware Debug Register Bit Map

BITS	TYPE	DEFAULT	FUNCTION
31-0	R/W	0	reserved

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Table 4-11: Hardware Status Register Bit Map

BITS	TYPE	DEFAULT	FUNCTION
31 - 16	R	0	reserved
15 - 8	R	00	HW Version (PCB Index)
7 - 0	R	01	Logic Version

Note: The HW version starts with 0, Logic Version with 1. It will be incremented for each released version.

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Chapter 5

System Considerations

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5. System Considerations

5.1 Introduction

In addition to the basic specification requirements for signals being presented to the CP371 which have been addressed in chapter 4, system integrators need to be aware of the overall system environment and the application needs when designing the interfacing to the CP371. There are certain basic considerations which require explicit resolution as well as others which are of a more subtle nature that may under circumstances impact the performance or validity of the analog to digital conversion process. The following chapters address a number of more apparent considerations which should be addressed but certainly not all of the possible situations which may be encountered. Many of the considerations presented here are recommendations, but some are definite requirements if the CP371 is to successfully achieve its purpose.

5.2 General

Considerations:

1. All **unused input channels** must have their pins tied to analog ground.
2. For input channels in use, the `I` pin is not connected except when required.
3. Distribute analog ground connections over all the available CON2 analog ground pins. Don't just use one or two pins.
4. It is recommended to use twisted pair wiring for input signals.
5. Mixing of input signal types (single-ended, differential, and current) presented to the CP371 is permitted.
6. The type of signal presented to each input channel the CP371 must correspond to the driver software configuration for that channel. If not the result will be erroneous and the CP371 may be damaged.
7. Care must be taken to ensure that proper grounding concepts are followed, and that the integrity of the grounding system within the application be maintained.
8. Input wire routing should avoid proximity to high voltage or current sources.
9. Where possible input wiring length should be kept as short as possible.

5.3 Shielding

Considerations:

1. Input cable shielding in general is recommended.
2. The requirements for shielding can be seen primarily as a function of the system design and environment, but empirical results must also be considered.
3. The CON2 connector has a metal housing which is connected to the CP371 shield and is isolated from the analog ground.
4. Ensure that if shielding is used that it is not in anyway connected to the analog ground.

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5.4 Process-side Signal Conditioning

Considerations:

1. Input signals presented to the CP371 must be within the ranges specified for the signal type or erroneous results will occur as well as possible damage to the CP371.
2. Ensure that when analog ground pins on CON2 are used that on the process side no grounding loops are created. Refer to chapter 4 for further information.

5.5 Cable Interfacing

Considerations:

1. No modification to the CP371 itself is permitted (i.e. connector pin shorting).
2. If necessary, cabling to the CP371 CON2 connector should physically fixed to prevent strain on the CON2 connector.

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