CP372

8 Channel CompactPCI
Analog Output Controller

Manual ID: 25780, Rev. Index 01
21 November, 2002

The product described in this manual is in compliance with all applied CE standards.

25780.01.VC.021121/111235

Revision History

Publication Title:	CP372	
ID Number:	25780	
Rev. Index	Brief Description of Changes	Date of Issue
01	Initial Issue	21 Nov, 2002

Imprint

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Caution, Electric Shock!

This symbol and title warn of hazards due to electrical shocks (> 60V) when touching products or parts of them. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your material.

Please refer also to the section “High Voltage Safety Instructions” on the following page.



Warning, ESD Sensitive Device!

This symbol and title inform that electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Please read also the section “Special Handling and Unpacking Instructions” on the following page.



Warning!

This symbol and title emphasize points which, if not fully understood and taken into consideration by the reader, may endanger your health and/or result in damage to your material.



Note...

This symbol and title emphasize aspects the reader should read through carefully for his or her own advantage.

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High Voltage Safety Instructions



Warning!

All operations on this device must be carried out by sufficiently skilled personnel only.



Caution, Electric Shock!

Before installing your new Kontron product into a system always ensure that yo ur mains power is switched off. This applies also to the installation of piggybacks.

Serious electrical shock hazards can exist during all installation, repair and maintenance operations with this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing work.

Special Handling and Unpacking Instructions



ESD Sensitive Device!

Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory back-up, ensure that the board is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the board.

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This device should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This applies also to the operational temperature range of the specific board version, which must not be exceeded. If batteries are present their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, please follow only the instructions supplied by the present manual.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the board please re-pack it as nearly as possible in the manner in which it was delivered.

Special care is necessary when handling or unpacking the product. Please, consult the special handling and unpacking instruction on the previous page of this manual.

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Chapter 1

Introduction

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1. Introduction

1.1 System Overview

The CompactPCI board described in this manual operates with the PCI bus architecture to support additional I/O and memory-mapped devices as required by various industrial applications. For detailed information concerning the CompactPCI standard, please consult the complete Peripheral Component Interconnect (PCI) and CompactPCI Specifications. For further information regarding these standards and their use, visit the homepage of the *PCI Industrial Computer Manufacturers Group (PICMG)*.

Many system relevant CompactPCI features that are specific to Kontron Modular Computers CompactPCI systems may be found described in the Kontron CompactPCI System Manual. Please refer to the section “Related Publications” at the end of this chapter for the relevant ordering information.

The CompactPCI System Manual includes the following information:

- Common information that is applicable to all system components, such as safety information, warranty conditions, standard connector pinouts etc.
- All the information necessary to combine PEP racks, boards, backplanes, power supply units and peripheral devices in a customized CompactPCI system, as well as configuration examples.
- Data on rack dimensions and configurations as well as information on mechanical and electrical rack characteristics.
- Information on the distinctive features of PEP CompactPCI boards, such as functionality, hot swap capability. In addition, an overview is given for all existing PEP CompactPCI boards.
- Generic information on the PEP CompactPCI backplanes, such as the slot assignment, PCB form factor, distinctive features, clocks, power supply connectors and signalling environment, as well as an overview of the PEP CompactPCI standard backplane family.
- Generic information on the PEP CompactPCI power supply units, such as the input/output characteristics, redundant operation and distinctive features, as well as an overview of the PEP CompactPCI standard power supply unit family.

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1.2 Product Overview

The CP372 Analog Output Controller is a part of a comprehensive concept to provide CompactPCI system integrators with a complete range of CompactPCI I/O products which include the functions of analog input, analog output, digital input, and digital output implemented as separate individual boards. This concept ensures a maximum degree of system design flexibility thus allowing efficient and effective usage of available resources.

The basic functions of this board are to provide interfacing to the application software, perform digital to analog signal conversion, and to make the analog output signal available to the application process. The major components involved in these processes are: the Digital to Analog Conversion Process and Communications (DAC ProComm) controller which is realized in a field-programmable gate array (FPGA), digital to analog converters (DACs), and the front end (process side) signal conditioning. The DAC ProComm Controller is designed to provide effective and efficient control of the digital to analog conversion process as well as interfacing to the CPCI System Controller.

The following table provides a quick overview of the CP372 board.

Table 1-1: CP372 Product Overview

CP372 FEATURES	DESCRIPTION
Product Type	CompactPCI Analog Output Controller: • Form factor: 3U, 4HP • 33 MHz system clock • 32-bit address and data bus • Designed for Plug and Play • Complies with the CPCI specification
Outputs	Primary: Up to eight channels (divided into two clusters) of the following analog signal types: • Voltages: 0 to 5 V, 0 to 10 V, ± 5 V, and ± 10 V • Current: 0 to 20 mA Secondary: N/A
Inputs	Primary: Up to eight logical channels of digital data (12-bit channel resolution) which are provided by the application software Secondary: External power supply source voltage(s) – V_{ext} – for use in the generation of analog current outputs
Monitor and Control	M/C functionality includes: • External cluster enable/disable control • Cluster active LEDs • DAC ProComm controller • System Master driver software

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1.3 Board Overview

1.3.1 Board Introduction

The CP372 is an eight channel, dual cluster (four channels each), analog output board. Application software can provide up to eight logical channels of digital data per board for processing to analog signal outputs. Output data is presented to the CP372 via the CompactPCI interface for conversion to either an output voltage or output current and makes it available for application process use.

Output signal generation begins with the presentation of digital data to the DAC ProComm Controller which is responsible for controlling the digital to analog data conversion process as well as the interface to the CompactPCI bus. The DAC ProComm controller then in turn provides data to the two DACs accordingly. The analog outputs of the DACs are then processed through appropriate signal conditioning prior to being made available to the application process at the board's front panel interface.

Output signal types and ranges are as follows:

- Voltages:
  - Unipolar:
    - 0 to 5 V
    - 0 to 10 V
  - Bipolar:
    - ± 5 V
    - ± 10 V
- Current:
  - 0 to 20 mA

    (requires external power supply source voltage for analog current output)

Input data are:

- Up to eight logical channels of digital data for conversion to analog output signals

  (supplied by the application software)

1.3.2 Board Specific Information

Specific board components involved in the digital to analog conversion and data handling process are:

- One front panel connector (62-pin, female, D-Sub type)
- Eight channels of output signal conditioning
- Two, 12-bit DACs (one for each cluster of 4 channels each)
- Ten optocouplers (four dual high speed and six general purpose (four quad, and two singles)
- One FPGA (the DAC ProComm controller)
- One CompactPCI bus connector (J1, board to backplane, 132-pin, female, six row)
- One JTAG/ISP on board programming connector (10-pin, male, dual row)
- Two DC/DC converters (one +5 V and one ± 15 V, both with 3 kV isolation)
- One EEPROM (Capability ROM)

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1.4 System Relevant Information

The following system relevant information is general in nature but should still be considered when developing applications using the CP372.

Table 1-2: System Relevant Information

SUBJECT	INFORMATION
System Configuration	The CP372 operates with a system clock frequency of 33 MHz. The number of CP372's which can be installed in any one system depends solely on the number of CPCI slots available.
Master/Slave Functionality	The CP372 functions only as a slave. As such it requires a system master for servicing.
System Controller	The CP372 cannot function as a system controller.
Analog Outputs	The process interfacing to the CP372 must comply with the output specifications set forth in this manual. In particular, for analog current outputs, an external power source is required to supply an input voltage for generation of the analog output current. Because this type of output is a direct function of the application, this input voltage can only be provided by the application.

1.4.1 System Configuration

When implementing applications, precautions must be taken to ensure that the output signals of the CP372 are properly terminated in accordance with the specifications set forth in this manual. For this reason it will be necessary system integrators to ensure proper signal conditioning for their applications before accepting analog outputs from the CP372. In addition, it is imperative that signal interference be kept to a minimum. Refer to chapters 4 and 5 for further information.

1.4.2 Driver Software

The CP372 is supplied with appropriate driver software which provides software interfacing to the system master.

1.5 Board Diagrams

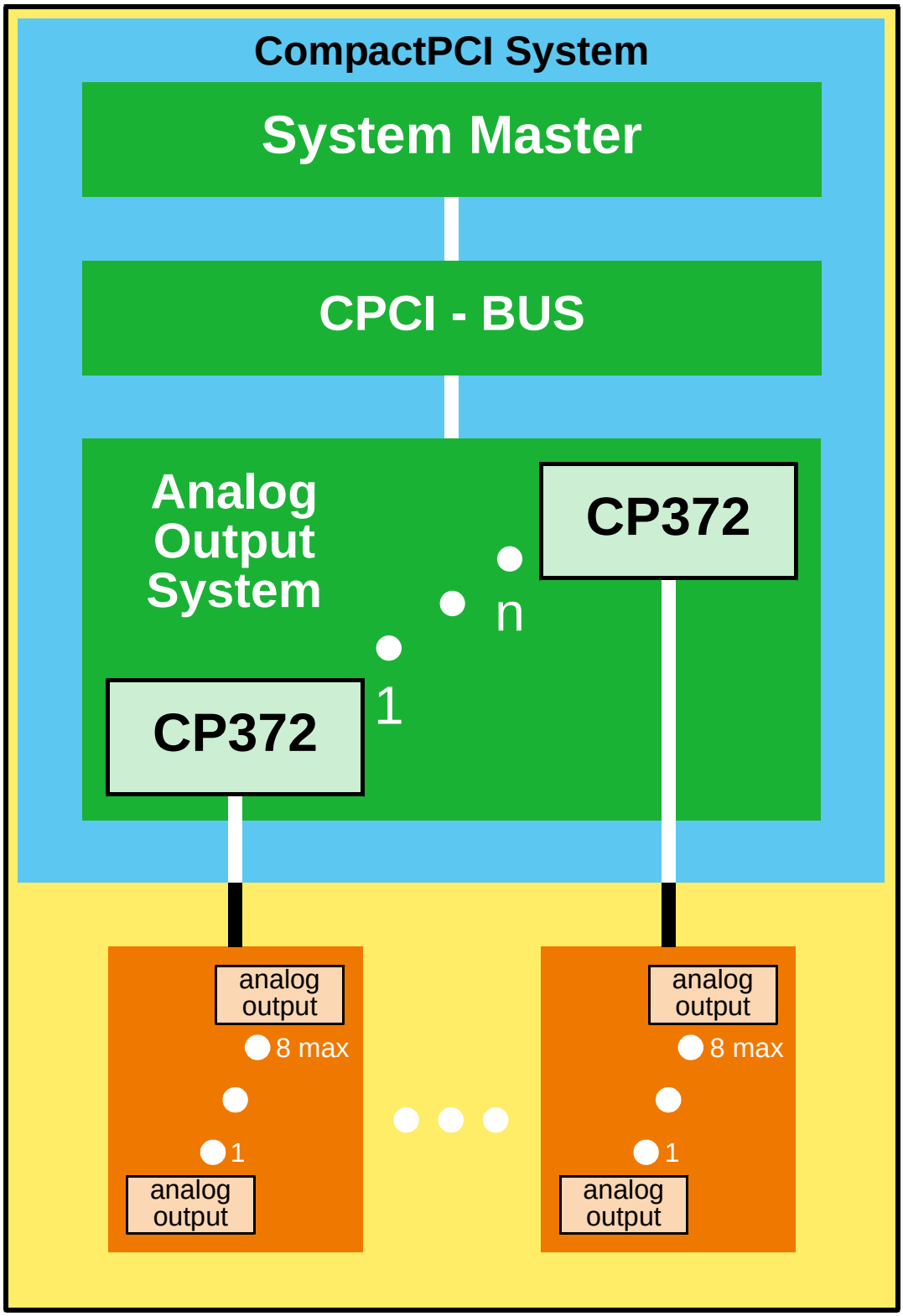
The following diagrams provide additional information concerning board functionality and component layout.

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1.5.1 System Level Interfacing

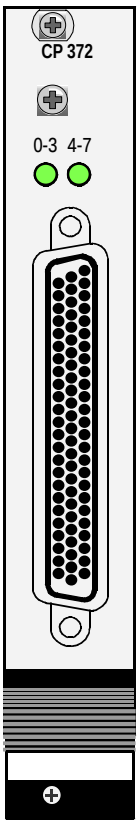
Figure 1-1: CP372 System Level Interfacing Diagram



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1.5.2 Front Panel

Figure 1-2: CP372 Front Panel



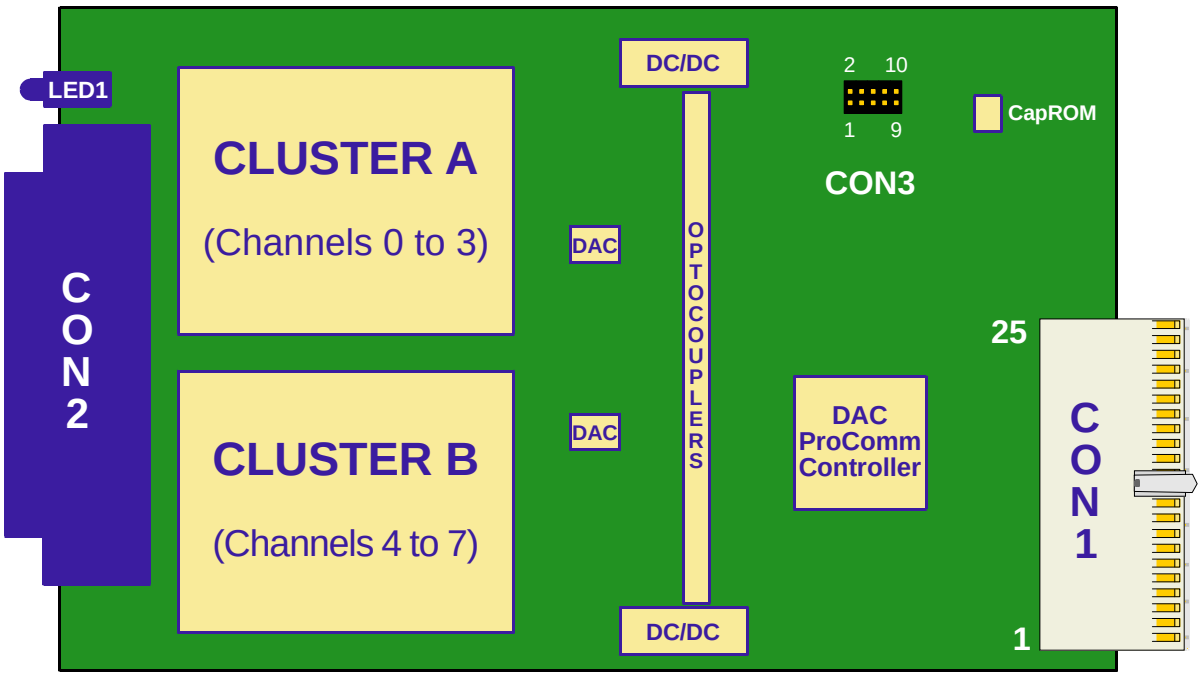
LEGEND:

0-3 when LED is active: cluster A is activated

4-7 when LED is active: cluster B is activated

1.5.3 Board Layout

Figure 1-3: CP372 Board (Front View)



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1.6 Technical Specifications

Table 1-3: CP372 Main Specifications

GROUP	TYPE	DESCRIPTION
DAC ProComm Controller and Related	FPGA Logic Device	Provides PCI interfacing and IO control logic
Peripheral Memory	CapROM	4 kBit (512 byte) EEPROM
External Interfaces	Analog Output	One, 62-pin, female, three row, D-sub connector Supports up to eight analog output channels
	CPCI Bus	One, 132-pin, female, six row connector (standard CPCI type connector for J1)
Internal Interfaces	JTAG/ISP	JTAG/ISP 10-pin SMD connector for programming and testing purposes
Indicators	Front Panel LED	Two, green LED's for indicating cluster operation status (enabled or disabled)
General	Mechanical	Conforms with IEEE 1101.1
	Power Requirements	Voltages: 3.3 V 5 V VCC
	Power Consumption	Watts: 0.5 W for the 3.3 V power source 2.9 W for the 5 V power source
	Temperature Range	Operational: 0ºC to +70ºC Standard -40ºC to +85ºC E2 Storage: -55ºC to +125ºC
	Humidity	0% to 95% non-condensing
	Dimensions	100 mm x 160 mm single height Eurocard
	Board Weight	155 g (2 cluster configuration)
Software Driver Information	PCI Header	Device ID: 0x5555 Vendor ID: 0x1556 Class Code: 0x118000 Subsystem Device ID: 0x0100 Subsystem Vendor ID: 0x1518 Note: The Device ID and Vendor ID refer to the chip manufacturer. In the Class Code value given, "11" relates to the data acquisition and signal processing controllers and "8000" relates to the Analog IO modules. Subsystem Device ID and Subsystem Vendor ID are defined by PEP. In addition, the CP372 uses 64kB in PCI memory space, BAR0, is not pre-affectable, and no interrupts are used.

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Table 1-4: CP372 Analog Output Specifications

TYPE	DESCRIPTION
Output Types / Ranges	VOLTAGES: Unipolar: 0 to 5 V 0 to 10 V Bipolar: ± 5 V ± 10 V (Note: Maximum output current for analog voltages is 5 mA per channel.) CURRENT: 0 to 20 mA (Note: Requires V_{ext} for generation.)
V_{ext}	This external source voltage is required for the generation of analog current outputs. The V_{ext} requirement for each output channel is a function of the application and is dependent upon the channel source resistance (R_s). As such it is possible for each channel of analog current output to have a different V_{ext} requirement. The absolute specification for a given V_{ext} is: 28.0 VDC maximum 6.0 VDC minimum whereby the actual minimum source voltage required must be determined based on the actual source resistance. The minimum source voltage indicated above is required to ensure full scale, 0 to 20 mA, operation. It is imperative that the application complies with the above specification, otherwise, the CP372 may be damaged or fail to function properly. For more information refer to chapters 2 and 4.
Channels	Standard: 8 channels total (two clusters of 4 channels each) Optional: 4 channels total (one cluster of 4 channels)
Channel Connections	8 dedicated connector pins for voltage outputs; 8 dedicated connector pins for current outputs; 8 analog ground pins distributed over the connector; 4 dedicated pins for common tie points for external source voltages (V_{ext}) for current outputs; and 2 pins for external cluster enable/disable control.
Conversion	Continuous serial sampling of the digital 16-bit output words (2 bits address and 12 bits data) per cluster from the DAC ProComm Controller available for the DAC (digital serial interface). The digital to analog converter generates four voltage outputs and updates the outputs simultaneously. The initial analog signal value of each output channel after power on is 0V.
Throughput Rate	31.25 kHz per channel
Resolution	12-bit
Accuracy	See table 1-5
Output Protection	8 kV ESD; short circuit; and EMI filtering
Isolation	2 kV process to system

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Table 1-5: CP372 Accuracy

	OUTPUT SIGNAL - TYPE and RANGE	SIGNAL ACCURACY at 23°C ± % of FULL SCALE	ACCUMULATING DEVIATION % per K (S and E1 BOARDS)	ACCUMULATING DEVIATION % per K (E2 BOARDS)
BEST CASE ACCURACY	0 V – 5 V	0.05	0.001	0.001
	0 V – 10 V	0.05	0.001	0.001
	- 5 V – + 5 V	0.05	0.001	0.001
	- 10 V – + 10 V	0.05	0.001	0.001
	0 mA – 20 mA	0.1	0.002	0.002
ACCURACY	0 V – 5 V	0.05	0.001	0.001
	0 V – 10 V	0.075	0.001	0.001
	- 5 V – + 5 V	0.075	0.001	0.001
	- 10 V – + 10 V	0.1	0.001	0.001
	0 mA – 20 mA	0.1	0.002	0.002

Note:

BEST CASE ACCURACY: best case calibration (not supported by Kontron)

ACCURACY: calibration by Kontron (at delivery)

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1.7 Applied Standards

The *PEP Modular Computers'* CompactPCI systems comply with the requirements of the following standards:

Table 1-6: Applied Standards

	TYPE	STANDARD
CE	Emission	EN50081-1
	Immunity, Industrial Environment	EN61000-6-2
	Immunity, IT Equipment	EN55024
	Electrical Safety	EN60950 Note: The CP372 is specified I/O only for: SELV and EVL. It is NOT SPECIFIED for "Hazardous"
MECHANICAL	Mechanical Dimensions	IEEE 1101.1
ENVIRONMENTAL TESTS	Vibration, Sinusoidal	IEC 60068-2-6
	Random Vibration, Broadband	IEC 60068-2-64
	Bump	IEC 60068-2-29
	Single Shock	IEC 60068-2-27
	Temperature Tests A: Cold	IEC 60068-2-1
	Temperature Tests B: Dry Heat	IEC 60068-2-2

1.8 Related Publications

Table 1-7: Related Publications

	ISSUED BY	DOCUMENT
CompactPCI Systems	PICMG	CompactPCI Specification, V. 2.0, Rev. 3.0
	PEP Modular Computers	CompactPCI Systems Manual (ID 19953)

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Chapter 2

Functional Description

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2. Functional Description

The following chapters present more detailed, board level information about the CP372 analog output controller whereby the board components and their basic functionality are discussed in general.

2.1 General Information

The CP372 is comprised basically of the following:

- Signal conditioning
- Digital to analog converter
- Optocouplers
- DAC ProComm controller
  - Realized in an FPGA device
  - Controls analog signal generation and provides interfacing to the CPCI bus
- System interfaces for:
  - Analog outputs
    - Two, four channel clusters: Cluster A, Cluster B
    - One, 62-pin, female, 3-pin row, D-sub connector (CON2)
  - CompactPCI bus
    - 132-pin, female, 6-pin row connector (CON1)
    - CompactPCI specification
  - Testing and program development (JTAG/ISP) connector (CON3)
- On board memory: Capability EEPROM (CapROM)
- Monitor and Control
  - Two each, green status LED's for cluster activation (channels 0-3 and 4-7)
  - Cluster enable/disable control
- Software

2.1.1 Signal Conditioning

Analog output signal conditioning is comprised of two clusters (A and B) each of the following:

- Overvoltage Protection
- EMI Suppression Filters (each signal line)
- Gain and unipolar/bipolar conversion
- Generation of analog voltage output as required
- Generation of analog current output as required (external source voltage (V_{ext}) required)
- Analog switches for range selection

2.1.2 Digital to Analog Converter

For each cluster there is one, four channel, 12-bit digital to analog converter (DAC) available. After power on, the DAC ProComm controller automatically begins supplying each cluster DAC with channel control signals and a serial data stream with digital output values for each cluster channel. The actual channel digital input values are set to 0V initially and remain so until the application software supplies new values. The DAC itself converts the digital inputs to analog

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output signals and then presents these to the signal conditioning functions for appropriate processing before being made available to the front panel interface.

2.1.3 Optocouplers

The CP372 provides full galvanic isolation between the process and application control system. This is accomplished by the use of optocouplers for all data and control signal lines between the DAC ProComm controller and the DACs and signal conditioning functions.

Signals directly supplied to the DACs are isolated using special high speed dual optocouplers. Signals supplied to the signal conditioning functions are isolated using standard quad or single optocouplers as required.

2.1.4 DAC ProComm Controller

Within the CP372, the DAC ProComm controller is responsible for supervising and controlling the analog signal generation process and providing communications with the CompactPCI system master. Applications address the CP372 through its software driver interface within the system master whereby the controller accepts requests and digital output data from the driver, processes both of them accordingly, and supervises the digital to analog conversion process and the signal conditioning functions.

2.1.5 System Interfaces

The CP372 provides interfacing capability for the following system elements:

- Analog output
- CompactPCI bus
- Test and program development: JTAG/ISP

Analog output interfacing is achieved via the CON2 connector. Interfacing to the CompactPCI bus is accomplished via the CON1 connector. Test and program development is supported by the CON3 connector.

2.1.6 Monitor and Control

Various monitor and control functions are available for the operation of the CP372. Two cluster operational status LED's and an external cluster enable/disable function are available for operator interaction. In addition, applications have access via the System Master driver software to board specific registers.

2.1.7 Software

Driver software is available for the System Master application software.

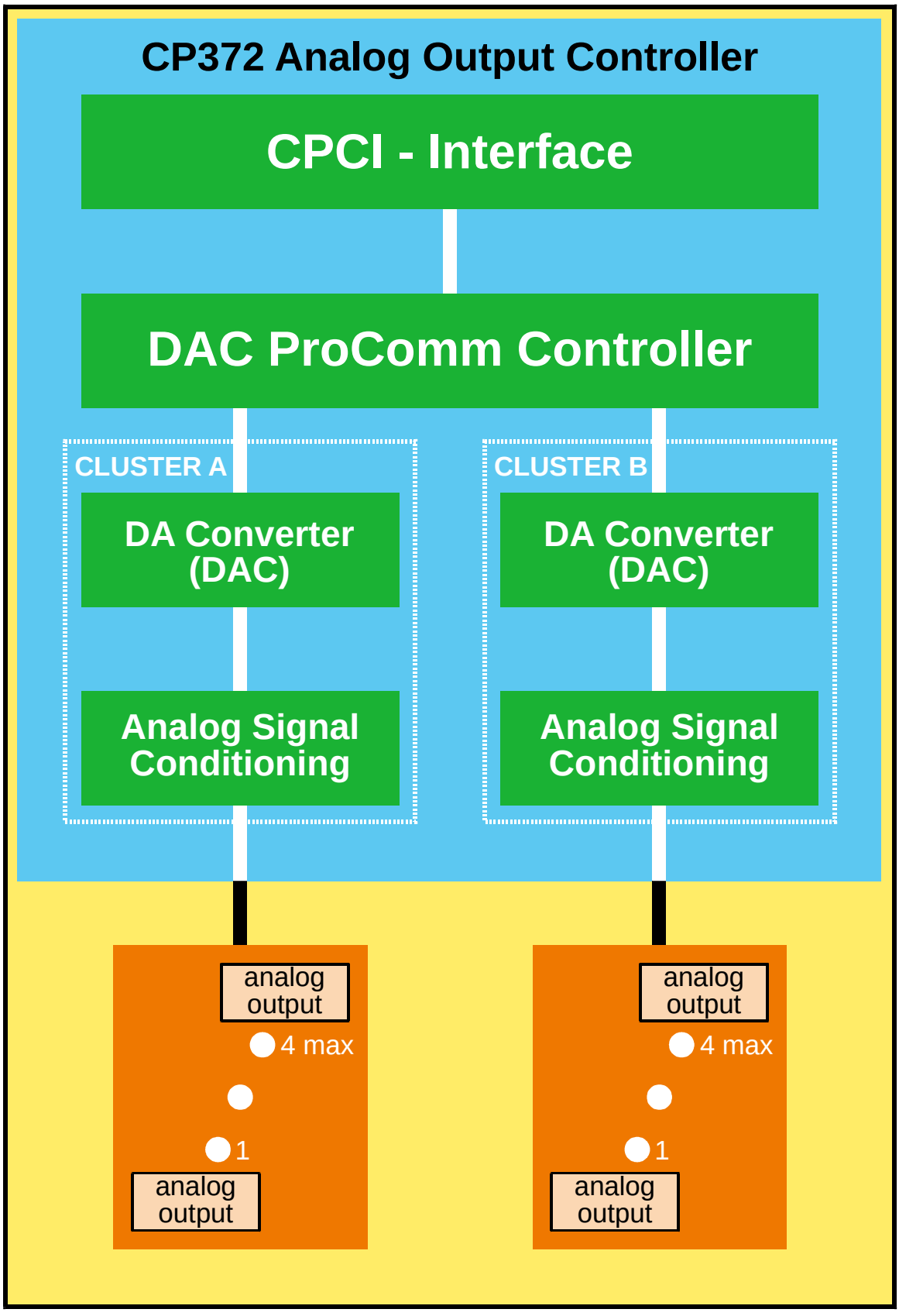
2.2 Board-Level Interfacing Diagram

The following figure demonstrates the interfacing structure between the internal processing modules of the CP372 and other major CP372 system components. Where CP372 system elements have common interfacing they are grouped into a block. Interfacing common to only one element of a block is indicated with a direct connecting line. The interfacing lines are shown in white where they are on board and in black for board external interfacing.

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Figure 2-1: CP372 Board Level Interfacing



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2.3 System Interfaces

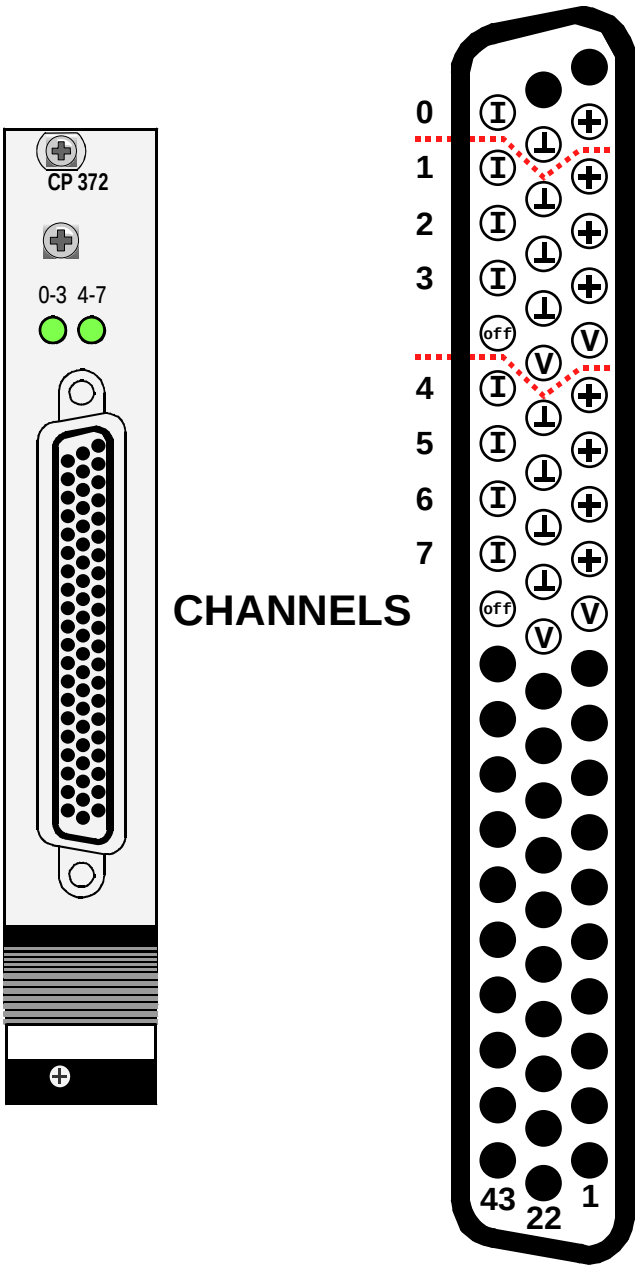
2.3.1 Analog Output Interface

The analog output interface is accomplished through the CON2 connector. This connector provides connections for analog outputs as well as the supplying of V_{ext} which is required for the generation of current outputs

2.3.1.1 Pin Layout and Signal Assignment of CON2

The following figure and table indicate the pin layout and signal pinout of connector CON2.

Figure 2-2: Pin Layout of the Analog Output Interface Connector CON2



Pin Naming Convention:

- ● not connected
- + Analog voltage output
- ⊥ Analog ground
- I Analog current output
- V V_{ext} common tie point
- off Cluster enable/disable

LED's

0-3 Cluster A activated (Channels 0 to 3)

4-7 Cluster B activated (Channels 4 to 7)

Note:

Each cluster has its own enable / disable and V_{ext} common tie point pins.

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Table 2-1: Pinout of the Analog Output Interface Connector CON2

	CHANNEL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
				42	NC	21	NC
CLUSTER A	0	62	IOUT0	41	AGND	20	VOUT0
	1	61	IOUT1	40	AGND	19	VOUT1
	2	60	IOUT2	39	AGND	18	VOUT2
	3	59	IOUT3	38	AGND	17	VOUT3
		58	EXT_EN_A	37	SUPPLY_A	16	SUPPLY_A
CLUSTER B	4	57	IOUT4	36	AGND	15	VOUT4
	5	56	IOUT5	35	AGND	14	VOUT5
	6	55	IOUT6	34	AGND	13	VOUT6
	7	54	IOUT7	33	AGND	12	VOUT7
		53	EXT_EN_B	32	SUPPLY_B	11	SUPPLY_B
		52	NC	31	NC	10	NC
		51	NC	30	NC	9	NC
		50	NC	29	NC	8	NC
		49	NC	28	NC	7	NC
		48	NC	27	NC	6	NC
		47	NC	26	NC	5	NC
		46	NC	25	NC	4	NC
		45	NC	24	NC	3	NC
		44	NC	23	NC	2	NC
		43	NC	22	NC	1	NC



WARNING !!!

Pins 16 and 37 (SUPPLY_A) are tied together and pins 11 and 32 (SUPPLY_B) are tied together on the board side of the connector. These pins can be used to provide a common tie point for an external source voltage (V_{ext}) if required.

However, in the event that different V_{ext} voltages are required, it is IMPERATIVE to ensure that their use does not create a hazard for the operation of the CP372, external equipment, or to operating personnel. Their misuse can result in electrical short circuiting, fire, or injury to operating personnel.

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2.3.1.2 V_{ext} Functionality by Analog Current Outputs

In order to generate analog current output signals, the CP372 requires that the application provide an appropriate external source voltage (V_{ext}) for each individual analog current output channel.

The source voltage to be provided is by definition a function of the total output channel source resistance and the maximum required output current. To take advantage of full scale, 0 to 20 mA, output, each channel must be supplied with a corresponding given minimum source voltage which in many cases will vary from channel to channel due to varying channel source resistance.

As the CP372 allows for any combination of signal outputs: voltage or current, and current with different source resistances, care must be taken to ensure that V_{ext} requirements are met as well as proper connection of output signals to their respective channels.

Where current outputs share a common V_{ext}, so called common tie point pins are available at CON2 for application usage. For each cluster there are two pins available, and the two pins of each cluster are permanently tied together on the CP372 side of the CON2 connector. For this reason only one common tie point is available for each cluster.

Refer to chapter 1 for the specification of V_{ext} and chapters 4 and 5 for further information concerning the configuration of analog outputs and system considerations for the integration of the CP372 in applications.

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2.3.2 CompactPCI Interface and Pinout

The CompactPCI interface is based on the specification PICMG 2.0 R 3.0, 10/1/99. The following figure and table indicate the pin layout and pinout of the CPCI connector, CON1 (J1).

Figure 2-3: CPCI Connector CON1 (J1)

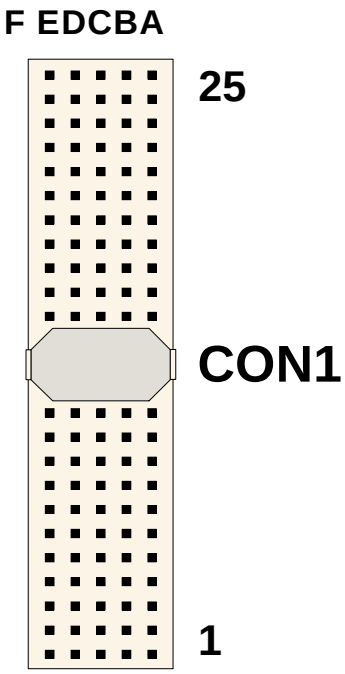


Table 2-2: CPCI Connector CON1 (J1)

PIN	PIN ROW					
	A	B	C	D	E	F
1	VCC	NC	NC	NC	VCC	GND
2	NC	VCC	NC	TDO	TDI	GND
3	NC	NC	NC	VCC	NC	GND
4	NC	GND	NC	NC	NC	GND
5	NC	NC	RST	GND	NC	GND
6	NC	GND	3,3V	CLK	AD[31]	GND
7	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND
8	AD[26]	GND	NC	AD[25]	AD[24]	GND
9	C/BE[3]	IDSEL	AD[23]	GND	AD[22]	GND
10	AD[21]	GND	3,3V	AD[20]	AD[19]	GND
11	AD[18]	AD[17]	AD[16]	GND	C/BE[2]	GND
12-14 Key Area						
15	3,3V	FRAME#	IRDY	GND	TRDY	GND
16	DEVSEL#	GND	NC	STOP	LOCK	GND
17	3,3V	NC	NC	GND	PERR	GND
18	SERR#	GND	3,3V	PAR	C/BE[1]	GND
19	3,3V	AD[15]	AD[14]	GND	AD[13]	GND
20	AD[12]	GND	NC	AD[11]	AD[10]	GND
21	3,3V	AD[9]	AD[8]	M66EN	C/BE[0]	GND
22	AD[7]	GND	3,3V	AD[6]	AD[5]	GND
23	3,3V	AD[4]	AD[3]	VCC	AD[2]	GND
24	AD[1]	VCC	NC	AD[0]	NC	GND
25	VCC	NC	NC	3,3V	VCC	GND

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2.3.3 Test and Program Development

2.3.3.1 JTAG/ISP Interface and Pinout

A JTAG/ISP interface is provided on the CP372 for the manufacturer's use (logic programming, JTAG test). This is a SAMTEC 10-pin, male, dual row connector (0.050" pin pitch).

Figure 2-4: JTAG Connector (CON3)

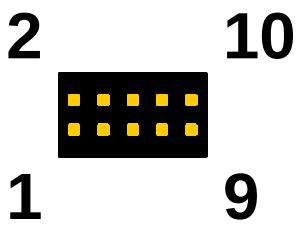


Table 2-3: JTAG Connector (CON3) Pinout

SIGNAL	PIN	PIN	SIGNAL
TCK	1	2	GND
TDO	3	4	VCC
TMS	5	6	NC
NC	7	8	N/C
TDI	9	10	GND

2.4 CapROM EEPROM

The CapROM is a 4 kBit (512 byte) EEPROM for storing gain and offset error correction data as well as providing the ability to store board control relevant information for allowing software configuration of the CP372.

2.5 Monitor and Control (M/C)

Monitor and Control functions are divided essentially into Pre-operation and Operation. Pre-operation M/C deals with board configuration and system requirements. Operation M/C covers direct operator interfaces.

2.5.1 Pre-Operation M/C

Pre-operation M/C is a direct function of the application and the system requirements. These requirements dictate the analog output configuration as well as the overall system integration. Analog output configuration is addressed in detail in chapters 4 and 5. These chapters provide detailed information concerning output signal conditioning and environmental aspects which re-

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late to the operation and performance of the CP372. Overall system integration and compliance with its requirements is beyond the scope of this manual.

2.5.2 Operation M/C

Operation M/C is primarily a function of the CP372 driver software and the application. However, when the CP372 is in operation, there are cluster operational status LEDs available as well as an external cluster enable/disable function.

The cluster activation LEDs (0-3 for cluster A; 4-7 for cluster B) indicate when lit that the corresponding cluster has been activated for operation.

Use of the external cluster enable/disable function requires the process side of the application to provide switching functionality in order to disable all of the outputs of each single cluster at one time. This function permits the separate physical disabling of all of each cluster's outputs independent of the application software. This functionality may either be controlled by an operator or automatically by an independent process function. For further information concerning this function refer to chapters 4 and 5.

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Chapter 3

Installation

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3. Installation

The CP372 has been designed for easy installation. However, the following standard precautions, installation procedures, and general information must be observed to ensure proper installation and to preclude damage to the board or injury to personnel.

3.1 Hardware Installation

The product described in this manual can be installed in any available 3U slot of a CompactPCI system except for the system master slot.

3.1.1 Safety Requirements

The board must be securely fastened to the chassis using the two front panel retaining screws located at the top and bottom of the board to ensure proper grounding and to avoid loosening caused by vibration or shock.

In addition the following electrical hazard precautions must be observed.



Caution, Electric Shock Hazard!

Ensure that the system main power is removed prior to installing or removing this board. Ensure that there are no other external voltages or signals being applied to this board or other boards within the system. Failure to comply with the above could endanger your life or health and may cause damage to this board or other system components including process-side signal conditioning equipment.

The CP372 is designed to accept external source voltages (V_{ext}) which can, depending on the application configuration, represent a hazard. In particular, it is possible that hazardous voltages are present on the application interfacing cable to the CP372 front panel connector. It is IMPERATIVE to ensure that the V_{ext} voltages are removed prior to connecting or disconnecting the interface cable.

If this is not possible, it is IMPERATIVE to ensure that no contact is made with the interface cable pins during cable handling, and that when the cable is connected to the CP372, that no short circuiting of cable pins occurs.



ESD Equipment!

This PEP board contains electrostatically sensitive devices. Please observe the following precautions to avoid damage to your board:

Discharge your clothing before touching the assembly. Tools must be discharged before use.

Do not touch any on board components, connector pins, or board conductive circuits.

If working at an anti-static workbench with professional discharging equipment, ensure compliance with its usage when handling this product.

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3.1.2 Installation Procedures

To install the board proceed as follows:

1. Ensure that the safety requirements indicated in chapter 3.1.1 are observed.



Warning!

Failure to comply with the instruction below may cause damage to the board or result in improper system operation. Please refer to chapters 4 and 5 for configuration information.

2. Ensure that the board is properly configured for operation before installing.



Note...

Care must be taken when applying the procedures below to ensure that when the board is inserted it is not damaged through contact with other boards in the system.

3. To install the board perform the following:
   1. Prior to installation of the board disengage the insertion/extraction handle by first unlocking the handle and pressing it down.
   2. Insert the board into an appropriate slot, and, using the insertion/extraction handle, ensure that it is properly seated in the backplane. (Front panel is flush with the rack front; the insertion/extraction handle is locked.)
4. Fasten the front panel retaining screws.



Warning!

Proper and safe operation of the CP372 Analog Output Controller depends on the correct configuration of external source voltages (V_{ext}) and output signal conditioning. System integrators must ensure that all signals to and from the CP372 comply with the specifications set forth in this manual. In particular, at no time may V_{ext} exceed 28 V including times when there is no power applied to the CP372 or system.

DO NOT PROCEED with the next step of this procedure before ensuring compliance with the above mentioned safety requirement.

Failure to comply with the above may cause damage to the board or result in improper system operation. Please refer to chapters 4 and 5 for configuration information.

5. Connect external interfacing cable(s) to the board as required.
6. Ensure that the interfacing cables are properly secured.

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3.1.3 Removal Procedures

To remove the board proceed as follows:

1. Ensure that the safety requirements indicated in chapter 3.1.1 are observed.



Warning!

Care must be taken when applying the procedures below to ensure that when the board is removed it is not damaged through contact with other boards in the system.

2. Disconnect any interfacing cable(s) that may be connected to the board.
3. Loosen both of the front panel retaining screws.
4. To remove the board from the backplane perform the following:
    1. Unlock the insertion/extraction handle by pressing down on the grey locking mechanism in the middle of the handle. (This should be achievable with a minimum of force. If necessary lift the handle up slightly while pressing down on the grey locking mechanism.)
    2. Disengage the board from the backplane by pressing down on the insertion/extraction handle and pull the board out of the slot ensuring that the board does not make contact with adjacent boards. (If the handle does not move, it is not unlocked. Repeat the unlocking procedure above and try again. Do not use force!)
5. Dispose the board as required observing applicable environmental regulations governing the handling and disposition of this type of product.

3.2 Software Installation

Installation of the CP372 driver software is a function of the application operating system. For further information refer to the appropriate software documentation.

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Chapter 4

Configuration

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4. Configuration

The following chapters provide information for configuring the CP372 board for operation.

4.1 Jumper Settings

The CP372 does not have any jumpers which require configuring.

4.2 Analog Output Signal Requirements

In addition to the output signal types and their ranges which have been specified in chapter 1, system integrators must be aware of the need for certain types of output and input configuration requirements for the CP372. The following chapters describe each of the signal types with regards to their individual connection configuration requirements.

4.2.1 Channels

The pinout of the CON2 connector of the CP372 is designed so that for each output channel there are three output pins per channel available. This allows for each channel to be configured separately as required. As can be seen from Figure 2-2, each channel's respective pins are grouped together starting at the top of the connector with channel 0 (cluster A). The configuration of each channel is dependent on the type of analog output signal generated by the CP372. The following chapters address the basic requirements for each type of possible signal.

4.2.2 Analog Voltage Output Signals

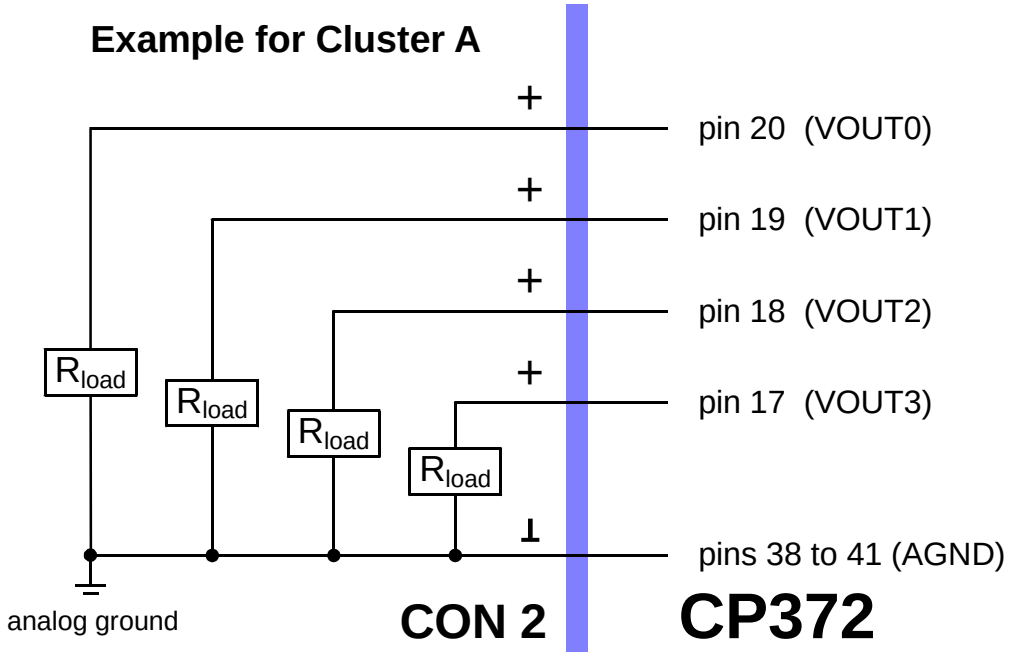
The analog voltage output signals are single-ended with a variety of ranges: uni-polar: 0V to 5V and 0V to 10V; and bipolar: -5V to +5V and -10V to +10V. The current of each output is limited to 5 mA. For the ranges 0 to 5 volts and - 5 to + 5 volts, a load of at least 1 k ohm is required. For the ranges 0 to 10 volts and - 10 to + 10 volts, a load of at least 2 k ohm is required.

Signals of this type are required to be connected: plus to plus, and ground to ground. Refer to Figure 4-1 for this type of connection.

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Figure 4-1: Analog Voltage Signal Output Configuration



4.2.3 Analog Current Output Signals

The analog current output signals are single-ended with a range of 0 to 20 mA. Signals of this type are required to be connected: R_s to **I** and analog ground to ⊥. Refer to Figure 4-2 for this type of connection.

As can be seen from Figure 4-2, V_{ext} is a function of the source resistance for each individual output channel of the CP372. To determine the minimum V_{ext} required for each channel, use the following formula:

$$V_{ext} = I_{out} * (R_{ds\ on} + R_{bias} + R_s)$$

where:
- V_{ext} = required minimum external supply voltage
- I_{out} = 0.02 A
- R_{dson} = 40 ohms (drain - source resistance)
- R_{bias} = 250 ohms bias resistance
- R_s = <nnnn> ohms source resistance

Example:

I_{out} = 0.02 A; R_s = 1 k ohms

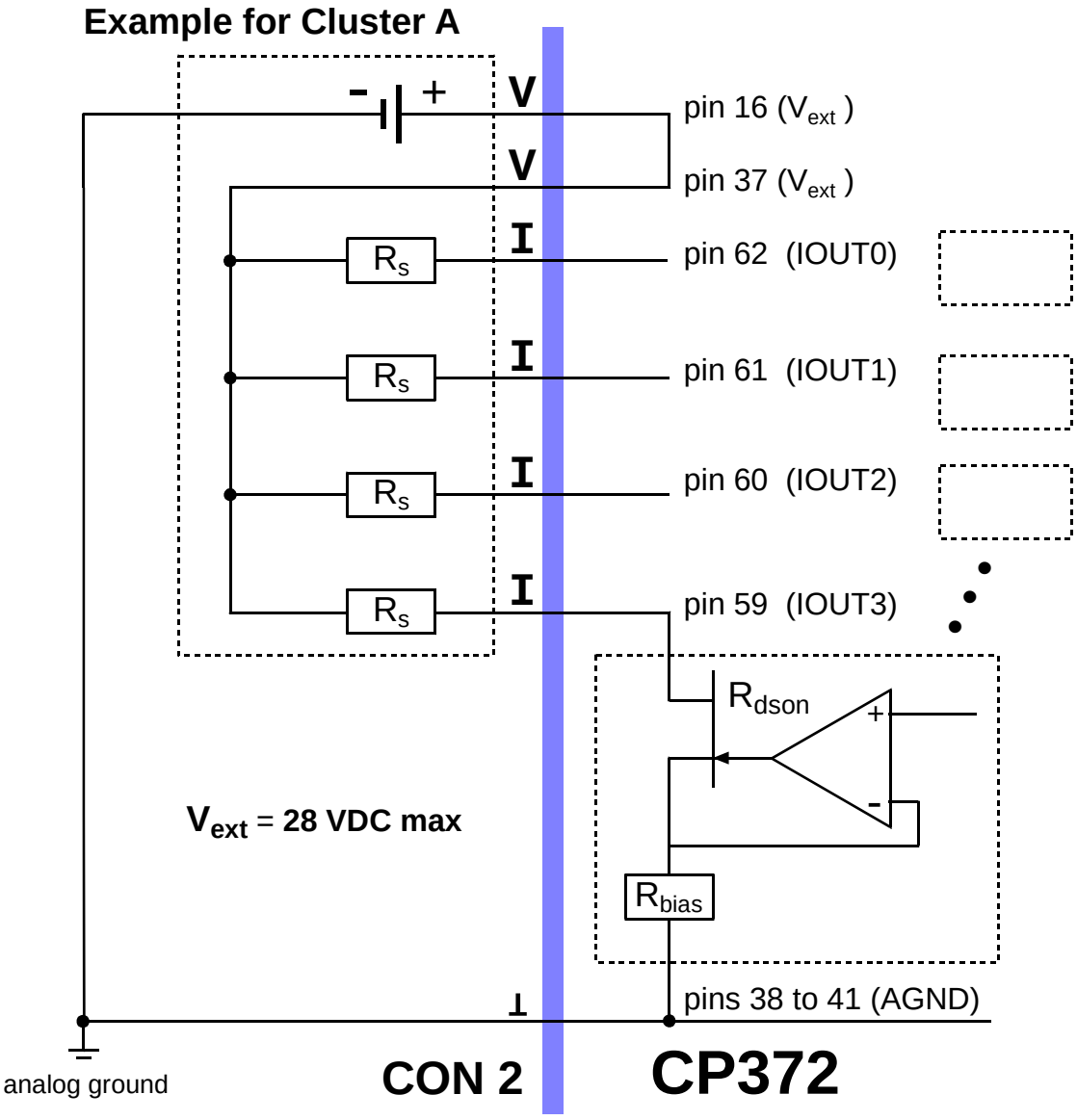
V_{ext} = 0.02A * (40 + 250 + 1000)Ω = **25.8V** (minimum external supply voltage)

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The following two figures, Figures 4- 2 and 4-3, provide examples of the configuration of analog current signal outputs.

Figure 4-2 indicates a configuration where the external source voltage (V_{ext}) is the same for all four channels of cluster A. This example demonstrates the use of the common tie point pins for V_{ext}.

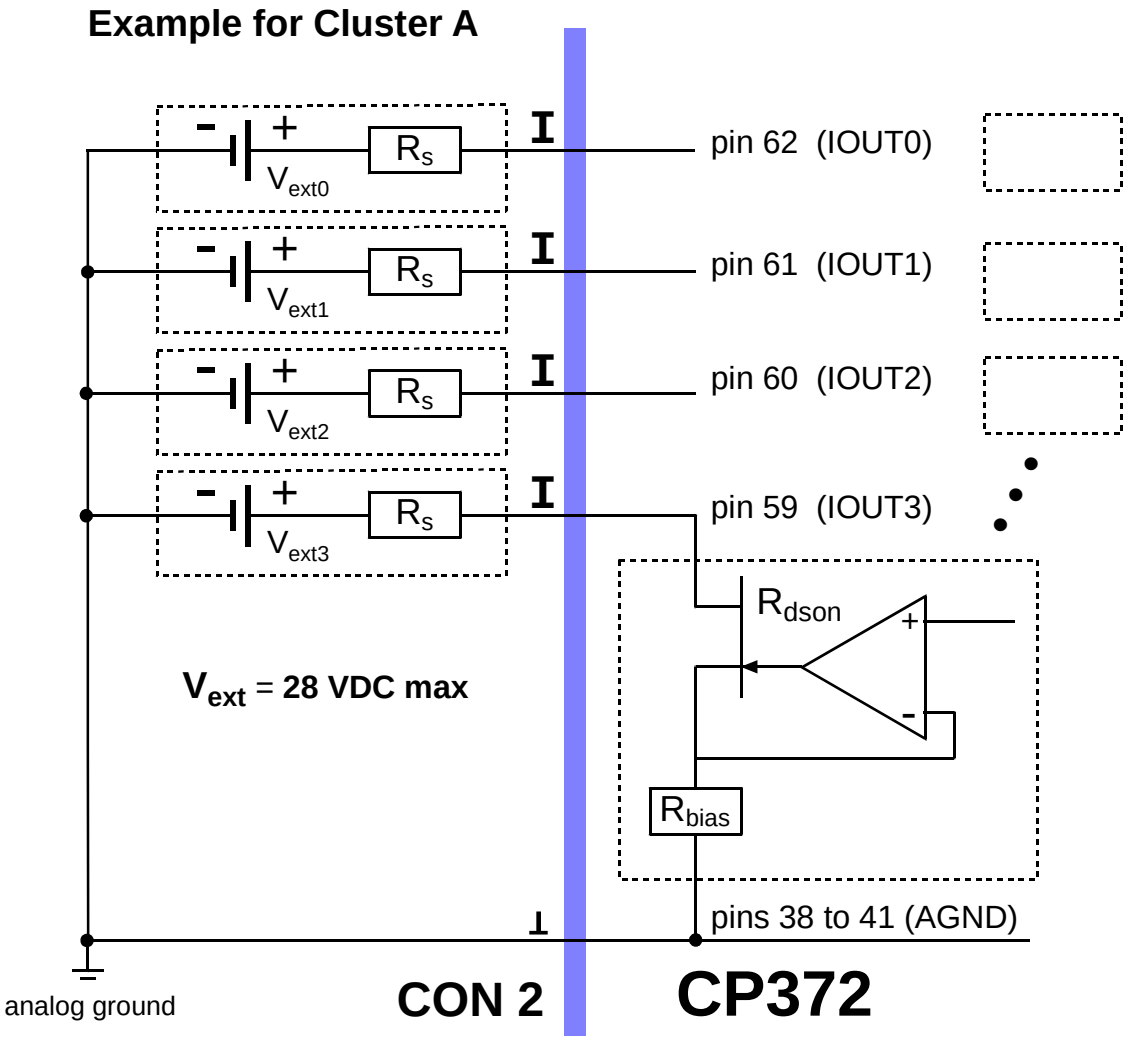
Figure 4-2: Current Output Configuration With a Common External Source Tie Point



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Figure 4-3 demonstrates a configuration for cluster A where each output channel's external source voltage is different due to different source resistances (R_S).

Figure 4-3: Current Output Configuration With Different External Sources (V_{ext})



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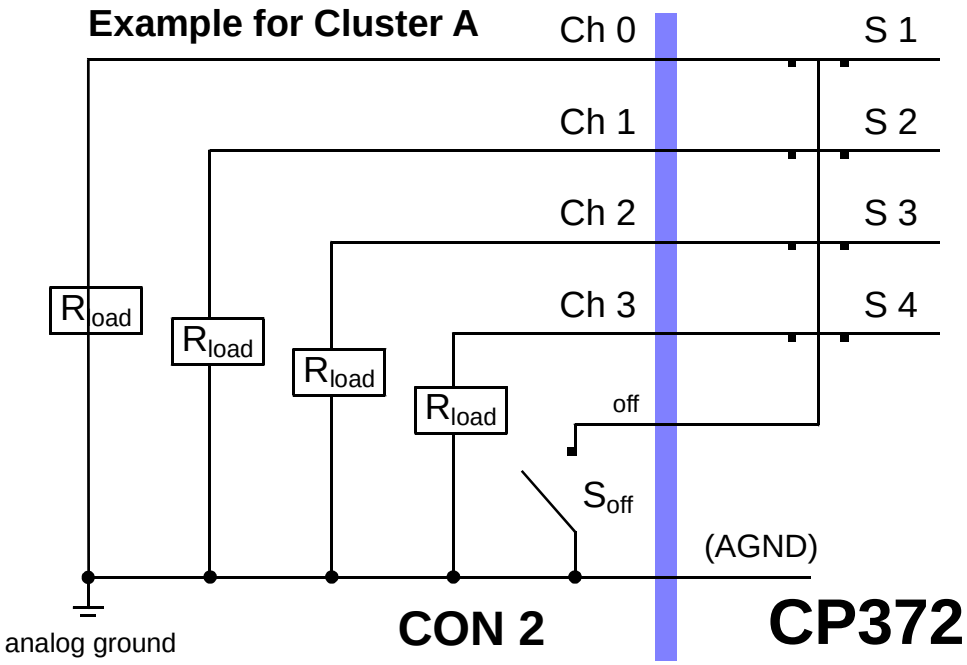
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4.2.4 External Cluster Enable/Disable

The CP372 provides two possibilities to enable or disable all the outputs of an entire cluster at one time. Each individual cluster may be controlled either per software or hardware, whereby the hardware control has priority over the software control. Information regarding the software control is provided with the driver software. The hardware control capability is described as follows.

To make use of the hardware control capability the application must provide some form of external switching capabilty. Figure 4-3 provides basic information for configuring an external switch. Upon power up of the CP372, the output of each cluster is disabled until such time as the application software requests an output of the cluster. After cluster output is enabled, it can still be controlled by external switching. This feature permits external intervention either automatically or manually at any time independent of the applicaton software.

Figure 4-4: External Cluster Enable/Disable

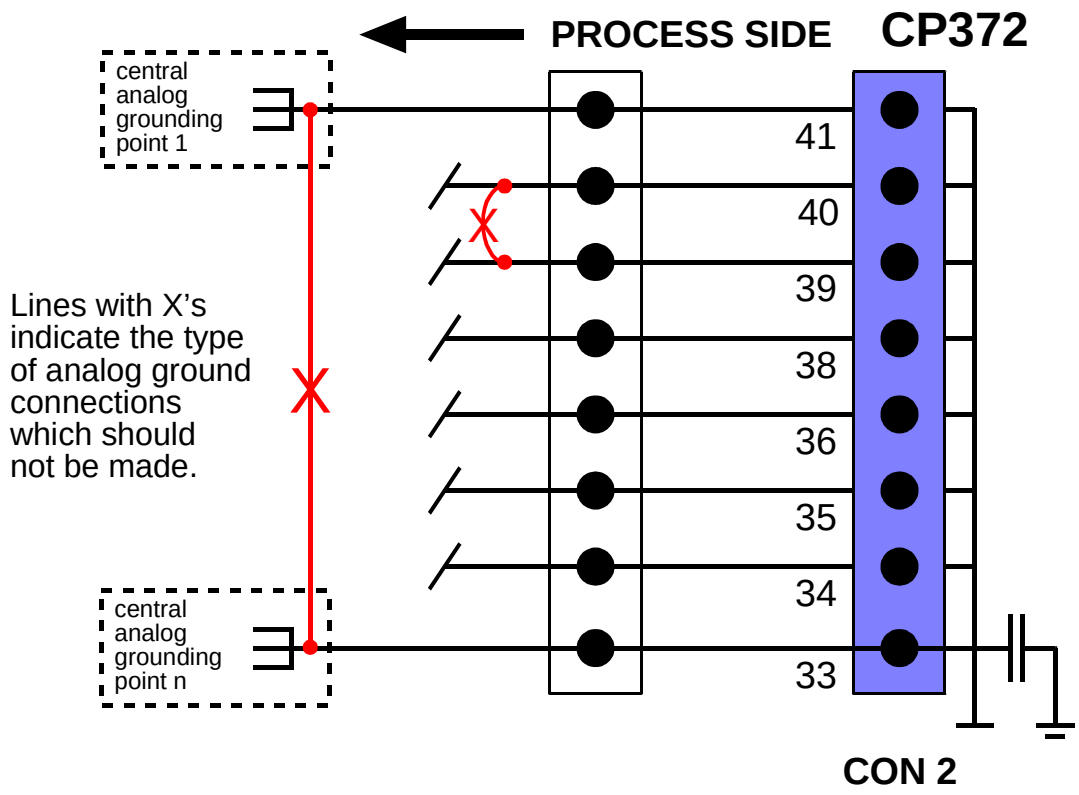


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4.2.5 Analog Ground Usage

Analog ground usage must be carefully considered in order to avoid ground loops or floating signals which can ultimately lead to the degradation of the system performance. The figure below indicates the nominal analog grounding situation, but is, of course, very much subject to the requirements of the application as a whole. What is important, however, is to ensure that ground loops do not get created in the course of the wiring up of the various system components. Additionally, it may be necessary to use heavier gauge wiring to avoid excessive loading of single wires.

Figure 4-5: Analog Grounding



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4.3 Programming Interface

4.3.1 Access Control Logic

All the resources of the CP372 are mapped within the 64KB PCI memory address space which itself is set in the PCI configuration register BAR0. The port size of all local or backend registers is 32-bit by default. The address map of the registers is as follows.

Table 4-1: I/O Address Map of CP372

BASE ADDRESS (BAR0)	SIZE	FUNCTION
+ 0x0000	4 kB	COMMON BOARD REGISTER
0x0800	32 bit	com_sta Hardware Status Register
0x0C00	32 bit	com_ctl Hardware Debug Register
+ 0x1000	4 kB	CAPABILITY ROM, SERIAL EEPROM
0x1000	32 bit	cmd_r Command Register
0x1400	32 bit	ctl_r Control Register
0x1800	32 bit	sta_r Status Regsiter
0x1C00	32 bit	dat_r Data Register
+ 0x2000	4 kB	DAC CLUSTER A
0x2400	32 bit	ctl_a, Cluster a Common Control Register
0x2C00	32 bit	dat_a_0 DAC Data channel # 0
0x2C04	32 bit	dat_a_1 DAC Data channel # 1
0x2C08	32 bit	dat_a_2 DAC Data channel # 2
0x2C0C	32 bit	dat_a_3 DAC Data channel # 3

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Table 4-1: I/O Address Map of CP372

BASE ADDRESS (BAR0)	SIZE	FUNCTION
+ 0x3000	4 kB	DAC CLUSTER B
0x3400	32 bit	ctl_b, Cluster b Common Control Register
0x3C00	32 bit	dat_b_0 DAC Data channel # 0
0x3C04	32 bit	dat_b_1 DAC Data channel # 1
0x3C08	32 bit	dat_b_2 DAC Data channel # 2
0x3C0C	32 bit	dat_b_3 DAC Data channel # 3
+0x4000 0xFFFF	48 kB	reserved for additional clusters

4.3.2 DAC Control Logic

This part of the IO Control Logic controls the communication with the DAC. The DAC integrates 4 channels per chip (2 clusters for a total of 8 channels) and has a serial bus interface operating at 2 MHz.

DAC operating mode is individually programmable for each channel, i.e. the polarity (unipolar/ bipolar) and range (5/10V and 20mA). After initialization of the corresponding DAC Control Registers an Enable Bit must be set to ‘1’.

The DAC Control Logic handles the cyclic setup of the necessary DAC control word including start bit, channel address, channel mode, and clock mode without any software intervention. The digital output data are automatically stored in dual-ported data registers. An arbiter avoids access conflicts between PCI access and DAC access to the same data register.

The architecture of the CP372 integrates the memory mapped data registers which are visible to the programmer only and the actual DAC channel registers which are not visible to the programmer. Data is serialized and transferred between data register and the actual DAC by a hardware sequencer automatically and continuously in a loop.

The DAC data registers can be written to at any time and independently of whether the DAC cluster is enable or not.

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Table 4-2: DAC Common Control Register Bit Map

BITS	TYP.	DEF.	FUNCTION
31	R/W	0	Enable
30 - 8	R/W	00	reserved
7 - 6	R/W	00	RNG, BIP for DAC channel # 3
5 - 4	R/W	00	RNG, BIP for DAC channel # 2
3 - 2	R/W	00	RNG, BIP for DAC channel # 1
1 - 0	R/W	00	RNG, BIP for DAC channel # 0

Table 4-3: RNG, BIP Bits

RNG	BIP	INPUT RANGE
0	0	0 – 5 V 0 - 20 mA
1	0	0 – 10 V
0	1	± 5 V
1	1	± 10 V

Table 4-4: DAC Data Registers Bit Map

BITS	TYPE	DEFAULT	FUNCTION
31 - 12	R	0	reserved
11 - 0	R	0	Data, 12 bit digit

4.3.3 Programming the Board Capability ROM

Besides correction data for gain and offset errors other board specific capabilities can be stored in this dedicated onboard ROM. The purpose is to allow the software to configure itself according to the hardware version (e.g. type, number of channels, insertion of components, input circuit, etc.).

The Board Capability ROM is implemented using a 4 KBit serial EEPROM of the type 93LC66 from Microchip.

The serial interface of the device has been realized in hardware resulting in a very simple register based programming interface with command, control, and data registers. All protocol and serial timing specifications are resolved by hardware.

Programming of the Board Capability ROM is undertaken as follows:

Tthe control word is written into the ROM Control Register including command opcode and internal address. Then optional data (in case of Write action) is written into the ROM Data Register. Command execution is started by setting the Startbit in the ROM Command Register. Then Ready/Busy must be polled in the ROM Status Register. After reaching Ready status, the next command can be set up and data (in case of Read action) can be fetched from the ROM Data Register.

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Table 4-5: ROM Command Register Bit Map

BITS	TYPE	DEFAULT	FUNCTION
31	R/W	0	Startbit
30 - 0	R/W	00	reserved

Note: The Startbit will automatically be reset as soon as an action is completed.

Table 4-6: ROM Control Register Bit Map

BITS	TYPE	DEFAULT	FUNCTION
31 - 18	R/W	0	reserved
17 - 16	R/W	00	Opcode
15 - 9	R/W	00	reserved
8 - 0	R/W	00	internal address (A8..A0)

Note: The commands READ, EWEN (write enable) and WRITE are sufficient for all purposes.

Table 4-7: Opcodes and Commands

OPCODE	A8 ... A0	COMMAND
00	11xxxxxxx	EWEN
10	xxxxxxxxx	READ
01	xxxxxxxxx	WRITE

Note: The EWEN (Erase and Write enable) command must be executed once before the first write.

Table 4-8: ROM Status Register Bit Map

BITS	TYPE	DEFAULT	FUNCTION
31	R/W	0	Busy
30 - 0	R/W	00	reserved

Note: As soon as the Startbit is set the Busy/Ready bit becomes active (Busy=1). It remains set as long as the command is executed and is reset when command execution is complete.

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Table 4-9: ROM Data Register Bit Map

BITS	TYPE	DEFAULT	FUNCTION
31-8	R/W	0	reserved
7-0	R/W	0	Data (for data read and write commands)

4.3.4 Common Board Registers

These registers are for internal test and debug only. The Common Status Register contains Logic Version and PCB Version. The Common Control Register is a read/write register without any further functionality. Neither of these should be used by standard software.

Table 4-10:Hardware Debug Register Bit Map

BITS	TYPE	DEFAULT	FUNCTION
31-0	R/W	0	reserved

Table 4-11:Hardware Status Register Bit Map

BITS	TYPE	DEFAULT	FUNCTION
31 - 16	R	0	reserved
15 - 8	R	00	HW Version (PCB Index)
7 - 0	R	01	Logic Version

Note: The HW version starts with 0, Logic Version with 1. It will be incremented for each released version.

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Chapter 5

System Considerations

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5. System Considerations

5.1 Introduction

In addition to the basic specification requirements for signals to and from the CP372 which have been addressed in the previous chapters, system integrators need to be aware of the overall system environment and the application needs when designing the interfacing to the CP372. There are certain basic considerations which require explicit resolution as well as others which are of a more subtle nature that may under circumstances impact the performance or validity of the digital to analog conversion process. The following chapters address a number of more apparent considerations which should be addressed but certainly not all of the possible situations which may be encountered. Many of the considerations presented here are recommendations, but some are definite requirements if the CP372 is to successfully achieve its purpose.

5.2 General

Considerations:

1. For output channels, the **I** or **V** pins respectively are not to be connected except when required.
2. It is recommended to use twisted pair wiring for output signals.
3. Mixing of output signal types to be generated by the CP372 is permitted.
4. The type of signal expected to be generated for each output channel of the CP372 must correspond to the driver software configuration for that channel. If not the result will be erroneous and the CP372 may be damaged.
5. Care must be taken to ensure that proper grounding concepts are followed, and that the integrity of the grounding system within the application be maintained.
6. Output wire routing should avoid proximity to high voltage or current sources.
7. Where possible output wiring length should be kept as short as possible.

5.3 Shielding

Considerations:

1. Output cable shielding in general is recommended.
2. The requirements for shielding can be seen primarily as a function of the system design and environment, but empirical results must also be considered.
3. The CON2 connector has a metal housing which is connected to the CP372 shield and is isolated from the analog ground.
4. Ensure that if shielding is used that it is not in anyway connected to the analog ground.

5.4 Process-side Signal Conditioning

Considerations:

1. Output signal conditioning on the process side of the application must be as specified for the signal type or erroneous results will occur as well as possible damage to the CP372.
2. Ensure that when analog ground pins on CON2 are used that on the process side no grounding loops are created. Refer to chapter 4 for further information.

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5.5 Cable Interfacing

Considerations:

1. No modification to the CP372 itself is permitted (i.e. connector pin shorting).
2. The resistance of cabling contacts should be kept to an absolute minimum. In any event the contact resistance must be taken into consideration when determining the signal conditioning requirements of the application. In particular, for analog current outputs this can be a significant factor in determining V_{ext} requirements as well as being a source of operational performance degradation.
3. If necessary, cabling to the CP372 CON2 connector should physically be fixed to prevent strain on the CON2 connector.

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