Modular Computers®

CP381

30 Channel CompactPCI
Digital Input Controller

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The product described in this manual is in compliance with all applied CE standards.

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This manual was realized by: **TPD/Engineering, PEP Modular Computers GmbH**.

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CE Conformity

This symbol indicates that the product described in this manual is in compliance with all applied CE standards. Please refer also to the section “Applied Standards” in this manual.



Caution, Electric Shock!

This symbol and title warn of hazards due to electrical shocks (> 60V) when touching products or parts of them. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your material.

Please refer also to the section “High Voltage Safety Instructions” on the following page.



Warning, ESD Sensitive Device!

This symbol and title inform that electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Please read also the section “Special Handling and Unpacking Instructions” on the following page.



Warning!

This symbol and title emphasize points which, if not fully understood and taken into consideration by the reader, may endanger your health and/or result in damage to your material.



Note...

This symbol and title emphasize aspects the reader should read through carefully for his or her own advantage.

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For Your Safety

Your new *PEP* product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new *PEP* product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions



Warning!

All operations on this device must be carried out by sufficiently skilled personnel only.



Caution, Electric Shock!

Before installing your new PEP product into a system always ensure that your mains power is switched off. This applies also to the installation of piggybacks.

Serious electrical shock hazards can exist during all installation, repair and maintenance operations with this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing work.

Special Handling and Unpacking Instructions



ESD Sensitive Device!

Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory back-up, ensure that the board is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the board.

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This device should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This applies also to the operational temperature range of the specific board version, which must not be exceeded. If batteries are present their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, please follow only the instructions supplied by the present manual.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the board please re-pack it as nearly as possible in the manner in which it was delivered.

Special care is necessary when handling or unpacking the product. Please, consult the special handling and unpacking instruction on the previous page of this manual.

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Chapter 1

Introduction

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1. Introduction

1.1 System Overview

The CompactPCI board described in this manual operates with the PCI bus architecture to support additional I/O and memory-mapped devices as required by various industrial applications. For detailed information concerning the CompactPCI standard, please consult the complete Peripheral Component Interconnect (PCI) and CompactPCI Specifications. For further information regarding these standards and their use, visit the homepage of the *PCI Industrial Computer Manufacturers Group (PICMG)*.

Many system relevant CompactPCI features that are specific to PEP Modular Computers CompactPCI systems may be found described in the PEP CompactPCI System Manual. Please refer to the section “Related Publications” at the end of this chapter for the relevant ordering information.

The CompactPCI System Manual includes the following information:

- Common information that is applicable to all system components, such as safety information, warranty conditions, standard connector pinouts etc.
- All the information necessary to combine PEP’s racks, boards, backplanes, power supply units and peripheral devices in a customized CompactPCI system, as well as configuration examples.
- Data on rack dimensions and configurations as well as information on mechanical and electrical rack characteristics.
- Information on the distinctive features of PEP CompactPCI boards, such as functionality, hot swap capability. In addition, an overview is given for all existing PEP CompactPCI boards with links to the relating data sheets.
- Generic information on the PEP CompactPCI backplanes, such as the slot assignment, PCB form factor, distinctive features, clocks, power supply connectors and signalling environment, as well as an overview of the PEP CompactPCI standard backplane family.
- Generic information on the PEP CompactPCI power supply units, such as the input/output characteristics, redundant operation and distinctive features, as well as an overview of the PEP CompactPCI standard power supply unit family.

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1.2 Product Overview

The CP381 Digital Input controller is part of a comprehensive concept whose goal is to provide CompactPCI system integrators with a complete range of CompactPCI I/O products which include the functions of analog input, analog output, digital input and digital output implemented on separate individual boards. This concept ensures the maximum degree of system design flexibility thus allowing for the efficient and effective usage of available resources.

The CP381 is a 3U/4HP CompactPCI board which provides 30 digital input channels and has some useful optional features (such as debouncing, input event detection, input capture and-compare).

The basic functions of this board are to provide interfacing to the application (process), perform D/D signal conversion, and to make the raw digitized data available for further processing.

The major components involved in these processes are the front end (process side) Signal Conditioning and the Digital Input Process and Communications (DIProcomm) Controller which is realized within a Field-Programmable Gate Array (FPGA). The DI ProComm controller is designed to provide effective and efficient control of digital input signal conditioning as well as interfacing with the CPCI system controller.

The following table provides a quick overview of the CP381 board.

Table 1-1: CP381 Product Overview

CP381 FEATURES	DESCRIPTION
Digital Input Board	CompactPCI: 3U, 4HP 33 MHz system clock 32-bit address and data bus Designed for Plug&Play Complies with the CPCI specification
Input Signals	Voltage range: low: -3V to +5V high: +11V to + 30 V (+24V standard) Maximum current: 5 mA
Output Data	A maximum of 30 measured digital values Interrupt messages (optional) Programmable registers (writeable compare, event and latch registers)
Debouncing	Range of settings available: 33 MHz, 128 kHz, 32 kHz, 8 kHz, 2 kHz, 500 Hz, 125 Hz, 31 Hz (30ns default)
Monitor and Control	Two green LED's: RUN and HIT DI ProComm controller System Master driver software

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1.3 Board Overview

1.3.1 Board Introduction

The CP381 is a 30 channel digital input board. The source of the digital inputs must be a voltage generator. The board accepts only single-ended voltages up to a maximum of +30V. The input current is limited to 5 mA over the specified input voltage range.

Input signal processing begins with the presentation of the signal to the front panel connector. Signal conditioning prior to the signal reaching the DI ProComm controller includes: overvoltage protection, ESD, low-pass filtering, inverse polarity protection, defined low and high ranges, current limitation, optoisolation and buffering.

After signal conditioning, all parallel digital data is routed to the DI ProComm controller, where the control and status registers are set.

The DI ProComm controller controls the interface with the CompactPCI bus and the dedicated software.

Input signal types and ranges are as follows:

- Edge frequency:
  - Maximum 10 kHz
- Voltage Ranges:
  - High range: +11V to +30V (+24V nominal)
  - Low range: -3V to +5V
- Signal is single-ended

Output data:

The following outputs are routed from the DI ProComm controller to the CompactPCI bus:-

- Input data for all channels as a 32-bit value (each bit from 0 - 29 represents the status of the respective input channel)
- Flag set information from the control and status registers
- Interrupts

1.3.2 Board Specific Information

Specific board components involved in the signal conditioning and data handling processes are:

- One front panel connector (62-pin, female, D-sub type)
- 30 channels of input signal conditioning
- Optoisolation for each channel
- One FPGA (the DI ProComm controller)
- One CompactPCI bus connector (J1, board to backplane, 132-pin, female, six row)
- JTAG/ISP onboard programming connector (10-pin, male, dual row)
- One EEPROM (CapROM)

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1.4 System Relevant Information

The following system relevant information is general in nature but should still be considered when developing applications using the CP381.

Table 1-2: System Relevant Information

SUBJECT	INFORMATION
System Configuration	The CP381 operates with a system clock frequency of 33 MHz. The number of CP381's which can be installed in any one system depends solely on the number of CPCI slots available.
Master/Slave Functionality	The CP381 functions only as a slave. As such it requires a system master for servicing.
System Controller	The CP381 cannot function as a system controller.
Digital Inputs	Digital inputs to the CP381 must be conform to the inputs specifications set forth in this manual for the CP381. In most cases, some form of signal conditioning will be required on the process side prior to a signal being presented to the CP381.

1.4.1 System Configuration

When implementing applications, precautions must be taken to ensure that the input signals presented to the CP381 comply with the specifications set forth in this manual. For this reason it will be necessary for most applications to provide signal conditioning prior to presenting the digital inputs to the CP381. In addition, it is imperative that signal interference be kept to a minimum. Please refer to chapters 4 and 5 for further information.

1.4.2 Driver Software

The CP381 is supplied with appropriate driver software which provides software interfacing with the system master.

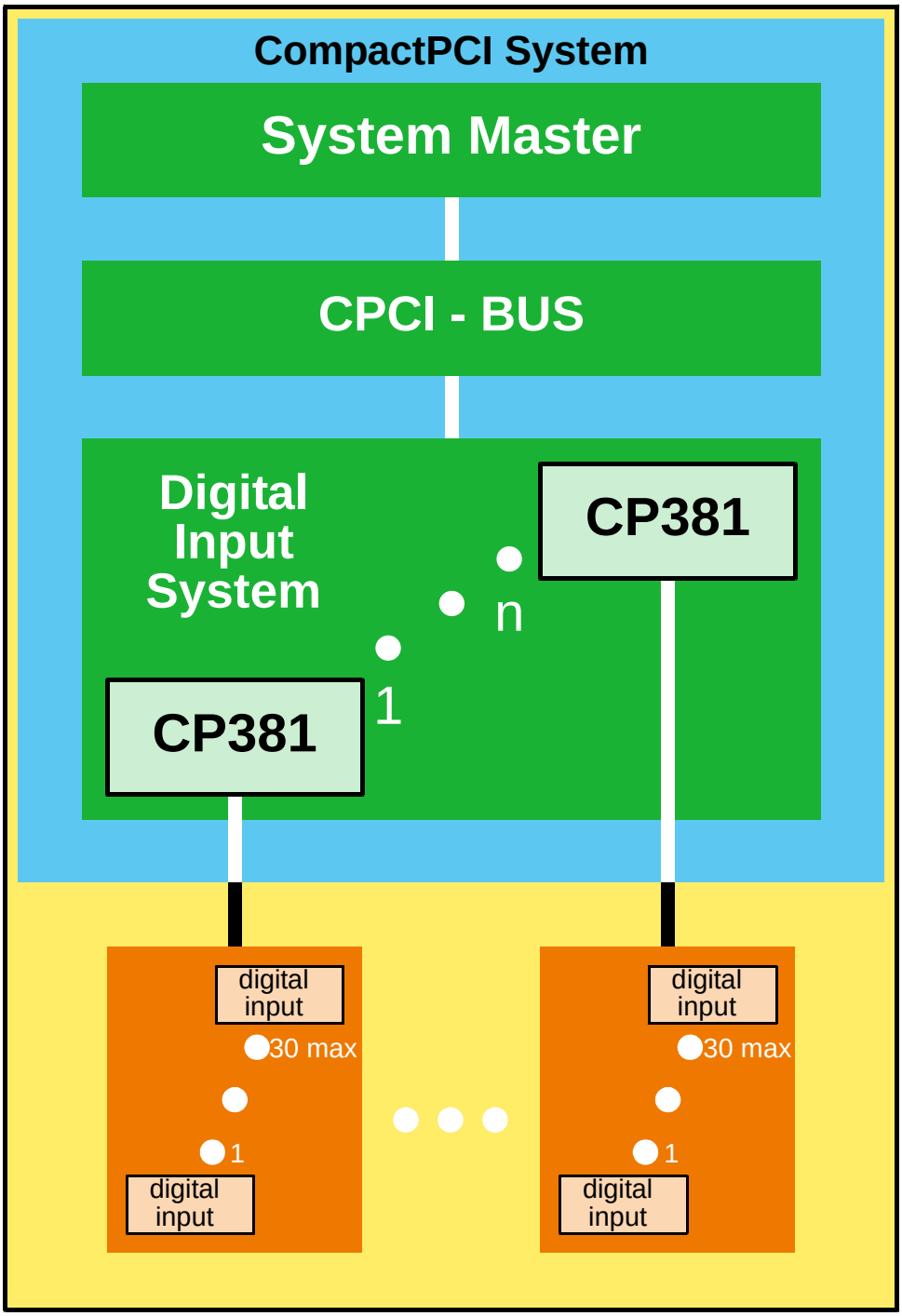
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1.5 Board Diagrams

The following diagrams illustrate board functionality and component layout.

1.5.1 System Level Interfacing

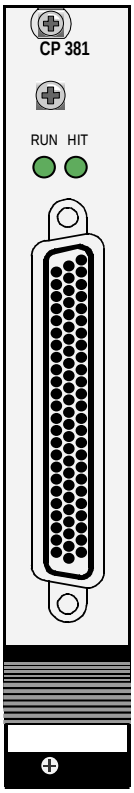
Figure 1-1: CP381 System Level Interfacing Diagram



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1.5.2 Front Panel

Figure 1-2: CP381 Front Panel

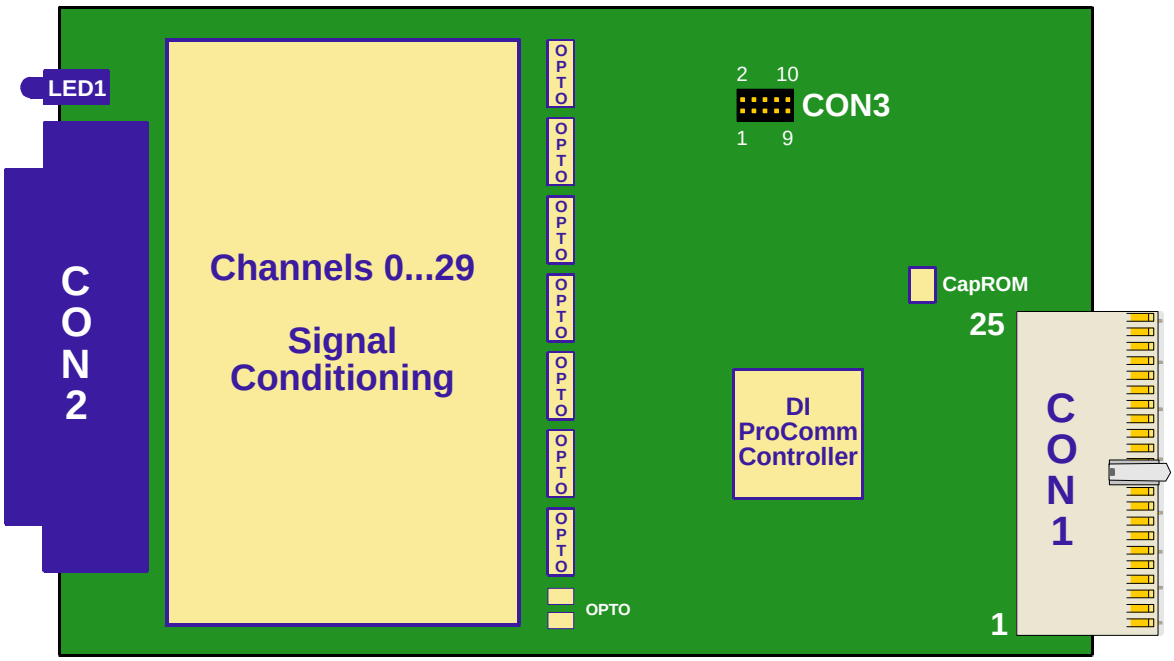


LEGEND:

"RUN" and "HIT" are status LED's. The different LED status combinations are illustrated and an explanation of their meaning given in the Operation M/C section in chapter 2.5

1.5.3 Board Layout

Figure 1-3: CP381 Board (Front View)



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1.6 Technical Specifications

Table 1-3: CP381 Main Specifications

GROUP	TYPE	DESCRIPTION
DI ProComm Controller and Related	FPGA Logic Device	Provides CompactPCI interfacing and IO control logic
Peripheral Memory	CapROM	4 kBit (512 byte) EEPROM
External Interfaces	Digital Input	One 62-pin, female, three row, D-sub connector Supports up to thirty digital input channels
	CompactPCI Bus	One, 132-pin, female, six row connector (standard CPCI type connector for J1)
Internal Interfaces	JTAG/ISP	JTAG/ISP 10-pin SMD connector for programming and testing purposes
Indicators	Front Panel LED's	Two green LED's to indicate operational status
General	Mechanical	Conforms with IEEE 1101.1
	Power Requirements	Voltage: 3.3V
	Power Consumption	370 mW maximum
	Temperature Range	Operational: 0ºC to +70ºC Standard -40ºC to +85ºC E2 Storage: -55ºC to +125ºC
	Humidity	0% to 95% non-condensing
	Dimensions	100 mm x 160 mm single height Eurocard
	Board Weight	145 grams
Software Driver Information (See note below)	PCI Header	Device ID: 0x5555 Vendor ID: 0x1556 Class Code: 0x110000 Subsystem Device ID: 0x00E0 Subsystem Vendor ID: 0x1518



Note...

The Device ID and Vendor ID refer to the chip manufacturer. In the Class Code value given, "11" relates to the data acquisition and signal processing controllers and "0000" relates to the DPIO modules. Subsystem Device ID and Subsystem Vendor ID are defined by *PEP*.

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Table 1-4: CP381 Analog Input Specifications

TYPE	DESCRIPTION
Input Voltage Range	Low: -3V to +5V High: +11V to +30V
Channels	30 channels
Channel Connections	2 pins per channel
Input Filter (edge frequency)	10 kHz
Input Protection	8 kV ESD
Isolation	2 kV process to system
Input Impedance	Minimum: 1.5 k ohm Maximum: 6 k ohm at 30V

1.7 Applied Standards

The *PEP Modular Computers'* CompactPCI systems comply with the requirements of the following standards:

Table 1-5: Applied Standards

	TYPE	STANDARD
CE	Emission	EN50081-1
	Immunity, Industrial Environment	EN50082-2
	Immunity, IT Equipment	EN55024
	Electrical Safety	EN60950
MECHANICAL	Mechanical Dimensions	IEEE 1101.1
ENVIRONMENTAL TESTS	Vibration, Sinusoidal	IEC68-2-6
	Random Vibration, Broadband	IEC68-2-64 (3U boards)
	Permanent Shock	IEC68-2-29
	Single Shock	IEC68-2-27

1.8 Related Publications

Table 1-6: Related Publications

	ISSUED BY	DOCUMENT
CompactPCI Systems	PICMG	CompactPCI Specification, V. 2.0, Rev. 3.0
	PEP Modular Computers	CompactPCI Systems Manual (ID 19953)

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Chapter 2

Functional Description

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2. Functional Description

The following sections present more detailed, board level information about the CP381 digital input controller whereby the board components and their basic functionality are discussed in general.

2.1 General Information

The CP381 is comprised basically of the following:

- Signal conditioning
- DI ProComm controller
  - Controls digital data acquisition and provides interfacing to the CompactPCI bus
- System interfaces for:
  - Digital inputs
    - 30 channels
    - One 62-pin, female, 3-pin row, D-sub connector (CON2)
  - CompactPCI bus
    - 132-pin, female, 6-pin row connector (CON1)
    - CompactPCI specification
  - Testing and program development (JTAG/ISP) connector (CON3)
- On board memory: Capability EEPROM (CapROM)
- Monitor and Control
  - Two green LED's
  - Registers
- Software

2.1.1 Signal Conditioning

The digital input signal conditioning consists of the following:

- Overvoltage protection
- Low-pass signal filtering
- Current limitation
- Inverse polarity protection
- Input signal high-low determination
- Output signal stabilization buffering
- Optoisolation: galvanic isolation of process side from system side

2.1.2 DI ProComm Controller

The DI ProComm controller is responsible for supervising and controlling the digital data acquisition process and maintaining communication with the CompactPCI system master. Applications address the CP381 through its software driver interface within the system master whereby the controller accepts requests from the driver and executes them accordingly. Digital data from the signal conditioning is processed through the DI ProComm controller and then made available to the system master.

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2.1.3 System Interfaces

The CP381 provides interfacing capability for the following system elements:

- Digital input
- CompactPCI bus
- Test and program development: JTAG/ISP

Digital input interfacing is achieved via the CON2 connector. Interfacing to the CompactPCI bus is accomplished via the CON1 connector. Test and program development is supported by the CON3 connector.

2.1.4 Monitor and Control

Various monitor and control functions are available for the operation of the CP381. Two LED's are available for operator interaction. In addition, applications have access via the System Master driver software to board specific registers.

2.1.5 Software

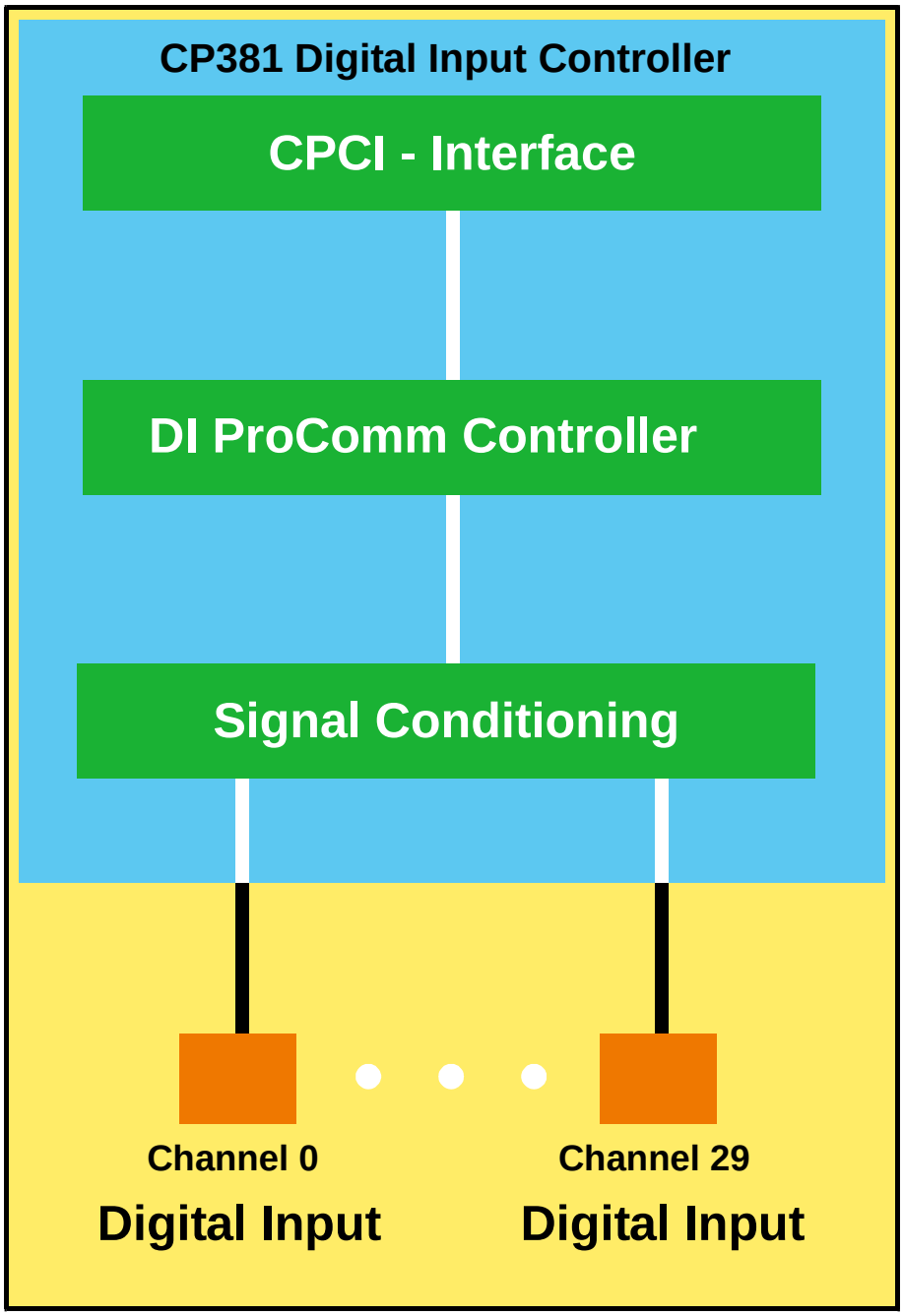
Driver software is available for the System Master application software.

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2.2 Board Level Interfacing Diagram

The following figure demonstrates the interfacing structure between the internal processing modules of the CP381 and other major CP381 system components. Where CP381 system elements have common interfacing they are grouped into a block. Interfacing common to only one element of a block is indicated with a direct connecting line. The interfacing lines are shown in white where they are onboard and in black for board external interfacing.

Figure 2-1: CP381 Board Level Interfacing



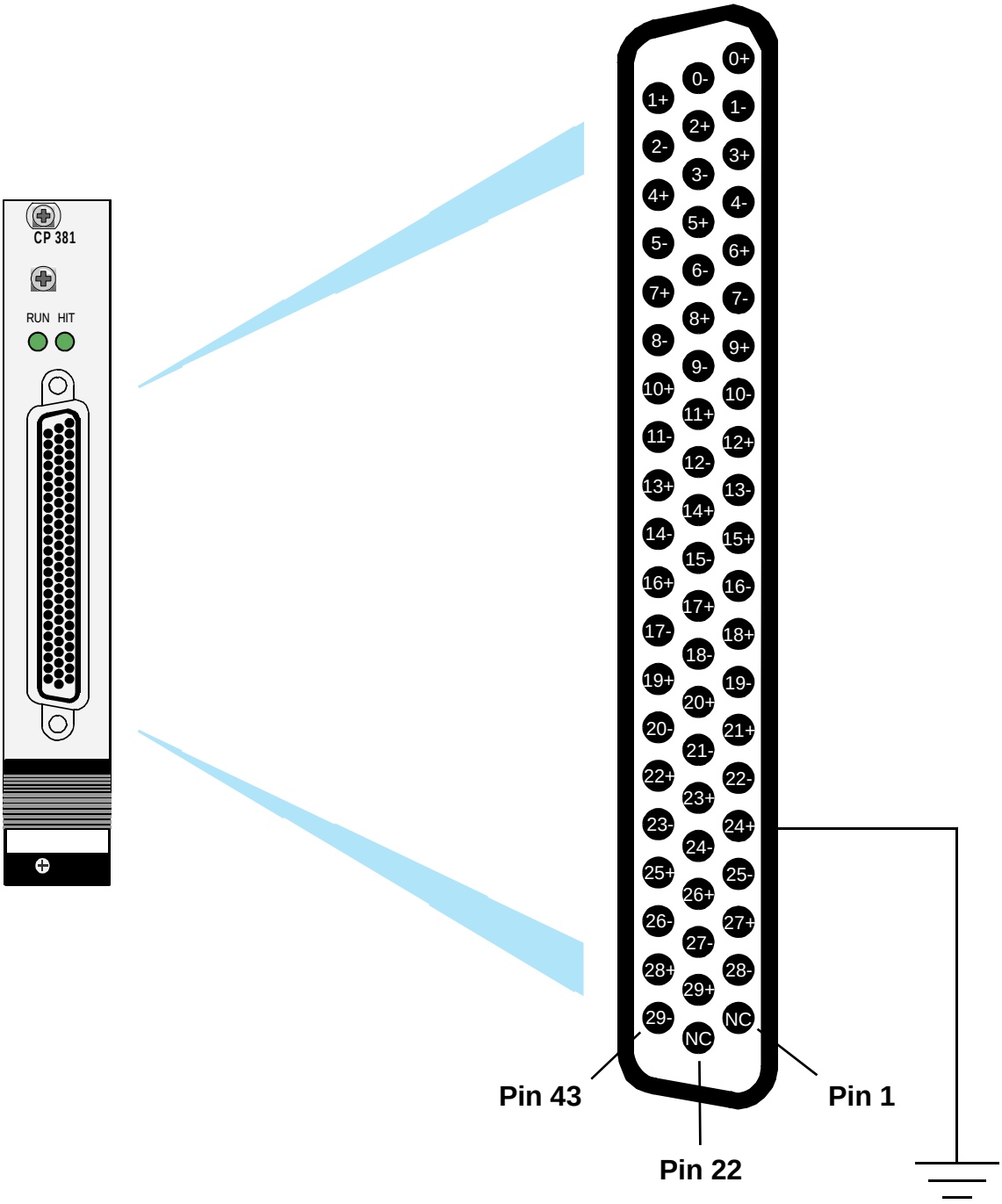
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2.3 System Interfaces

2.3.1 Digital Input Interface

The digital input interface is routed through the CON2 connector. The following figure and table indicate the pin layout and pinout of this connector.

Figure 2-2: Pin Layout of the Digital Input Interface Connector CON2



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Table 2-1: Pinout of the Digital Input Interface Connector CON2

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	NC	22	NC	43	DIGIN 29-
2	DIGIN 28-	23	DIGIN 29+	44	DIGIN 28+
3	DIGIN 27+	24	DIGIN 27-	45	DIGIN 26-
4	DIGIN 25-	25	DIGIN 26+	46	DIGIN 25+
5	DIGIN 24+	26	DIGIN 24-	47	DIGIN 23-
6	DIGIN 22-	27	DIGIN 23+	48	DIGIN 22+
7	DIGIN 21+	28	DIGIN 21-	49	DIGIN 20-
8	DIGIN 19-	29	DIGIN 20+	50	DIGIN 19+
9	DIGIN 18+	30	DIGIN 18-	51	DIGIN 17-
10	DIGIN 16-	31	DIGIN 17+	52	DIGIN 16+
11	DIGIN 15+	32	DIGIN 15-	53	DIGIN 14-
12	DIGIN 13-	33	DIGIN 14+	54	DIGIN 13+
13	DIGIN 12+	34	DIGIN 12-	55	DIGIN 11-
14	DIGIN 10-	35	DIGIN 11+	56	DIGIN 10+
15	DIGIN 9+	36	DIGIN 9-	57	DIGIN 8-
16	DIGIN 7-	37	DIGIN 8+	58	DIGIN 7+
17	DIGIN 6+	38	DIGIN 6-	59	DIGIN 5-
18	DIGIN 4-	39	DIGIN 5+	60	DIGIN 4+
19	DIGIN 3+	40	DIGIN 3-	61	DIGIN 2-
20	DIGIN 1-	41	DIGIN 2+	62	DIGIN 1+
21	DIGIN 0+	42	DIGIN 0-		

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2.3.2 CompactPCI Interface and Pinout

The CompactPCI interface is based on the specification PICMG 2.0 R 3.0, 10/1/99. The following figure and table indicate the pin layout and pinout of the CompactPCI connector, CON1 (J1).

Figure 2-3: CPCI Connector CON1 (J1)

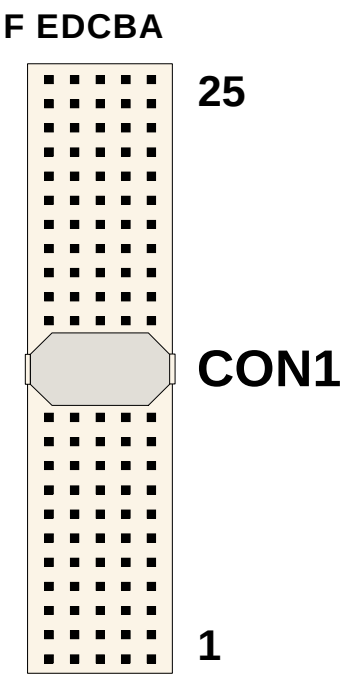


Table 2-2: CompactPCI Connector CON1 (J1)

PIN	PIN ROW					
	A	B	C	D	E	F
1	NC	NC	NC	NC	NC	GND
2	NC	NC	NC	TDO	TDI	GND
3	INTA#	NC	NC	NC	NC	GND
4	NC	GND	NC	NC	NC	GND
5	NC	NC	RST	GND	NC	GND
6	NC	GND	3,3V	CLK	AD[31]	GND
7	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND
8	AD[26]	GND	NC	AD[25]	AD[24]	GND
9	C/BE[3]	IDSEL	AD[23]	GND	AD[22]	GND
10	AD[21]	GND	3,3V	AD[20]	AD[19]	GND
11	AD[18]	AD[17]	AD[16]	GND	C/BE[2]	GND
12-14 Key Area						
15	3,3V	FRAME#	IRDY	GND	TRDY	GND
16	DEVSEL#	GND	NC	STOP	LOCK	GND
17	3,3V	NC	NC	GND	PERR	GND
18	SERR#	GND	3,3V	PAR	C/BE[1]	GND
19	3,3V	AD[15]	AD[14]	GND	AD[13]	GND
20	AD[12]	GND	NC	AD[11]	AD[10]	GND
21	3,3V	AD[9]	AD[8]	M66EN	C/BE[0]	GND
22	AD[7]	GND	3,3V	AD[6]	AD[5]	GND
23	3,3V	AD[4]	AD[3]	NC	AD[2]	GND
24	AD[1]	NC	NC	AD[0]	NC	GND
25	NC	NC	NC	3,3V	NC	GND

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2.3.3 Test and Program Development

2.3.3.1 JTAG/ISP Interface and Pinout

A JTAG/ISP interface is provided on the CP381 for the manufacturer's use (logic programming, JTAG test). This is a SAMTEC 10-pin, male, dual row connector (0.050" pin pitch).

Figure 2-4: JTAG Connector (CON3)

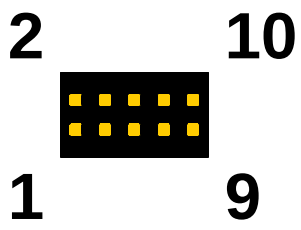


Table 2-3: JTAG Connector (CON3) Pinout

SIGNAL	PIN	PIN	SIGNAL
TCK	1	2	GND
TDO	3	4	3.3V
TMS	5	6	NC
NC	7	8	NC
TDI	9	10	GND

2.4 CapROM EEPROM

The CapROM is a 4 kBit (512 byte) EEPROM which provides the capability to store board control relevant information to allow software configuration of the CP381.

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2.5 Monitor and Control (M/C)

Monitor and Control functions are divided essentially into Pre-operation and Operation. Pre-operation M/C deals with board configuration and system requirements. Operation M/C covers direct operator interfaces.

2.5.1 Pre-Operation M/C

Pre-operation M/C is a direct function of the application and the system requirements. These requirements dictate the digital input configuration as well as the overall system integration. Digital input configuration is addressed in detail in chapters 4 and 5. These chapters provide detailed information concerning input signal conditioning and environmental aspects which relate to the operation and performance of the CP381. Overall system integration and compliance with its requirements is beyond the scope of this manual.

2.5.2 Operation M/C

The front panel of the board is equipped with two green LED's whose status combinations provide information for the operator on the operational status of the boards. The following tables describe the LED status combinations and the meanings of the modes

Table 2-4: System Status Indicators

LED	State	Description
Run	ON	The different LED status combinations have the following meanings: Run / Hit / Description Off / Off / Board is disabled On / Off / Board is enabled and the modes ("Event-hit", "Compare-hit" and "Latch-hit") are disabled or no hit has occurred. Off / On / Board is enabled and "Latch-hit" mode is enabled; a defined event has occurred and the input will be captured. On / On / Board is enabled and an "Event-hit" or "Compare-hit" is detected, but not a "Latch-hit".
	OFF	
Hit	ON	
	OFF	

Table 2-5: Function Modes of the CP381

Mode	Description
Event hit	The CP381 monitors the input ports and detects any change in their state: - Whenever individual input channels are enabled they are monitored. - The direction of the change-of-state may be set. - A status register reports the detected events.
Latch hit	In addition to standard event detection (i.e. event-hit) there is a latch mode extension. This mode is used in the event that it is necessary to capture the inputs when a defined event has occurred.
Compare hit	It is possible to detect a complete input pattern automatically. The input vector is continuously compared with the content of the mask register. Single inputs may also be individually masked out.

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Chapter 3

Installation

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3. Installation

The CP381 has been designed for easy installation. However, the following standard precautions, installation procedures and general information must be observed to ensure proper installation and to preclude damage to the board or injury to personnel.

3.1 Hardware Installation

The product described in this manual can be installed in any available 3U slot of a CompactPCI system except for the system master slot.

3.1.1 Safety Requirements

The board must be securely fastened to the chassis using the two front panel retaining screws located at the top and bottom of the board to ensure proper grounding and to avoid loosening caused by vibration or shock.

In addition the following electrical hazard precautions must be observed.



Caution, Electric Shock Hazard!

Ensure that the system main power is removed prior to installing or removing this board. Ensure that there are no other external voltages or signals being applied to this board or other boards within the system. Failure to comply with the above could endanger your life or health and may cause damage to this board or other system components including process-side signal conditioning equipment.



ESD Equipment!

This PEP board contains electrostatically sensitive devices. Please observe the following precautions to avoid damage to your board:

Discharge your clothing before touching the assembly. Tools must be discharged before use.

Do not touch any on board components, connector pins, or board conductive circuits.

If working at an anti-static workbench with professional discharging equipment, ensure compliance with its usage when handling this product.

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3.1.2 Installation Procedures

To install the board proceed as follows:

1. Ensure that the safety requirements indicated above are observed.



Warning!

Failure to comply with the instruction below may cause damage to the board or result in improper system operation. Please refer to chapters 4 and 5 for configuration information.

2. Ensure that the board is properly configured for operation before installing.



Note...

Care must be taken when applying the procedures below to ensure that when the board is inserted it is not damaged through contact with other boards in the system.

3. To install the board perform the following:
   1. Prior to installation of the board disengage the insertion/extraction handle by first unlocking the handle and pressing it down.
   2. Insert the board into an appropriate slot, and, using the insertion/extraction handle, ensure that it is properly seated in the backplane. (Front panel is flush with the rack front; the insertion/extraction handle is locked.)
4. Fasten the front panel retaining screws.



Warning!

Proper and safe operation of the CP381 Digital Input Controller depends on the correct configuration of input signals and signal conditioning. System integrators must ensure that all signals presented to the CP381 comply with the specifications set forth in this manual.

Failure to comply with the above may cause damage to the board or result in improper system operation. Please refer to chapters 4 and 5 for configuration information.

5. Connect external interfacing cables to the board as required.
6. Ensure that the interfacing cables are properly secured.

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3.1.3 Removal Procedures

To remove the board proceed as follows:

1. Ensure that the safety requirements indicated above are observed.



Warning!

Care must be taken when applying the procedures below to ensure that when the board is removed it is not damaged through contact with other boards in the system.

2. Disconnect any interfacing cables that may be connected to the board.
3. Loosen both of the front panel retaining screws.
4. To remove the board from the backplane perform the following:
    1. Unlock the insertion/extraction handle by pressing down on the grey locking mechanism in the middle of the handle. (This should be achievable with a minimum of force. If necessary lift the handle up slightly while pressing down on the grey locking mechanism.)
    2. Disengage the board from the backplane by pressing down on the insertion/extraction handle and pull the board out of the slot ensuring that the board does not make contact with adjacent boards. (If the handle does not move, it is not unlocked. Repeat the unlocking procedure above and try again. Do not use force!)

3.2 Software Installation

Installation of the CP381 driver software is a function of the application operating system. For further information refer to the appropriate software documentation.

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Chapter 4

Configuration

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4. Configuration

This chapter provides information for configuring the CP381 board for operation.

4.1 Jumper Settings

The CP381 does not have any jumpers which require configuring.

4.2 Digital Input Signal Requirements.

In addition to the input signal type and its range, which have been specified in chapter 1, paragraph 1.3.1, system integrators must be aware of certain input configuration requirements for the CP381. The following paragraphs provide some information regarding individual connection configuration requirements.

4.2.1 Channels

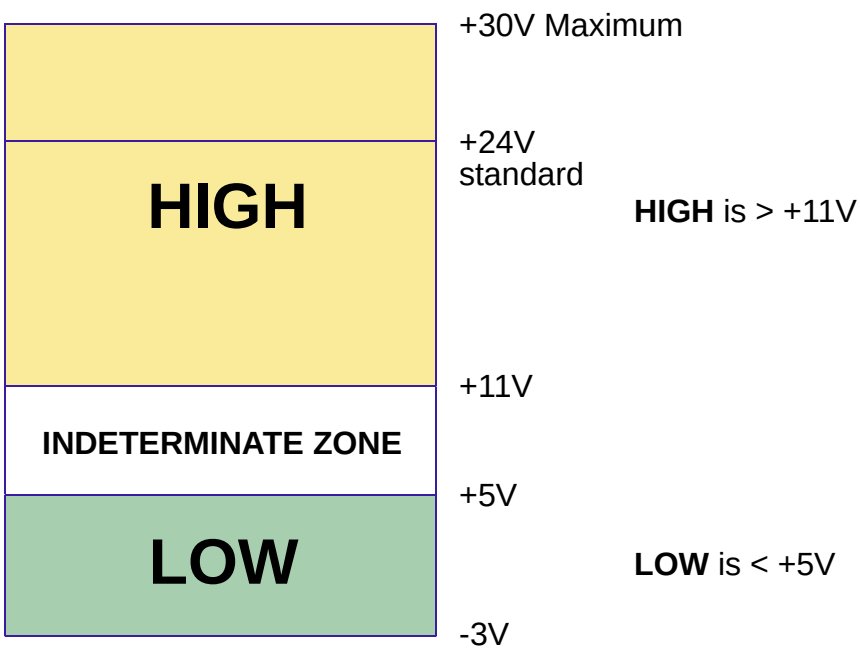
The CON2 connector of the CP381 is designed so that there are two input pins per channel. This allows each channel to be configured separately as required. This is illustrated in Figure 2-2, which shows the front panel connector pinout, with the 30 channels shown starting at the top of the connector with channel 0.

The following sections address the basic requirements.

4.2.2 Signal Characteristics

The signals are single-ended and the specified voltage ranges illustrated in the following table should be observed.

Figure 4-1: Voltage Ranges



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4.2.3 Channel Configuration

Signals require to be connected: plus to plus, minus to ground as shown in figure 4-2 below

Figure 4-2: Input Configuration (Example for Channel 0)

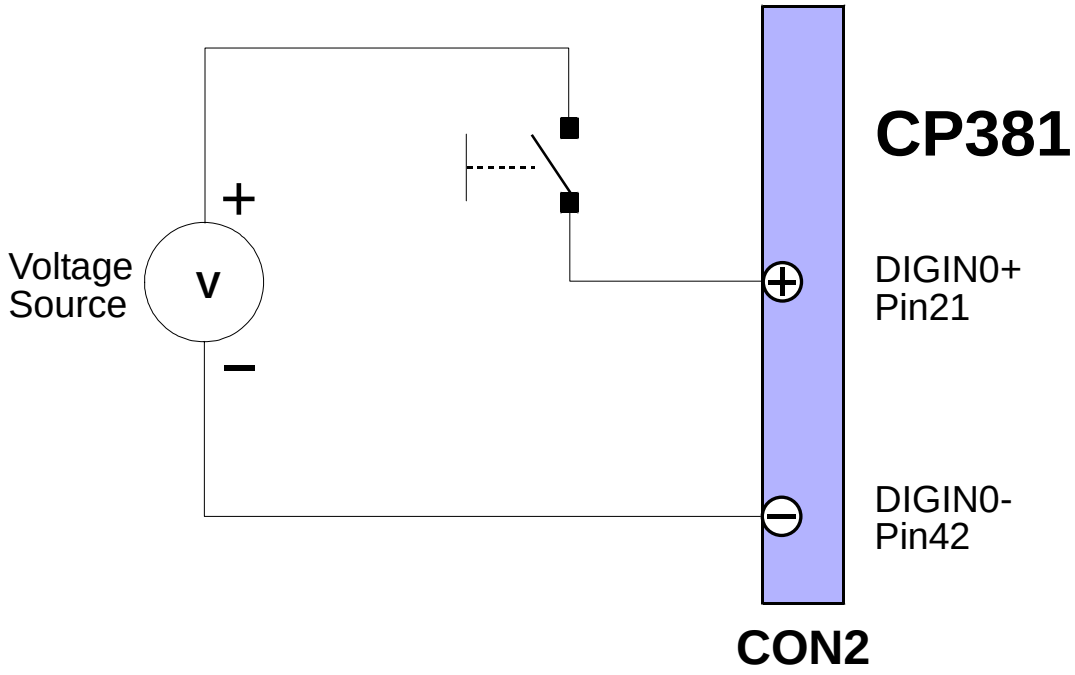
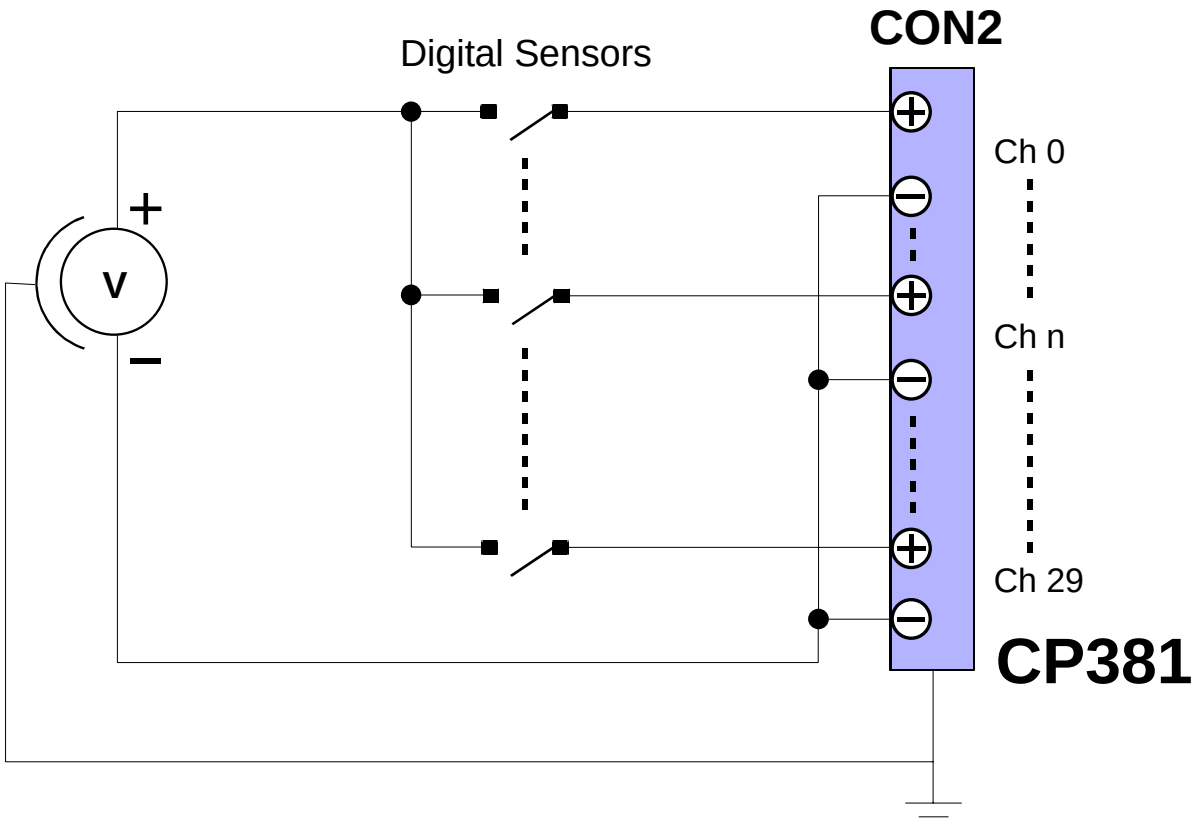
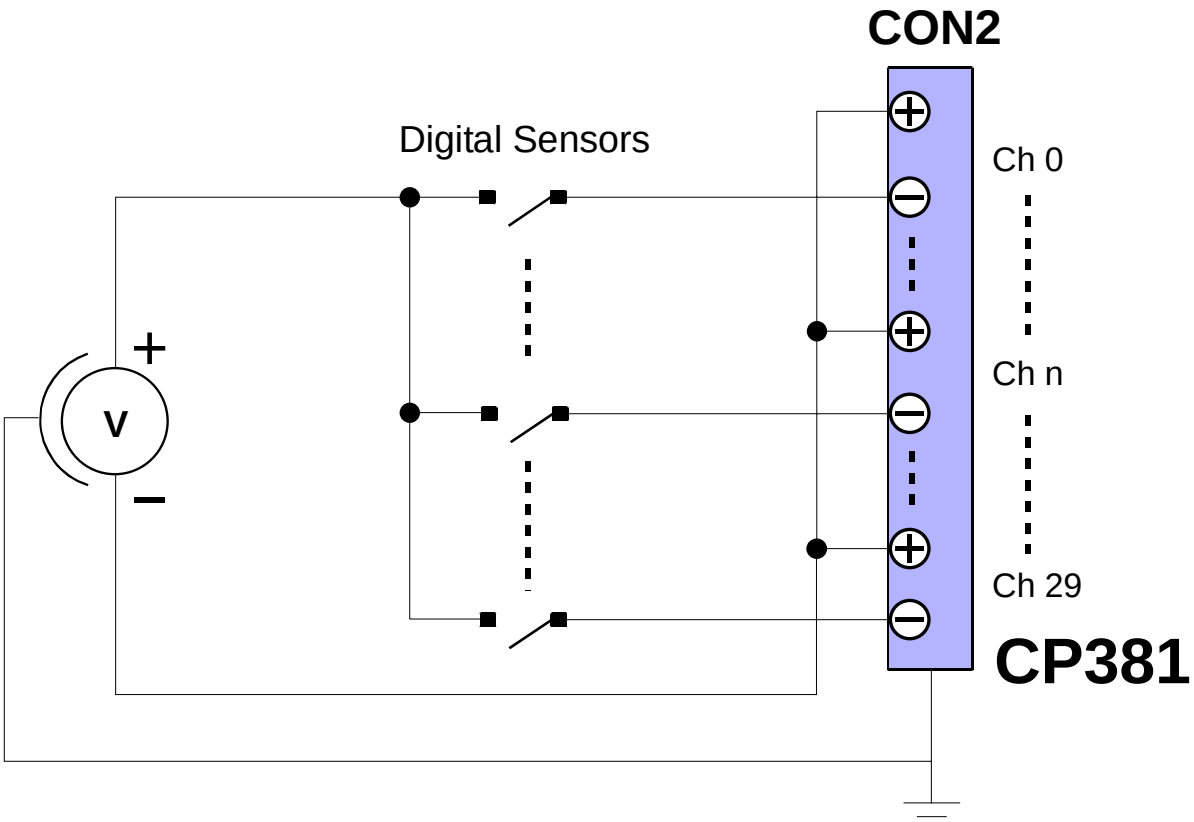


Figure 4-3: Configuration Diagram for All Channels



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Figure 4-4: Configuration Diagram for All Channels



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4.3 Programming Interface

4.3.1 Access Control Logic (Address Decoder)

All the resources of the CP381 are mapped within the 64 kB PCI memory address space which itself is set in the PCI configuration register BAR0. The port size of all local or backend registers is 32-bit by default. The address map of the registers is as follows.

Table 4-1: Backend Register Address Map

Base Address	Size	Function
bar0 + 0x0000	4 K	Common Board Registers
0x0400	32 bit	g_irq General Interrupt Enable Register
0x0800	32 bit	hsr Hardware Status Register
0x0804	32 bit	i_pen General Interrupt Pending Register
0x0c00	32 bit	hdr Hardware Debug Register
bar0 + 0x1000	4 K	Capability ROM, serial EEPROM
0x1000	32 bit	r_cmd Command Register
0x1400	32 bit	r_ctl Control Register
0x1800	32 bit	r_sta Status Register
0x1c00	32 bit	r_dat Data Register
bar0 + 0x2000	2 K	Input Control
0x2400	32 bit	i_ctl Input Control Register
0x2408	32 bit	i_irqen Input Irq Enable Register
0x240c	32 bit	e_pol Input Event Polarity Register
0x2410	32 bit	e_msk Input Event Mask Register
0x2414	32 bit	e_len Input Latch-on-Event Register
0x2418	32 bit	c_cmp Input Pattern Compare Register
0x241c	32 bit	c_msk Input Pattern Mask Register
bar0 + 0x2800	1 K	Input Status
0x2800	32 bit	i_event, Input Status Register
bar0 + 0x2c00	1 K	Input Data
0x2c00	32 bit	d_in, Input Data Register
0x2c04	32 bit	input, Transparent Input Data
bar0 + 0x3000 – 0xffff	52 K	Reserved

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4.3.2 Reading Input Data

The input ports are made visible via the Input Data Register. This register reflects the inputs after them having passed the digital programmable debouncer. An active input appears there as a logical "1" whereas an open or inactive input port appears as a logical "0". The bit ordering naturally corresponds with the numbering of the input ports at the connector.

Table 4-2: Input Data Register Bit Map

Bits	Type	Default	Function
31-30	r	0	Reserved
29-0	r	-	Input (debounced)



Note...

Where the enhanced features such as interrupts, pattern or event detection are not required, only the input data register is relevant.

Table 4-3: Transparent Input Data Register Bit Map

Bits	Type	Default	Function
31-30	r	0	Reserved
29-0	r	-	Input (transparent)



Note...

In addition to the Input Data Register, there is a second non-latched input register (debouncer bypassed).

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4.3.3 Debouncing Inputs

By default, all inputs are filtered through a passive analog low-pass filter placed immediately behind the input connector. Additionally, the CP381 provides a programmable digital debouncer which is common for all inputs. It functions as follows; the input ports are sampled at a programmable sample rate which is derived from PCI bus clock. Two consecutive samples must be equal before being stored in the input data register. By this means, bouncing and spikes on inputs can be filtered out. For example, with a selected input sample rate of 500 Hz, input pulses which are shorter than 2 ms are filtered out.

Table 4-4: Input Control Register

Bits	Type	Default	Function
31-8	r/w	0	Reserved
7	r/w	0	Input enable
6	r/w	0	Event detect enable
5	r/w	0	Latch mode enable
4	r/w	0	Pattern detect enable
2-0	r/w	000	Debounce control deb[2..0]



Note...

The Inputs are sampled through the debouncer after the Input Enable bit is set. Additional features such as event and pattern detection and latch mode are also enabled in the input control register, after being configured within the corresponding mode registers.

Table 4-5: Programmable Input Sample Rates

deb[2..0]	Clock Divider	Input Sample clock @ 33MHz PCI	Input Sample period @ 33MHz PCI
000	1	33 MHz	30 ns
001	2^8	128 KHz	8 us
010	2^10	32 KHz	32 us
011	2^12	8 KHz	128 us
100	2^14	2 KHz	0.5 ms
101	2^16	0.5 KHz	2 ms
110	2^18	125 Hz	8 ms
111	2^20	31 Hz	32 ms



****Note...***

The clock divider default value is 1. In addition to the choice of debouncing filters, there is an analog filter implemented on board with an edge frequency at 10 kHz.

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4.3.4 Detecting Input Events

Detecting events on input means that the CP381 hardware can supervise the input ports upon their changing state and without being continuously polled. This mode is controlled by three control registers. In the Input Event Mask Register, individual input events can be enabled which should be monitored. In the Input Polarity Register the direction of the change-of-state is set. Detected events are reported in the corresponding Input Event Status Register.

Table 4-6: Input Event Mask Register, Bit Map

Bits	Type	Default	Function
31-30	r/w	0	Not used
29 - 0	r/w	1	Input event mask bits



Note...

A set bit means that event detection is disabled for the corresponding input port.

Table 4-7: Input Event Polarity Register, Bit Map

Bits	Type	Default	Function
31-30	r/w	0	Not used
29 - 0	r/w	0	Input event polarity bits



Note...

A bit setting of 0 bit means that an event is detected when the input port changes from 0 to 1 whereas a setting of 1 means that an event is detected when the input changes from 1 to 0.

Table 4-8: Input Status Register, Bit Map

Bits	Type	Default	Function
31	r/w	0	Input latch-on-event status flag
30	r/w	0	Input compare status flag
29 - 0	r/w	0	Input event status flags



Note...

A set bit means that an event was detected on the corresponding input port. Events must be cleared by writing a "1" to the corresponding input event flag. Otherwise, consecutive events on the same input would no longer be detected.

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4.3.5 Latching on Input Events

In addition to the standard event detection described above, there is a latch mode extension. This mode is used in cases where it is necessary to capture the inputs when one of the defined events occurs.

Table 4-9: Input Latch-on-Event Register, Bit Map

Bits	Type	Default	Function
31-30	r	0	Not used
29 – 0	r	0	Latch on event, enable bits to activate



Note...

A set bit means that a detected event on the corresponding input is latched. If all bits are enabled all inputs are latched immediately. To switch back from latch mode into active mode all detected events and the input latch-on-event status flag have to be reset by writing "1" to the corrresponding bits in the Input Status Register.

4.3.6 Comparing Input Patterns

In addition to the Event Detection Mode it is also possible to detect a complete input pattern automatically. In this mode the input vector is continuously compared with the content of the Input Pattern Compare Register. In the case of a match a flag is set within the Input Status Register. Single inputs can also be masked out individually in the Input Pattern Mask Register.

Table 4-10: Input Pattern Mask Register, Bit Map

Bits	Type	Default	Function
31-30	r/w	0	Not used
29 - 0	r/w	1	Input event mask bits



Note...

A set bit means that the corresponding input is masked out for pattern recognition. There is no special enable for pattern recognition since it is switched off by default as long as all mask bits are set.

Table 4-11: Input Pattern Compare Register, Bit Map

Bits	Type	Default	Function
31-30	r/w	0	Not used
29 - 0	r/w	1	Input pattern compare bits



Note...

This register stores the input compare data. A compare match is reported within the Input Status Register (Bit 31). To reset a compare match, the status flag has to be reset by writing "1" to it and also the match condition must cease.

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4.3.7 Hardware Debug/Test Registers

These registers are for internal test and debug only. The Common Status Register contains Logic-Version and PCB -Version. The Common Control Register is a read/write register without any further functionality. Neither of these registers should be used by standard software.

Table 4-12: Hardware Debug Register Bit Map

Bits	Type	Default	Function
31-0	r/w	0	Used for test purposes

Table 4-13: Hardware Status Register Bit Map

Bits	Type	Default*	Function
31-16	r	0	Reserved
15-8	r	00	HW Version (PCB Index)
7-0	r	01	Logic Version



Note...

The HW version starts with 0, the Logic version starts with 1. At each further release it will be incremented by 1.

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4.3.8 Generating Interrupts

Any detected event or, more clearly, any event flag set in the Input Status Register can trigger an interrupt. Thus, any input can be enabled individually for interrupt generation.

Regardless of the cause of the interrupt, a board interrupt is always handled on the hardware level in the same way, as follows; after having set the input control registers where compare data and events are defined, interrupts can be enabled individually within the Input IRQ Enable Register. The final step is to enable the board interrupt in the General Interrupt Enable Register. Within the interrupt service routine interrupts should be handled as follows.

1. Check if the board is the cause of the interrupt (General Interrupt Pending is set)
2. If yes, check the reason for the interrupt by reading the input status register
3. Reset the corresponding Input Event Flag by writing a 1 to a set status bit.
4. Reset the boards' IRQ by resetting the General Interrupt Pending Bit by writing a 1 to that status bit
5. Return from Interrupt

Table 4-14: General Interrupt Enable Register, Bit Map

Bits	Type	Default	Function
31	r/w	0	Board Interrupt Enable
30 - 0	r/w	0	Reserved



Note...

The board will continue issuing an interrupt until all interrupt sources are completely dealt with and no interrupt condition remains.

A set bit means that the boards' interrupt is enabled.

Table 4-15: General Interrupt Pending Register, Bit Map

Bits	Type	Default	Function
31	r/w	0	Board Interrupt Pending
30 - 0	r/w	0	Reserved



Note...

A set bit means that the boards' interrupt is pending. A board interrupt must be cleared by writing a "1" to the corresponding input event flag.

Table 4-16: Input IRQ Enable Register, Bit Map

Bits	Type	Default	Function
31	r/w	0	Not used
30	r/w	0	Input compare interrupt enable
29 - 0	r/w	0	Input event interrupt enable

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4.3.9 Programming the Board Capability ROM

The Board Capability ROM contains all the board data necessary to identify board, version, optional features, etc., and to setup the basic software. The BCR is implemented using a 4 KBit serial EEPROM of the type Microchip 93LC66.

(The contents list of the BCR is not described here.)

The serial interface of the device has been realized in hardware resulting in a very simple register based programming interface with command, control, status and data registers. All protocol and serial timing specifications are resolved by hardware.

Programming of the BCR is undertaken as follows: The control word is written into the ROM Control Register including command opcode and internal address. Then optional data (in case of Write action) is written into the ROM Data Register. Command execution is started by setting the Startbit in the ROM Command Register. Then Ready/Busy must be polled in the ROM Status Register. After reaching Ready status, the next command can be set up and data (in case of Read action) can be fetched from the ROM Data Register.

Table 4-17: ROM Command Register Bit Map

Bits	Type	Default	Function
31	r/w	0	Startbit
30-0	r/w	00	Reserved



Note...

The Startbit will be automatically reset as soon as an action is completed.

Table 4-18: ROM Control Register Bit Map

Bits	Type	Default	Function
31-18	r/w	0	Reserved
17-16	r/w	00	Opcode
15-9	r/w	00	Reserved
8-0	r/w	00	Internal address (A8..A0)



Note...

The commands READ, EWEN (Write Enable) and WRITE are sufficient for all purposes.

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Table 4-19: Opcodes and Commands

Opcode	A8..A0	Command
00	11xxxxxxx	EWEN
10	xxxxxxxxx	READ
01	xxxxxxxxx	WRITE



Note...

The EWEN (Erase and Write Enable) command must be executed once before the first write.

Table 4-20: ROM Status Register Bit Map

Bits	Type	Default	Function
31	r/w	0	Busy/Ready
30-0	r/w	00	Reserved



Note...

As soon as the Startbit is set the Busy/Ready bit becomes active (Busy=1). It remains set as long as the command is executed and is reset when command execution is complete.

Table 4-21: ROM Data Register Bit Map

Bits	Type	Default	Function
31-8	r/w	0	Reserved
7-0	r/w	0	Data (for data read and write commands)

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Chapter 5

System Considerations

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5. System Considerations

5.1 Introduction

In addition to the basic specification requirements for signals being presented to the CP381 which have been addressed in chapter 4, system integrators need to be aware of the overall system environment and the application needs when designing the interfacing to the CP381. The following chapters address a number of more apparent considerations which should be addressed but certainly not all of the possible situations which may be encountered. Many of the considerations presented here are recommendations, but some are definite requirements if the CP381 is to successfully achieve its purpose.

5.2 General

Considerations:

1. Care must be taken to ensure that proper grounding concepts are followed, and that the integrity of the grounding system within the application be maintained.
2. Input wire routing should avoid proximity to high voltage or current sources.
3. Where possible input wiring length should be kept as short as possible.

5.3 Shielding

Considerations:

1. Input cable shielding in general is recommended.
2. The requirements for shielding can be seen primarily as a function of the system design and environment, but empirical results must also be considered.
3. The CON2 connector has a metal housing which is connected to the CP381 shield and is isolated from the system ground.
4. Ensure that if shielding is used that it is not in anyway connected to the system ground.

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5.4 Debouncing

On the CP381 it is possible to select from a number of debouncing times, dependant on the type of switches/sensors in use. For example, when using mechanical switches or relays to switch the input, bouncing will always occur and therefore debouncing is necessary. A debounce period may be selected from a range of values available, accessible via software in the register depending on the settle time. Where it is known that an application does not generate bouncing problems, the debounce period may be set to the default value.

Table 5-1: Debouncing Periods

Clock Divider	Input Sample Clock @ 33 MHz PCI CLK	Input Sample Period @ 33 MHz PCI CLK
1 (default value - see note below)	33 MHz	30 ns
2^8	128 kHz	8 us
2^10	32 kHz	32 us
2^12	8 kHz	128 us
2^14	2 kHz	0.5 ms
2^16	0.5 kHz	2 ms
2^18	125 Hz	8 ms
2^20	31 Hz	32 ms



Note...

The clock divider default value is 1. In addition to the choice of debouncing filters, there is an analog filter implemented on board with an edge frequency at 10 kHz.

5.5 Process-side Signal Conditioning

Considerations:

1. Input signals presented to the CP381 must be within the ranges specified for signals in chapter 1.3.1 or erroneous results will occur as well as possible damage to the CP381.

5.6 Cable Interfacing

Considerations:

1. No modification to the CP381 itself is permitted.
2. If necessary, cabling to the CP381 CON2 connector should be physically fixed to prevent strain on the CON2 connector.

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