Modular Computers®

CP382

24 Channel CompactPCI
Digital Output Controller

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The product described in this manual is in compliance with all applied CE standards.

Revision History

Manual/Product Title:	CP382		
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Rev. Index	Brief Description of Changes	Board Index	Date of Issue
01	Initial Issue	00	Mar. 2002

Imprint

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CE Conformity

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Caution, Electric Shock!

This symbol and title warn of hazards due to electrical shocks (> 60V) when touching products or parts of them. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your material.

Please refer also to the section “High Voltage Safety Instructions” on the following page.



Warning, ESD Sensitive Device!

This symbol and title inform that electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Please read also the section “Special Handling and Unpacking Instructions” on the following page.



Warning!

This symbol and title emphasize points which, if not fully understood and taken into consideration by the reader, may endanger your health and/or result in damage to your material.



Note...

This symbol and title emphasize aspects the reader should read through carefully for his or her own advantage.

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For Your Safety

Your new *PEP* product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new *PEP* product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions



Warning!

All operations on this device must be carried out by sufficiently skilled personnel only.



Caution, Electric Shock!

Before installing your new PEP product into a system always ensure that your mains power is switched off. This applies also to the installation of piggybacks.

Serious electrical shock hazards can exist during all installation, repair and maintenance operations with this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing work.

Special Handling and Unpacking Instructions



ESD Sensitive Device!

Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory back-up, ensure that the board is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the board.

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This device should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This applies also to the operational temperature range of the specific board version, which must not be exceeded. If batteries are present their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, please follow only the instructions supplied by the present manual.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the board please re-pack it as nearly as possible in the manner in which it was delivered.

Special care is necessary when handling or unpacking the product. Please, consult the special handling and unpacking instruction on the previous page of this manual.

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Chapter 1

Introduction

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1. Introduction

1.1 Product Overview

The CP382 digital output controller has been designed to provide a large number of automatically controlled, flexible digital outputs within a ruggedised board equipped with features for electrical protection. The flexibility is due to the fact that the 24 channels provided are organised into 3 separate clusters of 8 channels each, allowing the user to configure up to 3 different voltages as required. Reliability is assured by features which include overtemperature thermal shutdown, overcurrent and undervoltage protection. Use of the widely available D-sub 62 front panel connector means that the board may be used in a broad range of application fields. On the software side the board may be used with all major operating systems.

This product is part of a comprehensive concept whose goal is to provide CompactPCI system integrators with a complete range of I/O products which include the functions of analog input, analog output, digital input and digital output implemented as separate integral boards. This concept ensures the maximum degree of system design flexibility thus allowing for the efficient and effective usage of available resources..

Table 1-1: CP382 Main Features

FEATURE	DESCRIPTION
Channels	24 digital output channels in 3 independent groups of 8 channels each. Each group may be set to operate at different voltages for different loads within the prescribed output voltage limits.
Protective Features	The design of the board incorporates a range of protective features including the following: Signal Output Overcurrent Protection Input Voltage Undervoltage Protection Overtemperature Protection Isolation: system side protected by optocouplers *Details of these protective features are provided in table 1-4, Digital Output Specifications*
External Interfaces	2 external interfaces, the digital output interface connector CON2 on the front panel and a single CompactPCI connector at the rear. The digital output interface connector supports up to 24 digital output channels. The connector pins are subdivided into 3 clusters or groups which are independent from each other and can operate at different voltages to meet the requirements of different loads. The CompactPCI connector is the standard CPCI type connector for J1
Indicators	One green LED (Run) and one red LED (Fail), which are user configurable
Temperature Range	The board is qualified to operate over a wide range of temperatures as follows: Operational: 0ºC to +70ºC Standard -40ºC to +85ºC E2 Storage: -55ºC to +125ºC

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1.2 Board Overview

1.2.1 Board Introduction

The CP382 is a digital output board which provides twenty-four output channels grouped into three clusters of eight channels each. The major components involved are the front end High Side Driver switches (HSD = High Side Driver switch), output signal optoisolation, and the Digital Output Process and Communications (DO ProComm) controller which is realized within a Field-Programmable Gate Array (FPGA). The DO ProComm Controller is designed for effective and efficient control of the digital output signals as well as providing interfacing with the CPCI system controller.

Digital output requests from the System Controller are processed accordingly by the DO ProComm controller and are then routed to the HSD's which in turn create the actual digital output utilizing the external supply voltage as the power source.

An external reset input is provided to simultaneously switch off all the outputs per cluster and sets all the High Side Driver Switches to open. Each cluster has its own separate reset signal input.

This reset can be used by the application to keep the inputs low after a fault condition.

1.2.2 Board Specific Information

Specific board components involved in the digital output process:

- One front panel connector (62-pin, female, D-sub type)
- 6 HSD switches (4 channels per switch, 2 switches per cluster)
- Optoisolation for each output channel
- One FPGA (the DO ProComm controller)
- One CompactPCI bus connector (J1, board to backplane, 132-pin, female, six row)
- One EEPROM (CapROM)

1.3 System Relevant Information

The following system relevant information is general in nature but should still be considered when developing applications using the CP382.

Table 1-2: System Relevant Information

SUBJECT	INFORMATION
System Configuration	The CP382 operates with a system clock frequency of 33 MHz. The maximum number of CP382's which may be installed in any one system depends on the system configuration.
Master/Slave Functionality	The CP382 functions only as a slave. As such it requires a system master for servicing.
System Controller	The CP382 cannot function as a system controller.
Voltage Source	The voltage source for the CP382 must conform with the specifications set forth in this manual.

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1.3.1 System Configuration

The external supply voltage (VCC) used as the output voltage on the CP382, must be within the specified supply voltage range. In addition, it should be a DC supply with good ripple and noise characteristics. Please refer to chapters 4 and 5 for further information.

1.3.2 Driver Software

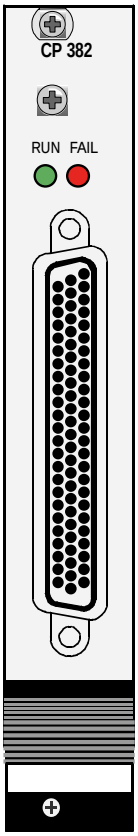
The CP382 is supplied with appropriate driver software which provides software interfacing with the system master.

1.4 Board Diagrams

The following diagrams illustrate board functionality and component layout.

1.4.1 Front Panel

Figure 1-1: CP382 Front Panel

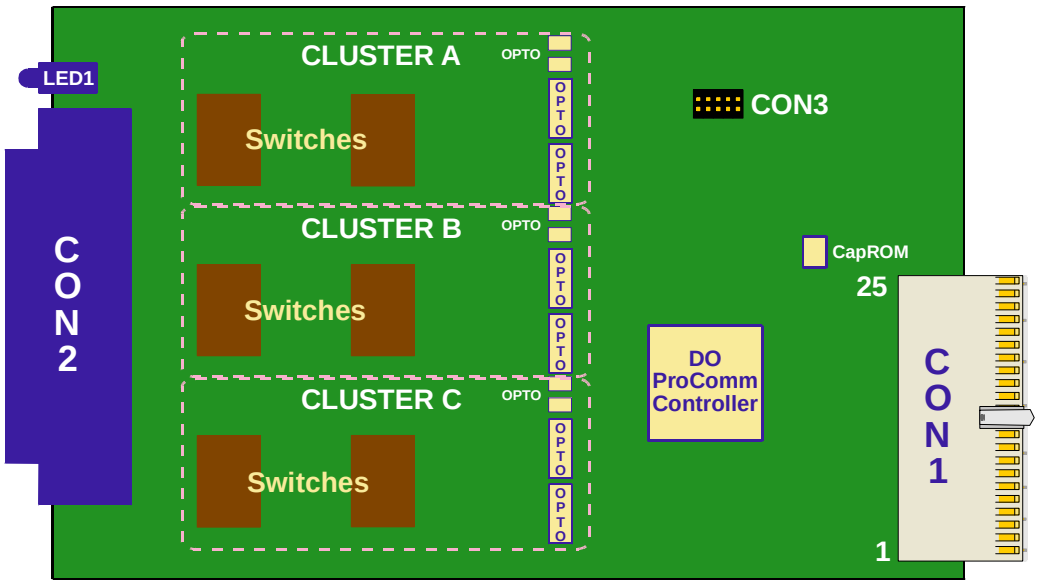


A green “Run” LED and a red “Fail” LED have been placed on the front panel, to cater for the most likely use of these LED’s. However, they are user configurable and may be employed for user defined purposes.

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1.4.2 Board Layout

Figure 1-2: CP382 Board (Front View)



NOTE

CON3 is a test connector for manufacturer's use only

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1.5 Technical Specifications

Table 1-3: CP382 Main Specifications

GROUP/ INTERFACE	TYPE	DESCRIPTION
DO ProComm Controller and Related	FPGA Logic Device	Provides CompactPCI interfacing and IO control logic
Peripheral Memory	CapROM	4 kBit (512 byte) EEPROM
CompactPCI Interface ***(See note at foot of table)***	Realized on 132-pin, female, six row connector (standard CPCI type connector for J1)	Bus Width: 32-bit, Bus Speed: 33 MHz 64 kB memory space, non-prefetchable PCI Header: Device ID: 0x5555 Vendor ID: 0x1556 Class Code: 0x110000 Subsystem Device ID: 0x00F0 Subsystem Vendor ID: 0x1518
Digital Output Interface	One 62-pin, female, three row, D-sub connector	Supports up to 24 digital output channels
Indicators	Front Panel LED's	One green and one red LED to indicate operational status
General	Form Factor	3U, 4HP
	Mechanical	Conforms with IEEE 1101.1
	System Power Consumption	+ 3.3V: maximum 860 mW (all 24 channels activated)
	Temperature Range	Operational: 0ºC to +70ºC Standard -40ºC to +85ºC E2 Storage: -55ºC to +125ºC
	Humidity	0% to 95% non-condensing
	Dimensions	100 mm x 160 mm single height Eurocard
	Board Weight	155 grams



Note...

The Device ID and Vendor ID refer to the chip manufacturer. In the Class Code value given, "11" relates to the data acquisition and signal processing controllers and "0000" relates to the DPIO modules. Subsystem Device ID and Subsystem Vendor ID are defined by *PEP*.

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Table 1-4: CP382 Digital Output Specifications

TYPE	DESCRIPTION
Output Voltage Range	Low state: =< +1.5 V High state: > +8.0 V and < +35 V Current per channel: max. 0.5 A Leakage current: 20 µA
Channels	24 channels grouped into three clusters of eight channels each
Channel Connections	1 pin per channel
External Reset	The output of each cluster has two means of being halted: • externally via the EXTRESET signal • internally on request from the application via the DO ProComm controller
External Voltage	+9.5 V to +35 V
Switch “On” Resistance	$R_{ds,on}$ = 1.8 Ohm
Max Output Frequency	2.5 kHz
System Switching Delay Time	$T_{d,on}$ = 4 µs, $T_{d,off}$ = 90 µs
Signal Output Overcurrent Protection	For output currents of greater than 0.8 A, the output will be switched to a failure mode: square wave signal with a maximum current amplitude of 0.4A and an on/off time (t_{on}, t_{off}) of 100 µs. This type of system failure indication is made available to the DO ProComm controller.
Undervoltage Protection for external power supply	For the voltage source (EXTVCC) <= +8.5V, the outputs are switched off This type of system failure indication is made available to the DO ProComm controller.
Overtemperature	If the case temperature of the High Side Driver switches exceeds 150°C the outputs are switched off This type of system failure indication is made available to the DO ProComm controller.
Isolation	2 kV process to system

1.6 Software Support

The CP382 is supplied with appropriate driver software which provides software interfacing to the system master. The CP382 supports Windows XP®, Windows NT 4.0®, VxWorks® and Linux.

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1.7 Applied Standards

The *PEP Modular Computers'* CompactPCI systems comply with the requirements of the following standards:

Table 1-5: Applied Standards

	TYPE	STANDARD
CE	Emission	EN50081-1
	Immunity, Industrial Environment	EN50082-2
	Immunity, IT Equipment	EN55024
	Electrical Safety	EN60950
MECHANICAL	Mechanical Dimensions	IEEE 1101.1
ENVIRONMENTAL TESTS	Vibration, Sinusoidal	IEC68-2-6
	Random Vibration, Broadband	IEC68-2-64 (3U boards)
	Permanent Shock	IEC68-2-29
	Single Shock	IEC68-2-27

1.8 Related Publications

Table 1-6: Related Publications

	ISSUED BY	DOCUMENT
CompactPCI Systems	PICMG	CompactPCI Specification, V. 2.0, Rev. 3.0
	PEP Modular Computers	CompactPCI Systems Manual (ID 19953)
CP382	ST Microelectronics	L6376 0.5A High-Side Driver Quad Intelligent Power Switch

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Chapter 2

Functional Description

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2. Functional Description

The following sections present more detailed, board level information about the CP382 Digital Output controller whereby the board components and their basic functionality are discussed in general.

2.1 General Information

The CP382 is comprised basically of the following:

- High Side Driver switches
- Optocouplers
- DO ProComm controller
  - Controls digital output and provides interfacing to the CompactPCI bus
- System interfaces for:
  - Front Panel
    - 24 channels of digital outputs
    - External supply connection for each cluster
    - External hardware reset for each cluster
    - One 62-pin, female, 3-pin row, D-sub connector (CON2)
  - CompactPCI bus
    - 132-pin, female, 6-pin row connector (CON1)
    - CompactPCI specification
- On board memory: Capability EEPROM (CapROM)
- Monitor and Control
  - Two operational status LED’s
  - External reset
  - Output failure indicators
- Software

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2.1.1 High Side Driver Switches

The High Side Driver switches (HSD switches) are able to drive inductive, capacitive or resistive loads. Diagnostic information for the system master and extensive use of electrical protection are among their main characteristics.

The HSD switches (type L6376 manufactured by SGS THOMSON) constitute the most important part of the front end. The L6376 switch realizes a QUAD intelligent power switch which adapts the digital output signals to the prevailing voltage and current levels and also provides corresponding mechanisms to protect against undervoltage, overcurrent and overtemperature.

The output voltage level is adapted to the external supply voltage for high level and for low level output voltage respectively via the integrated FET transistor output stage within the HSD switch. The HSD switch implements a clamp diode for inductive load driving.

The voltage source for the CP382 front end is implemented using an external voltage source (nominal +24V, also in the range +9.5V to +35V).

The input signals to the HSD switches are derived from the system side, directly from the outputs of the optocoupler devices.

2.1.2 Optoisolation

The process side is galvanically isolated from the system side. The process side of the board is separated from the system side by a bank of optocouplers which serve to protect the system side from any excess voltages or voltage spikes.

2.1.3 DO ProComm Controller

The DO ProComm controller is responsible for supervising and controlling the digital data output process and maintaining communication with the CompactPCI system master. Applications address the CP382 through its software driver interface within the system master whereby the controller accepts requests from the driver and executes them accordingly. Digital data from the system master is processed through the DO ProComm controller and then routed to the HSD switches.

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2.1.4 System Interfaces

The CP382 provides interfacing capability for the following system elements:

- Front Panel connector
- CompactPCI bus

Digital outputs, external voltage, and external reset are routed via the CON2 connector. Interfacing to the CompactPCI bus is accomplished via the CON1 connector. Test and program development is supported by the CON3 connector.

External supply each Cluster:

The connection for the external supply (+24V DC [9.5V to 35V] each cluster) is realized by reserved/ defined pins within each cluster at the front panel connector CON2.



Important...

In addition to supplying the current for the logic parts of the power switches which are linked to the digital outputs, the external voltage supplies also have to supply the current for the 8 digital output loads per cluster.

External reset for each cluster:

The digital outputs will be brought to zero output level on power-up. In addition to the reset by software, the reset-lines (one each cluster) are routed to the front panel.

2.1.5 Monitor and Control

Various monitor and control functions are available for the operation of the CP382. Two LED's are available for operator interaction. There are also system failure indicators available. In addition, applications have access via the System Master driver software to board specific registers.

2.1.6 Software

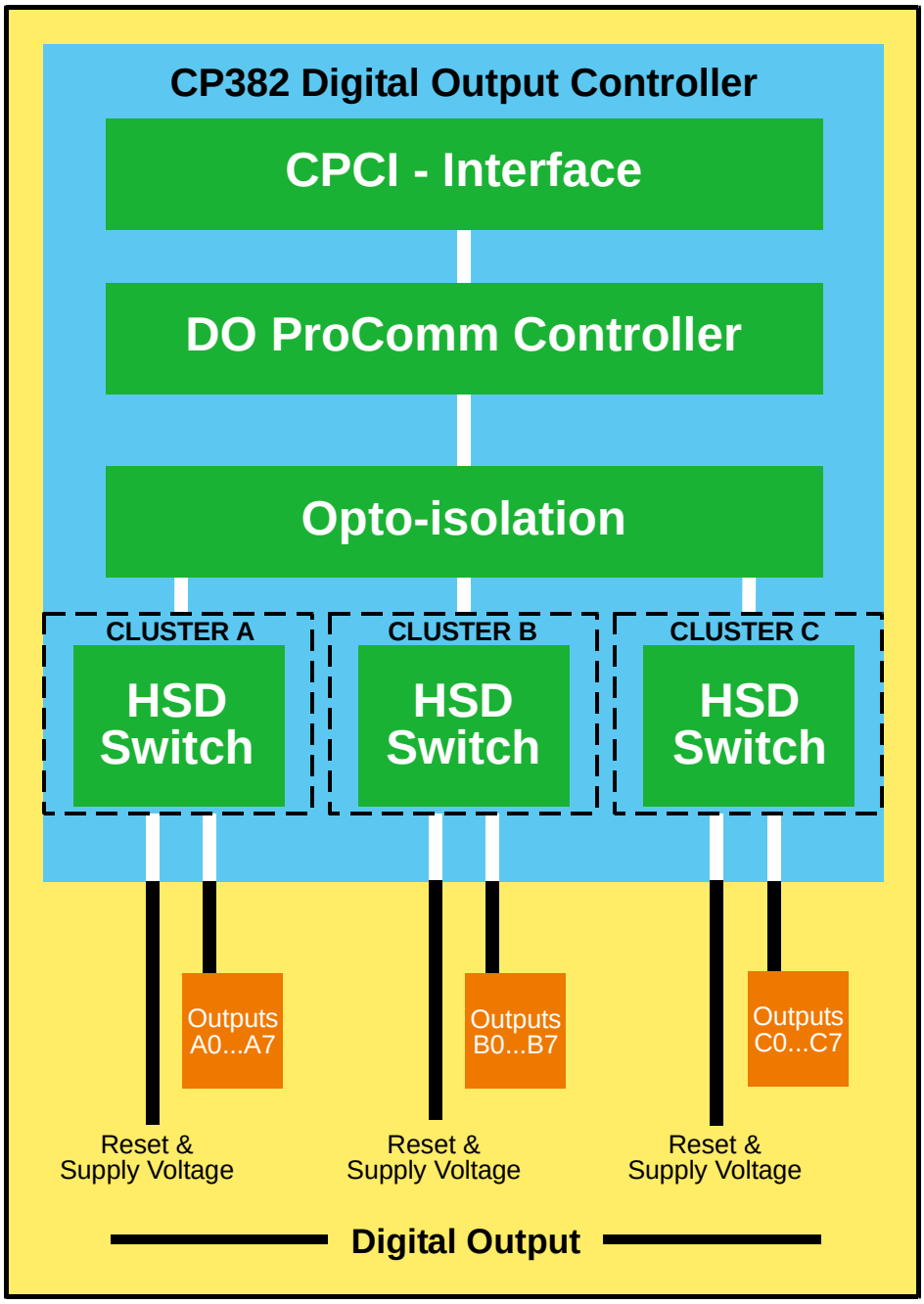
Driver software is available for the System Master application software.

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2.2 Board Level Interfacing Diagram

The following figure demonstrates the interfacing structure between the internal processing modules of the CP382 and other major CP382 system components. Where CP382 system elements have common interfacing they are grouped into a block. Interfacing common to only one element of a block is indicated with a direct connecting line. The interfacing lines are shown in white where they are onboard and in black for board external interfacing.

Figure 2-1: CP382 Board Level Interfacing



NOTE

HSD = High Side Driver switch

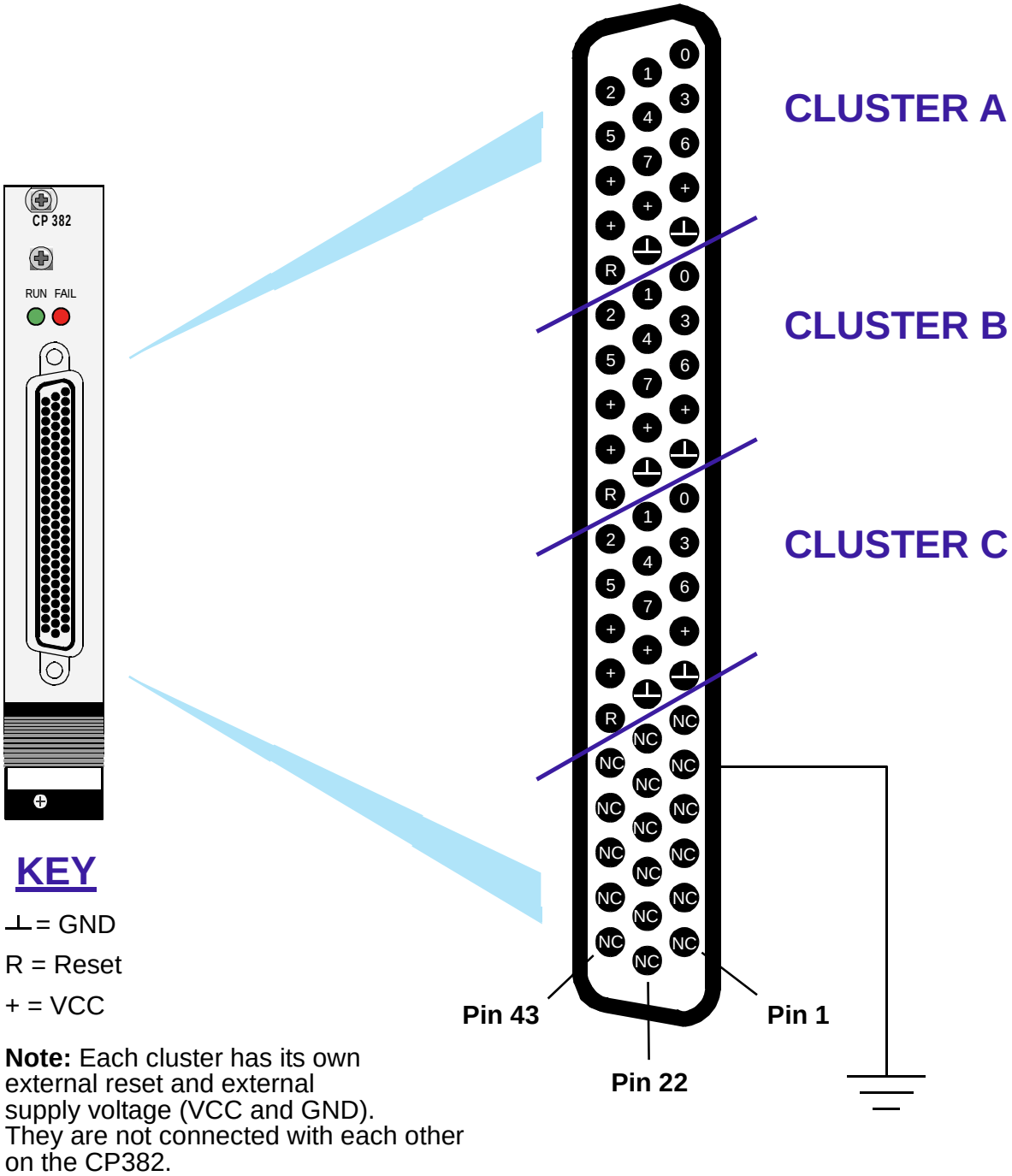
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2.3 System Interfaces

2.3.1 Digital Output Interface

The digital output interface is routed through the CON2 connector. The following figure and table indicate the pin layout and pinout of this connector.

Figure 2-2: Pin Layout of the Digital Output Interface Connector CON2



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Table 2-1: Pinout of the Digital Output Interface Connector CON2

CLUSTER	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
	1	NC	22	NC		
	2	NC	23	NC	43	NC
	3	NC	24	NC	44	NC
	4	NC	25	NC	45	NC
	5	NC	26	NC	46	NC
	6	NC	27	NC	47	NC
CLUSTER C	7	EXTGND_C	28	EXTGND_C	48	EXTRESET_C
	8	EXTVCC_C	29	EXTVCC_C	49	EXTVCC_C
	9	DOUT_C6	30	DOUT_C7	50	EXTVCC_C
	10	DOUT_C3	31	DOUT_C4	51	DOUT_C5
	11	DOUT_C0	32	DOUT_C1	52	DOUT_C2
CLUSTER B	12	EXTGND_B	33	EXTGND_B	53	EXTRESET_B
	13	EXTVCC_B	34	EXTVCC_B	54	EXTVCC_B
	14	DOUT_B6	35	DOUT_B7	55	EXTVCC_B
	15	DOUT_B3	36	DOUT_B4	56	DOUT_B5
	16	DOUT_B0	37	DOUT_B1	57	DOUT_B2
CLUSTER A	17	EXTGND_A	38	EXTGND_A	58	EXTRESET_A
	18	EXTVCC_A	39	EXTVCC_A	59	EXTVCC_A
	19	DOUT_A6	40	DOUT_A7	60	EXTVCC_A
	20	DOUT_A3	41	DOUT_A4	61	DOUT_A5
	21	DOUT_A0	42	DOUT_A1	62	DOUT_A2

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2.4 CapROM EEPROM

The CapROM is a 4 kBit (512 byte) EEPROM which provides the capability to store board control relevant information to allow software configuration of the CP382.

2.5 Monitor and Control (M/C)

The front panel of the board is equipped with two LED's for user defined purposes. One green (RUN) and one red (FAIL) have been placed on the front panel in anticipation of their most likely use. However they are freely programmable, the indicators being selected by the system master (access to the hardware debug register (hdr)).

The system failure indicators regarding undervoltage, overcurrent and overtemperature are made available to the DO ProComm controller. These indicators are automatically reset by the HSD switches once the conditon has been corrected and the output returns to normal mode.

An input signal Halt/Reset is available to set an inactive state for each individual cluster and also to shut down each individual cluster during operation as necessary.

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Chapter 3

Installation

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3. Installation

The CP382 has been designed for easy installation. However, the following standard precautions, installation procedures and general information must be observed to ensure proper installation and to preclude damage to the board or injury to personnel.

3.1 Hardware Installation

The product described in this manual can be installed in any available 3U slot of a CompactPCI system except for the system master slot.

3.1.1 Safety Requirements

The board must be securely fastened to the chassis using the two front panel retaining screws located at the top and bottom of the board to ensure proper grounding and to avoid loosening caused by vibration or shock.

In addition the following electrical hazard precautions must be observed.



Caution, Electric Shock Hazard!

Ensure that the system main power is removed prior to installing or removing this board. Ensure that there are no other external voltages or signals being applied to this board or other boards within the system. Failure to comply with the above could endanger your life or health and may cause damage to this board or other system components.



ESD Equipment!

This PEP board contains electrostatically sensitive devices. Please observe the following precautions to avoid damage to your board:

Discharge your clothing before touching the assembly. Tools must be discharged before use.

Do not touch any on board components, connector pins, or board conductive circuits.

If working at an anti-static workbench with professional discharging equipment, ensure compliance with its usage when handling this product.

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3.1.2 Installation Procedures

To install the board proceed as follows:

1. Ensure that the safety requirements indicated above are observed.



Warning!

Failure to comply with the instruction below may cause damage to the board or result in improper system operation. Please refer to chapters 4 and 5 for configuration information.

2. Ensure that the board is properly configured for operation before installing.



Note...

Care must be taken when applying the procedures below to ensure that when the board is inserted it is not damaged through contact with other boards in the system.

3. To install the board perform the following:
   1. Prior to installation of the board disengage the insertion/extraction handle by first unlocking the handle and pressing it down.
   2. Insert the board into an appropriate slot, and, using the insertion/extraction handle, ensure that it is properly seated in the backplane. (Front panel is flush with the rack front; the insertion/extraction handle is locked.)
4. Fasten the front panel retaining screws.
5. Connect external interfacing cables to the board as required.
6. Ensure that the interfacing cables are properly secured.



Warning!

Proper and safe operation of the CP382 Digital Output Controller depends on the correct configuration of the external voltage and loads. System integrators must ensure that all voltages presented to the CP382 comply with the specifications set forth in this manual.

Failure to comply with the above may cause damage to the board or result in improper system operation. Please refer to chapters 4 and 5 for configuration information.

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3.1.3 Removal Procedures

To remove the board proceed as follows:

1. Ensure that the safety requirements indicated above are observed.



Warning!

Care must be taken when applying the procedures below to ensure that when the board is removed it is not damaged through contact with other boards in the system.

2. Disconnect any interfacing cables that may be connected to the board.
3. Loosen both of the front panel retaining screws.
4. To remove the board from the backplane perform the following:
    1. Unlock the insertion/extraction handle by pressing down on the grey locking mechanism in the middle of the handle. (This should be achievable with a minimum of force. If necessary lift the handle up slightly while pressing down on the grey locking mechanism.)
    2. Disengage the board from the backplane by pressing down on the insertion/extraction handle and pull the board out of the slot ensuring that the board does not make contact with adjacent boards. (If the handle does not move, it is not unlocked. Repeat the unlocking procedure above and try again. Do not use force!)

3.2 Software Installation

Installation of the CP382 driver software is a function of the application operating system. For further information refer to the appropriate software documentation.

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Chapter 4

Configuration

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4. Configuration

This chapter provides information for configuring the CP382 board for operation.

4.1 Jumper Settings

The CP382 does not have any jumpers which require configuring.

4.2 Digital Output Signal Properties

In addition to the output signal type and its range, which have been specified in chapter 1, paragraph 1.3.1, system integrators must be aware of certain output configuration requirements for the CP382. The following paragraphs provide some information regarding individual connection configuration requirements.

4.2.1 Channels

The CON2 connector of the CP382 is designed so that there is one output pin per channel. This is illustrated in Figure 2-2, which shows the front panel connector pinout, with the 24 channels shown starting at the top of the connector with channel 0 (cluster A).

The following sections address the basic requirements.

4.2.2 Connection of External Supply

The CP382 requires an external voltage for operation.

The input connection for this voltage is realized via the 62-pin front panel connector CON2. The pinout of this connector is provided in table 2-1.

The three clusters have split supply planes, so that it is possible to provide each cluster (clusters A, B and C) with a separate voltage, with different voltage values within the defined range (see also table 1-1).



Note...

Each channel has a maximum current of 0.5 A. In situations where many channels are carrying a high current, separate, larger gauge cables for the external power supply should be used.

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4.2.3 Channel Connection

The following diagrams illustrate the external connection of the CP382 to the application.

Figure 4-1: Digital Output Connection for One Cluster

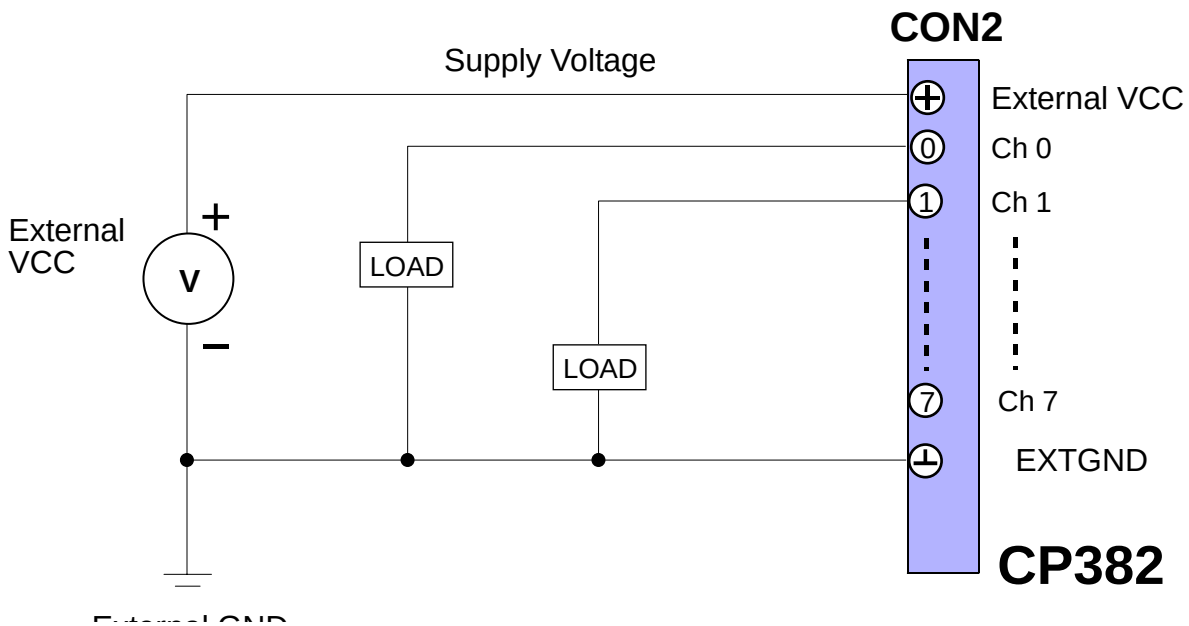
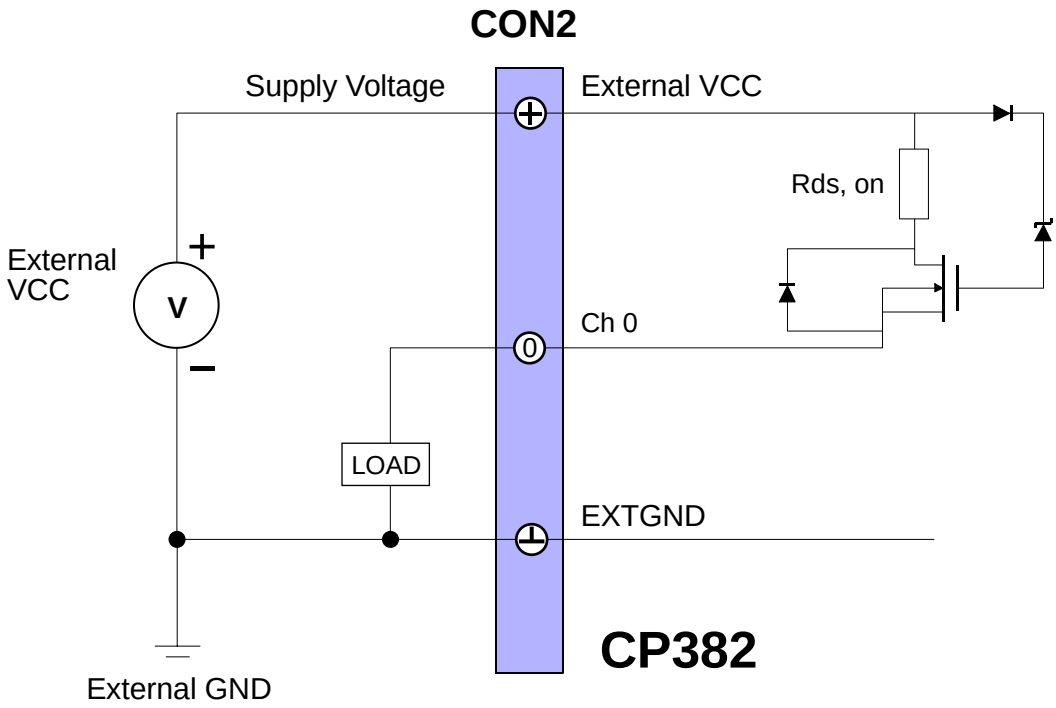
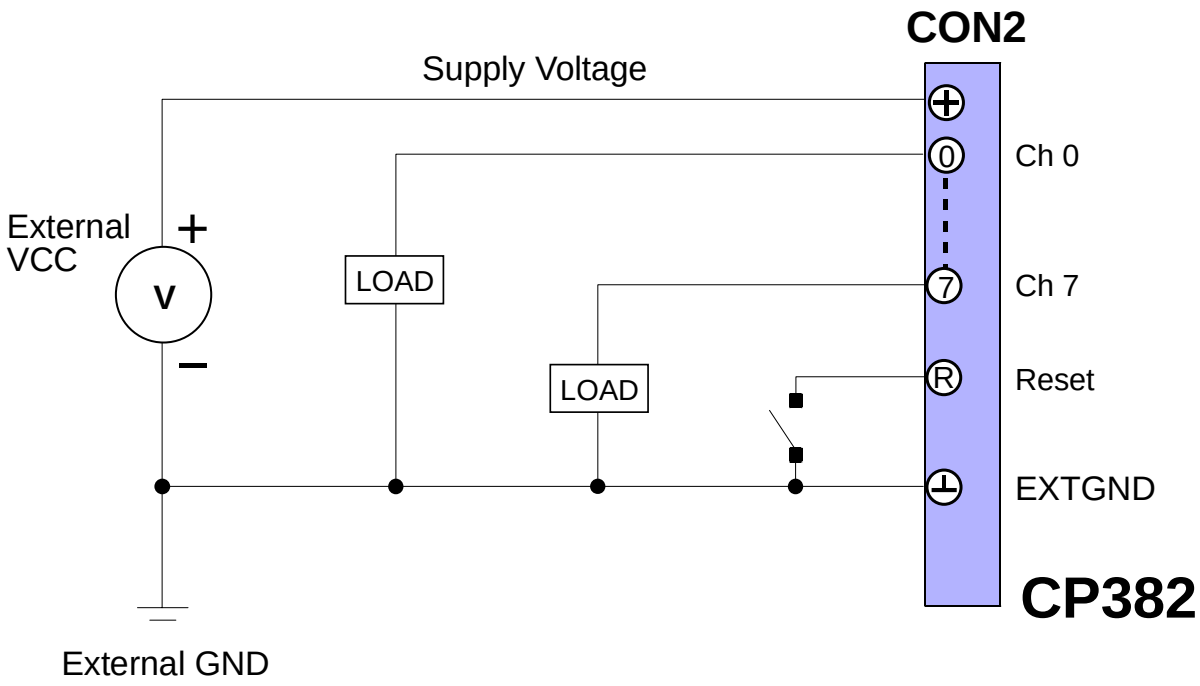


Figure 4-2: Digital Output Circuit for One Channel



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Figure 4-3: External Reset Connection for One Cluster



Note...

The voltage source for each cluster is an external supply (in the range +9.5V to +35V DC). Therefore the GND reference for the digital output is the ground potential of this external voltage supply.

Important...

Individual outputs should not be cascaded as it cannot be guaranteed that power sharing will be proportional, due to the transistor characteristics of each HSD (HighSide Driver switch).

4.2.4 Connection of Inductive Loads

The outputs have internal clamping diodes for each channel, which are able to demagnetize inductive loads.

The limitation is the peak power dissipation of the digital outputs at the front end. Where there are large loads or if there is the possibility that additional loads require demagnetization simultaneously, external demagnetization circuits are required.

There are two possible topologies for the demagnetization versus ground or versus supply voltage.

Note...

For more detailed information about the external demagnetization circuits, please refer to the L6376 datasheet referenced under chapter 1.8 Related Publications.

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4.3 Programming Interface

4.3.1 Access Control Logic (Address Decoder)

All the resources of the CP382 are mapped within the 64 kB PCI memory address space which itself is set in the PCI configuration register BAR0. The port size of all local or backend registers is 32-bit by default. The address map of the registers is as follows.

Table 4-1: Backend Register Address Map

Base Address	Size	Function
bar0 + 0x0000	4 K	Common Board Registers
0x0400	32 bit	g_irq General Interrupt Enable Register
0x0800	32 bit	hsr Hardware Status Register
0x0804	32 bit	i_pen General Interrupt Pending Register
0x0c00	32 bit	hdr Hardware Debug Register
bar0 + 0x1000	4 K	Capability ROM, serial EEPROM
0x1000	32 bit	r_cmd Command Register
0x1400	32 bit	r_ctl Control Register
0x1800	32 bit	r_sta Status Register
0x1c00	32 bit	r_dat Data Register
bar0 + 0x2000	4 K	DigOUT Cluster A
0x2400	32 bit	o_ctl_a Output Control Register
0x2800	32 bit	o_sta_a Output Status Register
0x2c00	32 bit	o_dat_a Output Data Register
bar0 + 0x3000	4 K	DigOUT Cluster B
0x3400	32 bit	o_ctl_b Output Control Register
0x3800	32 bit	o_sta_b Output Status Register
0x3c00	32 bit	o_dat_b Output Data Register
bar0 + 0x4000	4 K	DigOUT Cluster C
0x4400	32 bit	o_ctl_c Output Control Register
0x4800	32 bit	o_sta_c Output Status Register
0x4c00	32 bit	o_dat_c Output Data Register
bar0 + 0x5000 - 0xffff	44 K	Reserved

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4.3.2 Writing Output Data

Table 4-2: Output Data Register Bit Map

Bits	Type	Default	Function
31-8	r/w	0	Reserved
7-0	r/w	0	Data, 8 bit digit



Note...

Output data is 8 bit (each cluster); this register is read/write enable.

Table 4-3: Output Control Register

Bits	Type	Default	Function
31-2	r/w	0	Reserved
1	r/w	0	irqen
0	r/w	1	Reset



Note...

irqen is for diagnostic issuing an interrupt.

The reset bit should be set to 0 to activate a cluster.

Table 4-4: Output Status Register, Bit Map

Bits	Type	Default	Function
31	r	0	Fail
30	r	0	Diag
29-0	r	0	Reserved



Note...

The Diag status flag is the diagnostic bit from the HSD switch; Fail is the latched diag status flag.

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4.3.3 Hardware Debug/Test Registers

These registers are for internal test and debug only. The Common Status Register contains Logic-Version and PCB -Version. The Common Debug Register is a read/write register without any further functionality besides the front panel monitor and control LED's.

Table 4-5: Hardware Debug Register Bit Map

Bits	Type	Default	Function
31-2	r/w	0	Reserved
1	r/w	0	FAIL
0	r/w	0	RUN

Table 4-6: Hardware Status Register Bit Map

Bits	Type	Default*	Function
31-16	r	0	Reserved
15-8	r	00	HW Version (PCB Index)
7-0	r	01	Logic Version



Note...

The HW version starts with 0, the Logic version starts with 1. At each further release it will be incremented by 1.

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4.3.4 Generating Interrupts

A detected fail flag set in the register can trigger an interrupt.

1. Check if the board is the cause of the interrupt (General Interrupt Pending is set)
2. If yes, check the reason for the interrupt by reading the fail flag in the output status register
3. Reset the corresponding Flag by writing a 1 to a set status bit (fail).
4. Reset the boards' IRQ by resetting the General Interrupt Pending Bit by writing a 1 to that status bit
5. Return from Interrupt

Table 4-7: General Interrupt Enable Register, Bit Map

Bits	Type	Default	Function
31	r/w	0	Board Interrupt Enable
29 - 0	r/w	0	Reserved



Note...

The board will continue issuing an interrupt until all interrupt sources are completely dealt with and no interrupt condition remains.

A set bit means that the boards' interrupt is enabled.

Table 4-8: General Interrupt Pending Register, Bit Map

Bits	Type	Default	Function
31	r/w	0	Board Interrupt Pending
29 - 0	r/w	0	Reserved



Note...

A set bit means that the boards' interrupt is pending. A board interrupt must be cleared by writing a "1" to the corresponding output irqen event flag.

Table 4-9: Output Status Register, Bit Map

Bits	Type	Default	Function
31	r	0	Fail
30	r	0	Diag
29 - 0	r	0	Reserved

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4.3.5 Programming the Board Capability ROM

The Board Capability ROM contains all the board data necessary to identify board, version, optional features, etc., and to setup the basic software. The BCR is implemented using a 4 KBit serial EEPROM of the type Microchip 93LC66.

(The contents list of the BCR is not described here.)

The serial interface of the device has been realized in hardware resulting in a very simple register based programming interface with command, control, status and data registers. All protocol and serial timing specifications are resolved by hardware.

Programming of the BCR is undertaken as follows: The control word is written into the ROM Control Register including command opcode and internal address. Then optional data (in case of Write action) is written into the ROM Data Register. Command execution is started by setting the Startbit in the ROM Command Register. Then Ready/Busy must be polled in the ROM Status Register. After reaching Ready status, the next command can be set up and data (in case of Read action) can be fetched from the ROM Data Register.

Table 4-10: ROM Command Register Bit Map

Bits	Type	Default	Function
31	r/w	0	Startbit
30-0	r/w	00	Reserved



Note...

The Startbit will be automatically reset as soon as an action is completed.

Table 4-11: ROM Control Register Bit Map

Bits	Type	Default	Function
31-19	r/w	0	Reserved
17-16	r/w	00	Opcode
15-8	r/w	00	Reserved
8-0	r/w	00	Internal address (A8..A0)



Note...

The commands READ, EWEN (Write Enable) and WRITE are sufficient for all purposes.

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Table 4-12: Opcodes and Commands

Opcode	A8..A0	Command
00	11xxxxxxx	EWEN
10	xxxxxxxxx	READ
01	xxxxxxxxx	WRITE



Note...

The EWEN (Erase and Write Enable) command must be executed once before the first write.

Table 4-13: ROM Status Register Bit Map

Bits	Type	Default	Function
31	r/w	0	Busy/Ready
30-0	r/w	00	Reserved



Note...

As soon as the Startbit is set the Busy/Ready bit becomes active (Busy=1). It remains set as long as the command is executed and is reset when command execution is complete.

Table 4-14: ROM Data Register Bit Map

Bits	Type	Default	Function
31-8	r/w	0	Reserved
7-0	r/w	0	Data (for data read and write commands)

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Chapter 5

System Considerations

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5. System Considerations

5.1 Introduction

In addition to the basic specification requirements for the CP382 which have been addressed in chapter 4, system integrators need to be aware of the overall system environment and the application needs when designing the interfacing to the CP382. The following chapters address a number of more apparent considerations which should be addressed but certainly not all of the possible situations which may be encountered. Many of the considerations presented here are recommendations, but some are definite requirements if the CP382 is to successfully achieve its purpose.

5.2 General

Considerations:

1. Care must be taken to ensure that proper grounding concepts are followed, and that the integrity of the grounding system within the application be maintained.
2. Where possible input wiring length should be kept as short as possible.

5.3 Shielding

Considerations:

1. Input cable shielding in general is recommended.
2. The requirements for shielding can be seen primarily as a function of the system design and environment, but empirical results must also be considered.
3. The CON2 connector has a metal housing which is connected to the CP382 shield and is isolated from the system ground.
4. Ensure that if shielding is used that it is not in anyway connected to the system ground.

5.4 External Power Supply

Considerations:

1. Voltage sources presented to the CP382 must be within the ranges specified in chapter 1.3.1 or erroneous results will occur as well as possible damage to the CP382.
2. In addition to supplying the current for the logic parts of the power switches which are linked to the digital outputs, the external voltage supplies also have to supply the current for the 8 digital output loads per cluster.

5.5 Cable Interfacing

If necessary, cabling to the CP382 CON2 connector should be physically fixed to prevent strain on the CON2 connector.



Warning!

Each channel has a maximum current of 0.5 A. In situations where many channels are carrying a high current, separate, larger gauge cables for the external power supply should be used.

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