CP384

16 Digital Inputs - 8 Digital Outputs (Relay)
CompactPCI Controller

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User Guide

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Environmental Protection Statement

This product has been manufactured to satisfy environmental protection requirements where possible. Many of the components used (structural parts, printed circuit boards, connectors, batteries, etc.) are capable of being recycled.

Final disposition of this product after its service life must be accomplished in accordance with applicable country, state, or local laws or regulations.

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Explanation of Symbols



CE Conformity

This symbol indicates that the product described in this manual is in compliance with all applied CE standards. Please refer also to the section “Applied Standards” in this manual.



Caution, Electric Shock!

This symbol and title warn of hazards due to electrical shocks (> 60V) when touching products or parts of them. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your material.

Please refer also to the section “High Voltage Safety Instructions” on the following page.



Warning, ESD Sensitive Device!

This symbol and title inform that electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Please read also the section “Special Handling and Unpacking Instructions” on the following page.



Warning!

This symbol and title emphasize points which, if not fully understood and taken into consideration by the reader, may endanger your health and/or result in damage to your material.



Note ...

This symbol and title emphasize aspects the reader should read through carefully for his or her own advantage.

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For Your Safety

Your new Kontron product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new Kontron product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions



Warning!

All operations on this device must be carried out by sufficiently skilled personnel only.



Caution, Electric Shock!

Before installing your new Kontron product into a system always ensure that your mains power is switched off. This applies also to the installation of piggybacks.

Serious electrical shock hazards can exist during all installation, repair and maintenance operations with this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing work.

Special Handling and Unpacking Instructions



ESD Sensitive Device!

Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the board is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the board.

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General Instructions on Usage

In order to maintain Kontron's product warranty, this product must not be altered or modified in any way. Changes or modifications to the device, which are not explicitly approved by Kontron Modular Computers GmbH and described in this manual or received from Kontron's Technical Support as a special handling instruction, will void your warranty.

This device should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This applies also to the operational temperature range of the specific board version, which must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, please follow only the instructions supplied by the present manual.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the board, please re-pack it as nearly as possible in the manner in which it was delivered.

Special care is necessary when handling or unpacking the product. Please consult the special handling and unpacking instruction on the previous page of this manual.

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If the customer's eligibility for warranty has not been voided, in the event of any claim, he may return the product at the earliest possible convenience to the original place of purchase, together with a copy of the original document of purchase, a full description of the application the product is used on and a description of the defect. Pack the product in such a way as to ensure safe transportation (see our safety instructions).

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Chapter 1

Introduction

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1. Introduction

1.1 System Overview

The CompactPCI board described in this manual operates with the PCI bus architecture to support additional I/O and memory-mapped devices as required by various industrial applications. For detailed information concerning the CompactPCI standard, please consult the complete Peripheral Component Interconnect (PCI) and CompactPCI Specifications. For further information regarding these standards and their use, visit the home page of the *PCI Industrial Computer Manufacturers Group (PICMG)*.

Many system relevant CompactPCI features that are specific to Kontron Modular Computers CompactPCI systems may be found described in the Kontron CompactPCI System Manual. Please refer to the section “Related Publications” at the end of this chapter for the relevant ordering information.

The CompactPCI System Manual includes the following information:

- Common information that is applicable to all system components, such as safety information, warranty conditions, standard connector pinouts etc.
- All the information necessary to combine Kontron’s racks, boards, backplanes, power supply units and peripheral devices in a customized CompactPCI system, as well as configuration examples.
- Data on rack dimensions and configurations as well as information on mechanical and electrical rack characteristics.
- Information on the distinctive features of Kontron CompactPCI boards, such as functionality, hot swap capability. In addition, an overview is given for all existing Kontron CompactPCI boards with links to the relating data sheets.
- Generic information on the Kontron CompactPCI backplanes, such as the slot assignment, PCB form factor, distinctive features, clocks, power supply connectors and signalling environment, as well as an overview of the Kontron CompactPCI standard backplane family.
- Generic information on the Kontron CompactPCI power supply units, such as the input/output characteristics, redundant operation and distinctive features, as well as an overview of the Kontron CompactPCI standard power supply unit family.

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1.2 Product Overview

The CP384 Digital Input and Digital Output Controller is part of a comprehensive concept to provide CompactPCI system integrators with a complete range of CompactPCI I/O products which include the functions of analog input, analog output, digital input, and digital output implemented as separate individual boards. This concept ensures a maximum degree of system design flexibility thus allowing efficient and effective usage of available resources.

As an enhancement to this concept, the CP384 combination board has been designed to implement digital input and digital output functions on one board. The CP384 is a 3U/4HP CompactPCI board which provides 24 channels that are organized into two separate clusters, one cluster consisting of 16 channels for digital input, and one cluster consisting of 8 channels of relay switched (SPDT) digital output.

The basic functions of this board are on the one hand to provide interfacing to the application (process), perform D/D signal conversions, and to make raw digitized data available for further processing via the 16 input channels, and on the other hand to provide a large number of automatically controlled, flexible digital outputs within a ruggedized board. The digital output cluster requires external input voltages (process side) for operation, both for the outputs as well as the supply voltage for the relay coils.

The major components involved in these processes are the front end (process side) signal conditioning (digital input and digital output), the relays for the digital outputs, and the Digital Input and Output Process and Communications (DIO ProComm) Controller which is realized in a field-programmable gate array (FPGA). The DIO ProComm Controller is designed to provide effective and efficient control of the digital input and output processes as well as interfacing to the CPCI system controller.

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The following table provides a quick overview of the CP384 board.

Table 1-1: CP384 Product Overview

CP384 FEATURES	DESCRIPTION
Digital Input and Output Board	• CompactPCI: 3U, 4HP • 33 MHz system clock • 32-bit address and data bus • Designed for Plug and Play • Complies with the CPCI specification
Digital Input Channel	• Input Signals: Voltage range:low: -3V to +5V high: +11V to +30 V (+24V standard) Maximum current: 5 mA • Channel Isolation: The input channels are isolated from the system side and do not share common GND or VCC. • Output Data: A maximum of 16 measured digital values Interrupt messages (optional) Programmable registers (read/write, compare, event and latch) • Debouncing: Range of settings available: 33 MHz, 128 kHz, 32 kHz, 8 kHz, 2 kHz, 500 Hz, 125 Hz, 31 Hz (30 ns default)
Digital Output Channels	One cluster of 8 channels of relay switched digital outputs Each channel has its own set of single pole, double throw relay contacts: common, normally open, and normally closed. The cluster permits only one supply voltage (24V ± 20%) for the relay coils. The relay contacts may be supplied with different voltages within the allowable range. The output channels are galvanically isolated from the system side and from each other within the CP384.
External Interfaces	2 external interfaces: the digital input and output interface connector (CON2) on the front panel and a single CompactPCI connector (CON1(J1)) at the rear. The digital input and output interface connector supports up to 16 digital input and 8 3-pin digital output channels. The connector pins are subdivided into 2 clusters or groups. The CompactPCI connector is the standard CPCI type connector for CON1.
Indicators	One green LED (Run) and one red LED (Fail) which are user configurable
Temperature Range	The board is qualified to operate over a wide range of temperatures as follows: • Operational: 0ºC to +60ºC Standard -40ºC to +85ºC E2 • Storage: -40ºC to +115ºC

1.3 Board Overview

1.3.1 Board Introduction

The CP384 is a digital input and digital output board which provides 24 channels grouped into one digital input cluster consisting of 16 channels and one digital output clusters consisting of 8 channels.

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1.3.1.1 Board Introduction - Digital Input

The digital input cluster consists of 16 input channels. The source of the digital inputs must be a voltage generator. The board accepts only differential voltages up to a maximum of +30V. The input current is limited to 5 mA over the specified input voltage range.

Input signal processing begins with the presentation of the signal to the front panel connector. Signal conditioning prior to the signal reaching the DIO ProComm Controller includes: overvoltage protection, ESD, low-pass filtering, inverse polarity protection, defined low and high ranges, current limitation, optoisolation and buffering.

After signal conditioning, all parallel digital data is routed to the DIO ProComm Controller, where the control and status registers are set.

The DIO ProComm Controller controls the interface with the CompactPCI bus and the dedicated software.

Input signal types and ranges are as follows:

- Edge frequency:
  - Maximum 10 kHz
- Voltage Ranges:
  - High range: +11V to +30V (+24V nominal)
  - Low range: -3V to +5V
- Channel isolation
  - The input channels are isolated from the system side and do not share common GND or VCC.
- Differential input

Output data:

The following outputs are routed from the DIO ProComm Controller to the CompactPCI bus:

- Input data for all channels as a 32-bit value (each bit from 0 - 15 represents the status of the respective input channel)
- Flag set information from the control and status registers
- Interrupts

1.3.1.2 Board Introduction - Digital Output

The digital output clusters consist of 8 output channels. The digital output requests from the system controller are processed accordingly by the DIO ProComm Controller and are then routed to the relay drivers which switch the relays on or off using the external supply voltage as the relay coil power source.

An external input can be provided to simultaneously switch off all of the relays in the cluster and to connect Com (common) pin with NC (normally connected) pin on all of the relays. The same operation may be done using the internal reset signal generated by the system side.

This reset can be used by the application to keep the inputs low after a fault condition occurs.

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1.3.2 Board Specific Information

Specific board components involved in the digital output process:

- One front panel connector (62-pin, female, D-sub type)
- 16 channels of input signal conditioning
- 8 channels of output signal conditioning: 8 single pole, double throw (SPDT) 3 circuit relays: common (COM), normally open (NO), normally closed (NC)
- Optoisolation for each input and output channel from the system side
- One FPGA (the DIO ProComm Controller)
- One CompactPCI bus connector (CON1, board to backplane, 132-pin, female, six row)
- One EEPROM (CapROM)

1.4 System Relevant Information

The following system relevant information is general in nature but should still be considered when developing applications using the CP384.

Table 1-2: System Relevant Information

SUBJECT	INFORMATION
System Configuration	The CP384 operates with a system clock frequency of 33 MHz. The number of CP384s which can be installed in any one system depends solely on the number of available slots within the system.
Master/Slave Functionality	The CP384 functions only as a slave. As such it requires a System Master for servicing.
System Controller	The CP384 cannot function as a system controller.
Digital Inputs	Digital inputs to the CP384 must be conform to the inputs specifications set forth in this manual for the CP384. In most cases, some form of signal conditioning will be required on the process side prior to a signal being presented to the CP384.
Digital Outputs	The voltage source for the digital outputs of CP384 must conform with the specifications set forth in this manual.

1.4.1 System Configuration

When implementing applications, precautions must be taken to ensure that the input signals presented to the CP384 comply with the specifications set forth in this manual. For this reason it will be necessary for most applications to provide signal conditioning prior to presenting the digital inputs to the CP384.

The external supply voltage (VCC) used to supply the output cluster relay coils must be within the specified supply voltage range. In addition, it should be a DC supply with good ripple and noise characteristics. Please refer to chapters 4 and 5 for further information.

1.4.2 Driver Software

The CP384 is supplied with appropriate driver software which provides software interfacing with the System Master.

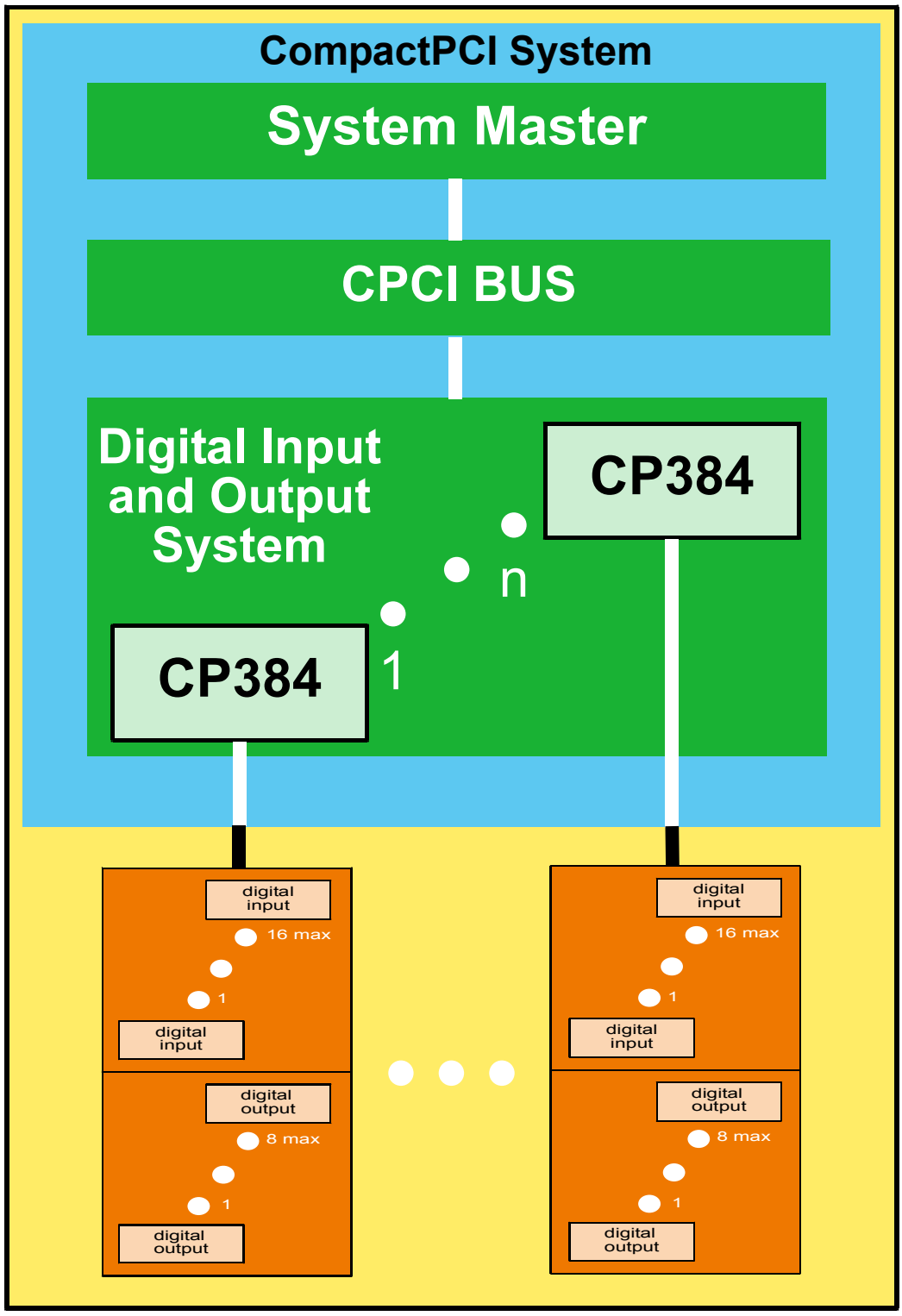
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1.5 Board Diagrams

The following diagrams illustrate board functionality and component layout.

1.5.1 System Level Interfacing

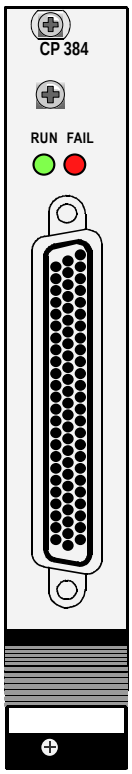
Figure 1-1: CP384 System Level Interfacing Diagram



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1.5.2 Front Panel

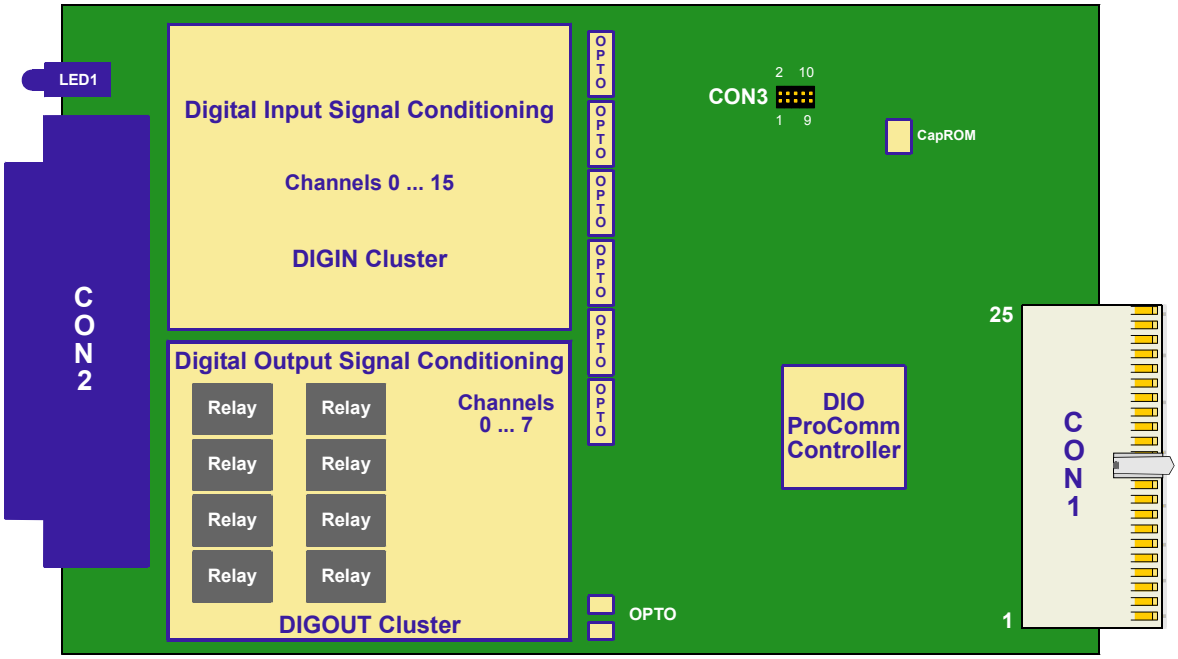
Figure 1-2: CP384 Front Panel



A green “Run” LED and a red “Fail” LED have been placed on the front panel, to cater for the most likely use of these LEDs. However, they are user configurable and may be employed for user defined purposes.

1.5.3 Board Layout

Figure 1-3: CP384 Board (Front View)



1.6 Technical Specifications

Table 1-3: CP384 Main Specifications

GROUP/ INTERFACE	TYPE	DESCRIPTION
DIO ProComm Controller and Related	FPGA Logic Device	Provides CompactPCI interfacing and IO control logic
Peripheral Memory	CapROM	4 kbit (512 byte) EEPROM
CompactPCI Interface *(See note at foot of table)*	Realized on 132-pin, female, six row connector (standard CPCI type connector for CON1)	Bus Width: 32-bit, Bus Speed: 33 MHz 64 kB memory space, non-prefetchable Utilizes interrupt line INTA
	Software Driver Information	PCI Header: Device ID: 0x5555 Vendor ID: 0x1556 Class Code: 0x110000 Subsystem Device ID: 0x0121 Subsystem Vendor ID: 0x1518
	PCI Interface	VI/O voltage is neither relevant nor used
	Master / Slave Functionality	Only slave functionality provided
Digital Input and Output Interface	One 62-pin, female, three row, D-sub connector	Supports up to 16 digital input channels and 8 digital output channels
Indicators	Front Panel LEDs	One green and one red LED to indicate operational status
General	Form Factor	3U, 4HP
	Mechanical	Conforms with IEEE 1101.1
	System Power Consumption	only + 3.3V: maximum 600 mW (all IO channels activated)
	Temperature Range	Operational: 0ºC to +60ºC Standard Storage: -40ºC to +115ºC
	Climatic Humidity	93 % RH at 40°C, non-condensing (acc. to IEC 60068-2-78)
	Dimensions	100 mm x 160 mm single height Eurocard
	Board Weight	180 grams



Note ...

The Device ID and Vendor ID refer to the chip manufacturer. In the Class Code value given, “11” relates to the data acquisition and signal processing controllers and “0000” relates to the DPIO modules. Subsystem Device ID and Subsystem Vendor ID are defined by Kontron.

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Table 1-4: CP384 Digital Input Specifications

TYPE	DESCRIPTION
Input Voltage Range	Low: -3V to +5V High: +11V to +30V
Channels	16 channels isolated from the system side. They do not share common GND or VCC.
Channel Connections	2 pins per channel; differential input
Input Filter (edge frequency)	10 kHz
Input Protection	8 kV ESD
Isolation	2 kV process to system
Input Impedance	Minimum: 1.5 k ohm Maximum: 6 k ohm at 30V

Table 1-5: CP384 Digital Output Specifications

TYPE	DESCRIPTION
Channels	8 channels of relay switched digital outputs grouped into one cluster
Channel Connections	Each channel is comprised of a single pole, double throw set of relay contacts: • COM (common): relay middle pole • NO (normally open): when the relay is switched off this pin is not connected to the COM pin • NC (normally closed): when the relay is switched off this pin is connected to the COM pin All relay contacts are routed to the front panel connector. Within the CP384 each relay and its contacts are galvanically isolated from the system and from the other relays and their contacts.
External Reset	All digital output channels of a cluster can be collectively switched to the normally closed (NC) position by using one of the following methods: • externally via the EXTRESET signal • internally on request from the application via the DIO ProComm controller This results in all outputs being switched to the NC position irrespective of the input data for these channels.
Switching Voltage Range (Resistive Load)	The CP384 is designed to switch up to 250V DC/AC and up to 0.5A of current, but the total power per contact being switched must be less then 15W. A relay's life time is about $2x10^6$ switches at switching voltage 24V and switching current 0.5A.
Switch Contact Resistance	< 50 milliohms
Switching Delay Time	T_{on} = 3 ms (typical at 24V) T_{off} = 2 ms (typical at 24V with no coil suppression)
Switching Bounce Time	T_{bounce} = 3 ms (typical at 24V)

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Table 1-5: CP384 Digital Output Specifications (Continued)

TYPE	DESCRIPTION
External Supply Voltage (VCC)	+ 24V ± 20% (working range)
External Supply Current (VCC)	All relays ON: • 90 mA at 19.2V • 110 mA at 24 V • 130 mA at 28.8V
Signal Output Over Current Protection	No over current protection is provided by the CP384 for the digital outputs. If over current protection is required, it must be provided by the application system.
External Power Supply	For proper operation of the output channels the external power supply voltage (EXTVCC) must be within the range: + 19.2 V to 28.8 V DC. If the EXTVCC is below or above the specified range, proper operation of the output channels is not guaranteed. For invalid values of EXTVCC, the output cluster is forced into the reset state resulting in all relays being switched off and the outputs switched to the NC position.
Output RC units	There are capacitor filters connected to the output channel pins: COM, NO, NC.
Isolation	2 kV process to system

1.7 Software Support

The CP384 is supplied with appropriate driver software which provides software interfacing to the System Master. The CP384 supports Windows XP®, Windows NT 4.0®, Windows 2000®, VxWorks® and Linux®.

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1.8 Applied Standards

The Kontron Modular Computers' CP384 board complies with the requirements of the following standards:

Table 1-6: Applied Standards

COMPLIANCE	TYPE	STANDARD	TEST LEVEL
CE	Emission	EN55022 EN61000-6-3	--
	Immission	EN55024 EN61000-6-2	--
	Electrical Safety	EN60950-1	--
Mechanical	Mechanical Dimensions	IEEE 1101.10	--
	Transport and Storage	IEC 61131-2	--
Environmental and Health Aspects	Vibration (sinusoidal)	IEC60068-2-6	--
	Shock	IEC60068-2-27	--
	Bump	IEC60068-2-29	--
	Vibration, broad-band random (digital control) and guidance	IEC60068-2-64	--
	Climatic Humidity	IEC60068-2-78	93% RH at 40°C, non-condensing

1.9 Related Publications

Table 1-7: Related Publications

	ISSUED BY	DOCUMENT
CompactPCI Systems	PICMG	CompactPCI Specification, V. 2.0, Rev. 3.0
	Kontron Modular Computers	CompactPCI Systems Manual (ID 19953)
CP384	American Zettler	AZ832 polarized DIP relay single side stable

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Chapter 2

Functional Description

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2. Functional Description

The following chapters present more detailed, board level information about the CP384 Digital Input and Digital Output Controller whereby the board components and their basic functionality are discussed in general.

2.1 General Information

The CP384 is comprised basically of the following:

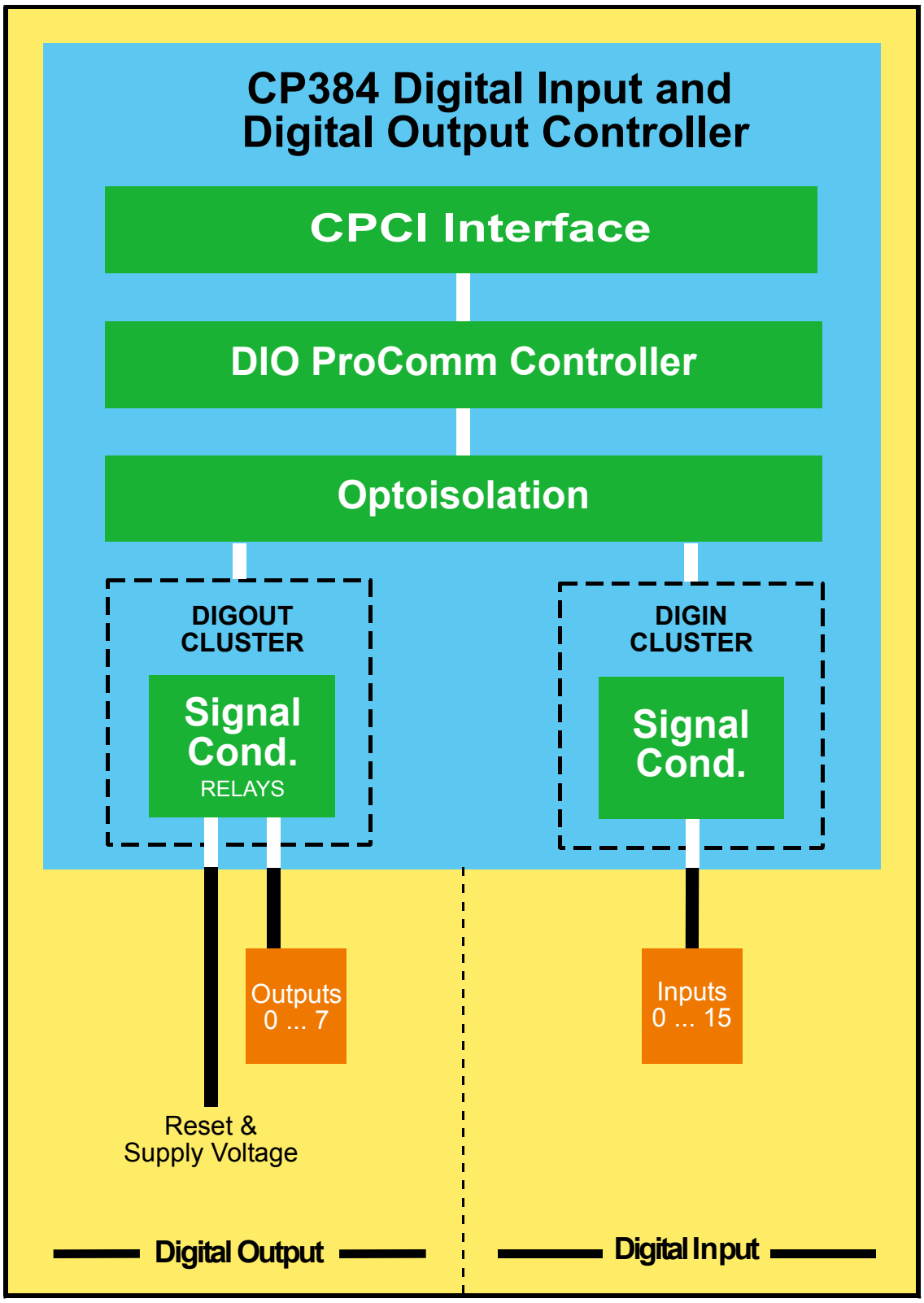
- Digital input signal conditioning
- Digital output signal conditioning (2 Form C relays), external supply for the output cluster
- Optocouplers
- DIO ProComm Controller
  - Controls digital inputs and outputs
  - Provides interfacing to the CompactPCI bus
- System interfaces for:
  - Front panel
    - 16 channels of digital input and 8 channels of 3-pin digital output
    - External supply connection for the digital output cluster
    - External hardware reset for the digital output cluster
    - One 62-pin, female, 3-pin row, D-sub connector (CON2)
  - CompactPCI bus
    - 132-pin, female, 6-pin row connector (CON1)
    - CompactPCI specification
- Onboard memory: Capability EEPROM (CapROM)
- Monitor and Control
  - Two operational status LEDs for user-defined purposes
  - External reset
  - Output failure indicators
- Software

2.2 Board Level Interfacing Diagram

The following figure demonstrates the interfacing structure between the internal processing modules of the CP384 and other major CP384 system components. Where CP384 system elements have common interfacing they are grouped into a block. Interfacing common to only one element of a block is indicated with a direct connecting line. The interfacing lines are shown in white where they are onboard and in black for board external interfacing.

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Figure 2-1: CP384 Board Level Interfacing



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2.3 Digital Input Signal Conditioning

The digital input signal conditioning consists of the following:

- Overvoltage protection
- Low-pass signal filtering
- Current limitation
- Inverse polarity protection
- Input signal high-low determination
- Output signal stabilization buffering

2.4 Digital Output Signal Conditioning

The major element of the digital output signal conditioning is the 2 Form C relay which is able to switch inductive, capacitive or resistive loads. The 2 Form C relays are double pole, double throw relays with a common single coil where one set of three contacts (COM, NC, NO) are available to the application and the other set of three contacts is reserved.

For proper operation the relay requires a minimum coil supply voltage of 18V. The voltage supervisor monitors the input supply voltage to the coil for under/over voltage condition, and, if detected, switches the coil input suppy off. Under voltage cutoff is 18,6V with 0,3V of hysteresis. Overvoltage cutoff is 29,7V with a histeresis of 0,4V. Within the range of 19,2V to 28,8V proper operation is guaranteed.

The digital output relays are driven by the DIO ProComm Controller via optocoupler devices.

2.5 Optoisolation

The process side is galvanically isolated from the system side. The process side of the board is separated from the system side by a bank of optocouplers which serve to protect the system side from any excess voltages or voltage spikes.

2.6 DIO ProComm Controller

The DIO ProComm Controller is responsible for supervising and controlling the digital acquisition and the digital data output process, and maintaining communication with the CompactPCI System Master. Applications address the CP384 through its software driver interface within the System Master whereby the controller accepts requests from the driver and executes them accordingly. Digital data from the signal conditioning is processed through the DIO ProComm Controller and then made available to the System Master. Digital data from the System Master is processed through the DIO ProComm Controller and then routed to the relay drivers.

2.7 System Interfaces

The CP384 provides interfacing capability for the following system elements:

- Front panel connector
- CompactPCI bus

Digital inputs, digital outputs, external voltage, and external reset are routed via the CON2 connector. Interfacing to the CompactPCI bus is accomplished via the CON1 connector. Test and program development is supported by the CON3 connector.

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The connection for the external supply (+24V DC ± 20%) is realized by reserved/defined pins within the output cluster at the front panel connector CON2.

Note ...

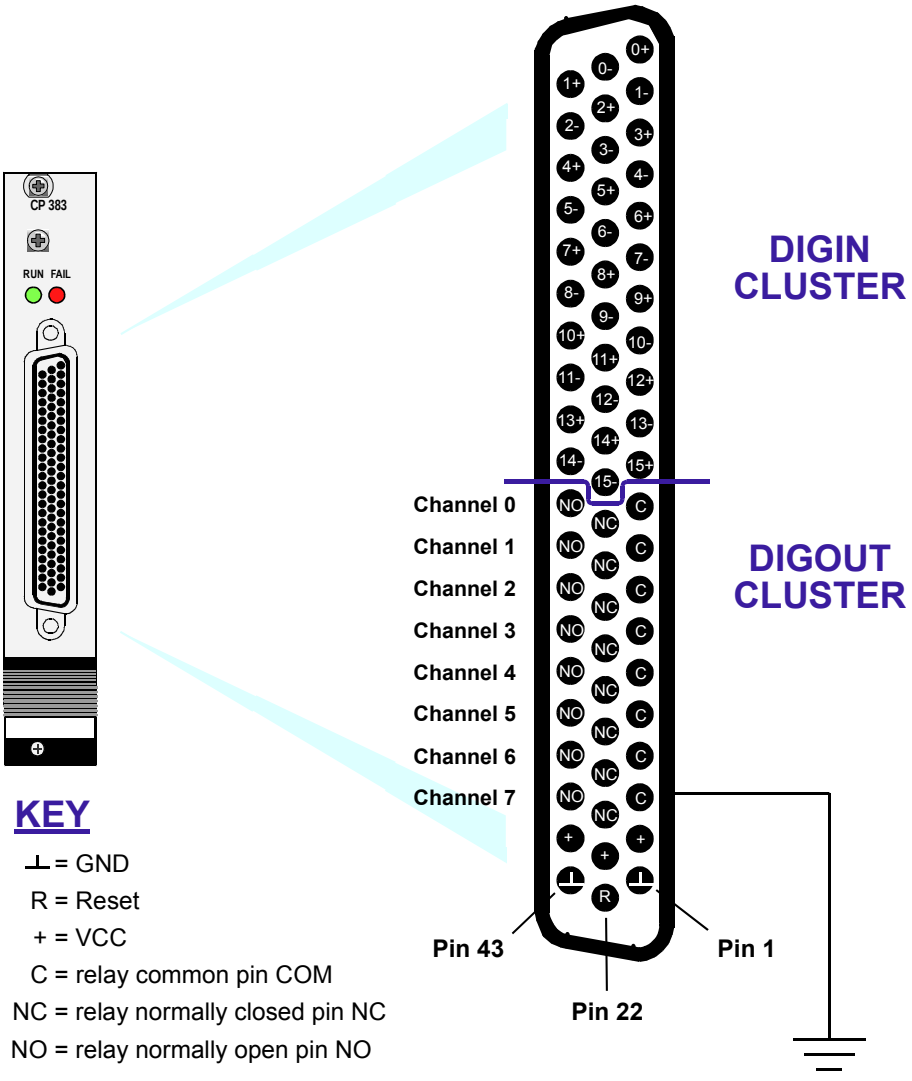
The external power is supplied only to the relay coils. Within the CP384, the external supply power is galvanically isolated from all digital output pins on CON2

At power up, all digital outputs are switched off (NC). In the course of operation they can be collectively switched off, either by software (RESET) or by the application via the EXTRESET signal to the CON2 connector.

2.7.1 Digital Input and Output Interface

The digital input and output interface is routed through the CON2 connector. The following figure and table indicate the pin layout and pinout of this connector.

Figure 2-2: Pin Layout of the Digital Input and Output Interface Connector CON2



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Table 2-1: Pinout of the Digital Input and Output Interface Connector CON2

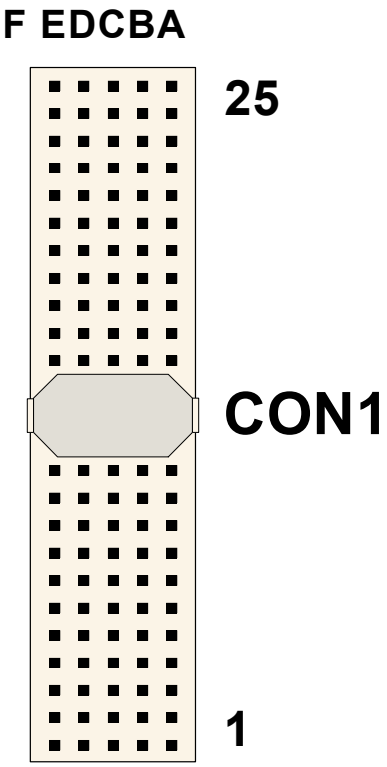
CLUSTER	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
DIGIN			42	DIN0-	21	DIN0+
	62	DIN1+	41	DIN2+	20	DIN1-
	61	DIN2-	40	DIN3-	19	DIN3+
	60	DIN4+	39	DIN5+	18	DIN4-
	59	DIN5-	38	DIN6-	17	DIN6+
	58	DIN7+	37	DIN8+	16	DIN7-
	57	DIN8-	36	DIN9-	15	DIN9+
	56	DIN10+	35	DIN11+	14	DIN10-
	55	DIN11-	34	DIN12-	13	DIN12+
	54	DIN13+	33	DIN14+	12	DIN13-
	53	DIN14 -	32	DIN15-	11	DIN15+
DIGOUT	52	DOUT0_NO	31	DOUT0_NC	10	DOUT0_Com
	51	DOUT1_NO	30	DOUT1_NC	9	DOUT1_Com
	50	DOUT2_NO	29	DOUT2_NC	8	DOUT2_Com
	49	DOUT3_NO	28	DOUT3_NC	7	DOUT3_Com
	48	DOUT4_NO	27	DOUT4_NC	6	DOUT4_Com
	47	DOUT5_NO	26	DOUT5_NC	5	DOUT5_Com
	46	DOUT6_NO	25	DOUT6_NC	4	DOUT6_Com
	45	DOUT7_NO	24	DOUT7_NC	3	DOUT7_Com
	44	EXTVCC	23	EXTVCC	2	EXTVCC
	43	EXTGND	22	EXTRESET	1	EXTGND

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2.7.2 CPCI Interface and Pinout

The CPCI interface is based on the specification PICMG 2.0 R 3.0, 10/1/99. The following figure and table indicate the pin layout and pinout of the CPCI connector, CON1 (J1).

Figure 2-3: CPCI Connector CON1 (J1)



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Table 2-2: Pinout of the CPCI Connector CON1 (J1)

PIN	PIN ROW					
	A	B	C	D	E	F
1	NC	NC	NC	NC	NC	GND
2	NC	NC	NC	TDO	TDI	GND
3	INTA#	NC	NC	NC	NC	GND
4	NC	GND	NC	NC	NC	GND
5	NC	NC	RST	GND	NC	GND
6	NC	GND	3.3V	CLK	AD[31]	GND
7	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND
8	AD[26]	GND	NC	AD[25]	AD[24]	GND
9	C/BE[3]	IDSEL	AD[23]	GND	AD[22]	GND
10	AD[21]	GND	3.3V	AD[20]	AD[19]	GND
11	AD[18]	AD[17]	AD[16]	GND	C/BE[2]	GND
12-14 Key Area						
15	3.3V	FRAME#	IRDY#	GND	TRDY#	GND
16	DEVSEL#	GND	NC	STOP#	LOCK#	GND
17	3.3V	NC	NC	GND	PERR#	GND
18	SERR#	GND	3.3V	PAR	C/BE[1]	GND
19	3.3V	AD[15]	AD[14]	GND	AD[13]	GND
20	AD[12]	GND	NC	AD[11]	AD[10]	GND
21	3.3V	AD[9]	AD[8]	M66EN	C/BE[0]	GND
22	AD[7]	GND	3.3V	AD[6]	AD[5]	GND
23	3.3V	AD[4]	AD[3]	NC	AD[2]	GND
24	AD[1]	NC	NC	AD[0]	NC	GND
25	NC	NC	NC	3.3V	NC	GND

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2.8 CapROM EEPROM

The CapROM is a 4 kbit (512 byte) EEPROM which provides the capability to store board control relevant information to allow software configuration of the CP384.

2.9 Monitor and Control (M/C)

Various monitor and control functions are available for the operation of the CP384. The front panel of the board is equipped with two LEDs for user-defined purposes. One green (RUN) and one red (FAIL) have been placed on the front panel in anticipation of their most likely use. However they are freely programmable, the indicators being selected by the System Master (access to the hardware debug register (hdr)).

The following table describes the digital input function modes of the CP384.

Table 2-3: Digital Input Function Modes of the CP384

MODE	DESCRIPTION
Event hit	The CP384 monitors the input ports and detects any change in their state: - Whenever individual input channels are enabled they are monitored. - The direction of the change-of-state may be set. - A status register reports the detected events.
Latch hit	In addition to standard event detection (i.e. event-hit) there is a latch mode extension. This mode is used in the event that it is necessary to capture the inputs when a defined event has occurred.
Compare hit	It is possible to detect a complete input pattern automatically. The input vector is continuously compared with the content of the mask register. Single inputs may also be individually masked out.

The system failure indicators regarding undervoltage and overvoltage are made available to the DIO ProComm Controller, and are automatically reset by the voltage supervisor circuit once the condition has been corrected.

An input signal (Reset) is available to set an inactive state for each individual output cluster and also to shut down each individual output cluster during operation as necessary.

2.10 Software

Driver software is available for the System Master application software.

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Chapter 3

Installation

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3. Installation

The CP384 has been designed for easy installation. However, the following standard precautions, installation procedures, and general information must be observed to ensure proper installation and to preclude damage to the board or injury to personnel.

3.1 Hardware Installation

The product described in this manual can be installed in any available 3U slot of a CompactPCI system except for the system master slot.

3.1.1 Safety Requirements

The board must be securely fastened to the chassis using the two front panel retaining screws located at the top and bottom of the board to ensure proper grounding and to avoid loosening caused by vibration or shock.

In addition, the following electrical hazard precautions must be observed.



Caution, Electric Shock Hazard!

Ensure that the system main power is removed prior to installing or removing this board. Ensure that there are no other external voltages or signals being applied to this board or other boards within the system. Failure to comply with the above could endanger your life or health and may cause damage to this board or other system components including process-side signal conditioning equipment.



ESD Equipment!

This Kontron board contains electrostatically sensitive devices. Please observe the following precautions to avoid damage to your board:

Discharge your clothing before touching the assembly. Tools must be discharged before use.

Do not touch any onboard components, connector pins, or board conductive circuits.

If working at an anti-static workbench with professional discharging equipment, ensure compliance with its usage when handling this product.

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3.1.2 Installation Procedures

To install the board proceed as follows:

1. Ensure that the safety requirements indicated above are observed.



Warning!

Failure to comply with the instruction below may cause damage to the board or result in improper system operation. Please refer to chapters 4 and 5 for configuration information.

2. Ensure that the board is properly configured for operation before installing.



Note ...

Care must be taken when applying the procedures below to ensure that when the board is inserted it is not damaged through contact with other boards in the system.

3. To install the board perform the following:
   1. Prior to installation of the board disengage the insertion/extraction handle by first unlocking the handle and pressing it down.
   2. Insert the board into an appropriate slot, and, using the insertion/extraction handle, ensure that it is properly seated in the backplane. (Front panel is flush with the rack front; the insertion/extraction handle is locked.)
4. Fasten the front panel retaining screws.
5. Connect external interfacing cables to the board as required.
6. Ensure that the interfacing cables are properly secured.



Warning!

Proper and safe operation of the CP384 Digital Input and Digital Output Controller depends on the correct configuration of the external voltage and loads. System integrators must ensure that all voltages presented to the CP384 comply with the specifications set forth in this manual.

Failure to comply with the above may cause damage to the board or result in improper system operation. Please refer to chapters 4 and 5 for configuration information.

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3.1.3 Removal Procedures

To remove the board proceed as follows:

1. Ensure that the safety requirements indicated above are observed.



Warning!

Care must be taken when applying the procedures below to ensure that when the board is removed it is not damaged through contact with other boards in the system.

2. Disconnect any interfacing cables that may be connected to the board.
3. Loosen both of the front panel retaining screws.
4. To remove the board from the backplane perform the following:
    1. Unlock the insertion/extraction handle by pressing down on the grey locking mechanism in the middle of the handle. (This should be achievable with a minimum of force. If necessary lift the handle up slightly while pressing down on the grey locking mechanism.)
    2. Disengage the board from the backplane by pressing down on the insertion/extraction handle and pull the board out of the slot ensuring that the board does not make contact with adjacent boards. (If the handle does not move, it is not unlocked. Repeat the unlocking procedure above and try again. Do not use force!)
5. Dispose of the board as required observing applicable environmental regulations governing the handling and disposition of this type of product.

3.2 Software Installation

Installation of the CP384 driver software is a function of the application operating system. For further information refer to the appropriate software documentation.

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Chapter 4

Configuration

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4. Configuration

This chapter provides information for configuring the CP384 board for operation.

4.1 Jumper Settings

The CP384 does not have any jumpers which require configuring.

4.2 Digital Input Signal Requirements

In addition to the input signal type and its range, which have been specified in table 1-4, system integrators must be aware of certain input configuration requirements for the CP384. The following paragraphs provide information regarding individual connection configuration requirements.

4.2.1 Channels

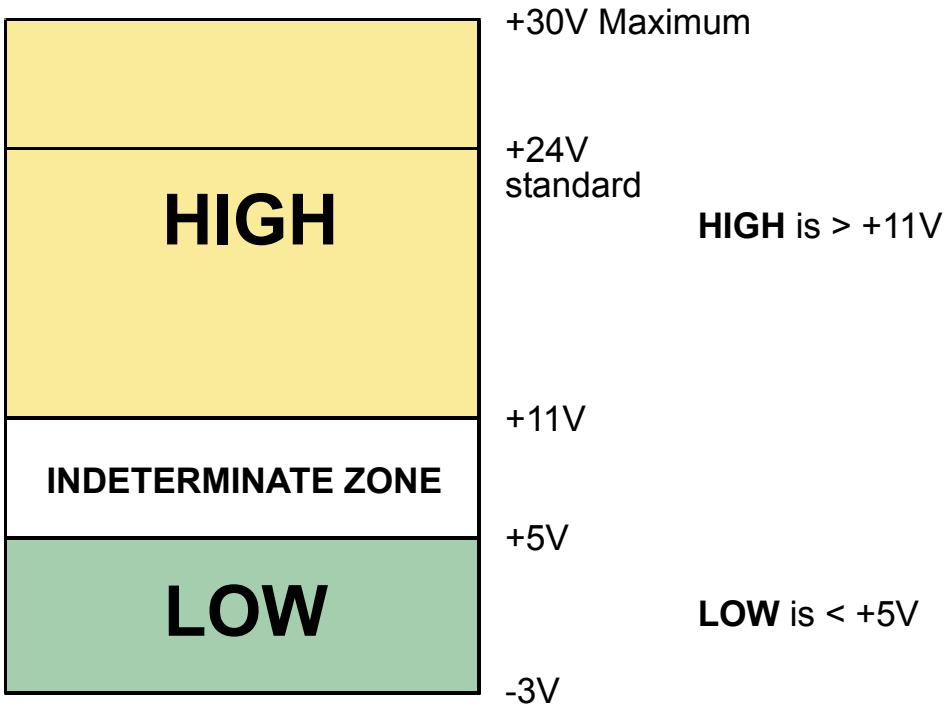
The CON2 connector of the CP384 provides two input pins per channel. This allows each channel to be configured separately as required. This is illustrated in figure 2-2, which shows the front panel connector pinout, with the 16 input channels shown starting at the top of the connector with channel 0 (DIGIN cluster).

The following sections address the basic requirements.

4.2.2 Signal Characteristics

The signals are differential and the specified voltage ranges illustrated in the following figure should be observed.

Figure 4-1: Voltage Ranges

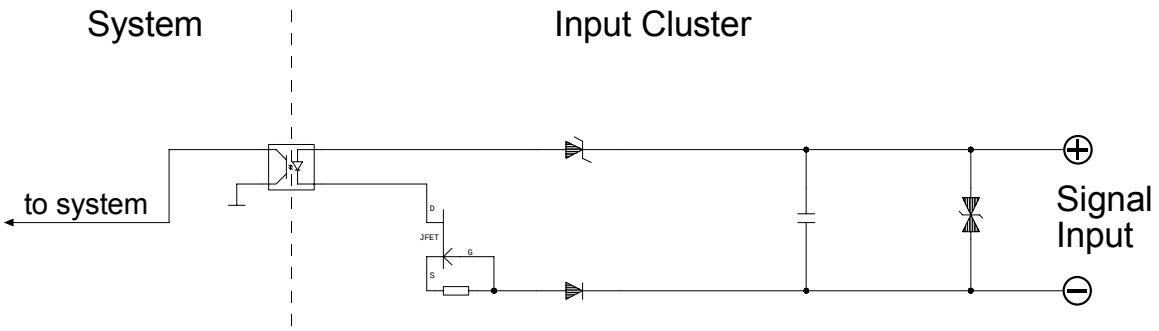


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4.2.3 Channel Configuration

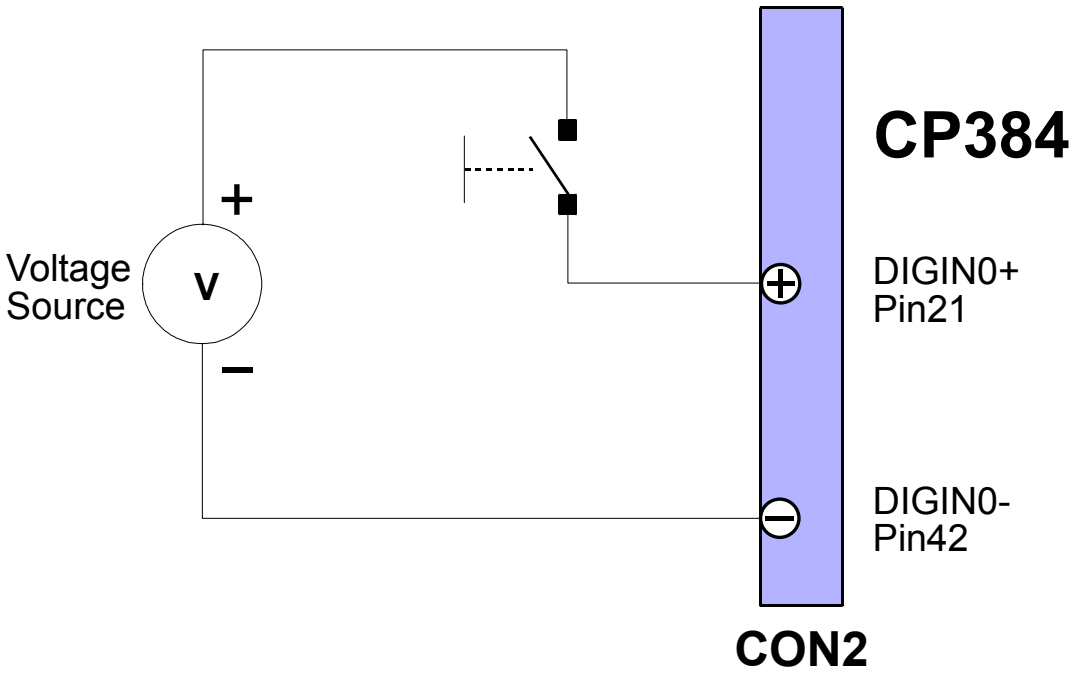
The following figure illustrates the typical schematic of an input channel.

Figure 4-2: Input Channel Schematic



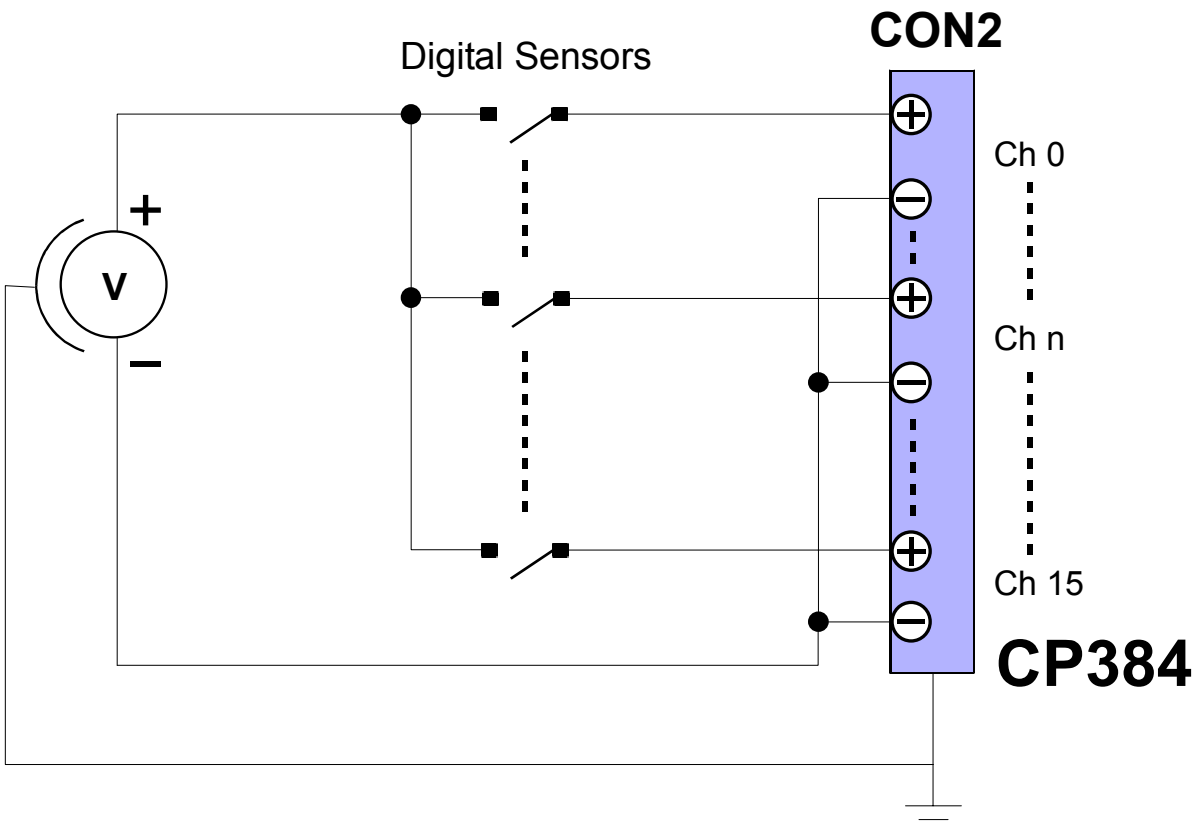
Signal inputs are required to be connected: plus to plus, minus to ground as shown in figure 4-3 below.

Figure 4-3: Input Configuration (Example for Channel 0)



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Figure 4-4: Configuration Diagram for All Input Channels



4.3 Digital Output Signal Properties

In addition to the output signal type and its range, which have been specified in table 1-5, system integrators must be aware of certain output configuration requirements for the CP384. The following paragraphs provide some information regarding individual connection configuration requirements.

4.3.1 Channels

The CON2 connector of the CP384 provides two output pins per channel. This is illustrated in figure 2-2, which shows the front panel connector pinout with the 8 output channels shown starting at the middle of the connector with channel 0.

The following sections address the basic requirements.

4.3.2 Connection of External Supply

The CP384 requires an external voltage for operation. This external power source supplies the board internal circuits for the relay coils, their drivers, and the voltage supervisor. The digital output channels are galvanically isolated from the external power supply.

The input connection for this voltage is realized via the 62-pin front panel connector CON2. The pinout of this connector is provided in table 2-1.

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4.3.3 Channel Connection

The following diagrams illustrate the external connection of the CP384 to the application.

Figure 4-5: Digital Output Connectionr

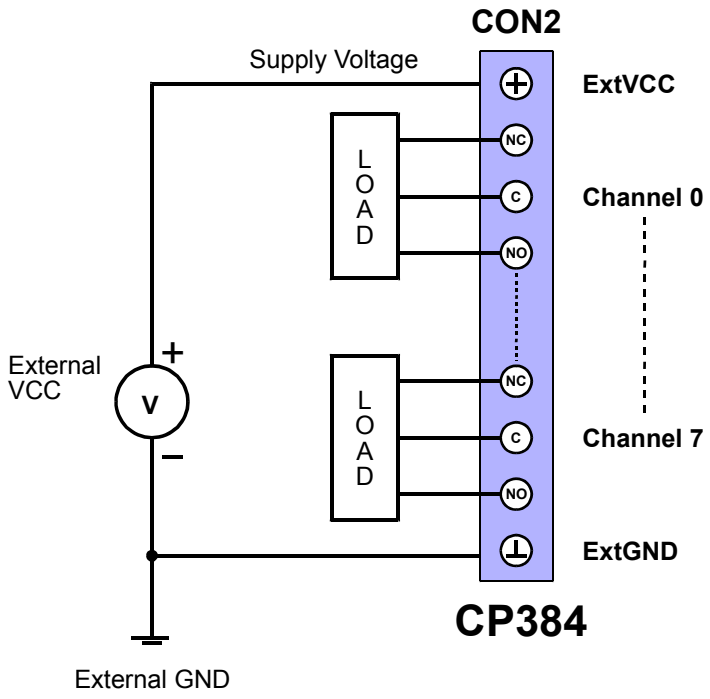
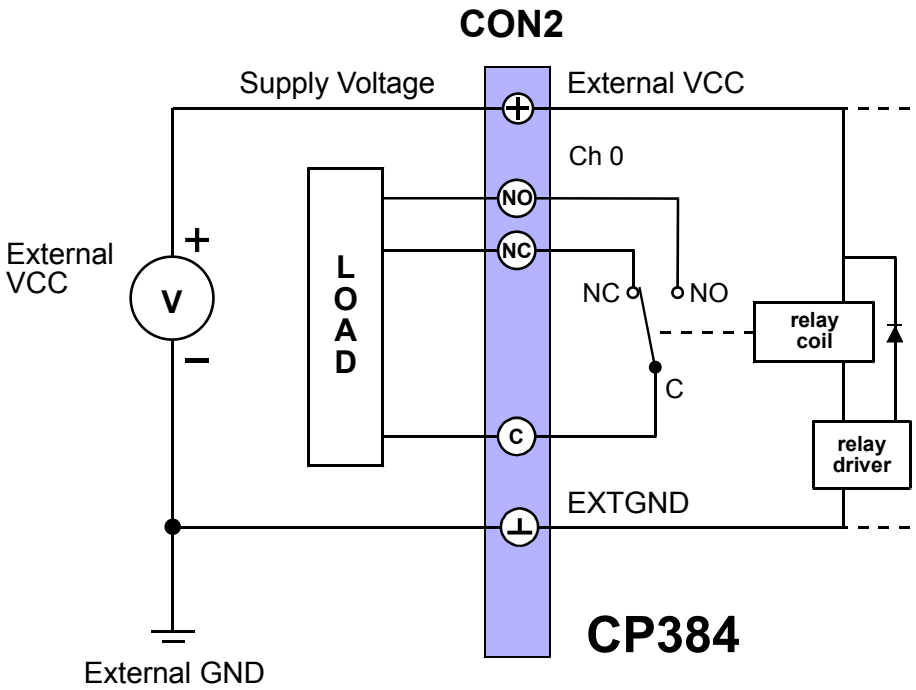
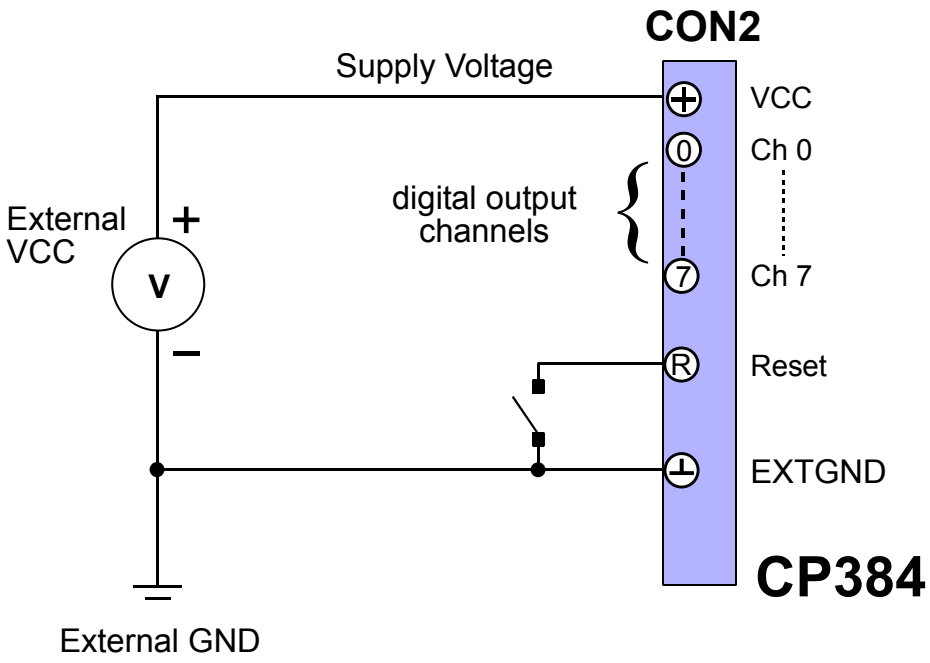


Figure 4-6: Digital Output Circuit



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Figure 4-7: External Reset Connection



Note ...

The voltage source for the cluster is an external supply in the range 24V DC ± 20%, and it supplies only the power to drive the relay control circuits, but not the output channels themselves.

The channel output pins are galvanically isolated from the VCC within the CP384 board.

4.4 Programming Interface

4.4.1 Access Control Logic (Address Decoder)

All the resources of the CP384 are mapped within the 64 kB PCI memory address space which itself is set in the PCI configuration register BAR0. The port size of all local or backend registers is 32-bit by default. The address map of the registers is as follows.

Table 4-1: Backend Register Address Map

BASE ADDRESS (BAR0)	SIZE	FUNCTION	
+ 0x0000	**4 kB**	**COMMON BOARD REGISTER**	
0x0400	32 bit	g_irq	General Interrupt Enable Register
0x0800	32 bit	hsr	Hardware Status Register
0x0804	32 bit	i_pen	General Interrupt Pending Register
0x0C00	32 bit	hdr	Hardware Debug Register
+ 0x1000	**4 kB**	**CAPABILITY ROM, SERIAL EEPROM**	
0x1000	32 bit	r_cmd	Command Register
0x1400	32 bit	r_ctl	Control Register
0x1800	32 bit	r_sta	Status Regsiter
0x1C00	32 bit	r_dat	Data Register
+ 0x2000	**4 kB**	**DIGOUT CLUSTER**	
0x2400	32 bit	o_ctl_a	Output Control Register
0x2800	32 bit	o_sta_a	Output Status Register
0x2C00	32 bit	o_dat_a	Output Data Register
+ 0x4000	**4 kB**	**DIGIN CLUSTER**	
0x4400	32 bit	i_ctl	Input Control Register
0x4408	32 bit	i_irquen	Input Irq Enable Register
0x440C	32 bit	e_pol	Input Event Polarity Register
0x4410	32 bit	e_msk	Input Event Mask Register
0x4414	32 bit	e_len	Input Latch-on Event Register
0x4418	32 bit	c_cmp	Input Pattern Compare Register
0x441C	32 bit	c_msk	Input Pattern Mask Register
0x4800	32 bit	i_event	Input Status Register
0x4C00	32 bit	d_in	Input Data Register
0x4C04	32 bit	input	Transparent Input Data
+ 0x5000	**44 kB**	**Reserved**	

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4.4.2 Reading Input Data

The input ports are made visible via the Input Data Register. This register reflects the inputs after them having passed the digital programmable debouncer. An active input appears there as a logical "1" whereas an open or inactive input port appears as a logical "0". The bit ordering naturally corresponds with the numbering of the input ports at the connector.

Table 4-2: Input Data Register

BITS	TYPE	DEFAULT	FUNCTION
31-16	r	0	Reserved
15-0	r	-	Input (debounced)



Note ...

Where the enhanced features such as interrupts, pattern or event detection are not required, only the input data register is relevant.

Table 4-3: Transparent Input Data Register

BITS	TYPE	DEFAULT	FUNCTION
31-16	r	0	Reserved
15-0	r	-	Input (transparent)



Note ...

In addition to the Input Data Register, there is a second non-latched input register (debouncer bypassed).

4.4.3 Debouncing Inputs

By default, all inputs are filtered through a passive analog low-pass filter placed immediately behind the input connector. Additionally, the CP384 provides a programmable digital debouncer which is common for all inputs. The input ports are sampled at a programmable sample rate which is derived from PCI bus clock. Two consecutive samples must be equal before being stored in the input data register. By this means, bouncing and spikes on inputs can be filtered out. For example, with a selected input sample rate of 500 Hz, input pulses which are shorter than 2 ms are filtered out.

Table 4-4: Input Control Register

BITS	TYPE	DEFAULT	FUNCTION
31-8	R/W	0	RESERVED
7	r/w	0	Input enable
6	r/w	0	Event detect enable
5	r/w	0	Latch mode enable
4	r/w	0	Pattern detect enable
3	r/w	0	Reserved
2-0	r/w	000	Debounce control deb [2 ... 0]

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Note ...

The inputs are sampled through the debouncer after the Input Enable bit is set. Additional features such as event and pattern detection and latch mode are also enabled in the input control register, after being configured within the corresponding mode registers.

Table 4-5: Programmable Input Sample Rates

deb [2 ... 0]	CLOCK DIVIDER	INPUT SAMPLE CLOCK @ 33MHz PCI	INPUT SAMPLE PERIOD @ 33MHz PCI
000	1	33 MHz	30 ns
001	2^8	128 KHz	8 µs
010	2^10	32 KHz	32 µs
011	2^12	8 KHz	128 µs
100	2^14	2 KHz	0.5 ms
101	2^16	0.5 KHz	2 ms
110	2^18	125 Hz	8 ms
111	2^20	31 Hz	32 ms



Note ...

The clock divider default value is 1. In addition to the choice of debouncing filters, there is an analog filter implemented on the board with an edge frequency at 10 kHz.

4.4.4 Detecting Input Events

Detecting events on input means that the CP384 hardware can supervise the input ports upon their changing state and without being continuously polled. This mode is controlled by three control registers. In the Input Event Mask Register, individual input events can be enabled which should be monitored. In the Input Polarity Register the direction of the change-of-state is set. Detected events are reported in the corresponding Input Event Status Register.

Table 4-6: Input Event Mask Register

BITS	TYPE	DEFAULT	FUNCTION
31-16	r/w	0	Not used
15 - 0	r/w	1	Input event mask bits



Note ...

A set bit means that event detection is disabled for the corresponding input port.

Table 4-7: Input Event Polarity Register

BITS	TYPE	DEFAULT	FUNCTION
31-16	r/w	0	Not used
15 - 0	r/w	0	Input event polarity bits



Note ...

A bit setting of 0 bit means that an event is detected when the input port changes from 0 to 1 whereas a setting of 1 means that an event is detected when the input changes from 1 to 0.

Table 4-8: Input Status Register

BITS	TYPE	DEFAULT	FUNCTION
31	r/w	0	Input latch-on-event status flag
30	r/w	0	Input compare status flag
15 - 0	r/w	0	Input event status flags



Note ...

A set bit means that an event was detected on the corresponding input port. Events must be cleared by writing a "1" to the corresponding input event flag. Otherwise, consecutive events on the same input would no longer be detected.

4.4.5 Latching on Input Events

In addition to the standard event detection described above, there is a latch mode extension. This mode is used in cases where it is necessary to capture the inputs when one of the defined events occurs.

Table 4-9: Input Latch-on-Event Register

BITS	TYPE	DEFAULT	FUNCTION
31-16	r	0	Not used
15 – 0	r	0	Latch on event, enable bits to activate

Note ...



A set bit means that a detected event on the corresponding input is latched. If all bits are enabled, all inputs are latched immediately. To switch back from latch mode into active mode, all detected events and the input latch-on-event status flag have to be reset by writing a "1" to the corresponding bits in the Input Status Register.

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4.4.6 Comparing Input Patterns

In addition to the Event Detection Mode, it is also possible to detect a complete input pattern automatically. In this mode the input vector is continuously compared with the content of the Input Pattern Compare Register. In the case of a match a flag is set within the Input Status Register. Single inputs can also be masked out individually in the Input Pattern Mask Register.

Table 4-10: Input Pattern Mask Register

BITS	TYPE	DEFAULT	FUNCTION
31-16	r/w	0	Not used
15 - 0	r/w	1	Input event mask bits



Note ...

A set bit means that the corresponding input is masked out for pattern recognition. There is no special enable for pattern recognition since it is switched off by default as long as all mask bits are set.

Table 4-11: Input Pattern Compare Register

BITS	TYPE	DEFAULT	FUNCTION
31-16	r/w	0	Not used
15 - 0	r/w	1	Input pattern compare bits



Note ...

This register stores the input compare data. A compare match is reported within the Input Status Register (Bit 31). To reset a compare match, the status flag must be reset by writing a "1" to it and also the match condition must cease.

4.4.7 Writing Output Data

Table 4-12: Output Data Register

BITS	TYPE	DEFAULT	FUNCTION
31-8	r/w	0	Reserved
7-0	r/w	0	Data, 8-bit digit



Note ...

Output data is 8 bit; this register is read/write enable.

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Table 4-13: Output Control Register

BITS	TYPE	DEFAULT	FUNCTION
31-2	r/w	0	Reserved
1	r/w	0	irqen
0	r/w	1	Reset



Note ...

irqen is for enabling of a diagnostic interrupt.

The reset bit should be set to 0 to activate the cluster.

Table 4-14: Output Status Register

BITS	TYPE	DEFAULT	FUNCTION
31	r	0	Fail
30	r	0	Diag
29-0	r	0	Reserved



Note ...

The Diag status flag is the diagnostic bit from the external voltage supervisor; Fail is the latched Diag status flag.

4.4.8 Hardware Debug/Test Registers

These registers are for internal test and debug only. The Common Status Register contains logic version and PCB version. The Common Debug Register is a read/write register without any further functionality besides the front panel monitor and control LEDs.

Table 4-15: Hardware Debug Register

BITS	TYPE	DEFAULT	FUNCTION
31-2	r/w	0	Reserved
1	r/w	0	FAIL
0	r/w	0	RUN

Table 4-16: Hardware Status Register

BITS	TYPE	DEFAULT *	FUNCTION
31-16	r	0	Reserved
15-8	r	00	Reserved
7-0	r	01	Logic Version

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4.4.9 Generating Interrupts

For digital outputs, a detected fail flag set in the register can trigger an interrupt. For digital inputs, a detected event or in other words any event flag set in the Input Status Register can trigger an interrupt. Thus, any input can be enabled individually for interrupt generation.

Independent of the interrupt cause, a board interrupt is handled on the hardware level always in the same way.

After having set the input control registers where compare data and events are defined, interrupts can be enabled individually within the Input IRQ Enable Register. Within the interrupt service routine, interrupts should be handled as follows.

1. Check if the board is the cause of the interrupt (General Interrupt Pending is set).
2. If yes, check the reason for the interrupt by reading the fail flag in the output status register and by reading the digital input status register.
3. Reset the corresponding Flag by writing a "1" to a set status bit (fail) or to the Input Event Flag.
4. Reset the board's IRQ by resetting the General Interrupt Pending Bit by writing a "1" to that status bit.
5. Return from Interrupt.



Note ...

The board will continue issuing an interrupt until all interrupt sources are handled completely and no interrupt condition remains.

Table 4-17: General Interrupt Enable Register

BITS	TYPE	DEFAULT	FUNCTION
31	r/w	0	Board Interrupt Enable
30 - 0	r/w	0	Reserved



Note ...

A set bit means that the board's interrupt is enabled.

Table 4-18: General Interrupt Pending Register

BITS	TYPE	DEFAULT	FUNCTION
31	r/w	0	Board Interrupt Pending
29 - 0	r/w	0	Reserved



Note ...

A set bit means that the board's interrupt is pending. A board interrupt must be cleared by writing a "1" to the corresponding output irqen event flag.

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Table 4-19: Output Status Register

BITS	TYPE	DEFAULT	FUNCTION
31	r	0	Fail
30	r	0	Diag
29 - 0	r	0	Reserved

Table 4-20: Input IRQ Register

BITS	TYPE	DEFAULT	FUNCTION
31	r/w	0	Not used
30	r/w	0	Input compare interrupt enable
29 - 0	r/w	0	Input event interrupt enable

4.4.10 Programming the Board Capability ROM

The Board Capability ROM contains all the board data necessary to identify board, version, optional features, etc., and to setup the basic software. The BCR is implemented using a 4 kbit serial EEPROM of the type Microchip 93LC66.

(The contents list of the BCR is not described here.)

The serial interface of the device has been realized in hardware resulting in a very simple register based programming interface with command, control, status and data registers. All protocol and serial timing specifications are resolved by hardware.

Programming of the BCR is undertaken as follows: The control word is written into the ROM Control Register including command opcode and internal address. Then optional data (in case of Write action) is written into the ROM Data Register. Command execution is started by setting the Startbit in the ROM Command Register. Then Ready/Busy must be polled in the ROM Status Register. After reaching Ready status, the next command can be set up and data (in case of Read action) can be fetched from the ROM Data Register.

Table 4-21: ROM Command Register

BITS	TYPE	DEFAULT	FUNCTION
31	r/w	0	Startbit
30-0	r/w	00	Reserved



Note ...

The Startbit will be automatically reset as soon as an action is completed.

Table 4-22: ROM Control Register

BITS	TYPE	DEFAULT	FUNCTION
31-19	r/w	0	Reserved
17-16	r/w	00	Opcode
15-8	r/w	00	Reserved
8-0	r/w	00	Internal address (A8 ... A0)



Note ...

The commands READ, EWEN (Write Enable) and WRITE are sufficient for all purposes.

Table 4-23: Opcodes and Commands

OPCODE	A8 ... A0	COMMAND
00	11xxxxxxx	EWEN
10	xxxxxxxxx	READ
01	xxxxxxxxx	WRITE



Note ...

The EWEN (Erase and Write Enable) command must be executed once before the first write.

Table 4-24: ROM Status Register

BITS	TYPE	DEFAULT	FUNCTION
31	r/w	0	Busy/Ready
30-0	r/w	00	Reserved



Note ...

As soon as the Startbit is set the Busy/Ready bit becomes active (Busy=1). It remains set as long as the command is executed and is reset when command execution is complete.

Table 4-25: ROM Data Register

BITS	TYPE	DEFAULT	FUNCTION
31-8	r/w	0	Reserved
7-0	r/w	0	Data (for data read and write commands)

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Chapter 5

System Considerations

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5. System Considerations

5.1 Introduction

In addition to the basic specification requirements for the CP384 which have been addressed in chapter 4, system integrators need to be aware of the overall system environment and the application needs when designing the interfacing to the CP384. The following chapters address a number of more apparent considerations which should be addressed, but certainly not all of the possible situations which may be encountered. Many of the considerations presented here are recommendations, but some are definite requirements if the CP384 is to successfully achieve its purpose.

5.2 General

Care must be taken to ensure that proper grounding concepts are followed, and that the integrity of the grounding system within the application be maintained.

Input wire routing should avoid proximity to high voltage or current sources.

Where possible input wiring length should be kept as short as possible.

5.3 Shielding

Input cable shielding in general is recommended.

The requirements for shielding can be seen primarily as a function of the system design and environment, but empirical results must also be considered.

The CON2 connector has a metal housing which is connected to the CP384 shield and is isolated from the system ground.

Ensure that if shielding is used that it is not in anyway connected to the system ground.

5.4 Debouncing for Digital Inputs

On the CP384 it is possible to select from a number of debouncing times, dependant on the type of switches/sensors in use. For example, when using mechanical switches or relays to switch the input, bouncing will always occur and therefore debouncing is necessary. A debounce period may be selected from a range of values available, accessible via software in the register depending on the settle time. Where it is known that an application does not generate bouncing problems, the debounce period may be set to the default value.

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Table 5-1: Debouncing Periods

CLOCK DIVIDER	INPUT SAMPLE CLOCK @ 33 MHz PCI CLK	INPUT SAMPLE PERIOD @ 33 MHz PCI CLK
1 (default value - see note below)	33 MHz	30 ns
2^8	128 kHz	8 µs
2^10	32 kHz	32 µs
2^12	8 kHz	128 µs
2^14	2 kHz	0.5 ms
2^16	0.5 kHz	2 ms
2^18	125 Hz	8 ms
2^20	31 Hz	32 ms



Note ...

The clock divider default value is 1. In addition to the choice of debouncing filters, there is an analog filter implemented on board with an edge frequency at 10 kHz.

5.5 Process-Side Signal Conditioning for Digital Inputs

Input signals presented to the CP384 must be within the ranges specified for signals in table 1-4 or erroneous results will occur as well as possible damage to the CP384.

5.6 External Power Supply for Digital Outputs

Voltage sources presented to the CP384 must be within the ranges specified in table 1-5 or erroneous results will occur as well as possible damage to the CP384.

In addition to the external supply of the input voltage for the relay logic parts which are linked to the digital outputs, the operational voltages for the outputs must also be supplied externally.

5.7 Cable Interfacing

No modification to the CP384 itself is permitted.

If necessary, cabling to the CP384 CON2 connector should be physically fixed to prevent strain on the CON2 connector.



Warning!

Each channel has a maximum current of 0.5 A. In situations where many channels are carrying a high current, separate, larger gauge cables for the external power supply should be used.

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