CP6923 USER GUIDE

6U CPCI Ethernet Switch with 24 Channels

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Final disposition of this product after its service life must be accomplished in accordance with applicable country, state, or local laws or regulations.

Explanation of Symbols



CE Conformity

This symbol indicates that the product described in this manual is in compliance with all applied CE standards. Please refer also to the section “Applied Standards” in this manual.



Caution, Electric Shock!

This symbol and title warn of hazards due to electrical shocks (> 60V) when touching products or parts of them. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your material.

Please refer also to the section “High Voltage Safety Instructions” on the following page.



Warning, ESD Sensitive Device!

This symbol and title inform that electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Please read also the section “Special Handling and Unpacking Instructions” on the following page.



Warning!

This symbol and title emphasize points which, if not fully understood and taken into consideration by the reader, may endanger your health and/or result in damage to your material.



Note...

This symbol and title emphasize aspects the reader should read through carefully for his or her own advantage.

For Your Safety

Your new Kontron product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new Kontron product, you are requested to conform with the following guidelines.

Safety Instructions



Warning!

All operations on this device must be carried out by sufficiently skilled personnel only.



Warning!

Do not connect a switch port to a telephone line.



Warning!

For intallation in a Hot-Plug system, observe the safety instructions specific to the system. Read the relevant documentation.



Caution, Electric Shock!

High voltages are present inside the chassis when the unit's power cord is plugged into an electrical outlet. Turn off system power, turn off the power supply, and then disconnect the power cord from its source before removing the chassis cover. Turning off the system power switch does not remove power to components.



Caution, Laser Light!

Laser light from fiber-optic transmission cables and components can damage your eyes. The laser components plugged into the switch are Class 1 laser components. Class 1 laser is considered incapable of producing damaging radiation levels during normal operation or maintenance.

To avoid damaging your eyes and to continue safe operation in case of abnormal circumstances:

- Never look directly into the outlets of fiber-optic transmission components or fiber-optic cables with unprotected eyes.
- Never allow fiber-optic transmission path to operate until all the connections have been made.
- Always fit protective plugs to any unused ports of the switch.

Special Handling and Unpacking Instructions



ESD Sensitive Device!

Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing mezzanines, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory back-up, ensure that the board is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the board.

General Instructions on Usage

In order to maintain Kontron's product warranty, this product must not be altered or modified in any way. Changes or modifications to the device, which are not explicitly approved by Kontron AG and described in this manual or received from Kontron's Technical Support as a special handling instruction, will void your warranty.

This device should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This applies also to the operational temperature range of the specific board version, which must not be exceeded. If batteries are present their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, please follow only the instructions supplied by the present manual.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the board please re-pack it as nearly as possible in the manner in which it was delivered.

Special care is necessary when handling or unpacking the product. Please, consult the special handling and unpacking instruction on the previous page of this manual.

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If the customer's eligibility for warranty has not been voided, in the event of any claim, he may return the product at the earliest possible convenience to the original place of purchase, together with a copy of the original document of purchase, a full description of the application the product is used on and a description of the defect. Pack the product in such a way as to ensure safe transportation (see our safety instructions).

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Chapter 1

Introduction

1. Introduction

1.1 Product Overview

The Kontron CP6923 is a PICMG 2.16 compliant Standard Fabric 6U CompactPCI managed Gigabit Ethernet Switch with up to 26 ports.

Three different base variants of the CP6923 are available:

- CP6923-C (Copper)
  In addition to the 20 backplane links (19 node boards and one fabric board), four GbE switch ports are available on the front plate via RJ45 connectors.
- CP6923-O (Optical)
  In addition to the 20 backplane links (19 node boards and one fabric board), four front plate ports are implemented as SFP cages, two 10 GbE ports are accessible via XFP cages.
- CP6923-R (Rear)
  All 24 GbE ports connect to the backplane (four additional extended node board links).

The three base variants are designed to be operated in a standard environment (rugged level R1). The CP6923-R variant is additionally available in two ruggedized versions (rugged level R2 and R3). The three rugged levels are defined as follows:

- Rugged level R1 (CP6923-C, CP6923-O, CP6923-R):
  Standard temperature range of 0°C to +55°C, standard shock and vibration resistibility (20G)
- Rugged level R2 (CP6923-R-R2-E2):
  Extended temperature range of -40°C to +85°C, increased shock and vibration resistibility (30G)
- Rugged level R3 (CP6923-R-R3-E2):
  Extended temperature range of -40°C to +85°C, increased shock and vibration resistibility (40G), conduction cooling

1.1.1 CP6923 Features

The board is composed of the following building blocks:

- Ethernet Infrastructure
- Ethernet Switch Controller and Memory
- IPMI
- Power Supply

Ethernet Infrastructure

- Broadcom StrataXGS®III Chip
  - BCM56500: 24 Port Gigabit Ethernet Layer-3 Switch (CP6923-C, CP6923-R)
  - BCM56502: 24 Port Gigabit Ethernet Layer-3 Switch with 2 10GbE Uplinks (CP6923-O)
- PCI 32b/66MHz Management IF

- Line rate switching for all packet sizes and conditions
- Supports 19x Link Ports to Node boards [10/100/1000Base-T via external Copper PHY]
- Supports 1x Link Port to Fabric board [10/100/1000Base-T via external Copper PHY].
- Supports optional 4x 10/100/1000Base-T Copper based uplinks to front (CP6923-C).
- Supports optional 4x 1GbE SFP uplinks to front (CP6923-O).
- Supports optional 2x 10GBase-R XFP uplinks to front (CP6923-O).
- Supports 4x Link Ports to extended Node boards [10/100/1000Base-T via external Copper PHY] to rear (CP6923-R)
- Broadcom BCM5488 OctalPHY for copper based links
- Broadcom BCM8704 single 10GbE PHY for uplinks (CP6923-O)

Ethernet Switch Controller and System Memory

- Socketless PowerPC IBM PPC405GPr 400 MHz
- Used for switch provisioning, diagnostics and protocol handling
- 256 MBytes SDRAM 133 MHz
- 64 MBytes FLASH

IPMI

- Renesas H8S2166 16-bit µController (PM)
- PICMG 2.9 / IPMI 1.5 compliant
- Renesas R5F21144 Firmware Update Manager (FUM)
- 512 kByte Flash (Boot Image)
- 64 kByte PROM (FRU)
- Voltage, current monitoring with ADC of PM
- Temperature monitoring with LM83

Power Supply

- 5V and 3.3V only board, no 12V or -12V required
- IPMB_PWR or 5V used for 3.3V PM (generated by LDO)
- Hot Swap support
- PoL converter with 2.5V, 1.8V, 1.25V and 1.0V

Miscellaneous

- Management connection to Switch Controller (CLI, SNMP) via RS232 and Fast Ethernet via RJ45 connectors
- Management connection to Switch Controller via RS232 on J4
- Serial EEPROM for FRU storage (serial ID)
- Board support package includes Montavista or Wind River Linux, device drivers, protocol stacks and diagnostics

- Metalwork compliant to PICMG® 2.0 6U/4HP (233.35 mm by 160 mm) / (20.32 mm typ.)



Note…

SFP and XFP modules are not included with the CP6923-O. An application note with a list of SFP and XFP modules successfully operated in the CP6923-O is available upon request.

1.1.2 General compliances

The CP6923 is conform to the following specifications:

- PICMG® 2.0 R3.0 CompactPCI® Specification, as amended by ERN 2.0-3.0-002
- PICMG® 2.1 R2.0 CompactPCI® Hot Swap Specification
- PICMG® 2.5 R1.0 CompactPCI® Computing Telephony Specification
- PICMG® 2.9 R1.0 CompactPCI® System Management Specification
- PICMG® 2.10 R1.0 Keying of CompactPCI® System Management Specification
- PICMG® 2.16 R1.0 Sep. 5, 2005 Packet Switching Backplane Specification
- Intelligent Platform Management Interface Specification V1.5
- IEEE 802.3, 2000
- IEEE 802.3ae 2002
- Small Form-factor Pluggable (SFP) Transceiver MultiSource Agreement (MSA), Sept. 14th, 2000
- SFF Committee, INF-80077i, rev. 4.0, 10 Gigabit Small Form Factor Pluggable Module (XFP)
- ANSI/Vita 30.1-2002 American National Standard for 2mm Connector Equipment Practice on Conduction Cooled Euroboards (option)

1.1.3 Hot Swap Capability

The board supports Full Hot Swap capability as required by PICMG 2.1 R2.0. It can be removed or inserted in a powered slot. Please refer to the PICMG 2.1 R2.0 specification for additional details.

1.2 Optional Accessories

1.2.1 RIO Module

The Kontron CP-RIO6-923 provides additional GbE switch ports and out-of-band management access via RS232. With an appropriate backplane, all switch ports of the CP6923 that connect to the backplane can be accessed using the RIO module.

For more information on the CP-RIO6-923, see chapter 3.2.

1.3 Technical Specification

Table 1-1: CP6923 Main Specifications

CP6923	SPECIFICATIONS
Mechanical	• 6U/4HP form factor mechanically compliant to PICMG 2.0 • 233.35 mm x 160 mm • Weight (R1): 520g • Weight (R2): 680g • Weight (R3): 780g
Power Requirements	• Maximum: 50W • Operating Voltage: 5V (5A max.), 3.3V (7A max.)
Temperature	• Operating (R1): 0°C to 55°C • Operating (R2/R3): -40°C to 85°C • Storage: -50°C to 105°C
Humidity	• Operating: 93% RH at 40°C, non-condensing • Storage: 5% - 95%, non-condensing
Altitude	• Operating (R1/R2): 15,000 ft (additional cooling might be required above 6,000 ft) • Operating (R3): 60,000 ft • Storage: 60,000 ft
Vibration	• Operating (R1): 5Hz to 100Hz Power Spectral Density (PSD)= 0.04 g²/Hz • Operating (R2): 5Hz to 100Hz PSD increasing at 3dB/octave 100 Hz to 1000 Hz PSD = 0.04g²/Hz 1000Hz to 2000Hz PSD decreasing at 6dB/octave • Operating (R3): 5Hz to 100Hz PSD increasing at 3dB/octave 100 Hz to 1000 Hz PSD = 0.1g²/Hz 1000Hz to 2000Hz PSD decreasing at 6dB/octave
Shock	• Operating (R1): 20G/11ms • Operating (R2): 30G/11ms • Operating (R3): 40G/11ms
Safety	• CB report to IEC 60950-1 • complies with EN/CSA/ UL 60950-1
EMC	• FCC 47 CFR Part 15, Subpart B • EN55022, EN55024 • EN 300 386
WEEE	Compliant to: • Directive 2002/96/EC: Waste electrical and electronic equipment

Table 1-1: CP6923 Main Specifications (Continued)

CP6923	SPECIFICATIONS
RoHS	Compliant to: • Directive 2002/95/EC: Restriction of the use of certain hazardous substances in electrical and electronic equipment
Reliability	• MTBF acc. to Telcordia SR-332, Issue 1 (30°C): > 198,000 hours • MTBF acc. to MIL-HDBK-217 FN2 (Ground Benign 25°C): > 149,000 hours

LEDs	• IPMB Status LED
	  • Hot Swap LED
	  • "Healthy" and "Activity" LED (LED 1 and 2, green)
	• Gigabit Ethernet Link Port Status LED
	  • 20 LEDs (status indication for standard fabric interfaces)
	• PowerPC 10/100BASE-T Management LEDs
	  • Green LED: Link/Activity
	  • Amber LED: Speed

Board Management	• based on IPMI 1.5 • FRU Management • Sensors (Voltage, Current, Temperature, Fuse) • Status and Alerting • Hot Swap Management • Local SEL



Note…

The indicated Shock and Vibration requirements for the CP6923-R-R2-E2 are met if appropriate measures are taken. These include using guide rails with a clamping mechanism and removing all wires from front board connectors.

1.4 Software Support

The following table contains information related to software supported by the CP6923.

Table 1-2: CP6923 Software Specification

CP6923	SPECIFICATIONS
General	• Reliable field upgrades for all software components • Dual boot images with roll-back capability • Management via SNMP and Command Line Interface • System access via TELNET, SSH and serial line • Hot-Swap support (IPMI)
Ethernet/Bridging	• Static link aggregation (IEEE 802.3ad) • Classic and rapid spanning tree algorithms(IEEE 802.1D, IEEE 802.1w) • Multiple Spanning Tree (IEEE 802.S) • Quality Of Service on all ports (IEEE 802.1p) • Full Duplex operation and flow control on all ports (IEEE 802.3x) • Static MAC filtering • Port Authentication (IEEE 802.1X) • Auto negotiation of speeds and operational mode on all external copper GE interfaces as well as on all base fabric interfaces • Layer 2 multicast services using GARP/GMRP (IEEE 802.1p) • VLAN support including VLAN tagging (IEEE 802.3ac), dynamic VLAN registration with GARP/GVRP (IEEE 802.1Q) and Protocol based VLANs (IEEE 802.1v) • Double VLAN tagging • Port Mirroring
IP Routing	• Redundancy of routing functionality using a second switch hub board • IPv4 Forwarding on all base channels and connected uplink ports • Quality of service according to the DiffServ standards • ARP for all routable interfaces • ICMP for all routable interfaces • OSPF routing protocol version 2 • RIP routing protocol version 2 • VRRP (virtual router redundancy protocol) for transparent fail over of default routers • IGMP snooping
QoS	• CoS (Class of Service) • DifffServ (Differentiated Services) • ACL (Access Control List)

Table 1-2: CP6923 Software Specification (Continued)

CP6923	SPECIFICATIONS
IP Multicast	• DVMRP • PIM-DM • PIM-SM • IGMP (Internet Group Message Protocol) v2 and v3 • IGMP Proxy
Applications	• SNTP client for retrieving accurate time and date information • DHCP server • Onboard event management • Test and trace facilities • POST (power on self tests) diagnostics • Standards based SNMP implementation supporting SNMP v1, v2 and v3 for monitoring and management purposes • Persistent storage of configuration across restarts • Support for retrieving and installing multiple configurations • Support for startup configurations based on the cPCI SGA number (Shelf GeographicAddress)
Supported MIBS	• For a list of supported MIBs please see chapter 4.2
Bootloader	u-boot Version 1.1.2 • POST • multi image support • reliable field upgradable • H/W protected • KCS interface to PM • serial console support
Operating System	• MontaVista Linux Professional Edition 3.1 (for GA 2.xx SW releases) • Wind River PNE 1.5 (for GA 3.xx SW releases)

Chapter 2

Installation

2. Installation

The CP6923 has been designed for easy installation. However, the following standard precautions, installation procedures, and general information must be observed to ensure proper installation and to preclude damage to the board, other system components, or injury to personnel.

2.1 Safety Requirements

The following safety precautions must be observed when installing or operating the CP6923. Kontron assumes no responsibility for any damage resulting from failure to comply with these requirements.



Warning!

Due care should be exercised when handling the board due to the fact that the heat sink can get very hot. Do not touch the heat sink when installing or removing the board.

In addition, the board should not be placed on any surface or in any form of storage container until such time as the board and heat sink have cooled down to room temperature.



ESD Equipment!

This CompactPCI board contains electrostatically sensitive devices. Please observe the necessary precautions to avoid damage to your board:

- Discharge your clothing before touching the assembly. Tools must be discharged before use.
- When unpacking a static-sensitive component from its shipping carton, do not remove the component's antistatic packing material until you are ready to install the component in a computer. Just before unwrapping the antistatic packaging, be sure you are at an ESD workstation or grounded. This will discharge any static electricity that may have built up in your body.
- When transporting a sensitive component, first place it in an antistatic container or packaging.
- Handle all sensitive components at an ESD workstation. If possible, use antistatic floor pads and workbench pads.
- Handle components and boards with care. Do not touch the components or contacts on a board. Hold a board by its edges or by its metal mounting bracket.
- Do not handle or store system boards near strong electrostatic, electromagnetic, magnetic, or radioactive fields.



Warning!

Be careful when handling the CP6923. Some parts have sharp edges which might lead to injuries:

- The SFP cages of the CP6923-O.
- The heat sinks, especially the one of the CP6923-R-R2-E2.

2.2 CP6923 Initial Installation Procedures

The following procedures are applicable only for the initial installation of the CP6923 in a system. Procedures for standard removal and hot swap operations are found in their respective chapters.

To perform an initial installation of the CP6923 in a system proceed as follows:

1. Ensure that the safety requirements indicated in chapter 2.1 are observed.



Warning!

Failure to comply with the instruction below may cause damage to the board or result in improper system operation.

2. Ensure that the board is properly configured for operation in accordance with application requirements before installing. For information regarding the configuration of the CP6923 refer to the CLI Reference Manual.



Warning!

Care must be taken when applying the procedures below to ensure that neither the CP6923 nor other system boards are physically damaged by the application of these procedures.

3. To install the CP6923 perform the following:

   a. Ensure that no power is applied to the system before proceeding.
   b. Carefully insert the board into the slot designated by the application requirements for the board until it makes contact with the backplane connectors.



Warning!

DO NOT push the board into the backplane connectors. Use the ejector handles to seat the board into the backplane connectors.

   c. Using both ejector handles, engage the board with the backplane. When the ejector handles are locked, the board is engaged.
   d. Fasten the front panel retaining screws.
   e. Connect all external interfacing cables to the board as required.
   f. Ensure that the board and all required interfacing cables are properly secured.

4. The CP6923 is now ready for operation.



Warning!

During power-up, the 3.3V input power supply must be able to provide a minimum peak current of 10A to the CP6923. This applies for each CP6923 in a given systems.

Failure to comply with the above warning may result in damage to or improper operation of the CP6923.

2.3 Standard Removal Procedures

To remove the board proceed as follows:

1. Ensure that the safety requirements indicated in chapter 2.1 are observed.



Warning!

Care must be taken when applying the procedures below to ensure that neither the CP6923 nor system boards are physically damaged by the application of these procedures.

2. Ensure that no power is applied to the system before proceeding.
3. Disconnect any interfacing cables that may be connected to the board.
4. Unscrew the front panel retaining screws.



Warning!

Due care should be exercised when handling the board due to the fact that the heat sink can get very hot. Do not touch the heat sink when changing the board.

5. Disengage the board from the backplane by first unlocking the board ejection handles and then by pressing the handles as required until the board is disengaged.
6. After disengaging the board from the backplane, pull the board out of the slot.
7. Dispose of the board as required.

2.4 Software Installation

The CP6923 comes as a pre-installed system with all necessary OS, filesystem, drivers and applications factory-installed with default configurations.

Updating the Software with new operating system or applications or new versions is provided by a dedicated update mechanism, which is described in Chapter 4.

2.5 Quick Start

This section gives instructions for (initially) accessing the CLI (Command Line Interface) of the CP6923 using either in-band access via the ethernet fabric or the out-of-band management interfaces (serial port or Fast Ethernet) accessible from the front plate serial connector or via an appropriate RIO module. The CLI is required for configuring the GbE switch.

2.5.1 Out-of-Band CLI Access

The CLI can be accessed via serial port (using the front plate connector and provided adapter or an appropriate RIO module) or Fast Ethernet (via the front plate RJ45 connector).

2.5.1.1 Serial Port

The serial port is ready to use offhand without further configuration.

Port settings are:

- 9600 bps (serial speed might be different for customized board variants)
- 8 bit, no parity, 1 stop bit (8N1)
- no flow control

2.5.1.2 Fast Ethernet Serviceport

The Fast Ethernet serviceport on the CP6923 front plate has no IP address set by default, it is necessary to assign an IP address statically to the network port or enable dhcp on the serviceport. Because the required configuration steps are done in the CLI, an initial access using the serial port is required.

The procedure for assigning an IP address to the serviceport is described in the following. User input is printed in bold letters.

1. Connect to serial port on the front plate (using the Kontron DB9 adapter cable) or RIO module (using a RJ45 straight cable).
2. Ensure that the board is powered up.
3. Log in as admin and enter privileged mode by typing '**enable**' (no passwords required by default).

```
User:admin
Password:
(Ethernet Fabric) >enable
Password:

(Ethernet Fabric) #
```

4. Set IP address and netmask. (see below for an example IP address setting)

```
(Ethernet Fabric) #serviceport ip 192.168.50.107 255.255.255.0
```

The FE management interface is available from now on.

Alternatively, DHCP can be set for the serviceport

```
(Ethernet Fabric) #serviceport protocol dhcp
```

An IP address will be given to the serviceport by a DHCP server.

5. Save configuration by copying it to the flash, confirm by typing '**y**'

```
(Ethernet Fabric) #copy system:running-config nvram:startup-config

This operation may take a few minutes.
Management interfaces will not be available during this time.

Are you sure you want to save? (y/n) y

Config file 'current/startup-config' created successfully.

Configuration Saved!

(Ethernet Fabric) #
```

To access the CLI via Fast Ethernet serviceport, open a telnet connection to the configured IP address, port 23.

2.5.2 In-Band CLI Access

The GbE switch network port (in-band management access) on the CP6923 has no IP address set by default, it is necessary to assign an IP address either statically or by using DHCP to the network port. Because the required configuration steps are done in the CLI, an initial access using the serial port is required.

The procedure for assigning an IP address to the network port is described in the following. User input is printed in bold letters.

1. Connect to serial port on the front plate (using the Kontron DB9 adapter cable) or RIO module (using a RJ45 straight cable).
2. Ensure that the board is powered up.
3. Log in as admin and enter privileged mode by typing '**enable**' (no passwords required by default).

```
User:admin
Password:
(Ethernet Fabric) >enable
Password:

(Ethernet Fabric) #
```

4. Set IP address, netmask and default gateway. (see below for an example IP address setting)

```
(Ethernet Fabric) #network parms 192.168.50.107 255.255.255.0 192.168.50.254
```

The FE management interface is available from now on.

Alternatively, DHCP can be set for the network port

```
(Ethernet Fabric) #network protocol dhcp
```

An IP address will be given to the network port by a DHCP server.

5. Save configuration by copying it to the flash, confirm by typing '**y**'

```
(Ethernet Fabric) #copy system:running-config nvram:startup-config

This operation may take a few minutes.
Management interfaces will not be available during this time.

Are you sure you want to save? (y/n) y

Config file 'current/startup-config' created successfully.

Configuration Saved!

(Ethernet Fabric) #
```

To access the CLI via Fast Ethernet networkport, open a telnet connection to the configured IP address, port 23.

It might make sense to separate the management network from the data path by setting appropriate VLANs

For additional information on the system configuration, refer to the *CP6923 CLI Reference Manual*.

Chapter 3

Hardware Description

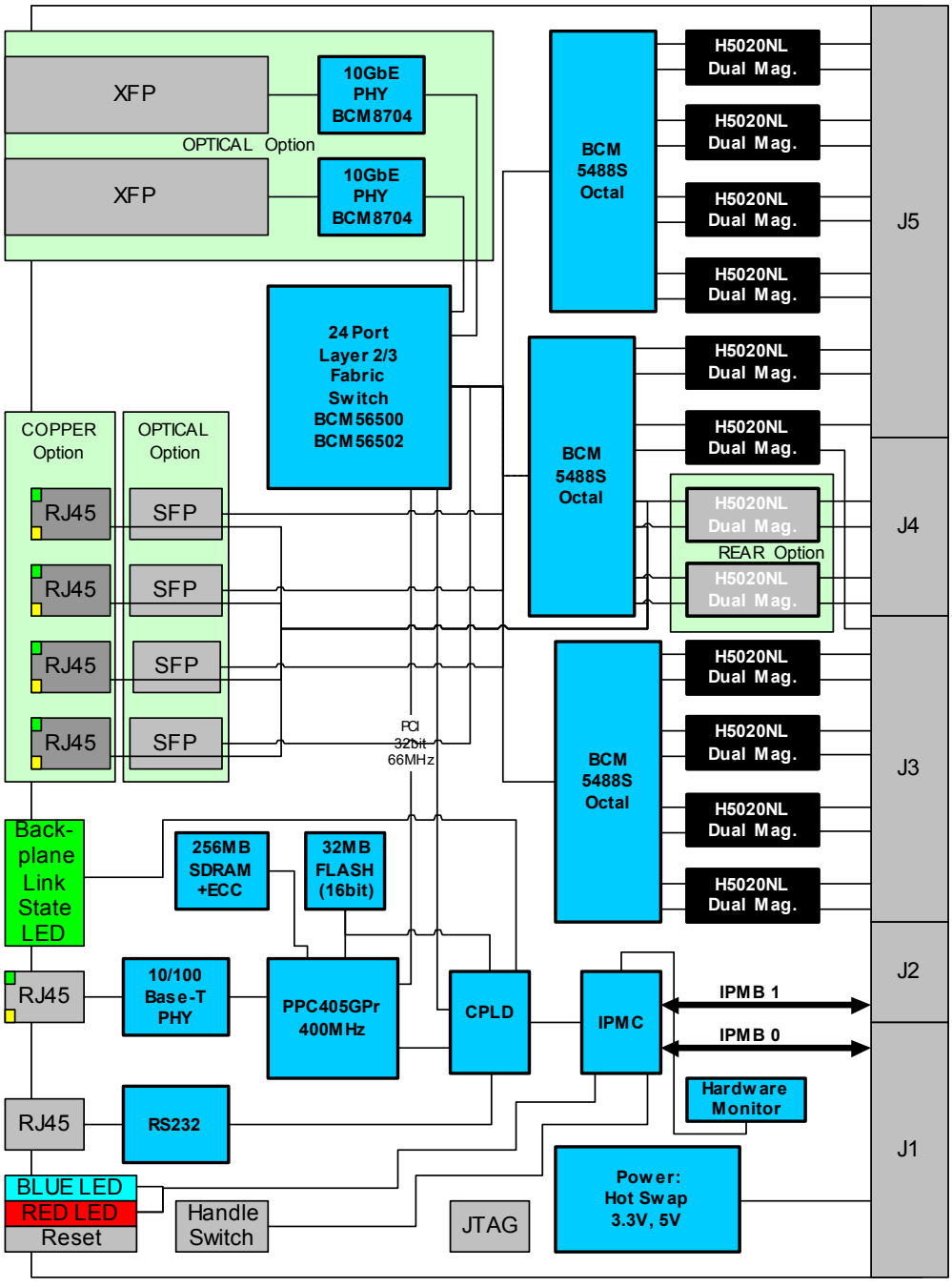
3. Hardware Description

This chapter describes the board specific items of the CP6923. Also described is the Rear-Panel I/O board CP-RIO6-923 used for management access and I/O extension.

3.1 Base Board

The base board is a standard Fabric 6U CompactPCI Gigabit Ethernet Switch with 24 channels.

Figure 3-1: Functional Block Diagram CP6923



The main building blocks of the CP6923 are:

- Fabric Switch
- CPU and Memory
- IPMI
- Power Supply with Hot Swap

3.1.1 Fabric Switch

The fabric switch is composed of a Broadcom Strata XGSIII 24 port GbE multilayer switch and three Broadcom BCM5488S octal 10/100/1000BASE-T PHYs. Two Broadcom BCM8704 10GbE PHYs are used in the CP6923-O variant. 20 Gigabit Ethernet Links are connected to the backplane, the four remaining GbE ports are used as 10/100/1000BASE-T Uplink ports (CP6923-C), SFP optical links (CP6923-O) or 4 additional extended fabric links (CP6923-R). The Broadcom Strata XGSIII switch supports SGMII to the PHYs. and SERDES interfaces to the SFP. Two types of Broadcom Strata XGSIII are currently defined:

- BCM56502, with advanced Layer 3 switching features for IPv4 and IPv6 routing (full featured) and 2 10GbE ports.
- BCM56500, with advanced Layer 3 switching features for IPv4 and IPv6 routing (full featured).

For details on the Broadcom Strata XGSIII features please refer to the corresponding datasheets.

3.1.1.1 PCI Interface

The PCI interface is a 32bit/66MHz system to control the fabric switch. The internal PCI arbiter of the PowerPC 405 GPr is used. There is no connection to the backplane.

3.1.1.2 Port Mapping

The CPCI interface numbering is according to the PICMG 2.16 Specification, labelled 1 to 23 (Node Slots) and F (other Fabric Slot). However, the on-board management software identifies the interfaces as 0/1 to 0/24. The CP6923-O has 2 additional interfaces, 0/25 and 0/26, for the 10GbE uplinks.



Note...

The CLI ID numbering is independent from the CPCI interface numbers and link LED indexes. This is due to layout considerations. The translation between CLI ID and Interface/LED numbers is given in the table below.

Table 3-1: Port Mapping

CLI ID	CP6923-C		CP6923-O		CP6923-R	
	Interface	LED	Interface	LED	Interface	LED
0/1	FL08	8	FL08	8	FL08	8
0/2	FL07	7	FL07	7	FL07	7
0/3	FL06	6	FL06	6	FL06	6
0/4	FL05	5	FL05	5	FL05	5
0/5	FL04	4	FL04	4	FL04	4
0/6	FL03	3	FL03	3	FL03	3
0/7	FL02	2	FL02	2	FL02	2
0/8	FL01	1	FL01	1	FL01	1
0/9	FL11	11	FL11	11	FL11	11
0/10	FL10	10	FL10	10	FL10	10
0/11	FL09	9	FL09	9	FL09	9
0/12	FL_f	F	FL_f	F	FL_f	F
0/13	Gig.Ethernet20	On RJ45	SFP20	SFP 20	FL20	20
0/14	Gig.Ethernet21	On RJ45	SFP21	SFP 21	FL21	21
0/15	Gig.Ethernet22	On RJ45	SFP22	SFP 22	FL22	22
0/16	Gig.Ethernet23	On RJ45	SFP23	SFP 23	FL23	23
0/17	FL19	19	FL19	19	FL19	19
0/18	FL18	18	FL18	18	FL18	18
0/19	FL17	17	FL17	17	FL17	17
0/20	FL16	16	FL16	16	FL16	16
0/21	FL15	15	FL15	15	FL15	15
0/22	FL14	14	FL14	14	FL14	14
0/23	FL13	13	FL13	13	FL13	13
0/24	FL12	12	FL12	12	FL12	12
0/25	-	-	XFP1	XFP 1	-	-
0/26	-	-	XFP2	XFP 2	-	-

Note...



- CP6923-R variants support Fabric Links 20 to 23 to the backplane
- CP6923-C supports Fabric Links 20 to 23 on the Frontpanel (RJ45, 1000Base-T)
- CP6923-O supports Fabric Links 20 to 23 on the Frontpanel (SFP, 1000Base-X) and 2 10GbE Uplinks via XFP

3.1.1.3 Standard Fabric Links

The board supports 19x 10/100/1000BASE-T Standard Fabric links and one 10/100/1000BASE-T link to the redundant CompactPCI Switch in the system (F-Link).

The pin assignment for J3 and J5 corresponds to the PICMG 2.16, see chapter 3.1.10.2 for a detailed pin assignment.

3.1.1.4 Extended Fabric Uplinks

The CP6923-R variant supports 4x10/100/1000BASE-T Extended Fabric links (FL20 to FL23) .

The pin assignment for J4 corresponds to the PICMG 2.16, see chapter 3.1.10.2 for a detailed pin assignment.

3.1.1.5 Copper Uplinks

The CP6923-C supports four 10/100/1000BASE-T RJ45 fabric switch uplinks to the front panel. The switch is connected to the RJ45 connectors with integrated magnetics and status LEDs on the front panel via external PHYs.

The RJ45 connectors have the following pin assignment (MDI-X hub mode).

Table 3-2: Copper Uplink RJ45 Pin Assignment

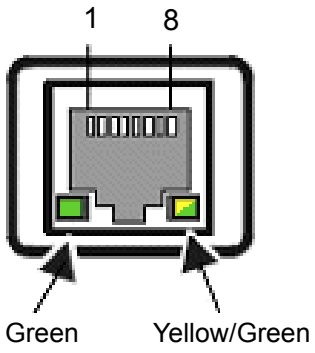
Contact	MDI-X	
1	BI_DB+	
2	BI_DB-	
3	BI_DA+	
4	BI_DD+	
5	BI_DD-	
6	BI_DA-	
7	BI_DC+	
8	BI_DC-	

Table 3-3: Copper Uplink LEDs Signification

Green LED (Link/Activity)	
OFF	Port did not perform linkup
ON	Port performed linkup but no activity
BLINKING	Port performed linkup and there is activity
Green/Yellow LED (Speed)	
OFF	10BASE-T
YELLOW ON	100BASE-Tx
GREEN ON	1000BASE-T

3.1.1.6 1000BASE-xX SFP Uplinks

The CP6923-O supports four Gigabit Ethernet SFP fabric switch uplinks to the front panel. The SFPs uplink ports are according the Small Form-factor Pluggable (SFP) Transceiver Multi-Source Agreement (MSA), Sept. 14th, 2000.



Note...

SFP modules are not included with the CP6923-O. An application note with a list of SFP modules successfully operated in the CP6923-O is available upon request.

The fabric switch controls the SFPs via an I²C bus. The SFP connectors have the following pin assignment:

Table 3-4: SFP Connectors Pin Assignment

Signal	Contact	Contact	Signal
GND	1	20	GND
TX_FAULT	2	19	TD-
TX_DIS	3	18	TD+
MODDEF2	4	17	GND
MODDEF1	5	16	3.3V TX
MODDEF0	6	15	3.3V RX
R_SEL	7	14	GND
LOS	8	13	RD+
GND	9	12	RD-
GND	10	11	GND



Caution! Laser Light

Do not look into the laser beam!
The SFP modules are fitted with a class 1 or 1M laser. To avoid possible exposure to hazardous levels of invisible laser radiation, do not exceed maximum ratings.

3.1.1.7 10GBASE-xX XFP Uplinks

The CP6923-O supports two 10 Gigabit Ethernet XFP Fabric Switch uplinks to the front panel. The fabric switch is connected via a BCM8704 10GbE transceiver to XFP connectors.

The BCM8704 is managed from the Fabric Switch XMDIO management interface (MDC/MDIO).

The XFP uplink ports are according the SFF Committee, INF-80077i, rev. 4.0, 10 Gigabit Small Form Factor Pluggable Module (XFP). XFP Modules with -5.0V are not supported.



Note...

XFP modules are not included with the CP6923-O. An application note with a list of XFP modules successfully operated in the CP6923-O is available upon request.

The XFP connectors have the following pin assignment.

Table 3-5: XFP Connectors Pin Assignment

Signal	Contact	Contact	Signal
GND	1	30	GND
NC	2	29	TD+
MOD_DE_SEL	3	28	TD-
INTERRUPT#	4	27	GND
TX_DIS	5	26	GND
5V	6	25	REFCLK-
GND	7	24	REFCLK+
3.3V	8	23	GND
3.3V	9	22	1.8V
SCL	10	21	PDWN/RST
SDA	11	20	1.8V
MOD_ABS	12	19	GND
MOD_NR	13	18	RD+
RX_LOS	14	17	RD-
GND	15	16	GND



Caution! Laser Light

Do not look into the laser beam!
The XFP modules are fitted with a class 1 or 1M laser. To avoid possible exposure to hazardous levels of invisible laser radiation, do not exceed maximum ratings.

3.1.2 CPU and Memory

The CPU is an IBM PowerPC 405 GPr 400MHz 32-bit RISC processor with 16KB D-cache.

3.1.2.1 SDRAM

The CPU operates with a 133MHz and 32 bit SDRAM interface. Five 256Mbit devices, soldered directly onto the PCB, provide 256 Mbyte of SDRAM plus 64 MByte for ECC.

3.1.2.2 FLASH

The CPU has 64Mbyte of Flash Memory. It is connected to the 16 bit peripheral data bus of the PowerPC 405 GPr.

The upper sectors containing the bootloader are write-protected. Jumper FWPD disables the protection, for additional information see chapter 4.5, for additional information concerning write protection, see chapter 3.1.6.

3.1.2.3 Fast Ethernet Management Interface

The internal Fast Ethernet MAC of the PowerPC 405 GPr is used as a management interface. A Fast Ethernet PHY transceiver and a RJ45 Connector with integrated magnetics and two LED's, located on the front panel, are used to complete the network interface.

The default setting of the PHY is to operate in auto-negotiation enabled mode, 10/100, Full or Half duplex. The LEDs indicate Link/Activity (LED: Green) and Speed (LED: Yellow).

The standard RJ45 connector has the following pin assignment:

Table 3-6: FE Management RJ45 Connector Pin Assignment

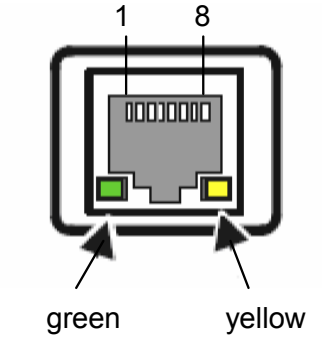
Pin	Function	
1	TX+	
2	TX-	
3	RX+	
4	NU	
5	NU	
6	RX-	
7	NU	
8	NU	

Table 3-7: FE Management LEDs Signification

Green LED (Link/Activity)	
OFF	Port did not perform linkup
ON	Port performed linkup but no activity
BLINKING	Port performed linkup and there is activity
Yellow LED (Speed)	
OFF	10BASE-T
ON	100BASE-Tx



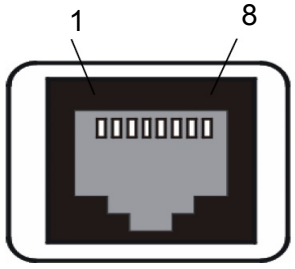
Warning!

The RJ45 connection on the CP6923-R-R3-E2 is for production porposes only and shall not be used by the customer. Connecting to this interface may lead to disfunction of the board.

3.1.2.4 RS232 Management Interface

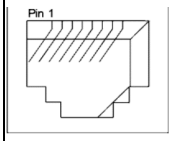
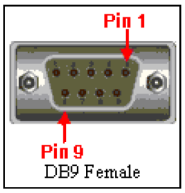
The UART0 interface of the PowerPC is connected to the front plate serial RJ45 port and also to the backplane connector J4. This allows accessing the RS232 management port using an appropriate RIO module.

Table 3-8: Serial Port (RJ45) Pin Assignment

Signal	Pin	
RTS	1	
DTR	2	
TXD	3	
GND	4	
GND	5	
RXD	6	
DSR	7	
CTS	8	

External connection is established with a straight through Ethernet cable and a RJ45 (female) to SubD (female) adapter if required. The adapter is described in table 3-9.

Table 3-9: Serial console terminal cable interface: RJ45 Female to DB9 Female

RJ45 Female	RJ45 Pin Number	Signal	Connected	Description	DB9 Pin Number	DB9 Female
 Front View	1	RTS	Y	Request To Send	8	 Front View
	2	DTR	Y	Data Terminal Ready	76	
	3	TXD	Y	Transmit	2	
	4	GND	N	Ground	-	
	5	GND	Y	Ground	5	
	6	RXD	Y	Receive	3	
	7	DSR	Y	Data Set Ready	4	
	8	CTS	N	Clear To Send	7	
	-	RI	N	Ring Indicator (Not Used)	9	
	-	DCD	N	Carrier Detect (Not Used)	1	

The pin assignment of the RIO RS232 connection is included in chapter 3.2.

3.1.3 IPMI

The CP6923 board supports an intelligent hardware management system, based on the Intelligent Platform Management Interface Specification 1.5. The hardware management system provides the ability to manage the power, cooling and interconnect needs of intelligent devices; to monitor events; and to log events to a central repository intelligent FRU (Field Replaceable Unit) contain a Peripheral Manager.

The main building blocks of the IPMI architecture of the CP6923 are:

- PM Peripheral Manager
- FUM Firmware Update Manager

3.1.3.1 PM

The Peripheral Manager is a 16-bit microcontroller for IPMI applications and it is compliant to IPMI version 1.5 specification. The microcontroller has large on chip memory of 512 Kbyte Flash and 40Kbyte SRAM. It provides six I²C interfaces to have access to the dedicated BMC A and B and the on board peripheral devices such as SEEPROM, temperature sensor and others.

One LPC interface for communication between PM and PPC over KCS protocol is implemented by CPLD. By default the PM is in reset until the FUM is alive.

A requirement for the PM is to monitor voltages and currents. The PM has 8 A/D converter inputs for monitoring.

3.1.3.2 FUM

The Firmware Update Manager (FUM) is a microcontroller with embedded 16Kbyte data flash ROM and 1Kbyte RAM.

The FUM is responsible for field upgrades, rollbacks and watchdog functions of the PM. The microcontroller provides four SPI compatible memory devices. Each memory device has 256kbyte memory space. Two devices contain the current firmware for the PM and the other two devices can be programmed with the new firmware for the PM. The FUM is able to update the PM during the normal operation of the board. In the case of a fault during the update process, the FUM can reconfigure the PM with the last version of firmware that is kept in its memory space. The FUM is also the watchdog timer for the PM. There are several control signals to supervise the PM.

3.1.4 Power Supply and Hot Swap

The CP6923 is supplied by the 3.3V and the 5.0V from the backplane. The PM on the CP6923 operates also with the IPMB_PWR from the backplane, when no other supply rails are available.

The CP6923 supports Hot Swap according PIGMG® 2.1 R2.0. All supply voltages from the backplane are enabled with a predefined ramp-up time. The inrush current is limited by Hot-Swap controllers.

3.1.4.1 Power Up and Power Down Sequencing

The CP6923 supports Hot Swapping and could be inserted into a live backplane. In this case the longest 3.3V and the longest 5V pins from the backplane are used to supply the management devices CPLD and PM.

When the board is totally seated into the slot and the handle is closed, an active BD_SEL# signal triggers the CPLD to start the payload power up sequence.

The power down sequence is initiated by opening the handle switch. When the payload voltages are disabled, the CPLD turns on the blue LED. The board can be removed.

3.1.4.2 Reset

The reset chain is based on seven elements. The first element in the chain is the voltage supply monitor, followed by the CPLD, FUM, PM, Payload voltage, PPC and finally the Fabric Interface.

The reset switch will perform a reset on the CPU when pressed for less than 1 second and a complete board reset (including IPMI) when pressed for more than 2 seconds.

3.1.5 Jumpers

The CP6923 provides one jumper for board configuration. When the Flash Write Protection Disable (FWPD) jumper is set, the bootloader code in the flash is unprotected. When it is removed (default setting), writing to the bootloader sectors is not possible.

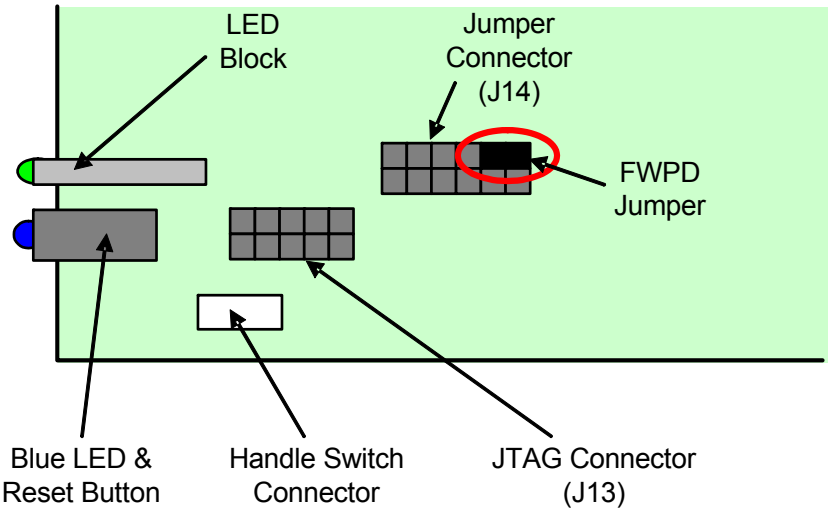
Warning!

Warning: For normal operation, the jumper is not required. Modifying or deleting the bootloader can leave the board inoperable.

The rugged variants of the CP6923 support a more extensive write protection mechanism which is described in chapter 3.1.6.

Following figure shows the position of the FWPD jumper on the CP6923.

Figure 3-2: Position of FWPD jumper in the lower left corner of the CP6923



Note that on the CP6923-R-R3-E2, not all elements shown are actually stuffed.

3.1.6 Write Protection Feature for Rugged Variants

The rugged variants CP6923-R-R2-E2 and CP6923-R-R3-E2 support hardware driven write protection for all non-volatile memories. Depending on the device, the protection is implemented either by a dedicated write protection signal, by disabling the write enable signal, or the whole interface.

Three levels of HW write protection are supported: unprotected, standard and enhanced write protection. The protection level is chosen by the combination of the state of on-board jumper (FWPD, see chapter 3.1.5) and a backplane signal (EWP). The backplane signal is located on connector J4, pin A9. If left open, the signal is inactive. If pulled to GND, the signal is active.

The following table shows how to configure the desired write protection level. Default setting is ‘standard’.

Table 3-10: Write protection level set by FWPD and EWP

FWPD Jumper	EWP Signal	Write Protection Level
set	don't care	unprotected
open	inactive (3.3V or open)	standard
open	active (GND)	enhanced

Standard write protection provides protection for SPD data and PowerPC Flash data, enhanced write protection provides protection for all memories.

Table 3-11: Non-volatile memories on the CP6923

Description	Size	Part Type	Protected by Level
CPU Bootloader + Firmware	64 MB	Flash	standard, enhanced
IPMI Firmware	256 MB	Flash	enhanced
FRU Data	512 MB	EEPROM	enhanced
SPD Data	64 MB	EEPROM	standard, enhanced
PM Internal Flash	512 MB	Flash	enhanced
FUM Internal Flash	16 MB	Flash	enhanced

3.1.7 Temperature Sensors

The CP6923 has an external (PCB) temperature sensor which ensures operation within the specified temperature limits. The rugged variants CP6923-R-R2-E2 and CP6923-R-R3-E2 have a total of six sensors, three internal and three external ones. All sensors are accessible via the Peripheral Manager. Although temperature sensing information is made available to the PM, the CP6923 itself does not provide any active means of temperature regulation.

Table 3-12: Temperature sensors

Sensor Name	Type	Position	Comment
Temp PCB1	PCB	U50	
Temp PCB2	PCB	U95	only on E2
Temp CC REF	PCB	Q26	only on E2
Temp PHY1	on-chip	U16	only on E2
Temp PHY2	on-chip	U17	only on E2
Temp PHY3	on-chip	U18	only on E2

The on-chip sensors monitor the die temperature of the octal PHYs which are the most temperature critical devices on the CP6923. As long as their value stays below their upper critical threshold, all componentes on the CP6923 are considered to be operated within their specified temperature range. PCB sensors measure the board temperature at the indicated positions, see figure “Sensor Location TOP” in chapter 3.1.7 and figure “Sensor Location BOT” in chapter 3.1.7. The threshold values of each sensor are listed in chapter 4.4.2.2.

Figure 3-3: Sensor Location TOP

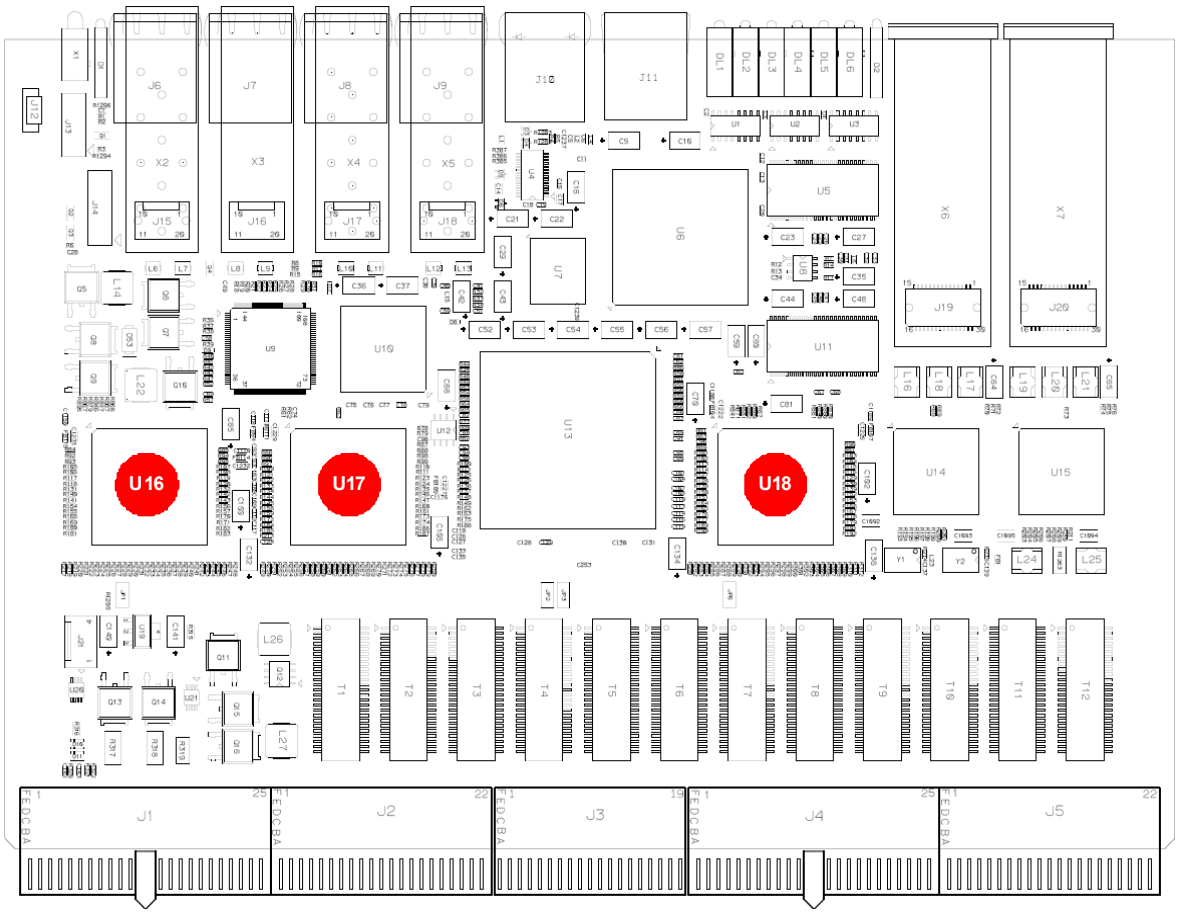
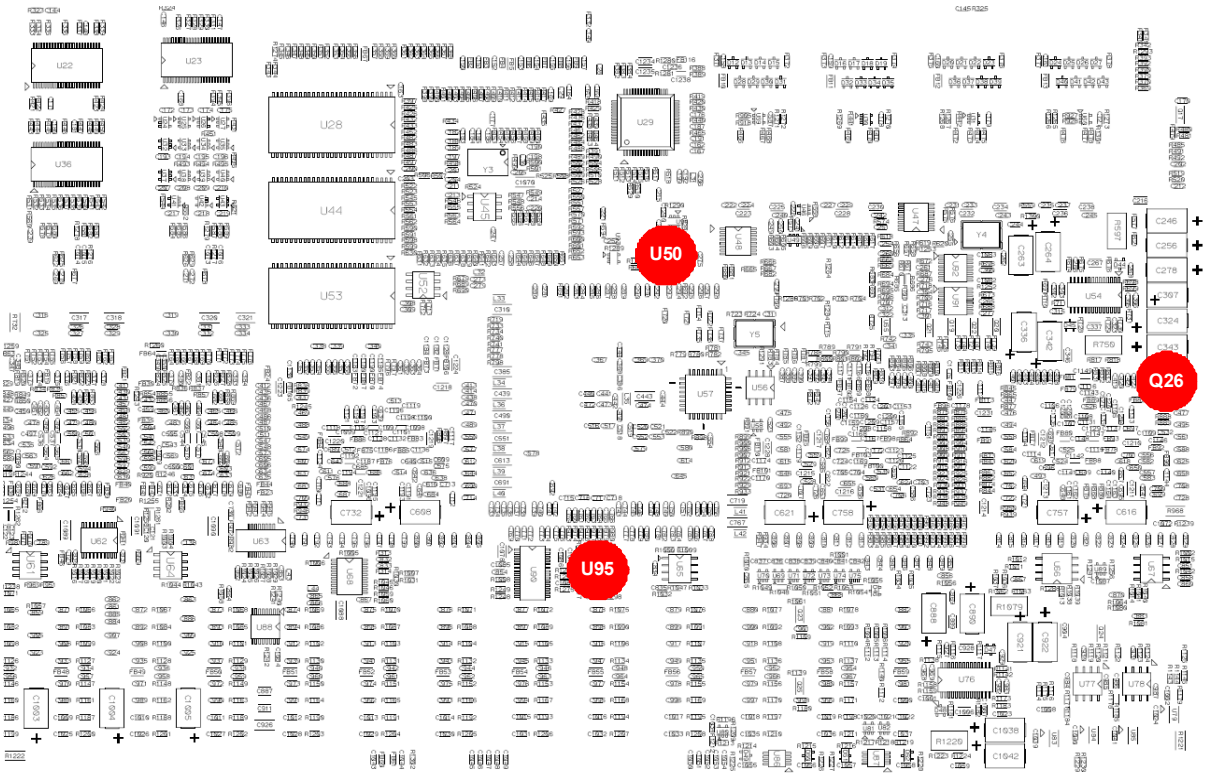


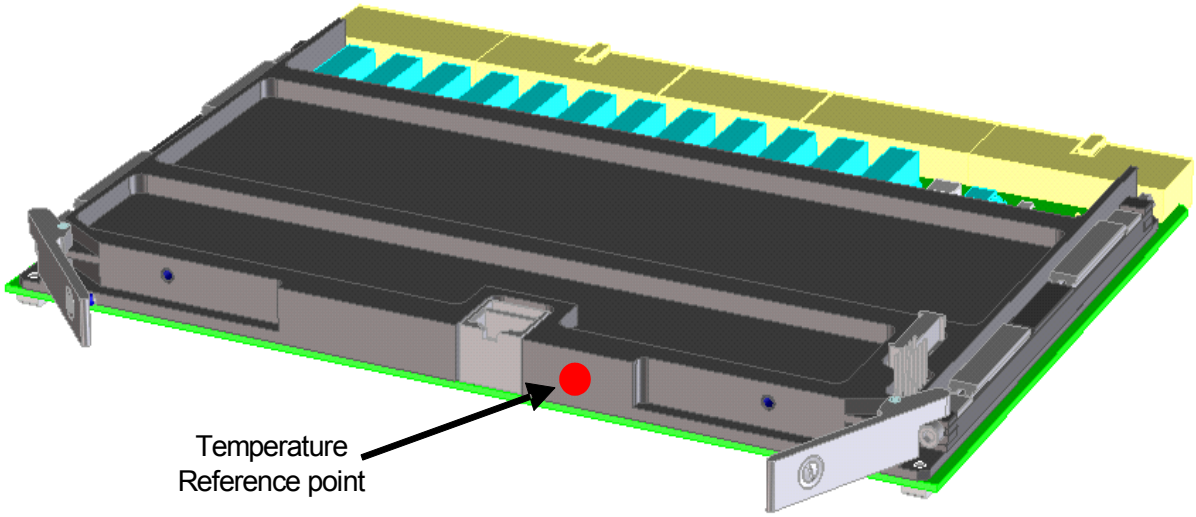
Figure 3-4: Sensor Location BOT



3.1.8 Conduction Cooling

The CP6923-R-R3-E2 is designed for conduction cooled applications according ANSI/Vita 30.1-2002. The temperature range of the CP6923-R-R3-E2 is specified from -40°C to 85°C. This temperature range refers to the value measured at one of the reference temperature points. This can either be the reference point at the front side of the conduction cooled frame (see figure “3D drawing of the CP6923-R-R3-E2 with temperature reference point” in chapter 3.1.8) for manual measurement or the on-board sensor Temp CC REF (see chapter 3.1.7).

Figure 3-5: 3D drawing of the CP6923-R-R3-E2 with temperature reference point



The temperature at the reference point provides an indication of the overall thermal conditions. The relation between the reference temperature value and the ambient temperature strongly depends on the construction of the conduction cooled frame. Using a frame with good conduction cooling capabilities can decrease the difference between reference and ambient temperature.

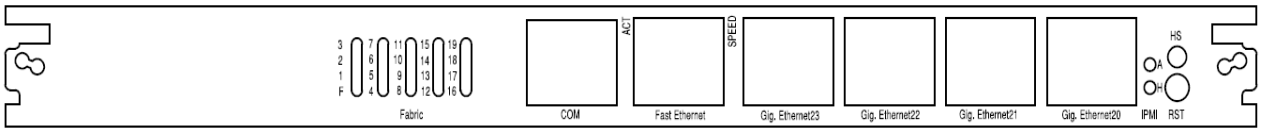
Warning!

It is highly recommended that system integrators as well as end users confirm that the operational environment of the CP6923-R-R3-E2 complies with the thermal requirements defined by the thresholds of the on-board temperature sensors. In the completely assembled system, operated at maximum load, none of the CP6923 board sensors shall exceed its upper critical limit.

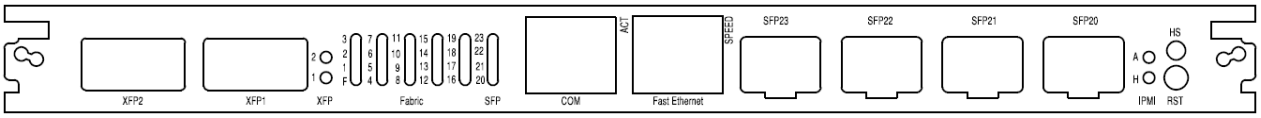
3.1.9 Front Panel Elements

Figure 3-6: Front Panels of the CP6923

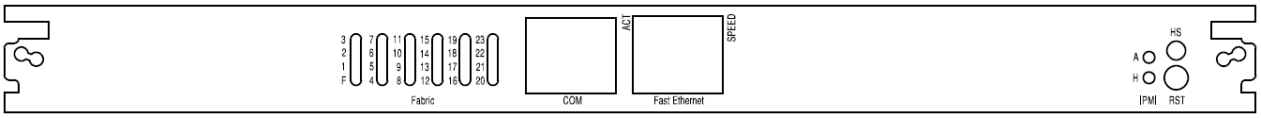
CP6923-C



CP6923-O



CP6923-R



The tables below describe the Hot Swap and PM status LEDs:

Table 3-13: Hot Swap LED Signification

Blue LED (Hot Swap LED)	
ON	Ready for hot swap
OFF	Normal Operation

Table 3-14: PM Status LED Signification

Green LED 1 and Green LED 2	
Healthy	ON = PM operational
Activity	ON = PM activity

The front panel provides 20 LEDs for status indication for the standard fabric interfaces. The color is green with the following states:

Table 3-15: Standard Fabric Interface LED Signification

Green LED (Standard Fabric Interface)	
OFF	Port did not perform linkup
ON	Port performed linkup but no activity
BLINKING	Port performed linkup and there is activity

The front panel provides 4 additional LEDs for status indication for the extended fabric interfaces (CP6923-R) or the SFP optical connectors (CP6923-O). The color is green with the following states:

Table 3-16: Extended Fabric Interface LED Signification

Green LED (Extended Fabric Interface)	
OFF	Port did not perform linkup
ON	Port performed linkup but no activity
BLINKING	Port performed linkup and there is activity

The RJ45 for 10/100/1000BASE-T Uplinks (CP6923-C) provide integrated LEDs; green and green/yellow:

Table 3-17: Copper Uplink LEDs Signification

Green LED (Link/Activity)	
OFF	Port did not perform linkup
ON	Port performed linkup but no activity
BLINKING	Port performed linkup and there is activity
Green/Yellow LED (Speed)	
OFF	10BASE-T
YELLOW ON	100BASE-Tx
GREEN ON	1000BASE-T

Table 3-18: FE Management LEDs Signification

Green LED (Link/Activity)	
OFF	Port did not perform linkup
ON	Port performed linkup but no activity
BLINKING	Port performed linkup and there is activity
Yellow LED (Speed)	
OFF	10BASE-T
ON	100BASE-Tx

The reset switch will perform a reset on the CPU when pressed for less than 1 second and a complete board reset (including IPMI) when pressed for more than 2 seconds.

3.1.10 CompactPCI Bus Connector

The complete CompactPCI connector configuration comprises five connectors named J1 to J5. Their functions are as follows:

- J1, J2: management, IPMB and power. PCI is not supported.
- J3, J4 and J5 have rear I/O interface functionality, providing GbE to the backplane or RIO module and an RS232 interface to a RIO module

The board supports signaling voltages V(I/O) of either 3.3 V or 5 V. No keying is required on J1 which designates universal V(I/O).

3.1.10.1 CompactPCI Connectors J1 and J2 Pinouts

The CP6923 is provided with two 2 mm x 2 mm pitch female CompactPCI bus connectors, J1 and J2.

Table 3-19: Connector J1 Pinout

Pin	Row A	Row B	Row C	Row D	Row E	Row F
25	V_5V_CPCI	NC	NC	V_3V3_CPCI	V_5V_CPCI	GND
24	NC	V_5V_CPCI	V_IO_CPCI	NC	NC	GND
23	V_3V3_CPCI	NC	NC	V_5V_CPCI	NC	GND
22	NC	GND	V_3V3_CPCI	NC	NC	GND
21	V_3V3_CPCI	NC	NC	NC	NC	GND
20	NC	GND	V_IO_CPCI	NC	NC	GND
19	V_3V3_CPCI	NC	NC	GND	NC	GND
18	NC	GND	V_3V3_CPCI	NC	NC	GND
17	V_3V3_CPCI	IPMB0_SCL	IPMB0_SDA	GND	NC	GND
16	NC	GND	V_IO_CPCI	NC	NC	GND
15	V_3V3_CPCI	NC	NC	CPCI_BD_SEL#	NC	GND

Table 3-19: Connector J1 Pinout (Continued)

Pin	Row A	Row B	Row C	Row D	Row E	Row F
14	Key Area					
13						
12						
11	NC	NC	NC	GND	NC	GND
10	NC	GND	V_3V3_CPCI	NC	NC	GND
9	NC	NC	NC	GND	NC	GND
8	NC	GND	V_IO_CPCI	NC	NC	GND
7	NC	NC	NC	GND	NC	GND
6	NC	NC	V_3V3_CPCI	NC	NC	GND
5	NC	NC	CPCI_PCI_RST#	GND	NC	GND
4	V_5V_IPMB_PWR	CPCI_HEALTHY#	V_IO_CPCI	NC	NC	GND
3	NC	NC	NC	V_5V_CPCI	NC	GND
2	NC	V_5V_CPCI	NC	NC	NC	GND
1	V_5V_CPCI	NC	NC	NC	V_5V_CPCI	GND

Table 3-20: Connector J2 Pinout

Pin	Row A	Row B	Row C	Row D	Row E	Row F
22	CPCI_GA[4]	CPCI_GA[3]	CPCI_GA[2]	CPCI_GA[1]	CPCI_GA[0]	GND
21	NC	NC	NC	NC	NC	GND
20	NC	NC	NC	NC	NC	GND
19	NC	NC	IPMB1_SDA	IPMB1_SCL	IPMB_ALERT#	GND
18	NC	NC	NC	NC	NC	GND
17	NC	NC	NC	NC	NC	GND
16	NC	NC	NC	NC	NC	GND
15	NC	NC	NC	NC	NC	GND
14	NC	NC	NC	NC	NC	GND
13	NC	NC	NC	NC	NC	GND
12	NC	NC	NC	NC	NC	GND
11	NC	NC	NC	NC	NC	GND
10	NC	NC	NC	NC	NC	GND
9	NC	NC	NC	NC	NC	GND
8	NC	NC	NC	NC	NC	GND
7	NC	NC	NC	NC	NC	GND
6	NC	NC	NC	NC	NC	GND
5	NC	NC	NC	NC	NC	GND
4	NC	NC	NC	NC	NC	GND
3	NC	NC	NC	NC	NC	GND
2	NC	NC	NC	NC	NC	GND
1	NC	NC	NC	NC	NC	GND

3.1.10.2 CompactPCI Rear I/O Connectors J3-J5 and Pinouts

The CP6923 conducts all backplane I/O signals connectors J3, J4 and J5. These are the GbE interfaces and the rear RS232 interface.

For accessing these I/O signals with a rear I/O module, a special backplane is necessary. The CP6923 is compatible with all standard 6U CompactPCI passive backplanes with rear I/O support on the system slot.

Table 3-21: Connector J3 Pinout

Pin	Row A	Row B	Row C	Row D	Row E	Row F
19	CPCI_SA[4]	CPCI_SA[3]	CPCI_SA[2]	CPCI_SA[1]	CPCI_SA[0]	GND
18	FL_DA24_f+	FL_DA24_f-	GND	FL_DC24_f+	FL_DC24_f-	GND
17	FL_DB24_f+	FL_DB24_f-	GND	FL_DD24_f+	FL_DD24_f-	GND
16	FL_DA8+	FL_DA8-	GND	FL_DC8+	FL_DC8-	GND
15	FL_DB8+	FL_DB8-	GND	FL_DD8+	FL_DD8-	GND
14	FL_DA7+	FL_DA7-	GND	FL_DC7+	FL_DC7-	GND
13	FL_DB7+	FL_DB7-	GND	FL_DD7+	FL_DD7-	GND
12	FL_DA6+	FL_DA6-	GND	FL_DC6+	FL_DC6-	GND
11	FL_DB6+	FL_DB6-	GND	FL_DD6+	FL_DD6-	GND
10	FL_DA5+	FL_DA5-	GND	FL_DC5+	FL_DC5-	GND
9	FL_DB5+	FL_DB5-	GND	FL_DD5+	FL_DD5-	GND
8	FL_DA4+	FL_DA4-	GND	FL_DC4+	FL_DC4-	GND
7	FL_DB4+	FL_DB4-	GND	FL_DD4+	FL_DD4-	GND
6	FL_DA3+	FL_DA3-	GND	FL_DC3+	FL_DC3-	GND
5	FL_DB3+	FL_DB3-	GND	FL_DD3+	FL_DD3-	GND
4	FL_DA2+	FL_DA2-	GND	FL_DC2+	FL_DC2-	GND
3	FL_DB2+	FL_DB2-	GND	FL_DD2+	FL_DD2-	GND
2	FL_DA1+	FL_DA1-	GND	FL_DC1+	FL_DC1-	GND
1	FL_DB1+	FL_DB1-	GND	FL_DD1+	FL_DD1-	GND

Table 3-22: Connector J4 Pinout

Pin	Row A	Row B	Row C	Row D	Row E	Row F
25	FL_DA20+	FL_DA20-	GND	FL_DC20+	FL_DC20-	GND
24	FL_DB20+	FL_DB20-	GND	FL_DD20+	FL_DD20-	GND
23	FL_DA21+	FL_DA21-	GND	FL_DC21+	FL_DC21-	GND
22	FL_DB21+	FL_DB21-	GND	FL_DD21+	FL_DD21-	GND
21	FL_DA22+	FL_DA22-	GND	FL_DC22+	FL_DC22-	GND
20	FL_DB22+	FL_DB22-	GND	FL_DD22+	FL_DD22-	GND
19	FL_DA23+	FL_DA23-	GND	FL_DC23+	FL_DC23-	GND
18	FL_DB23+	FL_DB23-	GND	FL_DD23+	FL_DD23-	GND
17	NC	NC	NC	NC	NC	GND
16	NC	NC	NC	NC	NC	GND
15	NC	NC	NC	NC	NC	GND
14	Key Area					
13						
12						
11	NC	NC	NC	NC	NC	GND
10	NC	NC	NC	NC	NC	GND
9	EWP (*)	NC	NC	RTM_TXD# (*)	RTM_RXD# (*)	GND
8	NC	NC	NC	NC	NC	GND
7	NC	NC	NC	NC	NC	GND
6	NC	NC	NC	NC	NC	GND
5	NC	NC	NC	NC	NC	GND
4	NC	NC	NC	NC	NC	GND
3	NC	NC	NC	NC	NC	GND
2	NC	NC	NC	NC	NC	GND
1	NC	NC	NC	NC	NC	GND



Note…

RTM_TXD# (driven by CP6923) and RTM_RXD# (driven by RIO module) are the two-pin RS232 rear I/O interface.



Note...

FL20 to FL23 are only supported on CP6923-R.



Note...

Signal EWP is only implemented on the CP6923-R-R2-E2 and the CP6923-R-R3-E2, see chapter 3.1.6.

Table 3-23: Connector J5 Pinout

Pin	Row A	Row B	Row C	Row D	Row E	Row F
22	FL_DA19+	FL_DA19-	GND	FL_DC19+	FL_DC19-	GND
21	FL_DB19+	FL_DB19-	GND	FL_DD19+	FL_DD19-	GND
20	FL_DA18+	FL_DA18-	GND	FL_DC18+	FL_DC18-	GND
19	FL_DB18+	FL_DB18-	GND	FL_DD18+	FL_DD18-	GND
18	FL_DA17+	FL_DA17-	GND	FL_DC17+	FL_DC17-	GND
17	FL_DB17+	FL_DB17-	GND	FL_DD17+	FL_DD17-	GND
16	FL_DA16+	FL_DA16-	GND	FL_DC16+	FL_DC16-	GND
15	FL_DB16+	FL_DB16-	GND	FL_DD16+	FL_DD16-	GND
14	FL_DA15+	FL_DA15-	GND	FL_DC15+	FL_DC15-	GND
13	FL_DB15+	FL_DB15-	GND	FL_DD15+	FL_DD15-	GND
12	FL_DA14+	FL_DA14-	GND	FL_DC14+	FL_DC14-	GND
11	FL_DB14+	FL_DB14-	GND	FL_DD14+	FL_DD14-	GND
10	FL_DA13+	FL_DA13-	GND	FL_DC13+	FL_DC13-	GND
9	FL_DB13+	FL_DB13-	GND	FL_DD13+	FL_DD13-	GND
8	FL_DA12+	FL_DA12-	GND	FL_DC12+	FL_DC12-	GND
7	FL_DB12+	FL_DB12-	GND	FL_DD12+	FL_DD12-	GND
6	FL_DA11+	FL_DA11-	GND	FL_DC11+	FL_DC11-	GND
5	FL_DB11+	FL_DB11-	GND	FL_DD11+	FL_DD11-	GND
4	FL_DA10+	FL_DA10-	GND	FL_DC10+	FL_DC10-	GND
3	FL_DB10+	FL_DB10-	GND	FL_DD10+	FL_DD10-	GND
2	FL_DA9+	FL_DA9-	GND	FL_DC9+	FL_DC9-	GND
1	FL_DB9+	FL_DB9-	GND	FL_DD9+	FL_DD9-	GND

3.2 CP-RIO6-923

The CP-RIO6-923 is a PICMG 2.0 compliant Rear-panel I/O board that enables PICMG 2.16 compliant switches, like CP6923 and CP6925, to access the management and I/O of the CPCI switch cards.

The CP-RIO6-923 is fully RoHS compliant and appears in two versions:

- 4HP width, with 12 10/100/1000Base-T Ethernet ports
- 8HP width, with 24 10/100/1000Base-T Ethernet ports

The CP-RIO6-923 provides a serial RS232 interface. For RS232 access, a RJ45 connector is provided.

8HP version supports 24 10/100/1000Base-T ports connected to FL1 to FL23 and FLf (Fabric to Fabric Link Port).

4HP version supports 12 10/100/1000Base-T ports connected to FL12 to FL23.



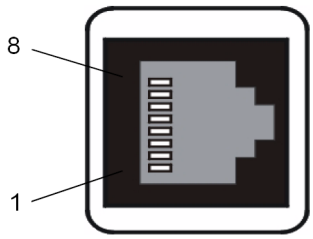
Warning!

The CP-RIO6-923 connects to CPCI backplanes supporting RIO connections. The corresponding backplane connectors provide the same signals that are also routed to other slots in the system. The user/system designer has to make sure that the combination of CP6923, CP-RIO6-923, its cabling, the backplane and other cards present in the system does not lead to multiple connections.

3.2.1 Serial RS232 Interface

The RS232 signals from connector J4 are routed to a RJ45 connector in the faceplate. The connector has the following pin assignment:

Table 3-24: Serial Port (RJ45) Pin Assignment

Signal	Pin	
N.C.	1	
N.C.	2	
TXD	3	
GND	4	
GND	5	
RXD	6	
N.C.	7	
N.C.	8	

3.2.2 10/100/1000BASE-T Ports

The following tables show the port assignment of the 24 10/100/1000Base-T ports at the tree RJ45 modules on the faceplate.

Table 3-25: RIO Port Assignment

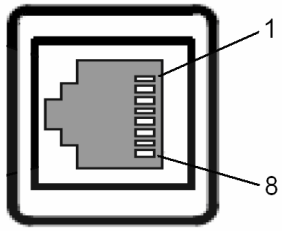
PICMG 2.16 Backplane Port	Faceplate 8HP Connector	Faceplate 4HP Connector
FL_f	Fx	NC
FL_01	1x	NC
FL_02	2x	NC
FL_03	3x	NC
FL_04	4x	NC
FL_05	5x	NC
FL_06	6x	NC
FL_07	7x	NC
FL_08	8x	NC

Table 3-25: RIO Port Assignment (Continued)

PICMG 2.16 Backplane Port	Faceplate 8HP Connector	Faceplate 4HP Connector
FL_09	9.x	NC
FL_10	10x	NC
FL_11	11x	NC
FL_12	12x	12x
FL_13	13x	13x
FL_14	14x	14x
FL_15	15x	15x
FL_16	16x	16x
FL_17	17x	17x
FL_18	18x	18x
FL_19	19x	19x
FL_20	20x	20x
FL_21	21x	21x
FL_22	22x	22x
FL_23	23x	23x

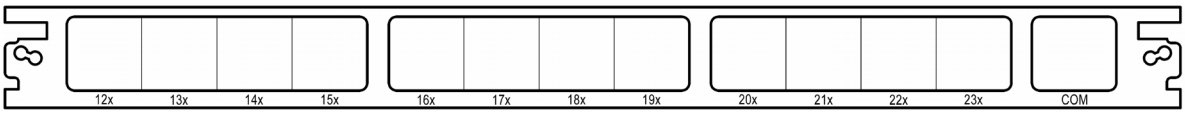
The next table shows the pin assignment of one 10/100/1000BASE-T RJ45 connector.

Table 3-26: MDI-X RJ45 Pin Assignment

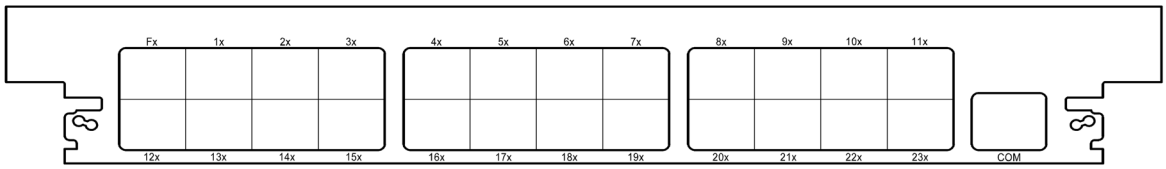
Signal	Pin	
BI_DB+	1	
BI_DB-	2	
BI_DA+	3	
BI_DD+	4	
BI_DD-	5	
BI_DA-	6	
BI_DC+	7	
BI_DC-	8	

3.2.3 Front Panel Elements

- 4 HP Rear-panel I/O board front panel with standard handles



- 8 HP Rear-panel I/O board front panel with standard handles
-



Software Description

4. Software Description

Software on the CP6923 includes the following parts:

- Bootloader
- initrd (including rootFS, kernel and application software)
- IPMI FW

The Software accomplishes operation of the switching hardware and is therefore also referenced as firmware. It is preinstalled on the system and can only be updated by a dedicated update procedure. This manual only describes bootloader, its self tests and IPMI Firmware and introduces the update procedure.

For additional information of system configuration using CLI commands refer to documentation "*CP6923 CLI Reference Manual*".

4.1 Supported RFCs

The Software supports the following standards and RFCs.

4.1.1 Management

- RFC 826 - ARP
- RFC 854 - Telnet
- RFC 855 - Telnet Option
- RFC 1155 - SMI v1
- RFC 1157 - SNMP
- RFC 1212 - Concise MIB Definitions
- RFC 1901 - Community based SNMP v2
- RFC 2246 - The TLS Protocol, Version 1.0
- RFC 2271 - SNMP Framework MIB
- RFC 2295 - Transparent Content Negotiation
- RFC 2296 - Remote Variant Selection; RSVA/1.0 State Management "cookies"
- RFC 2346 - AES Ciphersuites for Transport Layer Security
- RFC 2576 - Coexistence between SNMP v1,v2 & v3
- RFC 2578 - SMI v2
- RFC 2579 - Textual Conventions for SMI v2
- RFC 2580 - Conformance statements for SMI v2
- RFC 3410 - Introduction and Applicability Statements for Internet Standard Management Framework
- RFC 3411 - An Architecture for Describing SNMP Management Frameworks
- RFC 3412 - Message Processing and Dispatching (December 2002)
- RFC 3413 - SNMP Applications (December 2002)
- RFC 3414 - User-based Security Model (December 2002)
- RFC 3415 - View-based Access Control Model (December 2002)
- RFC 3416 - Version 2 of SNMP Protocol Operations (December 2002)
- RFC 3417 - Transport Mappings (December 2002)
- RFC 3418 - MIB for the Simple Network Management Protocol.
- RFC 3635 - Definition of Managed Objects for Ethernet-like Interface Types
- SSL 3.0 & TLS 1.0
- SSH 1.5 & 2.0

- Draft-ietf-secsh-transport-16 - SSH Transport Layer Protocol
- Draft-ietf-secsh-userauth-17 - SSH Authentication Protocol
- DRAFT-ietf-secsh-connect-17 - SSH Connection Protocol
- Draft-ietf-secsh-architecture-14 - SSH Protocol Architecture
- Draft-ietf-secsh-publickeyfile-03 - SECSH Public Key File Format
- Draft-ietf-secsh-dh-group-exchange-04 - Diffie-Hellman Group exchange for the SSH Transport Layer Protocol
- Configurable Management VLAN ID
- Industry Standard CLI

4.1.2 Switching

- IEEE 802.3ac - VLAN Tagging
- IEEE 802.3ad - Link Aggregation with Static LAG and LACP support
- IEEE 802.1S - Multiple Spanning Tree
- IEEE 802.1W - Rapid Spanning Tree
- IEEE 802.1D - Spanning Tree
- GARP
- GVRP - Dynamic VLAN Registration
- GMRP - Dynamic L2 Multicast Registration
- IEEE 802.1Q - Virtual LANs with Port Based VLANs
- IEEE 802.1v - Protocol based VLANs
- IEEE 802.1p - Ethernet Priority with User Provisioning & Mapping
- IEEE 802.1X - Port Authentication
- IEEE 802.3x - Flow Control
- IGMP Snooping
- Port Mirroring
- Broadcast Storm Recovery
- Static MAC Filtering
- Double VLAN / vMAN Tagging
- Jumbo Frames
- IPv6 Classification APIs
- XMODEM
- RFC 768 - UDP
- RFC 783 - TFTP
- RFC 791 - IP
- RFC 792 - ICMP
- RFC 793 - TCP
- RFC 951 - BOOTP
- RFC 1321 - Message Digest Algorithm (MD5)
- RFC 1534 - Interoperation between BOOTP and DHCP
- RFC 2030 - Simple Network Time Protocol (SNTP) Version 4 for IPv4, IPv6 and OSI
- RFC 2131 - DHCP Client
- RFC 2131 - DHCP Server
- RFC 2132 - DHCP Options and BOOTP Vendor Extensions
- RFC 2865 - RADIUS Client
- RFC 2866 - RADIUS Accounting
- RFC 2868 - RADIUS Attributes for Tunnel Protocol Support
- RFC 2869 - RADIUS Extensions
- rfc2869bis - RADIUS support for EAP

- RFC 3176 - InMon Corporation's sFlow: A Method for Monitoring Traffic in Switched and Routed Networks
- RFC 3396 - Encoding Long Option in the Dynamic Host Configuration Protocol (DHCPv4)
- RFC 3580 - 802.1X RADIUS Usage Guidelines
- Draft-ietf-magma-snoop-11.txt - Considerations for IGMP and MLD Snooping Switches

4.1.3 Routing

- Weighted Static Routes
- RFC 819 - Domain Naming Convention for Internet User Applications
- RFC 826 - Ethernet ARPRFC 894 - Transmission of IP Datagrams over Ethernet Networks
- RFC 896 - Congestion Control in IP/TCP Networks
- RFC 919 - Broadcasting Internet Datagrams
- RFC 922 - Broadcasting Internet Datagrams in the presence of subnets
- RFC 950 - Internet Standard Subnetting Procedure
- RFC 1027 - Using ARP to implement transparent subnet gateways
- RFC 1058 - RIP v1
- RFC 1256 - ICMP Router Discovery Messages
- RFC 1321 - Message Digest Algorithm (MD5)
- RFC 1519 - CIDR
- RFC 1723 - RIP v2
- RFC 1765 - OSPF Database Overflow
- RFC 1812 - Requirements for IP Version 4 Routers
- RFC 2328 - OSPF v2 w/ Equal Cost Multipath support
- RFC 3046 - DHCP/BootP Relay
- RFC 3101 - OSPF with NSSA support
- RFC 3768 - Virtual Router Redundancy Protocol (VRRP)
- Route Redistribution across RIP and OSPF
- VLAN Routing

4.1.4 QoS

- Bandwidth Policing (Min and Max; per port/per VLAN)
- Committed Information Rate (CIR)
- Maximum Burst Rate (MBR)
- Per Port (Interface)
- Per VLAN
- Filtering (L3/L4 Access Lists)
- IP Classification - 6 Tuple Classification
- RFC 2474 - DiffServ Definition
- RFC 2475 - DiffServ Architecture
- RFC 2597 - Assured Forwarding PHB
- RFC 3246 - An Expedited Forwarding PHB
- RFC 3260 - New Terminology and Clarifications for DiffServ

4.1.5 Multicast

- RFC 1112 - Host Extensions for IP Multicasting (IGMPv1)
- RFC 2236 - IGMPv2

- RFC 2362 - PIM-SM
- IP Multicast Traceroute
- RFC 2365 - Administratively Scoped Multicast
- RFC 3376 - Internet Group Management Protocol, Version 3
- Draft-ietf-pim-v2-dm-03 - PIM-DM
- Draft-ietf-idmr-dvmrp-v3-10 - DVMRP
- Draft-iet.magma-mgmd-mib-03.txt
- Static Configuration of RP

4.2 Supported MIBs

The Software supports the following MIBs.

4.2.1 Enterprise MIB

- Support for all managed objects not contained in standards based MIBs.

4.2.2 Switching Package MIBs

- RFC 1213 - MIB-II
- RFC 1493 - Bridge MIB: Definitions of Managed Objects for Bridges (dot1d)
- RFC 1643 – Definitions of managed objects for the Ethernet-like interface types
- RFC 2233 - The Interfaces Group MIB using SMI v2
- RFC 2618 - RADIUS Authentication Client MIB
- RFC 2620 - RADIUS Accounting MIB
- RFC 2674 - VLAN & Ethernet Priority MIB: The Bridge MIB Extension module for managing Priority and Multicast Filtering, defined by IEEE 802.1D-1998.
- RFC 2674 - Q-BRIDGE-MIB: The VLAN Bridge MIB module for managing Virtual Bridged Local Area Networks
- RFC 2737 – Entity MIB version 2
- RFC 2819 - RMON Groups 1,2,3 & 9
- RFC 2863 – Interfaces Group MIB
- RFC 3291 - Textual Conventions for Internet Network Addresses
- RFC 3635 - Etherlike-MIB: Definitions of Managed Objects for the Ethernet-like Interface Types
- IANA-ifType-MIB
- IEEE 802.1X MIB (IEEE8021-PAE-MIB)
- IEEE 802.3AD MIB (IEEE8021-AD-MIB)
- IEEE 802.1AB – LLDP MIB
- ANSI/TIA 1057 – LLDP-MED MIB
- RADIUS-ACC-CLIENT-MIB: RADIUS Accounting Client MIB
- RADIUS-AUTH-CLIENT-MIB: RADIUS Authentication Client MIB

4.2.3 Routing Package MIBs

- Draft-ietf-ipv6-rfc2096-update-07.txt - IP Forwarding Table MIB
- IANA-Address-Family-Numbers-MIB
- RFC 1724 - RIP v2 MIB Extension
- RFC 1850 - OSPF-MIB: OSPF Version 2 Management Information Base
- RFC 1850 - OSPF-TRAP-MIB: The MIB module to describe traps for the OSPF Version 2 Protocol.

- RFC 2787 - VRRP MIB: Definitions of Managed Objects for the Virtual Router Redundancy Protocol
- DVMRP-STD-MIB: Distance-Vector Multicast Routing Protocol MIB
- IANA-RTPROTO-MIB: IANA IP Route Protocol and IP MRoute Protocol Textual Conventions

4.2.4 QoS Package MIBs

- RFC 3289 - DIFFSERV-MIB: Management Information Base for the Differentiated Services Architecture
- RFC 3289 - DIFFSERV-DCSP-TC MIB: Management Information Base for the Textual Conventions used in DIFFSERV-MIB

4.2.5 Multicast package MIBs

- RFC 2932 – IPv4 multicast routing MIB
- RFC 2933 - IGMP MIB
- RFC 2934 – PIM MIB for IPv4 (PIMDMv4)
- Draft-ietf-pim-mib-v2-03 (PIM-SM MIB)
- Draft-ietf-magma-mgmd-mib-05.txt – Multicast group membership discovery MIB
- Draft-ietf-idmr-dvmrp-mib-11.txt - DVMRP MIB
- IANA-RTP-PROTO_MIB

4.2.6 SNMP MIBs

- RFC 1907 - SNMPv2-MIB: The MIB module for SNMPv2 entities
- SNMP-COMMUNITY-MIB: This MIB module defines objects to help support coexistence between SNMPv1, SNMPv2 and SNMPv3.
- SNMP-FRAMEWORK-MIB: The SNMP Management Architecture MIB
- SNMP-MPD-MIB: The MIB for Message Processing and Dispatching
- SNMP-NOTIFICATION-MIB: The Notification MIB Module
- SNMP-TARGET-MIB: The Target MIB Module
- SNMP-USER-BASED-SM-MIB: The management information definitions for the SNMP User-based Security Model.
- SNMP-VIEW-BASED-ACM-MIB: The management information definitions for the View-based Access Control Model for SNMP.

4.3 Bootloader

On the CP6923 Switch board, the bootloader ‘u-boot‘ (universal bootloader) is used. The bootloader initializes the main components of the board like CPU, SDRAM, serial lines etc. for operation. After this, kernel and application are started from flash.

4.3.1 Power On Self Test

4.3.1.1 Test Routines

Upon power on or system reset, the bootloader performs a set of Power On Self Tests (POST) to check the integrity of specific components. Components where a POST is available are:

- SDRAM
- PPC405 serial line
- PPC405 I2C
- PPC405 FE

In the case that a POST fails, a POST error code is written into the postcode high byte register of the onboard CPLD. The boot process is not stopped as there are good chances the board can boot even in case of POST errors. The postcode high byte register is also accessible by the PM which can report error codes to a separate management instance. Thus more comprehensive diagnostic tests could be started.

The following table shows a list of available POST routines including POST error codes.

Table 4-1: POST routines and error codes

Device	Test	POST Numerical Error Code	POST Error Code
SDRAM	Data bus - walking 1 test	0x20	PCW_DLINE
SDRAM	Address bus - walking 1 test	0x40	PCW_ALINE
SDRAM	Memory - read/write test	0x80	PCW_MEM
PPC405 UART	Serial loopback teststring	0x01	PCW_SERIAL
PPC405 I2C	Bus scan for devices from I2C_ADDR_LIST	0x02	PCW_I2C
PPC405 FE	Phy access	0x08	PCW_ETH1
PPC405 FE	Phy loopback test using special Ethernet test frame	0x10	PCW_ETH2
KCS	KCS READY signal test	0x04	KCSCTL

4.3.1.2 Boot Steps

In addition to the Power On Self Tests described above, the bootloader logs the board startup sequence in the postcode low byte register. A postcode value is written each time a step in the start sequence has been completed successfully. The postcode stored is also accessible by the PM. In the case that an error occurs during execution of a step, the boot sequence is stopped because a fatal error has occurred with great likelihood. In this case, a management instance can read the last postcode written via the PM and thus determine where the fatal error has occurred.

A list of defined postcodes is shown in the table below.

Table 4-2: POST Boot Steps

POST Step Code	Value	Boot Step
PC_INIT	0x00	Initial PC, EBC has been set up
PC_BINIT	0x01	Board early init (interrupt settings)
PC_CLOCKS	0x02	Get system clocks
PC_TIMEB	0x03	Init timebase
PC_ENVINIT	0x04	Init environment
PC_BAUD	0x05	Init baudrate
PC_SERIAL	0x06	Init UART
PC_CPU	0x07	Check CPU
PC_PHY	0x08	Setup PHY
PC_I2C	0x09	Init I2C
PC_INITRAM	0x0A	Init SDRAM controller and SDRAM
PC_TESTRAM	0x0B	Test SDRAM
PC_INITSEQ	0x0F	Board init sequence completed
PC_INITBOARD	0x10	Board init ok, stack set up ok, board info struct set up
PC_RELOC	0x11	Relocation completed
PC_TRAP	0x18	Setup trap handler
PC_FLASH	0x19	Flash OK
PC_CPU2	0x1A	Init higher level parts of CPU
PC_RELOCENV	0x1B	Relocation of environment Ok
PC_BDINFO	0x1C	Fill missing fields of bdinfo
PC_PCI	0x1D	PCI configuration done
PC_DEVICES	0x1E	Device init done
PC_JUMPTABLE	0x1F	Jumptable init done
PC_CONSOLE	0x20	Console init done
PC_MAIN	0x2F	Enter main loop
PC_START_OS	0x3F	Pass control to OS, leave bootloader

4.4 IPMI Firmware

The PPC communicates with the Peripheral Manager (PM) using the Keyboard Controller Style (KCS) interface. The bootloader is able to communicate with the PM, e.g. for POST error logging purposes and fault resilient purposes.

The memory subsystem of the PM consists of an integrated flash memory to hold the PM operation code and integrated RAM for data. The field replaceable unit (FRU) inventory information is stored in the nonvolatile memory on an EEPROM connected via a local I2C interface to the PM microcontroller. It is possible to store up to 4 Kbytes within the FRU inventory information. Communication over IPMB bus to the ShMC ensures that ‘post-mortem’ logging information is available even if the main processor becomes disabled.

The PM provides several I2C bus connections. Two are used as the redundant IPMB bus connections to the backplane, one for the Board Sensors and one is for local EEPROM storage.

If an IPMB bus fault or PM failure occurs, IPMB isolators are used to switch and isolate the backplane/system IPMB bus from the faulted Hub Board. If possible, the PM activates the redundant IPMB bus to re-establish system management communication to report the fault.

The onboard DC voltage, current, and temperature sensors are monitored by the PM microcontroller continuously. The PM will log an event into the ShMC’s System Event Log (SEL) if any of the thresholds are exceeded.

To increase the reliability of the Hub board management subsystem, an external watchdog supervisor for the PM is implemented. The PM strobes the external watchdog at two-second intervals to ensure continuity of operation of the board’s management subsystem. If the PM ceases to strobe the watchdog supervisor for more than six seconds, the watchdog isolates the PM from the IPMBs and resets the PM. The watchdog supervisor does not reset the payload power and the restart of the PM will not affect the payload. The external watchdog supervisor is not configurable and must not be confused with the IPMI v1.5 watchdog timer commands.

This external watchdog of the PM is implemented in a second microcontroller. This Firmware Upgrade Manager (FUM) is responsible for monitoring the PM and for managing the PM fail safe firmware upgrade process. The FUM keeps two PM Firmware code images in two external SEEPROM memories. If a failure occurs during firmware upgrade, the FUM will automatically rollback to the last known working PM firmware image.

4.4.1 Supported IPMI Commands

4.4.1.1 Standard Commands

Part of the command list in IPMI specification 2.0

M = mandatory, O = optional

Table 4-3: Standard Commands

	IPMI 2.0 Spec. section	NetFn	CMD	Support on CP6923
IPM Device "Global" Commands				**M**
Get Device ID	20.1	App	01h	M / **Yes** [1]
Cold Reset	20.2	App	02h	O / **Yes**
Warm Reset	20.3	App	03h	O / No
Get Self Test Results	20.4	App	04h	O / **Yes**
Manufacturing Test On	20.5	App	05h	O / No
Set ACPI Power State	20.6	App	06h	O / No
Get ACPI Power State	20.7	App	07h	O / No
Get Device GUID	20.8	App	08h	O / No
Broadcast "Get Device ID"	20.9	App	01h	M / **Yes**
BMC Watchdog Timer Commands				**O**
Reset Watchdog Timer	27.5	App	22h	O / **Yes**
Set Watchdog Timer	27.6	App	24h	O / **Yes**
Get Watchdog Timer	27.7	App	25h	O / **Yes**
BMC Device and Messaging Commands				**O**
Set BMC Global Enables	22.1	App	2Eh	O / **Yes**
Get BMC Global Enables	22.2	App	2Fh	O / **Yes**
Clear Message Flags	22.3	App	30h	O / **Yes**
Get Message Flags	22.4	App	31h	O / **Yes**
Enable Message Channel Receive	22.5	App	32h	O / **Yes**
Get Message	22.6	App	33h	O / **Yes**
Send Message	22.7	App	34h	O / **Yes**
Read Event Message Buffer	22.8	App	35h	O / **Yes**
Get BT Interface Capabilities	22.9	App	36h	O / **Yes**
Get System GUID	22.14	App	37h	O / No
Get Channel Authentication Capabilities	22.13	App	38h	O / No

Table 4-3: Standard Commands (continued)

	IPMI 2.0 Spec. section	NetFn	CMD	Support on CP6923
Get Session Challenge	22.15	App	39h	O / No
Activate Session	22.17	App	3Ah	O / No
Set Session Privilege Level	22.18	App	3Bh	O / No
Close Session	22.19	App	3Ch	O / No
Get Session Info	22.20	App	3Dh	O / No
Get AuthCode	22.21	App	3Fh	O / No
Set Channel Access	22.22	App	40h	O / No
Get Channel Access	22.23	App	41h	O / No
Get Channel Info	22.24	App	42h	O / No
Set User Access	22.26	App	43h	O / No
Get User Access	22.27	App	44h	O / No
Set User Name	22.28	App	45h	O / No
Get User Name	22.29	App	46h	O / No
Set User Password	22.30	App	47h	O / No
Activate Payload	24.1	App	48h	O / No
Deactivate Payload	24.2	App	49h	O / No
Get Payload Activation Status	24.4	App	4Ah	O / No
Get Payload Instance Info	24.5	App	4Bh	O / No
Set User Payload Access	24.6	App	4Ch	O / No
Get User Payload Access	24.7	App	4Dh	O / No
Get Channel Payload Support	24.8	App	4Eh	O / No
Get Channel Payload Version	24.9	App	4Fh	O / No
Get Channel OEM Payload Info	24.10	App	50h	O / No
Master Write-Read	22.11	App	52h	O / **Yes**
Get Channel Cipher Suits	22.15	App	54h	O / No
Suspend/Resume Payload Encryption	24.3	App	55h	O / No
Set Channel Security Keys	22.25	App	56h	O / No
Get System Interface Capabilities	22.9	App	57h	O / No
Chassis Device Commands				**O / Yes**
Get Chassis Capabilities	28.1	Chassis	00h	O / **Yes**
Get Chassis Status	28.2	Chassis	01h	O / **Yes**
Chassis Control	28.3	Chassis	02h	O / No
Chassis Reset	28.4	Chassis	03h	O / No
Chassis Identify	28.5	Chassis	04h	O / No

Table 4-3: Standard Commands (continued)

	IPMI 2.0 Spec. section	NetFn	CMD	Support on CP6923
Set Chassis Capabilities	28.7	Chassis	05h	O / No
Set Power Restore Policy	28.8	Chassis	06h	O / No
Get System Restart Cause	28.11	Chassis	07h	O / No
Set System Boot Options	28.12	Chassis	08h	O / No
Get System Boot Options	28.13	Chassis	09h	O / No
Get POH Counter	28.14	Chassis	0Fh	O / **Yes** [2]
Event Commands				**M**
Set Event Receiver	29.1	S/E	01h	M / **Yes**
Get Event Receiver	29.2	S/E	02h	M / **Yes**
Platform Event (a.k.a. “Event Message”)	29.3	S/E	03h	M / **Yes**
PEF and Alerting Commands				**O**
Get PEF Capabilities	30.1	S/E	10h	O / No
Arm PEF Postpone Timer	30.2	S/E	11h	O / No
Sensor Device Commands				**M**
Get Device SDR Info	35.2	S/E	20h	M / **Yes**
Get Device SDR	35.3	S/E	21h	M / **Yes**
Reserve Device SDR Repository	35.4	S/E	22h	M / **Yes**
Get Sensor Reading Factors	35.5	S/E	23h	O / No
Set Sensor Hysteresis	35.6	S/E	24h	O / **Yes**
Get Sensor Hysteresis	35.7	S/E	25h	O / **Yes**
Set Sensor Threshold	35.8	S/E	26h	O / **Yes**
Get Sensor Threshold	35.9	S/E	27h	O / **Yes**
Set Sensor Event Enable	35.10	S/E	28h	O / **Yes**
Get Sensor Event Enable	35.11	S/E	29h	O / **Yes**
Re-arm Sensor Events	35.12	S/E	2Ah	O / No
Get Sensor Event Status	35.13	S/E	2Bh	O / No
Get Sensor Reading	35.14	S/E	2Dh	M / **Yes**
Set Sensor Type	35.15	S/E	2Eh	O / No
Get Sensor Type	35.16	S/E	2Fh	O / No
FRU Device Commands				**M**
Get FRU Inventory Area Info	34.1	Storage	10h	M / **Yes**
Read FRU Data	34.2	Storage	11h	M / **Yes**

Table 4-3: Standard Commands (continued)

	IPMI 2.0 Spec. section	NetFn	CMD	Support on CP6923
Write FRU Data	34.3	Storage	12h	M / **Yes**
SDR Device Commands				**O**
Get SDR Repository Info	33.9	Storage	20h	O / **Yes**
Get SDR Repository Allocation Info	33.10	Storage	21h	O / **Yes**
Reserve SDR Repository	33.11	Storage	22h	O / **Yes**
Get SDR	33.12	Storage	23h	O / **Yes**
Add SDR	33.13	Storage	24h	O / **Yes**
Partial Add SDR	33.14	Storage	25h	O / **Yes**
Delete SDR	33.15	Storage	26h	O / **Yes**
Clear SDR Repository	33.16	Storage	27h	O / **Yes**
Get SDR Repository Time	33.17	Storage	28h	O / No
Set SDR Repository Time	33.18	Storage	29h	O / No
Enter SDR Repository Update Mode	33.19	Storage	2Ah	O / No
Exit SDR Repository Update Mode	33.20	Storage	2Bh	O / No
Run Initialization Agent	33.21	Storage	2Ch	O / **Yes**
SEL Device Commands				**O / Yes**
Get SEL Info	40.2	Storage	40h	O / **Yes**
Get SEL Allocation Info	40.3	Storage	41h	O / **Yes**
Reserve SEL	40.4	Storage	42h	O / **Yes**
Get SEL Entry	40.5	Storage	43h	O / **Yes**
Add SEL Entry	40.6	Storage	44h	O / **Yes**
Partial Add SEL Entry	40.7	Storage	45h	O / No
Delete SEL Entry	40.8	Storage	46h	O / **Yes**
Clear SEL	40.9	Storage	47h	O / **Yes**
Get SEL Time	40.10	Storage	48h	O / **Yes**
Set SEL Time	40.11	Storage	49h	O / **Yes**
Get Auxiliary Log Status	40.12	Storage	5Ah	O / No
Set Auxiliary Log Status	40.13	Storage	5Bh	O / No

Table 4-4: Standard PICMG 3.0 Commands

AdvancedTCA	PICMG 3.0 Table	CMD	Support on CP6923
Get PICMG Properties	3-9	00h	M / **Yes**
Get Address Info	3-8	01h	N/A
Get Shelf Address Info	3-13	02h	N/A
Set Shelf Address Info	3-14	03h	N/A
FRU Control	3-22	04h	M / **Yes** [3]
Get FRU LED Properties	3-24	05h	M / **Yes**
Get LED Color Capabilities	3-25	06h	M / **Yes**
Set FRU LED State	3-26	07h	M / **Yes**
Get FRU LED State	3-27	08h	M / **Yes**
Set IPMB State	3-51	09h	N/A
Set FRU Activation Policy	3-17	0Ah	N/A
Get FRU Activation Policy	3-18	0Bh	N/A
Set FRU Activation	3-16	0Ch	N/A
Get Device Locator Record ID	3-29	0Dh	M / **Yes**
Set Port State	3-41	0Eh	N/A
Get Port State	3-42	0Fh	N/A
Compute Power Properties	3-60	10h	N/A
Set Power Level	3-62	11h	N/A
Get Power Level	3-61	12h	N/A
Renegotiate Power	3-66	13h	N/A
Get Fan Speed Properties	3-63	14h	N/A
Set Fan Level	3-65	15h	N/A
Get Fan Level	3-64	16h	N/A
Bused Resource	3-44	17h	N/A
Get IPMB Link Info	3-49	18h	N/A

[1] Has oem extensions.

[2] Response byte 2: hours, byte 3: minutes after module start. Bytes 4..6: void

[3] Only 1 = Cold Reset and 2 = Warm Reset

4.4.1.2 OEM Commands and Extensions

Get Device ID Command with OEM Extensions

	LUN	NetFn	CMD
Get Device ID command with OEM extensions	00h	App = 06h	01h

	Byte	Data Field
Request Data	-	-
Response Data	1	Completion Code
	2:12	Regular Get Device ID Command response fields
	13	Release number 1… of the IPMI controller firmware. The open ipmi tool ‘ ipmitool’ [1] displays this as ‘SDR’ in the answer on command ‘ipmitool fwum status’.
	14	Module Geographical Address (slot number): 1 … = Module in chassis slot 1…
	15	Reserved
	16	Reserved

Get Release Information

	LUN	NetFn	CMD
Get Release Information	00h	OEM = 3Eh	01h

	Byte	Data Field
Request data	1…5	Token ~’C’ = BCh ~’6’ = C9h ~’9’ = C6h ~’2’ = CDh ~’3’ = CCh
Response data	1	Completion code
	2…6	Release
	7…12	Subrelease
	13…20	Date [YYYYMMDD]

Set Firmware Parameters

The command below permits the selection of interrupts to be used during KCS communication.

	LUN	NetFn	CMD
Set Firmware Parameters	03h	OEM = 3Eh	05h

	Byte	Data Field
Request data	1	Reserved B4h
	2	Reserved 90h
	3	Reserved 91h
	4	Reserved 8Bh
	5	Cmd Flags [6:2] Reserved [1] 0b = get only, 1b = set parameters [0] 0b = do not reset, 1b = reset Management Controller after setting parameters
	6	Operating Modes [7:5] Reserved [4] 0b = IPMB in redundancy [3:1] Reserved [0] 0b = BMC, 1b = SMC
	7	IRQ number FFh = do not use interrupts 0Ah = use IRQ10 0Bh = use IRQ11 Any other values Reserved.
Response data	1	Completion Code
	2	Cmd Flags
	3	Operating Modes
	4	IRQ number

Init Memory Clear

	LUN	NetFn	CMD
Init memory Clear	00h	OEM = 3Eh	A0h

	Byte	Data Field
Request data	1...5	Token ~'C' = BCh ~'6' = C9h ~'9' = C6h ~'2' = CDh ~'3' = CCh
	6	Action ID 00h: Memory Clear finished 01h: Start memory Clear Short 02h: Start memory Clear Long
	7	Reserved
Response data	1	Completion Code

4.4.2 Board Sensors

The Management Controller includes many sensors for voltage or temperature monitoring and various others for pass/fail type signal monitoring.

Every sensor is associated with a Sensor Data Record (SDR). Sensor Data Records contain information about the sensors identification such as sensor type, sensor name, sensor unit. SDRs also contain the configuration of a specific sensor such as thresholds, hysteresis, event generation capabilities, etc. that specify the sensor's behavior. Some fields of the sensor SDR are configurable through IPMI v1.5 command and are set to a built-in initial value.

Module sensors that have been implemented are listed in the sensor list below.

4.4.2.1 Sensor List

The sensor name (ID string) has a name prefix which is 'Sxx:' in the lists below. When reading the sensor name after module insertion this prefix becomes automatically adapted to the role (BMC or SMC) and the physical position (slot number) of the module in a rack. If the module's Management Controller is set up as a BMC the prefix will be 'BMC:' independent of the slot where it resides. If the module's Management Controller is set up as a SMC the prefix will be 'Sxx:' where xx is the slot number (e.g. 09).

The sensor number is the number which identifies the sensor e.g. when using the IPMI command "Get Sensor Reading". Please note that 'ipmitool' accepts sensor numbers in decimal (e.g. '10') or hexadecimal (e.g. '0xa') notation.

Please note that the IPMI tool ‘ipmitool’ displays for command ‘ipmitool sdr list’ the contents of the sensor data record repository (SDRR) of the whole rack if the SDRR is generated. The generation of the SDRR has always to be done new after adding or subtracting any board to or from the rack.

For OEM (Kontron) specific sensor types and reading types in the following table please refer to the next chapter.

Table 4-5: Sensor List

SENSOR Number / ID string	SENSOR TYPE (CODE) / EVENT/READING TYPE (CODE)	Ass. Mask/ Deass. Mask/ Reading Mask	DESCRIPTION
0 / Sxx:Watchdog	Watchdog2 (23h) / Sensor-specific (6Fh)	010Fh / 0000h / 010Fh	IPMI Watchdog
1 / Sxx:IPMB0 Link			
2 / Sxx:SEL State	Event Logging Disabled (10h) / Sensor-specific (6Fh)	003Ch / 0000h / 003Ch	State of event logging
3 / Sxx:IPMI Info-1	OEM Firmware Info 1 (C0h) / OEM (70h)	0003h / 0000h / 7FFFFh	For internal use only
4 / Sxx:IPMI Info-2	OEM Firmware Info 2 (C0h) / OEM (71h)	0003h / 0000h / 7FFFFh	For internal use only
6 / Sxx:FW Upg Mng	Firmware Upgrade Manager (C7h) / Sensor-specific (6Fh)	010Fh / 0000h / 010Fh	Status of Firmware Upgrade Manager
7 / Sxx:Temp PCB1	Temperature (01h) / Threshold (01h)	2285h / 2285h / 1B1Bh	Temp Board PCB1
8 / Sxx: Temp PHY 3	Temperature (01h) / Threshold (01h)	2285h / 2285h / 1B1Bh	Temp Board PHY3 / only present on revision 4 boards
9/ Sxx: Temp PHY 2	Temperature (01h) / Threshold (01h)	2285h / 2285h / 1B1Bh	Temp Board PHY2 / only present on revision 4 boards
10/ Sxx: Temp PCB2	Temperature (01h) / Threshold (01h)	2285h / 2285h / 1B1Bh	Temp Board PCB2 / only present on revision 4 boards
11/ Sxx: Temp PHY 1	Temperature (01h) / Threshold (01h)	2285h / 2285h / 1B1Bh	Temp Board PHY1 / only present on revision 4 boards

Table 4-5: Sensor List (continued)

SENSOR Number / ID string	SENSOR TYPE (CODE) / EVENT/READING TYPE (CODE)	Ass. Mask/ Deass. Mask/ Reading Mask	DESCRIPTION
12/ Sxx: Temp CC REF	Temperature (01h) / Threshold (01h)	2285h / 2285h / 1B1Bh	Temp Board CC REF / only present on revision 4 boards
13 / Sxx:Vcc 5.0v	Voltage (02h) / Threshold (01h)	2285h / 2285h / 1B1Bh	Board 5.0V supply
14 / Sxx:Icc 5.0v	Current (03h) / Threshold (01h)	0280h / 3280h / 1818h	Board 5.0V current
15 / Sxx:Vcc 3.3v	Voltage (02h) / Threshold (01h)	2285h / 2285h / 1B1Bh	Board 3.3V supply
16 / Sxx:Icc 3.3v	Current (03h) / Threshold (01h)	0280h / 3280h / 1818h	Board 3.3V current
17 / Sxx:Vcc 2.5v	Voltage (02h) / Threshold (01h)	2285h / 2285h / 1B1Bh	Board 2.5V supply
18 / Sxx:Vcc 1.85v	Voltage (02h) / Threshold (01h)	2285h / 2285h / 1B1Bh	Board 1.85V supply
19 / Sxx:Vcc 1.25v	Voltage (02h) / Threshold (01h)	2285h / 2285h / 1B1Bh	Board 1.25V supply
20 / Sxx:Vcc 1.0v	Voltage (02h) / Threshold (01h)	2285h / 2285h / 1B1Bh	Board 1.0V supply
21 / Sxx:Vcc 5.0vCPCI	Voltage (02h) / Threshold (01h)	2285h / 2285h / 1B1Bh	Board 5.0V CPCI supply
22 / Sxx:Vcc 3.3vCPCI	Voltage (02h) / Threshold (01h)	2285h / 2285h / 1B1Bh	Board 3.3V CPCI supply
23 / Sxx:Vcc 3.3vCPLD	Voltage (02h) / Threshold (01h)	2285h / 2285h / 1B1Bh	Board 3.3V CPLD supply
24 / Sxx:Icc 3.3vCPLD	Current (03h) / Threshold (01h)	0280h / 3280h / 1818h	Board 3.3V CPLD current

Table 4-5: Sensor List (continued)

SENSOR Number / ID string	SENSOR TYPE (CODE) / EVENT/READING TYPE (CODE)	Ass. Mask/ Deass. Mask/ Reading Mask	DESCRIPTION
25 / Sxx:Vcc 3.3v SUS	Voltage (02h) / Threshold (01h)	2204h / 2204h / 1212h	Board 3.3V SUS supply
26 / Sxx:Vcc 5.0vIPMB	Voltage (02h) / Threshold (01h)	2285h / 2285h / 1B1Bh	Board 5.0V IPMB supply
27 / Sxx:Icc 5.0vIPMB	Current (03h) / Threshold (01h)	0280h / 3280h / 1818h	Board 5.0V IPMB current
28 / Sxx:SFP-1 Status	Platform Alert (24h) / 'digital' Discrete (03h)	0000h / 0000h / 0007h	SFP1 Status
29 / Sxx:SFP-2 Status	Platform Alert (24h) / 'digital' Discrete (03h)	0000h / 0000h / 0007h	SFP2 Status
30 / Sxx:SFP-3 Status	Platform Alert (24h) / 'digital' Discrete (03h)	0000h / 0000h / 0007h	SFP3 Status
31 / Sxx:SFP-4 Status	Platform Alert (24h) / 'digital' Discrete (03h)	0000h / 0000h / 0007h	SFP4 Status
32 / Sxx:XFP-1 Status	Platform Alert (24h) / 'digital' Discrete (03h)	0000h / 0000h / 0007h	XFP1 Status
33 / Sxx:XFP-1 Status	Platform Alert (24h) / 'digital' Discrete (03h)	0000h / 0000h / 0007h	XFP1 Status
34 / Sxx:Board Reset	OEM (CFh) / 'digital' Discrete (03h)	0002h / 0000h / 0003h	Board reset event
35 / Sxx:Boot Cycle	OEM (C4h) / 'digital' Discrete (03h)	0001h / 0000h / 0001h	Board Boot Cycle
36 / Sxx:HandleSwitch	System Slot (21h) / 'digital' Discrete	0000h / 0000h / 0040h	Board Handle Switch
37 / Sxx:Memory State	Platform Alert (24h) / 'digital' Discrete	0002h / 0000h / 0003h	Board Memory State

4.4.2.2 Sensor Thresholds

Following tables show sensor thresholds for temperature, voltage and current sensors. E2 denotes values which are valid for the extended temperature range variantes CP6923-R-R2-E2 and CP6923-R-R3-E2.

Table 4-6: Temperature Sensor Thresholds [°C]

SENSOR Number / ID string	Lower critical	Lower non critical	Normal min	Nominal	Normal max	Upper non critical	Upper critical
7/Sxx:Temp PCB1	-4 E2: -42	4 E2: -36	25	25	79	80 E2: 89	85 E2: 94
8/Sxx: Temp PHY 3	0 E2: -42	0 E2: -36	25	25	100	112 E2: 119	125 E2: 124
9/Sxx: Temp PHY 2	0 E2: -42	0 E2: -36	25	25	100	112 E2: 119	125 E2: 124
10/ Sxx: Temp PCB2	0 E2: -42	0 E2: -42	25	25	100	105 E2: 89	110 E2: 94
11/ Sxx: Temp PHY 1	0 E2: -42	0 E2: -36	25	25	100	112 E2: 119	125 E2: 124
12/ Sxx: Temp CC REF	0 E2: -42	0 E2: -42	25	25	100	105 E2: 80	110 E2: 85

Table 4-7: Voltage/Current Sensor Thresholds

SENSOR Number / ID string	Lower critical	Lower non critical	Normal min	Nominal	Normal max	Upper non critical	Upper critical
13/ Sxx: Vcc 5.0v	4.641 V	4.760 V	4.784 V	4.998 V	5.331 V	5.355 V	5.450 V
14/Sxx: Icc 5.0v	n.a.	n.a.	n.a.	4.290 A	n.a	7.215 A	7.995 A
15/ Sxx:Vcc 3.3v	3.072 V	3.136 V	3.152 V	3.296 V	3.520 V	3.536 V	3.600 V
16/Sxx:Icc 3.3v	n.a.	n.a.	n.a.	4.745 A	n.a.	8.970 A	9.945 A
17/ Sxx:Vcc 2.5v	2.374 V	2.423 V	2.435 V	2.497 V	2.558 V	2.571 V	2.620 V
18/Sxx: Vcc 1.85v	1.744 V	1.784 V	1.793 V	1.852 V	1.911 V	1.921 V	1.950 V
19/Sxx: Vcc 1.25v	1.127 V	1.186 V	1.225 V	1.245 V	1.274 V	1.313 V	1.372 V
20/ Sxx: Vcc 1.0v	0.804 V	0.882 V	0.980 V	1.000 V	1.019 V	1.068 V	1.205 V
21/Sxx: Vcc 5.0vCPCI	4.641 V	4.760 V	4.784 V	4.998 V	5.331 V	5.355 V	5.450 V
22/Sxx: Vcc 3.3vCPCI	3.072 V	3.136 V	3.152 V	3.296 V	3.520 V	3.536 V	3.600 V
23/Sxx: Vcc 3.3vCPLD	3.072 V	3.136 V	3.152 V	3.296 V	3.520 V	3.536 V	3.600 V



Note...

LNR (Lower Non Recoverable) and UNR (Upper Non Recoverable) values and values marked n.a. are not defined.

4.4.2.3 OEM sensor types and OEM sensor event/reading types

Table 4-8: OEM sensor types

OEM SENSOR TYPE (CODE)	OEM EVENT/READING TYPE (CODE)	DESCRIPTION	
Firmware Info 1 (C0h)	70h	Internal Diagnostic Data	
Firmware Info 2 (C0h)	71h	Internal Diagnostic Data	
Initialization Agent (C2h)	03h (‘digital’ Discrete)	Offsets / events: 0: Initialization O.K. 1: Initialization Error	
IPMBL State (C3h)	6Fh (sensor type specific)	Sensor discrete State	Meaning
		08h	IPMB-L running
		others	IPMB-L not running
FRU Agent (C5h)	0Ah (Discrete)	FRU initialization agent, using a standard reading type.	
Post Value (C6h)	6Fh (sensor type specific)	Error is detected if the POST code is != 0 and doesn’t change for a defined amount of time. In case of no error: Bits [7:0] = POST code (payload Port 80h) In case of error: Bits [15:0] = 4000h Data2 = POST code, low nibble Data3 = POST code, high nibble	
Firmware Upgrade Manager (C7h)	6Fh (sensor type specific)	Offsets / events: 0 : First Boot after upgrade 1 : First Boot after rollback (error) 2 : First Boot after errors (watchdog) 3 : First Boot after manual rollback 4..7 : Reserved 8 : Firmware Watchdog Bite, reset occured	

4.4.2.4 IPMB Link Sensor

The CP6923 provides two IPMB links to increase communication reliability to the shelf manager and other IPM devices on the IPMB. These IPMB links work together for increased throughput where both busses are actively used for communication at any time. A request might be received over IPMB Bus A, and the response is sent over IPMB Bus B. Any requests that time out are retried on the redundant IPMB bus. In the event of any link state change, the events are written to the CP6923 SEL. The PM monitors the bus for any link failure and isolates itself from the bus if it detects that it is causing errors on the bus. Events are sent to signal the failure of a bus or, conversely, the recovery of a bus.

4.4.3 Board FRU Information

This FRU information contains the IPMI defined Board and Product Information areas that hold the part number and serial number of the board and the Multirecord Information Area that contains the PICMG defined Point to Point Information records.

The Internal Use Area is preallocated to 384 bytes and is free for customer use. This FRU information responds to FRU ID #0, which is the ID for the PM.

4.4.3.1 Structure and Functionality

The Management Controller provides 4 kB non-volatile storage space for FRU information.

Full low level access to read or write a module's FRU Information is provided by regular IPMI FRU Device commands. Please be careful when writing FRU information directly using standard IPMI commands because there is no write protection. Damaging the FRU Information e.g. may confuse a shelf management software which uses the FRU data.

4.4.3.2 Board Specific FRU Data

Supported are the following FRU data areas and data fields (shown values are examples, which may differ, depending on the used board typ):

FRU Board Info Area

- Manufacturing date / time
- Board manufacturer (C7): "Kontron"
- Board Product Name (C8): CP6923-R" *)
- Board Serial Number (CA): "1234567890" *)
- Board Part Number (C5): "12345" *)
- FRU File ID (C8): "CP6923-R -01" *)
- CustomData(D8): 'MAC=CC:CC:CC:CC:CC:CC/40" *)

FRU Product Info Area

- Product manufacturer(C7): "Kontron"
- Product Name (C8): "CP6923-R" *)
- Product Part Number (C5): "12345" *)
- Product Version (C2): "04"*)
- Product Serial Number (CA): "1234567890" *)
- Asset Tag (C0): not present
- FRU File ID (CB): "CP6923-R -01" *)

*) Shown values are examples and may differ depending on board variant.

4.4.4 PM Firmware Code

PM firmware code is organized into boot code and operational code, both are stored in a flash module. Upon an PM reset, the PM executes the boot code and performs the following:

1. Self test to verify the status of its hardware and memory.
2. Calculates a checksum of the operational code.
3. Communicates with the Firmware Upgrade Manager (FUM) in order to inform the PM watchdog that the current PM firmware is suitable for execution.

Upon successful verification of the operational code checksum, the firmware will jump to the operational code.

4.4.4.1 Health LED (Green LED)

The CP6923 Switch Board supports a Health LED mounted on the front panel. The following states are possible:

Table 4-9: Health LED state

LED state	Description
ON	normal state when board is in operation, PM is running.
Off	PM is not in operational status
Blinking	The FUM is programming the PM due to firmware update or rollback

4.4.4.2 Activity LED (Green LED)

The CP6923 supports a green Activity LED mounted on the front panel. The position of this LED is near the bottom handle beside the health LED. This heartbeat LED blinks every 4 seconds

Table 4-10: Activity LED state

LED state	Description
Blinking	Heartbeat of PM

4.5 Firmware Administration

A running CP6923 system requires – after the bootloader has passed control to the kernel – the kernel itself, the root file system (initrd), the FASTPATH switching application and a configuration file for the switch. These software components, together with the PM image, make up the CP6923 firmware.

The flash holding the software is divided into 7 partitions. There are partitions to store two bootloader and two Software Images integrating initrd, kernel and applications. Two partitions are reserved for the bootloader environments, one partition is used to hold up to nine images of the switching application (depending on the size of the images) and one partition is used to hold up to 99 configuration setting files. The partition scheme of the flash is shown below:

Table 4-11: FLASH Partition Scheme (64MB)

Partition	Size	MTD
U-Boot Loader primary image (write protected)	256KB	6
U-Boot Loader secondary image, updatable (optional)	256KB	5
U-Boot primary environment	256KB	4
U-Boot secondary environment	256KB	3
Software Image secondary partition (Image_B)	28MB	2
Software Image primary partition (Image_B)	28MB	1
JFFS Configuration File Partition CONFIGURATION text file F CONFIGURATION text file 01 CONFIGURATION text file ... CONFIGURATION text file 99 CONFIGSLOTS file containing multiple combination for selection through CLI	7MB	0

The firmware update procedure is designed to provide a fail-safe capability to update IPMI FW and Software settings separately. Each combination of these components can be used as a startup configuration, though they must be compatible to each other. Please allways follow Kontron documentation for all your upgrades. Software versions provided with an official release are known to work together.

In the following, the CLI commands to setup, change and activate startup configuration and the CLI commands necessary to perform firmware upgrades are described. The CLI commands described below are executed in the privileged mode of the CLI hierarchy, which is entered by executing the ‘enable’ command. Please refer to the “ *CP6923 CLI Reference Manual*“ for more information regarding the CLI commands and the way to use them.

4.5.1 Startup Configurations

A startup configuration is a combination of a software image and a configuration file for the switch. The IPMI FW image is not part of the configuration and is updated separately. Several configurations (up to 99) can be defined but only one is active at a time. To display the currently available startup configurations, the CLI command ‘show’ is used.

```
(Ethernet Fabric) #show startupconfig startup
ACT NR SYSTEM         BASE-CONFIG
--- -- -------------- ---------------
     F A CP6923 3.02  F  factory
*A  01 A CP6923 3.02  01 standard

(Ethernet Fabric) #
```

In this example, two startup configurations are available. Startup configuration 01 is the currently active configuration which is indicated by the ‘*’ in the first column. This configuration consists of:

- Software version GA 3.02 which is located in initrd partition A
- Switch configuration file which is stored in slot 01 of the configuration partition.

The user can define other startup configurations and combine images and configuration files as needed. To set up a new startup configuration, it is necessary to change into the CLI’s configuration mode using the ‘configure’ command. In this mode, the ‘startupslot’ command is used as shown in the following example:

```
(Ethernet Fabric) (Config)#startupslot 2 config 1 initrd A

Successfully set startup slot 2
You may mark it active now and reboot to use the new configuration.

(Ethernet Fabric) (Config)#exit

(Ethernet Fabric) #

(Ethernet Fabric) #show startupconfig startup
ACT NR SYSTEM         BASE-CONFIG
--- -- -------------  ---------------
     F A CP6923 3.02  F  factory
*A  01 A CP6923 3.02  01 standard
    02 A CP6923 3.02  01 standard

(Ethernet Fabric) #
```

A new startup configuration has been added to the list combining the software images given in the previous command.

The startup configuration created before can be deleted by entering exactly the same command string preceeded by ‘no’:

```
(Ethernet Fabric) (Config)#no startupslot 2 config 1 initrd A
```

The ‘show’ command can also be used to display available versions of initrd and configurations or all of them. The syntax is:

```
show startupconfig startup|sga-mapping|kernel|initrd|config|all
```

The configuration mode is also used to activate one of the available startup configurations. The syntax is:

```
startupslot 2 activate [once]
```

This command would activate the startup configuration 2 upon next system reset. The optional parameter ‘once’ would start configuration 2 only once after the next system reset and start the previously active configuration 1 on following resets. This is used to implement the failsafe upgrade procedure described below.

4.5.2 Updating Firmware

The firmware is updated using the CLI. To get a reliable and failsafe update procedure, the following precautions must be fulfilled:

- Two independent partitions for the initrd, one holding initrd A and the other one holding initrd B. The active system is either A or B. See the flash partition scheme shown above for more detail.
- One Time Boot capability: After having updated the inactive kernel and root file system, the new system has to be started by rebooting the board. In the case that the update has installed an inoperable system which would cause the board to hang when booting, the next board reset must restart the previous known good version of the initrd. This is achieved by programming the bootloader environment appropriately.
- Redundant bootloader environment sectors: When the system is updated, the bootloader environment must be changed to be able to start the updated version. The bootloader environment sector is stored twice in flash, one active version and one backup version in case the active version is deleted during update due to power loss or similar errors. In this case, the redundant environment would cause the bootloader to start the previous known good version of kernel and root file system.

A software update of the CP6923 Switch Board is done by performing the following steps:

1. Download initrd image into the appropriate slot of the flash memory. Ensure that the currently active image will not be overwritten.
2. Select a configuration for the switch for the new software release. This can be done by choosing the factory default or by storing the running system configuration into flash.
3. Create a startup configuration by combining the slots with the update image and the configuration slot for the switch.
4. Activate the selected startup configuration for One Time Boot.
5. Restart the board.
6. Activate the new startup configuration permanently

A software release for the CP6923 consists of one software package, that includes kernel, initrd and application software. The package is a tar archive containing the image itself and a MD5 checksum file for consistency check. The name of the package file is arbitrary but the file names in the archive must not be altered.

When performing a firmware update, the software package is loaded from a remote TFTP server in the first step. This is done by means of the frontpanel FE port of the Hub board. To load a software package via TFTP into a specified slot, the CLI command ‘download’ is used:

```
(Ethernet Fabric) #download initrd tftp://192.168.50.5/initrd.pkg B

Downloading image, this may take a while...
```

```
Successfully transferred kernel image tftp://192.168.50.5/initrd.pkg to slot B
You may mark it active now and reboot to use the new kernel image.

(Ethernet Fabric) #
```

This downloads the specified software package file via TFTP and writes the image into the initrd partition of the specified slot (B). The MD5 checksum of the image is checked before writing it into flash. It is important not to overwrite the slot containing the currently active software, otherwise the One Time Boot mechanism does not make sense.

After the software image has been downloaded into flash, the configuration slot for the switch must be selected. In case that no appropriate configuration the switch is available, the factory default configuration should be used for the startup configuration of the new software release. Alternatively, the running configuration settings of the switch can be stored on flash using the following CLI command:

```
(Ethernet Fabric) #copy system:running-config nvram:startup-config slot 3

This operation may take a few minutes.
Management interfaces will not be available during this time.

Are you sure you want to save? (y/n) y

Configuration Saved!

(Ethernet Fabric) #
```

Finally, a startup configuration containing the slot of the new software release and the configuration slot must be selected or a new startup configuration must be created as described above. After this step has been completed, the startup configuration is activated only for the next boot and the board is rebooted. This is done with the ‘startupslot’ CLI command in the configure mode:

```
(Ethernet Fabric) (Config)#startupslot 3 activate once
```

This command enables the startup configuration 3 only for the next system restart. In the case that the board hangs due to a corrupted software image, this will be detected and the board is automatically rebooted with the previous known good startup configuration. This way, a failsafe upgrade of the CP6923 software is possible.

To restart the board with the new startup configuration, the CLI command ‘reload’ is used:

```
(Ethernet Fabric) (Config)#reload
```

If the new startup configuration is considered functional after the reboot, it must be activated permanently, or else the one that is still active will be used again:

```
(Ethernet Fabric) (Config)#startupslot 3 activate
```

4.5.3 Updating IPMI

Updating the IPMI firmware is different from updating the other software parts as updating is done directly when invoking the download command. In the case that the update procedure fails or the update image is corrupted, the PM will be able to restart all the same by means of its rollback functionality. The IPMI Firmware file is stored in the result/ppc405/firmware path of the release directory tree. To update the IPMI firmware, the CLI command ‘download’ is used:

```
(Ethernet Fabric) #download ipmifw tftp://192.168.50.5/ipmi.pkg
```

```
Flashing a new IPMI firmware will disable the IPMI Controller for some minutes.
Are you sure to update the IPMI firmware? (y/n)y
...
(Ethernet Fabric) #
```