CXM-DIN2/3

Industrial Digital Input Module

Order No. 5262-00A/014
User's Manual
Publication No. 5262-UM-0101
Issue 1

Unpacking and Special Handling Instructions

This PepCard product is carefully designed for a long and fault-free life; nonetheless, its life expectancy can be drastically reduced by improper treatment during unpacking and installation.

Observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings, etc. If the product contains batteries for RTC or memory back-up, ensure that the board is not placed on conductive surfaces, including anti-static plastics or sponges. These can cause shorts and damage to the batteries or tracks on the board.

When installing the board, switch off the power mains to the chassis. Do not disconnect the mains as the ground connection prevents the chassis from static voltages, which can damage the board as it is inserted.

Furthermore, do not exceed the specified operational temperature ranges of the board version ordered. If batteries are present, their temperature restrictions must be taken into account.

Keep all of the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the board, re-pack it as it was originally packed.

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REVISION HISTORY
CXM-DIN2/3 User's Manual
5262-0-UM-0101

Issue	Brief Description of Changes	PCB Index	Date of Issue
1	First Issue	01	December, 1993

PCB Index = Printed Circuit Board/Schematics Revision Number. This column provides a valid "from—to" range for the PCB index covered by each issue. These numbers combine to form the last four digits of the publication number. "/n" numbers suffixed to the index number show modifications to a local instruction note (addition of wires).

Date of issue = the release date of the issue. This date does not necessarily reflect the date the improvements were first made.

A thick bar to the left of any text indicates that the text has changed from the previous issue of the manual.

A double thin bar to the left of any text indicates that new text (paragraphs) has been added.
Changes and additions to drawings and boxed text, such as notes or jumper setting tables, cannot be marked in the above way; therefore this marking system is used only for changes to "normal" body text.

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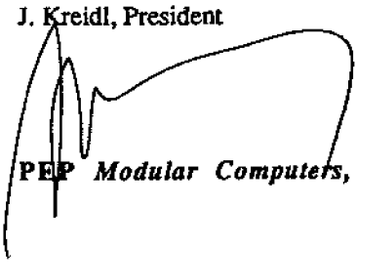
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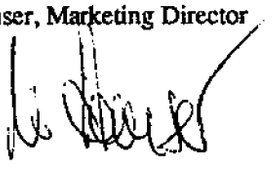
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PEP *Modular Computers*,

N. Hauser, Marketing Director



G. Rücker, Technical Director



Friday, July 29, 1988

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TABLE OF CONTENTS

Chapter/Section/Sub-section **Page**

1. Introduction **1-1**
1.1 Product Overview 1
1.2 Ordering Information 1
1.3 Specifications 2
1.4 Board Overview 3
1.5 Glossary of Terms 4
1.6 Related Publications 4
1.7 Block Diagram 4

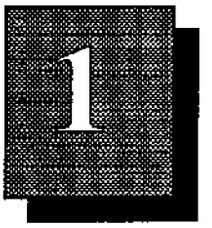
2. Functional Description **2-1**
Figure 2.0.0.1 Front Panel *1*
2.1 Addressing the Board 2
2.1.1 CXC 2
2.2 CXM-DIN2/3 Address Map 3
2.2.1 Inputs 3
2.2.2 ID Byte 3

3. Configuration **3-1**
Figure 3.0.0.1 Solder Jumper Location *1*
3.1 Jumpers and Chip Select 2

4. Pin-outs **4-1**
Figure 4.0.0.1 Connector Locations *1*
4.1 ST1 Screw Terminal (Phoenix) 2
Figure 4.1.0.1 Input Connection 2
4.2 ST3A/B/C CXC Connector 3
4.3 BU4 3

Appendix Controller eXtension Connector
Insertion A Board Layout
Insertion B Circuit Diagram

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1. INTRODUCTION

1.1 Product Overview

The CXM-DIN2 and CXM-DIN3 are digital input piggybacks for the CXC interface. The DIN2 has 24 opto-isolated inputs for 24V, whilst the DIN3 has 24 opto-isolated inputs for up to 60V, both are with LED and screw terminal. Both are operated by the CXC.

1.2 Ordering Information

Name	Description	Order Nr.
CXM-DIN2	24 opto-isolated inputs for 24V	5262-00A
CXM-DIN3	24 opto-isolated inputs for up to 60V	5262-014

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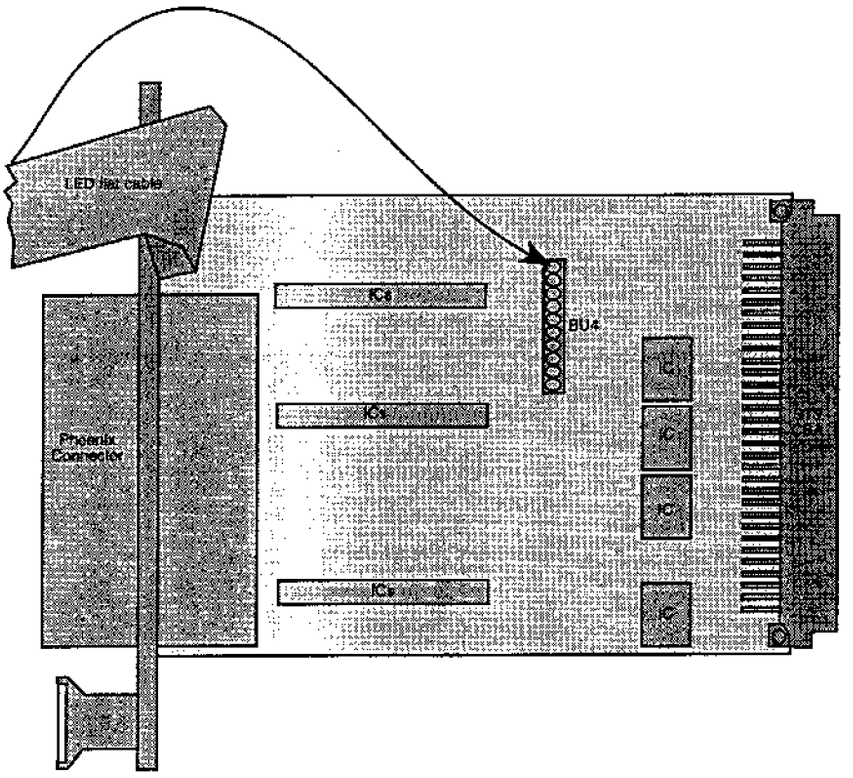
1.3 Specifications

Input	24 digital
Isolation	opto-coupler
Isolation voltage	1500V external to internal according to VDE 0805 A / EN 60950, table 6
Input voltage range	
CXM-DIN2	0-24V
CXM-DIN3	0-60V
Input signal	DC
Relation between inputs	two groups of 12 with common ground
Low signal voltage	0...8V
Low signal external	"0" internal at data bus
High signal voltage	10...60V
High signal external	"1' internal at data bus
Switching level	
CXM-DIN2	approx. 10V
CXM-DIN3	approx. 9V
Input current high	
CXM-DIN2	3mA at 24V, dependent of input voltage
CXM-DIN3	4mA independent of input voltage
Switch ON delay	approx. 2ms (at 24V)
Switch OFF delay	approx. 2ms
Filter	low pass 2ms/200Hz
Overvoltage protection	300V / <10µs
LED	green with external high signal
LED position	internal circuit
ID Byte	
CXM-DIN2	$A
CXM-DIN3	$14
General Specifications	
Power supply	+5V DC (via CXC)
Supply current (typ.)	20mA (LEDs off), 80mA (LEDs on)
Operating temperature	0...70°C standard, -40...85°C extended
Storage temperature	-55...85°C
Operating humidity	0...95% non-condensing

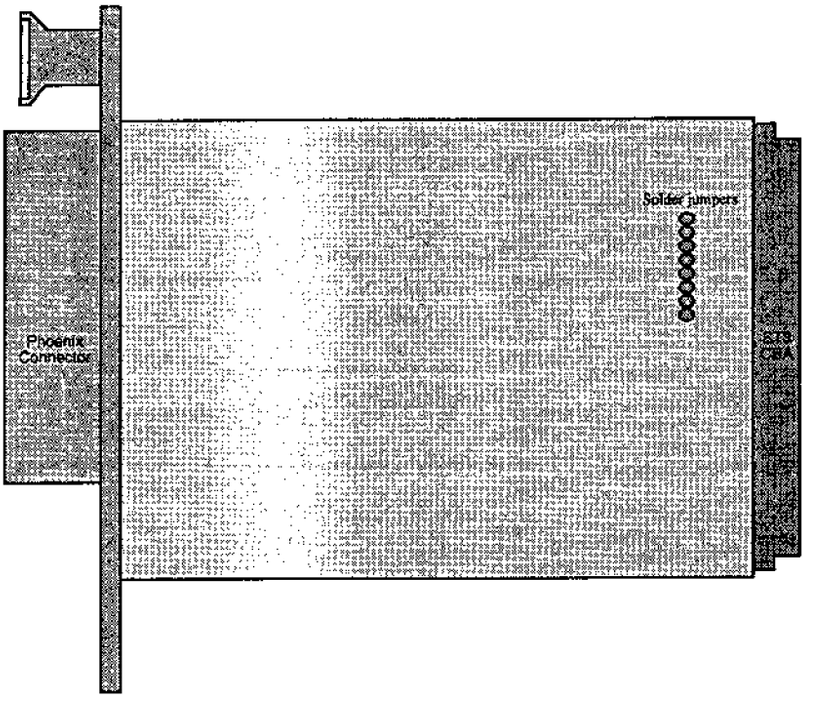
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1.4 Board Overview

Component Side



Solder Side



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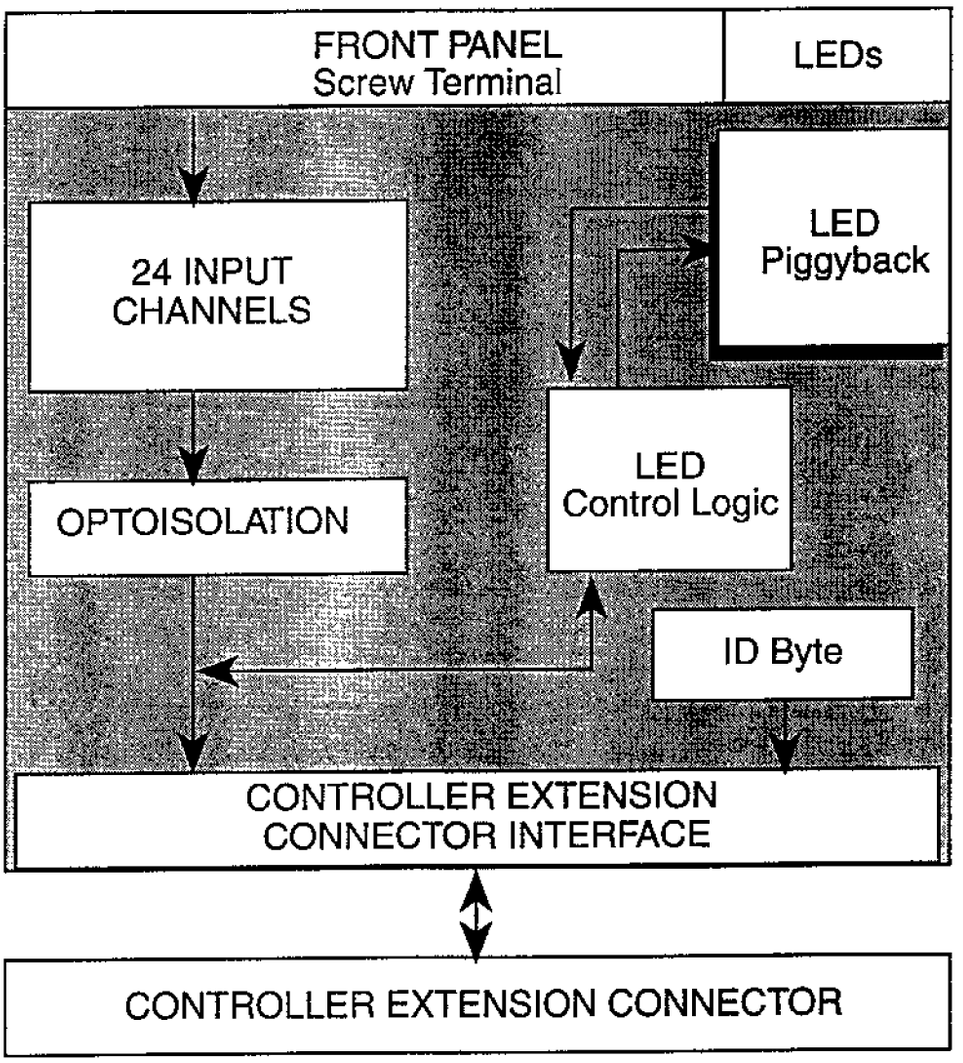
1.5 Glossary of Terms

CXC Controller eXtension Connector
CXM Controller eXtension Module

1.6 Related Publications

PEP CXC Specification Manual

1.7 Block Diagram

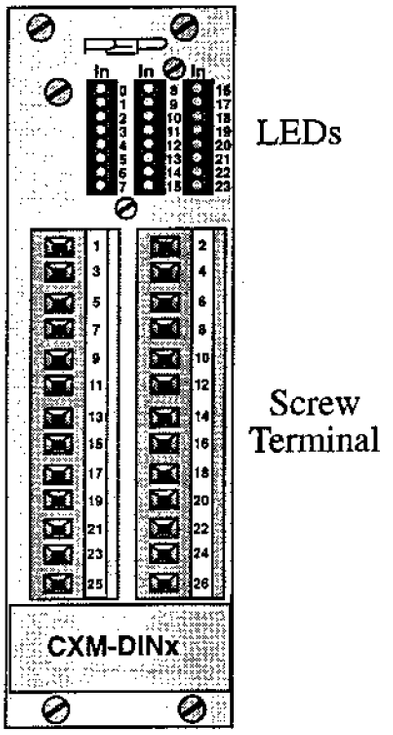


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2

2. FUNCTIONAL DESCRIPTION

Figure 2.0.0.1 Front Panel



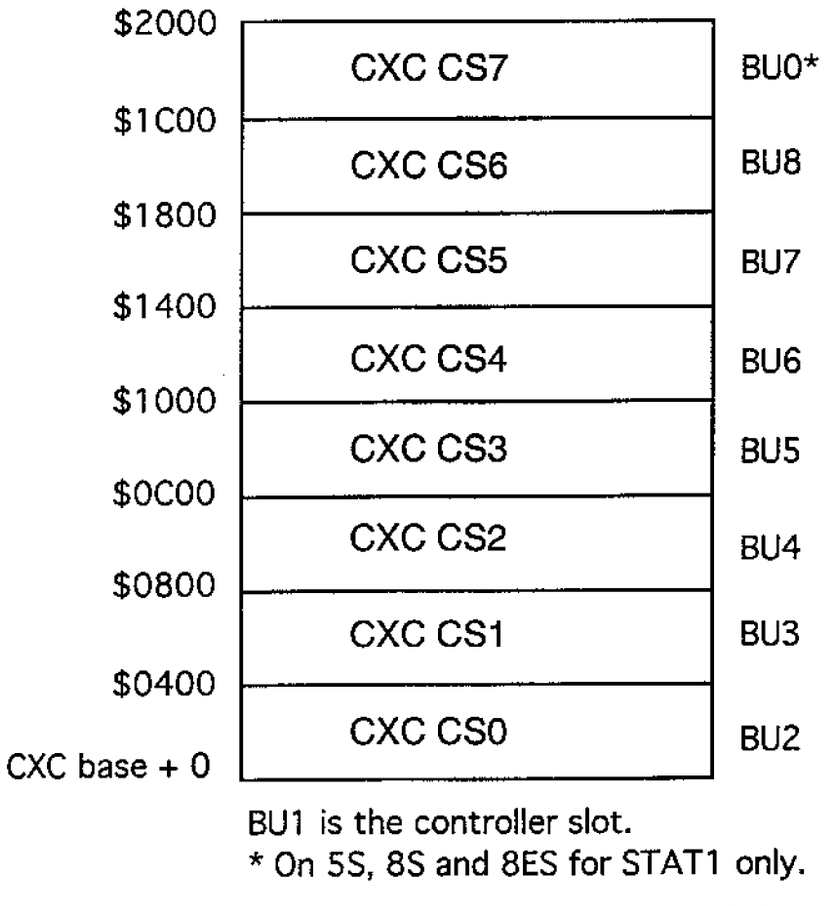
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2.1 Addressing the Board

The CS-CXM (internal 68302 chip select logic, initialised to $F70000 for the [V]IUC/VSBC-4 and $C1F70000 for the VM30 by the PEPbug), is the base for the CXC chip select CS0...CS7, with $400 offset steps. The CS-CXM is programmed via the chip select registers inside the 68302 for chip select line CS3 (please refer to the PEP [V]IUC manual or the 68302 manual). Please refer to Appendix CXC Backplanes.

2.1.1 CXC

The base address of the CXC is programmable via CS3 of the MC68302 (internal chip select logic).



CXC.address.map

CXC Base Address	Board Type
$C1F70000	VM30
$F70000	[V]IUC and VSBC-4

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2.2 CXM-DIN2/3 Address Map

Address	Byte/Word	Read/Write	Function
BASE + $00 BASE + $02	Dependent on register access	Read / Write	Inputs
BASE + $FF	Byte	Read	ID Byte

2.2.1 Inputs

The addresses for the inputs are dependant on the type of register access employed by the user. There are three types of register access possible; *byte access*, *word access* and *long word access*. The address maps for each case are shown below.

Byte Access

	D7	D0
BASE+$00	IN7 - IN0	
BASE+$01	IN15 - IN8	
BASE+$02	IN23 - IN16	

Word Access

	D15	D7	D0
BASE+$00	IN15 - IN0		
BASE+$02	Not used	IN23 - IN16	

Long Word Access

	D31	D23	D0
BASE+$02*	Not used	IN23 - IN0	

* In order that the data is accessed in the correct order using long word access, the data is situated at the address BASE + $02.

2.2.2 ID Byte

An ID Byte is present at address BASE + $FF. It has a value of:

CXM-DIN2 = $A
CXM-DIN3 = $14

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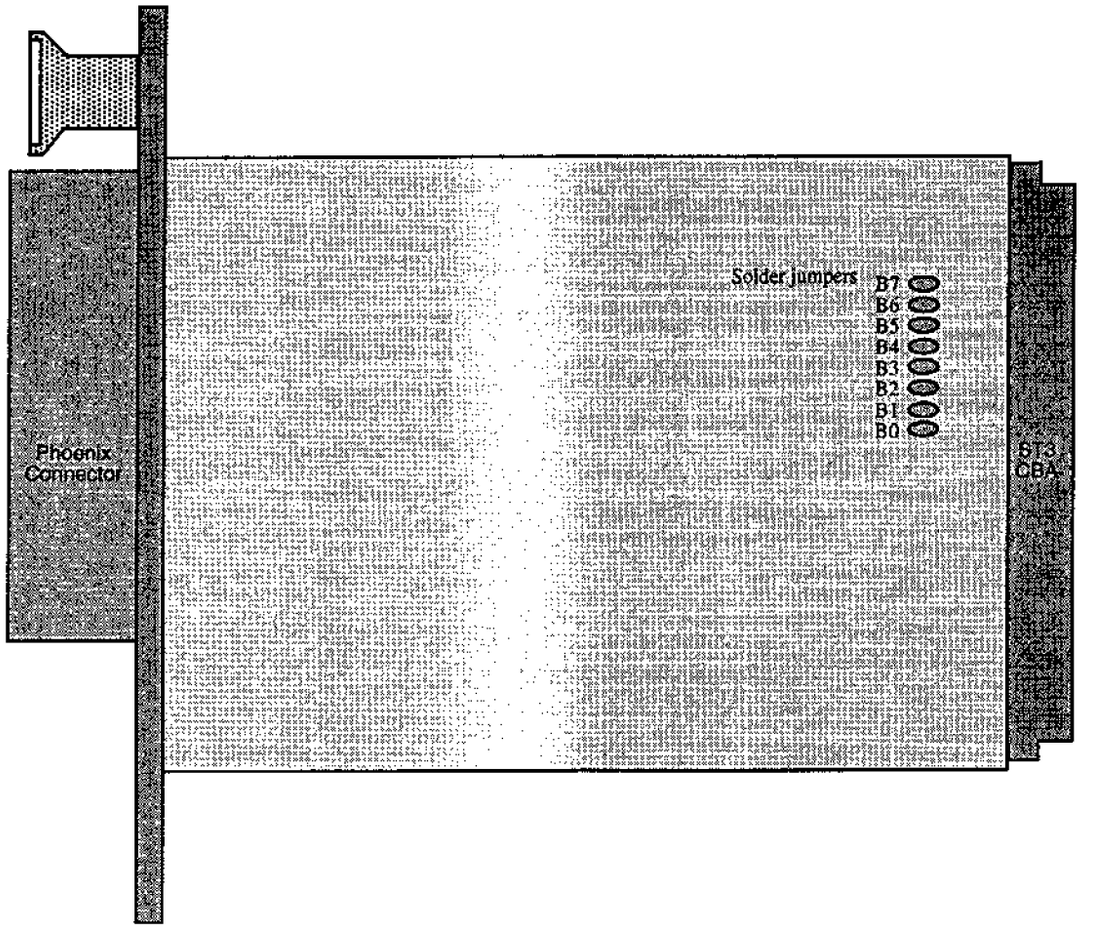
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3

3. CONFIGURATION

There are 8 solder jumpers on the solder side of the board. These are used for selecting the base address.

Figure 3.0.0.1 Solder Jumper Location



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3.1 Jumpers and Chip Select

B1	B2	B3	B4	B5	B6	B7	B8	CXC
set	open	open	open	open	open	open	open	CS0 of CXC is board select
open	set	open	open	open	open	open	open	CS1 of CXC is board select
open	open	set	open	open	open	open	open	CS2 of CXC is board select
open	open	open	set	open	open	open	open	CS3 of CXC is board select
open	open	open	open	set	open	open	open	CS4 of CXC is board select
open	open	open	open	open	set	open	open	CS5 of CXC is board select
open	open	open	open	open	open	set	open	CS6 of CXC is board select
open	open	open	open	open	open	open	set	CS7 of CXC is board select
set	*set*	*set*	*set*	*set*	*set*	*set*	*set*	*default setting**

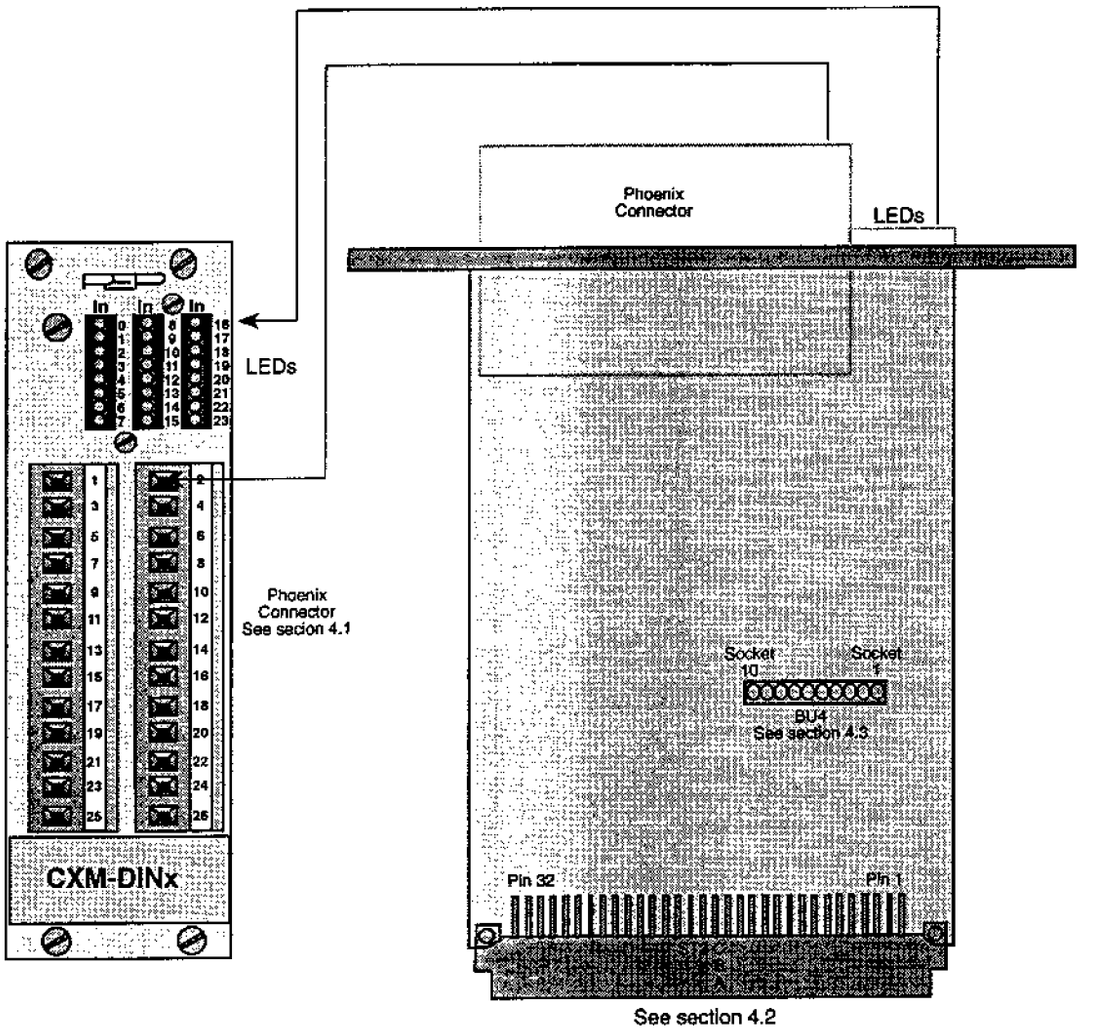
* For use with CXC, with identical jumper settings on several boards. This setting allocates one chip-select per slot, addressing all the boards.

See also Appendix CXC

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4. PIN-OUTS

Figure 4.0.0.1 Connector Locations



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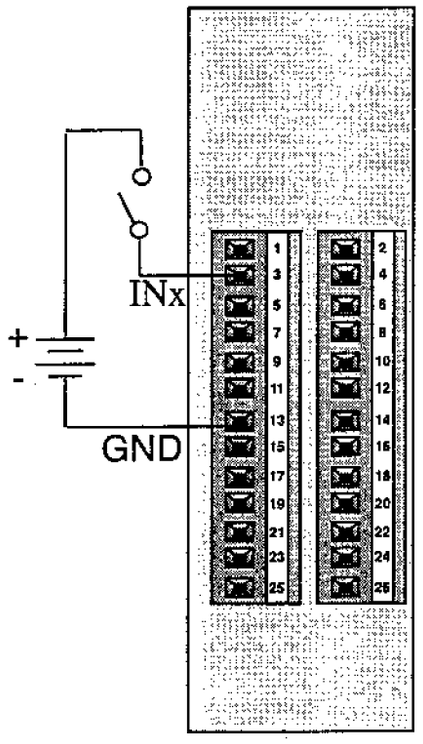
4.1 ST1 Screw Terminal (Phoenix)

PIN #	INPUT #	PIN #	INPUT #
1	IN0	2	IN1
3	IN2	4	IN3
5	IN4	6	IN5
7	IN6	8	IN7
9	IN8	10	IN9
11	IN10	12	IN11
13	PGND0	14	PGND1
15	IN12	16	IN13
17	IN14	18	IN15
19	IN16	20	IN17
21	IN18	22	IN19
23	IN20	24	IN21
25	IN22	26	IN23

The input circuit on the process side is divided into two process ground planes connected over two pins.

PGND0	IN0-IN11
PGND1	IN12-IN23

Figure 4.1.0.1 Input Connection



Switch	Read
Open	Logical 0
Closed	Logical 1

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4.2 ST3A/B/C CXC Connector

Situated at the rear of the board this is the boards Controller eXtension Connector (CXC) and has three rows. The CXM-STAT1 can be used with all backplanes and in any slot. Optimal results are obtained by using slot 2 with CS0.

Pin Number	Row A Signals	Row B Signals	Row C Signals
1	PB11 (INTERRUPT)	Rclk1 (SCC1)	PA15/DONE (IDMA)
2	PB10 (INTERRUPT)	Tclk1 (SCC1)	PA14/DACK (IDMA)
3	PB9 (INTERRUPT)	GND	PA13/DREQ (IDMA)
4	PB8 (INTERRUPT)	TxD1 (SCC1)	PA12/BRG3 (SCC3)
5	PB7/WDOG	RTS1* (SCC1)	PA11/Tclk3 (SCC3)
6	PB6/TOUT2	GND	PA10/Rclk3 (SCC3)
7	VCC	RTS3* (SCC3)	VCC
8	PB5/TIN2	CD3* (SCC3)	PA9/TxD3 (SCC3)
9	PB4/TOUT1	GND	PA8/RxD3 (SCC3)
10	PB3/TIN1	RxD1 (SCC1)	PA7/BRG2/SDS2 (SCC2)
11	PB2	BRG1 (SCC1)	PA6/CD2 (SCC2)
12	PB1	GND	PA5/RTS2 (SCC2)
13	PB0	CTS1* (SCC1)	PA4/CTS2 (SCC2)
14	VCC	CD1* (SCC1)	VCC
15	CS-CXC* (CS3 of 68302)	GND	PA3/Tclk2 (SCC2)
16	IAS*	CTS3*	PA2/Rclk2 (SCC2)
17	R/W	SYSR*	PA1/TxD2 (SCC2)
18	UDS*	GND	PA0/RxD2 (SCC2)
19	LDS*	EDTACK*	VCC
20	VCC	16MHz CLOCK	CXC CS2*
21	A1	GND	CXC CS3*
22	A2	CXC CS0*	CXC CS4*
23	A3	CXC CS1*	CXC CS5*
24	A4	GND	CXC CS6*
25	A5	A6	CXC CS7*
26	VCC	A7	VCC
27	D0	GND	D10
28	D1	D6	D11
29	D2	D7	D12
30	D3	GND	D13
31	D4	D8	D14
32	D5	D9	D15

See also Appendix CXC

4.3 BU4

This is the socket row for the LED piggyback connection.

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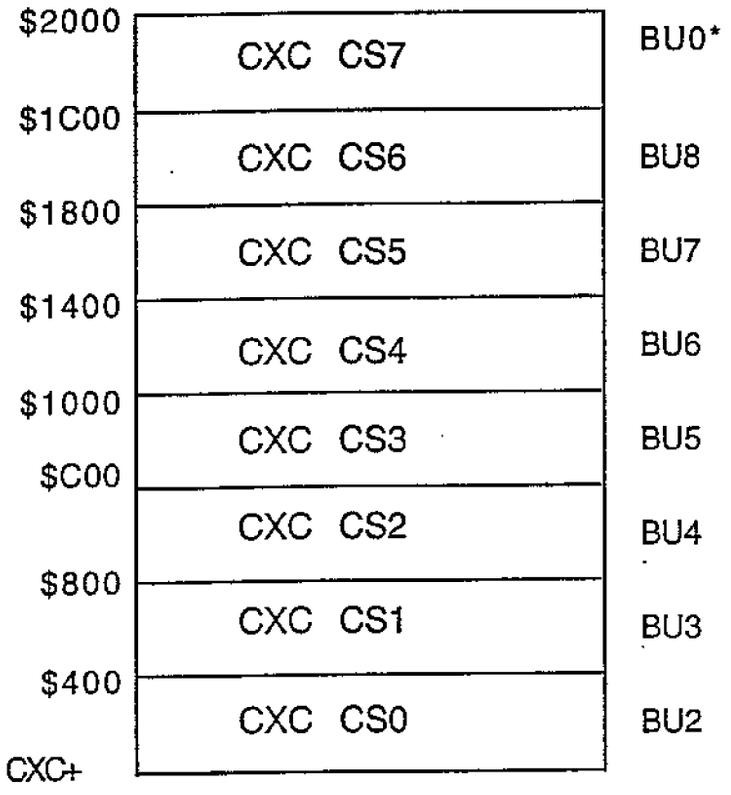
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APPENDIX CONTROLLER EXTENSION CONNECTOR

The Controller eXtension Connector (CXC) is the local interface. It contains a 16-bit data bus, 7 address lines, and 8 decoded chip select lines. Each chip select line has 256 bytes. Overall there are 8 control signals.

Figure 1.0.0.4 CXC Address Range

The base address of the CXC can be programmed via CS3 of the MC68302 (internal chip select logic). CS3 has a default of F70000 on the [V]IUC and VSBC-4, and C1F70000 on the VM30 and VIUC30.



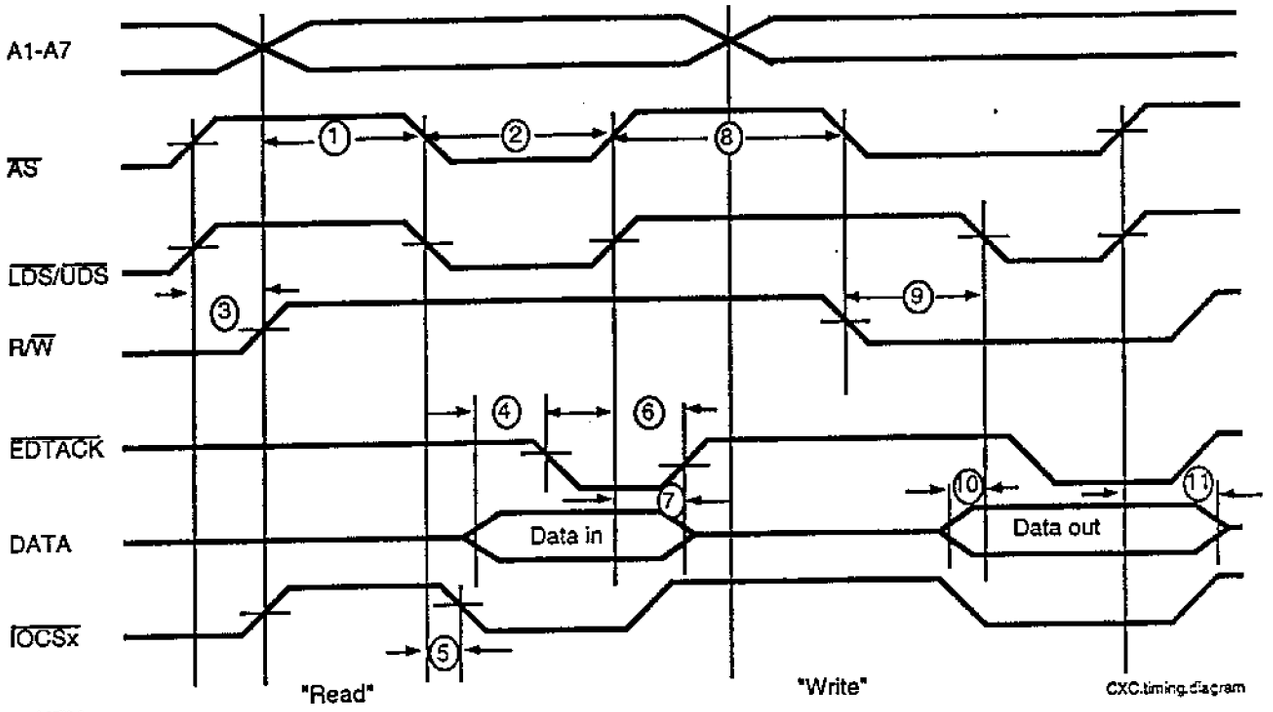
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2 Pin-outs

Pin Number	Row A Signals	Row B Signals	Row C Signals
1	PB11 (INTERRUPT)	Rclk1 (SCC1)	PA15/DONE (IDMA)
2	PB10 (INTERRUPT)	Tclk1 (SCC1)	PA14/DACK (IDMA)
3	PB9 (INTERRUPT)	GND	PA13/DREQ (IDMA)
4	PB8 (INTERRUPT)	TxD1 (SCC1)	PA12/BRG3 (SCC3)
5	PB7/WDOG	RTS1* (SCC1)	PA11/Tclk3 (SCC3)
6	PB6/TOUT2	GND	PA10/Rclk3 (SCC3)
7	VCC	RTS3* (SCC3)	VCC
8	PB5/TIN2	CD3* (SCC3)	PA9/TxD3 (SCC3)
9	PB4/TOUT1	GND	PA8/RxD3 (SCC3)
10	PB3/TIN1	RxD1 (SCC1)	PA7/BRG2/SDS2 (SCC2)
11	PB2	BRG1 (SCC1)	PA6/CD2 (SCC2)
12	PB1	GND	PA5/RTS2 (SCC2)
13	PB0	CTS1* (SCC1)	PA4/CTS2 (SCC2)
14	VCC	CD1* (SCC1)	VCC
15	CS-CXC* (CS3 of 68302)	GND	PA3/Tclk2 (SCC2)
16	IAS*	CTS3*	PA2/Rclk2 (SCC2)
17	R/W	SYSR*	PA1/TxD2 (SCC2)
18	UDS*	GND	PA0/RxD2 (SCC2)
19	LDS*	EDTACK*	VCC
20	VCC	16MHz CLOCK	CXC CS2*
21	A1	GND	CXC CS3*
22	A2	CXC CS0*	CXC CS4*
23	A3	CXC CS1*	CXC CS5*
24	A4	GND	CXC CS6*
25	A5	A6	CXC CS7*
26	VCC	A7	VCC
27	D0	GND	D10
28	D1	D6	D11
29	D2	D7	D12
30	D3	GND	D13
31	D4	D8	D14
32	D5	D9	D15

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3 Timing



KEY

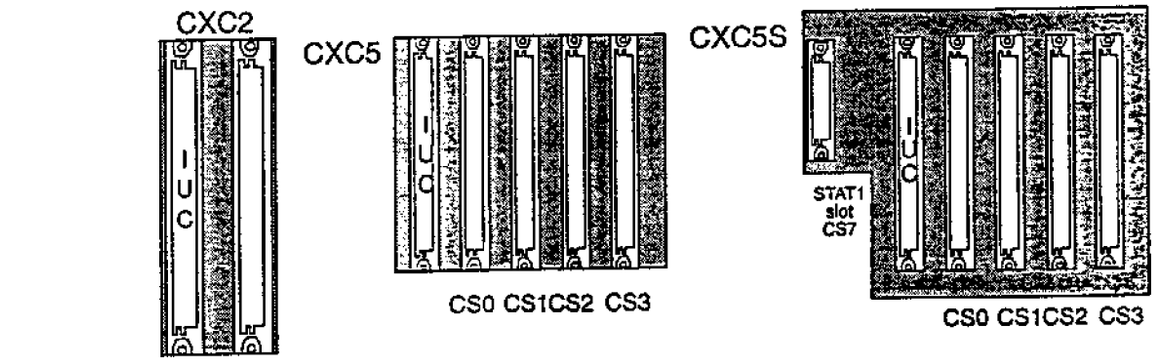
	min	max
1. Address valid to AS, DS	15ns	-
2. AS asserted	120ns	-
3. AS negated to R/W invalid	15ns	-
4. Data-in valid to EDTACK	0ns	-
5. IOCSx asserted to AS valid	-	25ns
6. EDTACK negated to AS negated	0ns	111ns
7. Data-in hold time	0ns	50ns
8. AS negated	60ns	-
9. AS, R/W asserted to DS asserted	30ns	-
10. Data-out valid to DS asserted	15ns	-
11. AS,DS negated to data-out invalid	15ns	-

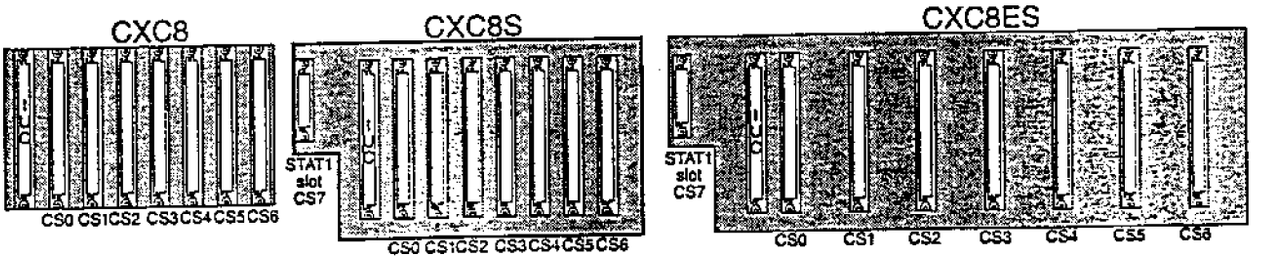
A1-A7: address lines
AS: address strobe
LDS/UDS: lower/upper data strobe
R/W: read not write
EDTACK: external data transfer acknowledge
IOCSx: IOCS0 to IOCS7

Recommended: Assert EDTACK with CSx and UDS/LDS and "data valid" during read
Latch data with CSx and UDS/LDS during write
Negate EDTACK with UDS/LDS invalid

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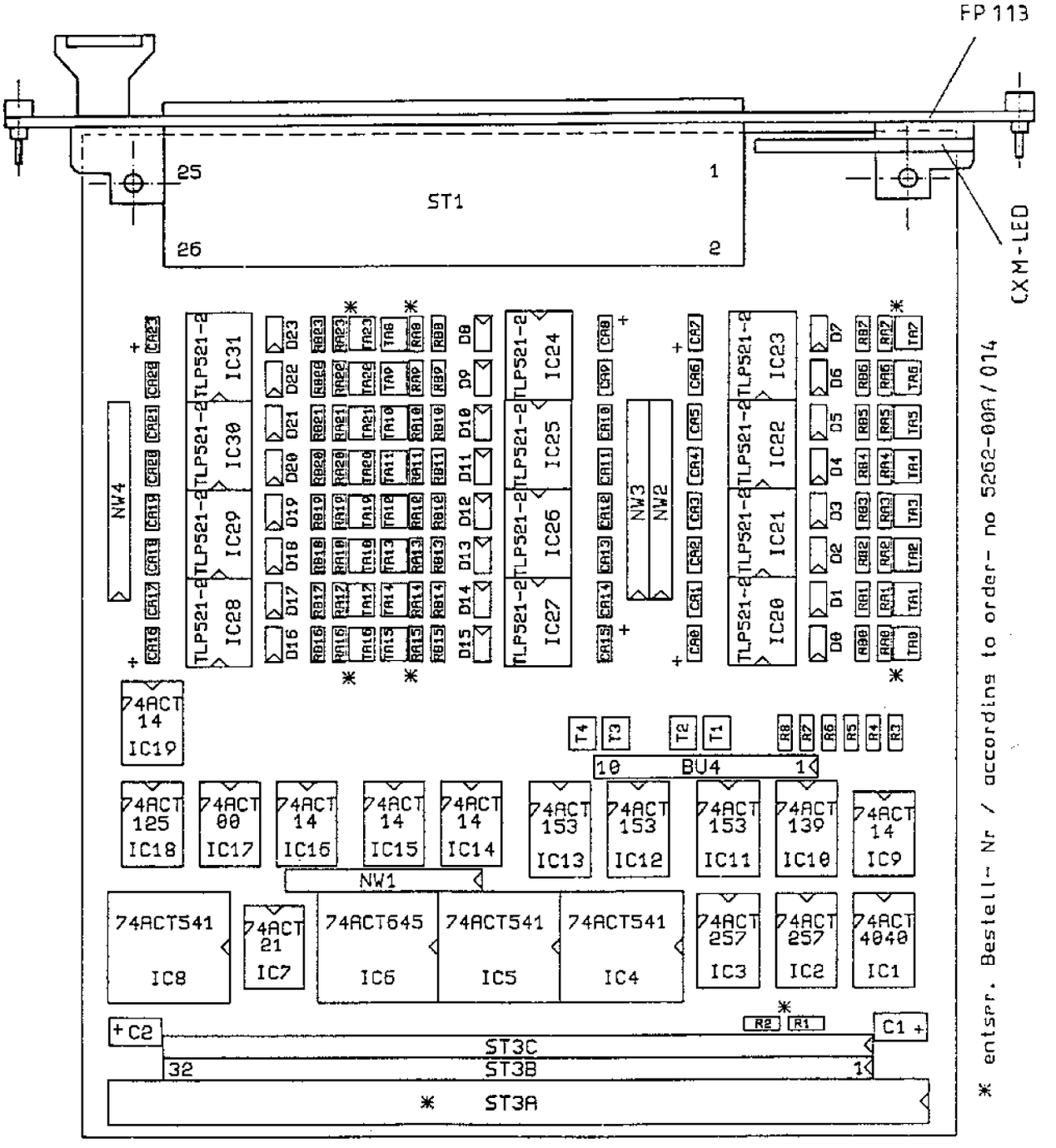
4. Connector Extension Connectors





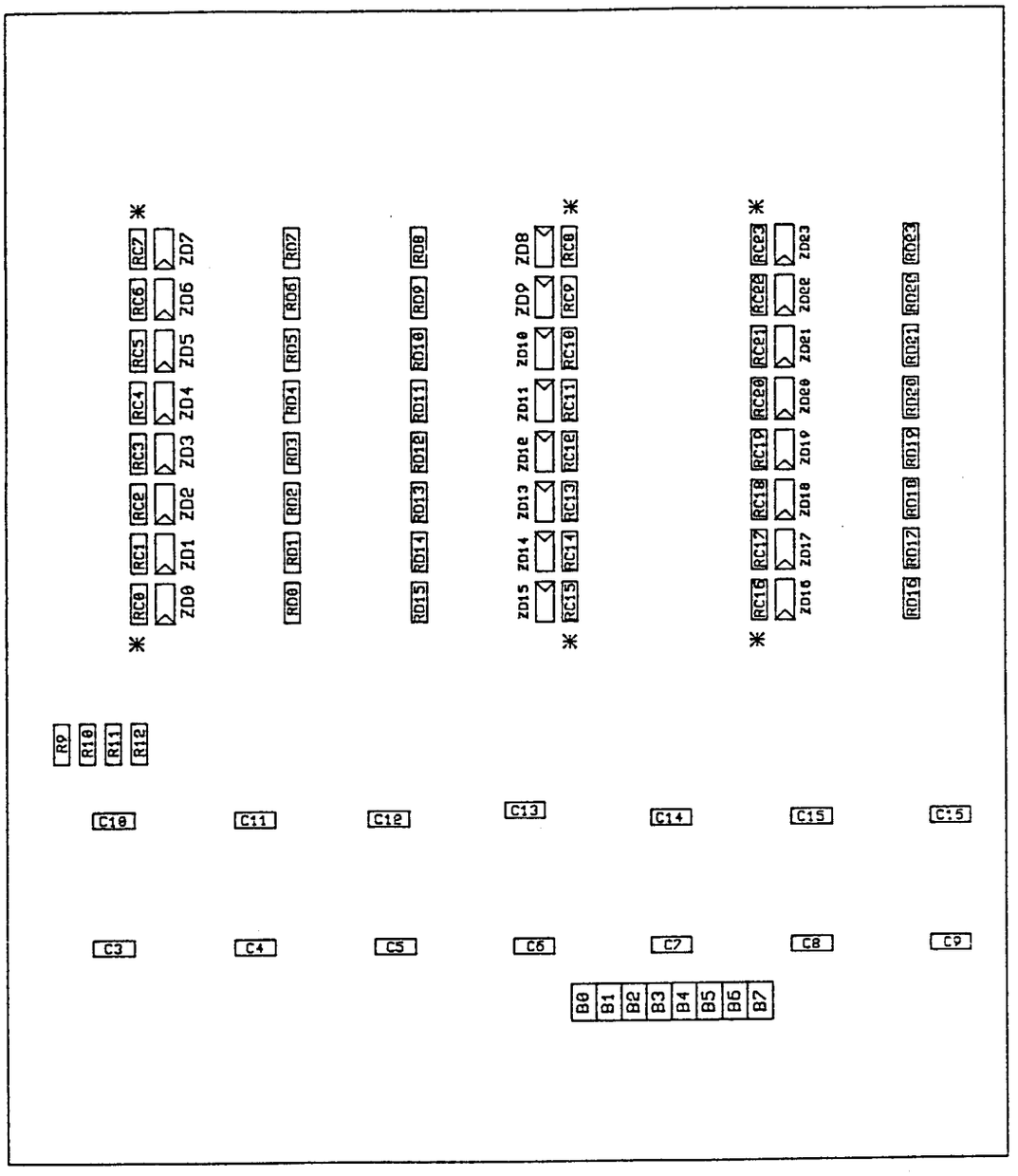
When using an 8TE board on the CXC5/5S/8/8S note that a slot will be lost between each borad. The CXC8ES has been designed specifically with this problem in mind, and no slots will be lost.

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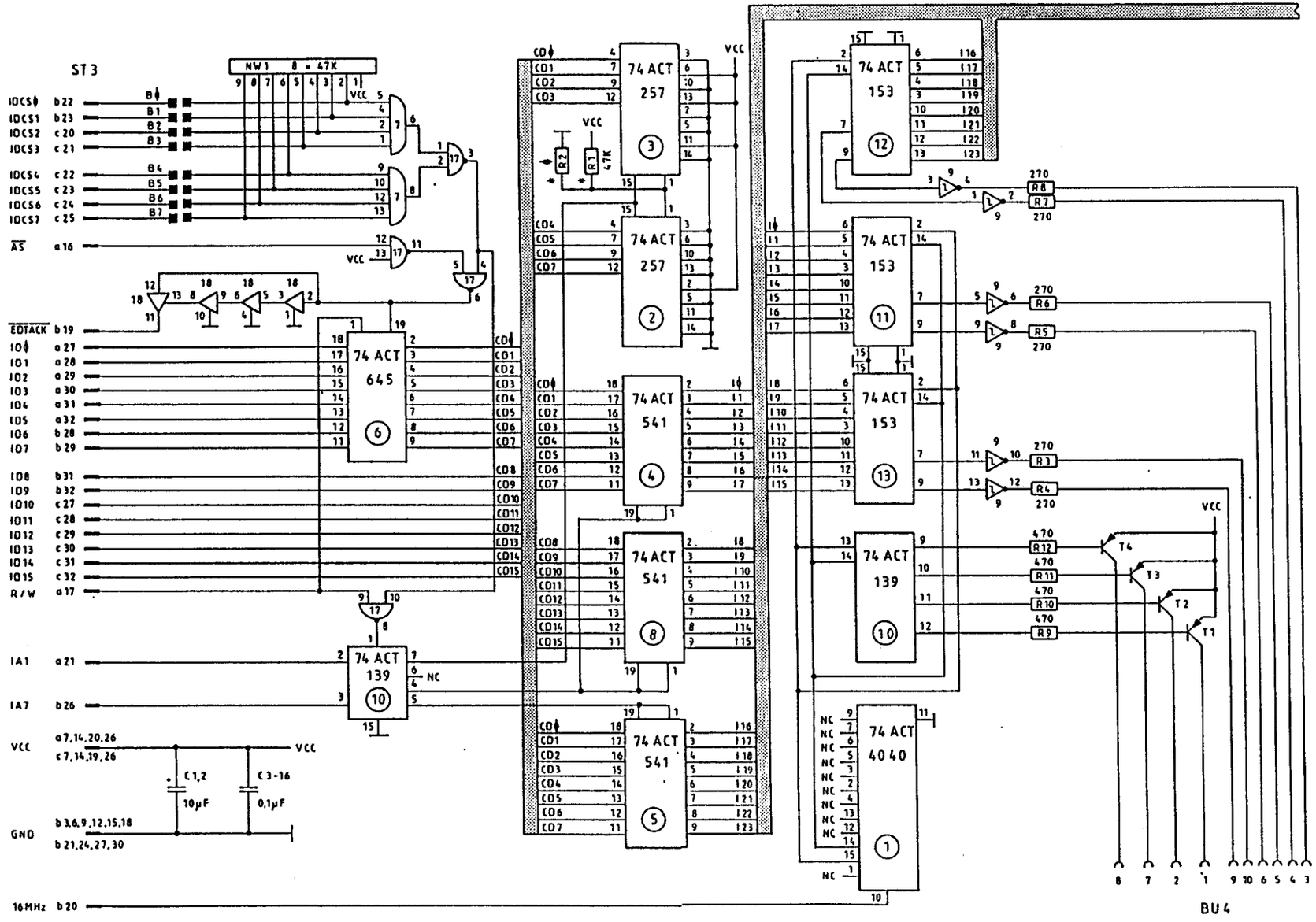


B-Seite / B-side

Modular Computers®	CXM – DIN 2/3		31.125 –1200.1
	Date	Mar 08,1993	Index 01
			Page 1 of 2



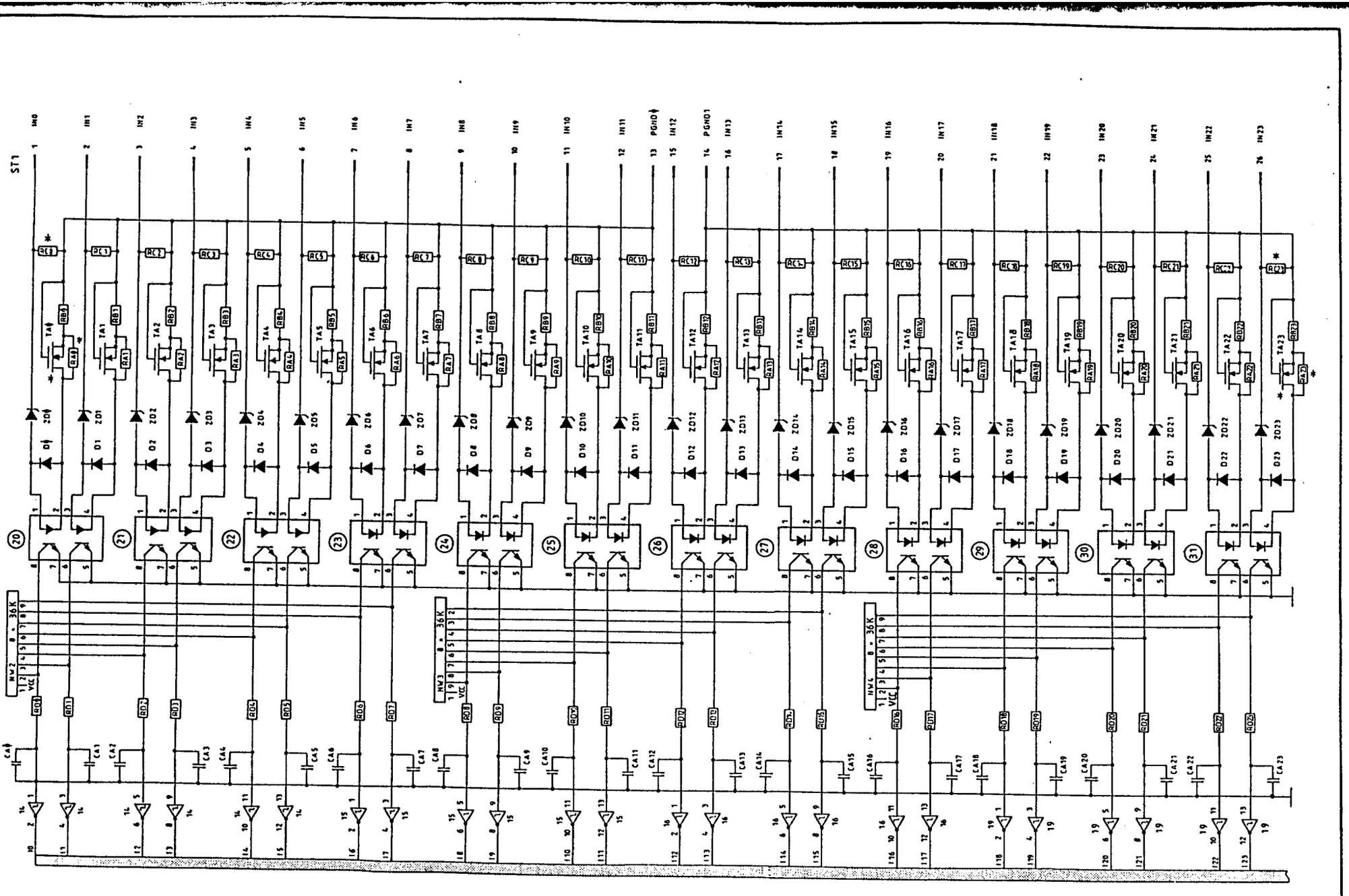
L-Seite / L-side



IC 17	74 ACT 00
IC 9,14,15,16,19	74 ACT 14
IC 7	74 ACT 21
IC 18	74 ACT 125
IC 20-31	TLP 521
RA∮-23	4,7K
RB∮-23	470
RC∮-23	100K
RD∮-23	36K
D∮-23	LL4448
ZD∮-23	BZV 55 C8V2
CA∮-23	0,1µF
T1-4	2N2907
TA∮-23	BSS139

* entspr. Bestell-Nr. / according to order-no 5262-00A/014

Modular Computers®	CXM - DIN 2/3	31.125-1200.1	
	Date Mar 08,1993	Index	01
		Page 1	of 2



Modular Computers®

CXM - DIN2/3		31.125 - 1200.1	
Date	Mar 08,1993	Index	01
		Page 2	of 2