CXM-DIO3

Industrial I/O Module

Order No.-5262-005
User's Manual
Publication No. 5262-UM-0101
1st Issue

Unpacking and Special Handling Instructions

This PepCard product is carefully designed for a long and fault-free life; nonetheless, its life expectancy can be drastically reduced by improper treatment during unpacking and installation.

Observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings, etc. If the product contains batteries for RTC or memory back-up, ensure that the board is not placed on conductive surfaces, including anti-static plastics or sponges. These can cause shorts and damage to the batteries or tracks on the board.

When installing the board, switch off the power mains to the chassis. Do not disconnect the mains as the ground connection prevents the chassis from static voltages, which can damage the board as it is inserted.

Furthermore, do not exceed the specified operational temperature ranges of the board version ordered. If batteries are present, their temperature restrictions must be taken into account.

Keep all of the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the board, re-pack it as it was originally packed.

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REVISION HISTORY
CXM-DIO3 User's Manual
5262-UM-0101

Issue	Brief Description of Changes	PCB Index	Date of Issue
1	Issue	01-01	July 1992
1	Issue 1 Corrections to Figs. 2 and 2.5, Table 4.0.0.2	01-01	20th January 1993

Issue = Manual Issue Number . Capital letters indicate draft issues. (P) indicates a preliminary version. Lower case letters suffixed to the issue number on the title page indicate a minor correction.

PCB Index = Printed Circuit Board/Schematics Revision Number. This column provides a valid "from—to" range for the PCB index covered by each issue. These numbers combine to form the last four digits of the publication number. "/n" numbers suffixed to the index number show modifications to a local instruction note (addition of wires).

Date of issue = the release date of the issue. This date does not necessarily reflect the date the improvements were first made.

A thick bar to the left of any text indicates that the text has changed from the previous issue of the manual.

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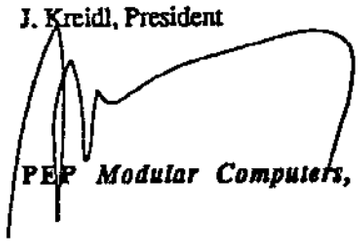
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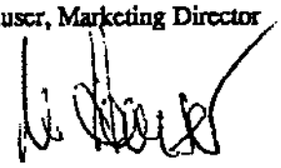
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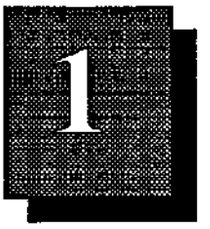
Friday, July 29, 1988

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1. INTRODUCTION

1.1 Product Overview

The CXM-DIO3 is a 24 channel digital input/output interface for the IUC9000 system. It provides 16 optoisolated digital inputs and 8 optoisolated outputs for use with industry standard externally powered 24V dc equipment. There is also an external reset input channel to set all outputs into a logic low state, i.e. emergency stop.

A green LED status display for input channels, a yellow LED status display for output channels and a green LED status display for external power, provide a rapid overview of the boards operating status.

The CXM-DIO3 is equipped with a Phoenix screw terminal for industrial environments.

1.2 Ordering Information

Name	Description	Order Number
CXM-DIO3	Digital I/O 16 optoisolated channels, inputs 24Vdc and 8 outputs, 24Vdc, 500mA	5262-005

1.3 Glossary of Terms

CXC Controller eXtension Connector allows an additional 7 CXMs to be added to the board
CXM Controller eXtension Module allows functions to be added to the board

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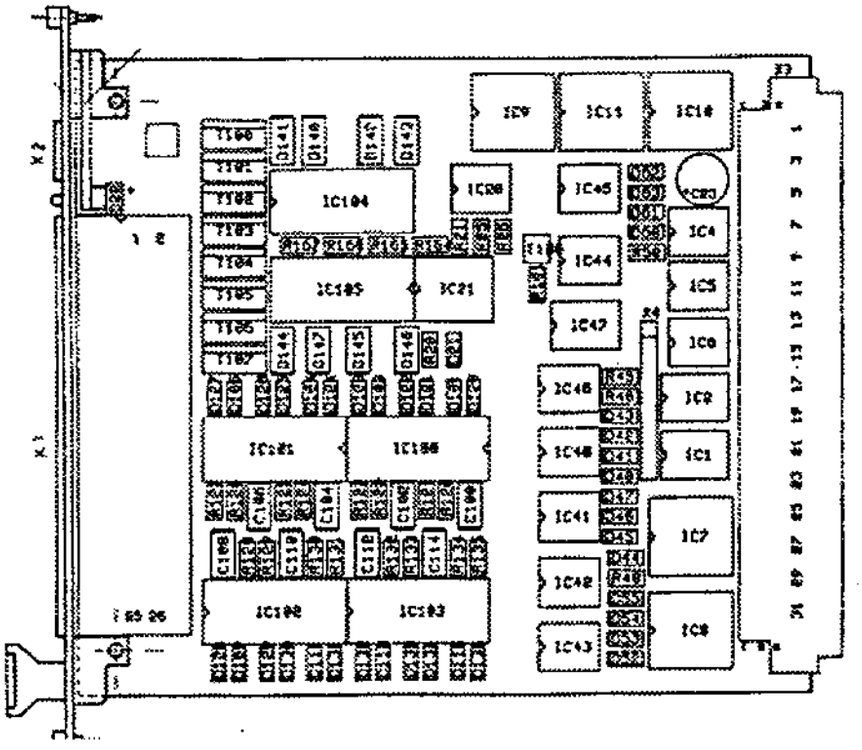
1.4 Specifications

External Interface	
Input	Optoisolated inputs, 24Vdc (±20%), level sensitive
Channels	16
Turn on time Turn off time	5 ms 5 ms
Voltage logic low state Voltage logic high state	<5V >10V
Isolation	According to IEC65A, 2kV between logic components and process.
Output	
Channels	8
Grounding	Common ground, electrically isolated from other CXC's or frame grounds.
Sink voltage/current	24V dc industry standard/500mA per channel. Integrated clamp diodes for inductive loads.
Safety status	Deactivated outputs during power-up, after RESET and after process power fail
Isolation	According to IEC65A, 2kV between logic components and process.
General	
Power requirements	CXC +5V dc (±5%) External +24V dc (±20%)
Temperature range operating storage Operating humidity Board size Connector Front panel width Front panel connectors	 -0°C to +70°C -55°C to +85°C 5% to 95% 100mm x 115mm DIN 41612 style C (96-pin) 8TE (40.6mm) 2 slots Phoenix MDSTB 2.5/13G1-5.08 (2x13 screw terminals) Phoenix MC 1.5/2-G-3.81 (2 screw terminals)

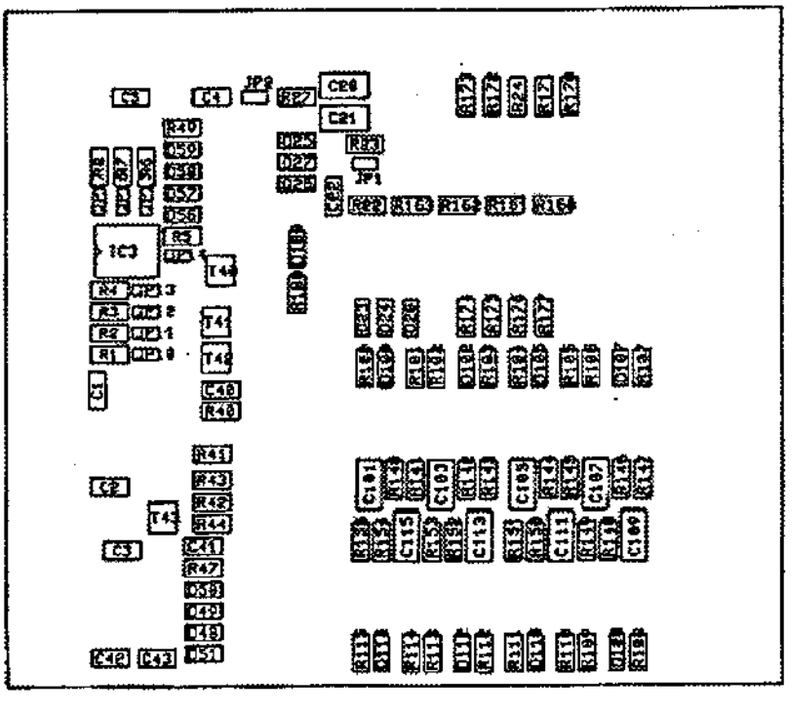
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1.5 Board Overview

Component side



Solder side



Front Panel

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1.6 Characteristics

- **Capable of handling industry standard input and output voltages.**
- **Cost-effective solutions.**
- **Quick and easy implementation.**
- **Can be used with wither the IUC, VIUC, VSBC-4 or VM30.**

1.7 Hardware Definitions

- **Full electric compatibility with the CXC interface.**
- **Optoisolated outputs. and input**

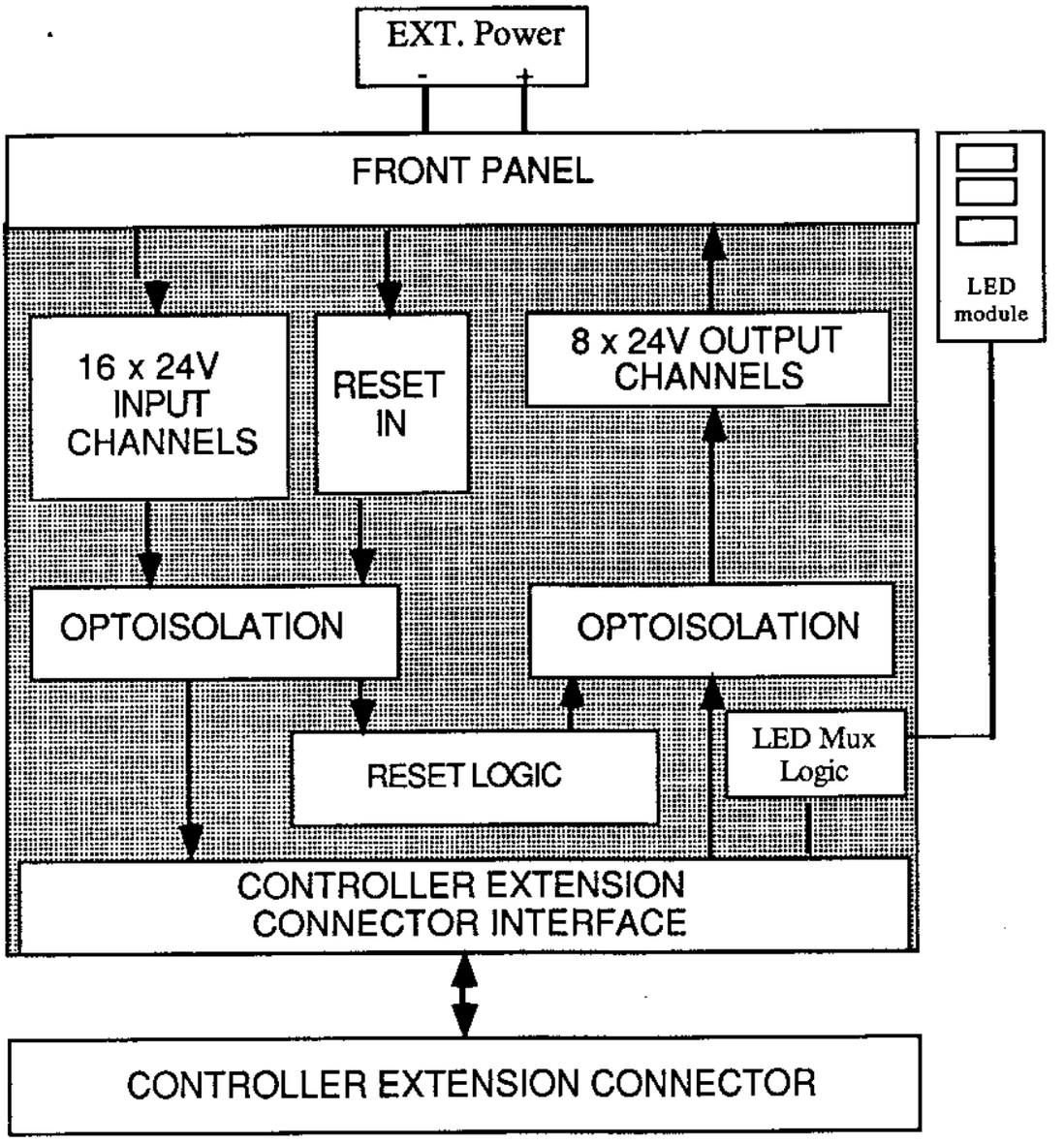
1.8 Related Publications

For more information regarding the CXM/CXC refer to:

IUV/VIUC/vsbc-4/VM30 User Manuals

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1.9 Block Diagram



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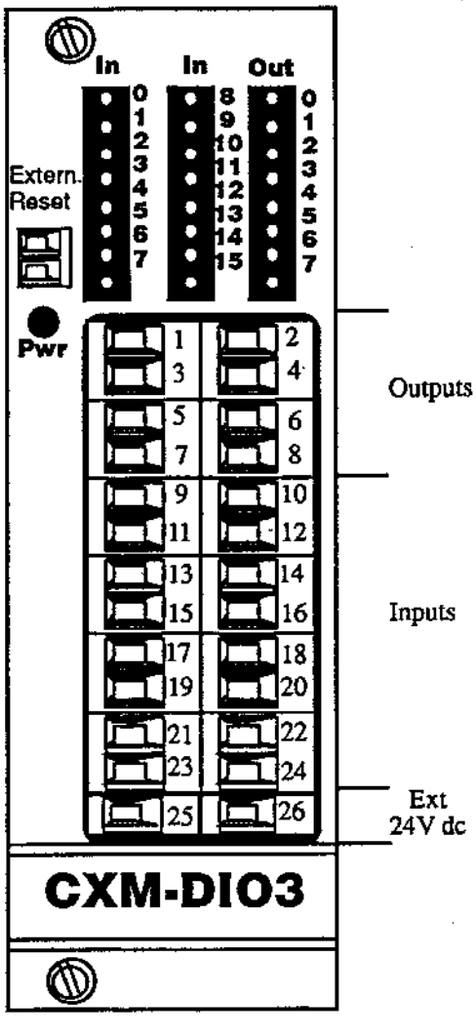
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2. FUNCTIONAL DESCRIPTION

Figure 2 Front Panel



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2.1 Addresses

The CXM-DIO3 has 4 different addresses for reading inputs, setting outputs, reading the reset status and reading the device ID code. Reading the input address by byte is through channel 0 to channel 7, whilst reading it by word is through channel 0 to 15.

Base address + offset $00	Data in
Base address + offset $02	Data out
Base address + offset $04	Reset status
Base address + offset $80	Device ID

2.2 ID Code

The ID code of the CXM-DIO3 is $05.

2.3 Reset Status

Bit No.	Status	Function
Bit 0	0	Process reset inactive
Bit 0	1	Process reset active
Bit 1	0	Process power fail inactive
Bit 1	1	Process power fail active
Bit 2*	0	IGP emergency off inactive
Bit 2*	2	IGP emergency off active

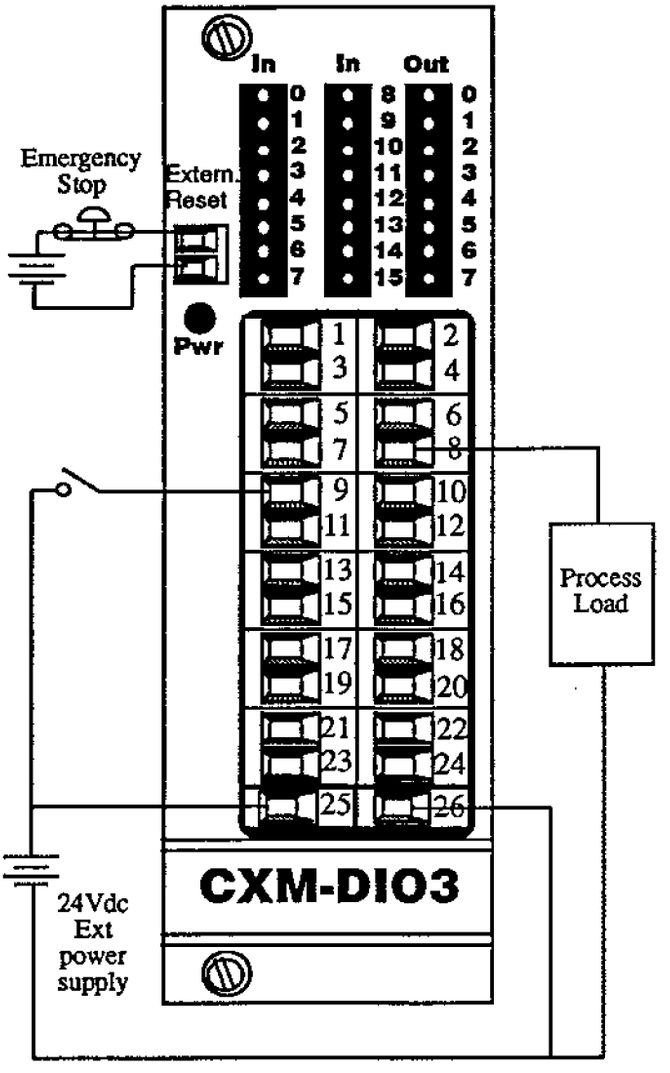
* If jumper J2 is set there is a special use of the CXC $\overline{CS7}$ line. The default setting is open.

2.4 External Reset

If J1 is closed, nor output or input will be enabled until the external Reset is powered by 24Vdc.

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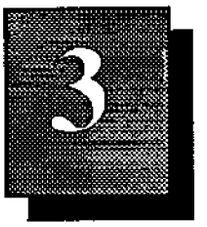
2.5 External Load Connection



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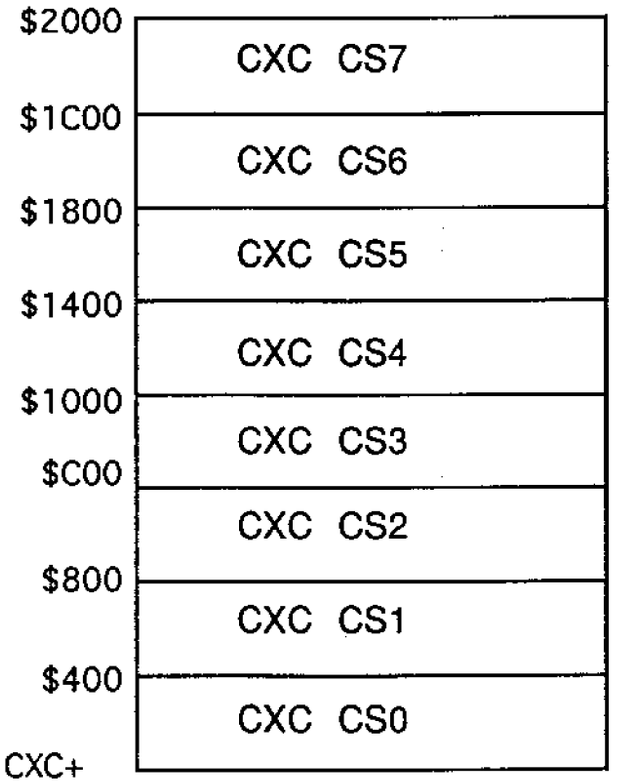
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3. CXC DESCRIPTION

The CXC is the local interface. It contains a 16-bit data bus and 8 decoded chip select lines, each with 256 bytes, and 7 address lines. Overall there are 8 control signals.

Figure 3 CXC address range



The base address of the CXC is programmable via CS3 of the MC68302 (internal chip select logic).

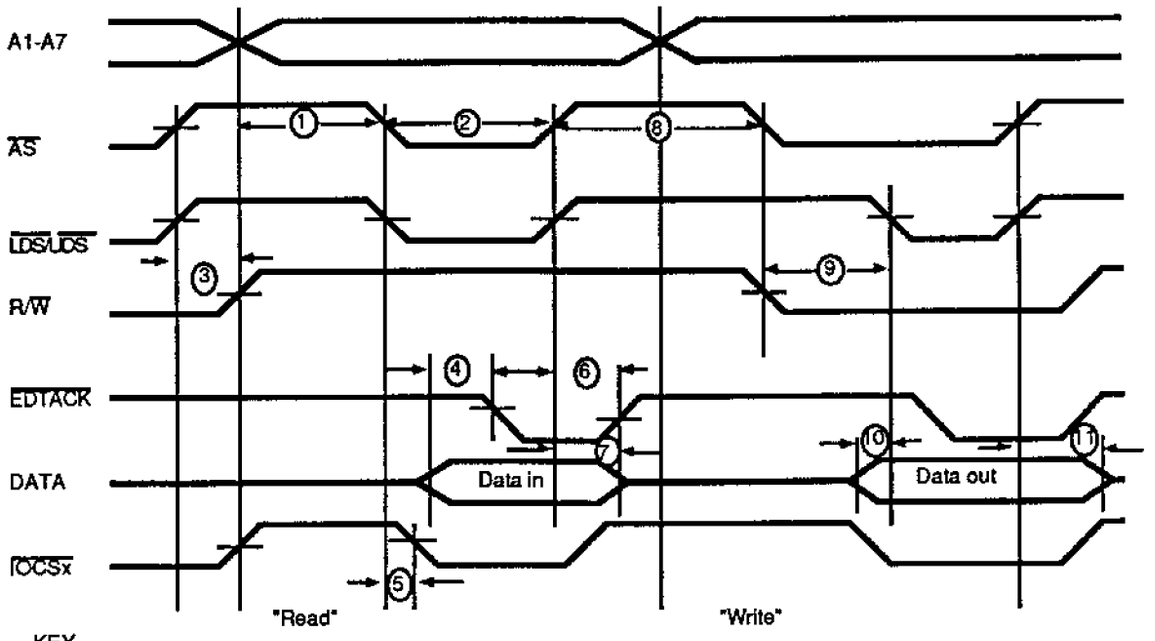
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3.1 Pin-outs

Pin Number	Row A SIGNALS	Row B SIGNALS	Row C SIGNALS
1	PB11 (INTERRUPT)	Rclk1 (SCC1)	PA15/DONE (IDMA)
2	PB10 (INTERRUPT)	Tclk1 (SCC1)	PA14/DACK (IDMA)
3	PB9 (INTERRUPT)	GND	PA13/DREQ (IDMA)
4	PB8 (INTERRUPT)	TxD1 (SCC1)	PA12/BRG3 (SCC3)
5	PB7/WDOG	RTS1* (SCC1)	PA11/Tclk3 (SCC3)
6	PB6/TOUT2	GND	PA10/Rclk3 (SCC3)
7	VCC	RTS3* (SCC3)	VCC
8	PB5/TIN2	CD3* (SCC3)	PA9/TxD3 (SCC3)
9	PB4/TOUT1	GND	PA8/RxD3 (SCC3)
10	PB3/TIN1	RxD1 (SCC1)	PA7/BRG2/SDS2 (SCC2)
11	PB2/IACK1	BRG1 (SCC1)	PA6/CD2 (SCC2)
12	PB1/IACK6	GND	PA5/RTS2 (SCC2)
13	PB0/IACK7	CTS1* (SCC1)	PA4/CTS2 (SCC2)
14	VCC	CD1* (SCC1)	VCC
15	CS-CXC* (CS3 of 68302)	GND	PA3/Tclk2 (SCC2)
16	IAS*	CTS3*	PA2/Rclk2 (SCC2)
17	R/W	SYSR*	PA1/TxD2 (SCC2)
18	UDS*	GND	PA0/RxD2 (SCC2)
19	LDS*	EDTACK*	VCC
20	VCC	16MHz CLOCK	CXC CS2*
21	A1	GND	CXC CS3*
22	A2	CXC CS0*	CXCCS4*
23	A3	CXC CS1*	CXC CS5*
24	A4	GND	CXC CS6*
25	A5	A6	CXC CS7*
26	VCC	A7	VCC
27	D0	GND	D10
28	D1	D6	D11
29	D2	D7	D12
30	D3	GND	D13
31	D4	D8	D14
32	D5	D9	D15

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3.2 Timing



KEY

	min	max
1. Address valid to AS, DS	15ns	-
2. AS asserted	120ns	-
3. AS negated to R/W invalid	15ns	-
4. Data-in valid to EDTACK	0ns	-
5. IOCSx asserted to AS valid	-	25ns
6. EDTACK negated to AS negated	0ns	111ns
7. Data-in hold time	0ns	50ns
8. AS negated	60ns	-
9. AS, R/W asserted to DS asserted	30ns	-
10. Data-out valid to DS asserted	15ns	-
11. AS,DS negated to data-out invalid	15ns	-

A1-A7: address lines
AS: address strobe
LDS/UDS: lower/upper data strobe
R/W: read not write
EDTACK: external data transfer acknowledge
IOCSx: IOCS0 to IOCS7

Recommended: Assert EDTACK with CSx and UDS/LDS and "data valid" during read cycles
Latch data with CSx and UDS/LDS during write cycles
Negate EDTACK with UDS/LDS invalid

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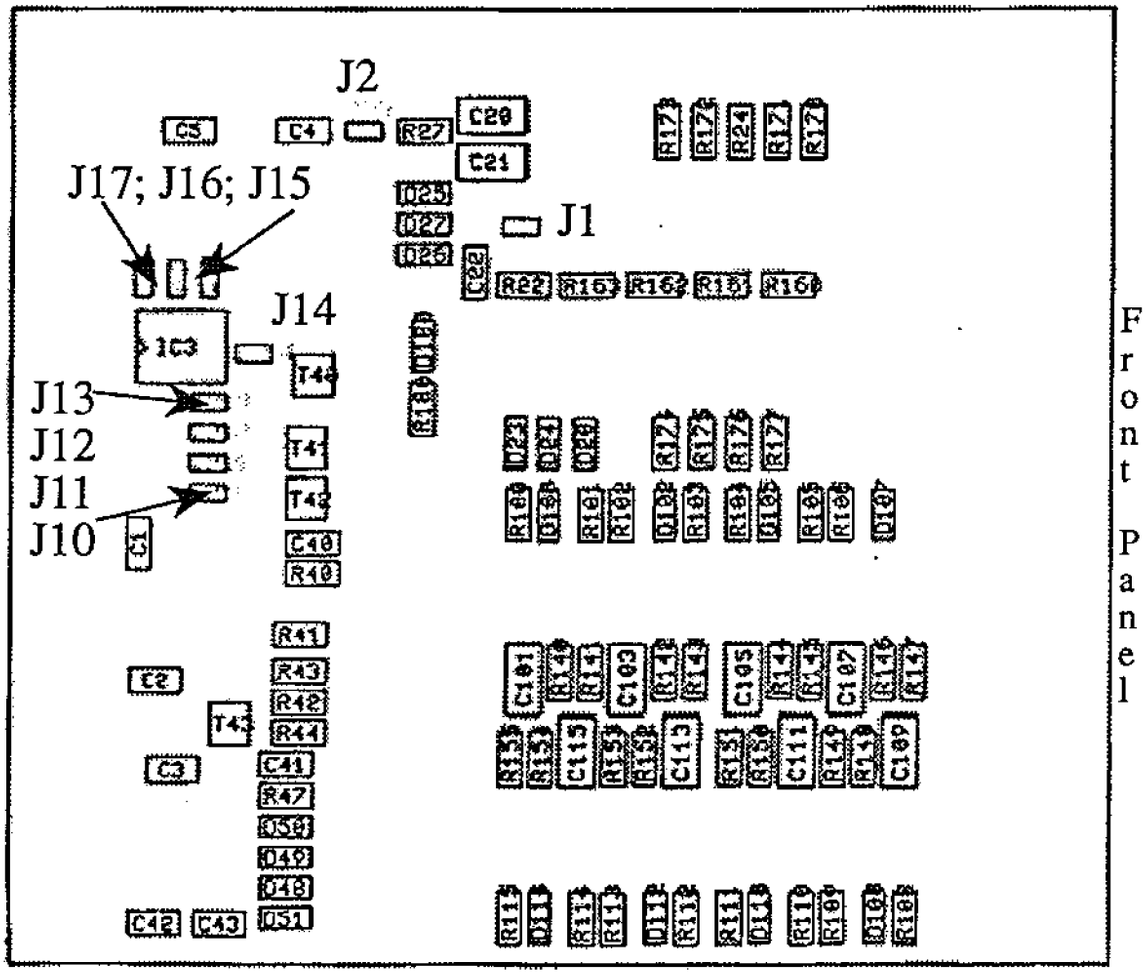
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4. CONFIGURING

Figure 4.0.0.1 Jumper Overview

The CXM-DIO3 has 10 solder pad jumpers located on the solder side of the board. An overview of the jumper settings is given overleaf.



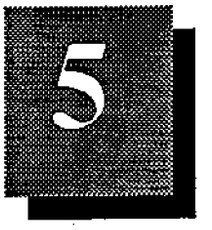
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Table 4.0.0.2 Jumper Overview

Jumper	Setting	Function
J1	open closed (d)	process reset disabled process reset enabled
J2	open (d) closed	IGP emergency off enabled IGP emergency off disabled
J10	open closed (d)	chip select 0 inactive chip select 0 active (base address + 0x0000)
J11	open closed (d)	chip select 1 inactive chip select 1 active (base address + 0x0400)
J12	open closed (d)	chip select 2 inactive chip select 2 active (base address + 0x0800)
J13	open closed (d)	chip select 3 inactive chip select 3 active (base address + 0x0C00)
J14	open closed (d)	chip select 4 inactive chip select 4 active (base address + 0x1000)
J15	open closed (d)	chip select 5 inactive chip select 5 active (base address + 0x1400)
J16	open closed (d)	chip select 6 inactive chip select 6 active (base address + 0x01800)
J17	open (d) closed	chip select 7 inactive chip select 7 active (base address + 0x1C00)

(d) = default setting

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5. SOFTWARE EXAMPLES

5.1 Example Program

```
#include <stdio.h>
#include <ermo.h>

/
/       Definitions
/

#define FOREVER for (;;)

short input (Address);

char in;
short
                *DIO_3_Input,
                *DIO_3_Output,
                *DIO_3_Status
                *DIO_3_ID;

/
/       Initialisations
/

init()
{


DIO_3_Input     =       0xF70000;       /*DIO-3 input address*/
DIO_3_Output    =       0xF70002;       /*DIO-3 ouput address*/
DIO_3_Status    =       0xF70004;       /*DIO-3 status address*/
DIO_3_ID        =       0xF70008;       /*DIO-3 ID code address*/
*DIO_3_Output   =       0x0000;         /*clear dio_3 output*/
}
```


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```
/
/       main program for DIO-3
/
main()
{
        init();
        FOREVER
        {
        /*test the ID code*/
                if ((input(DIO_3_ID) & 0x0005) == 0x0005)
                {
                        /*ID code is correct*/
                }
                else
                {
                        /*ID code is not correct*/
                }
        /*read input 0*/
                if (input ((DIO_3_Input)&0x0001) == 0x0001)
                {
                        /*channel 0 is set*/
                }
                else
                {
                        /*channel 0 is not set*/
                }
        /*set output 0*/
                *DIO_3_Output = 0x0001;         /*set output 0*/
        /*read status register (power fail)*/
                if ((input (DIO_3_Status) & 0x0002) == 0x0002)
                {
                        /*status is "power fail"*/
                }
                else
                {
                        /*status is not "power fail"*/
                }
        /*read status register (process reset)*/
                if ((input(DIO_3_Status) & 0x0001) == 0x0001)
                {
                        /*status is "process reset"*/
                }
                else
                {
                        /*status is not "process reset"*/
                }
}
short input (Address)
{
        short *pAddress;
        pAddress = Address;
        return(*pAddress);
}
```

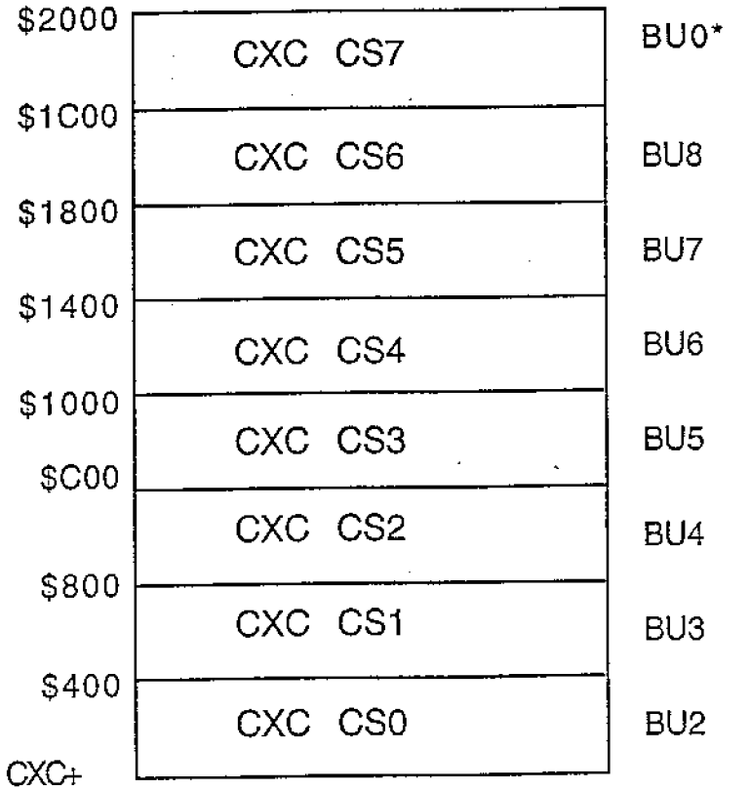

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CONTROLLER EXTENSION CONNECTOR

The Controller eXtension Connector (CXC) is the local interface. It contains a 16-bit data bus, 7 address lines, and 8 decoded chip select lines. Each chip select line has 256 bytes. Overall there are 8 control signals.

Figure 1.0.0.4 CXC address range

The base address of the CXC can be programmed via CS3 of the MC68302 (internal chip select logic). CS3 has a default of F70000 on the [V]IUC and VSBC-4, and C1F70000 on the VM30 and VIUC30.



BU1 is the controller slot.
*On 5S, 8S and 8ES, for STAT1 only.

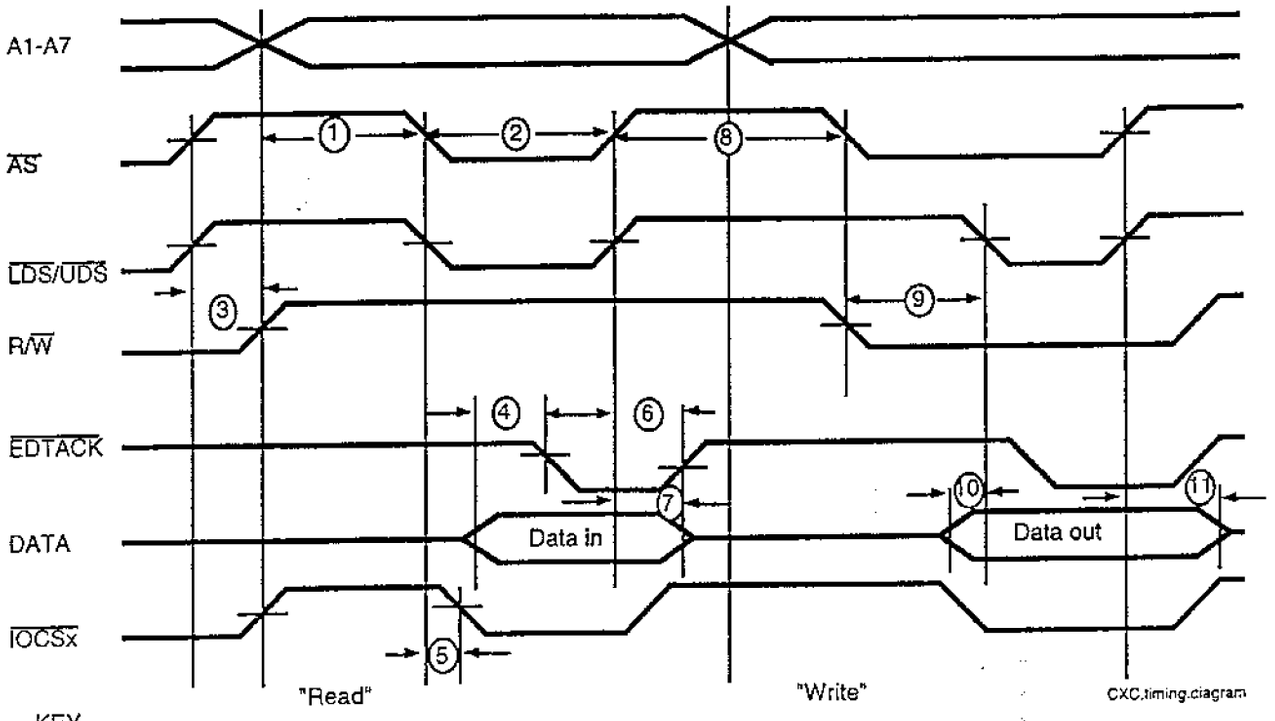
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2 Pin-outs

Pin Number	Row A Signals	Row B Signals	Row C Signals
1	PB11 (INTERRUPT)	Rclk1 (SCC1)	PA15/DONE (IDMA)
2	PB10 (INTERRUPT)	Tclk1 (SCC1)	PA14/DACK (IDMA)
3	PB9 (INTERRUPT)	GND	PA13/DREQ (IDMA)
4	PB8 (INTERRUPT)	TxD1 (SCC1)	PA12/BRG3 (SCC3)
5	PB7/WDOG	RTS1* (SCC1)	PA11/Tclk3 (SCC3)
6	PB6/TOUT2	GND	PA10/Rclk3 (SCC3)
7	VCC	RTS3* (SCC3)	VCC
8	PB5/TIN2	CD3* (SCC3)	PA9/TxD3 (SCC3)
9	PB4/TOUT1	GND	PA8/RxD3 (SCC3)
10	PB3/TIN1	RxD1 (SCC1)	PA7/BRG2/SDS2 (SCC2)
11	PB2	BRG1 (SCC1)	PA6/CD2 (SCC2)
12	PB1	GND	PA5/RTS2 (SCC2)
13	PB0	CTS1* (SCC1)	PA4/CTS2 (SCC2)
14	VCC	CD1* (SCC1)	VCC
15	CS-CXC* (CS3 of 68302)	GND	PA3/Tclk2 (SCC2)
16	IAS*	CTS3*	PA2/Rclk2 (SCC2)
17	R/W	SYSR*	PA1/TxD2 (SCC2)
18	UDS*	GND	PA0/RxD2 (SCC2)
19	LDS*	EDTACK*	VCC
20	VCC	16MHz CLOCK	CXC CS2*
21	A1	GND	CXC CS3*
22	A2	CXC CS0*	CXC CS4*
23	A3	CXC CS1*	CXC CS5*
24	A4	GND	CXC CS6*
25	A5	A6	CXC CS7*
26	VCC	A7	VCC
27	D0	GND	D10
28	D1	D6	D11
29	D2	D7	D12
30	D3	GND	D13
31	D4	D8	D14
32	D5	D9	D15

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3. Timing



KEY

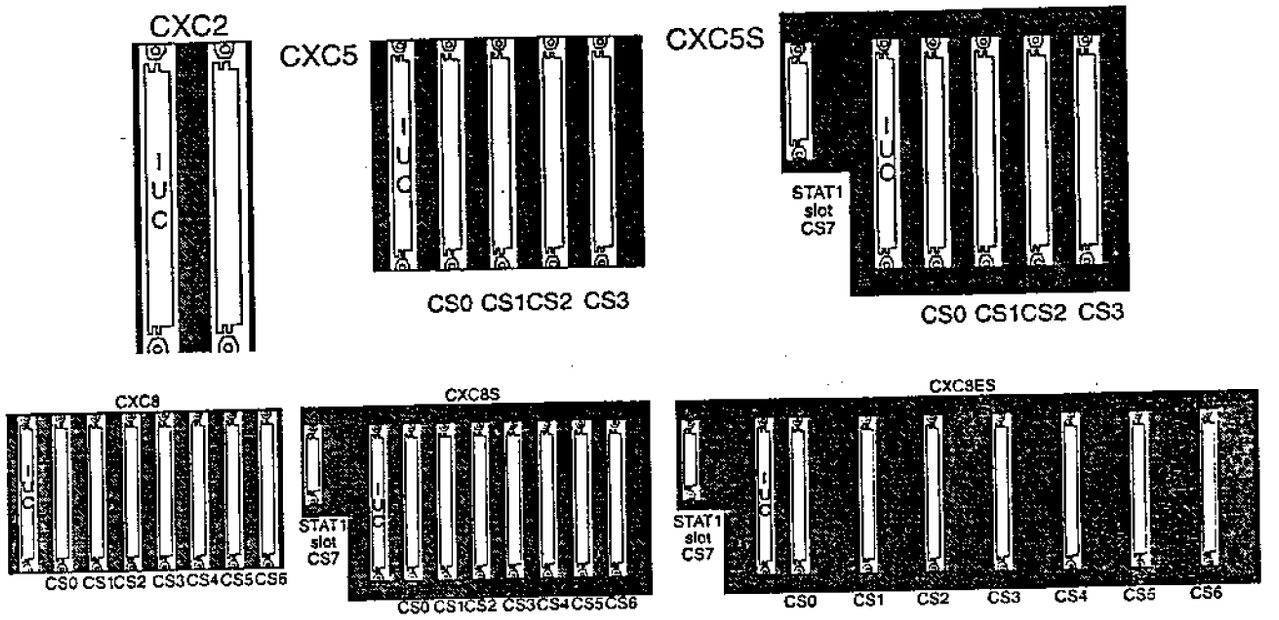
		min	max
1.	Address valid to AS, DS	15ns	-
2.	AS asserted	120ns	-
3.	AS negated to R/W invalid	15ns	-
4.	Data-in valid to EDTACK	0ns	-
5.	IOCSx asserted to AS valid	-	25ns
6.	EDTACK negated to AS negated	0ns	111ns
7.	Data-in hold time	0ns	50ns
8.	AS negated	60ns	-
9.	AS, R/W asserted to DS asserted	30ns	-
10.	Data-out valid to DS asserted	15ns	-
11.	AS,DS negated to data-out invalid	15ns	-

A1-A7: address lines
AS: address strobe
LDS/UDS: lower/upper data strobe
R/W: read not write
EDTACK: external data transfer acknowledge
IOCSx: IOCS0 to IOCS7

Recommended: Assert EDTACK with CSx and UDS/LDS and "data valid" during read
Latch data with CSx and UDS/LDS during write
Negate EDTACK with UDS/LDS invalid

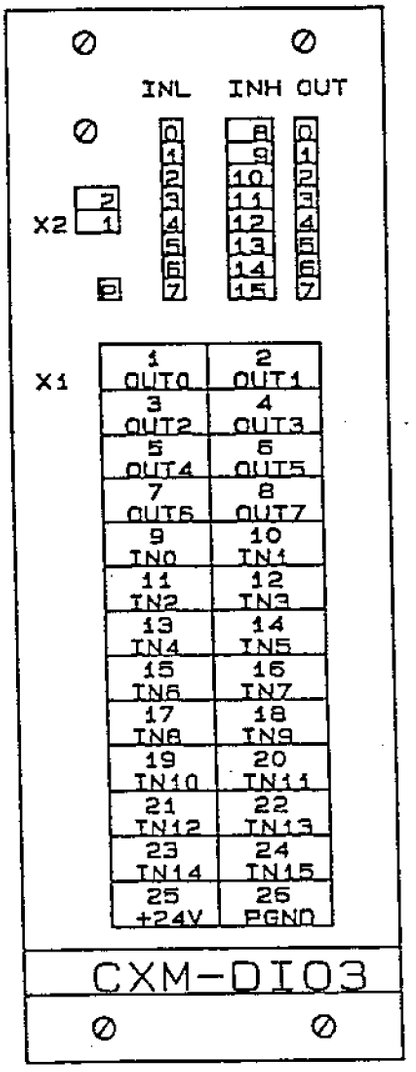
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4. BACKPLANES

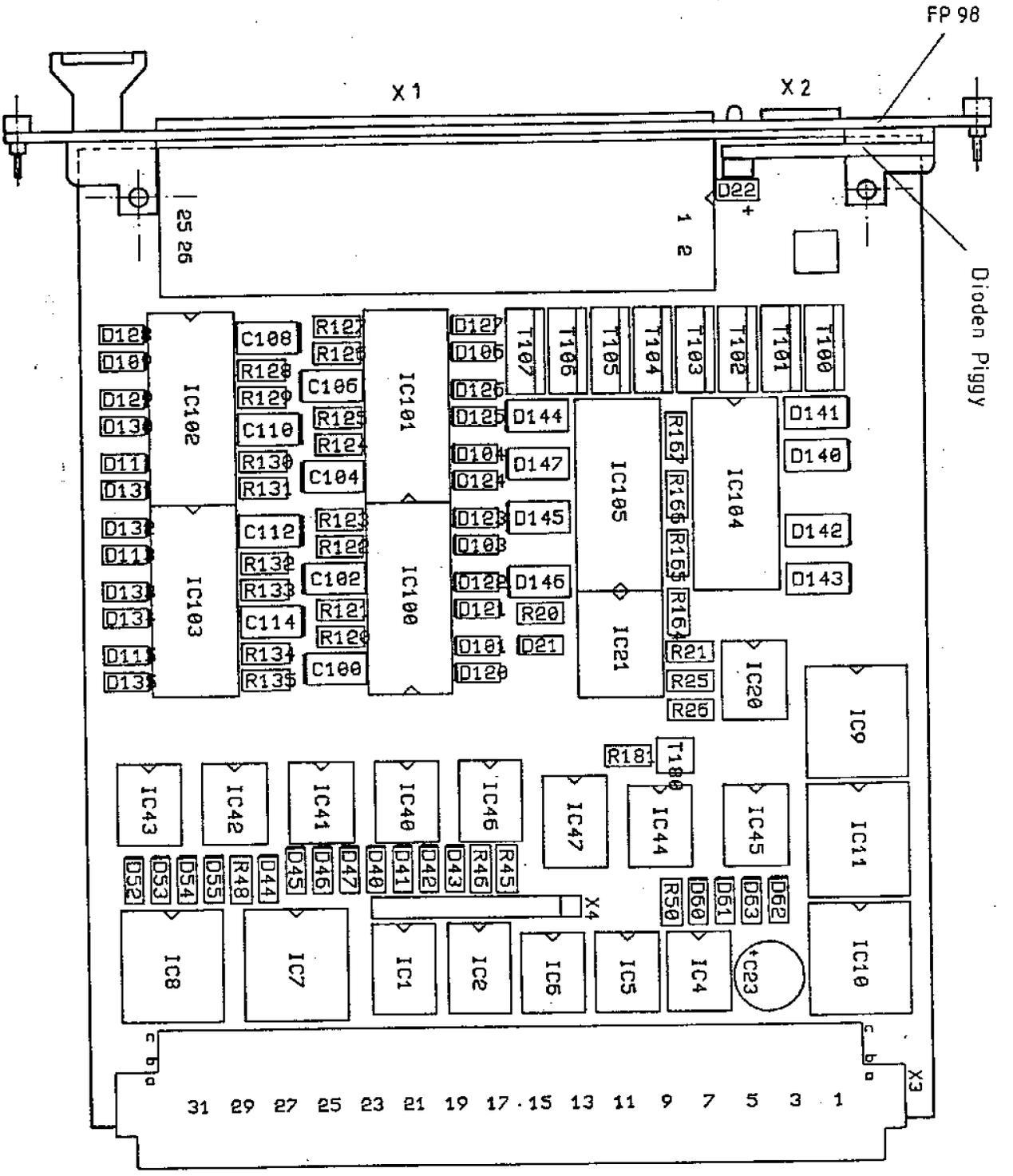


When using an 8TE board on the CXC5/5S/8/8S note that a slot will be lost between each borad. The CXC8Es has been designed specifically with this problem in mind, and no slots will be lost.

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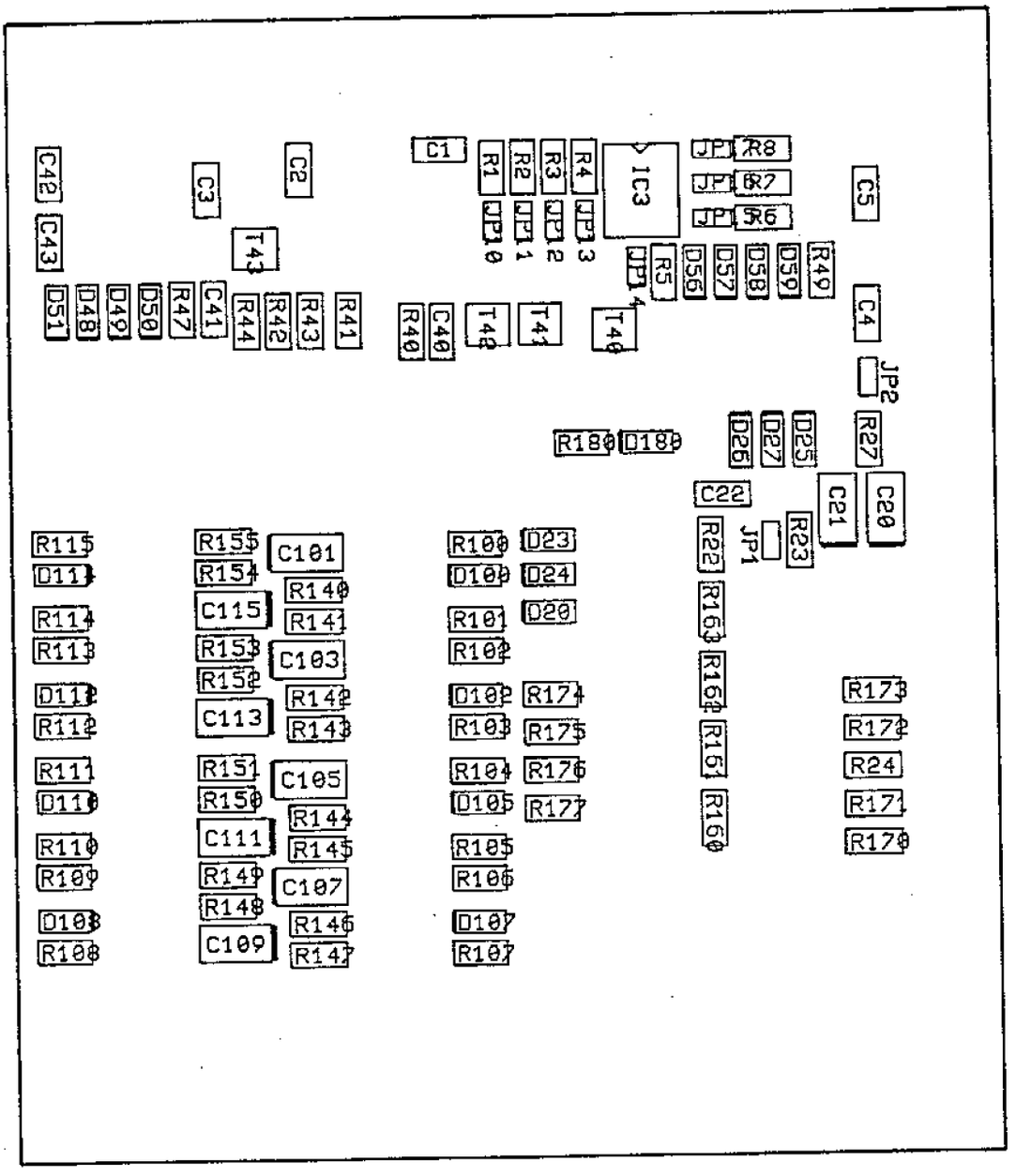
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B – Seite / B – side

* entspr. Bestell-Nr. / according to order-no 5262-005

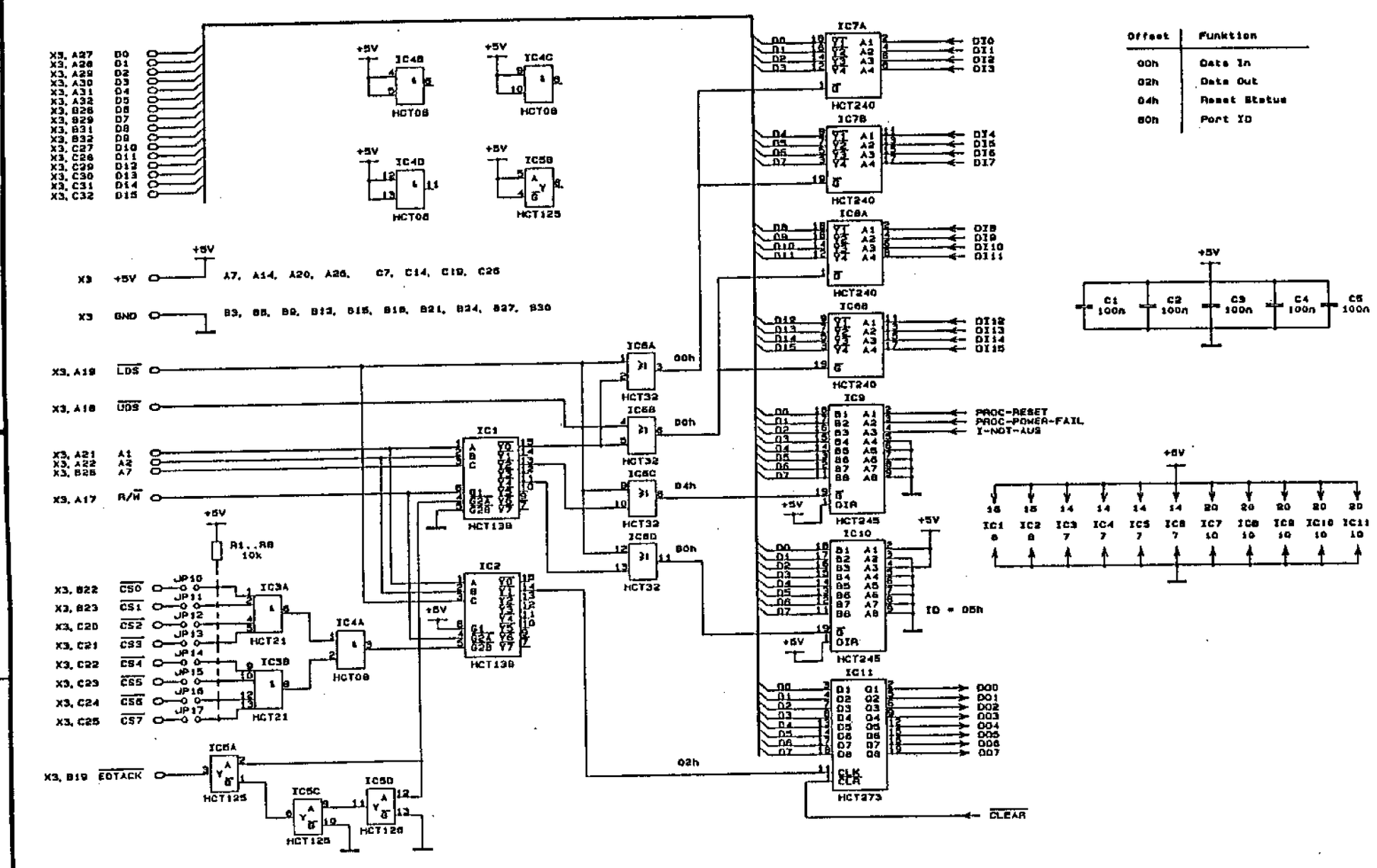
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L – Seite / L - side

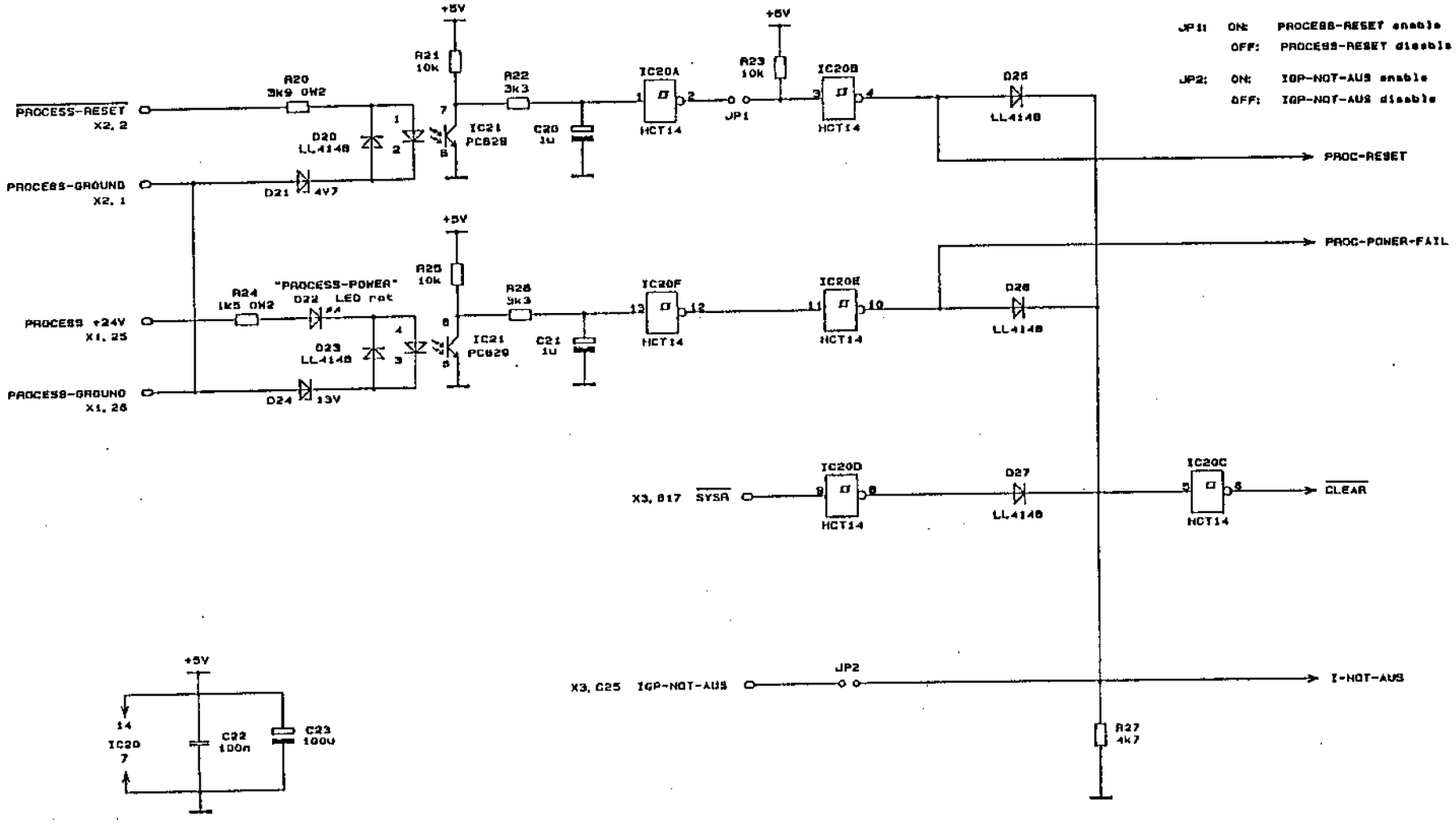
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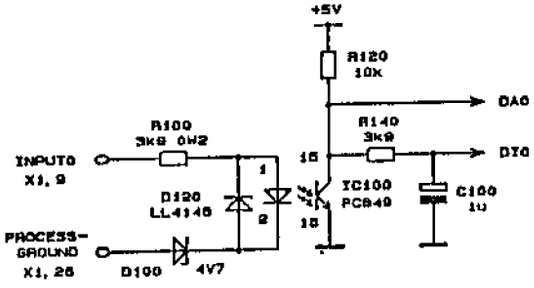


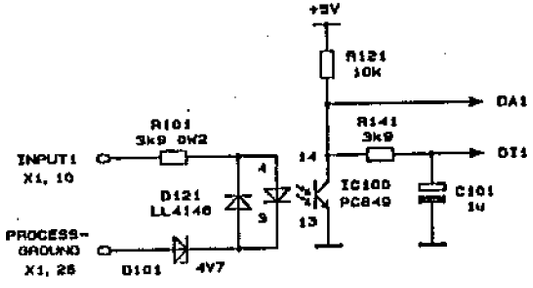
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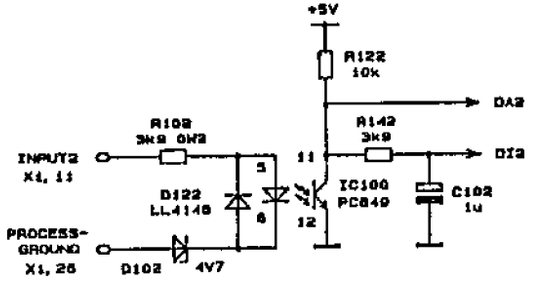
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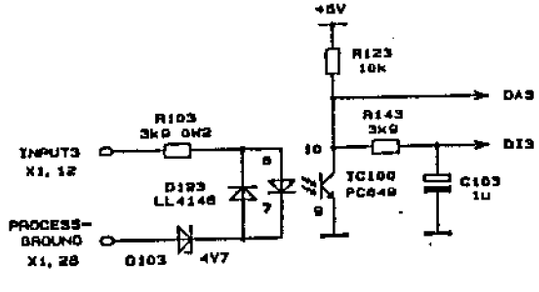
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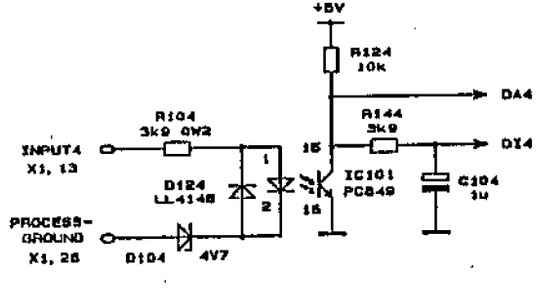
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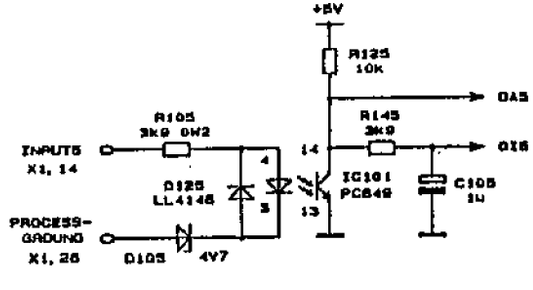


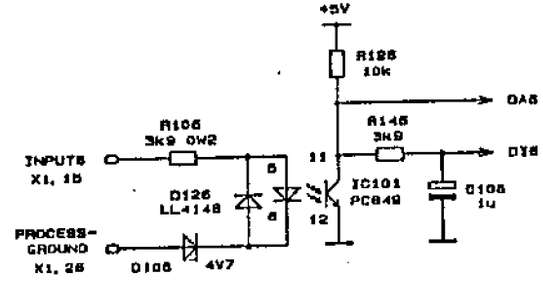


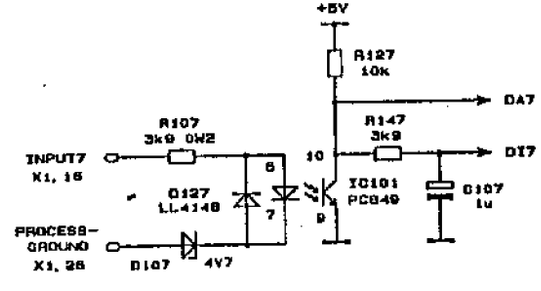


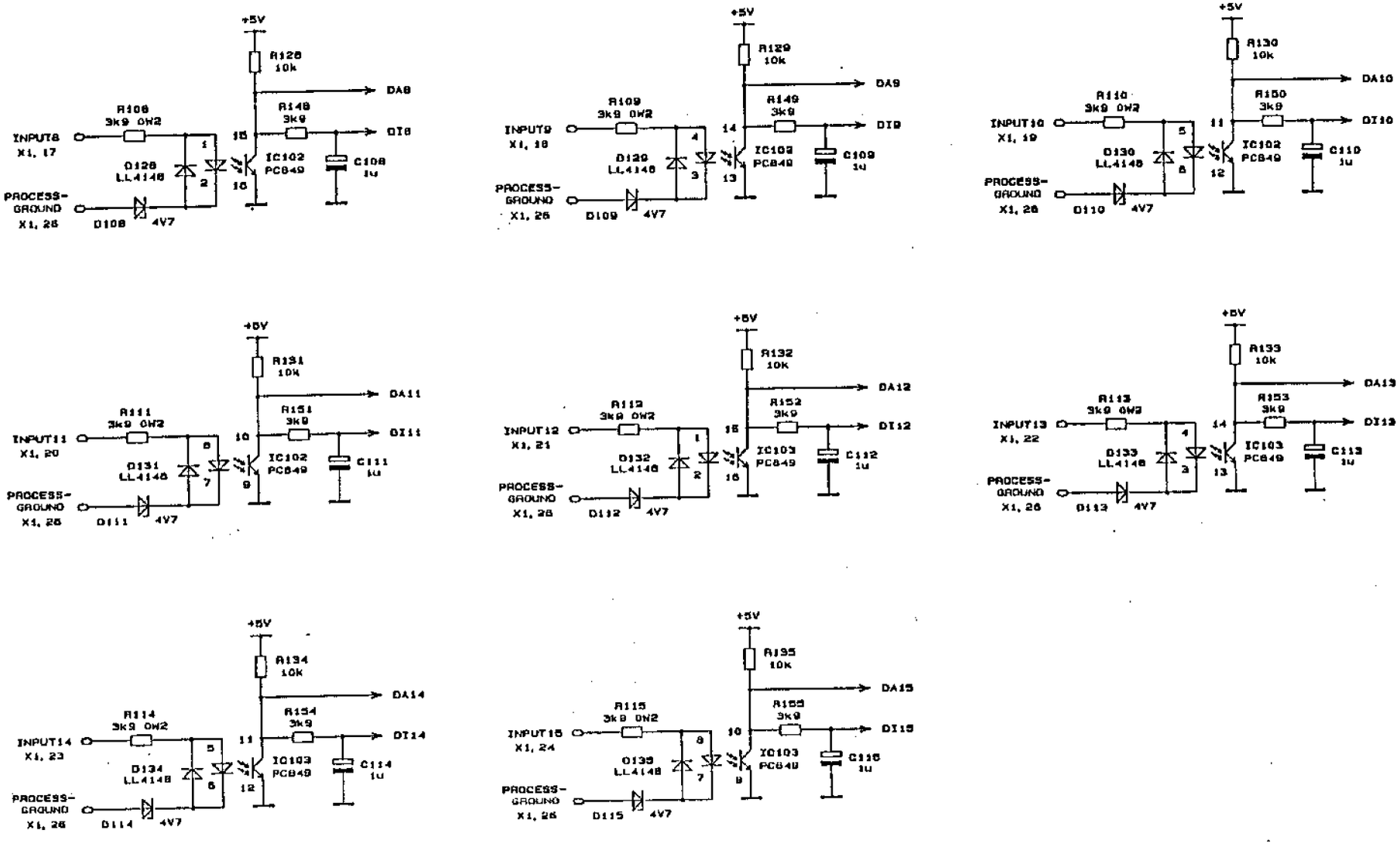






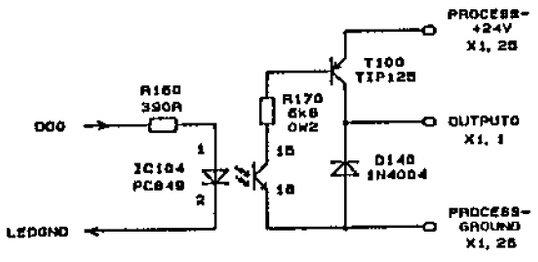


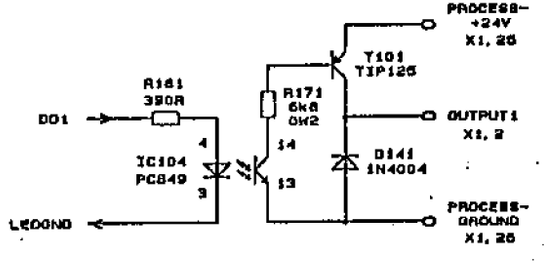


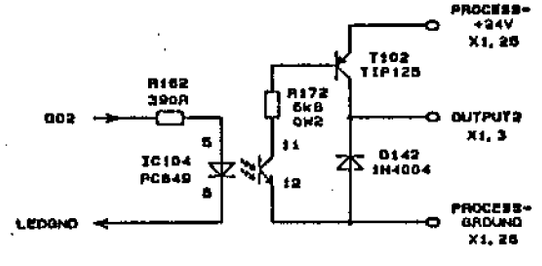


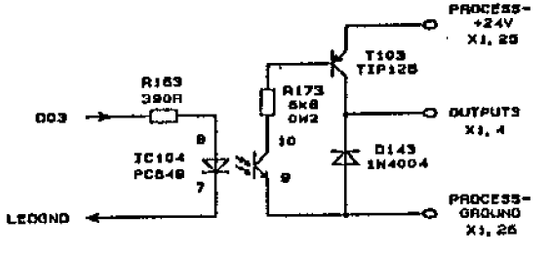
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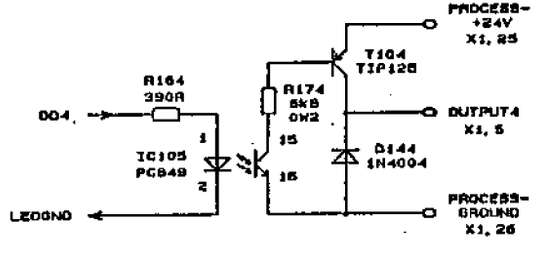
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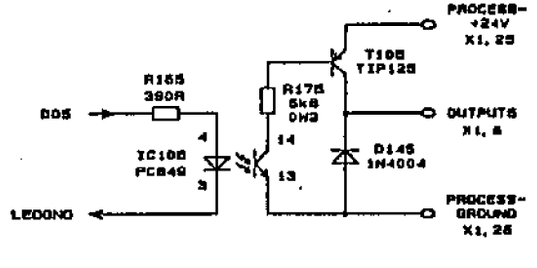


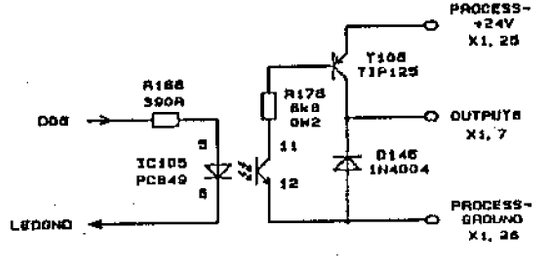


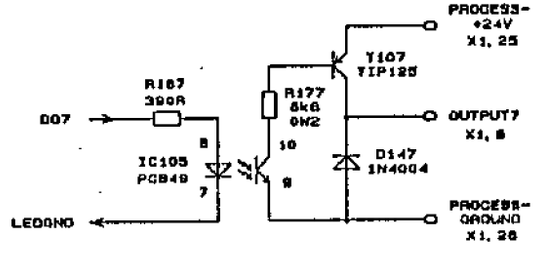


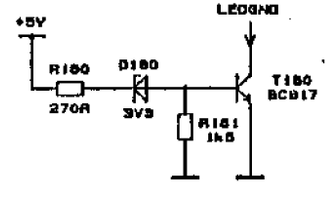






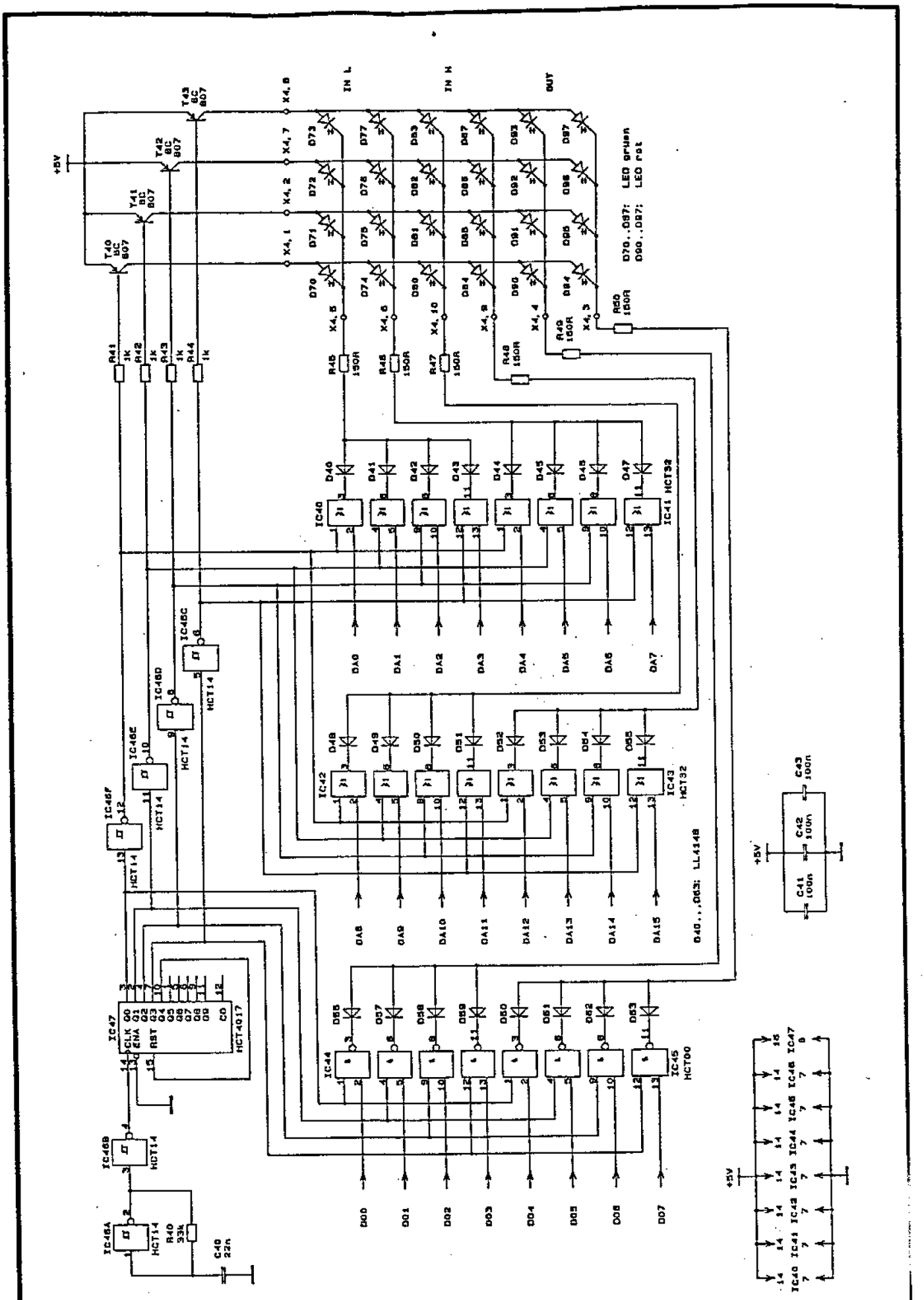






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