Kontron User's Guide



EPIC/CE

Document Revision 1.14

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Table of Contents

1 User Information 9

1.1 About This Document 9
1.2 Copyright Notice 9
1.3 Trademarks 9
1.4 Standards 9
1.5 Warranty 9
1.6 Technical Support 10

2 Introduction 11

2.1 EPIC/CE 11
2.2 The EPIC Family 11

3 Getting started 12

4 Specifications 13

4.1 Functional Specifications 13
4.2 Mechanical Specifications 15
4.2.1 PC/104 Bus Connector (ISA part) 15
4.2.2 PC/104-Plus Bus Connector (PCI part) 15
4.2.3 Dimensions 15
4.2.4 Height on Top 15
4.2.5 Height on Bottom 15
4.2.6 Weight 15
4.3 Electrical Specifications 16
4.3.1 Supply Voltages 16
4.3.2 Supply Voltage Ripple 16
4.3.3 Supply Current (typical) 16
4.3.4 Supply Current (maximum) 17
4.3.5 Real-time Clock (RTC) Battery 17
4.4 MTBF 18
4.5 Environmental Specifications 19
4.5.1 Temperature 19
4.5.2 Humidity 19

5 CPU, Chipset and Super I/O 20

5.1 CPU 20
5.2 Chipset 20
5.2.1 GMCH (815E Chipset) 20
5.2.2 ICH4 (82801DB) 22
5.3 Super I/O 23

5.4 CPU, Chipset and Super-I/O Configuration 23

6 System Memory 24

7 ISA and PCI Bus Expansion 25

7.1 PC/104 Bus (ISA part) 25
7.1.1 PC/104 Connectors 25
7.1.2 PC/104 Configuration 25
7.2 PC/104-Plus (PCI part) 26
7.2.1 PC/104-Plus Connector 26
7.2.2 PC/104-Plus Configuration 26

8 Keyboard and Mouse Interfaces 27

8.1 PS/2-Keyboard Connector 27
8.2 PS/2-Keyboard Configuration 27
8.3 PS/2-Mouse Connector 27
8.4 PS/2-Mouse Configuration 28

9 USB Interfaces 29

9.1 Front Connectors (USB 0 to USB 3) 29
9.2 Internal Connectors (USB 4 and USB 5) 29
9.2.1 Limitations of USB Ports 4 and 5 30
9.3 Configuration 30

10 Ethernet Interfaces 31

10.1 First Ethernet Controller 31
10.2 Second Ethernet Controller 32
10.3 Connectors 32
10.4 Configuration 33
10.5 Ethernet Technical Support 33

11 Graphics Interfaces 34

11.1 Video Controller 34
11.2 CRT Connector 34
11.3 DVO Connector (optional) 35
11.4 Flat Panel LVDS Interface (JILI) Connector 35
11.5 Display Power Considerations 36
11.6 Connecting a LCD Panel 36
11.7 Configuration 37
11.8 Graphics Technical Support 37
11.9 Available Video Modes 37
11.9.1 Standard IBM-Compatible VGA Modes 37

11.9.2 Extended VESA VGA Modes 38

12 Serial-Communication Interfaces 39

12.1 Serial Ports COM A to COM D 39
12.2 RS-232 Connectors 39
12.3 RS-485 Connector 40
12.4 Configuration 40

13 Parallel-Port Interface 41

13.1 Connector 41
13.2 Configuration 41

14 IDE Interfaces 42

14.1 Connector 42
14.2 CompactFlash Socket 43
14.3 Configuration 43

15 Floppy Interface 44

15.1 Connector 44
15.1.1 Connector Diagram 45
15.2 Configuration 45

16 Sound Interface 46

16.1 Connectors 46
16.1.1 Jack Connector 46
16.1.2 Line-In/Rear Speakers Connector 47
16.2 Configuration 47
16.3 Technical Support for Sound 48

17 General Purpose Inputs/outputs 49

17.1 Connector 49
17.2 Programming 50
17.2.1 16-Bit Operating Systems 50
17.2.2 32-Bit Operating Systems 52
17.3 Configuration 52

18 FAN Interface 53

18.1 Connector 53
18.2 Configuration 53

19 Power Interface 54

19.1 Power Interface Connectors 54

19.1.1 ATX Connector Version 54
19.1.2 +5V-only Power Supply on ATX connector 55
19.1.3 AT Connector Version 55
19.1.4 Configuration 55
19.2 ATX/Reset/2LED Interface 56
19.2.1 Configuration 56

20 Watchdog Timer 57

20.1 Configuration 57
20.2 Programming 57
20.2.1 Initializing the WDT 57
20.2.2 Triggering the WDT 57

21 Hardware Monitor 58

21.1 Configuration 58

22 Important Technology Information 59

22.1 Thermal Control 59
22.1.1 Thermal Management 59
22.1.2 ACPI Thermal Management 59
22.1.3 Processor Clock Throttling 60
22.2 I/O APIC vs. 8259 PIC Interrupt mode 60
22.3 Native vs. Compatible IDE mode 61
22.3.1 Compatible IDE Mode 61
22.3.2 Native Mode 61
22.3.3 Native Mode Configuration 61

23 Appendix A: System-Resource Allocation 62

23.1 Interrupt Request (IRQ) Lines 62
23.2 Direct Memory Access (DMA) Channels 63
23.3 Memory Map 64
23.3.1 Using Expanded Memory Managers 64
23.4 I/O Address Map 65
23.5 Peripheral Component Interconnect (PCI) Devices 66
23.6 SM Bus Devices 66

24 Appendix B: BIOS Operation 67

24.1 Determining the BIOS Version 67
24.2 Configuring the System BIOS 67
24.2.1 General Information 68
24.3 Main Menu 69
24.3.1 Master or Slave Submenus 70

24.4 Advanced Menu 71
24.4.1 Advanced Chipset Control Submenu 71
24.4.2 PCI/PNP Configuration Submenu 71
24.4.3 PCI Device, Slot #x Submenu 72
24.4.4 PCI/PNP ISA IRQ Resource Exclusion Submenu 72
24.4.5 Memory Cache Submenu 73
24.4.6 I/O Device Configuration Submenu 74
24.4.7 Keyboard Features Submenu 75
24.4.8 Hardware Monitor Submenu 75
24.4.9 Watchdog Timer Settings Submenu 75
24.4.10 Display Control Submenu 76
24.4.11 Miscellaneous Submenu 77
24.5 Security Menu 78
24.6 Power Menu 79
24.6.1 ACPI Resume Events 79
24.6.2 ACPI Control Submenu 81
24.6.3 Thermal Management Submenu 81
24.7 Boot Menu and Utilities 82
24.7.1 MultiBoot XP 82
24.7.2 Boot First Function 83
24.8 Exit Menu 84
24.9 Kontron BIOS Extensions 84
24.9.1 JIDA BIOS extension 85
24.9.2 Remote Control Client Extension 85
24.9.3 LAN PXE ROM 85
24.10 Updating or Restoring BIOS Using PhoenixPhlash 85
24.10.1 Flashing a BIOS 86
24.10.2 Preventing Problems When Updating or Restoring BIOS 87

25 Appendix C: Block Diagram 88

26 Appendix D: Mechanical Dimensions 89

26.1 Board Dimensions and Mounting Holes 89
26.1.1 Top View 89
26.1.2 Front View 89
26.2 Connector Locations (Pin 1) 90
26.3 Slot Dimensions 91
26.3.1 Front and Top View 91

27 Appendix E: Connector Layout 92

27.1 Top Side 92
27.2 Bottom Side 93
27.3 Connector Functions and Interface Cables 94

27.4 Pin-out Table 96

28 Appendix F: PC Architecture Information 99

28.1 Buses 99
28.1.1 ISA, Standard PS/2 - Connectors 99
28.1.2 PC/104, PCI 99
28.2 General PC Architecture 99
28.3 Ports 100
28.3.1 RS-232 Serial 100
28.3.2 ATA 100
28.3.3 USB 100
28.4 Programming 100

29 Appendix G: Document Revision History 101

1 User Information

1.1 About This Document

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Before contacting Kontron Embedded Modules GmbH technical support, please consult our Web site at http://www.kontron-emea.com/emd for the latest product documentation, utilities, and drivers. If the information does not help solve the problem, contact us by telephone or email.

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2 Introduction

2.1 EPIC/CE

The EPIC/CE hosts either an ULV Intel® Celeron® processor or an LV Intel® Celeron® processor in combination with an Intel® 815E chipset that includes an integrated graphics memory-controller hub. A SDRAM-SODIMM socket can hold either PC100 or PC133 SODIMM memory modules up to 500MB. Six USB 2.0 ports and two 10/100 MBit Ethernet interfaces extend the standard connectivity of four serial ports, one parallel port, and a PS/2 mouse/keyboard interface.

The EPIC/CE is designed in the EPIC (**E**mbedded **P**latform for **I**ndustrial **C**omputing) form factor, which is an international standard of the PC/104 Consortium and can be extended with standard PC/104 and PC/104-Plus extension modules. This provides a flexible, space-saving and cost-optimized industrial computer solution.

2.2 The EPIC Family

Each EPIC is a member of the EPIC family of Kontron Embedded Modules GmbH.

Each EPIC module has the same front connectivity for Reset/ATX feature, 4xUSB ports, 2 LAN interfaces, PS/2 Keyboard, PS/2 Mouse connector, Compact-Flash socket, VGA and one serial port. These family features allow the use of the same chassis over the whole product line and maximize design reuse.

EPIC modules allow the use of standard notebook SODIMM memory modules and full ATX power supplies. An optional 5V-only version is available, too. These homogeneous features facilitate easy upgrades within the EPIC product family.

Display connections are simplified when using the onboard standard JILI Interface (JUMPtec® Intelligent LVDS Interface). JILI automatically recognizes which display is connected and independently sets all video parameters. All EPIC modules are plug-and-work enabled to further reduce time-to-market.

As part of the standard features package, all EPIC modules come with a JUMPtec Intelligent Device Architecture (JIDA) interface, which is integrated into the BIOS. This interface enables hardware-independent access to EPIC features that cannot be accessed via standard APIs. Functions such as watchdog timer, brightness and contrast of LCD backlight, and user bytes in the EEPROM can be configured with ease by taking advantage of this standard EPIC module feature.

The EPIC line products support the PC/104-Plus (PCI) and the PC/104 (ISA) standard via Kontron's own, special PCI-to-ISA bridge. Because of the availability of both extension buses, all past and future PC/104 expansion assemblies with state-of-the-art processor performance can be accommodated.

3 Getting started

Getting started with the EPIC/CE is very easy. Take the following steps:

- Turn off the power supply.
- Connect the power supply to the EPIC's power supply connector. The board is available in an AT- (5V-only) or an ATX-version.
- Plug a memory module into the memory socket of the EPIC.
- Connect the CRT monitor to the CRT interface or a LCD panel to the JILI interface by using a corresponding adapter cable.
- Plug the keyboard and the mouse to the PS/2 connectors.
- Connect the floppy drive cable to the EPIC's floppy interface. Attach the floppy drive to the connector at the opposite end of the cable.
- Connect the power supply to the floppy's power connector.
- Plug a hard-drive data cable to the EPIC's hard-disk interface.
- Attach the hard disk to the connector at the opposite end of the cable.
- Connect the power supply to the hard disk's power connector.
- If required, plug the PC/104 and PC/104-Plus extension cards to the buses.
- Make sure all your connections have been made correctly.
- Turn on power.
- Enter the BIOS by pressing the F2 key during boot-up. Make all changes in the BIOS setup. See the BIOS chapter of this manual for details.

4 Specifications

4.1 Functional Specifications

Processor

- ULV Intel® Celeron® @ 400MHz or LV Intel® Celeron® @ 733MHz
- 1GHz LV Celeron (available only upon request)

Chipset

- Intel® 815E Chipset graphics memory-controller hub

Power Supply

- Full ATX power supply support
- +5V-only AT power-supply support as an option

Super I/O

- Two Winbond W83627HF

Cache

- On-die 256KB second level cache

Memory

- One 144-pin SODIMM interface that runs in synchronous (133/133) mode and in pseudo-synchronous (133/100) mode with FSB133 3.3V PC-133 or PC-100 unbuffered SDRAM, up to 512MB

Four Serial Ports (COM A to COM D)

- RS232C serial port (1 DSUB9 on the front; 3 internal, 10-pin headers)
- 16550-compatible
- One port configurable as RS422/485

One Parallel Port (LPT1)

- Enhanced Parallel Port (EPP) and Extended Capabilities Port (ECP) with bi-directional capability

Floppy Interface

Compact Flash Socket

Enhanced Intelligent Drive Electronics (EIDE)

- Two Peripheral Component Interconnect (PCI) Bus Masters
- One IDE port support: Ultra 100 Direct Memory Access (UDMA100) mode for master slave configuration
- One Compact Flash Type 1 as EIDE Secondary Master

Universal Serial Bus (USB)

- 6 USB 2.0 ports
  (4 external ports over-current protected; 2 internal ports unprotected)
- USB legacy keyboard support
- USB floppy-, CDROM-, USB stick boot support

Two Ethernet Controllers

- 1x integrated Intel® 82562 10/100BASE-T LAN
- 1x Davicom DM9102AE/DM9102DE PCI Ethernet Controller
- Follows the common criteria of the embedded technology market segment

Onboard Video Graphics Array (VGA)

- Intel® 815E Chipset graphics memory controller hub
- CRT (Cathode Ray Tube)
- LCD (Liquid Crystal Display) flat panel 2x24bit LVDS interface that uses JILI

Audio

- Integrated Intel® SoundBlaster™ AC97
- Windows Sound System™ compatible
- 3 jack plugs (Line-in/Line-out/Mic).
- Extra standard Line-in connector (Motherboard-like)
- 5.1 Sound compatible

Phoenix BIOS, 1024KB Flash BIOS

- NV-EEPROM for CMOS Setup Retention without Battery

PS/2 Mouse and PS/2 Keyboard Controller

- Separate connectors

Watchdog Timer (WDT)

Real Time Clock (RTC) with Onboard Battery Supply

26 General Purpose Input/Outputs (GPIOs)

4.2 Mechanical Specifications

4.2.1 PC/104 Bus Connector (ISA part)

- One 2 X 32 pin stack-through and one 2 X 20 pin stack-through connector

4.2.2 PC/104-Plus Bus Connector (PCI part)

- One 4 x 30 pin 2mm downward connector

4.2.3 Dimensions

- Length x Width: 115mm x 165mm (4,53" x 6,49")

4.2.4 Height on Top

- Maximum 32mm (1.26”)
- Height is depending upon DDR SDRAM module and CPU cooler/fan.

4.2.5 Height on Bottom

- Maximum 6.8mm (0.27”)

4.2.6 Weight

- About 340g (full featured version without SDRAM-SODIMM)

4.3 Electrical Specifications

4.3.1 Supply Voltages

EPIC CPU boards can be equipped with two different power-supply connectors. The ATX connector version requires at least +5V and +5V standby, while the AT connector version operates at +5V-only. The voltages +3.3V, +12V, -12V and –5V are not required for the operation of the EPIC itself. Varying voltages may be required for peripheral devices such as backlight inverters or PC/104 and PC/104-Plus extension modules.

- +5V DC +/- 5%
- +5V DC Standby +/- 5%
- +3,3V DC (required for 3.3V PC/104-Plus extension cards)
- +12V DC (required for some PC/104, PC/104-Plus extension cards or for JILI cables)
- -12V DC (required for some PC/104, PC/104-Plus extension cards)

4.3.2 Supply Voltage Ripple

- 100mV peak to peak 0 - 20MHz

4.3.3 Supply Current (typical)

The EPIC/CE is equipped with power-saving features. Different power-consumption tests were executed to give an overview of the electrical conditions for several operational states. The board used a 256MB SDRAM module for test results shown below. An attached hard disk was not supplied through the measurement path, and there was no extension module in the system.

EPIC/CE 400MHz

Operational State	ATX Power Supply		AT Power Supply
	+5V	+5V Standby	+5V only
DOS Prompt	2.32A	150mA	2,47A
DOS Standby	1.81A	150mA	1.95A
Windows Idle	1.91A	150mA	2.06A
Windows 100% CPU Load	2.22A	150mA	2.36A
Windows 3D performance	2.73A	150mA	2.96A

EPIC/CE 733MGHz

Operation State	ATX Power Supply		AT Power Supply
	+5V	+5V Standby	+5V only
DOS Prompt	3.07A	160mA	2.98A
DOS Standby	2.11A	160mA	2.37A
Windows Idle	2.19A	160mA	2.51A
Windows 100% CPU Load	3.05A	160mA	3.41A
Windows 3D performance	3.59A	160mA	4.01A

4.3.4 Supply Current (maximum)

Board	ATX Power Supply		AT Power Supply
	+5V	+3.3V	+5V only
EPIC/CE 400MHz	3.42A	170mA	3.70A
EPIC/CE 733MHz	4.49A	180mA	5.02A

(Calculated theoretical values from all components maximum supply currents)

4.3.5 Real-time Clock (RTC) Battery

- Voltage range: 2.5 - 4.0V (typ 3.0V)
- Quiescent current: max. 3,5uA@ 3.0 V

English:
CAUTION ! Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.

Deutsch:
VORSICHT ! Explosionsgefahr bei unsachgemäßem Austausch der Batterie. Ersatz nur durchden selben oder einen vom Hersteller empfohlenen gleichwertigen Typ. Entsorgung gebrauchter Batterien nach Angaben des Herstellers.

French:
ATTENTION ! Risque d'explosion avec l'échange inadéquat de la batterie. Remplacement seulement par le même ou un type équivalent recommandé par le producteur. L'évacuation des batteries usagées conformément à des indications du fabricant.

Danish:
ADVARSEL ! Lithiumbatteri – Eksplosionsfare ved fejlagtig Håndtering. Udskifting må kun skemed batteri af samme fabrikant og type. Lever det brugte batteri tilbage til leverandØren.

Finnish:
VAROITUS ! Paristo voi rãjãhtãã, jos se on virheellisesti asennettu. Vaihda paristo ainoastaan laltevalmistajan suosittelmaan tyyppiln. Havita kaytetty paristo valmistajan ohjeiden mukaisesti.

Spanish:
Precaución ! Peligro de explosión si la batería se sustituye incorrectamente. Sustituya solamente por el mismo o tipo equivalente recomendado por el fabricante. Disponga las baterías usadas según las instrucciones del fabricante.

The battery of this product is not considered to be accessible by the end user. Safety instructions are given only in English, German, French, Danish, Finish and Spanish. If the battery is accessible by the end user, it is in the responsibility of the customer to give the corresponding safety instructions in the required language(s).

4.4 MTBF

The following MTBF (Mean Time Between Failure) values were calculated using a combination of manufacturer's test data (if the data was available) and a Bellcore calculation for the remaining parts. The Bellcore calculation involved the "Method 1 Case 1" method. In that particular method, the components were assumed to be operating at a 50% stress level in a 40° C ambient environment, and the system was assumed to have not been burned in. Manufacturer's data was used wherever possible. The manufacturer's data, when used, was specified at 50° C, which means that the following results were slightly conservative. The MTBF values shown below were for a 40° C office or telecommunications environment. Higher temperatures and other environmental stresses (extreme altitude, vibration, and salt water exposure) will lower the MTBF values.

➤ System MTBF (hours) : To Be Done

Notes: *Fans shipped with Kontron Embedded Modules GmbH products have an operating life of up to 50,000 hours. The estimates above assumed that a passive heat-sinking arrangement was used instead of a fan. Estimated RTC battery life (as opposed to battery failures) was not accounted for in the above figures and needs separate consideration. Battery life depends on temperature and operating conditions. When the Kontron unit has external power, battery drain comes from leakage paths.*

4.5 Environmental Specifications

4.5.1 Temperature

The Intel® Celeron® is specified for proper operation when the junction temperature is within the specified range of 0°C to 100°C.

The Intel® 815E chipset temperature runs at a maximum of 100°C. The Intel® ICH4 I/O Controller Hub 4 (82801DB) case temperature runs at a maximum of 110°C.

The processor protects itself from catastrophic overheating by use of an internal thermal sensor at a temperature level of approximately 135°C.

- Operating: 0 to +60 C (*) (with appropriate airflow)
- Non-operating: -10 to +85 °C (non-condensing)

Note: *(*) The maximum operating temperature is the maximum measurable temperature on any spot on the module's surface. You must maintain the temperature according to the above specification.*

4.5.2 Humidity

- Operating: 10% to 90% (non-condensing)
- Non-operating: 5% to 95% (non-condensing)

5 CPU, Chipset and Super I/O

5.1 CPU

The EPIC/CE is available with an Intel® LV/ULV Celeron® central processing unit (CPU) at speeds of either 400MHz or 733MHz.

Intel® LV/ULV Celeron® CPU features include:

- Support for the Intel Architecture with Dynamic Execution
- On-die primary 16-Kbyte instruction cache and 16-Kbyte write-back data cache
- On-die second level cache (256-Kbyte) with Advanced Transfer Cache Architecture
- Data Pre-fetch Logic
- Integrated math co-processor
- Support for MMX™ technology
- Support for Streaming SIMD Extensions
- Power-Management Features, including Quick Start, Deep Sleep and Deeper Sleep modes, which provide low-power dissipation

5.2 Chipset

The chipset of the EPIC/CE consists of the Intel® 815E chipset GMCH (Graphics and Memory Controller Hub) and the Intel ® 82801DB ICH-4 (I/O Controller Hub 4).

5.2.1 GMCH (815E Chipset)

Processor/Host Bus Support

- Intel® Pentium® III processor and Intel® Celeron®
- Supports processor's 370-Pin Socket
- Supports 32-Bit System Bus Addressing
- 4 deep in-order queue; 4 or 1 deep request queue
- In-order and Dynamic Deferred Transaction Support
- 66/100/133MHz System Bus Frequency
- GTL+ I/O Buffer

Integrated SDRAM Controller

- 32MB to 512MB using 16Mb/64Mb/128Mb/256Mb technology
- 64-bit data interface
- 100/133MHz system memory bus frequency
- Support for Asymmetrical SDRAM addressing only
- Support for x8 and x16 SDRAM device width
- Un-buffered, non-ECC SDRAM only supported
- Refresh Mechanism: CBR ONLY supported
- Enhanced Open page arbitration SDRAM paging scheme

Integrated Graphics Controller

- 3D Hyper Pipelined Architecture
- Full 2D H/W Acceleration
- Motion Video Acceleration
- Mip Maps with Trilinear and Anisotropic Filtering
- 85MHz Flat-Panel Monitor/Digital CRT Interface Or Digital Video
- Integrated 24-bit 230MHz RAMDAC
- Gamma Corrected Video
- DDC2B Compliant
- Up to 1600x1200 in 8-bit Color at 85Hz Refresh
- Hardware Accelerated Functions
- 3 Operand Raster Bit BLTs
- 64x64x3 Color Transparent Cursor

Power-Management Functions

- Stop Clock Grant and Halt special cycle translation from the host to the hub interface
- ACPI compliant power management
- APIC buffer management

5.2.2 ICH4 (82801DB)

PCI 2.2 Bus interface at 33MHz

Integrated LAN controller

- WfM 2.0 and IEEE 802.3 compliant
- 10/100 Mbit/s Ethernet support

USB

- Three UHCI USB 1.1 or one EHCI high speed USB 2.0 host controller(s)
- Supports up to 6 ports (4 available on EPIC board's front; 2 internal)

AC-Link for AC'97 support

Integrated IDE controller

- Ultra ATA/100/66/33 and PIO mode support
- Two channels for up to 3 devices with independent timing
- Support of "Native Mode" register and interrupts

Interrupt Controller

- Two cascade 83C59 with 15 interrupts
- Integrated I/O APIC capability with 24 interrupts

Enhanced DMA

- Two cascaded 8237 controllers
- Supports PC/PCI DMA and LPC DMA
- Supports DMA collection buffers

Timers based on 82C54

Power-Management Logic

- ACPI 2.0 compliant
- Supports PCI PME#

Low Pin Count (LPC) interface

SM (System Management) Bus 2.0 interface

5.3 Super I/O

Two super I/O Winbond W83627HF devices are connected to the LPC (Low Pin Count) Bus. These devices provide the following additional features:

- Four serial ports (one RS232 available on EPIC board's front and three ports by internal
  connectors with one port capable of RS422/RS485 functionality)
- One Multi-Mode Parallel Port
- Floppy Disk Controller
- PS/2-Keyboard and PS/2-Mouse Interface
- 26 GPIOs

5.4 CPU, Chipset and Super-I/O Configuration

See the Advanced Menu and its submenus section in the Appendix B: BIOS chapter for information on setting choices.

6 System Memory

The EPIC/CE uses a 144-pin Small Outline-Dual Inline Memory Modules (SODIMM) on the bottom side of the board. One socket is available for 3.3 Volt (power level) un-buffered PC-133 or PC-100 Synchronous Dynamic Random Access Memory (SDRAM) of 8, 16, 32, 64, 128, 256 or 512MB.

The total amount of memory available on the SDRAM module is used for main memory and graphics memory on the EPIC/CE. The Unified Memory Architecture (UMA) manages how the system shares memory between the graphics controller and the processor. The full system memory size is not available for software applications. In legacy mode, up to 1MB of system memory is used for graphics memory. The graphics-controller driver of the operating system can extend the amount of video memory to a maximum of 32MB.

7 ISA and PCI Bus Expansion

The design of the EPIC/CE follows the standard EPIC (**E**mbedded **P**latform for **I**ndustrial **C**omputing) form factor and offers ISA- and PCI-bus signals. The PC/104-Plus standard is downward compatible with PC/104 and enables the use of standard PC/104 and PC/104-Plus adapter cards as on-top modules.

7.1 PC/104 Bus (ISA part)

The PC/104 bus consists of two connectors that use 104 pins in total.

- XT bus connector (64 pins)
- AT bus connector (40 pins, which is optional for 16-bit, data-bus system)

The pin-out of the PC/104 bus connectors corresponds to the pin-out of the ISA bus connectors with some added ground pins. The two PC systems with different form factors are electrically compatible.

The **XT bus connector**, Row A and B.

The corresponding 64-pin female header (ISA bus = 62pins) has two added ground pins at the end of the connector (Pin A32 and Pin B32). The pin-out between PC/104 bus and XT ISA bus is identical between A1 - A31 and B1 - B31.

The **AT bus extension connector**, Row C and D.

The corresponding 40-pin female header (ISA bus = 36 pins) has four added ground pins, including two on each side of the connector. To avoid confusion, the first two pins are defined as Pin C0 and Pin D0. The additional ground pins at the end of the connector are defined as C19 and D19. The pin-out between PC/104 bus and AT ISA bus is identical between C1 - C18 and D1 - D18.

7.1.1 PC/104 Connectors

The EPIC/CE features the XT bus and AT bus extension on two, dual-row socket connectors with a 2.54mm x 2.54mm grid (0.1" x 0.1").

The PC-104 bus is available through Connectors J16B and J16C.

A description of the signals, including electrical characteristics and timings is beyond the scope of this document. Please refer to the official ISA bus and PC/104 specifications for more details.

7.1.2 PC/104 Configuration

When using add-on boards on the PC/104 bus, make sure that there are no resource conflicts in the system. Carefully choose hardware interrupts, DMA channels, and memory and I/O address ranges to avoid resource conflicts, which are often the reason for a board or a feature not functioning correctly. See Appendix A: System Resource Allocation for information about the resources already used by the EPIC/CE.

7.2 PC/104-Plus (PCI part)

The EPIC/CE offers the PC/104-Plus bus on a quad-row female connector with a 2mm x 2mm (0.79" x 0.79") pitch. This connector implements the standard 32-bit PCI bus signals.

7.2.1 PC/104-Plus Connector

You can only use PC/104-Plus adapter boards on top of an EPIC/CE.

The PC/104-Plus bus is available through Connector J8.

A description of signals, including electrical characteristics and timings, is beyond the scope of this document. Please refer to the official PCI bus and PC/104-Plus specifications for more details.

Warning: EPIC-CE in 5V-only version supply the +3.3V to the PC/104-Plus connector via an onboard DC/DC converter. The DC/DC converter is only capable to supply a maximum of 500mA to +3.3V extension cards. As there is no protection on this +3.3V supply, the user has to make sure not to exceed this value with his PC/104-Plus add-on cards.

7.2.2 PC/104-Plus Configuration

Add-on boards on the PC/104-Plus bus have to be associated to a "PCI-slot." Make sure that there are no resource conflicts in the system. Carefully choose PCI interrupts, REQ/GNT pairs, and IDSEL for the add-on board. See the technical manual of the add-on board for more details.

The EPIC/CE's PCI bus can be configured to optimize your system. See the PCI Configuration Submenu in Appendix B: BIOS for more information on configuration.

8 Keyboard and Mouse Interfaces

The EPIC/CE offers a PS/2-keyboard and PS/2-mouse interface on Connector X18. The upper interface is for the Mouse and the lower interface for the Keyboard connection. To find the location of the keyboard and mouse connector, please see the Appendix E: Connector Layout chapter.

8.1 PS/2-Keyboard Connector

The following table shows the pin-out of the PS/2-keyboard connector on the front.

Header	Pin	Signal Name	Function
	1	KBDAT	PS/2 Keyboard data (bi-directional I/O)
	2	NC	Not connected
	3	GND	Ground
	4	VCC *	+5V
	5	KBCLK	PS/2 Keyboard clock (bi-directional I/O)
	6	NC	Not connected

Notes: *(*) To protect the external power lines of peripheral devices, make sure that:*
-- the wires have the right diameter to withstand the maximum available current
-- the enclosure of the peripheral device fulfils the fire-protecting requirements of
-- IEC/EN 60950.

8.2 PS/2-Keyboard Configuration

Refer to the Keyboard Features submenu and the I/O Device Configuration submenu in the Appendix B: BIOS chapter for information on configuration.

8.3 PS/2-Mouse Connector

The following table shows the pin-out of the PS/2-Mouse connector on the front.

Header	Pin	Signal Name	Function
	1	MSDAT	Mouse data (bi-directional I/O)
	2	NC	Not connected
	3	GND	Ground
	4	VCC *	+5V
	5	MSCLK	Mouse clock (bi-directional I/O)
	6	NC	Not connected

Notes: *(*) To protect the external power lines of peripheral devices, make sure that:*
-- the wires have the right diameter to withstand the maximum available current
-- the enclosure of the peripheral device fulfils the fire-protecting requirements of
-- IEC/EN 60950.

8.4 PS/2-Mouse Configuration

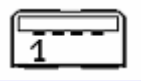
You can set the PS/2 mouse to enabled, disabled or auto-detect from the BIOS Setup. If you enable the mouse, IRQ12 is used as the interrupt and is no longer available for other devices. Please refer to the Miscellaneous Submenu in the Appendix B: BIOS chapter for additional information on configuration.

9 USB Interfaces

The EPIC/CE offers 6 USB ports. These ports are driven by three UHCI USB 1.1 controllers or one EHCI USB 2.0 controller(s). Four of the 6 USB ports are available on the EPIC/CE front and two more ports are available on internal connectors. You can expand the ports for up to 127 USB peripherals by using external USB hubs.

9.1 Front Connectors (USB 0 to USB 3)

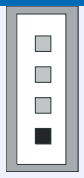
The four USB interfaces on the front are available through the multi-functional Connectors X5 and X21. To find the location of the USB connectors, please see the Appendix E: Connector Layout chapter. The following table shows the pin-out of these USB interfaces.

Header	Pin	Signal Name	Function
	1	VCC *	USB supply (max. 500mA)
	2	USB-	USB Port (-)
	3	USB+	USB Port (+)
	4	GND	USB Ground

Notes: *(*) To protect the external power lines of peripheral devices, make sure that:*
-- the wires have the right diameter to withstand the maximum available current
-- the enclosure of the peripheral device fulfils the fire-protecting requirements of
-- IEC/EN 60950.
The USB power lines are protected with a resetable fuse and are limited to 500mA.

9.2 Internal Connectors (USB 4 and USB 5)

The two internal USB interfaces are available through the Connectors X20 and X25 (4 pins). The following table shows the pin-out of these additional USB interfaces.

Header	Pin	Signal Name	Function
	1	VCC *	USB supply (max. 500mA)
	2	USB-	USB port (-)
	3	USB+	USB port (+)
	4	GND	USB Ground

Notes: *(*) To protect the external power lines of peripheral devices, make sure that:*
-- the wires have the right diameter to withstand the maximum available current
-- the enclosure of the peripheral device fulfils the fire-protecting requirements of
-- IEC/EN 60950.
The USB power lines are not protected. An additional resetable fuse is recommended.

9.2.1 Limitations of USB Ports 4 and 5

The power contacts for USB devices on Pin 1 and Pin 4 are not protected. They are suitable to supply connected USB devices with a maximum of 500mA power dissipation. Do not supply external USB devices with higher power dissipation through these pins. Always use a fuse when powering external USB devices through these pins, otherwise a defective USB device may damage the EPIC/CE. Kontron recommends using a resettable fuse, which follows the USB 1.1 specification, for power on external USB connectors.

9.3 Configuration

You can enable or disable the three USB UHCI Host Controllers in the BIOS Setup Utility for support of USB 1.1 devices. USB Host Controller 1 serves the two USB Ports 0 and 1 on the front. USB host Controller 2 serves the USB Ports 2 and 3 on the front. USB Controller 3 only needs to be enabled for the use of two more internal ports.

For high-speed USB 2.0 support of all 6 available ports, enable the USB EHCI Host Controller.

You also can enable or disable the legacy USB support. Legacy support is required for a USB keyboard and a USB Mouse when used with non USB aware operating systems such as Unix or DOS. It also is required to boot from USB mass storage devices. For more information, see the I/O Device Configuration Submenu section in Appendix B: BIOS Operation.

You can download available drivers or get driver download support information from the Kontron Web site. Kontron offers the latest Kontron-tested drivers, which can differ from newer ones. For further technical questions, contact your local support or get support information and downloadable software updates from Intel®.

Notes: *1.Some operating systems without USB 2.0 support do not work well with EHCI controller enabled. If you install such an OS at the EPIC/CE please disable the EHCI controller in the Setup Utility before installation.*
2.For operating systems not listed on our Web site please contact your OS distributor for an USB 2.0 driver. We are not allowed by law to ship USB 2.0 drivers.

10 Ethernet Interfaces

The EPIC/CE comes with two Ethernet interfaces. The first Ethernet interface uses the ICH4's integrated 32-bit PCI LAN controller in combination with the Intel® 82562 platform LAN connect device. The second Ethernet interface uses a Single Chip Fast Ethernet NIC Controller from Davicom (DM9102A/DM9102DE).

The two network controllers support a 10/100Base-T interface. The devices auto-negotiate the use of a 10Mbit/sec or 100Mbit/sec connection.

All major network-operating systems and several real-time and embedded operating systems support the interface.

10.1 First Ethernet Controller

Intel® 82562 features include:

- IEEE 802.3 10Base-T/100Base-TX Compliant Physical Layer Interface
- IEEE 802.3u Auto-Negotiation Support
- IEEE 802.3x Full Duplex Flow Control Standard
- Digital Adaptive Equalization Control
- Link Status Interrupt Capability
- 10Base-T auto-polarity correction
- Platform LAN Connect Interface Support
- Diagnostic Loop back Mode
- 1:1 transmit transformer ratio support
- Low power (less than 300mW in active transmit mode)
- Reduced power in "unplugged mode"

Note: *The Ethernet interface works according to the common criteria of the embedded technology market segment.*

10.2 Second Ethernet Controller

The Davicom DM9102A provides the following features:

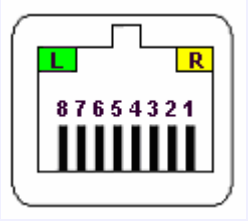
- Integrated Fast Ethernet MAC, Physical Layer, and transceiver on one chip
- Compliance with PCI Specification 2.2
- PCI-bus-master architecture
- EEPROM 93C46 interface supports node ID, access-configuration information
- Compliance with IEEE 802.3u 100Base-TX and 802.3 10Base-T
- Compliance with IEEE 802.3u auto negotiation protocol for automatic link- type selection
- Full-duplex/half-duplex capability
- Support IEEE 802.3x Full Duplex Flow Control
- Digital clock recovery circuit using advanced digital algorithm to reduce jitter
- High-performance 100Mbps clock generator and data-recovery circuit
- Loop back mode for easy system diagnostic

Note: *The Ethernet interface works according to the common criteria of the embedded technology market segment.*

10.3 Connectors

The 10/100Base-T interfaces are standard 8-pin RJ45 jacks. They are available at the front of the EPIC/CE through the multi-functional Connector X21 (Intel®) and Connector X5 (Davicom). To find the location of the Ethernet interfaces, please see the Appendix E: Connector Layout chapter.

The following table shows the pin-out of the Ethernet connectors.

Header	Pin	Signal Name	Function	In/Out
	1	TXD+	100/10BASE-T Transmit	Differential Output
	2	TXD-	100/10BASE-T Transmit	Differential Output
	3	RXD+	100/10BASE-T Receive	Differential Input
	4	NC **	For internal use only	
	5	NC **	For internal use only	
	6	RXD-	100/10BASE-T Receive	Differential Input
	7	NC **	For internal use only	
	8	NC **	For internal use only	
	L	Left LED	Link	Green/Orange
	R	Right LED	Activity	Yellow

NOTE: ***(*\)*** *Do not connect anything to these pins!*

10.4 Configuration

The onboard LAN controllers can be enabled or disabled from the BIOS Setup Utility. You also can enable the onboard LAN PXE boot ROM to allow the system to boot-up via a network connection from a PXE boot server. Refer to the I/O Device Configuration Submenu in the Appendix B: BIOS Operation chapter for additional information on configuration.

You can download available drivers from the Kontron Web site. For further information read the read-me file or contact technical support.

10.5 Ethernet Technical Support

You can solve some problems by using the latest drivers for both LAN controllers. Kontron provides you with the latest Kontron-tested drivers, which can differ from newer ones. For further technical support, contact either Kontron or get support information and downloadable software updates from Intel® and Davicom.

11 Graphics Interfaces

11.1 Video Controller

The EPIC/CE uses the graphics accelerator integrated in the Intel® 815E chipset. It delivers high performance 2D, 3D and video capabilities. With its interface to UMA (Unified Memory Architecture), up to 1MB of legacy system memory is used as video memory. The video memory can be extended to 32MB by the use of the available "Intel® Extreme Graphics" drivers.

The controller can drive two of three interfaces with its graphics engines on the EPIC/CE:

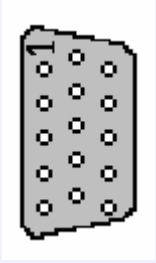
- Cathode Ray Tube (CRT) interface
- Low Voltage Differential Signaling (LVDS) interface

  -or-
- Optional Digital Video Output (DVO) port

11.2 CRT Connector

The CRT (Cathode Ray Tube) interface is available through the standard DSUB15 connector, which is part of the multi-function Connector X1 on the front. To find the location of the CRT interface, please see the Appendix E: Connector Layout chapter.

The following table shows the pin-out of the CRT connector.

Header	Pin	Signal Name	Function
	1	RED	Red Video
	2	GRN	Green Video
	3	BLU	Blue Video
	4	NC	Not connected
	5	GND	Ground
	6	GND	Ground
	7	GND	Ground
	8	GND	Ground
	9	NC	Not connected
	10	GND	Ground
	11	NC	Not connected
	12	DDDA	DDC Serial Data Line
	13	HSYNC	Horizontal Sync
	14	VSYNC	Vertical Sync
	15	DDCK	DDC Data Clock Line

11.3 DVO Connector (optional)

The optional DVO (Digital Video Output) interface is available on Connector X4, a 50-pin, flat-foil connector on the bottom side of the board. This connector is not available on standard products. To find the location of the DVO interface, please see the Appendix E: Connector Layout chapter. DVO interface usage excludes LVDS interface usage.

The following table shows the pin-out of the DVO connector.

Pin	Signal Name	Function	Pin	Signal Name	Function
1	NC	Not connected	2	DVOBD0	Data 0
3	NC	Not connected	4	VCC	+5V Power
5	DVOBD1	Data 1	6	NC	Not connected
7	DVOBD2	Data 2	8	VCC	+5V Power
9	NC	Not connected	10	DVOBD3	Data 3
11	NC	Not connected	12	GND	Ground
13	DVOBD4	Data 4	14	NC	Not connected
15	DVOBD5	Data 5	16	GND	Ground
17	NC	Not connected	18	DVOBD6	Data 6
19	NC	Not connected	20	GND	Ground
21	DVOBD7	Data 7	22	NC	Not connected
23	DVOBD8	Data 8	24	GND	Ground
25	NC	Not connected	26	DVOBD9	Data 9
27	NC	Not connected	28	GND	Ground
29	DVOBD10	Data 10	30	NC	Not connected
31	DVOBD11	Data 11	32	GND	Ground
33	CLKB0	Clock Out 0	34	CLKB1 (opt)	Clock Out 1
35	GND	Ground	36	NC	Not connected
37	NC	Not connected	38	PD_NS	
39	VSYNCB	Vertical Sync	40	HSYNCB	Horizontal Sync
41	/BLANKB	Flicker Blank	42	FLDSTLB	
43	NC	Not connected	44	NC	Not connected
45	NC	Not connected	46	NC	Not connected
47	DVOINT	LCD Interrupt	48	LTVDAT	LCD/TV Data
49	LTVCLK	LCD/TV Clock	50	VREF	Reference

11.4 Flat Panel LVDS Interface (JILI) Connector

The interface for the LCD Panel is available through Connector J4 (40 pins) on the bottom side of the board. To find the location of the LCD Panel interface connector, please see the Appendix E: Connector Layout chapter.

This connector represents the JILI interface (**J**UMPtec **I**ntelligent **L**VDS **I**nterface). The implementation of this subsystem complies with the JILI Specification from Kontron Embedded Modules GmbH. This supports the JILI3 implementation. A variety of cables for different display types are available from Kontron. Please refer to the actual cable list on the Kontron Web site for part numbers and cable names. A detailed description of the JILI interface standard also is available in a separate document JILIM???.PDF. The three question marks represent the documents revision number. You can download this document from the Kontron Web site, or contact your local Kontron technical support to receive it.

11.5 Display Power Considerations

When using a LCD Panel, additional voltages may be required to drive the display's logic and to supply the backlight converter and the contrast voltage.

The display logic may require +5V for standard or +3.3V for low-power LCDs. Contrast voltages for passive displays are normally very different and can range from –30V to +30V. Backlight converters usually are +5V or +12V types. When using a Kontron JILI cable, you do not need to determine the configuration. Display logic voltage and contrast voltage come pre-configured on the JILI cable. On occasion, the backlight voltage has to be adjusted on the cable.

Even though the EPIC/CE also is available as a +5V-only board, you need to supply the +12V for the backlight converter when using such a converter type.

The onboard 3.3V-circuitry of the EPIC/CE and the +3.3V logic voltage of low-voltage panels are powered by separate voltage regulators. The one for the LCD is mounted on the JILI adapter cable.

11.6 Connecting a LCD Panel

To determine whether your panel display is supported, check the Kontron Web site for panel lists. We regularly update the list of panels that have been tested with our boards.

Many panel adapters for a wide spread variety of displays are available through Kontron. If you use one of those adapters supplied by Kontron, configuration is easy:

- Check whether you have the correct adapter and cable for the panel you plan to use. Inspect the cable for damages.
- Disconnect the power from your system.
- Connect the panel adapter to the LCD Panel connector (JILI) on the EPIC/CE.
- Connect the other end of the cable to your display.
- Connect the backlight converter.
- Supply power to your system.
- If no image appears on your display, connect a CRT monitor to the CRT connector.
- If necessary program the EEPROM on the JILI cable with the matching configuration data.
- If you still do not see improvement, consider contacting the dealer for technical support.

11.7 Configuration

You can set the general configuration for the graphics controller in the BIOS setup utility. Refer to the Advanced Chipset Control submenu and the Display Control submenu in the Appendix B: BIOS Operation chapter for more configuration information.

You can download available drivers for the graphics controller from the Kontron Web site. For further information read the read-me or help files or contact technical support.

11.8 Graphics Technical Support

If problems occur, you can solve some of them by using the latest drivers for the graphics controller. Kontron provides you with the latest tested drivers, which can differ from newer ones. For further technical support, contact either Kontron, or obtain support information and downloadable software updates from Intel®.

11.9 Available Video Modes

The following list shows the video modes supported by the graphics controller with their maximum legacy frame-buffer size. When configured for smaller frame buffers and/or using a LCD panel on the JILI interface, not all of the video modes listed below may be available. Capability depends on the system configuration and on the display. Different operating systems also may not support all listed modes by the available drivers.

11.9.1 Standard IBM-Compatible VGA Modes

Video Mode	Type	Characters/Pixels	Colors/Gray val.
00h/01h	Text	40x25	16
02h/03h	Text	80x25	16
04h/05h	Graphics	320x200	4
06h	Graphics	640x200	2
0Dh	Graphics	320x200	16
0Eh	Graphics	640x200	16
0Fh	Graphics	640x350	Mono
10h	Graphics	640x350	16
11h	Graphics	640x480	2
12h	Graphics	640x480	16
13h	Graphics	320x200	256

11.9.2 Extended VESA VGA Modes

VESA	Display	Pixels	Colors
100h	Graphics	640x400	256
101h	Graphics	640x480	256
102h	Graphics	800x600	16
103h	Graphics	800x600	256
105h	Graphics	1024x768	256
109h	Text	132x25	16
10Ah	Text	132x43	16
10Bh	Text	132x50	16
10Ch	Text	132x60	16
10Eh	Graphics	320x200	64K
110h	Graphics	640x480	32K
111h	Graphics	640x480	64K
112h	Graphics	640x480	16M
113h	Graphics	800x600	32K
114h	Graphics	800x600	64K
11Ch	Text	128x37	16
11Dh	Graphics	320x200	256
127h	Graphics	640x400	64K
128h	Graphics	640x400	16M

12 Serial-Communication Interfaces

12.1 Serial Ports COM A to COM D

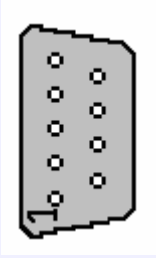
Four fully functional serial ports (COM A, COM B, COM C, and COM D) provide asynchronous serial communications. The serial ports support RS-232 operation modes and are compatible with the serial-port implementation used on the IBM Serial Adapter. You also can use COM D for RS-422/485 communications. The ports are 16550 high-speed UART compatible and support 16-byte FIFO buffers for transfer rates up to 115.2Kbaud. COM A is available on a standard DSUB9 connector on the front while the other COM ports are available on internal connectors.

COM A is available through the standard DSUB9 connector, which is part of the multi-function Connector X1 on the front. COM B to COM D are available through Connectors X15, X16 and X17 (10 pins in line). To find the location of the serial ports on the board, please see the Appendix E: Connector Layout chapter.

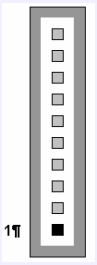
12.2 RS-232 Connectors

COM A is available through the standard DSUB9 connector, which is part of the multi-function Connector X1 on the front.

The following table shows the pin-out.

Header	Pin	Signal Name	Function	In / Out
	1	/DCD1	Data Carrier Detect	In
	2	SIN1	Receive Data	In
	3	SOUT1	Transmit Data	Out
	4	/DTR1	Data Terminal Ready	Out
	5	GND	Signal Ground	--
	6	/DSR1	Data Set Ready	In
	7	/RTS1	Request to Send	Out
	8	/CTS1	Clear to Send	In
	9	/RI1	Ring Indicator	In

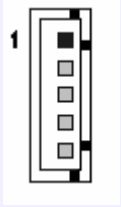
COM B to COM D are available through Connectors X15, X16 and X17 (10 pins in line). To have the signals available on the standard serial interface connectors DSUB9 or DSUB25, an adapter cable is required. A 9-pin DSUB cable is available from Kontron (KAB-DSUB9-3, Part Number 96061-0000-00-0).

Header	Pin	Signal Name	Function	In / Out	DSUB-25	DSUB-9
	1	/DCD	Data Carrier Detect	In	8	1
	2	/DSR	Data Set Ready	In	6	6
	3	SIN	Receive Data	In	3	2
	4	/RTS	Request to Send	Out	4	7
	5	SOUT	Transmit Data	Out	2	3
	6	/CTS	Clear to Send	In	5	8
	7	/DTR	Data Terminal Ready	Out	20	4
	8	/RI	Ring Indicator	In	22	9
	9	GND	Signal Ground	--	7	5
	10	VCC (*)	+5V	--	--	--

Notes: *(*) To protect the external power lines of peripheral devices, make sure that:*
-- the wires have the right diameter to withstand the maximum available current
-- the enclosure of the peripheral device fulfils the fire-protecting requirements of
-- IEC/EN 60950.

12.3 RS-485 Connector

You can use Connector X19 (COM D) for RS422/485 purposes.

Header	Pin	Signal Name	Function
	1	485_1RXD+	Channel A positive terminal
	2	485_1RXD-	Channel A negative terminal
	3	GND	Ground
	4	485_1TXD+	Channel B positive terminal
	5	485_1TXD-	Channel B negative terminal

The serial port COM D can only be used either as RS232 (Connector X17) or as RS422/RS485 (Connector X18).

12.4 Configuration

From the BIOS set-up utility, you can set the serial input/output interfaces to enabled, disabled or auto. The base I/O-addresses 3F8h, 2F8h, 3E8h, or 2E8h can be configured when enabled, as well as the interrupts IRQ3, IRQ4, IRQ10 and IRQ11. COM D can be set to the RS232 or RS485 interface. Refer to the I/O Device Configuration submenu in the Appendix B: BIOS Operation chapter for information on configuration.

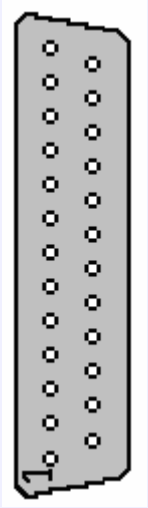
13 Parallel-Port Interface

The EPIC/CE incorporates an IBM XT/AT compatible parallel port. It supports uni-directional, bi-directional, EPP and ECP operating modes.

13.1 Connector

The parallel port is available through the standard DSUB25 connector which is part of the multifunctional Connector X1 on the front. To find the location of the parallel port, please see the Appendix E: Connector Layout chapter.

The following table shows the pin-out of the connector.

Header	Pin	Signal Name	Function	In / Out
	1	/STB	Strobe	Out
	2	PD0	Data 0	I/O
	3	PD1	Data 1	I/O
	4	PD2	Data 2	I/O
	5	PD3	Data 3	I/O
	6	PD4	Data 4	I/O
	7	PD5	Data 5	I/O
	8	PD6	Data 6	I/O
	9	PD7	Data 7	I/O
	10	/ACK	Acknowledge	In
	11	/BUSY	Busy	In
	12	PE	Paper out	In
	13	/SLCT	Select out	In
	14	/AFD	Autofeed	Out
	15	/ERR	Error	In
	16	/INIT	Init	Out
	17	/SLIN	Select in	Out
	18 - 25	GND	Signal Ground	--

13.2 Configuration

The parallel-port mode, I/O addresses, and IRQs are changeable from the BIOS Setup Utility. You can program the base I/O-address 378h (default), 3BCh or 278h. You can set the parallel port mode to disable, enable or AUTO (default). You can choose IRQ5 or IRQ7 as the parallel-port interrupt.

Refer to the I/O Device Configuration Submenu in the Appendix B: BIOS Operation chapter for additional information on configuration.

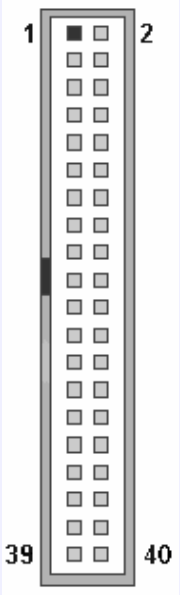
14 IDE Interfaces

PCI-bus devices serve as primary and secondary IDE hosts on the EPIC/CE. The controller supports up to Ultra DMA 100 mode, up to PIO mode 4 timing and multiword DMA mode 1 and 2 with independent timing. It also supports IDE legacy and IDE native mode configuration. The EPIC/CE features one IDE interface that can drive two hard disks and one CompactFlash socket. When two IDE devices share a single adapter, they are connected in a master/slave, daisy-chain configuration. If only one drive is in the system, you must set it as the master. The CompactFlash socket is implemented through the secondary host as master.

14.1 Connector

The IDE interface is available through Connector X24 (40 pins). To find the location of IDE interface, please see the Appendix E: Connector Layout chapter.

This interface is designed in 0.1" grid for optimal connectivity to a 3.5" hard drive. The following table shows the pin-out of the IDE connector.

Header	Pin	Signal Name	Function
	1	/HDRST	Reset
	2	GND	Ground
	3-18	PIDE_D1..D15	Primary IDE ATA data bus
	19	GND	Ground
	20	NC	Not connected
	21	PIDE_DRQ	Primary IDE DMA Request for IDE master
	22	GND	Ground
	23	/PIDE_IOW	Primary IDE IOWJ Command
	24	GND	Ground
	25	/PIDE_IOR	Primary IDE IORJ Command
	26	GND	Ground
	27	PIDE_RDY	Primary IDE ready
	28	PIDE_PD1	IDE1 Cable Select (470Ω to Ground)
	29	/PIDE_AK	Primary IDE DACK for IDE master
	30	GND	Ground
	31	PIDE_IRQ	IDE IRQ Primary
	32	NC	Not connected
	33	PIDE_A1	Primary IDE ATA address bus
	34	PIDE_ATAD	UDMA detection
	35	PIDE_A0	Primary IDE ATA address bus
	36	PIDE_A2	Primary IDE ATA address bus
	37	/PIDE_CS1	IDE chipselect 1 for primary channel 0
	38	/PIDE_CS3	IDE chipselect 2 for primary channel 1
	39	PIDE_ACT	Drive Activity
	40	GND	Ground

14.2 CompactFlash Socket

The CompactFlash socket (Connector X13 - 50 pins) for commercial CompactFlashes (Type I) is integrated on the bottom side of the EPIC/CE board. To find the location of the socket, please see the Appendix E: Connector Layout chapter.

Because the signals of the socket are connected to the secondary IDE, the socket is not a hot-plug interface. Turn off power to the system before adding or removing a CompactFlash card.

The following table shows the pin-out of the CompactFlash socket.

Pin	Signal Name	Function	Pin	Signal Name	Function
1	GND	Ground	2	D3	Data 3
3	D4	Data 4	4	D5	Data 5
5	D6	Data 6	6	D7	Data 7
7	/CS1	Chip select 1	8	GND	Ground
9	GND	Ground	10	GND	Ground
11	GND	Ground	12	GND	Ground
13	VCC	+5V	14	GND	Ground
15	GND	Ground	16	GND	Ground
17	GND	Ground	18	SA2	Addr. 2
19	SA1	Addr. 1	20	SA0	Addr. 0
21	D0	Data 0	22	D1	Data 1
23	D2	Data 2	24	IOCS16	16 bit CS
25	GND	Ground	26	GND	Ground
27	D11	Data 11	28	D12	Data 12
29	D13	Data 13	30	D14	Data 14
31	D15	Data 15	32	/CS3	Chip select 3
33	GND	Ground	34	/IOR	I/O read
35	/IOW	I/O write	36	VCC	+5V
37	IRQ	Interrupt	38	VCC	+5V
39	GND	Ground	40	NC	Not connected
41	/RESET	Reset	42	IOCHRDY	Ready
43	DRQ	DMA Request	44	DACK	Acknowledge
45	SIDE_ACT	Drive Activity	46	ATADET	ATA detect
47	D8	Data 8	48	D9	Data 9
49	D10	Data 10	50	GND	Ground

14.3 Configuration

The IDE interfaces offer several configuration settings. Refer to the Main Menu, the ACPI Control submenu, the I/O Device Configuration Submenu, and the Master or Slave Submenu in the Appendix B: BIOS Operation chapter for additional information on configuration.

Notes: *1. Use an UDMA flat-ribbon cable (80 lines) to drive UDMA66 or UDMA100 devices.*
2. When using a standard ribbon cable (40 lines) with UDMA66 or UDMA100 devices, disable the Ultra DMA Mode in the BIOS Setup Utility.

15 Floppy Interface

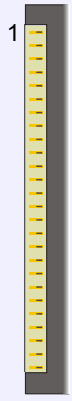
The floppy-drive interface of the EPIC/CE uses a 2.88MB super I/O floppy-disk controller and can support one floppy disk drive with densities that range from 360kB to 2.88MB.

15.1 Connector

The floppy disk interface is available on the flat-foil Connector X2 (26 pins). To find the location of floppy-drive interface on the EPIC/CE board, please see the Appendix E: Connector Layout chapter. This type of connector is often internally used in notebooks to connect a slim-line floppy drive.

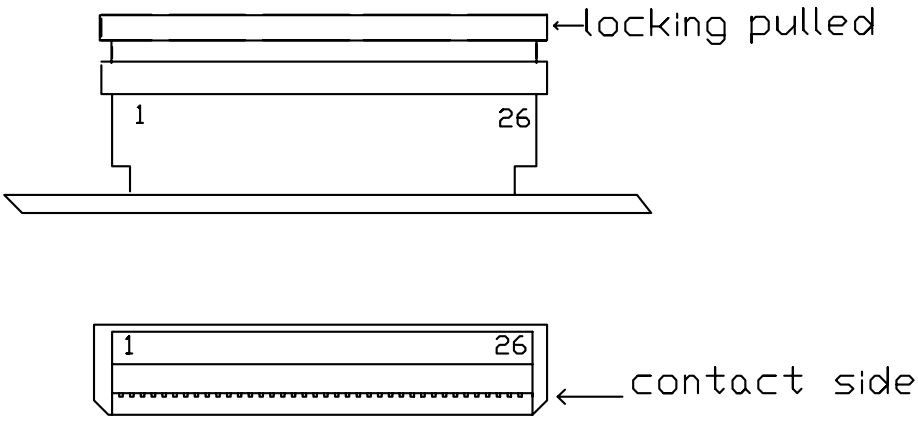
Accessories are available for this interface from Kontron. To connect a standard 3.5" floppy drive, use an adapter cable (ADA-FLOPPY-2, Part Number 96001-0000-00-0). If you have a slim-line 3.5" floppy drive, you may need a flat foil cable (KAB-FLOPPY/MOPS-1, Part Number 96019-0000-00-0). It also is possible to get a slim line 3.5" floppy drive with cable from Kontron (FLOPPY-MOPS-1, Part Number 96010-0000-00-0).

The following table shows the connector pin-out:

Header	Pin	Signal Name	Function	Pin	Signal Name	Function
	1	VCC *	+5V	2	/IDX	Index
	3	VCC *	+5V	4	/DR0	Drive Select 0
	5	VCC *	+5V	6	/DSKCHG	Disk Change
	7	NC	Not connected	8	NC	Not connected
	9	NC	Not connected	10	/MTR0	Motor on 0
	11	NC	Not connected	12	/FDIR	Direction Select
	13	NC	Not connected	14	/STEP	Step
	15	GND	Ground	16	/WDATA	Write Data
	17	GND	Ground	18	/WGATE	Write Gate
	19	GND	Ground	20	/TRK0	Track 00
	21	GND	Ground	22	/WRTPRT	Write Protect
	23	GND	Ground	24	/RDATA	Read Data
	25	GND	Ground	26	/HDSEL	Side One Select

Notes: *(*) To protect the external power lines of peripheral devices, make sure that:*
-- the wires have the right diameter to withstand the maximum available current
-- the enclosure of the peripheral device fulfils the fire-protecting requirements of
-- IEC/EN 60950.

15.1.1 Connector Diagram



15.2 Configuration

You can configure the floppy disk interface in the BIOS Setup Utility. You can choose the 3.5" (common) or 5.25" drive types with densities of 360kB, 720kB, 1.2MB, 1.25MB, 1.44MB or 2.88MB. Refer to the Main Menu and the Miscellaneous Menu section of the Appendix B: BIOS Operation chapter for more information on configuring the floppy drive.

You also can disable the floppy-disk interface in the I/O Device Configuration Submenu.

16 Sound Interface

The EPIC/CE uses a Realtek ALC650 sound codec. The ALC650 is an 18-bit, full duplex AC'97 2.2 compatible stereo audio CODEC designed for PC multimedia systems, including host/soft audio and AMR/CNR based designs. The ALC650 incorporates proprietary converter technology to achieve a high SNR, greater than 90 dB.

All major operating systems support the interface.

The ALC650 features:

- High-performance CODEC with high S/N ratio (>90 dB)
- 18-bit ADC and 20-bit DAC resolution
- Compliant with AC'97 2.2 Specifications
- 18-bit stereo full-duplex CODEC with independent and variable sampling rate
- One analog line-level stereo input with 5-bit volume control: LINE_IN, (CD_IN is possible)
- Stereo Output with 5-bit volume control
- MIC input
- Power-management capabilities
- Embedded 50mW/20ohm OP at front LINE output
- 6 Channel output for multi-channel applications

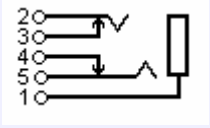
16.1 Connectors

The EPIC/CE offers two connectors related to the Sound feature. One is the jack connector on the front of the board and one is an internal connector.

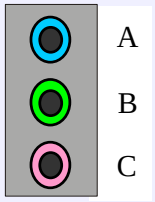
16.1.1 Jack Connector

The standard 3 position jack connector (X23) complies with the standard pin-out used in many commercially available motherboards. To find the location of the connector on the EPIC/CE board, please see the Appendix E: Connector Layout chapter. A special version of the EPIC/CE may only be equipped with a 2 position jack connector (for applications with mechanical restrictions). In this case only jacks „B" and „C" are available. The signals for Jack „A" are available on the internal connector X14.

The following table shows the general connection of each single audio jack.

Jack	Pin	Signal	Description
	1	ASGND	Analog Sound Ground
	2	XX	See Next Table
	3	NC	Not connected
	4	NC	Not connected
	5	XX	See Next Table

The individual pin-out of each jack connector is shown in the following table. (The configuration for multi-channel applications is described in *Italics*)

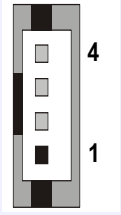
Header	Jack	Pin	Signal Name	Function
	A	2	AUXAL_C/ *REAR_L*	Line-input left. *Left Rear Speaker output for multi-channel applications*
		5	AUXAR_C/ *REAR_R*	Line-input right. *Right Front Speaker output for multi-channel applications*
	B	2	LEFT/ *FRONT_L*	Line-level stereo output left. *Left Front Speaker output for multi-channel applications*
		5	RIGHT/ *FRONT_R*	Line-level stereo output right. *Right Front Speaker output for multi-channel applications*
	C	2	MIC_C/ *CENTER*	Mono Microphone input. *Center Speaker output for multi-channel applications.*
		5	*LFE*	*Low Frequency output for multi-channel applications.*

16.1.2 Line-In/Rear Speakers Connector

Line-In or Rear Speaker signals (depending on the configuration) are always available on Connector X14. To find the location of the connector on the EPIC/CE board, please see the Appendix E: Connector Layout chapter.

If using these signals as Line-In, a CDROM can be connected using a standard CDROM Audio cable.

The pin-out of this connector complies with the standard pin-out used in many commercially available motherboards and it is shown in the following table.

Header	Pin	Signal Name	Function
	4	AUXAL_C/ *REAR_L*	Auxiliary A input left. Normally intended for connection to an internal or external CD-ROM analog output. *Left Rear Speaker output for multi channel applications*
	3	ASGND	Analog ground.
	2	AUXAR_C/ *REAR_R*	Auxiliary A input right. Normally intended for connection to an internal or external CD-ROM analog output. *Right Rear Speaker output for multi channel applications*
	1	ASGND	Analog ground.

16.2 Configuration

From the BIOS Setup Utility you can set the onboard legacy AC97 audio controller to Disabled or Enabled (default). Refer to I/O Device Configuration submenu in the Appendix B: BIOS operation for more details.

You can download available drivers for the sound controller from the Kontron Web site or use the drivers provided by the manufacturer Realtek. Search for ALC650 drivers for the required operating system and instructions on how to enable multi-channel support.

16.3 Technical Support for Sound

If problems occur, you can solve some of them by using the latest drivers for the Sound controller. Kontron provides you with the latest tested drivers, which can differ from newer ones. For further technical support, contact either Kontron, or obtain support information and downloadable software updates from Realtek.

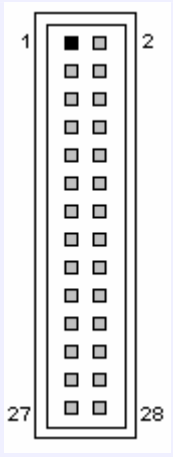
17 General Purpose Inputs/outputs

The EPIC/CE Board comes with 26 General Purpose Input/Outputs (GPIOs). Each pin is individually configurable as an input or open-drain output. When configured as output the user must provide a pull-up resistor to the desired output voltage level. All output pins have 12mA drive strength. (See the connector table in Appendix E for detailed information on each pin). The output low level is max. 0,4V.

17.1 Connector

The GPIOs are available on the 2mm grid 2 row connector X3 (28 pins). To find the location of the Connector on the EPIC/CE board, please see the Appendix E: Connector Layout chapter.

The following table shows the pin-out of the connector.

GPIO	Pin	Connector Top View	Pin	GPIO
GP0 *(12csu)	1		2	GP14 *(12t)
GP1 *(12csu)	3		4	GP15 *(12t)
GP2 *(12cs)	5		6	GP16 *(12t)
GP3 *(12cs)	7		8	GP17 *(12t)
GP4 *(12cs)	9		10	GP18 *(24t)
GP5 *(12cs)	11		12	GP19 *(12t)
GP6 *(12cs)	13		14	GP20 *(12t)
GP7 *(12csu)	15		16	GP21 *(24t)
GP8 *(24t)	17		18	GP22 *(12csu)
GP9 *(12t)	19		20	GP23 *(12cs)
GP10 *(12t)	21		22	GP24 *(12cs)
GP11 *(12t)	23		24	GP25 *(12cs)
GP12 *(12t)	25		26	GND
GP13 *(12t)	27		28	GND

Notes: **(12cs)* *CMOS level Schmitt-trigger bi-directional pin and open-drain output with 12mA sink capability*

**(12csu)* *CMOS level Schmitt-trigger bi-directional pin with internalpull up resistor and open-drain output with 12mA sink capability*

**(12t)* *TTL level bi-directional pin and open-drain output with 12mA sink capability*

**(24t)* *TTL level bi-directional pin and open-drain output with 24mA sink capability*

All of these signals are not galvanically isolated from the board. To ensure that the EPIC/CE Board is protected from electrical damage, implement external protection circuitry such as optocouplers at each signal.

17.2 Programming

17.2.1 16-Bit Operating Systems

The 26 GPIOs are driven by the two onboard Winbond W83627HF Super-I/O controllers on the Low Pin Count (LPC) bus. The second controller serves the GPIOs 0 to 21 via ports 4E/4Fhex; the first controller takes care of GPIOs 22 to 25 at ports 2E/2Fhex.

The W83627HF Super I/O controller consists of several logical devices, which correspond to individual functionality. Each Logical Device has its own configuration registers. The designer can access the desired configuration registers by selecting a logical device through the Extended Functions Data Register (I/O port index register 4Eh and data register 4Fh, or 2Eh and 2Fh respectively). The following table shows the relationship between Super I/O and GPIOs.

GPIO	Controller	Logical Device	Index Register Address	Data Register Address
GP0-7	Super-I/O 2	Logical Device 7	4Eh	4Fh
GP8-13	Super-I/O 2	Logical Device 9	4Eh	4Fh
GP14-21	Super-I/O 2	Logical Device 8	4Eh	4Fh
GP22-25	Super-I/O 1	Logical Device 7	2Eh	2Fh

The programming of the GPIOs is done in 4 steps:

Switch the Super-I/O to Extended Configuration access.

Select the logical device to be accessed.

Reprogram the configuration register of the logical device.

Disable the Extended Configuration access.

Switching to Extended Configuration Access

To enable the Extended Configuration Access, the Index Register of the corresponding Super-I/O has to be written two times with a value of 87hex. The example below shows how to enable the first Super-I/O for Extended Configuration accesses.

Example code:

```
MOV DX,2EH          ;Index Register Address
MOV AL,87H          ;Enable Code
CLI                 ;Disable Interrupts
OUT DX,AL           ;First Write
JMP $+2             ;Wait
OUT DX,AL           ;Second Write
STI                 ;Enable Interrupts
```

Selecting a Logical Device

You can select a logical device by writing the value 07hex to the Index Register address and the logical device number to the Data Register address. The example below shows how to select logical device 7 of the first Super-I/O controller.

Example code:

```
MOV DX,2EH        ;Index Register Address
MOV AL,07H        ;Logical Device Select Code
OUT DX,AL         ;
MOV DX,2FH        ;Data Register Address
MOV AL,07H        ;Logical Device Number
OUT DX,AL         ;
```

Reprogramming Configuration Registers of the Logical Device

After a logical device is selected, a set of configuration registers is available. These registers are responsible for the configuration of the GPIO functionality. You can set the direction (input/output) of every single GPIO with the configuration register F0hex. You also can invert every single GPIO for read as well as write operation by setting the corresponding bit in the configuration register F2hex. Configuration register F1hex is the data register to read from or write to.

Configuration Register	Purpose	Explanation	Default Value
F0hex	Direction	0 = output, 1 = input	11111111bin
F1hex	Data	Can only be read when programmed as input, can be read/written when programmed as output	00000000bin
F2hex	Inversion	0 = not inverted, 1 = inverted	00000000bin

The meaning of the single bits in each of these configuration registers is shown in the table below.

Super-I/O (Device)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2nd (7)	GP0	GP1	GP2	GP3	GP4	GP5	GP6	GP7
2nd (9)	RSVD (*)	RSVD (*)	GP8	GP9	GP10	GP11	GP12	GP13
2nd (8)	GP14	GP15	GP16	GP17	GP18	GP19	GP20	GP21
1st (7)	RSVD (*)	GP22	GP23	GP24	GP25	RSVD (*)	RSVD (*)	RSVD (*)

Notes: *(*) Do not write to bits marked as reserved (RSVD).*
These bits are used for other purposes. Normal operation of the board cannot be guaranteed if they are intentionally modified!

The example below shows how a selected GPIO port (logical device) of the first Super-I/O can be read.

Example code:

```
MOV DX,2EH        ;Index Register Address
MOV AL,F1H        ;Select config register for data
OUT DX,AL         ;
MOV DX,2FH        ;Data Register Address
IN AL,DX          ;Read data from data register
```

Disabling the Extended Configuration Access

To disable the Extended Configuration Access, the Index Register of the corresponding Super-I/O has to be written two times with a value of AAhex. The example below shows how to disable the first Super-I/O for Extended Configuration accesses.

Example code:

```
MOV DX,2EH          ;Index Register Address
MOV AL,AAH          ;Disable Code
CLI                 ;Disable Interrupts
OUT DX,AL           ;First Write
JMP $+2             ;Wait
OUT DX,AL           ;Second Write
STI                 ;Enable Interrupts
```

17.2.2 32-Bit Operating Systems

Kontron Embedded Modules GmbH offers a 32bit API (JIDA32), which also includes protected mode functions to read and write the GPIOs. This programmer's interface is available for the major 32-bit operating systems and can be downloaded from the Kontron Web site.

Detailed programming information about JIDA32 is beyond the scope of this document. Please refer to the JIDA32 documentation and the sample code, which is part of the JIDA32 package on the Kontron Web site.

17.3 Configuration

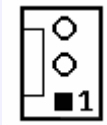
You cannot configure the GPIOs from the BIOS Setup utility. For programming see the section above.

18 FAN Interface

Some EPIC/CEs can be equipped with a fan. If a fan has to be changed or added, use this interface to connect a fan to cool the CPU. The connector and onboard system controller monitor the fan's speed. This connector supports 5V fans only.

18.1 Connector

The fan interface is available on Connector J1 (3 pins). For the location of the fan connector see Appendix E: Connector Layout.

Header	Pin	Signal Description	Function
	1	Sense	Speed Monitoring
	2	VCC *	+5V
	3	GND	Ground

Notes: *(*) To protect the external power lines of peripheral devices, make sure that:*
-- the wires have the right diameter to withstand the maximum available current
-- the enclosure of the peripheral device fulfils the fire-protecting requirements of
-- IEC/EN 60950.

18.2 Configuration

You can set the active trip point to a value from 40°C up to 100°C in the ACPI Control submenu of the BIOS Setup Utility. The fan will automatically turn on whenever this trip point temperature value is reached. Setting this item to disabled means the fan will always run, except when the operating system takes control of it.

19 Power Interface

The EPIC/CE is available with two power interface connectors. The boards can be powered by an ATX power connector or an AT power connector (+5V-only) version. The ATX-version has a 10 pin ATX connector as recommended by the PC/104 Consortium. The AT version uses the 4-pin power connector that also powers 3.5" hard disks.

19.1 Power Interface Connectors

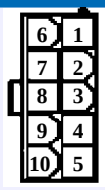
19.1.1 ATX Connector Version

This power connector is available through Connector X7 (10 pins). To find the location of this connector see Appendix E: Connector Layout.

The EPIC/CE requires +5V and +5V Standby. The +3.3V for the EPIC/CE's circuitry is generated onboard. The onboard generated +3.3V is not connected to the PC/104-Plus bus.

Additionally, some peripherals such as LCD panel backlight inverters, disk drives, and PC/104 as well as PC/104-Plus add-on cards may need more voltages (+12V, -12V, +3.3V). These voltages are not generated onboard the EPIC/CE and need to be supplied, too, as soon as peripheral devices require these voltages. We recommend that you use an ATX power supply with this type of EPIC/CE, even though not all voltages are required. An adapter cable to connect a standard ATX power supply to this connector is available from Kontron (KAB-ATX-20TO10, Part Number 96072-0000-00-0).

The following table shows the pin-out of the ATX connector.

Header	Pin	Signal Name	Function	Pin	Signal Name	Function
	1	PS_ON (**)	Power On	6	+5V_SB (*)	5V Standby
	2	GND	Ground	7	+5V (*)	+5V
	3	GND	Ground	8	+5V (*)	+5V
	4	+12V (*)	+12V	9	-12V (*)	-12V
	5	+3.3V (*)	+3.3V external (PC/104-Plus)	10	GND	Ground

Notes: *(*) To protect the external power lines of peripheral devices, make sure that:*
-- the wires have the right diameter to withstand the maximum available current
-- the enclosure of the peripheral device fulfils the fire-protecting requirements of
-- IEC/EN 60950.
The current on these pins is limited to 6A/pin.

(**) As an exception to the ATX specification, the EPIC/CE starts by switching on the primary supply voltage of the ATX power supply (auto start after power fail).

19.1.2 +5V-only Power Supply on ATX connector

If you intend to use a +5V-only power supply on the board equipped with the ATX connector, connect the +5V of the power supply to Pins 6, 7 and 8 (+5V and +5V_SB) and the Ground of the power supply to Pins 2, 3 and 10 (GND) of Connector X7. Leave all other pins (PS_ON included) unconnected. Peripherals requiring other voltages need to be supplied separately.

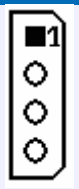
19.1.3 AT Connector Version

This power interface is an option to the ATX power interface and uses Connector X8 (4 pins). For the location of this connector see Appendix E: Connector Layout.

The EPIC/CE requires +5V-only. The +3.3V for onboard low-power devices is generated onboard by a DC/DC converter. Peripherals requiring +3.3V or other voltages need to be supplied separately. Any +3.3V PC/104-Plus add-on card will be affected this way.

Upon request, it is possible to modify the EPIC/CE so that the module can supply the +3.3V for PC/104-Plus devices via the onboard DC/DC converter. However, this modification has a limitation in which add-on PC/104-Plus cards cannot exceed a supply current of 1A (1.5A absolute maximum).

The following table shows the pin-out of the AT connector.

Header	Pin	Signal Description	Function
	1	V5S *	+5V
	2	GND	Ground
	3	GND	Ground
	4	VCC12 *	+12V

Notes: *(*) To protect the external power lines of peripheral devices, make sure that:*
-- the wires have the right diameter to withstand the maximum available current
-- the enclosure of the peripheral device fulfils the fire-protecting requirements of
-- IEC/EN 60950.
The current of the pins on this connector is limited to 13A/pin.

Warning: EPIC-CE in 5V-only version supply the +3.3V to the PC/104-Plus connector via an onboard DC/DC converter. The DC/DC converter is only capable to supply a maximum of 500mA to +3.3V extension cards. As there is no protection on this +3.3V supply, the user has to make sure not to exceed this value with his PC/104-Plus add-on cards.

19.1.4 Configuration

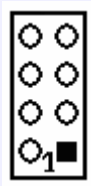
The EPIC/CE comes with a power-management system that supports APM 1.2 and ACPI 2.0 features. You can configure lots of options for power-saving states such as standby state with partial power reduction and suspend state with full-power reduction. Please refer to the Power menu section in the Appendix B: BIOS Operation chapter for more information on saving power.

19.2 ATX/Reset/2LED Interface

This interface on the EPIC/CE is an 8-pin female (Connector X6). For the location of this connector see Appendix E: Connector Layout. The interface's functions include:

- Power Button
- Reset Button
- Hard Disk LED
- CompactFlash LED

The following table shows the pin-out of the connector.

Header	Pin	Signal Description	Function
	1	HDLED *	Hard Disk LED (cathode)
	2	CFLED *	CompactFlash LED (cathode)
	3	VCC	+5V (anode)
	4	VCC	+5V (anode)
	5	/RESIN	Reset Input (low active)
	6	GND	Ground
	7	/PWRBTN	Power Button (low active)
	8	GND	Ground

Notes: *(*) This signal has an onboard 470 Ohm resistor. Directly connect the cathode of the LED to HDLED/CFLED and the anode to VCC.*

19.2.1 Configuration

The function of the power button can be set to either "power off" or "sleep" mode from the BIOS set-up utility. When set to "power off" the power button offers an On/Off function and when set to "Sleep" it offers a Sleep/Wake function. Please refer to the Power menu section in the Appendix B: BIOS Operation chapter for more information about power savings.

20 Watchdog Timer

The watchdog timer (WDT) is integrated in the Winbond W83627HF controller of the EPIC/CE and can issue a reset to the system or generate a non-maskable interrupt (NMI). The watchdog timer circuit has to be triggered within a specified time by the application software. If the watchdog timer is not triggered because proper software execution fails or a hardware malfunction occurs, it resets the system or generates the NMI.

20.1 Configuration

You can set the watchdog timer to disabled, reset or NMI mode. You can specify the delay time and the timeout (trigger period) from 1 second to 30 minutes. The delay time is the time after first initialization before the trigger period starts. The timeout is the time the watchdog timer has to be triggered within. You can make the initialization settings in the BIOS setup. Refer to the Watchdog Settings Submenu in the Appendix B: BIOS Operation chapter for information on configuration.

20.2 Programming

20.2.1 Initializing the WDT

You can initialize the watchdog timer from the BIOS setup. You also can set up the initialization from the application software with help of the JIDA (Jumptec Intelligent Device Architecture) programmer's interface.

20.2.2 Triggering the WDT

The watchdog timer needs to be triggered out of the application software within a specified timeout period. You can only do this in the application software with the help of the JIDA programmer's interface.

For information about the JIDA programmer's interface, refer to the JIDA BIOS extension section in the Appendix B: BIOS chapter and separate documents that are available in the JIDA software packages on the Kontron Web site.

21 Hardware Monitor

The Winbond W83627HF controller monitors several critical hardware parameters of the system, including power-supply voltages, fan speed and CPU temperature, which are very important for a high-end computer system to remain stable and function properly. This controller is connected via the SM (System Management) bus to the south bridge.

The following parameters are monitored:

- +3.3V from onboard DC/DC
- CPU core voltage
- +5V standby voltage
- Battery voltage
- CPU temperature with on-die diode
- CPU fan speed (planed)

21.1 Configuration

You can use the Hardware Monitor submenu in the BIOS Setup Utility to obtain information on voltages, fan speed and to check the temperature of the CPU die. For more information on this submenu, see the Appendix B: BIOS Operation chapter in this manual.

To monitor the parameters of this feature from your operating system, Kontron recommends that you use the 32-bit protected mode JUMP*tec*'s Intelligent Device Architecture driver (JIDA 32) with the test and demo application for Windows 95/98/ME/NT/2000/XP, which is available on the KONTRON Web site.

22 Important Technology Information

The following information will give the reader a better understanding of some of the features offered by the EPIC/CE. This information can be referenced when reading the Appendix A: System Resource Allocations and Appendix B: BIOS Operation sections that follow. There also are references to additional documentation that will help to develop a better understanding of the technical information. They are listed in the Appendix F: PC-Architecture Information.

22.1 Thermal Control

22.1.1 Thermal Management

The Thermal Management feature of the EPIC/CE helps control the processor's temperature by activating the automatic thermal throttling after the processor silicon reaches a certain temperature. This feature can be enabled and configured in the BIOS Setup utility. You can specify the temperature level when throttling starts, define a hysteresis value to get back to 100% CPU performance, and specify the percentage for CPU performance in throttling mode. Automatic thermal throttling mode does not require additional hardware, software drivers, or interrupt-handling routines.

This feature should be used with none ACPI-aware operating systems.

22.1.2 ACPI Thermal Management

ACPI allows the OS to play a role in thermal management. With the OS in control of the operating environment, cooling decisions can be made based on the application load on the CPU and the thermal heuristics of the system. This feature should be used with ACPI-aware operating systems. The ACPI thermal solution on EPIC/CE supports three cooling policies and their trip points, including:

Active Trip Point

Active cooling devices typically consume power and produce noise but are able to cool a thermal zone without limiting system performance. The active cooling trip point declares the temperature threshold that the OS uses to start/stop active cooling devices such as the fan.

Passive Cooling Trip Point

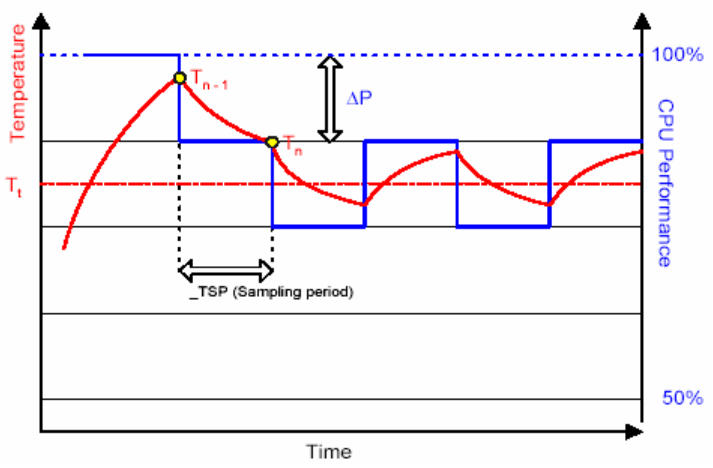
Passive cooling devices produce no noise but may not be effective enough to cool the thermal zone. The passive cooling trip point declares the temperature threshold in which the OS will start or stop passive cooling. In this case, it throttles the processor.

Critical Trip Point

The OS performs an orderly but critical shutdown of the system when the temperature reaches a critical trip point.

22.1.3 Processor Clock Throttling

The ACPI OS assesses the optimum CPU performance change necessary to lower the temperature using the following equation:



$$\Delta P[\%] = TC1\,(T_n - T_{n-1}) + TC2\,(T_n - T_t)$$

ΔP is the performance delta, T_t is the target temperature = critical trip point. The two coefficients TC1 and TC2 and the sampling period TSP are hardware-dependent constants that the end user must supply. (See the setup options in the ACPI Control submenu of the BIOS Operation chapter).

You can control the cooling preference of the system by setting the appropriate trip points in the BIOS setup.

Notes: *For more information, see Chapter 12 of the ACPI Specification.*

22.2 I/O APIC vs. 8259 PIC Interrupt mode

The I/O APIC (Advanced Programmable Interrupt Controller) handles interrupts differently than the 8259 PIC. Enable the I/O APIC mode in the BIOS Setup Utility, if your operating system supports it.

Notes: *The APIC is not supported by all operating systems. Only Windows XP supports APIC.*
Enable the APIC mode in the BIOS setup before the OS installation.
APIC only works in ACPI mode. For more detailed information about APIC, see:
Chapter 8 of the IA-32 Intel Architecture Software Developer's Manual, Volume 3.

The following information explains these differences to the standard 8259 PIC mode:

Method of interrupts transmission

The I/O APIC transmits interrupts through the system bus. Interrupts are handled without the need for the processor to run an interrupt-acknowledge cycle.

Interrupt priority

The priority of interrupts in the I/O APIC is independent of the interrupt number.

More interrupts

The I/O APIC in the chipset of the EPIC/CE supports a total of 24 interrupts.

22.3 Native vs. Compatible IDE mode

22.3.1 Compatible IDE Mode

The ATA controller emulates a legacy IDE controller, which is a non-standard extension of the ISA-based IDE controller. In compatible mode, the controller requires two ISA IRQs (14 and 15) that cannot be shared with other devices.

22.3.2 Native Mode

The ATA controller acts as a true PCI device that does not require dedicated legacy resources and can be configured anywhere in the system. ATA controllers running in native mode use their PCI interrupt for both channels and can share this interrupt pin with other devices in the system, like any other PCI device.

By requiring only one shareable interrupt instead of two non-shareable ones, native-mode controllers significantly decrease the likelihood that a user will install a device that cannot work because no interrupts are available.

Enable Native IDE Support in the BIOS Setup Utility if your OS supports this mode.

Notes: *The Native Mode is not supported by all operating systems. The Native mode must be enabled in the BIOS setup before the OS installation. Native Mode only works in ACPI mode.*
For more information see: Microsoft Windows platform design notes about Native-mode ATA.

22.3.3 Native Mode Configuration

Windows XP SP1 and Windows Server 2003 switch a native-mode-capable ATA controller from compatible to native mode if the BIOS indicates that the controller can be switched, the controller supports native mode, and the appropriate registry entry is set.

You must add a DWORD VALUE called **EnableNativeModeATA** under

`HKEY_LOCAL_MACHINE/System/CurrentControlSet/Control/PnP/PCI/`

and set 1 as the value.

23 Appendix A: System-Resource Allocation

23.1 Interrupt Request (IRQ) Lines

In 8259 PIC mode with I/O APIC mode disabled:

IRQ #	Use	Available	Comment
0	Timer0	No	
1	Keyboard	No	
2	Slave 8259	No	
3	COM2	No	Note (1)
4	COM1	No	Note (1)
5	Sound	No	Note (1), Note (2), Note (4)
6	FDC	No	Note (1)
7	LPT1	No	Note (1)
8	RTC	No	
9	SCI	Yes	Note (3)
10	COM4	No	Note (1)
11	COM3	No	Note (1)
12	PS/2 Mouse	No	Note (1)
13	FPU	No	
14	IDE0	No	Note (1)
15	CompactFlash IDE1	No	Note (1)

Notes: *(1) If the „used for"-device is disabled in setup, the corresponding interrupt is available for other devices.*

(2) Possible setting for LPT1. IRQ7 is the default setting.

(3) Available in default configuration. IRQ 9 is used as SCI, if ACPI is enabled.

(4) Used in Soundblaster compatibility mode.

In I/O APIC mode:

IRQ #	Use	Available	Comment
0	Timer0	No	
1	Keyboard	No	
2	Slave 8259	No	
3	COM2	No	Note (1)
4	COM1	No	Note (1)
5	Sound	No	Note (1), Note (2), Note (4)
6	FDC	No	Note (1)
7	LPT1	No	Note (1)
8	RTC	No	
9	SCI	No	Note (3)
10	COM4	No	Note (1)
11	COM3	No	Note (1)
12	PS/2 Mouse	No	Note (1)
13	FPU	No	
14	IDE0	No	Note (1), Note (5)
15	CompactFlash IDE1	No	Note (1), Note (5)
16	PIRQ[A]	For PCI	
17	PIRQ[B]	For PCI	
18	PIRQ[C]	For PCI	
19	PIRQ[D]	For PCI	
20	PIRQ[E]	No	
21	PIRQ[F]	No	
22	PIRQ[G]	No	
23	PIRQ[H]	No	

Notes: *(1) If the „used for"-device is disabled in setup, the corresponding interrupt is available for other devices.*
(2) Possible setting for LPT1. IRQ7 is the default setting.
(3) Available in default configuration. IRQ 9 is used as SCI, if ACPI is enabled.
(4) Used in Soundblaster compatibility mode.
(5) Available if IDE controller is in Native Mode.

23.2 Direct Memory Access (DMA) Channels

DMA #	Use	Available	Comment
0		Yes	
1	Sound	No	Note (1), (2)
2	FDC	No	Note (1)
3	LPT	Yes	Note (2)
4	Cascade	No	
5		Yes	
6		Yes	
7		Yes	

Notes: *(1) If the „used for"-device is disabled in setup, the corresponding DMA channel is available for other devices.*
(2) Possible setting for LPT1 if configured for ECP mode.

23.3 Memory Map

EPIC/CE processor modules can support up to 512MB of memory. The first 640KB of SDRAM are used as main memory.
Using DOS, you can address 1MB of memory directly. Memory area above 1MB (high memory, extended memory) is accessed under DOS via special drivers such as HIMEM.SYS and EMM386.EXE, which are part of the operating system. Please refer to the operating system documentation or special textbooks for information about HIMEM.SYS and EMM386.EXE.
Other operating systems (Linux or Windows versions) allow you to address the full memory area directly.

Upper Memory	Use	Available	Comment
A0000h – BFFFFh	VGA Memory	No	Mainly used by graphic adapter cards. If a PCI graphic card is in the system this memory area is mapped to the PCI bus.
C0000h – CFFFFh	VGA BIOS, RPL/PXE ROM	No	
D0000h – DFFFFh		Yes	Free for ISA bus or shadow RAM in standard configurations. If JRC software is used, a 16K block is shadowed for BIOS extension, starting with first free area at D0000h, D4000h, D8000hor DC000h. (BIOS extensions do not use the whole shadow block.).
E0000h – F0000h	System BIOS, USB legacy support	No	

23.3.1 Using Expanded Memory Managers

EPIC/CE extension BIOSes can be mapped to an upper memory area. (See the previous table.) Some add-on boards also have optional ROMs or use drivers that communicate with their corresponding devices via memory mapped I/O such as dual-ported RAM. These boards have to share the upper memory area with the Expanded Memory Manager's EMS frame. This often causes several problems in the system.

Most EMMs scan the upper memory area for extension BIOSes (optional ROMs) and choose a free memory area for their frame if it is not explicitly set. Normally, they are not always capable of detecting special memory-mapped I/O areas. You need to tell the EMM which memory areas are not available for the EMS frames, which is most of the time done by using special exclusion parameters.

If the Expanded Memory Manager you use cannot detect extension BIOSes (optional ROMs), make sure you excluded all areas in the upper memory, which are used by extension BIOSes, too. Your instruction in the CONFIG.SYS concerning the Expanded Memory Manager should look like this: (question marks for location of extension BIOS).

MS-DOS Example

```
DEVICE=EMM386.EXE X=????-???? X=E000-FFFF
```

Note: *When booting up your system using this configuration under MS-DOS, the exclusion of area F000 to FFFF causes a warning. Microsoft reports that this message will always appear when the F000 segment lies in the shadow RAM. This is a bug of EMM386, not of the EPIC/CE.*

Please read the technical manuals of add-on cards used with the EPIC/CE for the memory areas they use. If necessary, also exclude their memory locations to avoid a conflict with EMM386.

23.4 I/O Address Map

The I/O-port addresses of the EPIC/CE are functionally identical with a standard PC/AT. All addresses not mentioned in this table should be available. We recommend that you do not use I/O addresses below 0110hex with additional hardware for compatibility reasons, even if available.

Address (h)	Use	Available	Comment
0000 - 001F	DMA Controller 1	No	Fixed
0020 - 003D	Interrupt Controller 1	No	Fixed
002E - 002F	LPC Super I/O	No	Fixed
0040 - 0053	Timer, Counter	No	Fixed
004E - 004F	LPC Super I/O	No	Fixed
0060 - 0067	Keyboard controller	No	Fixed
0070 - 0077	RTC and CMOS Registers	No	Fixed
0080 - 008F	DMA Page Register	No	Fixed
0090 - 009F	DMA Control	No	Fixed
0092	Reset Generator	No	Fixed
00A0 00BF	Interrupt Controller 2	No	Fixed
00C0 - 00DF	DMA Controller 2	No	Fixed
00F0	Math. Coprocessor	No	Fixed
0100 - 010F	General Purpose I/O	No	Kontron Control Port, Fixed
0170 - 0177	Hard Disk Drive (Secondary)	No	Available if IDE port 2 is disabled or in native IDE mode
01F0 - 01F7	Hard Disk Drive (Primary)	No	Available if IDE port 1 is disabled or in native IDE mode
0200 - 026F	Sound	No	Fixed
0274 - 0277	ISA PNP Data	No	Fixed
0278 - 027F	LPT	Yes	Possible address for LPT
0280 - 028F	2nd LPC Super I/O	No	Fixed
02E8 - 02EF	COM4	No	Available if COM is disabled
02F8 - 02FF	COM2	No	Available if COM is disabled
0376	IDE Controller 2	No	Available if IDE port 2 is disabled or in native IDE mode
0378 - 037F	LPT	No	Available if LPT is disabled
03BC - 03C3	LPT	Yes	Possible address for LPT
03B0 - 03DF	Graphic Subsystem	No	Fixed
03E8 - 03EF	COM3	No	Available if COM is disabled
03F0 - 03F7	Floppy Controller	No	Available if floppy controller is disabled
03F6	IDE Controller 1	No	Available if IDE port 1 is disabled or in native IDE mode
03F8 - 03FF	COM1	No	Available if COM is disabled
04D0 - 04D1	Interrupt Select	No	Fixed
0800 - 080F	System Resources	No	Fixed
0A79	ISA PNP Data	No	Fixed
0CF8 - 0CFF	PCI Configuration	No	Fixed
1000 - 107F	System Resources	No	Fixed
1180 - 11BF	System Resources	No	Fixed
1400 - 147F	System Resources Sound	No	Available if sound is disabled
1454	System Resources	No	Fixed
14D4	System Resources	No	Fixed
1500 - 157F	System Resources	No	Fixed
1800 - 181F	USB Host Controller 1	No	Dynamic (address if all PCI onboard devices are on)
1C00 - 1C1F	USB Host Controller 2	No	Dynamic (address if all PCI onboard devices are on)
2000 - 201F	USB Host Controller 3	No	Dynamic (address if all PCI onboard devices are on)
2400 - 240F	Ultra ATA Controller	No	Dynamic (address if all PCI onboard devices are on)
2800 - 281F	SM-Bus Controller	No	Dynamic (address if all PCI onboard devices are on)
2C00 - 2C3F	Sound	No	Dynamic (address if all PCI onboard devices are on)
3000 - 307F	Sound	No	Dynamic (address if all PCI onboard devices are on)
3400 - 343F	System Resources	Yes	Used under some 32 bit operating systems
4000 - 40FF	Ethernet Contr. DM9102	No	Dynamic (address if all PCI onboard devices are on)
4400 - 443F	Ethernet Contr. Intel	No	Dynamic (address if all PCI onboard devices are on)

23.5 Peripheral Component Interconnect (PCI) Devices

All devices follow the PCI 2.1 specification. The BIOS and OS control memory and I/O resources. Please refer to the PCI 2.1 specification for details.

PCI Device (IDSEL)	PCI IRQ	REQ/ GNT	Comment
AGP Graphic	-	-	Separate bus, integrated in Intel chipset
Intel Ethernet (AD24)	INTE#	Discrete channel	
Davicom Ethernet (AD17	INTD#	REQ#3/GNT#3	PC/104-Plus allows 3 external masters REQ#0, REQ#1 and REQ#2
AC97 Sound	INTB#		Separate bus, integrated in Intel chipset
1st UHCI USB Controller	INTA#	-	Separate bus, integrated in Intel chipset
2nd UHCI USB Controller	INTD#	-	Separate bus, integrated in Intel chipset
3rd UHCI USB Controller	INTC#	-	Separate bus, integrated in Intel chipset
EHCI USB Controller	INTH#		Separate bus, integrated in Intel chipset

23.6 SM Bus Devices

The EPIC/CE uses an onboard SM (System Management) Bus. This bus is available on the JFLEX-extension connector. Look at the JFLEX specification, which is available on the Kontron Web site, for signal location.

The following SM Bus addresses are already used on the EPIC/CE.

SM Bus Address	SM Device	Comment
10h/11h	SM-Bus Host	Integrated in Intel ICH4
A0h/A1h	SPD EEPROM	Part of the DDR SDRAM module
D2h/D3h	Clock Generator	

Note: *Accesses to the onboard SM Bus devices that are not allowed may cause system failures. Problems resulting from this are not under warranty!*

24 Appendix B: BIOS Operation

The EPIC/CE comes with Phoenix BIOS 4.0, Release 6.1, which is located in the onboard Flash EEPROM in compressed from. The device has an 8-bit access. The shadow RAM feature offers faster access (16 bit). You can update the BIOS using a Flash utility. For complete Phoenix BIOS 4.0 information, visit the Phoenix Technologies Web site.

24.1 Determining the BIOS Version

To determine the BIOS version of the EPIC/CE, immediately press the <**Pause/Break**> key on your keyboard as soon as you see the following text display in the upper left corner of your screen:

```
PhoenixBIOS 4.0 Release 6.1
Copyright 1985-2003 Phoenix Technology Ltd.
All Rights Reserved
Kontron(R) BIOS Version <E815R111>
Copyright 2002-2005 Kontron Embedded Modules GmbH
```

Whenever you contact technical support about BIOS issues, providing a BIOS version <E815R???> is especially helpful.

The system BIOS provides additional information about the board's serial number, CPU, and memory information by displaying information similar to the following:

```
S/N: EPA010002

CPU = Mobile Intel(R) Celeron(TM) CPU 733MHz
254M System RAM Passed
256K Cache SRAM Passed
System BIOS shadowed
Video BIOS shadowed

UMB upper limit segment address: E4D4
```

The board's serial number has valuable information for technical support. EPIC/CE serial numbers always start with EP and are followed by a character and six digits. The first three positions represent the lot number (here A01), and the last four digits are the number of the board in that lot (here board number 2).

24.2 Configuring the System BIOS

The Phoenix BIOS setup utility allows you to change system behavior by modifying the BIOS configuration. Setup-utility menus allow you to make changes and turn features on or off.

BIOS setup menus represent those found in most models of the EPIC/CE. The BIOS setup utility for specific models can differ slightly.

Note: *Selecting incorrect values can cause system boot failure. Load setup-default values to recover by pressing <**F9**>.*

Start Phoenix BIOS Setup Utility

To start the Phoenix BIOS Setup Utility, press the **<F2>** key when the following string appears during boot-up.

```
Press <F2> to enter Setup
```

The Main Menu then appears.

24.2.1 General Information

The **Setup Screen** is composed of several sections:

Setup Screen	Location	Function
Menu Bar	Top	Lists and selects all top-level menus.
Legend Bar	Bottom	Lists setup navigation keys.
Item Specific Help Window	Right	Help for selected item.
Menu Window	Left Center	Selection fields for current menu.
General Help Window	Overlay (center)	Help for selected menu.

Menu Bar

The menu bar at the top of the window lists different menus. Use the left/right arrow keys to make a selection.

Legend Bar

Use the keys listed in the legend bar on the bottom to make your selections or exit the current menu. The table below describes the legend keys and their alternates.

Key	Function
<F1> or <Alt-H>	General Help window.
<Esc>	Exit menu.
← or → Arrow key	Select a menu.
↑ or ↓ Arrow key	Select fields in current menu.
<Tab> or <Shift-Tab>	Cycle cursor up and down.
<Home> or <End>	Move cursor to top or bottom of current window.
<PgUp> or <PgDn>	Move cursor to next or previous page.
<F5> or <->	Select previous value for the current field.
<F6> or <+> or <Space>	Select next value for the current field.
<F9>	Load the default configuration values for this menu.
<F10>	Save and exit.
<Enter>	Execute command or select submenu.
<Alt-R>	Refresh screen.

Selecting an Item

Use the ↑ or ↓ key to move the cursor to the field you want. Then use the + and - keys to select a value for that field. **Save Value** commands in the **Exit** menu save the values displayed in all menus.

Displaying Submenus

Use the ← or → key to move the cursor to the submenu you want. Then press **<Enter>**. A pointer (▸) marks all submenus.

Item Specific Help Window

The Help window on the right side of each menu displays the Help text for the selected item. It updates as you move the cursor to each field.

General Help Window

Pressing **<F1>** or **<Alt-F1>** on a menu brings up the General Help window that describes the legend keys and their alternates. Press **<Esc>** to exit the General Help window.

24.3 Main Menu

Feature	Option	Description
System Time	HH:MM:SS	Sets system time. Press <Enter> to move to MM or SS.
System Date	MM/DD/YYYY	Sets system date. Press <Enter> to move to DD or YYYY.
Legacy Diskette A	360 Kb, 5 ¼ " 1.2 MB, 5 ¼ " 720 Kb, 3 ½ " **1.44/1.25 MB, 3 ½ "** 2.88 MB, 3 ½ " Disabled	Select the type of floppy disk drive.
Legacy Diskette B	360 Kb, 5 ¼ " 1.2 MB, 5 ¼ " 720 Kb, 3 ½ " 1.44/1.25 MB, 3 ½ " 2.88 MB, 3 ½ " **Disabled**	Select the type of floppy disk drive.
▸ Primary Master	Autodetected drive	Displays result of PM autotyping.
▸ Primary Slave	Autodetected drive	Displays result of PS autotyping.
▸ Compact Flash	Autodetected drive	Displays result of CF autotyping.
Smart Device Monitoring	Disabled **Enabled**	Turns on Self-Monitoring Analysis-Reporting Technology, which monitors the condition of the hard drive and reports when a catastrophic IDE failure is about to happen.
System Memory	N/A	Displays amount of conventional memory detected during boot-up.
Extended Memory *	N/A	Displays amount of extended memory detected during boot-up.

Notes: *In the Option column, bold shows default settings.*
(*) Extended Memory = capacity of memory module – selected frame buffer memory size (Video boot type).

24.3.1 Master or Slave Submenus

Feature	Option	Description
Type	None User **Auto** CD-ROM IDE Removable ATAPI Removable Other ATAPI	None = Autotyping is not able to supply the drive type or end user has selected None, disabling any drive that may be installed. User = End user supplies HDD information. Auto = Autotyping. The drive itself supplies the information. CD-ROM = CD-ROM drive. ATAPI Removable = Read- and writeable media e.g. LS120 and USB-ZIP Other ATAPI = for ATAPI devices not supported by other HDD features.
Cylinders	1 to 65,536	Number of cylinders.
Heads	1 to 256	Number of read/write heads.
Sectors	1 to 63	Number of sectors per track.
Maximum Capacity	N/A	Displays the calculated size of the drive in CHS.
Total Sectors	N/A	Number of total sectors in LBA mode.
Maximum Capacity	N/A	Displays the calculated size of the drive in LBA.
Multi-Sector Transfer	**Disabled** 2 sectors 4 sectors 8 sectors 16 sectors	Any selection except Disabled determines the number of sectors transferred per block. The standard is one sector per block.
LBA Mode Control	**Disabled** Enabled	Enabling LBA causes Logical Block Addressing to be used in place of CHS.
32-Bit I/O	**Disabled** Enabled	Enables 32-bit communication between CPU and IDE card. Requires PCI or local bus.
Transfer Mode	**Standard** Fast PIO 1 Fast PIO 2 Fast PIO 3 Fast PIO 4 FPIO 3 / DMA 1 FPIO 4 / DMA 2	Selects the method for transferring the data between the hard disk and system memory.
Ultra DMA Mode *	Disabled MOD0 MOD1 MOD2 MOD3 MOD4 MOD5	Selects the UDMA mode to move data to/from the drive. Autotype the drive to select the optimum transfer mode. This feature is autodetected.
SMART Monitoring	Disabled Enabled	Shows whether a disk supports SMART.

Note: *In the Option column, bold shows default settings.*
(*) On the 40 pin IDE interface an 80 line UDMA 100 cable is required for proper operation in modes UDMA 3 and higher.

24.4 Advanced Menu

Feature	Option	Description
▸ Advanced Chipset Control	Sub menu	Opens Advanced Chipset Control sub menu.
▸ PCI/PNP Configuration	Sub menu	Opens PCI/PNP Config sub menu.
▸ Memory Cache	Sub menu	Opens Cache Control sub menu.
▸ I/O Device Configuration	Sub menu	Opens Peripheral Config sub menu.
▸ Keyboard Features	Sub menu	Opens Keyboard Features sub menu.
▸ Hardware Monitor	Sub menu	Shows hardware monitor current state.
▸ Watchdog Settings	Sub menu	Opens Watchdog Config sub menu.
▸ Display Control	Sub menu	Opens Display Control sub menu
▸ Miscellaneous	Sub menu	Opens sub menu with miscellaneous options.

24.4.1 Advanced Chipset Control Submenu

Feature	Option	Description
Video boot type	Disable Onboard Video Onboard Video 512K **Onboard Video 1MB**	Disable Onboard Graphics Device, sets the legacy UMA video memory to 512KByte or 1MB.
Enable Memory gap	**Disabled** Enabled	Allows enabling a 1MB memory gap for add-on cards at 15MB.

Note: *In the Option column, bold shows default settings.*

24.4.2 PCI/PNP Configuration Submenu

Feature	Option	Description
PNP OS installed	No **Yes**	If your system has a PnP OS (such as Win9x), select Yes to let the OS configure PnP devices not required for booting. No allows the BIOS to configure them.
Reset Configuration Data *	**No** Yes	Yes erases all configuration data in ESCD, which stores the configuration settings for plug-in devices. Select Yes when required to restore the manufacturer's defaults.
Secured Setup Configuration	**Yes** No	Yes prevents a Plug and Play OS from changing system settings.
▸ PCI Device, Slot #x	Sub menu	Opens sub menu to configure slot x PCI device.
PCI IRQ line 1 PCI IRQ line 2 PCI IRQ line 3 PCI IRQ line 4 Onboard LAN IRQ line Onboard USB EHCI IRQ line	Disabled **Auto Select** IRQ3, 4, 5, 7, 9, 10, 11, 12, 14,15	Select IRQs for external PIC interrupts A/B/C/D and the onboard Davicom LAN and USB2.0 host controller. Select Auto to let the BIOS assign the IRQ.
▸ PCI/PNP ISA IRQ Resource Exclusion	Sub menu	Opens IRQ Exclusion sub menu.

Notes: *In the Option column, bold shows default settings.*
(*) Setting this option to "yes", under certain circumstances, may help recovery from a system boot failure or a resource conflict.

24.4.3 PCI Device, Slot #x Submenu

Feature	Option	Description
Option ROM Scan	Disabled **Enabled**	Initialize device expansion ROM.
Enable Master	**Disabled** Enabled	Enables device in slot as a PCI bus master, not every device can function as a master. Check device documentation.
Latency Timer	**Default**, 20h, 40h, 60h, 80h, A0h, C0h, E0h	Minimum guaranteed time slice allocated for bus master in units of PCI bus clocks. A high-priority, high-throughput device may benefit from a greater value.

Note: *In the Option column, bold shows default settings.*

24.4.4 PCI/PNP ISA IRQ Resource Exclusion Submenu

Feature	Option	Description
IRQ3	**Available** Reserved	Reserves the specified IRQ for use by legacy ISA devices.
IRQ4	**Available** Reserved	See above.
IRQ5	**Available** Reserved	See above.
IRQ7	**Available** Reserved	See above.
IRQ9 *	**Available** Reserved	See above.
IRQ10	**Available** Reserved	See above.
IRQ11	**Available** Reserved	See above.
IRQ12	**Available** Reserved	See above.
IRQ14 **	**Available** Reserved	See above.
IRQ15 **	**Available** Reserved	See above.

Notes: *In the Option column, bold shows default settings.*
(*) IRQ9 is used for SCI in ACPI mode. Do not use IRQ9 for legacy ISA devices when ACPI enabled.
(**) Entry is only visible when primary IDE or secondary IDE is disabled.

24.4.5 Memory Cache Submenu

Feature	Option	Description
Memory Cache	Disabled **Enabled**	Enables or Disables L2 cache.
Cache System BIOS area	Uncached **Write Protect**	Controls caching of System BIOS area.
Cache Video BIOS area	Uncached **Write Protect**	Controls caching of Video BIOS area.
Cache Base 0-512K	Uncached Write Through Write Protected **Write Back**	Controls caching of base memory up to 512KB.
Cache Extended Memory area	Uncached Write Through Write Protected **Write Back**	Controls caching of system memory above 1MB.
D000 - D3FF D400 - D7FF D800 - DBFF DC00 - DFFF	**Disabled** Write Through Write Protected Write Back	Disabled: block is not cached. Write Through: Write are cached and sent to main memory at once. Write Protect: Writes are ignored. Write Back: Writes are cached but not sent to main memory until necessary.

Note: *In the Option column, bold shows default settings.*

24.4.6 I/O Device Configuration Submenu

Feature	Option	Description
Local Bus IDE adapter	Disabled, Primary, Secondary **Both**	Enables onboard PCI IDE device.
Primary IDE UDMA66/100	**Enabled** Disabled	Disabled limits maximum transfer rate to UDMA33. Enabled allows UDMA66 and UDMA100
Secondary IDE UDMA66/100	**Enabled *** Disabled	Disabled limits maximum transfer rate to UDMA33. Enabled allows UDMA66 and UDMA100
USB UHCI Host Controller 1	**Enabled** Disabled	Enable / Disable UHCI 1 Host Controller for USB ports 0 and 1 (EPIC front).
USB UHCI Host Controller 2	**Enabled** Disabled	Enable / Disable UHCI 2 Host Controller for USB ports 2 and 3 (EPIC front).
USB UHCI Host Controller 3	**Enabled** Disabled	Enable / Disable UHCI 3 Host Controller for USB ports 4 and 5 (internal).
USB EHCI Host Controller **	**Enabled** Disabled	Controls USB 2.0 functionality.
Legacy USB Support ***	**Enabled** Disabled	Enable support for USB keyboard and mice and boot from USB mass storage devices.
AC97 Audio Controller	**Enabled** Disabled	Enable/Disable the AC97 Audio device.
Onboard LAN Controller 1	Disabled **Enabled**	Enables the ICH4 internal LAN controller.
Onboard LAN PXE ROM	**Disabled** Enabled	Enables the remote boot BIOS extension for the onboard LAN controller 1.
Onboard LAN Controller 2	Disabled **Enabled**	Enables the Davicom LAN controller.
Floppy disk controller	Disabled **Enabled**	Enable / Disable the onboard FDC controller.
Serial port A, B, C, D	Disabled Enabled **Auto**	Disabled turns off the port. Enabled requires end user to enter the base I/O address and the IRQ. Auto makes the BIOS configure the port. Serial port A is available on the EPIC front. The other ports are available on internal connectors.
Base I/O address	3F8h, 2F8h, 3E8h, 2E8h	Select I/O base of port.
IRQ (port A and B)	IRQ 3, IRQ 4	Select IRQ of Port A and B
IRQ (port C and D)	IRQ10, IRQ11	Select IRQ of Port C and D
Interface	**RS232**, RS485	Set the mode for Serial Port D.
Parallel Port	Disabled Enabled **Auto**	Disabled turns off the port. Enabled requires end user to enter the base I/O address and the IRQ. Auto makes the BIOS configure the port.
Mode	Output only, **bi-directional,** EPP, ECP	Set the mode for the parallel port.
Base I/O address	**378h**, 278h, 3BCh	Select I/O base of port.
IRQ	IRQ 5, **IRQ 7**	Select IRQ of parallel port.
DMA	DMA1, **DMA3**	Select DMA channel of port if in ECP mode.

Notes: *In the Option column, bold shows default settings.*

(*) If you are not using a 80 line UDMA cable on the IDE interface set this entry to disabled.

(**) The USB ports are multiplexed between UHCI and EHCI. Ports are routed to EHCI if an USB 2.0 high-speed device is connected and an EHCI driver is loaded.

(***) If you want to use the USB boot feature, enable USB BIOS Legacy Support. A 16kb UMB area (most likely DC000h-DFFFFh) is used for USB BIOS Legacy Support.

24.4.7 Keyboard Features Submenu

Feature	Option	Description
Numlock	Auto **On** Off	On or Off turns NumLock on or off at boot-up. Auto turns NumLock on if it finds a numeric key pad.
Key Click	**Disabled** Enabled	Turns audible key click on.
Keyboard auto-repeat rate	**30/sec**, 26.7/sec, 21.8/sec, 18,5/sec, 13.3/sec, 10/sec, 6/sec, 2/sec	Sets the number of times to repeat a keystroke per second if you hold the key down.
Keyboard auto-repeat delay	¼ sec, **½ sec**, ¾ sec, 1 sec	Sets the delay time after the key is held down before it begins to repeat the keystroke.

Note: *In the Option column, bold shows default settings.*

24.4.8 Hardware Monitor Submenu

This submenu shows the current voltages, temperatures and the fan speed of the system.

Voltage/Temperature/Fan	Explanation
VCC 3.3V Voltage	3.3V power plane
CPU Core Voltage	CPU core voltage
5Vsb Voltage	5V-Standby voltage
Battery Voltage	Battery voltage
CPU Temperature	CPU Temperature in °C and °F
CPU Fan Speed (not available until BIOS revision E815R111)	CPU fan speed in rpm, "no function" will be displayed on boards with passive cooling

24.4.9 Watchdog Timer Settings Submenu

Feature	Option	Description
Mode	**Disabled** Reset NMI	Select watchdog-timer operation mode.
Delay	1s, 5s, 10s, **30s**, 1min, 5.5min, 10.5min, 30.5min	The time until the watchdog timer counter starts counting. Useful to handle longer boot times.
Timeout	1s, 5s, 10s, **30s**, 1min, 5.5min, 10.5min, 30.5min	Max. trigger period.

Note: *In the Option column, bold shows default settings.*

24.4.10 Display Control Submenu

Feature	Option	Description
Display Mode	CRT only LCD only **CRT+LCD**	Select display mode.
JDA Revision	x.x	Displays the revision of the JILI data area image.
Flat Panel Type	VGA * SVGA * XGA * XGA2 * SXGA * Enter PAID Enter FPID **Auto**	Select Auto to let the BIOS automatically detect the panel type or use one of the predefined fixed panel types. Choose Enter PAID or Enter FPID to manually set JILI3 ID values.
PAID/FPID **	0 – FFFF, default **0**	Enter the JILI3 ID.
Flat Panel Backlight ***	0 – 255, default **128**	Enter a value to adjust backlight of the LCD.
Flat Panel Contrast ****	0 – 63, default **32**	Enter a value to adjust contrast of the LCD.

Note: *In the Option column, bold shows default settings.*

(*) Standard timings for VGA to SXGA panels cannot drive all available displays of that type that are on the market. Use a JILI cable when ever possible.

(**) Only visible if Enter PAID or Enter FPID are selected.

(***) Only visible if the panel adapter is equipped with a MAX5362 DAC for backlight control.

(****) Only visible if the panel adapter is equipped with a Xicore X9429 digital potentiometer for contrast control.

24.4.11 Miscellaneous Submenu

Feature	Option	Description
Floppy Check	**Disabled** Enabled	Enabled verifies floppy type on boot; disabled speeds boot.
Summary Screen	**Disabled** Enabled	If enabled, a summary screen is displayed just before booting the OS to let the end user see the system configuration.
QuickBoot Mode	Disabled **Enabled**	Allows the system to skip certain tests while booting. This decreases the time needed to boot the system.
Extended Memory Testing	Normal * **Just zero it** None	Determines which type of tests will be performed on memory above 1MB.
Dark Boot	**Disabled** Enabled	If enabled, system comes up with a blank screen instead of the diagnostic screen during boot-up.
Halt On Errors	**Yes** No	Determines if post errors cause the system to halt.
PS/2 Mouse	**Auto Detect** Enabled Disabled	Selecting Disabled prevents any installed PS/2 mouse from functioning but frees up IRQ12. Selecting Autodetect frees IRQ12 if no mouse is detected.
Large Disk Access Mode	**DOS** Other	Select DOS if you have DOS. Select Other if you have another OS such as UNIX. A large disk is one that has more than 1024 cylinders, more than 16 heads or more than 63 sectors per track.

Note: *In the Option column, bold shows default settings.*
(*) *The option normal is not visible when QuickBoot is enabled.*

Dark Boot

After you turn on or reset the computer, Dark Boot displays a graphical logo (default is a blank screen) instead of the text based POST screen, which displays a number of PC diagnostic messages.

The graphical logo stays up until just before the OS loads unless:

- You press <Esc> to display the POST screen
- You press <F2> to enter Setup
- POST issues an error message
- The BIOS or an option ROM requests keyboard input

24.5 Security Menu

Feature	Option	Description
Supervisor Password is	**Clear** Set	Displays whether password is set.
User Password is	**Clear** Set	Displays whether password is set.
Set User Password *	Up to seven alphanumeric characters	Pressing <Enter> displays the dialog box for entering the user password. In related systems, this password gives restricted access to setup.
Set Supervisor Password *	Up to seven alphanumeric characters	Pressing <Enter> displays the dialog box for entering the user password. In related systems, this password gives full access to setup.
Diskette access	User **Supervisor**	Enabled requires supervisor password to access floppy disk.
Fixed disk boot sector	**Normal** Write protected	Write protect the boot sector on the hard disk for virus protection. Requires a password to format or Fdisk the hard disk.
Virus check reminder	**Disabled** Daily Weekly Monthly	Displays a message during boot-up asking (Y/N) if you backed up the system or scanned for viruses. Message returns on each boot until you respond with Y. Daily displays the message on the first boot of the day, Weekly on the first boot after Sunday, and monthly on the first boot of the month.
System backup reminder	**Disabled** Daily Weekly Monthly	Displays a message during boot-up asking (Y/N) if you backed up the system or scanned for viruses. Message returns on each boot until you respond with Y. Daily displays the message on the first boot of the day, Weekly on the first boot after Sunday, and monthly on the first boot of the month.
Password on boot	**Disabled** Enabled	Enabled requires a password on boot. Requires prior setting of the supervisor password. If supervisor password is set and this option is disabled, BIOS assumes user is booting.

Notes: *In the Option column, bold shows default settings.*

(*) Enabling Supervisor Password requires a password for entering Setup.

Passwords are not case sensitive.

User and Supervisor passwords are related. A User password is possible only if a Supervisor password exists.

24.6 Power Menu

In the BIOS Setup Utility, you can set up an Advance Power Management system (APM 1.2) to reduce the amount of energy used after specified periods of inactivity. The setup menu supports:

- Full On State
- Standby State with Partial Power Reduction
- Suspend State with Full Power Reduction

In addition you can enable an ACPI 1.0 support in the BIOS setup utility, if you intend to use an operating system supporting the Advanced Configuration and Power Management Interface. For logical reasons it is required to use an ATX power supply with the ACPI feature.

The following states are supported from the system:

- S0 (Working)
- S1 (Sleeping with processor context maintained)
- S5 (Soft off)

The state S2 (sleeping with processor context not maintained) and S3 (Save to RAM) is not supported. The state S4 (Save to Disk) is a matter of the used operating system.

24.6.1 ACPI Resume Events

The following events resume the system from S1:

- Power button
- PME#
- PS/2 keyboard and mouse
- USB keyboard and mouse activity
- USB resume event

Feature	Option	Description
Enable ACPI *	No **Yes**	Enables/Disables ACPI BIOS (Advanced Configuration and Power Interface). IRQ9 is used for SCI (System Control Interrupt).
▸ ACPI Control	Sub menu	Opens the ACPI sub menu
▸ Thermal Management **	Sub menu	Opens Thermal Management sub menu.
Power Savings	**Disabled** Customized Maximum Power Savings Maximum Performance	Maximum options select predefined values. Select Customized to make selections from the following fields. Disabled turns off power management.
Hard Disk Timeout	**Disabled**, 10 sec – 15 min	Inactivity period of hard disk required before standby (motor off).
Video Timeout	**Disabled**, 10 sec – 15 min	Inactivity period of user input device before the screen is turned off.
Resume on Modem Ring	**Off** On	Enabled wakes system on incoming calls detected by mode (RI).
Resume on Time	**Off** On	Enabled wakes the system at a specific time.
Resume Time	00:00:00	Specifies time when system wakes.
Power supply	**ATX** AT	Specifies whether an ATX or an AT power supply is used.
Power Button Function	Power Off **Sleep**	Determines if the system enters suspend or soft off when the power button is pressed.
Power Loss Control	Stay Off Power On **Last State**	Determines how the system behaves after a power failure. This only works in conjunction with a CMOS backup battery.

Notes: *In the Option column, bold indicates default setting.*

(*) Disable ACPI support whenever you are using an operating system without ACPI capability.

(**) See the chapter "Important Technology Information of this user's guide for more details about these features.

24.6.2 ACPI Control Submenu

Feature	Option	Description
Active Trip Point *	**Disabled** 40 °C – 100 °C	Determines the temperature of the ACPI Active Trip Point, the point at which the OS will turn on/off the CPU fan.
Passive Trip Point *	**Disabled** 40 °C – 100 °C	Determines the temperature of the ACPI Passive Trip Point, the point at which the OS will turn on/off CPU clock throttling.
Critical Trip Point *	40 °C – **110 °C**	This value controls the temperature of the ACPI Critical Trip Point – the point at which the OS will shut the system off.
APIC – IO APIC Mode *	**Disabled** Enabled	This item is valid only for Windows XP. Also, a fresh install of the OS must occur when APIC Mode is desired. Test the IO APIC by setting an item to Enabled. The APIC Table will then be pointed to by the RSDT, the Local APIC will be initialized, and the proper enable bits will be set in IHC4M. See section 14.1
Native IDE Support *	**Disabled** Enabled	Enable Native IDE support for WINXP by setting this item. The NATA Package will be created if this item is set to Enabled. Changing this item will have no effect in WIN98, WINME, or WIN2K. See section 13.2 for details.

Notes: *In the Option column, bold indicates default setting.*

(*) See the chapter "Important Technology Information of this user's guide for more details about these features.

24.6.3 Thermal Management Submenu

Feature	Option	Description
Auto Thermal Throttling *	**Enabled** Disabled	Enables/Disables the automatic thermal throttling of the processor's clock. If disabled, the other entries are not visible.
Temperature	**100°C** 75 °C – 110 °C	Sets the temperature level at which throttling starts.
Hysteresis	3°C, 4°C, **5 °C**, 6°C	When a level of Temperature – Hysteresis is reached, the throttling stops and 100% CPU performance is available again.
CPU Performance	13%, 25%, **50%,** 75%	Specifies the throttling percentage of the CPU performance.

Notes: *In the Option column, bold indicates default setting.*

(*) See the chapter "Important Technology Information of this user's guide for more details about these features.

24.7 Boot Menu and Utilities

MultiBoot is a boot utility integrated in the PhoenixBIOS 4.0. The EPIC/CE provides the MultiBoot XP version with integrated Boot First function.

24.7.1 MultiBoot XP

MultiBoot XP comes with a complete new look of the Boot Device Priority submenu. This submenu is now separated into two sections:

- Boot Priority Order
- Excluded from Boot Order

It can display the setup menus by each kind of device type and arrange the boot priority order with any sequence of devices. MultiBoot XP meets the requirements of PC 98 and accommodates more devices that are bootable. It employs a boot scheme that is generic and flexible enough to boot from any current device. You can select your boot device in Setup, or you can choose a different device each time you boot by selecting your boot device in the Boot First function.

An available bootable device can be easily switched between the two sections by just highlighting the device and then pressing <X>. To change the order, select the device to change and press <-> to decrease or <+> to increase priority. You also can choose between four default configurations for the boot order <1>-<4>.

Boot Priority Order

This section shows eight configuration entries for up to eight devices that can be arranged in boot priority order (1: highest priority, 8: lowest priority).

Excluded from Boot Order

This section shows all devices that are excluded from the boot order. Any device listed here will never be used as boot device and not appear in the Boot First function.

The following table shows a list of supported devices:

Device	Description
IDE 0	Primary master IDE hard drive
IDE 1	Primary slave IDE hard drive
IDE 2	Secondary master IDE hard drive
IDE 3	Secondary slave IDE hard drive
IDE CD	IDE compatible CD-ROM drive
Legacy Floppy Drives	Standard Legacy Diskette Drive
USB KEY	USB stick
USB FDC	USB Diskette Drive
USB HDD	USB Hard Drive and memory sticks that follow MMS specification
USB CDROM	USB CD-ROM Drive
USB ZIP	USB ZIP Drive
USB LS120	USB LS120 Drive
PCI BEV	Ethernet Controller on the PCI Bus with LAN Boot ROM
PCI SCSI	SCSI Controller on the PCI Bus with SCSI BIOS ROM

24.7.2 Boot First Function

Display the Boot First function by pressing <Esc> during POST. In response, the BIOS displays the message Entering Boot Menu and then displays the Boot Menu at the end of POST. With the MultiBoot XP feature only devices detected during boot-up are displayed.

Use the menu to select a following option:

- Override the existing boot sequence (for this boot only) by selecting another boot device. If the specified device does not load the OS, the BIOS reverts to the previous boot sequence.
- Enter Setup.
- Press <Esc> to continue with the existing boot sequence.

24.8 Exit Menu

The following sections describe the five options in Exit Menu. Pressing <Esc> does not exit this menu. You must select an item from the menu to exit.

Feature	Option	Description
Exit Saving Changes	Saves selections and exits setup. The next time the system boots, the BIOS configures the system according to the Setup selection stored in CMOS.	Exit saving changes.
Exit Discarding Changes	Exits Setup without storing in CMOS any new selections you may have made. The selections previously in effect remain in effect.	Exit discarding changes.
Load Setup Defaults	Displays default values for all the Setup menus.	Load setup defaults.
Discard Changes	If, during a Setup session, you change your mind about changes you have made and have not yet saved the values to CMOS, you can restore the values you saved to CMOS.	Discard changes.
Save Changes	Saves all the selection without exiting Setup. You can return to the other menus to review and change your selection.	Save changes.

24.9 Kontron BIOS Extensions

Besides the Phoenix System BIOS, the EPIC/CE comes with a few BIOS extensions that support special features. All extensions are located in the onboard Flash EEPROM. Some extensions are permanently available; some are loaded if required during boot-up. Supported features include:

- JIDA standard
- Remote Control feature (JRC)
- Onboard LAN RPL ROM

All enabled BIOS extensions require shadow RAM, which is loaded into the same 32K shadowed memory block, if possible. However, if the system memory cannot find free memory space because all the memory is already used for add-on peripherals, the BIOS extensions do not load.

24.9.1 JIDA BIOS extension

The JUMPtec Intelligent Device Architecture (JIDA) BIOS extension is not a true extension BIOS. It is part of the system BIOS and is located in the system BIOS segments after boot-up. It is permanently available and supports the JIDA 16-bit and JIDA 32-bit standard.

The JIDA 16-bit standard is a software interrupt 15hex driven programmers interface and offers lots of board information functions. For detailed information about programming, refer to the JIDA specification and a source code example (JIDAI???.ZIP), which you can find at the Kontron Web site. The three question marks represent the revision number of the file. You also can contact technical support for this file.

For other operating systems, special 32-bit drivers (JIDAIA??.ZIP) are available. You can download the zip file from the Kontron Web site.

24.9.2 Remote Control Client Extension

You can remotely control the EPIC/CE using software available from Kontron (JRC-1, Part Number 96047-0000-00-0). This software tool can communicate with the board via one of the serial ports. During boot-up, the system BIOS scans the serial ports for an available JRC connection. If detected, it loads the JRC client BIOS extension into the memory. With the JRC client loaded into the first detected free memory location between C0000hex and DFFFFhex, a 16K block is shadowed.

For more information on the Remote Control usage, refer to the JRC-1 technical manual or Application Note JRCUsage_E???.PDF, which you can find on the Kontron Web site.

24.9.3 LAN PXE ROM

If the onboard LAN PXE ROM is enabled in the system BIOS setup, a special optional ROM for the Ethernet controller loads into memory during boot-up. This optional ROM allows you to boot the EPIC/CE over an Ethernet connection. A server with Intel PXE boot support is required on the other side of the Ethernet connection. The setup and configuration of the server, including PXE support, is not the responsibility of Kontron.

The PXE ROM extension is loaded into the first free memory area between C0000hex and DFFFFhex and a 16K block of memory is shadowed.

24.10 Updating or Restoring BIOS Using PhoenixPhlash

PhoenixPhlash allows you to update the BIOS by using a floppy disk without having to install a new ROM chip. PhoenixPhlash is a utility used to flash a BIOS to the Flash ROM installed on the EPIC/CE.

Use PhoenixPhlash to:

- Update the current BIOS with a newer version
- Restore a corrupt BIOS

24.10.1 Flashing a BIOS

Use the following procedure to update or restore the BIOS.

➤ Download the Phoenix Phlash compressed file, CRDxE815.ZIP, from the KONTRON Embedded Modules Web site or contact your local technical support for it. The zip file contains the following:

File	Purpose
MAKEBOOT.EXE	Creates the custom boot sector on the Crisis Recovery Diskette.
CRISBOOT.BIN	Serves as the Crisis Recovery boot sector code.
MINIDOS.SYS	Allows the system to boot in Crisis Recovery Mode.
PHLASH16.EXE	Programs the flash ROM.
WINCRIS.EXE	Creates the Crisis Recovery Diskette from Windows.
WINCRIS.HLP	Serves as the help file of WINCRISES.EXE.
CRISDISK.BAT	Batch file for crisis disk.
BIOS.WPH	Serves as the actual BIOS image to be programmed into Flash ROM.

➤ Install Phoenix Phlash on a hard disk by unzipping the contents of the CRDxE815.ZIP into a local directory such as C:\PHLASH.

➤ Create a Crisis Recovery Diskette by inserting a blank diskette into Drive A: or B: and execute WINCRISIS.EXE. This copies three files onto the diskette.

File	Purpose
MINIDOS.SYS	Allows the system to boot in Crisis Recovery Mode.
PHLASH16.EXE	Programs the flash ROM.
BIOS.ROM	Serves as the actual BIOS image to be programmed into Flash ROM.

➤ If the BIOS image (BIOS.ROM) changes because of an update or bug fix, copy the new BIOS onto the diskette and name it BIOS.ROM.

Phoenix Phlash runs in either command line mode or crisis recovery mode.

➤ Use the command line mode to update or replace the BIOS. To execute Phlash in this mode, move to the Crisis Recovery Disk and type:

```
PHLASH16 <bios name>    (Example: PHLASH16 E815R112.WPH)
```

➤ PhoenixPhlash will update the BIOS. PhoenixPhlash can fail if the system uses memory managers. If this occurs, the utility displays the following message:

```
Cannot flash when memory manager are present.
```

➤ If you see this message after you execute Phlash, disable the memory manager or use parameter /x for Phlash16.exe.

```
PHLASH16 /X <bios name>
```

24.10.2 Preventing Problems When Updating or Restoring BIOS

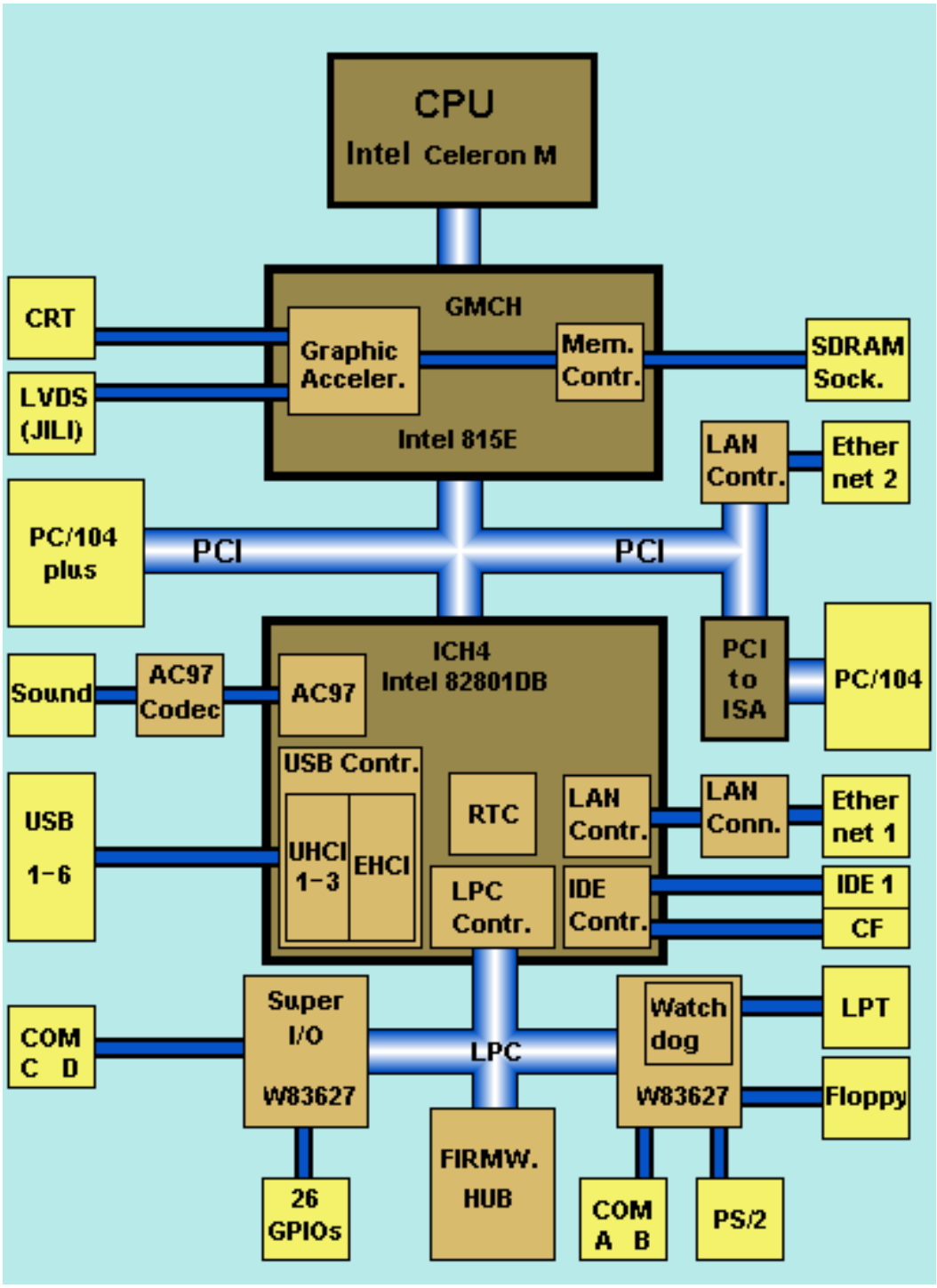
Updating the BIOS represents a potential hazard. Power failures or fluctuations can occur when you update the Flash ROM can damage the BIOS code, making the system unbootable.

To prevent this hazard, many systems come with a boot-block Flash ROM. The boot-block region contains a fail-safe recovery routine. If the boot-block code finds a corrupted BIOS (checksum fails), it boots into the crisis recovery mode and loads a BIOS image from a crisis diskette (see above).

Additionally, the end user can insert an update key into the parallel port (LPT) to force initiating the boot block recovery routine.

For further information on the update key and the crisis diskette, see the Application Note PHLASH_SCE???, which is available from the KONTRON Embedded Modules Web site. The three question marks stand for the revision number of the file.

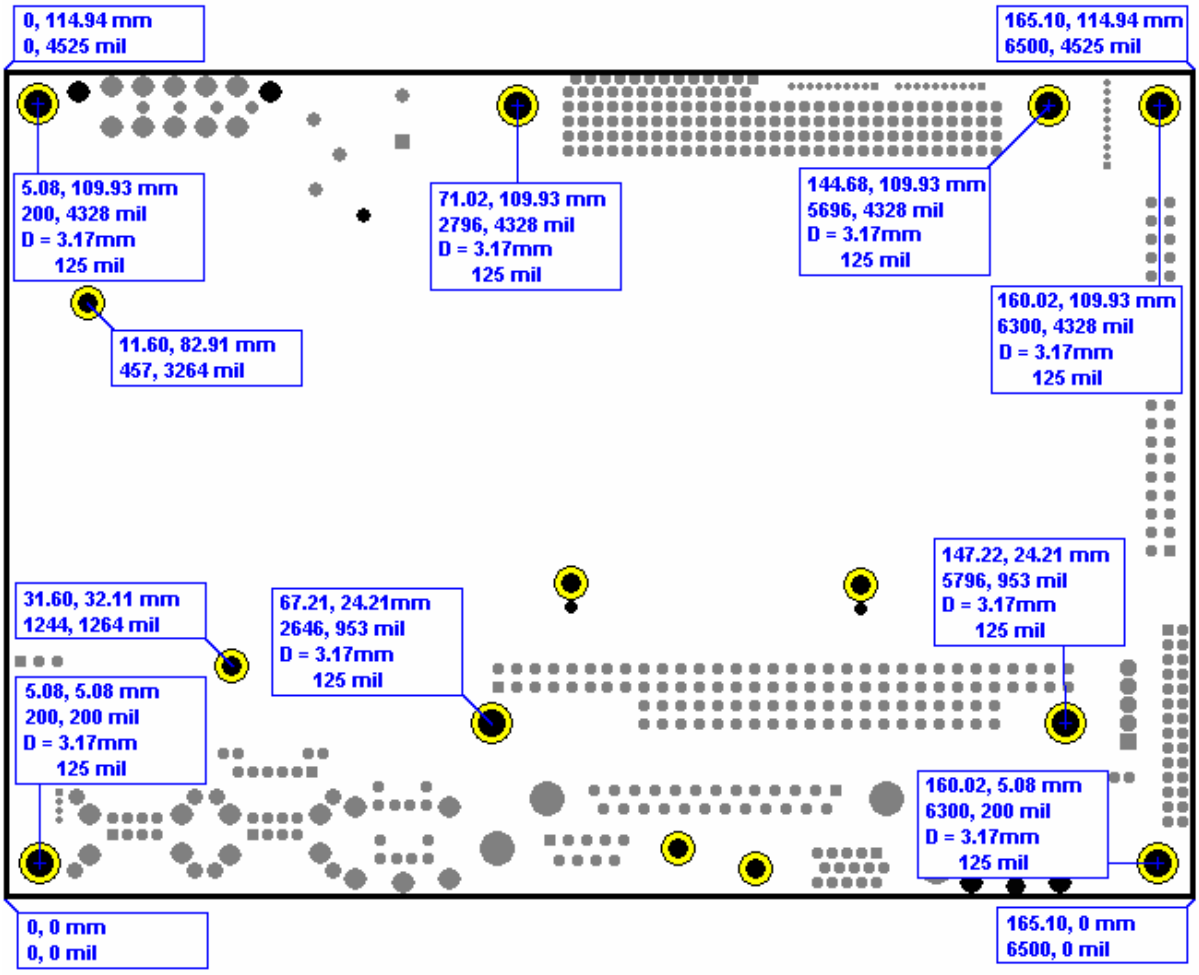
25 Appendix C: Block Diagram



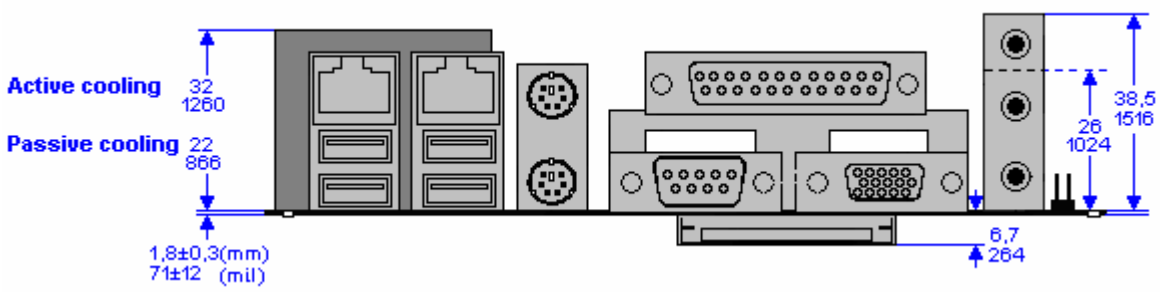
26 Appendix D: Mechanical Dimensions

26.1 Board Dimensions and Mounting Holes

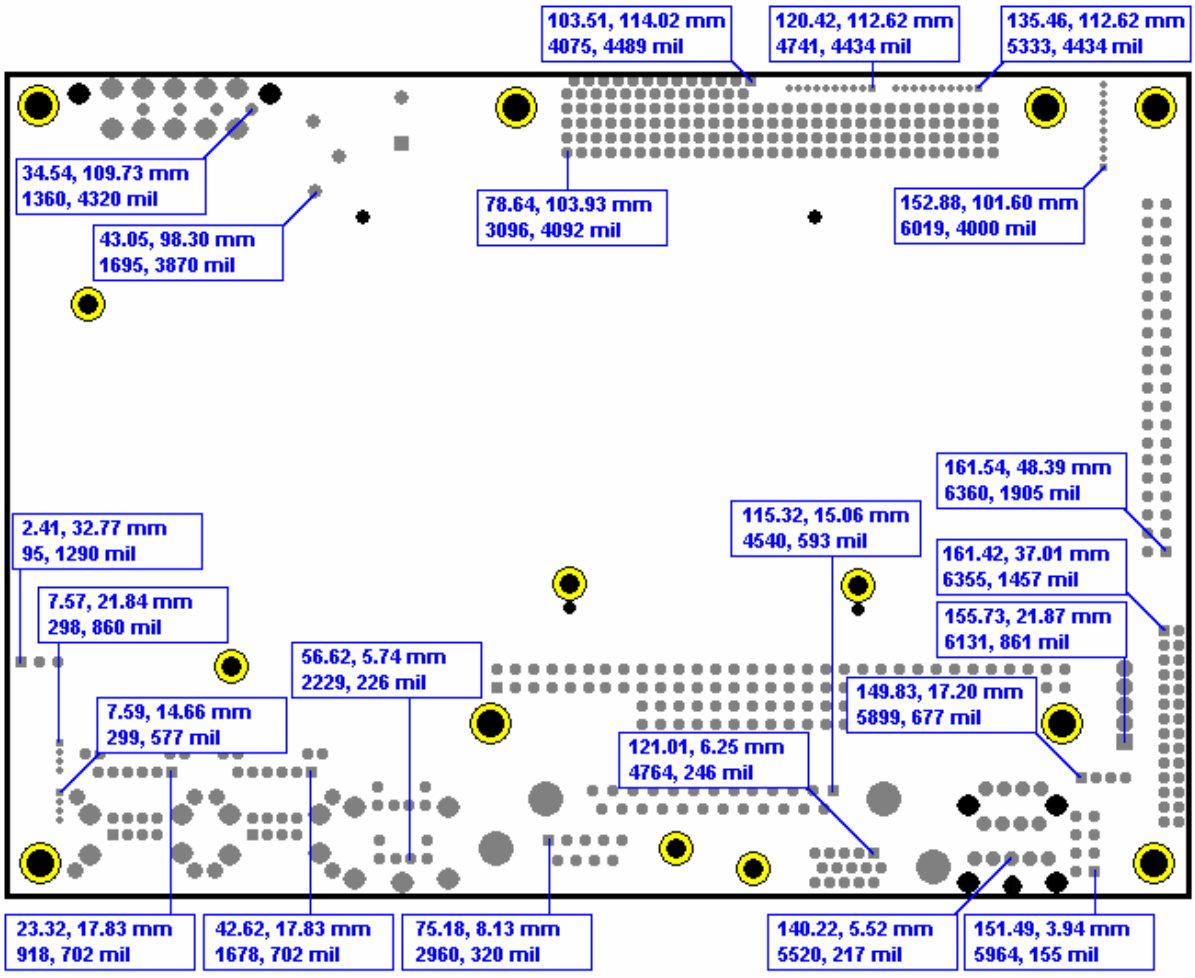
26.1.1 Top View



26.1.2 Front View

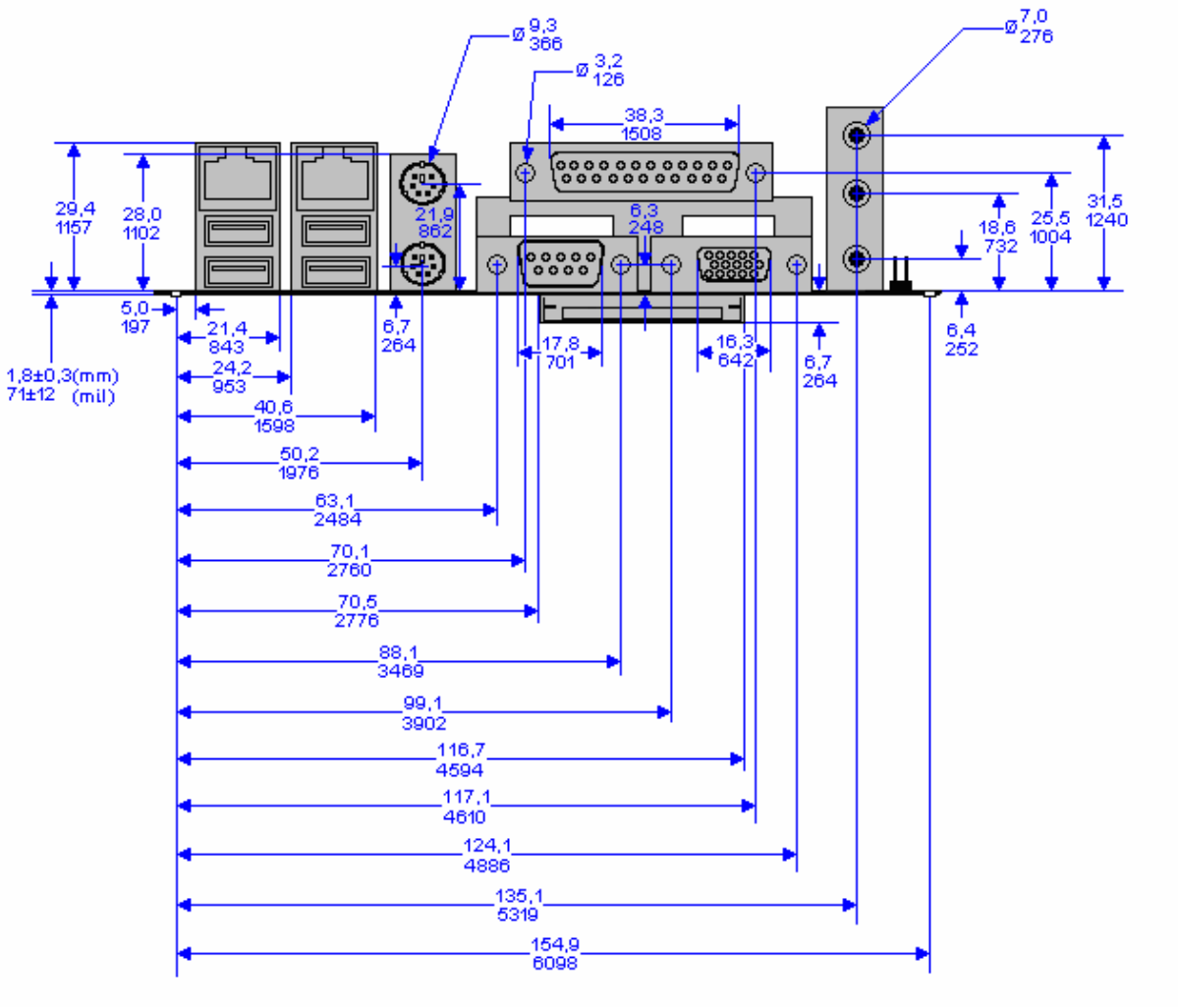


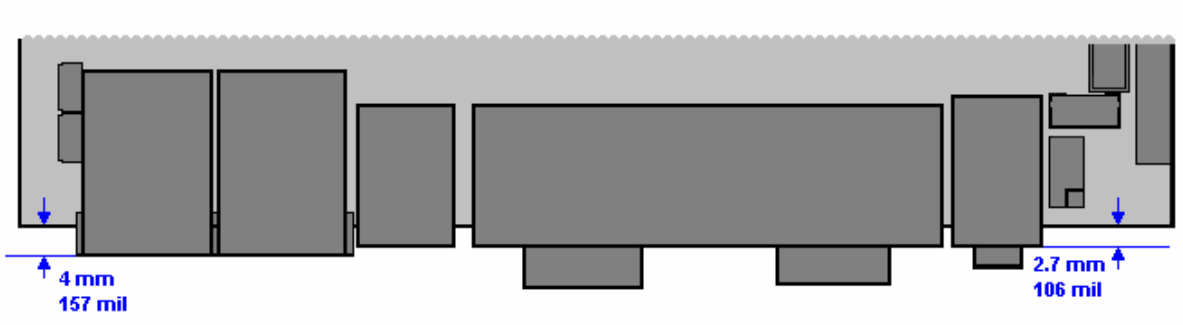
26.2 Connector Locations (Pin 1)



26.3 Slot Dimensions

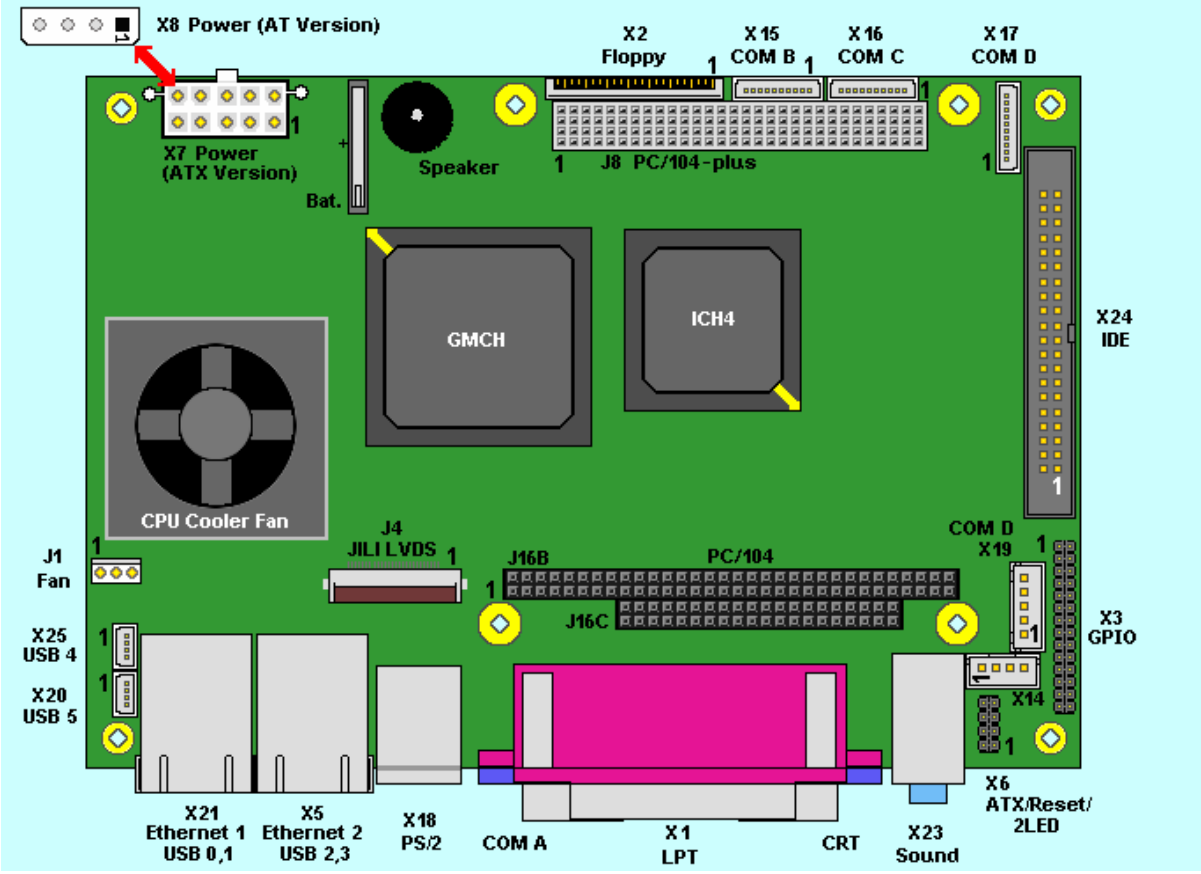
26.3.1 Front and Top View





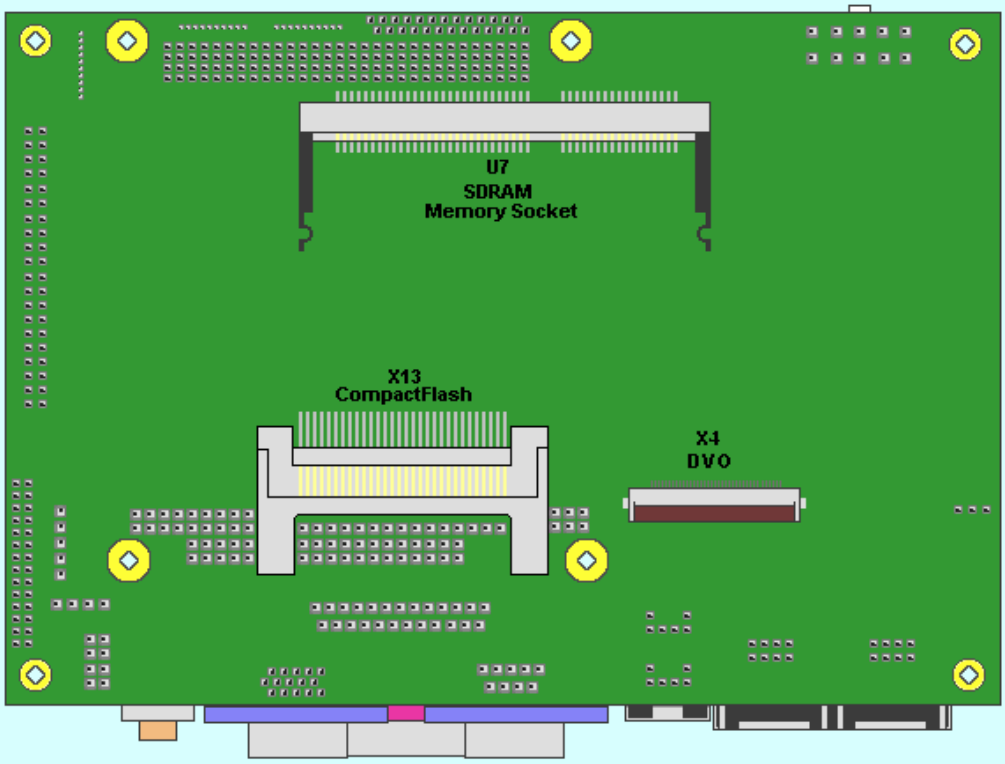
27 Appendix E: Connector Layout

27.1 Top Side



Notes: *The position of Pin 1 is marked with a quadratic pad on the PCB.*

27.2 Bottom Side



27.3 Connector Functions and Interface Cables

The table notes connector functions, as well as mating connectors and available cables.

Connector	Function	Mating Connector	Available Cable or Accessory	Description
J1	Fan Interface	2.54mm 3 pos. (AMP MTA-100 3-640440-3 or compatible)		For fan connection
J4	JILI LVDS Interface		KAB-JILI-?????? (see separate cable list)	For JILI interface cables
J8	PC/104-Plus Bus (PCI part)	2mm 120pos. (EPT 264-60303-12)		
J16B	PC/104 Bus (XT-Bus part)	2.54mm 64 pos. (EPT 962-60323-12 or compatible for board to board connection)		
J16C	PC/104 Bus (AT-Bus part)	2.54mm 40 pos. (EPT 962-60203-12 or compatible for board to board connection)		
X1	CRT Connector	Standard DSUB15 male plug		For CRT monitor connection
	Serial Interface Connectors (COM A)	Standard DSUB9 female plug.		For DSUB9 RS232 connection
	Parallel Interface LPT Connector	Standard DSUB25 male plug.		For DSUB 25 LPT connection
X2	Floppy Drive Interface Connector		ADA-FLOPPY-2 (PN 96001-0000-00-0) or KAB-FLOPPY/MOPS-1 (PN 96019-0000-00-0)	For 3.5" floppy or slim-line floppy.
X3	GPIO Connector	2mm 28 pos. female header		For general purpose I/O usage
X4	Optional DVO Connector			For DVO interfacing
X5	2 USB Connectors	Standard USB plug		For USB device connection
	Ethernet Connector	Standard RJ45 plug		For Ethernet connection
X6	ATX/Reset/2LED Connector	2.54mm 8 pos. female header		For power and reset button
X7	ATX Power Connector	AMP DUAC Connector or compatible	KAB-ATX-20T010 (PN 96072-0000-00-0)	For power connection
X8	AT Power Connector	Mate-N-Lok Connector (AMP 1-480424-0 or compatible)		For power connection
X13	CompactFlash Connector			For CompactFlash IDE storage devices.

Connector	Function	Mating Connector	Available Cable or Accessory	Description
X14	Line-In Connector	2mm 4 pos. (Molex 87369-0400 or compatible)		For internal line-in connection
X15, X16, X17	Serial Interface Connectors	1.25mm 10 pos. (Molex 51021-1000 or compatible)	KAB-DSUB9-3 (PN 96061-0000-00-0)	For DSUB 9 adaptation.
X18	PS/2 Keyboard and Mouse Interfaces	Standard PS/2 plugs		For PS/2 Mouse and Keyboard
X19	Serial Interface Connector COM D	2.5mm 5 pos. (JST XHP-5 or compatible)		For RS485 connection
X20, X25	USB interface connector	1.25mm 4 pos. (Molex 51021-0400 or compatible)	KAB-USB-1 (PN 96054-0000-00-0)	For standard USB adoption
X21	2 USB Connectors	Standard USB plug		For USB device connection
	Ethernet Connector	Standard RJ45 plug		For Ethernet connection
X23	Sound Interface	Standard audio plugs		For audio interfacing
X24	Primary IDE Hard Disk Interface Connector	2.54mm 40 pos. (AMP 4-215882-0 or compatible)	KAB-IDE-1 (PN 96022-0000-00-0)	For 3.5" HDD

27.4 Pin-out Table

Pin	COM A	COM B-D	COM D RS485	LPT	Floppy	Primary IDE	Compact Flash	ATX/ Reset/ 2LED	CRT
	X1	X15–X17	X19	X1	X2	X24	X13	X6	X1
1	/DCD1	/DCD	RXD+	/STB	VCC *	/HDRST	GND	HDLED	RED
2	SIN1	/DSR	RXD-	PD0	/IDX	GND	D3	CFLED	GRN
3	SOUT1	SIN	GND	PD1	VCC *	PIDE_D7	D4	VCC	BLU
4	/DTR1	/RTS	TXD+	PD2	/DR0	PIDE_D8	D5	VCC	NC
5	GND	SOUT	TXD-	PD3	VCC *	PIDE_D6	D6	/RESIN	GND
6	/DSR1	/CTS		PD4	/DSKCHG	PIDE_D9	D7	GND	GND
7	/RTS1	/DTR		PD5	NC	PIDE_D5	/CS1	/PWRBTN	GND
8	/CTS1	/RI		PD6	NC	PIDE_D10	GND	GND	GND
9	RI1	GND		PD7	NC	PIDE_D4	GND		NC
10		VCC *		/ACK	/MTR0	PIDE_D11	GND		GND
11				/BUSY	NC	PIDE_D3	GND		NC
12				PE	/FDIR	PIDE_D12	GND		DDDA
13				/SLCT	NC	PIDE_D2	VCC		HSYNC
14				/AFD	/STEP	PIDE_D13	GND		VSYNC
15				/ERR	GND	PIDE_D1	GND		DDCK
16				/INIT	/WDATA	PIDE_D14	GND		
17				/SLIN	GND	PIDE_D0	GND		
18				GND	/WGATE	PIDE_D15	SA2		
19				GND	GND	GND	SA1		
20				GND	/TRK0	NC	SA0		
21				GND	GND	PIDE_DRQ	D0		
22				GND	/WRTPRT	GND	D1		
23				GND	GND	/PIDE_IOW	D2		
24				GND	/RDATA	GND	IOCS16		
25				GND	GND	/PIDE_IOR	GND		
26					/HDSEL	GND	GND		
27						PIDE_RDY	D11		
28						PIDE_PD1	D12		
29						/PIDE_AK	D13		
30						GND	D14		
31						PIDE_IRQ	D15		
32						NC	/CS3		
33						PIDE_A1	GND		
34						PIDE_ATAD	/IOR		
35						PIDE_A0	/IOW		
36						PIDE_A2	VCC		
37						/PIDE_CS1	IRQ		
38						/PIDE_CS3	VCC		
39						PIDE_ACT	GND		
40						GND	NC		
41							/RESET		
42							IOCHRDY		
43							DRQ		
44							DACK		
45							SIDE_ACT		
46							ATADET		
47							D8		
48							D9		
49							D10		
50							GND		

Pin	Ethernet	PS/2 Keyboard	PS/2 Mouse	USB	Line-In	GPIO	Power ATX	Power AT	Fan
	X5, X21	X18	X18	X5, X20, X21, X25	X14	X3	X7	X8	J1
1	TXD+	KBDAT	MSDAT	VCC * ***	AUXL_C/REAR_L	GP0	PS_ON	V5S *	Sense
2	TXD-	NC	NC	USB-	ASGND	GP14	GND	GND	VCC *
3	RXD+	GND	GND	USB+	AUXR_C/ REAR_R	GP1	GND	GND	GND
4	NC **	VCC *	VCC *	GND	ASGND	GP15	+12V *	VCC12 *	
5	NC **	KBCLK	MSCLK			GP2	+3.3V *		
6	RXD-	NC	NC			GP16	+5V_SB		
7	NC **					GP3	+5V		
8	NC **					GP17	+5V		
9						GP4	-12V		
10						GP18	GND		
11						GP5			
12						GP19			
13						GP6			
14						GP20			
15						GP7			
16						GP21			
17						GP8			
18						GP22			
19						GP9			
20						GP23			
21						GP10			
22						GP24			
23						GP11			
24						GP25			
25						GP12			
26						GND			
27						GP13			
28						GND			

Notes: *(*) To protect the external power lines of peripheral devices, make sure that:*
-- the wires have the right diameter to withstand the maximum available current
-- the enclosure of the peripheral device fulfils the fire-protecting requirements of
-- IEC/EN 60950.

(**) Do not connect anything to these signals.

(***) The internal USB ports 4 and 5 are not protected on the power lines. An additional resetable fuse is recommended.

Pin	PC104 (A)	PC104 (B)	PC104 (C)	PC104 (D)	PC/104 Plus (A)	PC/104 Plus (B)	PC/104 Plus (C)	PC/104 Plus (D)
	J16B/C				J8			
0			GND	GND				
1	/IOCHCK	GND	/SBHE	/MEMCS16	GND	Reserved	VCC (**)	AD00
2	SD7	RESETDRV	LA23	/IOCS16	VCC (**)	AD02	AD01	AD03
3	SD6	VCC (**)	LA22	IRQ10	AD05	GND	AD04	AD03
4	SD5	IRQ9	LA21	IRQ11	C/BE0	AD07	GND	AD06
5	SD4	-5V (**)	LA20	IRQ12	GND	AD09	AD08	GND
6	SD3	DRQ2	LA19	IRQ15	AD11	VCC (**)	AD10	GND
7	SD2	-12V (**)	LA18	IRQ14	AD14	AD13	GND	AD12
8	SD1	/0WS	LA17	/DACK0	VCC3 (**)	C/BE1	AD15	VCC3 (**)
9	SD0	+12V (**)	/MEMR	DRQ0	SERR	GND	SB0	PAR
10	IOCHRDY	GND (*)	/MEMW	/DACK5	GND	PERR	VCC3 (**)	SDONE
11	AEN	/SMEMW	SD8	DRQ5	STOP	VCC3 (**)	LOCK	GND
12	SA19	/SMEMR	SD9	/DACK6	VCC3 (**)	TRDY	GND	DEVSEL
13	SA18	/IOW	SD10	DRQ6	FRAME	GND	IRDY	VCC3 (**)
14	SA17	/IOR	SD11	/DACK7	GND	AD16	VCC3 (**)	C/BE2
15	SA16	/DACK3	SD12	DRQ7	AD18	VCC3 (**)	AD17	GND
16	SA15	DRQ3	SD13	VCC (**)	AD21	AD20	GND	AD19
17	SA14	/DACK1	SD14	/MASTER	VCC3 (**)	AD23	AD22	VCC3 (**)
18	SA13	DRQ1	SD15	GND	IS0 (AD20)	GND	IS1 (AD21)	IS2 (AD22)
19	SA12	/REFRESH	GND	GND	AD24	C/BE3	VI/O	IS3 (AD23)
20	SA11	SYSCLK			GND	AD26	AD25	GND
21	SA10	IRQ7			AD29	VCC (**)	AD28	AD27
22	SA9	IRQ6			VCC (**)	AD30	GND	AD31
23	SA8	IRQ5			REQ0	GND	REQ1	VI/O
24	SA7	IRQ4			GND	REQ2	VCC (**)	GNT0
25	SA6	IRQ3			GNT1	VI/O	GNT2	GND
26	SA5	/DACK2			VCC (**)	CLK0	GND	CLK1
27	SA4	T/C			CLK2	VCC (**)	CLK3	GND
28	SA3	BALE			GND	INTD	VCC (**)	RST
29	SA2	VCC (**)			+12V (**)	INTA	INTB	INTC
30	SA1	OSC			-12V (**)	Reserved	Reserved	Reserved
31	SA0	GND						
32	GND	GND						

Notes: *(*) Key pin for PC/104; GND for PC/104+ specification*

(**) To protect the external power lines of peripheral devices, make sure that:
- the wires have the right diameter to withstand the maximum available current
- the enclosure of the peripheral device fulfils the fire protecting requirements of IEC/EN 60950.

28 Appendix F: PC Architecture Information

The following sources of information can help you better understand PC architecture.

28.1 Buses

28.1.1 ISA, Standard PS/2 - Connectors

- AT Bus Design: Eight and Sixteen-Bit ISA, E-ISA and EISA Design, Edward Solari, Annabooks, 1990, ISBN 0-929392-08-6
- AT IBM Technical Reference Vol 1&2, 1985
- ISA & EISA Theory and Operation, Edward Solari, Annabooks, 1992, ISBN 0929392159
- ISA Bus Specifications and Application Notes, Jan. 30, 1990, Intel
- ISA System Architecture, Third Edition, Tom Shanley and Don Anderson, Addison-Wesley Publishing Company, 1995, ISBN 0-201-40996-8
- Personal Computer Bus Standard P996, Draft D2.00, Jan. 18, 1990, IEEE Inc

28.1.2 PC/104, PCI

- Embedded PC 104 Consortium
  The consortium provides information about PC/104 and PC/104-Plus technology. You can search for information about the consortium on the Web.
- PCI SIG
  The PCI-SIG provides a forum for its ~900 member companies, who develop PCI products based on the specifications that are created by the PCI-SIG. You can search for information about the SIG on the Web.
- PCI & PCI-X Hardware and Software Architecture & Design, Fifth Edition, Edward Solari and George Willse, Annabooks, 2001, ISBN 0-929392-63-9.
- PCI System Architecture, Tom Shanley and Don Anderson, Addison-Wesley, 2000, ISBN 0-201-30974-2.

28.2 General PC Architecture

- Embedded PCs, Markt&Technik GmbH, ISBN 3-8272-5314-4 (German)
- Hardware Bible, Winn L. Rosch, SAMS, 1997, 0-672-30954-8
- Interfacing to the IBM Personal Computer, Second Edition, Lewis C. Eggebrecht, SAMS, 1990, ISBN 0-672-22722-3
- The Indispensable PC Hardware Book, Hans-Peter Messmer, Addison-Wesley, 1994, ISBN 0-201-62424-9
- The PC Handbook: For Engineers, Programmers, and Other Serious PC Users, John P. Choisser and John O. Foster, Annabooks, 1997, ISBN 0-929392-36-1

28.3 Ports

28.3.1 RS-232 Serial

- EIA-232-E standard
  The EIA-232-E standard specifies the interface between (for example) a modem and a computer so that they can exchange data. The computer can then send data to the modem, which then sends the data over a telephone line. The data that the modem receives from the telephone line can then be sent to the computer. You can search for information about the standard on the Web.
- RS-232 Made Easy: Connecting Computers, Printers, Terminals, and Modems, Martin D. Seyer, Prentice Hall, 1991, ISBN 0-13-749854-3
- National Semiconductor
  The Interface Data Book includes application notes. Type “232” as a search criteria to obtain a list of application notes. You can search for information about the data book on National Semiconductor’s Web site.

28.3.2 ATA

- AT Attachment (ATA) Working Group
  This X3T10 standard defines an integrated bus interface between disk drives and host processors. It provides a common point of attachment for systems manufacturers and the system. You can search for information about the working group on the Web.
  We recommend you also search the Web for information on *4.2 I/O cable*, if you use hard disks in a DMA3 or PIO4 mode.

28.3.3 USB

- USB Specification
  USB Implementers Forum, Inc. is a non-profit corporation founded by the group of companies that developed the Universal Serial Bus specification. The USB-IF was formed to provide a support organization and forum for the advancement and adoption of Universal Serial Bus technology. You can search for information about the standard on the Web.

28.4 Programming

- C Programmer’s Guide to Serial Communications, Second Edition, Joe Campbell, SAMS, 1987, ISBN 0-672-22584-0
- Programmer's Guide to the EGA, VGA, and Super VGA Cards, Third Edition, Richard Ferraro, Addison-Wesley, 1990, ISBN 0-201-57025-4
- The Programmer’s PC Sourcebook, Second Edition, Thom Hogan, Microsoft Press, 1991, ISBN 1-55615-321-X
- Undocumented PC, A Programmer’s Guide to I/O, CPUs, and Fixed Memory Areas, Frank van Gilluwe, Second Edition, Addison-Wesley, 1997, ISBN 0-201-47950-8

29 Appendix G: Document Revision History

Version	Date	Edited by	Changes
E815M101	20.01.2005	WEC	Created preliminary manual
E815M102	21.01.2005	BOM	Review prelim manual - update support contact and feature set list. Minor formatting.
E815M103	29.03.2005	WEC	Added Front Side measurements Changed PCB thickness
E815M104	31.05.2005	WEC	Updated current consumption values
E815M105	01.06.2005	WEC	Added top side dimensions
E815M106	06.07.2005	VGG	Added power consumption
E815M110	20.07.2005	VGG	Add 3.3V in PCI, mechanical drawings, RS485 connector, first official release
E815M111	01.09.2005	BHO	Changed to Kontron style, added lots of information
E815M112	07.09.2005	BHO, JL	Grammatical corrections, changed information about serial number in BIOS chapter
E815M113	09.02.2006	BHO	New Kontron logo, new support addresses, corrected overheat protection information in specifications chapter, updated I/O address map, corrected connector layout top side, corrected and added supply current values,
E815M114	31.07.2007	GUL	Updated to current Kontron Layout, changed DVO interface to optional, added warnings about +3.3V supply on +5V-only boards using PC/104 extension cards Release of E815M114.PDF