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EB860

E²Brain PowerPC Modules based on Motorola Power QUICC MPC8xx Processors

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E²BRAIN®

The product described in this manual is in compliance with all applied CE standards.

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Explanation of Symbols



CE Conformity

This symbol indicates that the product described in this manual is in compliance with all applied CE standards. Please refer also to the section “Applied Standards” in this manual.



Caution, Electric Shock!

This symbol and title warn of hazards due to electrical shocks (> 60V) when touching products or parts of them. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your material.

Please refer also to the section “High Voltage Safety Instructions” on the following page.



Warning, ESD Sensitive Device!

This symbol and title inform that electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Please read also the section “Special Handling and Unpacking Instructions” on the following page.



Warning!

This symbol and title emphasize points which, if not fully understood and taken into consideration by the reader, may endanger your health and/or result in damage to your material.



Note...

This symbol and title emphasize aspects the reader should read through carefully for his or her own advantage.

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For Your Safety

Your new Kontron product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new Kontron product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions



Warning!

All operations on this device must be carried out by sufficiently skilled personnel only.



Caution, Electric Shock!

Before installing your new Kontron product into a system always ensure that yo ur mains power is switched off. This applies also to the installation of piggybacks.

Serious electrical shock hazards can exist during all installation, repair and maintenance operations with this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing work.

Special Handling and Unpacking Instructions



ESD Sensitive Device!

Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory back-up, ensure that the board is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the board.

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General Instructions on Usage

In order to maintain Kontron's product warranty, this product must not be altered or modified in any way. Changes or modifications to the device, which are not explicitly approved by Kontron Modular Computers GmbH and described in this manual or received from Kontron's Technical Support as a special handling instruction, will void your warranty.

This device should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This applies also to the operational temperature range of the specific board version, which must not be exceeded. If batteries are present their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, please follow only the instructions supplied by the present manual.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the board please re-pack it as nearly as possible in the manner in which it was delivered.

Special care is necessary when handling or unpacking the product. Please, consult the special handling and unpacking instruction on the previous page of this manual.

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Chapter 1

Introduction

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1. Introduction

The E²Brain™ module described in this manual is designed to Kontron Modular Computers' "E²Brain™ Module Specification", revision 01. Section 1.1 provides general information regarding this specification and the system environment as envisioned for E²Brain™ modules. For more detailed information regarding the "E²Brain™ Module Specification", please contact Kontron Modular Computers.

The remaining sub-sections of the Introduction provide more specific details of the EB860 E²Brain™ module itself to familiarize the user with this product as a whole.

1.1 The E²Brain™ Concept

The E²Brain™ concept is a highly flexible approach to providing application developers with the ability to concentrate on the definition of application requirements without having to continuously factor in potential restrictions concerning available data processing and communications functionality.

More specific, data processing and communications requirements become a function of the application and not vice versa. This is possible through the implementation of the E²Brain™ concept. Unlike other approaches to providing application solutions, the E²Brain™ concept concentrates on the most essential aspects of providing data processing and communications without attempting to provide in one entity a complete, self-contained computer system.

The E²Brain™ specification first of all defines a PCB module with a form factor of 115 x 75 x 11.6 millimeters. For interfacing with applications, the specification calls for up to four connectors which provide not only interfacing capability for current industry standards but also for future standards or application specific requirements. The type, location, and usage of these connectors is also defined in the specification so as to guarantee standardized compatibility. The specification is open as to the data processing and communications functionality to be implemented which is by definition a function of the application requirements. In addition, the specification envisions considerations for thermal energy dissipation through the implementation of what are to be known as BrainCAP™s (E²Brain™ **C**ooling **A**ssembly, **P**rotector) which can range from heat spreaders to highly sophisticated heat sink cooling designs.

The key features of the E²Brain™ concept are:

- Very compact and robust form factor
- Independent of CPU architecture
- Scalable, flexible, and open system interface
- PCI Master and Agent Mode
- PCI-64 and PCI-X capability
- Versatile and very powerful communications interfaces
- Complete thermal design concept

1.1.1 E²Brain™ Functionality

E²Brain™ (Embedded Electronic Brain) is a new platform architecture for advanced computer modules. The E²Brain™ specification defines a very compact mechanical form factor and a comprehensive set of functional interfaces which can be adapted to a wide variety of applications. E²Brain™ modules provide complete computer cores integrating a high-performance CPU, system memory and - typical for E²Brain™ - advanced communications controllers. E²Brain™ modules are plugged into customized backplanes or standardized carrier boards

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which themselves provide the physical interfaces (PHYs) and connectors, power, and additional IO controllers. Through the use of E²Brain™ modules the system developer is relieved of the task of designing computers, and, instead, they permit him to concentrate on the specific product development.

E²Brain™ is a computer platform dedicated not just to one architecture like the PC and Windows architecture, but it is open for all architectures including PowerPC, ARM, SH, x86, and others. E²Brain™ modules are very suitable for “deeply” embedded applications requiring flexible computing power combined with versatile and high-performance communications power.

Although typical E²Brain™ modules are designed to be low power consumption devices, they are part of a well thought out thermal design concept which considers the thermal aspects right from the beginning. Where higher power consumption is unavoidable, E²Brain™ modules are fitted with appropriate BrainCAP™s. By utilizing BrainCAP™s, cooling, mechanical stabilization, and EMI protection are combined in a single concept to satisfy almost any application requirement.

1.1.2 Basic Architecture

The following figure illustrates the basic functional architecture of E²Brain™ modules. Common to all E²Brain™ modules are the data processing and communications core and the system and communications interfaces.

The application requirements determine the functionality required of the E²Brain™ module core which in turn mandates the functionality to be provided by the system and communications interfaces. Both of these interfaces are comprised of a base set and an extended set of functional features.

The system interface to the application is accomplished through connectors Pn1 and Pn2. Connector Pn1 provides the base set of system interfacing and Pn2 the extended set. If the application does not require extended system interfacing, it is not necessary to populate connector Pn2. The same analogy applies to the communications interfacing whereby connector Pn3 provides the base set of communications interfacing and Pn4 the extended set. Pn4 is not required to be populated if there is not an application requirement for it. This concept together with a corresponding core provides a maximum of scalability and flexibility to satisfy the most demanding of applications.

1.1.3 E²Brain™ System Environment

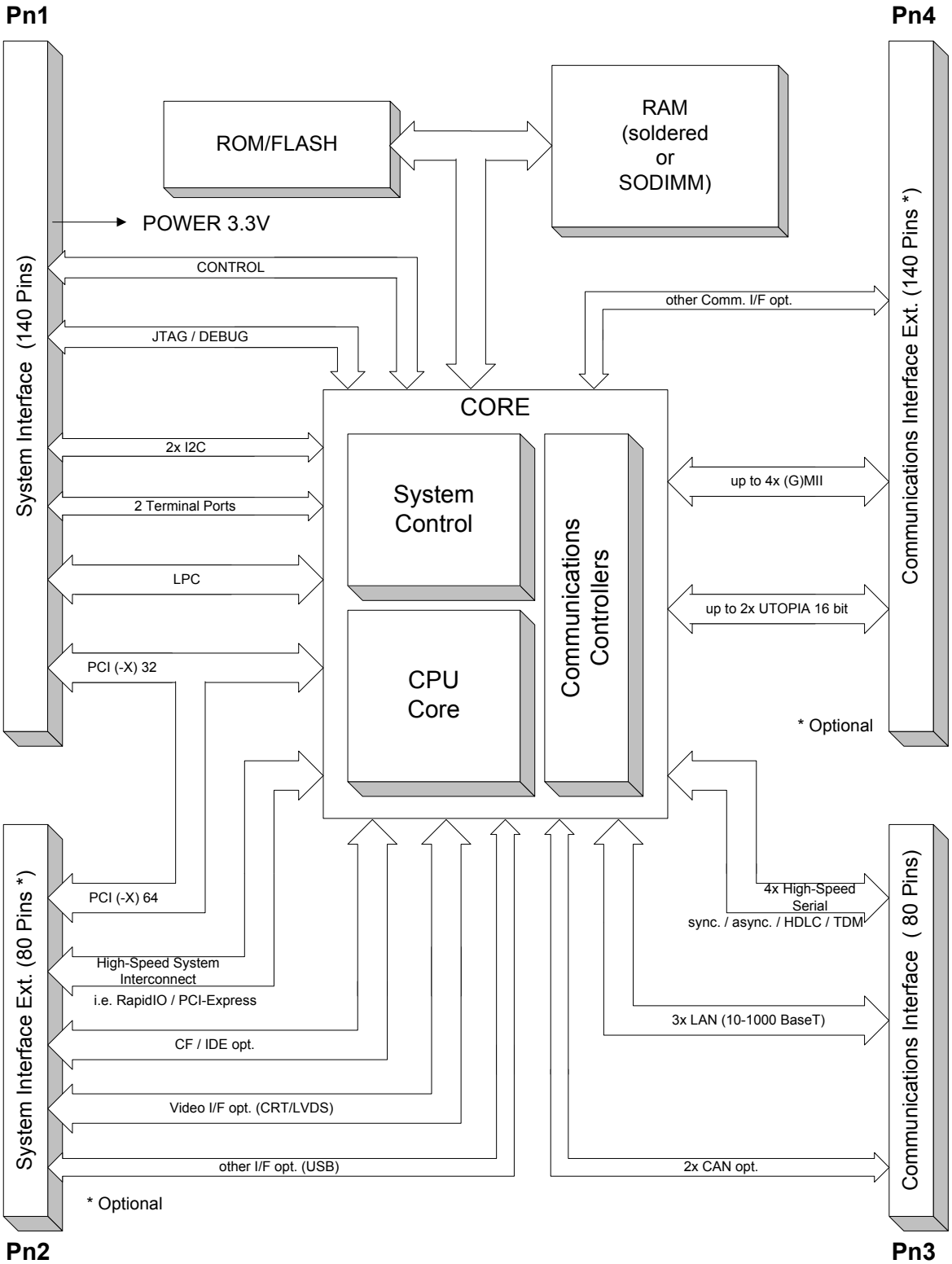
The E²Brain™ module form factor and mechnical and electrical interfacing are so conceived as to allow the use of E²Brain™ modules in practically any kind of system environment. These mezzanine modules can easily be integrated on most standardized carrier boards (VME, CompactPCI, PC PCI, etc.) as well as any other conceiveable type of carrier board capable of providing the required mechanical and electrical infrastructure.

In addition to this infrastructure, thermal energy dissipation requirements must be taken into consideration when implementing applications using E²Brain™ modules. The E²Brain™ concept basically calls for modules to provide their own thermal energy dissipation. It may, however, be necessary to add additional thermal energy dissipation capability depending on the overall system environment. To satisfy such requirements, E²Brain™ modules may be equipped with specially designed cooling devices that are adapted to the specific system environment.

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Figure 1-1: E²Brain™ Basic Architecture



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1.2 EB860 System Overview

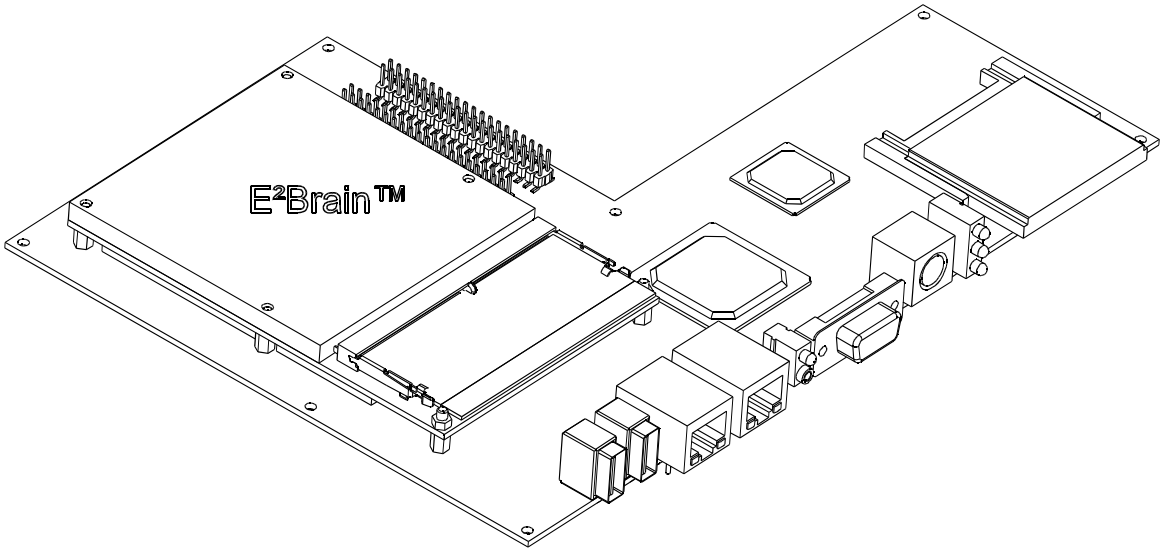
This E²Brain™ module is designed for applications requiring cost effective, high performance data processing capability where compact size, low power consumption, and interfacing flexibility are key factors for achieving a successful system design.

Specifically, system integrators are provided with a comprehensive set of industry standard interfaces from a range of low, medium, and high speed system level data exchange and monitor and control I/O's, and communications I/O's such as Ethernet and high speed serial data I/O's.

System integration of an EB860 E²Brain™ module requires a carrier board (industry standard or custom) which interfaces the application with the EB860 module. All signal conditioning, mechanical, and electrical interfacing with the application must be accomplished by the carrier board.

In addition, physical packaging and thermal energy dissipation must be provided by the system. As the EB860 is designed as a low power consumption device, it does not pose any special requirements for cooling. Integration on a carrier board is done via the four connectors and standoffs which allow for secure mounting to the carrier board. The following figure illustrates a typical integration of an E²Brain™ module on a custom carrier board.

Figure 1-2: E²Brain™ Module on a Custom Carrier Board



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1.3 Product Overview

The EB860 E²Brain™ High Performance PowerPC Processer Module is a part of an innovative concept to provide system integrators with a complete range of off-the-shelf as well as custom embedded computer cores for the most demanding of applications.

This module, designed around the Motorola POWER QUICC MPC 8xx processor family, provides a comprehensive set of standard computer functionality coupled with industry standard system and communications I/O capability. Realized on a compact, standardized, mezzanine board the EB860 provides a complete embedded computer core which can be readily integrated into most any application.

The basic functions of this board are to provide high performance data processing capability as well as flexible and comprehensive system and communications I/O. The major elements involved in these processes are: the MPC8xx communications processor, the Logic controller which is realized in a field-programmable gate array (FPGA), an Ethernet PHY, two system and two communications interfacing connectors. The EB860 provides five system I/Os: I²C, SPI, LPC, a PCI-bus, and a serial terminal and console. In addition, there are various onboard memory elements available: SDRAM, SRAM, FLASH, and EEPROM. For test and programming purposes there is also a JTAG/BDM interface available.

The following table provides a quick overview of the EB860 board

Table 1-1: EB860 Product Overview

EB860 FEATURES	DESCRIPTION
Product Type	High performance PowerPC embedded communications computer core: • Processor: Motorola MPC8xx communications Processor • Memory: SDRAM, SRAM, FLASH, EEPROM • Multiple system and communications I/Os • Form factor: E²Brain™ standard: 115 x 75mm • Complies with the E²Brain™ specification
I/Os	System: • I²C • SPI • LPC • PCI-bus • Serial: terminal and console Communications: • High speed serial UART • Fast Ethernet
Other	Test and Programming: • JTAG • BDM • ISP Monitor and Control: • GPIOs (General Purpose IOs) • Reset • LEDs • Switches

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1.4 Board Overview

1.4.1 Board Introduction

The EB860 is a high performance mezzanine computer module compliant to the Kontron Modular Computers' E²Brain™ Module Specification, revision 01.

This E²Brain™ module is comprised of a computer core, the Motorola MPC8xx Integrated Communications Processor, and a standard set of E²Brain™ system and communications interfaces as well as onboard memory.

The computer core provides direct interfacing for I²C, SPI, terminal and console, high speed serial, and test and programming. The remaining memory, system, and communications interfaces are realized using the core's memory controller interface in conjunction with corresponding interfacing and BPCC (Board Process/Communications Controller) devices (Ethernet, FPGA).

As thermal energy dissipation is a function of the application, the EB860 E²Brain™ module is only equipped with a BrainCAP™ when required.

1.4.2 Board Specific Information

Major board components of the EB860 E²Brain™ module are:

- Computer core: Motorola's MPC8xx Integrated Communications Processor with Embedded PowerPC core
- Board Process/Communications Controller (BPCC, realized in an FPGA)
- Fast Ethernet PHY
- Soldered SDRAM
- SRAM device
- Soldered FLASH device
- Serial EEPROM device
- RTC
- Reset controller
- GoldCap (SRAM and RTC backup)
- Two System Interface connectors
- Two Communications Interface connectors
- BrainCAP™ heatsink for EB860 (optional)

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1.5 System Relevant Information

The following system relevant information is general in nature but should still be considered when developing applications using the EB860.

Table 1-2: System Relevant Information

SUBJECT	INFORMATION
System Configuration	The EB860 operates with a PCI system clock frequency of 33 MHz. The number of EB860's which can be installed in any one system depends solely on the number of carrier interfaces available.
Master/Slave Functionality	The EB860 can function either as a PCI Master or PCI Agent.
System Controller	The EB860 can function as a system controller.
Application Interfacing	The application interfacing to the EB860 must comply with the specifications set forth in this manual.

1.5.1 System Configuration

System configuration is solely a function of the application, however, when implementing applications, precautions must be taken to ensure that the signals of the EB860 are properly terminated in accordance with the specifications set forth in this manual. For this reason it will be necessary for system integrators to ensure proper signal conditioning for their applications before interfacing with the EB860. In addition, it is imperative that signal interference be kept to a minimum.

1.5.2 Operating Software

The EB860 is supplied with appropriate operating system and board support software for board operation.

1.6 Board Diagrams

The following diagrams provide additional information concerning board functionality and component layout.

LEGEND FOR FIGURE 1-4 on page 1-11:

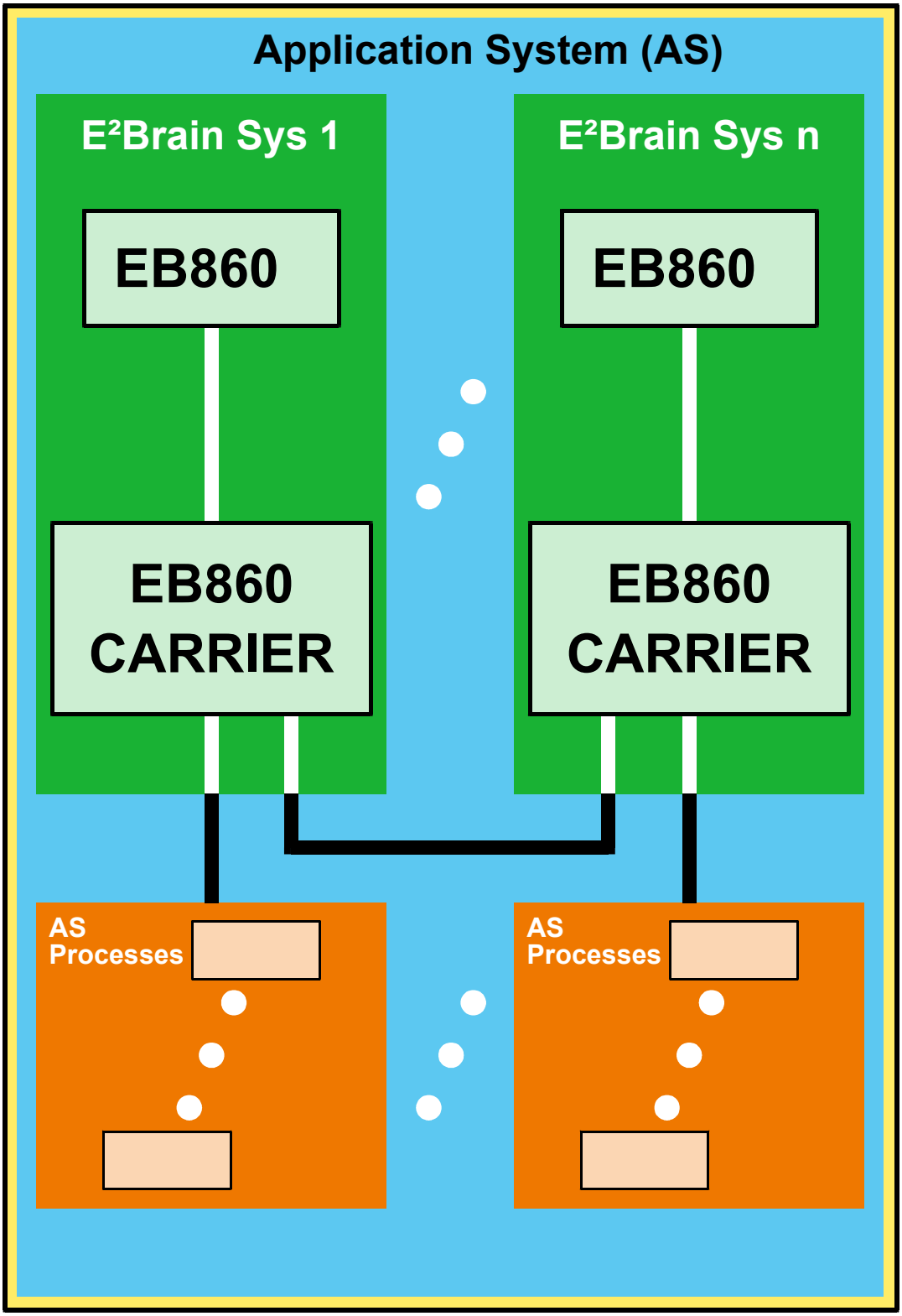
SPI	Serial Peripheral Interface
FE	Fast Ethernet
HSS	High Speed Serial
I²C	Inter-Integrated Circuit
LPC	Low Pin Count
M/C	Monitor and Control
PCI	Peripheral Component Interface
T/C	Terminal/Console (Serial Interface)
T/P	Test/Programming
UTOPIA	Universal Test and Operations PHY Interface for ATM

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1.6.1 Application System Interfacing

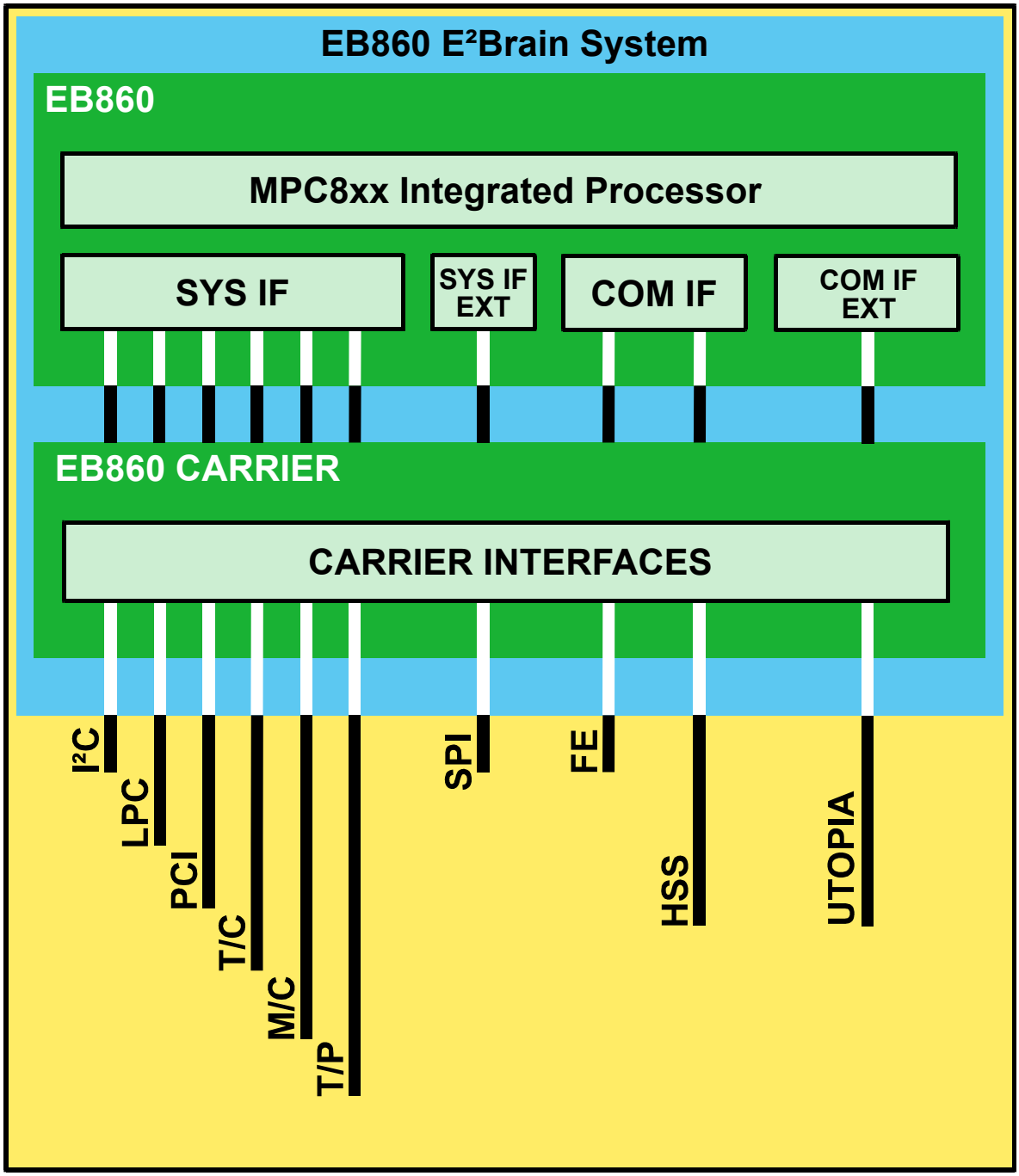
Figure 1-3: EB860 Application System Interfacing Diagram



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1.6.2 System Level Interfacing

Figure 1-4: EB860 System Level Interfacing Diagram



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1.6.3 Board Layout

Figure 1-5: EB860 Board (Top View)

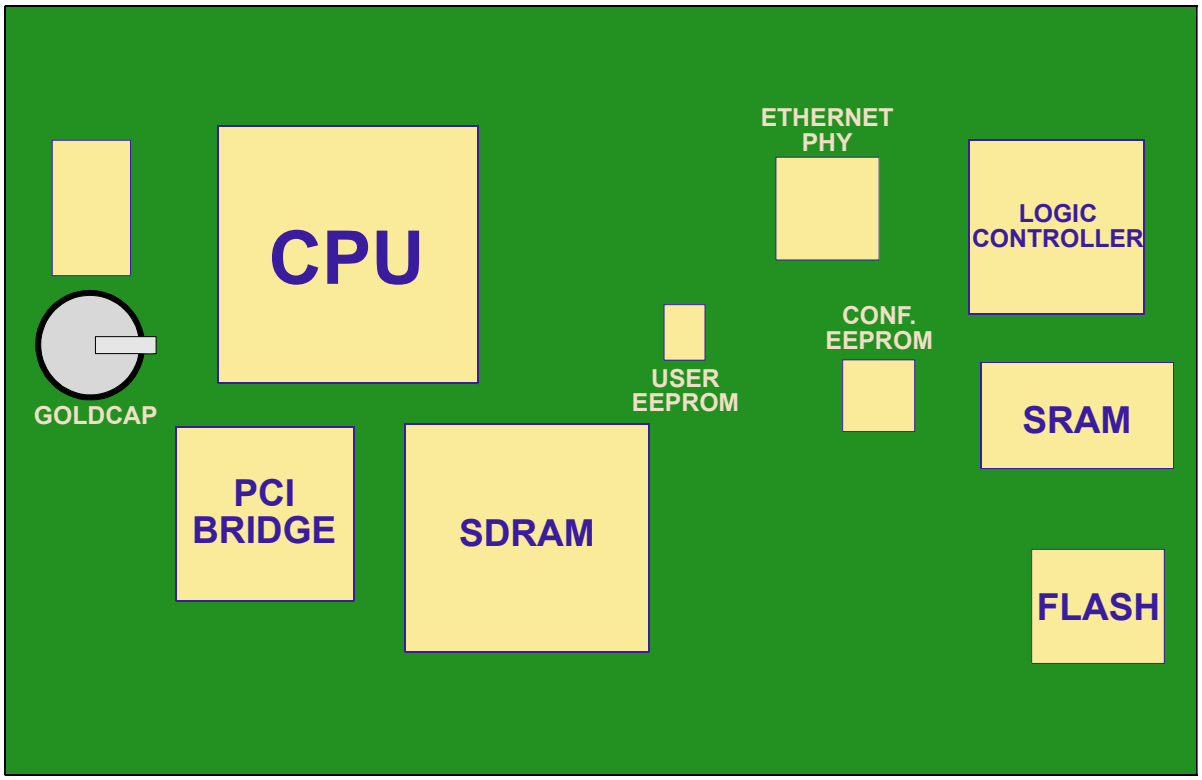
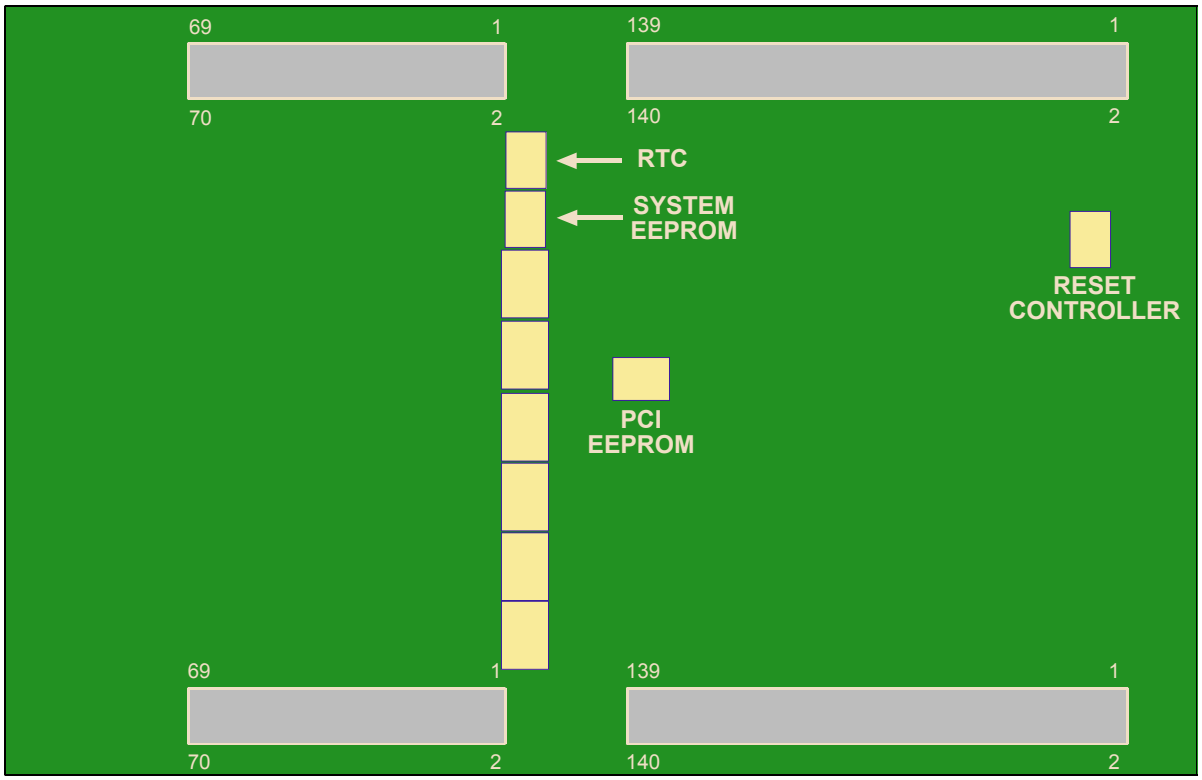


Figure 1-6: EB860 Board (Rear View)



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1.7 Technical Specifications

Table 1-3: EB860 Main Specifications

	EB860	Specifications
Processor and Related	Processor	In principle all Motorola MPC8xx Power QUICC processors can be used. Preferred choices: MPC855T, MPC857T, MPC859T, MPC860T, MPC862T, MPC866T ranging from 66MHz up to 133MHz (all in 1:2:1 mode)
	Boot device	Onboard soldered FLASH (default) or LPC Memory
	Main Memory	Soldered SDRAM: up to 128 MB, 32-bit
	Watchdog	Enabled by software with LED indication; generates Reset or NMI
	RTC	Real-time clock, backed up using GoldCap with the data retention being typically about 2 to 3 days. Longer backup times via auxiliary power from the carrier board are possible.
	BPCC	Board Process/Communications Controller: LPC interface, LEDs, operator switches, monitor and control functions
Peripheral Memory	SRAM	1 MB soldered, 512k x 16, backed up using Gold Cap with the data retention being typically about 2 to 3 days. Longer backup times via auxiliary power from the carrier board are possible.
	EEPROM (I²C)	64 kBit soldered, serial access
	Flash	Minimum of 4 MB and up to 32 MB soldered
External / Internal Interfaces	PCI	Tundra QSPAN II controller 32-bit, 33 MHz, PCI System Master and PCI Agent modes (no SDRAM access!)
	LPC	Low Pin Count sub-set, 8-bit IO and memory space access, realized in BPCC
	I²C	On-chip, message interface, full master/slave
	SPI	On-chip, configured for connection of slave devices to MPC8xx
	Fast Ethernet	10baseT, 100baseTX, Intel LXT972A Ethernet PHY
	Serial Ports	Terminal and console: SMC1: TERM (Terminal), TTL level SMC2: SER0 (Console), TTL level High speed serial: SCC1: SER1, TTL level SCC2: SER2, TTL level SCC3: SER3, TTL level SCC4: SER4, TTL level Note: SCC2 - SCC4 are only available on MPC86x CPU version
T/P Interfaces	Debug	BDM Debugging Option through the routing of the dedicated signals to the carrier board
	JTAG/ISP	Programming and testing is possible externally over the carrier board
M/C Interfaces	Inputs	Five system/application control inputs available
	Outputs	Five system/application monitor outputs available

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Table 1-3: EB860 Main Specifications (Continued)

	EB860	Specifications
General	Mechanical	Conforms with Kontron Modular Computers' "E²Brain™ Module Specification", revision 01
	Power Consumption	+3.3V / typically 1.0A (EB860 with 80MHz MPC860T, fully featured)
	Temperature Range	Operational: 0ºC to +70ºC Standard -40ºC to +85ºC E2 Storage: -55ºC to +125ºC
	Humidity	0% to 90% non-condensing
	Dimensions	115 mm L x 75 mm W
	Board Weight	50 grams

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1.8 Applied Standards

The Kontron Modular Computers' E²Brain™ modules comply with the requirements of the following standards:

Table 1-4: Applied Standards

	TYPE	STANDARD
CE	Emission	EN55022, EN61000-6-3
	Immunity, Industrial Environment	EN61000-6-2
	Immunity, IT Equipment	EN55024
	Electrical Safety	EN60950 Note: The EB860 is specified I/O only for: SELV and EVL. It is **NOT SPECIFIED** for "Hazardous"
MECHANICAL	Mechanical Dimensions	E²Brain™ Module Specification, Rev. 01
ENVIRONMENTAL	Vibration, Sinusoidal	IEC 60068-2-6
	Random Vibration, Broadband	IEC 60068-2-64
	Bump	IEC 60068-2-29
	Single Shock	IEC 60068-2-27
	Temperature Tests A: Cold	IEC 60068-2-1
	Temperature Tests B: Dry Heat	IEC 60068-2-2
	Climatic Humidity	IEC 60068-2-78
PRODUCT PACKAGING	Transport and Storage	IEC 61131-2
	ESD Protection	IEC 61340-5-1 and IEC 61340-5-2

1.9 Related Publications

Table 1-5: Related Publications

	ISSUED BY	DOCUMENT
PCI	PCI-SIG	PCI Local Bus Specification, R.2.2
LPC	Intel®	Intel® Low Pin Count (LPC) Interface Specification, Rev. 1.1
I²C	Philips	I2C-BUS SPECIFICATION, Rev. 2.1
E²Brain	Kontron Modular Computers	E²Brain™ Module Specification, Rev. 01

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Chapter 2

Functional Description

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2. Functional Description

The following chapters present more detailed, board level information about the EB860 E²Brain™ High Performance PowerPC Processer Module whereby the board components and their basic functionality are discussed in general.

2.1 General Information

The EB860 is comprised basically of the following:

- Motorola MPC8xx Integrated Communications Controller
- Board Process/Communications Controller (BPCC)
  - Realized in an FPGA device
  - Controls onboard interfacing
  - Provides LPC interface
  - Provides system monitor and control functions
- System interfaces for:
  - I²C bus
  - LPC bus
  - PCI bus
  - SPI bus
  - Terminal and Console (T/C) serial interfacing
  - Monitor and Control (M/C) interfacing
  - Test and Programming (T/P) interfacing
- Communications interfaces for:
  - High Speed Serial (HSS) communications
  - Fast Ethernet (FE)
  - Universal Test and Operations PHY Interface for ATM (UTOPIA)
- Memory
  - Soldered SDRAM as main memory
  - Soldered SRAM, backed-up using a GoldCap and/or auxiliary power line
  - Soldered FLASH
  - Serial EEPROM
- Monitor and Control
  - Interfacing for LED's, operator switches, system monitor/control signals (Reset, Abort, PFail etc.)
  - RTC
  - Watchdog timer
  - Clock generation
  - Reset generation
  - Board control registers
- Test and Programming
  - Debugging interface
  - JTAG/ISP interface
- Software
  - Operating system
  - Board Support Package
  - Boot Strap Loader (NetBoot Loader)

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2.1.1 CPU List

Table 2-1: CPU List

CPU Type	Frequency	Core voltage	IO voltage
MPC855T	66 MHz	3.3 V	3.3 V
MPC855T	80 MHz	3.3 V	3.3 V
MPC857T	80 MHz	3.3 V	3.3 V
MPC857T	100 MHz	3.3 V	3.3 V
MPC859T	100 MHz	1.8V	3.3V
MPC859T	133 MHz	1.8V	3.3V
MPC860T	66 MHz	3.3 V	3.3 V
MPC860T	80 MHz	3.3 V	3.3 V
MPC862T	80 MHz	3.3 V	3.3 V
MPC862T	100 MHz	3.3 V	3.3 V
MPC866T	100 MHz	1.8V	3.3V
MPC866T	133 MHz	1.8V	3.3V



Note...

The table above provides the first CPU choices on the EB860. Other Power QUICC derivates are available on request.

2.1.1.1 Processor Characteristics of Preferred CPU's

Table 2-2: Processor Characteristics of Preferred CPU's

Processor	SCC´s	HDLC channels	10BaseT Ethernet	Fast Ethernet/ ATM	UTOPIA	T1/E1	Core Voltage	Max. CPU Fr.
MPC855T	1	Up to 32	1	Mulitplexed → Either Ethernet or ATM	8Bit UTO-PIA I	1	3.3V	80MHz
MPC857T	1	Up to 32	1	Simultaneous Ethernet and ATM possible	8Bit UTO-PIA II	1	3.3V	100MHz
MPC859T	1	Up to 32	1	Simultaneous Ethernet and ATM possible	8Bit UTO-PIA II	1	1.8V	133MHz
MPC860T	4	Up to 64	Up to 4	Mulitplexed → Either Ethernet or ATM	8Bit UTO-PIA I	2	3.3V	80MHz
MPC862T	4	Up to 64	Up to 4	Simultaneous Ethernet and ATM possible	8Bit UTO-PIA II	2	3.3V	100MHz
MPC866T	4	Up to 64	Up to 4	Simultaneous Ethernet and ATM possible	8Bit UTO-PIA II	2	1.8V	133MHz

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2.1.2 Board Process/Communications Controller (BPCC)

The BPCC provides extensive interfacing and monitor/control functionality for the EB860. It provides control for most onboard devices, addressing, and clocking. The LPC interface and the watchdog timer are also realized in the BPCC in addition to a bus error timer. The various functional blocks are described in more detail later in this manual.

2.1.3 System Interfacing

The EB860 E²Brain™ module is supplied with a comprehensive set of system interfacing capabilities. The standard set of system interfaces is routed through the System Interface connector CON1 (Pn1). An extended set of system interfacing is routed through the System Interface Extension connector CON2 (Pn2).

The System Interface connector CON1 provides interfacing for the following:

- I²C bus
- LPC bus
- PCI bus
- Terminal and Console (T/C) serial interfacing (TERM and SER0)
- Monitor and Control (M/C) interfacing
- Test and Programming (T/P) interfacing

The System Interface Extension connector CON2 provides interfacing for the following:

- SPI interface

2.1.4 Communications Interfacing

The EB860 E²Brain™ module is also supplied with a comprehensive set of communications interfacing capabilities. The standard set of communications interfaces is routed through the Communications Interface connector CON3 (Pn3). An extended set of communications interfacing is routed through the Communications Interface Extension connector CON4 (Pn4).

The Communications Interface connector CON3 provides interfacing for the following:

- High Speed Serial (HSS) interfacing (TTL level) (SER1, SER2, SER3, SER4)
- Fast Ethernet (MDI interface)

The Communications Interface Extension connector CON4 provides interfacing for the following

- UTOPIA interface (TTL level)

2.1.5 Memory

Main memory for the EB860 is provided by soldered SDRAM up to 128 MB. One MB of GoldCap backed-up optional SRAM is provided for more permanent storage of application and system data. Up to 32 MB of soldered FLASH is available for ROMable operating systems and boot strap loaders. Finally, there is a 64 kBit (8 x 8 kbit) serial EEPROM connected to the I²C bus for system use, where 4 kBit are factory reserved and 60 kBit are available for the user.

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2.1.6 Monitor and Control (M/C)

Various monitor and control functions are available for use with the EB860 E²Brain™ module. Ten M/C signals are available on the System Interface for application usage. In addition, the EB860 provides a RTC, a watchdog timer, a bus error timer, clock generators, a reset controller, and variety of board control registers.

2.1.7 Test and Programming

The EB860 supports the comprehensive set of MPC8xx debugging and JTAG/BDM functionality. Interfacing for this functionality is available on the System Interface.

2.1.8 Software

The EB860 is supported by various operating systems. In addition, board support packages are available as well as the “NetBootLoader” bootstrap loader.

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2.2 Board-Level Interfacing Diagram

The following figure demonstrates the interfacing structure between the internal processing modules of the EB860 and other major EB860 module components. Where EB860 system elements have common interfacing they are grouped into a block. Interfacing common to only one element of a block is indicated with a direct connecting line. The interfacing lines are shown in white where they are on board and in black for board external interfacing.

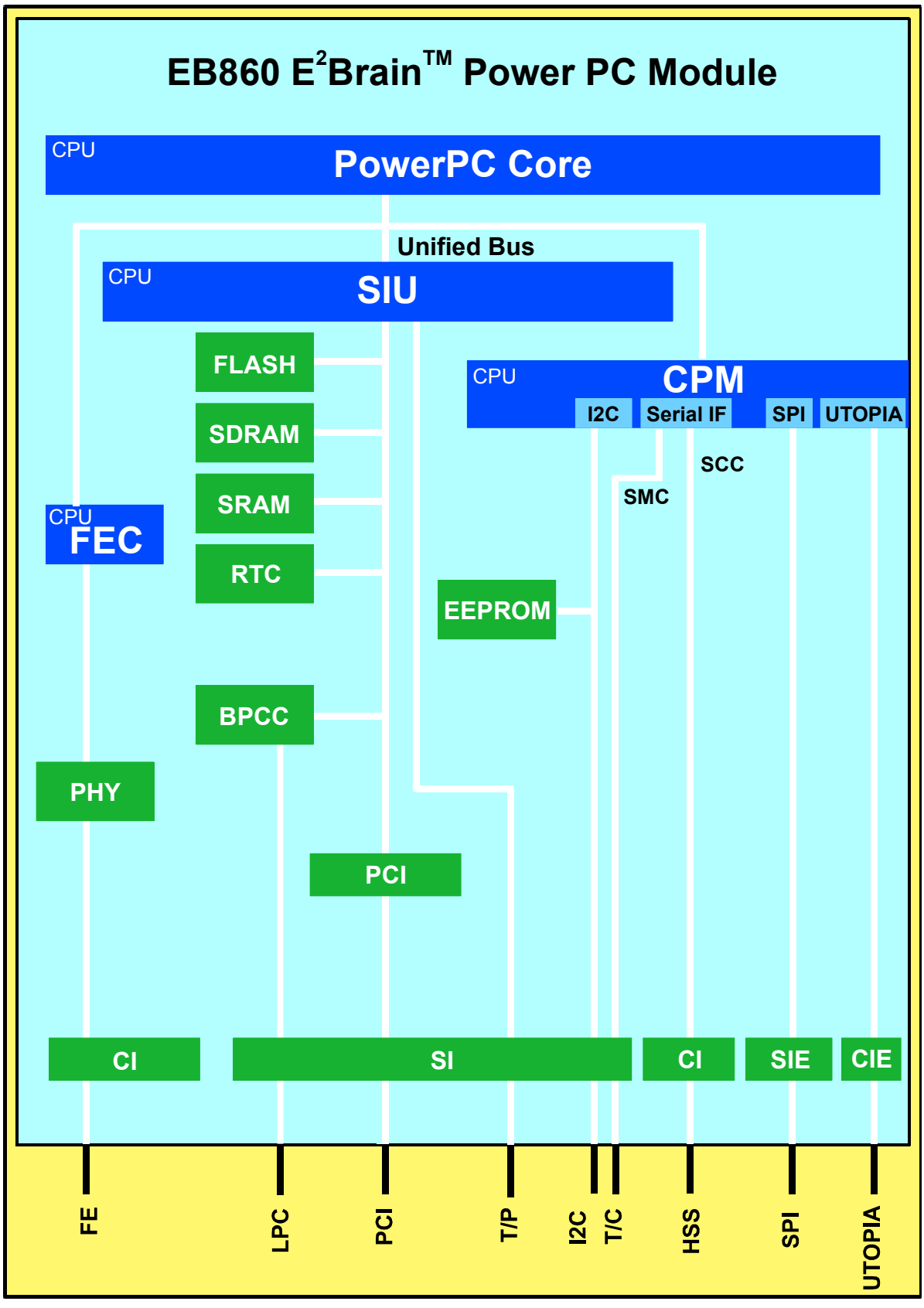
LEGEND FOR FIGURE 2-1 ON FOLLOWING PAGE

BPCC	Board Process/Communications Controller
CI	Communications Interface (CON3)
CIE	Communications Interface Extension (CON4)
FE	Fast Ethernet
FEC	Fast Ethernet Controller
HSS	High Speed Serial
I²C	Inter-Integrated Circuit
LPC	Low Pin Count
MEM IF	Memory Interface
PCI	Peripheral Component Interface
RTC	Real Time Clock
SI	System Interface (CON1)
SIE	System Interface Extension (CON2)
T/C	Terminal/Console (Serial Interface)
T/P	Test/Programming
SPI	Serial Peripheral Interface
UTOPIA	Universal Test and Operations PHY Interface for ATM

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Figure 2-1: EB860 Board Level Interfacing



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2.3 System Interfaces

As the name implies, this interface provides the basic application connection functionality required to integrate the EB860 E²Brain™ module either as a high performance core or as a dedicated, special purpose subsystem within comprehensive data processing and handling system.

The System Interface is realized using a 140-pin, HIROSE FX8C-140P-SV connector designated as CON1 (Pn1), which is designed to mate with a 140-pin, HIROSE FX8C-140S-SV connector on the EB860 carrier board. The following table provides an overview of the signal types and a brief description of the interfacing realized on this connector. The ensuing sections provide more detailed information concerning the signal specification for this interface.

Table 2-3: System Interface CON1 (Pn1) Signal Types

SIGNAL TYPE	DESCRIPTION
POWER	EB860 E²Brain™ module input power, grounds, battery backup power, PCI signaling voltage V(I/O)
MONITOR AND CONTROL (M/C)	Control signals for E²Brain™ module operation, configuration, and additional GPIO interfacing.
TEST AND PROGRAMMING (T/P)	JTAG and DEBUG signals. System programming signals
TERMINAL AND CONSOLE (T/C)	Two serial interfaces: one for connecting a terminal and one for use as a console interface
I^2C	One I^2C standard interface for low speed, serial, inter-chip communications
LPC	One LPC standard interface for (GP)IOs and simple memory interfacing
PCI	One PCI standard interface for PCI-bus interfacing

2.3.1 CON1 (Pn1) Connector Pinout

Because the E²Brain™ specification defines signal interfacing which is at the physical component level, the actual electrical characteristics of signals are for the most part different from those which are specified using accepted industry standards which apply more to unit-to-unit level signals. Only in those cases where the industry standard for such signals is at the physical component level are the characteristics of the signals specified compliant with the standard indicated, for example: PCI compliant signals.

The following table provides signal pinouts along with information concerning signal characteristics for connector CON1 (Pn1) of EB860 E²Brain™ module.

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Table 2-4: Pinout of CON1 (Pn1) Connector

PIN	SIGNAL	TYPE	SIGNAL GROUP	REMARKS
1	GND	I	POWER	
2	AUX-Power	I	POWER	Used to supply power to RTC and SRAM
3	SDA	I/O	I2C	Internal pull-up: 4.7kΩ; PB27 on MPC8xx. Note: PB27 may also have the SER_DTR3 functionality
4	SCL	I/O	I2C	Internal pull-up: 4.7kΩ; PB26 on MPC8xx. Note: PB26 may also have the SER_DTR2 functionality
5	MC6#	O	M/C	High, if Control Status Register 1 bit0 = 0; Low, if this bit is 1; can be used to drive a LED; this signal toggles during bootloader startup
6	+3.3V	I	POWER	
7	MC0	I	M/C	Debounced Reset input, active low, chip internal pull-up on MAX 704T Reset Controller
8	MC7#	O	M/C	Used for Watchdog activity LED, low if WD enabled
9	MC2	I	M/C	Reserved
10	MC1	I	M/C	Internal pull-up: 4.7kΩ; debounced, active low, NMI request, ABORT functionality during bootloader startup
11	+3.3V	I	POWER	
12	GND	I	POWER	
13	MC3	I	M/C	Internal pull-up: 4.7kΩ; debounced, active low, PFAIL functionality, indication through bit4 in the Board IRQ Pending Register
14	MC11#	O	M/C	High, if Control Status Register 1 bit1 = 0; Low if this bit is 1; can be used to drive a LED
15	MC4	I	M/C	Internal pull-up: 4.7kΩ; Boot Control functionality.
16	MC5	I	M/C	Reserved
17	MC9#	O	M/C	Open collector, internal pull-up: 4.7kΩ to PCI V(I/O); PME (Power Management Event) functionality
18	MC8	I	M/C	Internal pull-up: 4.7kΩ; leave this signal open if used in Standalone/ Master configuration; connect to GND to force Slave-Mode
19	GND	I	POWER	
20	MC10#	O	M/C	Open collector, reserved for future IREADY functionality, currently connected to GND in the BPCC
21	LPCCLK	O	LPC	
22	RESERVED			This pin must be left unconnected
23	LAD0	I/O	LPC	Internal pull-up: 4.7kΩ
24	LAD1	I/O	LPC	Internal pull-up: 4.7kΩ
25	LAD2	I/O	LPC	Internal pull-up: 4.7kΩ
26	+3.3V	I	POWER	
27	LFRAME#	O	LPC	
28	GND	I	POWER	

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Table 2-4: Pinout of CON1 (Pn1) Connector

PIN	SIGNAL	TYPE	SIGNAL GROUP	REMARKS
29	SERIRQ	I/O	LPC	Internal pull-up: 4.7kΩ
30	LAD3	I/O	LPC	Internal pull-up: 4.7kΩ
31	TER_TxD	O	T/C	TTL-Level; PB25 on MPC8xx. Note: PB25 may also have the UTP1_RxAddr3 functionality
32	RESERVED			This pin is not connected internally
33	+3.3V	I	POWER	
34	SER0_TxD	O	T/C	TTL-Level; PB21 on MPC8xx. Note: PB21 may also have the UTP1_TxAddr1 functionality
35	GND	I	POWER	
36	SER0_RxD	I	T/C	Internal pull-up: 100kΩ; input signal levels must not exceed 3.3V + 5%; PB20 on MPC8xx. Note: PB20 may also have the UTP1_TxAddr0 functionality
37	TER_RxD	I	T/C	Internal pull-up: 100kΩ; input signal levels must not exceed 3.3V + 5%; PB24 on MPC8xx. Note: PB24 may also have the UTP1_TxAddr3 functionality
38	VFLS0	O	T/P	
39	EMU_VCC	O	T/P	Provides the suitable IO voltage to an Emulation probe
40	HRESET	I	T/P	Internal pull-up: 1kΩ
41	VFLS1	O	T/P	
42	GND	I	POWER	
43	SRESET	O	T/P	Internal pull-up: 1kΩ
44	TMS	I	T/P	MPC8xx internal pull-up
45	TRST	I	T/P	
46	+3.3V	I	POWER	
47	TCK	I	T/P	Internal pull-down: 1kΩ
48	TDO	O	T/P	
49	RESERVED			This pin must be left unconnected
50	TDI	I	T/P	MPC8xx internal pull-up
51	GND	I	POWER	
52	RESERVED			This pin must be left unconnected
53	PCI-CLK-OUT-0	O	PCI	
54	V(I/O)	I	POWER	This pin defines the PCI Signaling Voltage. This pin must be connected to 5V or 3.3V according to the PCI devices on the carrier.
55	+3.3V	I	POWER	
56	PCI-CLK-IN	I	PCI	Clock input used in Agent-Mode; leave unconnected in Master-Mode
57	PCI-CLK-OUT-1	O	PCI	
58	GND	I	POWER	

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Table 2-4: Pinout of CON1 (Pn1) Connector

PIN	SIGNAL	TYPE	SIGNAL GROUP	REMARKS
59	PCI-RST#	I/O	PCI	Output in PCI master mode, Input in PCI slave mode
60	PCI-CLK-OUT-2	O	PCI	
61	INTA#	I/O	PCI	Master Mode: internal pull-up: 2.7kΩ, input; Slave Mode: no pull-up, output
62	INTC#	I	PCI	Master Mode: internal pull-up: 2.7kΩ; Slave Mode: no pull-up
63	INTB#	I	PCI	Master Mode: internal pull-up: 2.7kΩ; Slave Mode: no pull-up
64	GNT#0	I/O	PCI	Internal pull-up: 4.7kΩ
65	INTD#	I	PCI	Master Mode: internal pull-up: 2.7kΩ; Slave Mode: no pull-up
66	+3.3V	I	POWER	
67	GND	I	POWER	
68	GNT#1	O	PCI	
69	AD31	I/O	PCI	
70	GNT#2	O	PCI	
71	AD29	I/O	PCI	
72	REQ#0	I/O	PCI	Master Mode: internal pull-up: 2.7kΩ; Slave Mode: no pull-up
73	AD27	I/O	PCI	
74	REQ#1	I	PCI	Master Mode: internal pull-up: 2.7kΩ; Slave Mode: no pull-up
75	+3.3V	I	POWER	
76	GND	I	POWER	
77	AD25	I/O	PCI	
78	REQ#2	I	PCI	Master Mode: internal pull-up: 2.7kΩ; Slave Mode: no pull-up
79	C/BE3#	I/O	PCI	
80	AD30	I/O	PCI	
81	AD23	I/O	PCI	
82	AD28	I/O	PCI	
83	GND	I	POWER	
84	AD26	I/O	PCI	
85	AD21	I/O	PCI	
86	AD24	I/O	PCI	
87	V(I/O)	I	POWER	This pin defines the PCI Signaling Voltage. This pin must be connected to 5V or 3.3V according to the PCI devices on the carrier.
88	+3.3V	I	POWER	
89	AD19	I/O	PCI	
90	IDSEL	I/O	PCI	Leave unconnected in Master-Mode; IDSEL input in Agent-Mode
91	AD17	I/O	PCI	

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Table 2-4: Pinout of CON1 (Pn1) Connector

PIN	SIGNAL	TYPE	SIGNAL GROUP	REMARKS
92	GND	I	POWER	
93	C/BE2#	I/O	PCI	
94	AD22	I/O	PCI	
95	+3.3V	I	POWER	
96	AD20	I/O	PCI	
97	IRDY#	I/O	PCI	Master Mode: internal pull-up: 2.7kΩ; Slave Mode: no pull-up
98	AD18	I/O	PCI	
99	DEVSEL#	I/O	PCI	Master Mode: internal pull-up: 2.7kΩ; Slave Mode: no pull-up
100	AD16	I/O	PCI	
101	GND	I	POWER	
102	FRAME#	I/O	PCI	Master Mode: internal pull-up: 2.7kΩ; Slave Mode: no pull-up
103	PCI-X-CAP	I/O	PCI	Reserved for future PCI-X functionality; currently connected to GND in the BPCC
104	GND	I	POWER	
105	LOCK#	I/O	PCI	Master Mode: internal pull-up: 2.7kΩ; Slave Mode: no pull-up
106	TRDY#	I/O	PCI	Master Mode: internal pull-up: 2.7kΩ; Slave Mode: no pull-up
107	PERR#	I/O	PCI	Master Mode: internal pull-up: 2.7kΩ; Slave Mode: no pull-up
108	STOP#	I/O	PCI	Master Mode: internal pull-up: 2.7kΩ; Slave Mode: no pull-up
109	SERR#	I/O	PCI	Master Mode: internal pull-up: 2.7kΩ; Slave Mode: no pull-up
110	+3.3V	I	POWER	
111	GND	I	POWER	
112	PAR	I/O	PCI	
113	C/BE1#	I/O	PCI	
114	AD15	I/O	PCI	
115	AD14	I/O	PCI	
116	V(I/O)	I	POWER	This pin defines the PCI Signaling Voltage. This pin must be connected to 5V or 3.3V according to the PCI devices on the carrier
117	AD12	I/O	PCI	
118	AD13	I/O	PCI	
119	AD10	I/O	PCI	
120	AD11	I/O	PCI	
121	+3.3V	I	POWER	
122	AD9	I/O	PCI	
123	M66EN	I/O	PCI	Reserved for future 66 MHz PCI functionality; currently connected to GND in the BPCC
124	GND	I	POWER	

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Table 2-4: Pinout of CON1 (Pn1) Connector

PIN	SIGNAL	TYPE	SIGNAL GROUP	REMARKS
125	AD8	I/O	PCI	
126	C/BE0#	I/O	PCI	
127	AD7	I/O	PCI	
128	AD6	I/O	PCI	
129	AD5	I/O	PCI	
130	+3.3V	I	POWER	
131	GND	I	POWER	
132	AD4	I/O	PCI	
133	AD3	I/O	PCI	
134	AD2	I/O	PCI	
135	AD1	I/O	PCI	
136	AD0	I/O	PCI	
137	ACK64#	I/O	PCI	Master Mode: internal pull-up 2.7kΩ; Slave Mode: no pull-up, signal not used on this board
138	REQ64#	I/O	PCI	Master Mode: internal pull-up: 2.7kΩ; Slave Mode: no pull-up, signal not used on this board
139	+3.3V	I	POWER	
140	GND	I	POWER	



Warning!

The signal levels on the I^2C, T/C and T/P signal groups receive lines must not exceed 3.3V. Transients and signal levels higher than 3.3V may damage the board.

2.3.2 Power Interface

For the EB860 E²Brain™ module, a single power supply voltage of 3.3 VDC is specified. The following table summarizes the power specifications.

Table 2-5: EB860 Power Interface Requirements

VOLTAGE	DESCRIPTION
+ 3.3 VDC	Input voltage tolerance: +5% to -3% Supply voltage ripple: maximum 100 mV peak-to-peak
GND	Ground voltage reference input
AUX-Power	Optional auxiliary power input for battery backup of RTC and SRAM; input voltage must be 2.5V =< AUX-Power =< 3.6V
V(I/O)	PCI signalling voltage selection. Requires 5V if a connected PCI device on carrier is a 5V only PCI device, otherwise 3.3V.

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2.3.3 Monitor and Control Interface

This interface is comprised of a set of twelve IO signals which can be used to facilitate system integration.

The following table provides a listing of Monitor and Control signals along with a brief description.

Table 2-6: Monitor and Control Interface Signal Description

SIGNAL	DESCRIPTION
MC0	Input, RESET push button switch (low active), debounced
MC1	Input, ABORT push button switch (low active), non-maskable interrupt request, debounced
MC2	Input, not used on EB860
MC3	Input, FAL, power supply failure, low active, debounced
MC4	Input, used as boot control signal on the EB860; low = boot from LPC, high or open = boot from onboard flash
MC5	Input, not used on EB860
MC6#	Output, LED1, RUN or general purpose LED
MC7#	Output, LED2, WD_LED on when Watchdog enabled
MC8	Input, AGENT, low = Agent Mode, high or open = Master Mode
MC9#	Output, PME from QSPAN II PCI chip (Open Drain output)
MC10#	Output, IREADY, in PCI AGENT Mode; Input, IREADY, in Master Mode, reserved for future use, connected to GND
MC11#	Output, LED3, general purpose LED

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2.3.4 Test and Programming Interface

The Test and Programming interface supports JTAG/DEBUG and ISP operations. This interface can be used for connecting hardware emulators and debuggers (e.g. BDM), and for “in system programming” (ISP) of programmable hardware as well as in system testing (JTAG). It is comprised of a set of ten signals whereby some are common to all three interfaces and some are dedicated to only one.

The following table provides a listing of the Test and Programming interface signals and a brief description.

Table 2-7: Test and Programming Interface Signal Description

SIGNAL	DESCRIPTION
TCK	Test Clock in for JTAG/ISP and emulator/debugger
TDI	Test Data In for JTAG/ISP and emulator/debugger
TDO	Test Data Out JTAG/ISP and emulator/debugger
TMS	Test Mode Select, input for JTAG/ISP and emulator/debugger
TRST	Test Reset, input for JTAG/ISP and emulator/debugger
HRST	Hard Reset, emulator/debugger hard reset In
SRST	Soft Reset, emulator/debugger soft reset Out
VFLS0	Status Output of BDM emulator
VFLS1	Status Output of BDM emulator
EMU VCC	Reference Voltage of the JTAG/DEBUG core

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2.3.5 Terminal and Console Interface

The EB860 provides two serial interfaces for supporting a terminal port and a low speed communications interface (console) for firmware updating. These MPC8xx SMC channel interfaces are two signals wide and provide the standard UART protocol with XON/XOFF handshake protocol.

The following table provides a listing of the Terminal and Communications interface signals and a brief description.

Table 2-8: Terminal and Console Interface Signal Description

SIGNAL	DESCRIPTION
TxD1, TxD2	Serial Transmit Data outputs, channel 1 and 2
RxD1, RxD2	Serial Receive Data signal inputs, channel 1 and 2



Note...

The corresponding serial signals on the EB860 are TTL logic level signals.

Therefore, the transceivers for RS232 must be provided by the carrier board.



Warning!

The signal level on the receive lines must not exceed 3.3V. Transients and signal levels higher than 3.3V may damage the board.

2.3.6 I^2C Interface

The EB860 E²Brain™ module provides one I^2C serial interface for supporting direct interfacing EB860 and carrier board devices. This interface is two signals wide and fully supports the I^2C specification.

The following table provides a listing of the I^2C interface signals and a brief description.

Table 2-9: I^2C Interface Signal Description

SIGNAL	DESCRIPTION
SCL	Serial Clock Line
SDA	Serial Data line



Note...

The onboard mounted I^2C user EEPROM is hardcoded to address 0 on the I^2C bus. For this reason, additional devices connected to the I^2C interface have to start with address 1 or higher.

The first 4 kBit of the 64 kBit device are factory reserved and should not be used for user data.



Warning!

The signal level on the receive lines must not exceed 3.3V. Transients and signal levels higher than 3.3V may damage the board.

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2.3.7 LPC Interface

One Low Pin Count (LPC) interface for supporting simple IOs, simple static memory devices, and IO controllers is available with the EB860.

The controller is completely integrated in the BPCC and offers an 8-bit data access port to devices which use LPC I/O or memory access protocols. I/O and memory are selected using different address spaces.

The I/O address space is 64 kByte in size, whereas the memory area offers 16 MByte address space. The LPC interface is mapped into the MPC8xx address space. DMA, however, is not supported by this interface.

As a further part of the LPC interface, a serial IRQ controller is also implemented in the BPCC, controlling and collecting the serial LPC IRQ´s and converting and processing them to IRQ´s for the CPU. The serial IRQ controller is realized according to the “serialized IRQ support for PCI systems” specification, Rev. 6.0, Sept. 1 1995.

The following table provides a listing of the LPC interface signals and a brief description.

Table 2-10:LPC Interface Signal Description

SIGNAL	DESCRIPTION
LAD[0:3]	Multiplexed Command, Address, and Data lines
LFRAME#	Indicates start of a new cycle, termination of broken cycle
LPCCLK	33 MHz clock
SERIRQ	Serialized IRQ, optional for peripherals that need interrupt

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2.3.8 PCI Interface

In contrast to all other PCI based modules, the EB860 is capable of both PCI Master mode and PCI Agent mode. PCI agent mode can be selected by setting the AGENT signal on the system interface to Low.

In PCI Master mode mode, the EB860 operates as the host, initializing and controlling up to three PCI devices on the carrier, whereas, in the agent mode, the EB860 itself operates as a PCI target.

The following table identifies the EB860 PCI bus signals and provides a short description of each signal.

Table 2-11: PCI Interface Signal Description

SIGNAL	DESCRIPTION
AD [0:31]	PCI multiplexed address and data bus
INT [A, B, C, D]#	PCI interrupt requests
C/BE [0:3]#	PCI multiplexed bus command and byte enable
IRDY#	Initiator Ready indicates the current bus master is ready to complete the current data phase.
TRDY#	Target Ready indicates the selected device is ready to complete the current data phase.
PCI-RST#	PCI Reset signal, is also used for LPC devices and other devices on the carrier board.
PCI-CLK-OUT- [1:3]	PCI clock Outputs for up to 3 external bus PCI devices. All PCI signals except PCI_RST#, and INT [A, B, C, D] # are sampled on the rising edge. (Consider routing guidelines for Carrier board)
FRAME#	Indicate the beginning and duration of a PCI access.
STOP#	Indicates the target is requesting the master to stop the current transaction
DEVSEL#	Device select generated by the target when cycle refers to its own address.
REQ [0:2]#	PCI Arbiter requests
GNT [0:2]#	PCI Arbiter grants
PAR	Calculated/Checked Parity
PERR#	Parity Error
LOCK#	PCI Lock resource signal, not used on EB860. Master mode: termination with Pull Up Agent mode: no termination with Pull Up
SERR#	System Error
REQ64#	PCI request for a 64-bit access, not used on EB860. Master mode: termination with Pull Up Agent mode: no termination with Pull Up
ACK64#	PCI grant for a 64-bit access, not used on EB860. Master mode: termination with Pull Up Agent mode: no termination with Pull Up
PCI-CLK-IN	PCI clock input, used in agent mode
AGENT	PCI-agent mode logic input, 0 -> PCI agent mode, 1 -> system controller



Note...

The PCI interface on the EB860 is limited - no external PCI bus mastering (e.g. DMA transfers) to the onboard SDRAM is supported.

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2.4 System Interface Extension

The System Interface Extension is realized using an 80-pin, HIROSE FX8C-80P-SV connector designated as CON2 (Pn2), which is designed to mate with an 80-pin, HIROSE FX8C-80S-SV connector on the EB860 carrier board. This connector is used to provide CPU architecture specific system interfaces.

In the case of the EB860, an SPI interface is made available on the System Interface Extension. The following sections provide further information concerning the SPI interfacing.

2.4.1 SPI Interface

The table provides summary of the SPI signal implemented on the System Interface Extension connector.

Table 2-12:SPI Interface Signals

SIGNAL	DESCRIPTION
SPI_CLK	SPI bus clock signal
SPI_TXD	SPI output data
SPI_RXD	SPI input data
SPI_CS0	SPI chip select 0
SPI_CS1	SPI chip select 1
SPI_CS2	SPI chip select 2



Note...

The SPI interface on the EB860 is implemented as master interface, which means that only SPI slave devices can be connected to the system interface extension.



Warning!

The signal level on the SPI receive/RXD line must not exceed 3.3V. Transients and signal levels higher than 3.3V may damage the board.

The table on the following page provides pinout information for CON2 (Pn2) for the SPI interface.

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Table 2-13:Pinout of CON2 (Pn2) Connector

PIN	SIGNAL	REMARKS
1	GND	
2	NC	
3	NC	
4	NC	
5	NC	
6	+3.3V	
7	+3.3V	
8	NC	
9	NC	
10	NC	
11	NC	
12	GND	
13	GND	
14	NC	
15	NC	
16	NC	
17	NC	
18	+3.3V	
19	GND	
20	NC	
21	NC	
22	NC	
23	NC	
24	GND	
25	GND	
26	NC	
27	NC	
28	NC	
29	NC	
30	GND	
31	+3.3V	
32	NC	
33	NC	
34	NC	
35	NC	

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Table 2-13:Pinout of CON2 (Pn2) Connector

PIN	SIGNAL	REMARKS
36	+3.3V	
37	GND	
38	NC	
39	NC	
40	NC	
41	NC	
42	GND	
43	V(I/O)	This pin defines the PCI signaling voltage. This pin must be connected to 5V or 3.3V according to the PCI devices on the carrier.
44	NC	
45	NC	
46	NC	
47	NC	
48	GND	
49	+3.3V	
50	NC	
51	NC	
52	NC	
53	NC	
54	GND	
55	GND	
56	NC	
57	NC	
58	NC	
59	NC	
60	+3.3V	
61	GND	
62	SPI_CLK	SPI output clock from MPC8xx (PB30)
63	SPI_TXD	SPI output data from MPC8xx (PB29)
64	SPI_CS0	General purpose I/O port B bit15 (PB15) of MPC8xx used as CS0 on SPI bus. Note: PB15 may also have the UTP1_TxClav functionality
65	SPI_RXD	SPI input data to MPC8xx (PB28)
66	GND	
67	SPI_CS1	General purpose I/O port B bit14 (PB14) of MPC8xx used as CS1 on SPI bus. Note: PB14 may also have the UTP1_RxAddr2 functionality

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Table 2-13:Pinout of CON2 (Pn2) Connector

PIN	SIGNAL	REMARKS
68	SPI_CS2	Internal pull-up: 4.7 kΩ; general purpose I/O port B bit22 (PB22) of MPC8xx used as CS2 on SPI bus. Note: PB22 may also have the UTP1_TxAddr4 functionality or the internal DMA_ACK functionality for the QSPAN II (DMA_REQ signal connected to PC14 of MPC8xx)
69	NC	
70	NC	
71	+3.3V	
72	NC	
73	NC	
74	NC	
75	NC	
76	GND	
77	NC	
78	NC	
79	NC	
80	NC	

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2.5 Communications Interface

The Communications Interface Connector CON3 (Pn3), is used to provide a set of standard communications interfaces. In the case of the EB860, there are two types of interfaces provided: four high speed serial interfaces and one Fast Ethernet interface.

All of these interfaces are provided on the Communications Interface CON3 (Pn3) connector (an 80-pin, HIROSE FX8C-80P-SV connector), which is designed to mate with the 80-pin, HIROSE FX8C-80S-SV connector on the EB860 carrier board.

The following table provides pinout information for CON3 (Pn3).

Table 2-14:Pinout of CON3 (Pn3) Connector

PIN	SIGNAL	REMARKS
1	GND	
2	GND	
3	SER_TCLK1	PA4 on MPC8xx
4	SER_RCLK1	Internal pull-up: 100kΩ; PA7 on MPC8xx. Note: PA7 may also have the SER_DTR1 functionality
5	SER_RTS1	PB19 on MPC8xx
6	SER_CTS1	Internal pull-up: 100kΩ; PC11 on MPC8xx
7	SER_TXD1	PA14 on MPC8xx
8	SER_RXD1	Internal pull-up: 100kΩ; PA15 on MPC8xx
9	SER_DTR1	Internal pull-up: 100kΩ; PA7 on MPC8xx. Note: PA7 may also have the SER_RCLK1 functionality
10	SER_CD1	Internal pull-up: 100kΩ; PC10 on MPC8xx
11	GND	
12	SER_RCLK2	Internal pull-up: 100kΩ; per default not routed to MPC8xx
13	SER_TCLK2	PA5 on MPC8xx
14	SER_CTS2	Internal pull-up: 100kΩ; PC9 on MPC8xx
15	SER_RTS2	PB18 on MPC8xx. Note: PB18 may also have the UTP1_RxAddr4 functionality
16	SER_RXD2	Internal pull-up 100kΩ; PA13 on MPC8xx
17	SER_TXD2	PA12 on MPC8xx
18	SER_CD2	Internal pull-up: 100kΩ; PC8 on MPC8xx
19	SER_DTR2	Internal pull-up: 4.7kΩ; PB26 on MPC8xx. Note: PB26 may also have the I2C SCL functionality
20	SER_RCLK3	Internal pull-up: 100kΩ; per default not routed to MPC8xx
21	SER_TCLK3	PA3 on MPC8xx
22	GND	
23	SER_RTS3	Internal pull-up: 100kΩ; PB17 on MPC8xx. Note: PB17 may also have the UTP1_RxAddr1 functionality
24	SER_CTS3	Internal pull-up: 100kΩ; PC7 on MPC8xx

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Table 2-14:Pinout of CON3 (Pn3) Connector

PIN	SIGNAL	REMARKS
25	SER_TXD3	Internal pull-up: 100kΩ; PA10 on MPC8xx
26	SER_RXD3	Internal pull-up 100kΩ, PA11 on MPC8xx
27	SER_DTR3	Internal pull-up: 4.7kΩ; PB27 on MPC8xx. Note: PB27 may also have the I2C SDA functionality
28	SER_CD3	Internal pull-up: 100kΩ; PC6 on MPC8xx
29	SER_TCLK4	PA1 on MPC8xx
30	SER_RCLK4	Internal pull-up: 100kΩ; PA0 on MPC8xx
31	SER_RTS4	Internal pull-up: 100kΩ; PB16 on MPC8xx. Note: PB16 may also have the UTP1_RxAddr0 functionality
32	SER_CTS4	Internal pull-up: 100kΩ; PC5 on MPC8xx
33	SER_TXD4	Internal pull-up: 100kΩ; PA8 on MPC8xx
34	SER_RXD4	Internal pull-up 100kΩ; PA9 on MPC8xx
35	SER_DTR4	PB31 on MPC8xx
36	SER_CD4	Internal pull-up: 100kΩ; PC4 on MPC8xx
37	NC	
38	NC	
39	NC	
40	NC	
41	NC	
42	Reserved	Do not connect this pin externally
43	NC	
44	Reserved	Do not connect this pin externally
45	GND	
46	GND	
47	NC	
48	NC	
49	NC	
50	NC	
51	NC	
52	NC	
53	NC	
54	GND	
55	NC	
56	NC	

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Table 2-14:Pinout of CON3 (Pn3) Connector

PIN	SIGNAL	REMARKS
57	NC	
58	NC	
59	NC	
60	NC	
61	NC	
62	NC	
63	NC	
64	NC	
65	NC	
66	NC	
67	NC	
68	NC	
69	ETH1_T-	Internal termination, MDI interface, only magnetics required
70	ETH1_R-	Internal termination, MDI interface, only magnetics required
71	ETH1_T+	Internal termination, MDI interface, only magnetics required
72	ETH1_R+	Internal termination, MDI interface, only magnetics required
73	GND	
74	ETH1_SD	Reserved for future fiber interface; connected to GND
75	ETH1_LINK_LED	Internal pull-up: 4.7kΩ; Active low, drive capacity 9mA
76	NC	
77	ETH1_ACT_LED	Internal pull-up: 4.7kΩ; Active low, drive capacity 9mA
78	ETH1_SPEED_LED	Internal pull-up: 4.7kΩ; Active low, drive capacity 9mA
79	GND	
80	GND	



Warning!

The signal level on the four high speed serial interfaces receive lines must not exceed 3.3V. Transients and signal levels higher than 3.3V may damage the board.

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2.5.1 Synchronous/Asynchronous Serial Interfaces

Four serial ports are available on the EB860 E²Brain™ module. Eight signals per port are provided to realize either synchronous or asynchronous or synchronous high speed serial links interfaced using dedicated Controlling/Handshaking. Therefore, all serial communications standards like RS232, RS422, RS485, HDLC, etc. are supported.

Table 2-15:Serial Interface Signal Type and Description

SIGNAL	DESCRIPTION
TXD	Transmit data output
RXD	Receive data input
RTS	Request to send output
CTS	Clear to send input
DTR	Data terminal ready output
CD	Carrier detect input
TCLK/DSR	Transmit clock for synchronous transmissions/Data set ready input
RCLK/RI	Receive clock for synchronous transmissions/Ring indicator input



Note...

All signals are supplied at 3.3V TTL levels. Further signal conditioning via appropriate transceivers on the carrier board is required to support the respective communications standards.

When the controller is an MPC85x, only one high speed serial port is available (SCC1).

In addition, SER_DTR2 (SCC2) and SER_DTR3 (SCC3) are not available for full modem support of the SCC2 and SCC3 serial ports because PB26 (SER_DTR2) and PB27 (SER_DTR3) are used for the I2C interface.

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2.5.2 Ethernet Interface

The EB860 module provides one Fast Ethernet port (Intel LXT972A PHY) whose signals are already at copper Ethernet transmission voltage levels (physical levels) for CAT5 cabling. So the carrier board needs to add only the galvanic isolation (magnetics) function and the appropriate transmission connector type.

Additionally, for monitoring and control purposes, LED functionality is provided to indicate activity, link, and speed status information for the respective ports.

Table 2-16:Ethernet Port Signal Type and Description

SIGNAL	DESCRIPTION
ETH1_T+	Transmit pair in 10BaseT/100BaseTX configuration
ETH1_T-	
ETH1_R+	Receive pair in 10BaseT/100BaseTX configuration
ETH1_R-	
ETH1_SD	Reserved for fiber implementation (signal detect)
ETH1_ACT_LED	Indicates that link is actively transmitting or receiving data Blinking: traffic on link
ETH1_SPEED_LED	Indicates link speed Out: 10 Mb On: 100 Mb
ETH1_LINK_LED	Indicates that link is present Steady on: link is present



Note...

The dedicated LED signals are configured as open drain drivers and are therefore Low active. No further pullups are required on the carrier, because they are already provided onboard.

2.6 Communications Interface Extension

The Communications Interface Connector CON4 (Pn4), is used to provide a set of extended communications interfaces. In the case of the EB860, a UTOPIA interface is provided.

All of these interfaces are provided on the Communications Interface CON4 (Pn4) connector (an 140-pin, HIROSE FX8C-140P-SV connector), which is designed to mate with the 140-pin, HIROSE FX8C-140S-SV connector on the EB860 carrier board

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Table 2-17:Pinout of CON4 (Pn4) Connector

PIN	SIGNAL	REMARKS
1	GND	
2	GND	
3	NC	
4	NC	
5	NC	
6	NC	
7	NC	
8	NC	
9	NC	
10	NC	
11	GND	
12	GND	
13	NC	
14	NC	
15	NC	
16	NC	
17	NC	
18	NC	
19	NC	
20	NC	
21	NC	
22	GND	
23	NC	
24	NC	
25	NC	
26	NC	
27	NC	
28	NC	
29	NC	
30	NC	
31	NC	
32	NC	
33	NC	
34	GND	
35	GND	

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Table 2-17:Pinout of CON4 (Pn4) Connector

PIN	SIGNAL	REMARKS
36	NC	
37	NC	
38	NC	
39	NC	
40	NC	
41	NC	
42	NC	
43	NC	
44	NC	
45	GND	
46	GND	
47	NC	
48	NC	
49	NC	
50	NC	
51	NC	
52	NC	
53	NC	
54	NC	
55	NC	
56	GND	
57	NC	
58	NC	
59	NC	
60	NC	
61	NC	
62	NC	
63	NC	
64	NC	
65	NC	
66	GND	
67	NC	
68	NC	
69	GND	
70	NC	

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Table 2-17:Pinout of CON4 (Pn4) Connector

PIN	SIGNAL	REMARKS
71	NC	
72	NC	
73	NC	
74	NC	
75	NC	
76	UTP1_TXD/RXD0	PD15 on MPC8xx. Note: PD15 may also have the internal MII_RXD3 functionality
77	NC	
78	UTP1_TXD/RXD2	PD13 on MPC8xx. Note: PD13 may also have the internal MII_RXD1 functionality
79	UTP1_TXD/RXD1	PD14 on MPC8xx. Note: PD14 may also have the internal MII_RXD2 functionality
80	GND	
81	GND	
82	UTP1_TXD/RXD4	PD7 on MPC8xx. Note: PD7 may also have the internal MII_RX_ER functionality
83	UTP1_TXD/RXD3	PD12 on MPC8xx. Note: PD12 may also have the internal MII_MDC functionality
84	UTP1_TXD/RXD6	PD5 on MPC8xx. Note: PD5 may also have the internal MII_TXD3 functionality
85	UTP1_TXD/RXD5	PD6 on MPC8xx. Note: PD6 may also have the internal MII_RX_DV functionality
86	UTP1_RXD6	Internal pull-up: 3.3 kΩ; IPA6 on MPC8xx. Note: IPA6 may also have the internal MII_TX_ER functionality
87	UTP1_TXD/RXD7	PD4 on MPC8xx. Note: PD4 may also have the internal MII_TXD2 functionality
88	UTP1_RXD4	Internal pull-up: 3.3 kΩ; IPA4 on MPC8xx. Note: IPA4 may also have the internal MII_RX_CLK functionality
89	UTP1_RXD7	Internal pull-up: 3.3 kΩ; IPA7 on MPC8xx. Note: IPA7 may also have the internal MII_RX_DV functionality
90	GND	
91	UTP1_RXD5	Internal pull-up: 3.3 kΩ; IPA5 on MPC8xx. Note: IPA5 may also have the internal MII_RX_ER functionality
92	UTP1_RXD2	Internal pull-up: 3.3 kΩ; IPA2 on MPC8xx. Note: IPA2 may also have the internal MII_RXD1 functionality
93	UTP1_RXD3	Internal pull-up: 3.3 kΩ; IPA3 on MPC8xx. Note: IPA3 may also have the internal MII_RXD0 functionality
94	UTP1_RXD0	Internal pull-up: 3.3 kΩ; IPA0 on MPC8xx. Note: IPA0 may also have the internal MII_RXD3 functionality
95	UTP1_RXD1	Internal pull-up: 3.3 kΩ; IPA1 on MPC8xx. Note: IPA1 may also have the internal MII_RXD2 functionality
96	UTP1_RxAddr4	PB18 on MPC8xx. Note: PB18 may also have the SER_RTS2 functionality
97	UTP1_TxAddr4	Internal pull-up: 4.7 kΩ; PB22 on MPC8xx. Note: PB22 may also have the SPI_CS2 functionality, or the internal DMA_ACK functionality for the QSPAN II (DMA_REQ signal connected to PC14 of MPC8xx)
98	UTP1_RxAddr3	PB25 on MPC8xx. Note: PB25 may also have the TER_TXD functionality

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Table 2-17:Pinout of CON4 (Pn4) Connector

PIN	SIGNAL	REMARKS
99	UTP1_TxAddr3	Internal pull-up: 100 kΩ; PB24 on MPC8xx. Note: PB24 may also have the TER_RXD functionality
100	UTP1_RxAddr2	PB14 on MPC8xx. Note: PB14 may also have the SPI_CS1 functionality
101	UTP1_TxAddr2	PB23 on MPC8xx
102	GND	
103	UTP1_TxAddr1	PB21 on MPC8xx. Note: PB21 may also have the SER_TXD functionality
104	UTP1_RxAddr1	Internal pull-up: 100 kΩ; PB17 on MPC8xx. Note: PB17 may also have the SER_RTS3 functionality,
105	GND	
106	UTP1_RxAddr0	Internal pull-up: 100 kΩ; PB16 on MPC8xx. Note: PB16 may also have the SER_RTS4 functionality
107	UTP1_TxAddr0	Internal pull-up: 100 kΩ; PB20 on MPC8xx. Note: PB20 may also have the SER_RXD functionality
108	NC	
109	NC	
110	NC	
111	NC	
112	NC	
113	NC	
114	GND	
115	GND	
116	NC	
117	NC	
118	NC	
119	NC	
120	NC	
121	NC	
122	NC	
123	NC	
124	GND	
125	NC	
126	NC	
127	NC	
128	UTP1_TxClav	PB15 on MPC8xx. Note: PB15 may also have the SPI_CS0 functionality
129	UTP1_TxEnb	PD10 on MPC8xx. Note: PD10 may also have the internal MII_RXD0 functionality
130	UTP1_RxEnb	PD11 on MPC8xx Note: PD11 may also have the internal MII_TX_ER functionality

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Table 2-17:Pinout of CON4 (Pn4) Connector

PIN	SIGNAL	REMARKS
131	UTP1_TxSOC/ RxSOC	PD3 on MPC8xx. Note: PD3 may also have the internal MII_TXD1 functionality
132	UTP1_RxClav	PC15 on MPC8xx.
133	UTP1_RxSOC	Internal pull-up: 3.3 kΩ; WAIT_A on MPC8xx.
134	UTP1_RxCLK	OP0 on MPC8xx. Note: OP0 may also have the internal MII_TXD0 functionality
135	NC	
136	GND	
137	NC	
138	UTP1_TxCLK/RxCLK	PD9 on MPC8xx. Note: PD9 may also have the internal MII_TXD0 functionality
139	GND	
140	GND	



Note...

The UTOPIA interface on the EB860 is reserved for the newer CPU derivates of the MPC8xx family, such as the MPC857T, MPC859T, MPC862T or MPC866T. It is not accessible with a MPC855T or MPC860T! For further details about the signal mapping, please see chapter 2.6.1



Warning!

The signal levels on the UTOPIA receive lines must not exceed 3.3V. Transients and signal levels higher than 3.3V may damage the board.

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2.6.1 UTOPIA Interface

The UTOPIA (Universal Test & Operations PHY Interface for ATM) interface on the EB860 is optional and requires, as necessary, changes to the standard population of some resistors (routing options → special order number).

This interface is only available on CPU derivates of the MPC8xx family, which support simultaneous Ethernet and ATM, for example, the MPC857T, MPC859T, MPC862T or the MPC866T. It is not available on the MPC855T or the MPC860T or any other MPC860 derivate!

The signals provided are at 3.3V TTL voltage levels and must be adapted to the physical ATM levels through the use of appropriate transceivers on the carrier board.

The signal mapping of the UTOPIA interface on CON4 (Pn4) to the MPC8xx, which allows UTOPIA operation is as follows:

Table 2-18:Signal Mapping and Configurable Functions on the EB860

MPC8xx Signal	Configurable Signal Functions on the EB860	MPC8xx Signal	Configurable Signal Functions on the EB860
PB14	UTP1_RxAddr2, SPI_CS1	PD9	UTP1_TxCLK/RxCLK, MII_TXD0
PB15	UTP1_TxClav, SPI_CS0	PD10	UTP1_TxEnb, MII_RXD0
PB16	UTP1_RxAddr0, SER_RTS4	PD11	UTP1_RxEnb, MII_TX_ER
PB17	UTP1_RxAddr1, SER_RTS3	PD12	UTP1_TXD/RXD3, MII_MDC
PB18	UTP1_RxAddr4, SER_RTS2	PD13	UTP1_TXD/RXD2, MII_RXD1
PB20	UTP1_TxAddr0, SER_RXD	PD14	UTP1_TXD/RXD1, MII_RXD2
PB21	UTP1_TxAddr1, SER_TXD	PD15	UTP1_TXD/RXD0, MII_RXD3
PB22	UTP1_TxAddr4, SPI_CS2, QSPAN II DMA_ACK	IPA0	UTP1_RXD0, MII_RXD3
PB23	UTP1_TxAddr2	IPA1	UTP1_RXD1, MII_RXD2
PB24	UTP1_TxAddr3, TER_RXD	IPA2	UTP1_RXD2, MII_RXD1
PB25	UTP1_RxAddr3, TER_TXD	IPA3	UTP1_RXD3, MII_RXD0
PC15	UTP1_RxClav	IPA4	UTP1_RXD4, MII_RX_CLK
PD3	UTP1_TxSOC/RxSOC, MII_TXD1	IPA5	UTP1_RXD5, MII_RX_ER
PD4	UTP1_TXD/RXD7, MII_TXD2	IPA6	UTP1_RXD6, MII_TX_ER
PD5	UTP1_TXD/RXD6, MII_TXD3	IPA7	UTP1_RXD7, MII_RX_DV
PD6	UTP1_TXD/RXD5, MII_RX_DV	OP0	UTP1_RxCLK, MII_TXD0
PD7	UTP1_TXD/RXD4, MII_RX_ER	WAIT_A	UTP1_RxSOC

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The port D (PDxx) signals of the MPC8xx are used as MII signals for the onboard Ethernet PHY in the event the UTOPIA interface is not used with the EB860. If Ethernet and UTOPIA (simultaneous operation) is used, then the port D signals of the CPU are configured to work as UTOPIA data bus signals and the IPAx, OP0 and only onboard routed signals of the MPC8xx provide the MII signals. If a UTOPIA interface with separate transmit and receive data interfaces (split bus mode) is required, the Ethernet interface is no longer accessible and the WAIT_A signal works as the UTP1_RxSOC signal.



Warning!

The signal level of the receive lines must not exceed 3.3V. Transients and signal levels higher than 3.3V may damage the board.



Note...

For a detailed description of the UTOPIA interface implementation inside the CPU, please refer to the respective MPC8xx documentation. Not all MII signals are routed to the CON4 (Pn4) connector.

2.7 Monitor and Control (M/C)

Monitor and Control functions are divided essentially into Pre-operation and Operation. Pre-operation M/C deals with board configuration and system requirements. Operation M/C covers direct operational interfaces. For further information regarding Monitor and Control functions, refer to chapters 2.3.3 and chapter 4.

2.7.1 Pre-Operation M/C

Pre-operation M/C is a direct function of the application and the system requirements. These requirements dictate the EB860 configuration as well as the overall system integration. Overall system integration and compliance with its requirements is beyond the scope of this manual.

2.7.2 Operation M/C

Operation M/C is primarily a function of the EB860 driver software and the application. M/C signals are available and if implemented as part of the application the operator as well as application software has access to these functions.

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Chapter 3

Installation

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3. Installation

The EB860 has been designed for easy installation. However, the following standard precautions, installation procedures, and general information must be observed to ensure proper installation and to preclude damage to the board or injury to personnel.

3.1 Hardware Installation

The product described in this manual may only be mounted on an appropriate E²Brain™ carrier board which is specifically designed for this E²Brain™ module.

3.1.1 Safety Requirements

The module must be securely fastened to the carrier board using the mounting standoffs and screws provided with the module.

In addition the following electrical hazard precautions must be observed.



Caution, Electric Shock Hazard!

Ensure that the system main power is removed prior to installing or removing this board. Ensure that there are no other external voltages or signals being applied to this board or other boards within the system. Failure to comply with the above could endanger your life or health and may cause damage to this board or other system components including process-side signal conditioning equipment.



ESD Equipment!

This Kontron board contains electrostatically sensitive devices. Please observe the following precautions to avoid damage to your board:

Discharge your clothing before touching the assembly. Tools must be discharged before use.

Do not touch any on board components, connector pins, or board conductive circuits.

If working at an anti-static workbench with professional discharging equipment, ensure compliance with its usage when handling this product.

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3.1.2 Installation Procedures

To install this E²Brain™ module proceed as follows:

1. Ensure that the safety requirements indicated in chapter 3.1.1 are observed.



Warning!

Failure to comply with the instruction below may cause damage to the board or result in improper system operation. Please refer to chapters 4 and 5 for configuration information.

2. Ensure that the board is properly configured for operation before installing.



Note...

Care must be taken when applying the procedures below to ensure that when the board is inserted it is not damaged through contact with other boards in the system.

3. To install the E²Brain™ module perform the following:
   1. Orient the E²Brain™ module as appropriate to the carrier board and engage it with the carrier board.
   2. Fasten all mounting screws provided with the E²Brain™ module ensuring that the standoffs are also properly fastened.
   3. As appropriate, install the carrier board in the application system.

3.1.3 Removal Procedures

To remove this module proceed as follows:

1. Ensure that the safety requirements indicated in chapter 3.1.1 are observed.



Warning!

Care must be taken when applying the procedures below to ensure that when the board is removed it is not damaged through contact with other boards in the system.

2. Disconnect any interfacing cable(s) that may be connected to the module.
3. Remove all module mounting screws.
4. Disengage the module from the carrier board.
5. Reinstall the module mounting screws in the module standoffs.
6. Dispose of the module as required observing applicable environmental regulations governing the handling and disposition of this type of product.

3.2 Software Installation

Installation of the EB860 driver software is a function of the application operating system. For further information refer to the appropriate software documentation.

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Chapter 4

Configuration

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4. Configuration

The following sections provide system integrators with detailed information for configuring the EB860 module for operation

4.1 Board Address Map

The following table illustrates the address mapping of the EB860.

Table 4-1: Board Address Map

Address Range	Power QUICC CS	Area Name		Size	Description
0x0000 0000 - 0x3FFF FFFF	CS2	SDRAM		1 GB	Soldered SDRAM
0x4000 0000 - 0x7FFF FFFF	CS1	QSPAN2		1 GB	PCI page 1
0x8000 0000 - 0x84FF FFFF	CS4	LPCIO		80 MB	LPC I/O area
0x8500 0000 - 0x89FF FFFF	CS4	LPCMEM		80 MB	LPC memory area
0x8A00 0000 - 0x8AFF FFFF	CS4	RTC		16 MB	Real time clock
0x8B00 0000 - 0x8BFF FFFF	CS4	BCS-REG		16 MB	Board control and status registers
0x8C00 0000 - 0x8FFF FFFF	CS4	Reserved		64 MB	
0x9000 0000 - 0x9FFF FFFF	CS0	Bootjumper open	Bootjumper set	256 MB	Boot area (from soldered Flash or LPC memory) * read only
		Sold. Flash	FPGA ROM*		
0xA000 0000 - 0xAFFF FFFF	CS3	Bootjumper open	Bootjumper set	256 MB	Additional memory area * read only
		FPGA ROM*	Sold. Flash		
0xB000 0000 - 0xB7FF FFFF	CS5	Reserved		128 MB	
0xB800 0000 - 0xB8FF FFFF	CS7	SRAM		16 MB	SRAM memory area
0xB900 0000 - 0xBBFF FFFF	CS7	Reserved		48 MB	
0xBC00 0000 - 0xBCFF FFFF	CS6	QSPAN2		16 MB	QSPAN2 register
0xBD00 0000 - 0xBD00 FFFF		IMP (MPC-REG)		64 kB	IMMR register 64 kBytes resolution
0xBD01 0000 - 0xBFFF FFFF		Reserved		48 MB	
0xC000 0000 - 0xFFFF FFFF	CS1	QSPAN2		1 GB	PCI page 2

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Note...

The term “Bootjumper set” means that the dedicated monitor/control signal (MC4) from the CON1 connector is driven low from the carrier board.
“Bootjumper open” means driven high or left open.

The term “Boot from FPGA ROM” means that only the basic code is fetched, the further boot process will be performed over a connected LPC flash on the carrier (LPC memory area).

4.2 Board Control Registers

The Board Control registers may be accessed through byte-wide read and write operations.

Table 4-2: Board Control Registers

REGISTER	ADDRESS	ACCESS	
		READ	WRITE
LPC IRQ MASK Register for Interrupts 8 - 15	0x8B00 0001	X	X
LPC IRQ MASK Register for Interrupts 0 - 7	0x8B00 0003	X	X
Board-ID	0x8B00 0005	X	
Board Control/Status Register 1	0x8B00 0007	X	X
Board Control/Status Register 2	0x8B00 0009	X	X*
Board IRQ PEND Register	0x8B00 000B	X	
LPC IRQ Pending Register 8 - 15	0x8B00 000D	X	
LPC IRQ Pending Register 0 - 7	0x8B00 000F	X	
SDRAM SIZE Register	0x8B00 0011	X	X
Watchdog Control Register	0x8B00 0013	X	X
LPC Interrupt Polarity Register	0x8B00 0017	X	X
Software Compatibility ID	0x8B00 0019	X	
Board/Logic Revision Register	0x8B00 001B	X	

* note that not all bits are writable in this register

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4.2.1 LPC IRQ Mask Register 15..8

Table 4-3: LPC IRQ Mask Register 15..8

REGISTER NAME		LPC IRQ MASK REGISTER 15..8						ACCESS	
ADDRESS		0x8b00 0001						R	W
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		EN_ LPCI15	EN_ LPCI14	EN_ LPCI13	EN_ LPCI12	EN_ LPCI11	EN_ LPCI10	EN_ LPCI9	EN_ LPCI8
DEFAULT		0	0	0	0	0	0	0	0
BIT	**NAME**	**VAL**	**DESCRIPTION**						
0	EN_LPCI8	0	Disable LPC IRQ 8						
		1	Enable						
1	EN_LPCI9	0	Disable LPC IRQ 9						
		1	Enable						
2	EN_LPCI10	0	Disable LPC IRQ 10						
		1	Enables						
3	EN_LPCI11	0	Disable LPC IRQ 11						
		1	Enable						
4	EN_LPCI12	0	Disable LPC IRQ 12						
		1	Enable						
5	EN_LPCI13	0	Disable LPC IRQ 13						
		1	Enable						
6	EN_LPCI14	0	Disable LPC IRQ 14						
		1	Enable						
7	EN_LPCI15	0	Disable LPC IRQ 15						
		1	Enable						

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4.2.2 LPC IRQ Mask Register 7..0

Table 4-4: LPC IRQ Mask Register 7..0

REGISTER NAME		LPC IRQ MASK REGISTER 7..0						ACCESS	
ADDRESS		0x8b00 0003						R	W
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		EN_LPCI7	EN_LPCI6	EN_LPCI5	EN_LPCI4	EN_LPCI3	EN_LPCI2	EN_LPCI1	EN_LPCI0
DEFAULT		0	0	0	0	0	0	0	0
BIT	**NAME**	**VAL**	**DESCRIPTION**						
0	EN_LPCI0	0	Disable LPC IRQ 0						
		1	Enable						
1	EN_LPCI1	0	Disable LPC IRQ 1						
		1	Enable						
2	EN_LPCI2	0	Disable LPC IRQ 2						
		1	Enable						
3	EN_LPCI3	0	Disable LPC IRQ 3						
		1	Enable						
4	EN_LPCI4	0	Disable LPC IRQ 4						
		1	Enable						
5	EN_LPCI5	0	Disable LPC IRQ 5						
		1	Enable						
6	EN_LPCI6	0	Disable LPC IRQ 6						
		1	Enable						
7	EN_LPCI7	0	Disable LPC IRQ 7						
		1	Enable						

4.2.3 Board ID Register

The Board ID is used to identify the EB860 in a E²Brain™ system. The value for the EB860 is 0x40 which is factory set and cannot be changed.

Table 4-5: Board ID Register

REGISTER NAME	BOARD ID						ACCESS	
ADDRESS	0x8b00 0005						R	--
BIT POSITION	MSB 7	6	5	4	3	2	1	0 LSB
CONTENT	BID7	BID6	BID5	BID4	BID3	BID2	BID1	BID0
DEFAULT	0	1	0	0	0	0	0	0

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4.2.4 Control Status Registers

Table 4-6: Control Status Register 1

REGISTER NAME	CONTROL STATUS REGISTER 1						ACCESS	
ADDRESS	0x8b00 0007						R	W
BIT POSITION	MSB 7	6	5	4	3	2	1	0 LSB
CONTENT	res	res	BERRB	EN_WDG	TR_WDG	EN_BERRB	LED_R	LED_G
DEFAULT	0	0	0	0	1	1	0	BTL controlled*

BIT	NAME	VAL	DESCRIPTION
0	LED_G	0	Disabled
		1	Enables boot/general purpose LED1 on the carrier (low active)
1	LED_R	0	Disabled
		1	Enables general purpose LED3 on the carrier (low active)
2	EN_BERRB	0	Disabled
		1	Enables/Disables the onboard bus error timer. It monitors all onboard I/O cycles coupled to CS4, CS5 and CS7 of the MPC8xx (LPCIO, LPCMEM, RTC, BCS-REG, SRAM). Timeout = 15.5 µs
3	TR_WDG	0	When EN_WDG (bit4) set to 1, indicates that the Watchdog timer has not been re-triggered
		1	Triggers the watchdog timer.
4	EN_WDG	0	Disabled
		1	Enable the watchdog timer. It can only be set once and remains enabled until the next reset. In the case where the Watchdog NMI option is selected, it is reset to 0 after a timeout NMI is generated.
5	BERRB	0	Disabled
		1	Set by onboard bus error timer when timeout has been reached. Used to identify BERR caused by this timer
6	res	0	Reserved
		1	
7	res	0	Reserved
		1	



Note...

* “BTL controlled” means that during startup, the state of bit 0 is controlled by the Bootstrap Loader software. The LED is “off” (bit0 = 0), if no operating system has been detected and the LED is “on” (bit0 = 1), after bootup (blinking phase of LED) of the operating system. Afterwards, it is available as a general purpose LED.

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Table 4-7: Control Status Register 2

REGISTER NAME		CONTROL STATUS REGISTER 2						ACCESS	
ADDRESS		0x8b00 0009						R	W*
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		MASTER	BOOT	CPUSP1	CPUSP0	EN_P4	EN_P3	EN_P2	EN_P1
DEFAULT		Signal/Slot dependant	Signal depen-dant	Set during power-up	Set during power-up	0	0	0	0
BIT	**NAME**	**VAL**	**DESCRIPTION**						
0	EN_P1	0	Disable PCI INTA						
		1	Enable						
1	EN_P2	0	Disable PCI INTB						
		1	Enable						
2	EN_P3	0	Disable PCI INTC						
		1	Enable						
3	EN_P4	0	Disable PCI INTD						
		1	Enable						
4 5	CPUSP0 CPUSP1		Shows CPU/system clock speed Setting: 00: 66 MHz CPU (system clock: 33 MHz) 01: 80 MHz CPU (system clock: 40 MHz) 10: 100 MHz CPU (system clock: 50 MHz) 11: 133 MHz CPU (system clock: 66 MHz)						
6	BOOT	0	Boot from FPGA ROM / LPCMEM						
		1	Boot from onboard soldered Flash						
7	MASTER	0	PCI Master (1)/Agent (0) indication						
		1							

Note...

*Bits 4 through 7 are read only.

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4.2.5 Board IRQ Pending Register

Table 4-8: Board IRQ Pending Register

REGISTER NAME		BOARD IRQ PENDING REGISTER						ACCESS	
ADDRESS		0x8b00 000B						R	--
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		res	P_WDG	P_ABO	P_PD	P_PI4	P_PI3	P_PI2	P_PI1
DEFAULT		0	0	0	0	0	0	0	0
BIT	**NAME**	**VAL**	**DESCRIPTION**						
0	P_PI1	0	No interrupt pending						
		1	If 1, pending PCI INTA						
1	P_PI2	0	No interrupt pending						
		1	If 1, pending PCI INTB						
2	P_PI3	0	No interrupt pending						
		1	If 1, pending PCI INTC						
3	P_PI4	0	No interrupt pending						
		1	If 1, pending PCI INTD						
4	P_PD	0	No Power Down pending						
		1	If 1, pending Power Down from carrier board						
5	P_ABO	0	No Abort pending						
		1	If 1, pending Abort NMI						
6	P_WDG	0	No Watchdog NMI pending						
		1	If 1, pending Watchdog NMI (if Watchdog is previously configured to generate an NMI instead of a Reset)						
7	res	0	Reserved						
		1							

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4.2.6 LPC IRQ Pending Register 15..8

Table 4-9: LPC IRQ Pending Register 15..8

REGISTER NAME		LPC IRQ PENDING REGISTER 15..8						ACCESS	
ADDRESS		0x8b00 000D						R	--
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		P_LPCI15	P_LPCI14	P_LPCI13	P_LPCI12	P_LPCI11	P_LPCI10	P_LPCI9	P_LPCI8
DEFAULT		0	0	0	0	0	0	0	0
BIT	**NAME**	**VAL**	**DESCRIPTION**						
0	P_LPCI8	0	No interrupt pending						
		1	If 1, pending LPC IRQ8						
1	P_LPCI9	0	No interrupt pending						
		1	If 1, pending LPC IRQ9						
2	P_LPCI10	0	No interrupt pending						
		1	If 1, pending LPC IRQ10						
3	P_LPCI11	0	No interrupt pending						
		1	If 1, pending LPC IRQ11						
4	P_LPCI12	0	No interrupt pending						
		1	If 1, pending LPC IRQ12						
5	P_LPCI13	0	No interrupt pending						
		1	If 1, pending LPC IRQ13						
6	P_LPCI14	0	No interrupt pending						
		1	If 1, pending LPC IRQ14						
7	P_LPCI15	0	No interrupt pending						
		1	If 1, pending LPC IRQ15						

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4.2.7 LPC IRQ Pending Register 7..0

Table 4-10:LPC IRQ Pending Register 7..0

REGISTER NAME		LPC IRQ PENDING REGISTER 7..0						ACCESS	
ADDRESS		0x8b00 000F						R	--
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		P_LPCI7	P_LPCI6	P_LPCI5	P_LPCI4	P_LPCI3	P_LPCI2	P_LPCI1	P_LPCI0
DEFAULT		0	0	0	0	0	0	0	0
BIT	**NAME**	**VAL**	**DESCRIPTION**						
0	P_LPCI0	0	No interrupt pending						
		1	If 1, pending LPC IRQ0						
1	P_LPCI1	0	No interrupt pending						
		1	If 1, pending LPC IRQ1						
2	P_LPCI2	0	No interrupt pending						
		1	If 1, pending LPC IRQ2						
3	P_LPCI3	0	No interrupt pending						
		1	If 1, pending LPC IRQ3						
4	P_LPCI4	0	No interrupt pending						
		1	If 1, pending LPC IRQ4						
5	P_LPCI5	0	No interrupt pending						
		1	If 1, pending LPC IRQ5						
6	P_LPCI6	0	No interrupt pending						
		1	If 1, pending LPC IRQ6						
7	P_LPCI7	0	No interrupt pending						
		1	If 1, pending LPC IRQ7						

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4.2.8 SDRAM Size Register

Table 4-11: SDRAM Size Register

REGISTER NAME		SDRAM SIZE REGISTER						ACCESS	
ADDRESS		0x8b00 0011						R	W
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		res	res	res	res	res	res	RAM_SIZ1	RAM_SIZ0
DEFAULT		0	0	0	0	0	0	Set during power-up	Set during power-up
BIT	**NAME**	**VAL**	**DESCRIPTION**						
0	RAM_SIZ0	0	**SDRAM size information** **Bit** 0 0 16MB SDRAM mounted 0 1 32MB SDRAM mounted 1 0 64MB SDRAM mounted 1 1 128MB SDRAM mounted						
		1							
1	RAM_SIZ1	0							
		1							
2	res	0	Reserved						
		1							
3	res	0	Reserved						
		1							
4	res	0	Reserved						
		1							
5	res	0	Reserved						
		1							
6	res	0	Reserved						
		1							
7	res	0	Reserved						
		1							

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4.2.9 Watchdog Control Register

Table 4-12:Watchdog Control Register

REGISTER NAME		WATCHDOG CONTROL REGISTER						ACCESS	
ADDRESS		0x8b00 0013						R	W
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		res.	WD_R	WD_CCD	res.	WDT3	WDT2	WDT1	WDT0
DEFAULT		0	0	0	0	0	0	0	0

BIT	NAME	VAL	DESCRIPTION
0	WDT0	0	WDT3 WDT2 WDT1 WDT0
		1	0 0 0 0 0.5 seconds Watchdog timeout time
1	WDT1	0	0 0 0 1 1.0 seconds Watchdog timeout time
		1	0 0 1 0 1.5 seconds Watchdog timeout time
2	WDT2	0	0 0 1 1 2.0 seconds Watchdog timeout time
		1	0 1 0 0 2.5 seconds Watchdog timeout time
3	WDT3	0	0 1 0 1 3.0 seconds Watchdog timeout time
		1	0 1 1 0 3.5 seconds Watchdog timeout time
			0 1 1 1 4.0 seconds Watchdog timeout time
			1 0 0 0 4.5 seconds Watchdog timeout time
			1 0 0 1 5.0 seconds Watchdog timeout time
			1 0 1 0 5.5 seconds Watchdog timeout time
			1 0 1 1 6.0 seconds Watchdog timeout time
			1 1 0 0 6.5 seconds Watchdog timeout time
			1 1 0 1 7.0 seconds Watchdog timeout time
			1 1 1 0 7.5 seconds Watchdog timeout time
			1 1 1 1 8.0 seconds Watchdog timeout time
4	res	0	Reserved
		1	
5	WD_CCD	0	Normal Watchdog functionality
		1	Cascade mode: when Watchdog timeout occurs, an NMI will be generated, the Watchdog timer resets, the next timeout will result in a system reset (when WD_R is first set to 1)
6	WD_R	0	Causes hardware reset of system upon Watchdog timeout
		1	Causes generation of a non-maskable interrupt upon Watchdog timeout
7	res	0	Reserved
		1	

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4.2.10 LPC Interrupt Polarity Register

Table 4-13:LPC Interrupt Polarity Register

REGISTER NAME		LPC INTERRUPT POLARITY REGISTER						ACCESS	
ADDRESS		0x8b00 0017						R	W
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		res.	res.	res.	res.	LPC_POL4	LPC_POL3	LPC_POL2	LPC_POL1
DEFAULT		0	0	0	0	1	1	1	1
BIT	**NAME**	**VAL**	**DESCRIPTION**						
0	LPC_POL1	0 1	LPC interrupt 3..0 polarity 1: high active 0: low active						
1	LPC_POL2	0 1	LPC interrupt 7..4 polarity 1: high active 0: low active						
2	LPC_POL3	0 1	LPC interrupt 11..8 polarity 1: high active 0: low active						
3	LPC_POL4	0 1	LPC interrupt 15..12 polarity 1: high active 0: low active						
4	res	0 1	Reserved						
5	res	0 1	Reserved						
6	res	0 1	Reserved						
7	res	0 1	Reserved						

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4.2.11 Software Compatibility ID Register

The Software Compatibility ID will signal to the software when differences in hardware require different handling by the software. It starts with the value 0x00 and will be incremented with each change in hardware (software sensitive only). This register is set at the factory and is for use only by the boot strap loader “NetBootLoader” and the BSP software, and, as such, is not user relevant.

Table 4-14:Software Compatibility ID Register

REGISTER NAME	SOFTWARE COMPATIBILITY ID REGISTER						ACCESS	
ADDRESS	0x8B00 0019						R	
BIT POSITION	MSB 7	6	5	4	3	2	1	0 LSB
CONTENT	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0
DEFAULT	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a

4.2.12 Board Logic / Revision Register

The Board Revision Register may be used to identify the hardware (BRn) and logic status of the board by the software (LRn). It is set at the factory and starts with the value 0x00 for the initial board prototypes and will be incremented with each redesign / logic release.

Table 4-15:Board Logic / Revision Register

REGISTER NAME	BOARD LOGIC/REVISION REGISTER						ACCESS	
ADDRESS	0x8B00 001B						R	
BIT POSITION	MSB 7	6	5	4	3	2	1	0 LSB
CONTENT	LR3	LR2	LR1	LR0	BR3	BR2	BR1	BR0
DEFAULT	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a

4.3 EEPROM

Access to the onboard EEPROM is effected via the I2C bus of the MPC8xx. The EEPROM uses the hard-coded I2C address 0x0. Additional devices connected to this I2C bus on the carrier must start with address 0x1 or higher.

The first four kBit of the 64 kBit device are reserved for factory use. The other 60 kBit are available for the user.

For more detailed information please refer to the manuals for the MICROCHIP 24LC64 or Catalyst 24WC64, and the MOTOROLA MPC860 (I2C bus).

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4.4 IRQ Routing

The different processor external IRQ sources are collected and routed to the CPU in the following manner.

Table 1-16: IRQ Routing

MPC8xx Interrupt	Interrupt Source
IRQ0	Abort, Watchdog option
IRQ1	Power Fail from carrier
IRQ2	QSPAN II PCI bridge
IRQ3	Reserved
IRQ4	LPC IRQ's: 15...0
IRQ5	Reserved
IRQ6	PCI IRQ's: INTA - D
IRQ7	Not usable - used as Ethernet Clock



Note...

IRQ1 is the highest priority maskable level. IRQ0 is not maskable.



Note...

In the case of a PCI slave configuration of the EB860, a PCI interrupt can be generated with the help of the QSPAN II registers (for more details refer to the Tundra QSPAN II data sheet). On the EB860 the QSPAN II PINT# signal is routed to the BPCC, which generates an INTA signal to the PCI bus host.

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Chapter 5

NetBootLoader

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5. NetBootLoader

This E²Brain™ module is delivered with the NetBootLoader software already programmed into the onboard soldered Flash memory. The NetBootLoader itself is a software utility which initializes the module for operation before turning control over to either an application or to an operator. This software also provides the capability to monitor and control the operation of the NetBootLoader itself, display system status information, to program executable code and data to the Flash memory, and to load and start application software.

To attain full operational capability, the NetBootLoader FLASH must be programmed by the user with application software. Once the application has been programmed to Flash memory, the NetBootLoader will support the complete boot operation. The following chapters describe the functioning of the NetBootLoader and how to program the Flash memory.



Note...

The following description assumes a standard CPU board with appropriate hardware. In the event such hardware is not available, disregard the text that applies to the missing hardware and proceed as appropriate.

5.1 General Operation

Upon power on or a system reset, the NetBootLoader is started. The CPU board is configured for operation and control is either passed to an application or an operator. In the event a valid application has been programmed into the Flash memory and no operator intervention takes place, the application is copied from FLASH into SDRAM and control is passed to the application. If the NetBootLoader does not find a valid application or operator intervention has occurred, control is passed to the operator. The operator now has control to determine the system status, make configuration changes, read or program the Flash memory, or to restart or shut down the system.

The operator command interfacing with the NetBootLoader is accomplished either via the TERM serial port or the Ethernet port. During the boot operation a command interpreter is started which allows the operator to input commands to the NetBootLoader. Prior to interfacing via the Ethernet port the network must be configured. This is done via the TERM port.

5.2 NetBootLoader Interfaces

There are four possibilities to interface with the NetBootLoader:

- Via the MC1 (Abort) signal
- Via the TERM serial interface
- Via the SER0 serial interface
- Via the Ethernet interface

Gaining access to the NetBootLoader is a function of the contents of the Flash memory and the “BootWaitTime” setting. If there is no valid application programmed into the Flash memory, the boot operation automatically terminates after the module has been initialized and control is passed to the command interpreter. If there is a valid application in the Flash memory the boot operation is delayed according to the setting of the boot wait time, and the MC6 (LED1) output signal is alternately asserted indicating that the boot operation is in a wait state. During this time the operator may intervene in the boot operation either by asserting the MC1 (Abort) signal, entering the “abort” command via the TERM interface, or by performing a successful telnet login via the Ethernet interface. If the operator does not intervene, the boot operation is continued after the boot wait time has been exceeded.

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5.2.1 MC1 (Abort) Signal

The MC1 (Abort) signal is routed to the EB860 carrier board via the System Interface (CON1 connector) and, if made available on the carrier, provides the operator with the ability to directly terminate the boot operation during the boot wait time which is indicated by the alternately asserted MC6 (LED1) signal. This is the sole purpose of the MC1 (Abort) signal during the NetBootLoader operation.

5.2.2 TERM Serial Interface

The TERM serial port, if realized on the carrier board, is used to provide direct operator interfacing to the NetBootLoader. As soon as the CPU board has been initialized this port is activated and the operator may input commands. During the boot wait time the operator may terminate the boot operation and take control of the NetBootLoader. Once the boot wait time is exceeded the command interpreter is deactivated and the operator no longer has access to the NetBootLoader.

The TERM serial interface may either be directly connected to a terminal device or may interface with a terminal emulator.

5.2.3 SER0 Serial Interface

The SER0 serial port is used to provide the NetBootLoader with the ability to access Motorola S-Records for programming an application to FLASH. No command interpreter is available for this interface.

5.2.4 Ethernet Interface

The Ethernet interface provides the capability of remotely interfacing with the NetBootLoader. Prior to using this interface it is necessary to configure the NetBootLoader network settings. This is accomplished via the TERM interface. Once the network settings have been made, the remote operator has the same capabilities as with the TERM interface. During the boot wait time the operator gains control of the NetBootLoader by logging into it via the Ethernet interface. This causes the boot operation to be terminated and gives control to the remote operator.

The Ethernet interface uses the telnet protocol for operator interfacing with the NetBootLoader. In addition to the operator interface via Ethernet, the NetBootLoader also uses the Ethernet interface for ftp server access.

5.3 NetBootLoader Functions

In addition to initializing the CPU board for operation and the loading and starting of applications, the NetBootLoader provides the following operator monitor and control functions:

- NetBootLoader control
- system status monitoring
- ftp server access
- FLASH reading and programming operations
- Motorola S-Record acquisition

These functions are described in detail in the following chapters.



NOTE ...

The command title (CMD TITLE) is expressed in capital letters and is not the same as the syntax of the command. The command syntax is always written using small letters

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5.3.1 NetBootLoader Control

The NetBootLoader provides various functions for controlling the operation of the NetBoot-Loader itself as well as the setting of operational parameters. The following table provides an overview of available NetBootLoader control functions.

Table 5-1: NetBootLoader Control Commands

CMD TITLE	ALIAS	FUNCTION	REMARKS
ABORT	-	Terminate boot wait	
BW	Boot Wait	Set or display BootWaitTime	
HELP or ?	-	Display online HELP pages	
LOGOUT	-	Terminate telnet session	
NET	-	Set network parameters	Must be set before attempting telnet login
PASSWD	Password	Set telnet password	Must be set before attempting telnet login
PF	Port Format	Set serial port parameters	Used for both TERM and SER0 ports
RS	Reset	Resets system	

5.3.2 System Status Monitoring

The NetBootLoader provides various functions for monitoring the overall status of the system during the operation of the NetBootLoader. The following table provides an overview of avail-able system status monitoring functions.

Table 5-2: System Status Monitoring Commands

CMD TITLE	ALIAS	FUNCTION	REMARKS
CHECK	-	Application validation	Verifies validity of user image programmed to FLASH
INFO	-	Display system information	
MD	Memory Display	Display memory contents	Applies to all visible memory
PCI	-	Display PCI device information	
PING	-	Verify network status	
VER	Version	Display version number of NetBootLoader	

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5.3.3 ftp Server Access

The NetBootLoader provides various functions for interfacing with an ftp server. The following table provides an overview of available ftp server functions.

Table 5-3: ftp Server Commands

CMD TITLE	ALIAS	FUNCTION	REMARKS
BYE	-	Terminate session with ftp server	
CD	Change Directory	Change ftp server directory	
GET	-	Download a file from ftp server	Only for executable applications. Data buffer is target.
LOGIN	-	Login to ftp server	
LS	List Directory	List ftp server directory	Lists contents of directory.
PUT	-	Upload a file to ftp server	Data buffer is source.
PWD	Print Working Directory	Display current ftp server directory	Lists name of directory

5.3.4 FLASH Operation

The NetBootLoader provides various functions for performing operations with Flash memory. The following table provides an overview of available FLASH operation functions.

Table 5-4: FLASH Operation Commands

CMD TITLE	ALIAS	FUNCTION	REMARKS
CLONE	-	Program NetBootLoader to FLASH	Uses data buffer or socket as source
LF	Load FLASH	Program application to FLASH	Uses data buffer as source
SF	Store FLASH	Reads FLASH to data buffer	Uses data buffer as target

5.3.5 Motorola S-Records

The NetBootLoader provides one function for acquiring Motorola S-Records. The following table provides an overview of this function.

Table 5-5: Motorola S-Records Commands

CMD TITLE	ALIAS	FUNCTION	REMARKS
SL	SLoad	Download Motorola S-Records	Uses data buffer as target

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5.4 Operating the NetBootLoader

5.4.1 Initial Setup

The CPU board is delivered with the NetBootLoader already installed in the onboard soldered FLASH and is ready for operation. However, in order for the CPU board to be used in a system, application software must be made available for use. This is accomplished by programming the application also to the onboard soldered Flash memory where the NetBootLoader is located.

Upon initial power up the NetBootLoader is started automatically. As soon as the NetBootLoader has completed initialization of the CPU board, it checks to see if there is a valid application programmed in FLASH and at the same time initiates a command interpreter which the operator can access either via the TERM or telnet interfaces. If there is no valid application in memory, the NetBootLoader terminates the boot operation, and waits for operator intervention. As this is the case when the CPU board is first powered up, the operator now has the opportunity to program an application.

Prior to programming an application it may be necessary to configure the NetBootLoader or perform other functions depending on the user's application development environment or application requirements. Once this has be accomplished and the application has been programmed, the CPU board is ready for operation.

The following chapters provide information on how to set up and operate the NetBootLoader itself, initiation of the telnet interface, and how to program an application to FLASH.

5.4.2 Accessing the NetBootLoader

Initial access to the NetBootLoader can only be achieved via the TERM interface. Prior to using the telnet interface, the Ethernet parameters must be set and this can only be accomplished initially via the TERM interface. Once valid Ethernet parameters and the telnet login password have be set, the telnet interface is available for operation.

Use of the TERM interface requires either a terminal or a terminal emulator. Use of the telnet interface requires a remote telnet login to the NetBootLoader.

Availability of the command interpreter depends on the system status. If there is no valid application programmed, the command interpreter is available as long as the operator requires it. If a valid application is programmed, the command interpreter is only available for the duration of the boot wait time. If the operator requires the command interpreter for a longer time he must terminate the boot operation before the boot wait time is exceeded.

Upon initiation of the command interpreter, a prompt is sent to the TERM interface and commands may be entered. To gain access to the NetBootLoader from a remote location via Ethernet a telnet login must be performed. If the boot wait time has not been exceeded, a telnet login automatically terminates the boot operation and a command prompt is sent to the telnet remote interface.

Once the operator has control of the NetBootLoader, he may perform any required action. To continue with the operation of the CPU board, the system must either be cold started or the operator must issue a "reset" command. In either event, the NetBootLoader is restarted and the boot operation begins anew.

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5.4.3 NetBootLoader Configuration

There are several NetBootLoader commands which provide the operator with the capability to configure specific parameters which are used by the NetBootLoader for interfacing operations. These commands are:

- BW (BootWait)
- NET
- PASSWD
- PF (Port Format)

Default settings are available for all the above commands except for “net” which is dependent on the application environment.

5.4.3.1 BW

This command is used to display or set the actual boot wait time used by the NetBootLoader to delay the boot operation before proceeding with the loading and starting of an application. If this time is set too short it may only be possible to gain access to the NetBootLoader via the MC1 (Abort) signal.

The BootWaitTime value is stored in the boot section of the serial EEPROM. This section is validated with a CRC code to avoid the setting of random parameters.



Note ...

If the CRC of the boot section is not valid, changing the BootWaitTime will have no effect because the “bw” command does not validate an invalid CRC. In this case, a default timing of 5 seconds is always used.

To validate an invalid CRC, an operating system utility must be used, or, alternatively, the “-f” option of the “bw” command must be issued.



Warning !!!

Using the “bw -f” command to validate invalid entries may adversely impact the operation of the operating system.

5.4.3.2 NET

This command is used to set or display the parameters for the configuration of the Ethernet interface of the CPU board. The Ethernet interface is only available after these settings have been made. Once these settings have been made, the system must be cold started or reset for them to take effect.

5.4.3.3 PASSWD

This command is used to set the password used by the NetBootLoader for the operation of the telnet interface. No password is required for access from the TERM interface.

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5.4.3.4 PF

This command is used to set the port parameters for the TERM and SER0 serial interfaces only for the current operator session. The next system restart will cause these settings to revert to the default settings of: 9600 Baud, 8 bits per character, 1 stop bit, and no parity. This is done to preclude a system lockout when restarting due to incompatible settings.

5.4.4 telnet Login

A telnet login to the NetBootLoader is only possible during the boot wait time and only after the Ethernet network parameters have been set.

To effect a telnet login the operator performs the standard telnet login procedure during the boot wait time. The NetBootLoader responds by suspending the boot wait and requests a login password. The operator then enters a password. If the password is valid, the boot wait is terminated and the operator can now access the NetBootLoader. If the password is invalid, the telnet login procedure is terminated and the boot operation continues.

In the case of an invalid password, the login procedure may be repeated as often as required within the boot wait time. Once the boot wait time is exceeded, a telnet login is no longer possible.

5.4.5 FLASH Operations

To achieve an operable system for an application, the application software must be programmed to FLASH. The NetBootLoader supports the programming of the application to FLASH. In addition to this, it also supports the updating of the NetBootLoader itself as well as data transfer from the FLASH to the data buffer and from the data buffer to an ftp server. The following chapters provide information on performing the various types of FLASH operations.

5.4.5.1 FLASH Offsets

All FLASH is treated as one uniform FLASH, regardless of the physical addresses of the devices involved. All offsets are based from the beginning of the FLASH area. This means that 0x0 is the beginning of the first FLASH bank. The NetBootLoader itself is located at the beginning of the FLASH area and for this reason this area cannot be used for application image programming. To display an overview of the current FLASH organization use the “info” command.

If the application image is an operating system (which is the default case), it must be programmed without an offset. When such an image is programmed to FLASH, the image length and CRC information is also programmed along with the image to FLASH. This information is used by the NetBootLoader to determine the validity of the image during the boot operation. During system startup, a valid image is copied to SDRAM address 0x0 and started at offset 0x100 after the boot wait time is exceeded.

If an offset is specified, the image will be programmed exactly at this offset without adding length or CRC information. This option is intended for the storing of configuration information which is required to be located in FLASH.

5.4.5.2 Programming an Application

The application image itself must be compiled and linked to run from the SDRAM base address 0x0 of the CPU. The image must contain executable PPC code at offset 0x100 which is the usual case with ROM/Flash images.

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Gaining access to the image for programming to FLASH depends on where it is located. The NetBootLoader can access three different sources for images:

- ftp server
- Motorola S-Records
- memory within the visible address range of the CPU board

The NetBootLoader uses a single data buffer for downloading an image from an ftp server or an image as Motorola S-Records. These images must first be downloaded to the data buffer prior to being programmed to FLASH. An image located within the visible address range of the CPU board is directly accessible for programming.

To access an image located on an ftp server, the “get” command is used. To perform Motorola S-Record acquisition, the “sl” (SLoad) command is used. Once the image is in the data buffer, the FLASH is programmed using the “lf” (Load Flash) command. For an image within visible memory, the “lf” (LoadFlash) command is used to program directly to FLASH.

5.4.5.3 ftp Server Access

To gain access to an application image file stored on an ftp server the Ethernet interface is used. Images are downloaded to the data buffer using the ftp protocol. To use this interface the Ethernet parameters must first be set and then the system must be restarted. During boot wait the operator must gain control of the NetBootLoader and perform an ftp server login. After a successful login, the operator then locates the image file required and downloads it to the data buffer. As with any type of server session, the operator should logout when the session is finished.



Note ...

The commands “get” and “ls” use the same data buffer. Therefore if an “ls” command is issued after a “get” command the data buffer will be overwritten. If an “lf” command follows the “ls” the NetBootLoader refuses to program the overwritten data buffer to the FLASH.

5.4.5.4 Motorola S-Records

The NetBootLoader will also accept Motorola S-Records as an application image. The “sl”’ command accepts S1, S2 and S3 records. Operation is terminated by the appropriate S9, S8 or S7 record. Other types of records are ignored.

The checksum of every record except end records is checked. Bad records are rejected by the NetBootLoader. The address range of every record is also checked. Records which fall outside of the internal buffer are rejected.

The records must be 0-based. This means that it’s address must correspond to the address where they will be loaded in the data buffer relative to its start. If necessary, the base address can be modified with the -o option of the “sl” command.



Note ...

If the data buffer is programmed to FLASH without the -o option (program a startable image) the downloaded image is copied to RAM during startup and is executed there. For this reason application images which require to be programmed must start at the address 0x0.

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The image must start at the absolute address 0x0 and must contain executable PPC code at the absolute address 0x100. If S1 or S2 record input is preferred, please note that these records only include 16 and 24-bit wide addresses. If no switch to another record type is included it must be ensured that the code is not larger than the address range covered.



Note ...

Neither the “sl” nor “lf” command can be used to program Motorola S-Records to RAM areas.

For accessing the Motorola S-Records, both the TERM and SER0 interfaces can be used. The MC6 (LED1) signal is asserted alternately at a low rate while downloading indicating that the transfer is in progress. The transfer itself may take several minutes to complete.

Ensure that the XON/XOFF protocol is used on the host side. This is a fixed setting and cannot be changed. Additionally, ensure that the host does not stop transmission after a number of lines (e.g. OS-9: use the ‘nopause’ attribute).

The TERM and SER0 serial interface parameters can be modified with the “pf” command.

5.4.6 Updating the NetBootLoader

In addition to programming an application to FLASH, the NetBootLoader itself can be updated. The new version of the image is made available via an ftp server.

5.4.6.1 Updating With an Image Loaded Via an ftp Server

The image is downloaded in the same way as an application image (refer to chapter 5.4.5.3). The new version of NetBootLoader image is then programmed using the “clone -n” command.

5.4.7 Uploading a FLASH Area

The NetBootLoader also has the possibility to upload certain areas of the FLASH to a host using the Ethernet interface. To use this interface the Ethernet parameters must first be set and then the system must be restarted. During boot wait the operator must gain control of the NetBootLoader and perform an ftp server login. After a successful login, the operator then stores the FLASH area to be uploaded to the local data buffer using the “sf” command. Using the “put” command transfers the contents of the data buffer to the ftp server. As with any type of server session, the operator should logout when the session is finished.

5.5 Plug and Play

On the CPU board the NetBootLoader includes “Plug and Play” functionality. This ensures that the board is completely initialized and that all resources necessary for PCI devices (addresses, interrupts etc.) are assigned automatically. This important feature has the advantage that conflicts do not arise when PCI devices are added or removed. Furthermore, the operating system itself does not include the board initialization code.

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5.6 Porting an Operating System to the CPU Board

The image for the absolute address 0x0 should be linked with an entry point at the absolute address 0x100.

One should not attempt to reassign the PCI BAR registers. The assigned values should be read back and these should always be used in the drivers.

The “interrupt line” field in the PCI configuration header is initialized with the IRQ line number to which the INTA of the device is routed.

It is not necessary to rewrite the “IMMR” register in the MPC8xx as this has already been done by the NetBootLoader. The existing value should be used.

Downloaded images are never executed from the FLASH due to the fact that on the CPU board it is paged. The programmed image is always downloaded to SDRAM, the absolute address 0x0 being downloaded first. There is no configuration option available to amend this process. If it is necessary to relocate the image to another address after download, simply add a small assembly routine at the beginning of the code which will move the image to the correct address.

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5.7 Commands

The following commands are available with the NetBootLoader. Where an ellipsis (…) appears in the command syntax it means that the command is continued from the previous line. Observe any spaces that may be between the ellipsis and the remainder of the command.

ABORT

FUNCTION:	Terminate the NetBootLoader boot operation
SYNTAX:	**abort**
DESCRIPTION:	This command is used by the operator to to terminate the boot operation during the boot wait time to allow the operator to perform other NetBootLoader operations. To be asserted it must be issued during the boot wait time which is indicated by the alternating assertion of the MC6 (LED1) signal.

BW

FUNCTION:	Set or display the parameters of the boot wait function of the NetBootLoader
SYNTAX:	**bw [<time>| -f]** where: bw command <time> parameter: value: seconds 1, 2, 5, 10, 20, 50 -f option: force CRC update

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BW

DESCRIPTION:	The command “bw” displays the parameter “<time>” setting. The parameter “<time>” stipulates the waiting time in seconds that the boot operation is delayed before the application is loaded and started. No values other than these are supported. Bear in mind when setting the boot wait time that the MC6 (LED1) signal is asserted alternately at the rate of two times a second. Therefore, if the boot wait is set to 1 second the MC6 signal will only be alternately asserted two times. The option “-f” is used to force updating of the CRC value of boot section of the EEPROM. For further information refer to chapter 5.4.3.1.
USAGE:	Display setting of “<time>” parameter COMMAND / RESPONSE: **bw** **WaitTime: 20**
	Set boot wait time to 50 seconds COMMAND / RESPONSE (none): **bw 50**

BYE

FUNCTION:	Terminate an ftp server session
SYNTAX:	**bye**
DESCRIPTION:	An ftp server session which has been established with the command “login” is terminated with the command “bye”.

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CD

FUNCTION:	Change the current ftp server directory
SYNTAX:	**cd <new-path>** where: cd command <new-path> parameter: string new directory path
DESCRIPTION:	If an ftp server session has been established with the “login” command, the command “cd” is used to change the current ftp server directory. The argument “<new-path>” may be an absolute or relative path. The format depends on what the server accepts. For example, UNIX hosts require that the directory names must be entered exactly in the same case.

CHECK

FUNCTION:	Verify validity of application programmed to FLASH
SYNTAX:	**check**
DESCRIPTION:	When an application is programmed to FLASH, a CRC is performed and the results are stored in FLASH along with the application. The “check” command is used to verify that the current application image in FLASH is valid.
USAGE:	Veriy valid application is stored in FLASH COMMAND / RESPONSE: **check** **Check userimage CRC: ok**

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CLONE

FUNCTION:	Program the NetBootLoader to FLASH
SYNTAX:	**clone [-n]** where: clone command -n option: program from data buffer
DESCRIPTION:	To update the NetBootLoader itself, the command “clone” is used. The application image source for programming is the data buffer. The image must first be downloaded to the data buffer from an ftp server. To program from the data buffer, the command “clone -n” is used. The new image is checked for validity. If an image is invalid, the update is aborted. Additionally, the operation must be confirmed by typing the word “yes”. Any other or no input will cancel the operation.
USAGE:	Program NetBootLoader (normal operation) COMMAND / RESPONSE: **NetBtLd> clone -n** **clone: Fixup FLASH info from ftp buffer** **This will overwrite the current ... NetBootLoader, are you sure? [no] yes** **clone: System transferred; Start again, ... assure that Bootjumper is removed.** **NetBtLd>** Note: When responding to the overwrite query, “yes” must be spelled out. Any other response will terminate the cloning operation.

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CLONE

Program NetBootLoader (image not valid)

COMMAND / RESPONSE:

```
NetBtLd> clone -n
clone: Fixup FLASH info from ftp buffer
Image length invalid, image is damaged, abort.
NetBtLd>
```

GET

FUNCTION:	Download file from ftp server
SYNTAX:	**get <filename>** where: get — command <filename> — parameter: string name of image file to be downloaded, or path and name of image file to be downloaded
DESCRIPTION:	To download a file from the ftp server to the local data buffer, the command “get” is used. A successful ftp server login must be carried out before a file can be downloaded and the file must be in binary format. The argument “<filename>” must refer to an existing and accessible file on the server and the syntax must follow the requirements on the server, e.g. case sensitiveness. The argument may also include a path specification, if the server supports this.

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HELP or ?

FUNCTION:	Display online help pages
SYNTAX:	**help** **?**
DESCRIPTION:	This command displays the online help pages. The display of the help text varies between the different CPU's reflecting their differences. The syntax of every command and a brief description is shown. The display output pauses after every page. The output can be continued with any key. Entering a "." (period) aborts the help function.

INFO

FUNCTION:	Display system information
SYNTAX:	**info**
DESCRIPTION:	The command "info" is used to display an information summary for the running system. The CPU type, the board type, and the detected FLASH layout are displayed.

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LF

FUNCTION:	Load Flash
SYNTAX:	**`lf [-o[=]<offset> [-k]]`** **`… [-m[=]<adr> -l[=]<len>]`** where: lf command -o option: offset <offset> parameter: value: hexadecimal program to FLASH offset of ... -k option: keep retain surrounding contents -m option: memory (address) <adr> parameter: value: hexadecimal absolute address of image to be programmed -l option: length <len> parameter: value: hexadecimal length of image to be programmed
DESCRIPTION:	Without parameters, the FLASH is programmed using the contents of the data buffer. If no image is available in the data buffer, the FLASH programming is terminated. If no offset option (“-o”) is specified the image is considered to be valid and is therefore added along with CRC and length information. If the CRC is determined to be valid during the next startup, the image is copied to the absolute address 0x0 and started at 0x100 after the boot wait time has been exceeded. Normally, the local data buffer holds the image to be programmed. However, if the “-m” and “-l” parameters are specified, the image is programmed from the absolute address specified. If “<offset>” is specified, the contents are programmed exactly at this offset in FLASH. No length and no CRC information is added. The “-k” option can be specified to prevent deletion of the surrounding FLASH contents.

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LF

DESCRIPTION:	FLASH memory can only be erased sector-wise. If an image is programmed to a certain offset with the “-o” option, at least this sector (and maybe one or more of the following sectors depending on the size of the image) will be erased. The “-k” option can be used to retain the surrounding data, however, this slows down the operation significantly. To achieve fast programming of parameter images without destroying other FLASH contents, the data should be placed at a sector boundary and the sector(s) must not contain any other data or executable images. If organized this way, use of the “-k” option can be avoided. Note: The “lf” command cannot be used to program the NetBootLoader.
USAGE:	Program FLASH from data buffer and add CRC and image length COMMAND / RESPONSE (none): **`lf`**
	Program FLASH from data buffer to offset 0xF4240 COMMAND / RESPONSE (none): **`lf -o=f4240`**
	Program FLASH from visible address at 0x87000000 for length of 0x123456 COMMAND / RESPONSE (none): **`lf -m=87000000 -l=123456`**
	Program FLASH from data buffer to offset 0xF4240 and retain adjacent FLASH contents COMMAND / RESPONSE (none): **`lf -o=f4240 -k`**

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LOGIN

FUNCTION:	Initiate ftp server session
SYNTAX:	**login <ip-of-host> <username> [<password>]** where: login command <ip-of-host> parameter: value: numerical string IP address of host: nnn.nnn.nnn.nnn <username> parameter: value: string ftp server “username” <password> parameter: value: string user’s password
DESCRIPTION:	The command “login” is used to establish an ftp server session. The “<ip-of-host>” must be specified as four numbers separated by single dots. The “<password>” parameter is not necessary if the server does not request one.
USAGE:	Initiate ftp server session COMMAND / RESPONSE: **login 192.168.47.12 johndoe mypassword** (Response is dependent on the server accessed)

LOGOUT

FUNCTION:	Terminate telnet session with NetBootLoader
SYNTAX:	**logout**
DESCRIPTION:	A remote telnet session will be terminated with the command “logout”. No application is loaded and started if the session is terminated with “logout”. The NetBootLoader waits for a new session to be initiated or for a command entry from the serial console.

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LS

FUNCTION:	Display listing of the current ftp server directory
SYNTAX:	**ls**
DESCRIPTION:	To display a listing of the current ftp server directory the command “ls” is used. This command downloads the listing to the data buffer and then the listing is displayed. Any previously loaded image in the data buffer is overwritten. If an attempt is then made to program the FLASH after the “ls” command has been issued it will fail.

MD

FUNCTION:	Display visible memory
SYNTAX:	**md [<adr>]** where: md command <adr> parameter: value: hexadecimal starting address of a visible memory area
DESCRIPTION:	To display a visible memory area the command “md” is used. The first time the command “md” is issued, visible memory contents starting at the address 0x0 are displayed if no “<adr>” parameter is used. If issued again without the “<adr>” parameter, the display starts with the end address of the previous display. Data is displayed as hexadecimal 32-bit words and as ASCII dump.

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NET

FUNCTION:	Set or display the parameters for the Ethernet interface
SYNTAX:	**net [<ip-addr>][-netmask <netmask>]** **…[-gw <gateway>][-f]** where: net — command <ip-addr> — parameter: value: numerical string IP address of CPU board: nnn.nnn.nnn.nnn -netmask — option: netmask <netmask> — parameter: value: numerical string netmask of CPU board: nnn.nnn.nnn.nnn -gw — option: gateway <gateway> — parameter: value: numerical string gateway address for network: nnn.nnn.nnn.nnn -f — option: force CRC update
DESCRIPTION:	To set or display the parameters of the Ethernet interface the command “net” is used. Initially the CPU board does not have a valid Ethernet interface configuration, and, therefore, this interface is inoperable. The initial configuration must be done from the TERM interface using the command “net ... -f”. Using the “-f” option forces a CRC to be performed and stored along with the other configuration parameters in the serial EEPROM. Once the initialization of the Ethernet interface is done, the CPU board must be restarted for the parameters to take effect. Later changes to the parameters do not require the use of the “-f” option to force a CRC. This is done automatically. Only in the event that the Ethernet interface does not properly initialize, may it be necessary to re-enter the parameters using the “-f” option.

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PASSWD

FUNCTION:	Set the telnet password
SYNTAX:	**passwd [-f | -d]** where: passwd command -f option: if password is not known -d option: disable disable telnet login (remote access)
DESCRIPTION:	To set the password for telnet sessions with the NetBootLoader the command “passwd” is used. This command is interactive, meaning that after it is issued, the NetBootLoader responds with an appropriate request to the operator which must be properly acknowledged or the operation fails (refer to USAGE below). To set the password in the event it is unknown, use the option “-f”. This is can only be accomplished from the TERM interface and not from the Ethernet interface. With the option “-d”, the remote telnet login can be disabled by invalidating the password.
USAGE:	Set password COMMAND / RESPONSE: **NetBtLd> passwd** **Old Password: ***** New Password: ***** Type again : ***** NetBtLd>** (The old password must be known)
	Set password when the old password is not known COMMAND / RESPONSE: **NetBtLd> passwd** **New Password: ***** Type again : ***** NetBtLd>**

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PCI

FUNCTION:	Display PCI information
SYNTAX:	**pci**
DESCRIPTION:	The command “pci” is used to display detailed information on all detected PCI devices. The bus number, device number, function number, vendor, and device ID’s are displayed together with the configured base addresses and the assigned IRQ number.

PF

FUNCTION:	Set or display the serial port parameters (format)
SYNTAX:	**pf [<port> [<baud>][/[<bitschar>]** **…[/[<parity>][/<stops>]]]]**

where:

pf	command
<port>	parameter: string: “term” or “ser0” defines serial port to be configured
<baud>	parameter: value: numeric: “50, 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 7200, 9600, 19200, 38400, 115200” defines the baud rate for the port
<bitschar>	parameter: value: numeric: “7” or “8” defines the number of bits per character
<parity>	parameter: string: “n” (none), “o” (odd), “e” (even) defines parity to be used
<stops>	parameter: value: number: “1”, “2” defines number of stop bits

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PF

DESCRIPTION:	To set or display the operational parameters for the available serial interfaces the command “pf” is used. At startup the settings for the “TERM” and “SER0” interfaces are always set to the default values (9600/8/n/1). This is to avoid a possible system lockout. If other settings are required during operation of the NetBootLoader they may be made. If changes are made, it must be ensured that corresponding parameters are used for the operator consle. Issuing this command without parameters being specified will display the current serial port settings. Syntax-wise, no spaces are permitted between the parameters and they must be separated with a slash. Not all parameters must be specified, but the “/” characters must be present to distinguish the different parameters from each other. The sequence can be aborted after every option.
USAGE:	Set “TERM” to 300 Baud, 7 Bits/char, odd parity, and 2 stop bits COMMAND / RESPONSE (none): **`pf term 300/7/o/2`**
	Set the bits per character parameter of “SER0” to 7 COMMAND / RESPONSE (none): **`pf ser0 //7`**
	Set the stop bits parameter of “SER0” to 2 COMMAND / RESPONSE (none): **`pf ser0 ///2`**

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PING

FUNCTION:	Verify operability of the Ethernet interface
SYNTAX:	**ping <ip_addr> [-c <count>] [-s <size>]** **… [-w <wait>]** where: ping command <ip-addr> parameter: value: numerical string IP address of target: nnn.nnn.nnn.nnn -c option: count <count> parameter: value: numeric: “[n ...]n” number of packets to send -s option: size <size> parameter: value: numeric: “[n ...]n”: bytes size of packet to send -w option: wait <wait> parameter: value: numeric: “[n ...]n”: seconds wait time between packets
DESCRIPTION:	To verify the operational status of the Ethernet interface the command “ping” is used. This command tests the network connection and target server’s ability to respond. If no other parameters are specified, four requests will be sent. This can be changed with the parameter “-c”. The typical size of a ping packet can be changed with the parameter “-s” and the time between requests, which is typically one second, can be changed with the parameter “-w”. Reponses to the “ping” command are dependent on the performance of the network.
USAGE:	Send four packets COMMAND / RESPONSE: **ping 192.192.158.7**
	Send ten packets, 100 bytes long, and wait two seconds between packets COMMAND / RESPONSE: **ping 192.192.158.7 -c 10 -s 100 -w 2**

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PUT

FUNCTION:	Upload contents of the data buffer to the ftp server.
SYNTAX:	**put <filename>** where: put command <filename> parameter: string file name to be used for contents of data buffer to be uploaded
DESCRIPTION:	To upload the contents of the data buffer to a file on an ftp server, the command “put” is used. The file indicated by the parameter “<filename>” is created on the server. In the event that a file with this name already exists, its contents will be overwritten.

PWD

FUNCTION:	Display the current ftp server directory.
SYNTAX:	**pwd**
DESCRIPTION:	If a ftp connection has been established with the “login” command, the command “pwd” is used to display the complete path of the current directory on the ftp server.

RS

FUNCTION:	Reset the system
SYNTAX:	**rs**

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RS

DESCRIPTION:	To permit the operator to force a restart of the system, the command “rs” is used. This command terminates the NetBootLoader command interpreter and resets the entire system, generating a system reset with the onboard watchdog. If this command is issued over a remote telnet connection, the telnet session is terminated prior to the generation of the reset.

SF

FUNCTION:	Store FLASH contents to data buffer
SYNTAX:	**sf -o[=]<offset> -l[=]<length>** where: sf — command -o — option: offset <offset> — parameter: value: hexadecimal relative offset to start of FLASH contents to be stored to the data buffer -l — option: length <length> — parameter: value: hexadecimal length of FLASH contents to be stored to the data buffer
DESCRIPTION:	With the command “sf” a selected portion of the FLASH contents may be copied to the local data buffer, e.g. for a subsequent upload to the ftp server with the “put” command. The “<offset>” parameter refers to the relative offset within the FLASH area similar to the “lf” command. The parameter “<length>” specifies the length to store.
USAGE:	Store 64 kB of FLASH contents to the data buffer beginning at an offset of 1 MB COMMAND / RESPONSE (none): **sf -o=100000 -l=10000**

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SL

FUNCTION:	Download Motorola S-Records to data buffer
SYNTAX:	**sl [-o[=]<offset>] [-u]** where: sl command -o option: offset <offset> parameter: value: hexadecimal: unsigned offset to be subtracted from each record's address -u option: upper
DESCRIPTION:	With the command “sl” Motorola S-Records are downloaded to the data buffer and the record addresses modified accordingly as required for SDRAM operation (for copying to 0x0). The “<offset>” parameter may be used to change the record base to 0x0. The “-u” option selects the SER0 interface as source for the S-Records.
USAGE:	Download S-Records to data buffer and reduce each record’s address by 0x10000. COMMAND / RESPONSE (none): **sl -o=10000**

VER

FUNCTION:	Display version number
SYNTAX:	**ver**
DESCRIPTION:	The command “ver” displays the actual version number of the NetBootLoader.

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