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# EBC2

## E²Brain Module Carrier
## for EB405/EB425/EB8540 CPUs

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The product described in this manual is in compliance with all applied CE standards.

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## Environmental Protection Statement

This product has been manufactured to satisfy environmental protection requirements where possible. Many of the components used (structural parts, printed circuit boards, connectors, batteries, etc.) are capable of being recycled.

Final disposition of this product after its service life must be accomplished in accordance with applicable country, state, or local laws or regulations.

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## Explanation of Symbols



***CE Conformity***

This symbol indicates that the product described in this manual is in compliance with all applied CE standards. Please refer also to the section “Applied Standards” in this manual.



***Caution, Electric Shock!***

This symbol and title warn of hazards due to electrical shocks (> 60V) when touching products or parts of them. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your material.

Please refer also to the section “High Voltage Safety Instructions” on the following page.



***Warning, ESD Sensitive Device!***

This symbol and title inform that electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Please read also the section “Special Handling and Unpacking Instructions” on the following page.



***Warning!***

This symbol and title emphasize points which, if not fully understood and taken into consideration by the reader, may endanger your health and/or result in damage to your material.



***Note...***

This symbol and title emphasize aspects the reader should read through carefully for his or her own advantage.

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## For Your Safety

Your new Kontron product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new Kontron product, you are requested to conform with the following guidelines.

### High Voltage Safety Instructions



***Warning!***

All operations on this device must be carried out by sufficiently skilled personnel only.



***Caution, Electric Shock!***

Before installing your new Kontron product into a system always ensure that your mains power is switched off. This applies also to the installation of piggybacks.

Serious electrical shock hazards can exist during all installation, repair and maintenance operations with this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing work.

### Special Handling and Unpacking Instructions



***ESD Sensitive Device!***

Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory back-up, ensure that the board is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the board.

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# General Instructions on Usage

In order to maintain Kontron's product warranty, this product must not be altered or modified in any way. Changes or modifications to the device, which are not explicitly approved by Kontron Modular Computers GmbH and described in this manual or received from Kontron's Technical Support as a special handling instruction, will void your warranty.

This device should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This applies also to the operational temperature range of the specific board version, which must not be exceeded. If batteries are present their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, please follow only the instructions supplied by the present manual.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the board please re-pack it as nearly as possible in the manner in which it was delivered.

Special care is necessary when handling or unpacking the product. Please, consult the special handling and unpacking instruction on the previous page of this manual.

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If the customer's eligibility for warranty has not been voided, in the event of any claim, he may return the product at the earliest possible convenience to the original place of purchase, together with a copy of the original document of purchase, a full description of the application the product is used on and a description of the defect. Pack the product in such a way as to ensure safe transportation (see our safety instructions).

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Chapter 1

# Introduction

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# 1. Introduction

The E²Brain™ product described in this manual is designed to Kontron Modular Computers' "E²Brain™ Module Specification". Section 1.1 provides general information regarding this specification and the system environment as envisioned for E²Brain™ modules. For more detailed information regarding the "E²Brain™ Module Specification", please contact Kontron Modular Computers.

The remaining sub-sections of the Introduction provide more specific details of the EBC2 E²Brain™ carrier board itself to familiarize the user with this product as a whole.

## 1.1 The E²Brain™ Concept

The E²Brain™ concept is a highly flexible approach to providing application developers with the ability to concentrate on the definition of application requirements without having to continuously factor in potential restrictions concerning available data processing and communications functionality.

More specific, data processing and communications requirements become a function of the application and not vice versa. This is possible through the implementation of the E²Brain™ concept. Unlike other approaches to providing application solutions, the E²Brain™ concept concentrates on the most essential aspects of providing data processing and communications without attempting to provide in one entity a complete, self-contained computer system.

The E²Brain™ specification first of all defines a PCB module with a form factor of 115 x 75 x nn millimeters where nn is a function of the height of the board's components. For interfacing with applications, the specification calls for up to four connectors which provide not only interfacing capability for current industry standards but also for future standards or application specific requirements. The type, location, and usage of these connectors is also defined in the specification so as to guarantee standardized compatibility. The specification is open as to the data processing and communications functionality to be implemented which is by definition a function of the application requirements. In addition, the specification envisions considerations for thermal energy dissipation through the implementation of what are to be known as BrainCAP™s (E²Brain™ **C**ooling **A**ssembly, **P**rotector) which can range from heat spreaders to highly sophisticated heat sink cooling designs.

The key features of the E²Brain™ concept are:

- Very compact and robust form factor
- Independent of CPU architecture
- Scalable, flexible, and open system interface
- PCI Master and Agent Mode
- PCI-64 and PCI-X capability
- Versatile and very powerful communications interfaces
- Complete thermal design concept

### 1.1.1 E²Brain™ Functionality

E²Brain™ (Embedded Electronic Brain) is a new platform architecture for advanced computer modules. The E²Brain™ specification defines a very compact mechanical form factor and a comprehensive set of functional interfaces which can be adapted to a wide variety of applications. E²Brain™ modules provide complete computer cores integrating a high-performance CPU, system memory and - typical for E²Brain™ - advanced communications controllers.

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E²Brain™ modules are plugged into customized backplanes or standardized carrier boards which themselves provide the physical interfaces (PHYs) and connectors, power, and additional IO controllers. Through the use of E²Brain™ modules the system developer is relieved of the task of designing computers, and, instead, they permit him to concentrate on the specific product development.

E²Brain™ is a computer platform dedicated not just to one architecture like the PC and Windows architecture, but it is open for all architectures including PowerPC, ARM, SH, x86, and others. E²Brain™ modules are very suitable for “deeply” embedded applications requiring flexible computing power combined with versatile and high-performance communications power.

Although typical E²Brain™ modules are designed to be low power consumption devices, they are part of a well thought out thermal design concept which considers the thermal aspects right from the beginning. Where higher power consumption is unavoidable, E²Brain™ modules are fitted with appropriate BrainCAP™s. By utilizing BrainCAP™s, cooling, mechanical stabilization, and EMI protection are combined in a single concept to satisfy almost any application requirement.

### 1.1.2 Basic Architecture

The following figure illustrates the basic functional architecture of E²Brain™ modules. Common to all E²Brain™ modules are the data processing and communications core and the system and communications interfaces.

The application requirements determine the functionality required of the E²Brain™ module core which in turn mandates the functionality to be provided by the system and communications interfaces. Both of these interfaces are comprised of a base set and an extended set of functional features.

The system interface to the application is accomplished through connectors Pn1 and Pn2. Connector Pn1 provides the base set of system interfacing and Pn2 the extended set. If the application does not require extended system interfacing, it is not necessary to populate connector Pn2. The same analogy applies to the communications interfacing whereby connector Pn3 provides the base set of communications interfacing and Pn4 the extended set. Pn4 is not required to be populated if there is not an application requirement for it. This concept together with a corresponding core provides a maximum of scalability and flexibility to satisfy the most demanding of applications.

### 1.1.3 E²Brain™ System Environment

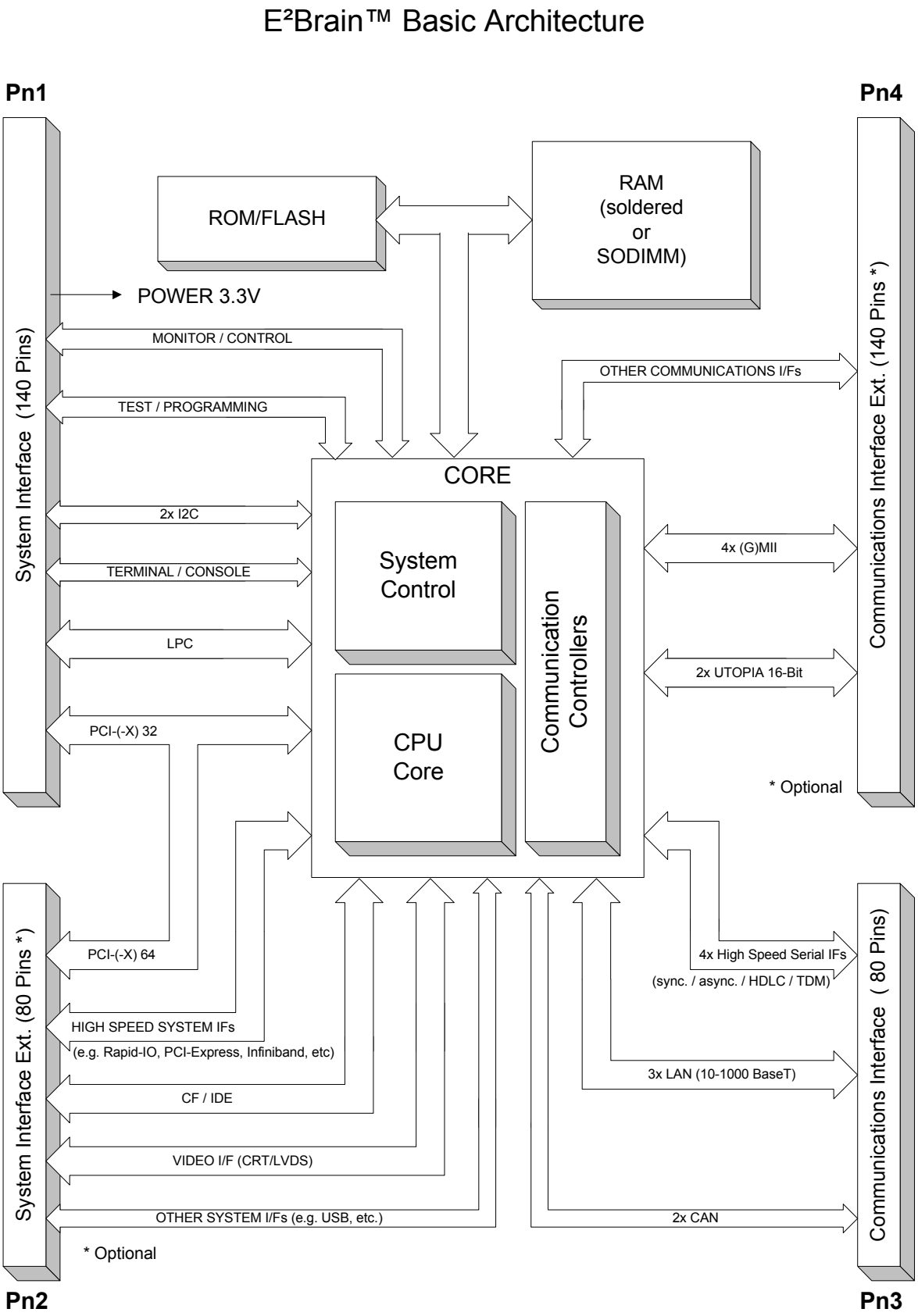
The E²Brain™ module form factor and mechanical and electrical interfacing are so conceived as to allow the use of E²Brain™ modules in practically any kind of system environment. These mezzanine modules can easily be integrated on most standardized carrier boards (VME, CompactPCI, PC PCI, etc.) as well as any other conceivable type of carrier board capable of providing the required mechanical and electrical infrastructure.

In addition to this infrastructure, thermal energy dissipation requirements must be taken into consideration when implementing applications using E²Brain™ modules. The E²Brain™ concept basically calls for modules to provide their own thermal energy dissipation. It may, however, be necessary to add additional thermal energy dissipation capability depending on the overall system environment. To satisfy such requirements, E²Brain™ modules may be equipped with specially designed cooling devices that are adapted to the specific system environment.

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**Figure 1-1: E²Brain™ Basic Architecture**





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## 1.2 EBC2 System Overview

The EBC2 is a special purpose E²Brain™ module carrier board which is designed to provide customers with a platform for the development of their own applications based on Kontron's E²Brain™ high performance processor modules. This carrier board takes advantage of an extensive range of the many features offered by these modules thus allowing developers to become familiar with their capabilities without having to first invest time and engineering resources in the development of an operational test environment.

In addition to supporting application development for the E²Brain™ modules themselves, the EBC2 can also be used as a model for the development of application specific carrier boards.

Designed as part of an overall system development kit, the EBC2 provides a comprehensive set of industry standard interfacing as well as test and programming interfaces. Coupled with an appropriate E²Brain™ module, board support package (BSP), and operating system it is an ideal starting basis for rapid efficient system application design and integration.

## 1.3 Product Overview

The EBC2 E²Brain™ carrier board is a part of an innovative concept to provide system integrators with a complete range of off-the-shelf as well as custom embedded computer cores for the most demanding of applications.

This carrier board which supports the EB405, EB425, or the EB8540 E²Brain™ module as its computer core provides a comprehensive set of standard computer functionality coupled with industry standard system and communications I/O capability.

The following table provides a quick overview of the EBC2 board.

**Table 1-1: EBC2 Product Overview**

| EBC2 FEATURES | DESCRIPTION |
|---|---|
| Product Type | E²Brain™ module carrier board:<br>• Core Processor types supported:<br>  • EB405<br>  • EB425<br>  • EB8540<br>  • other E²Brain™ compliant modules<br>• Form factor: 244 mm x 244 mm (micro ATX)<br>• Complies with the E²Brain™ specification |
| I/O Interfaces | System:<br>• I²C bus<br>• LPC bus<br>• PCI-bus<br>• Serial: terminal and console<br>• USB<br>• CompactFlash<br>• Digital I/O<br>• EEPROM<br>• LPC Flash |
| I/O Interfaces | Communications:<br>• Serial: high speed UART<br>• Fast Ethernet<br>• Giga Ethernet (Three Speed: 10 / 100 / 1000 Mbps)<br>• CAN |

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**Table 1-1: EBC2 Product Overview**

| EBC2 FEATURES | DESCRIPTION |
|---|---|
| Other | Test and Programming:<br>• EB405 JTAG/DEBUG<br>• EB425 JTAG/DEBUG<br>• EB8540 JTAG/DEBUG<br>• EBC2 logic<br>• ATMEL<br>Monitor and Control:<br>• Seven segment LED displays<br>• Signal inputs and outputs<br>• LEDs<br>• Switches<br>• Jumpers<br>• Resistors |

## 1.4 Board Overview

### 1.4.1 Board Introduction

The EBC2 is a custom simplified application interface (SAI) for E²Brain™ high performance mezzanine computer modules. It provides physical accommodations for mounting one E²Brain™ module and a comprehensive set of interfaces for application development.

### 1.4.2 Board Specific Information

Major board components of the EBC2 E²Brain™ SAI board are:

- Logic controller for digital IO and POST code display
- I2C EEPROM
- Computer core interface: two system connectors and two communications connectors
- PCI interface
- Low Pin Count (LPC) interface
- I²C interface
- High speed serial interfaces:
  - Four RS232 / RS422 / RS485 full modem, half or full duplex
  - Two RS232 only (no hardware handshaking)
- Two Fast Ethernet interfaces
- Two Giga Ethernet interfaces (Three Speed Ethernet)
- Two USB interfaces
- Two CAN interfaces
- Four digital input interfaces and four digital output interfaces (non-opto-isolated)
- LPC Flash interface (PLCC32)
- CompactFlash interface (Type I/II, IBM Microdrive)
- Two debugging interfaces
- Three programming interfaces
- Monitor and control interfaces
  - Two, seven segment LED displays
  - Twentytwo single LEDs

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- Various jumpers and resistors
- Eight control input signals
- One control output signal
- Two push button switches
- One eight pole DIP switch

- DC/DC power supply

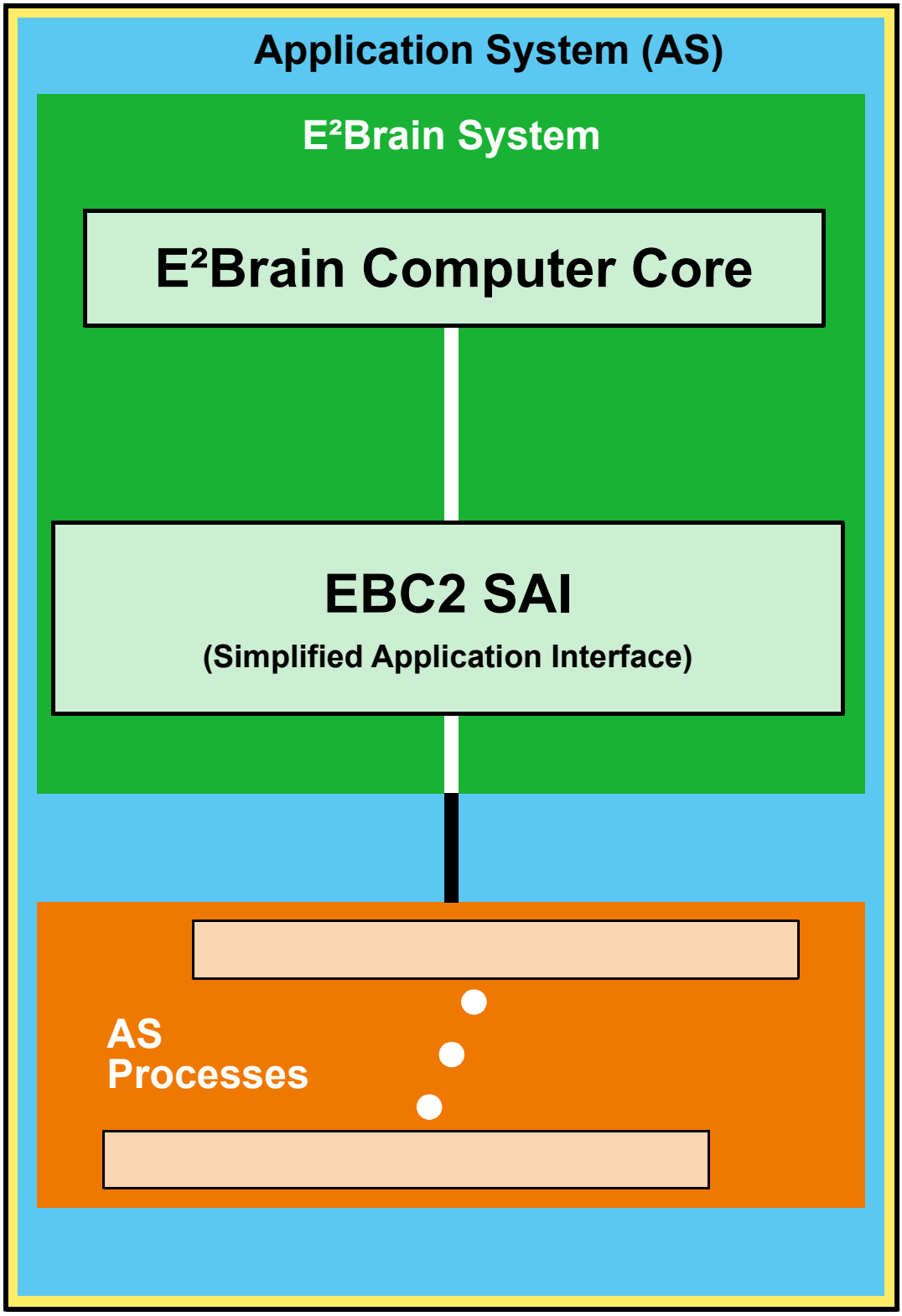
## 1.5 Board Diagrams

The following sections provide diagrams along with additional information concerning board functionality and component layout.


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### 1.5.1 Application System Interfacing

**Figure 1-2: EBC2 Application System Interfacing Diagram**





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### 1.5.2 System Level Interfacing

An E²Brain™ application sub-system is comprised of an E²Brain™ computer core and a simplified application interface (SAI). In this case, the EBC2 is the SAI, whereby its application functionality is to support E²Brain™ solutions development. The interfaces available on the EBC2 are representative of typical E²Brain™ application requirements and are best suited for application development. The following figure demonstrates the basic interfacing relationship of the E²Brain™ module to the EBC2 SAI. The following table provides a legend for Figure 1-3.

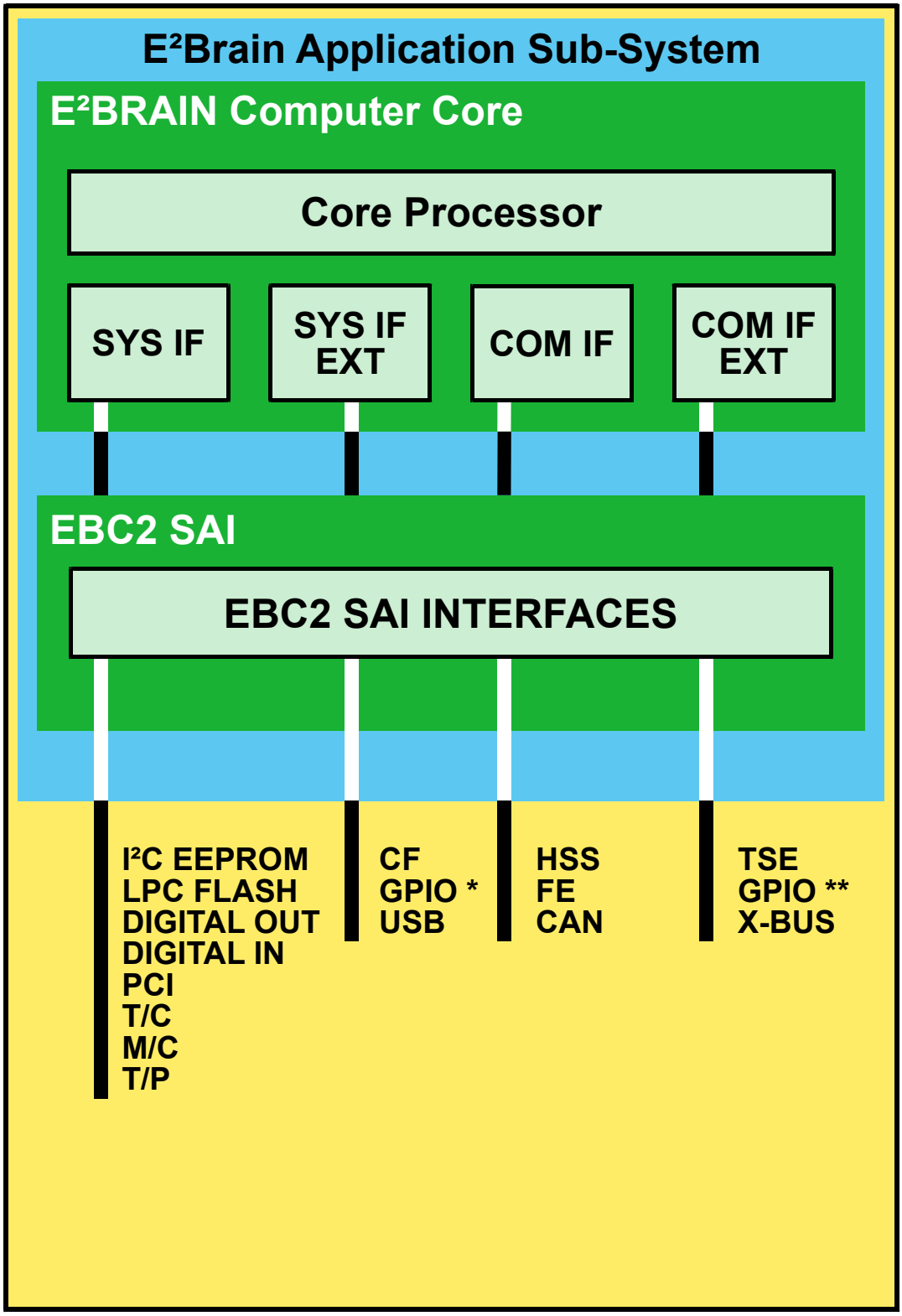
**Table 1-2: Legend for Figure 1-3**

| ITEM | DESCRIPTION |
|---|---|
| CAN | Controller Area Network |
| CF | CompactFlash |
| DIGITAL IN | Digital input |
| DIGITAL OUT | Digital output |
| FE | Fast Ethernet |
| GPIO * | General purpose input / output<br>This interface is supported only by the EB405 E²Brain™ module. |
| GPIO ** | General purpose input / output<br>This interface is supported only by the EB425 E²Brain™ module. |
| HSS | High Speed Serial interfaces |
| I²C EEPROM | I²C interface<br>EEPROM is installed for application development usage. |
| LPC Flash | Low Pin Count Flash<br>Supports PLCC32 socket. |
| M/C | Monitor / Control interface |
| PCI | PCI<br>Two standard PCI connectors plus one mini-PCI connector |
| T/C | Terminal / Console<br>Serial interface for terminal/console type operations (RS232) |
| T/P | Test / Programming<br>JTAG / DEBUG and programming |
| TSE | Three Speed Ethernet<br>This interface is supported only by the EB8540 E²Brain™ module. |
| X-BUS | Expansion bus<br>This interface is supported only by the EB425 E²Brain™ module. |

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Figure 1-3: EBC2 System Level Interfacing Diagram



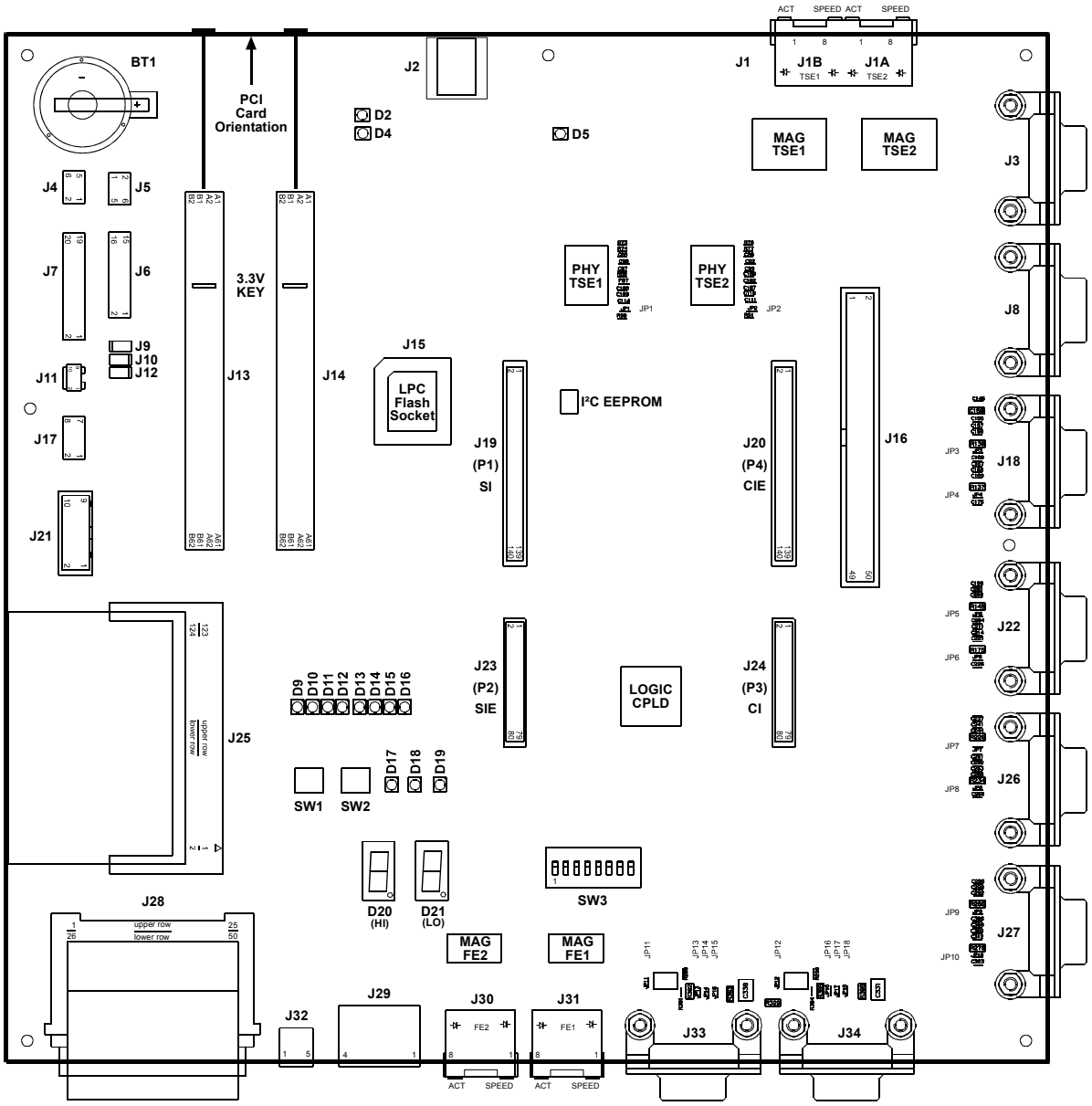


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### 1.5.3 Board Layout

The following figures illustrate the positioning of the interfaces and monitor and control elements on the EBC2 carrier board. The accompanying table provides an ordered listing of these items along with a short description. For further information refer to section 2.

**Figure 1-4: EBC2 Board (Front View)**




***Warning!***

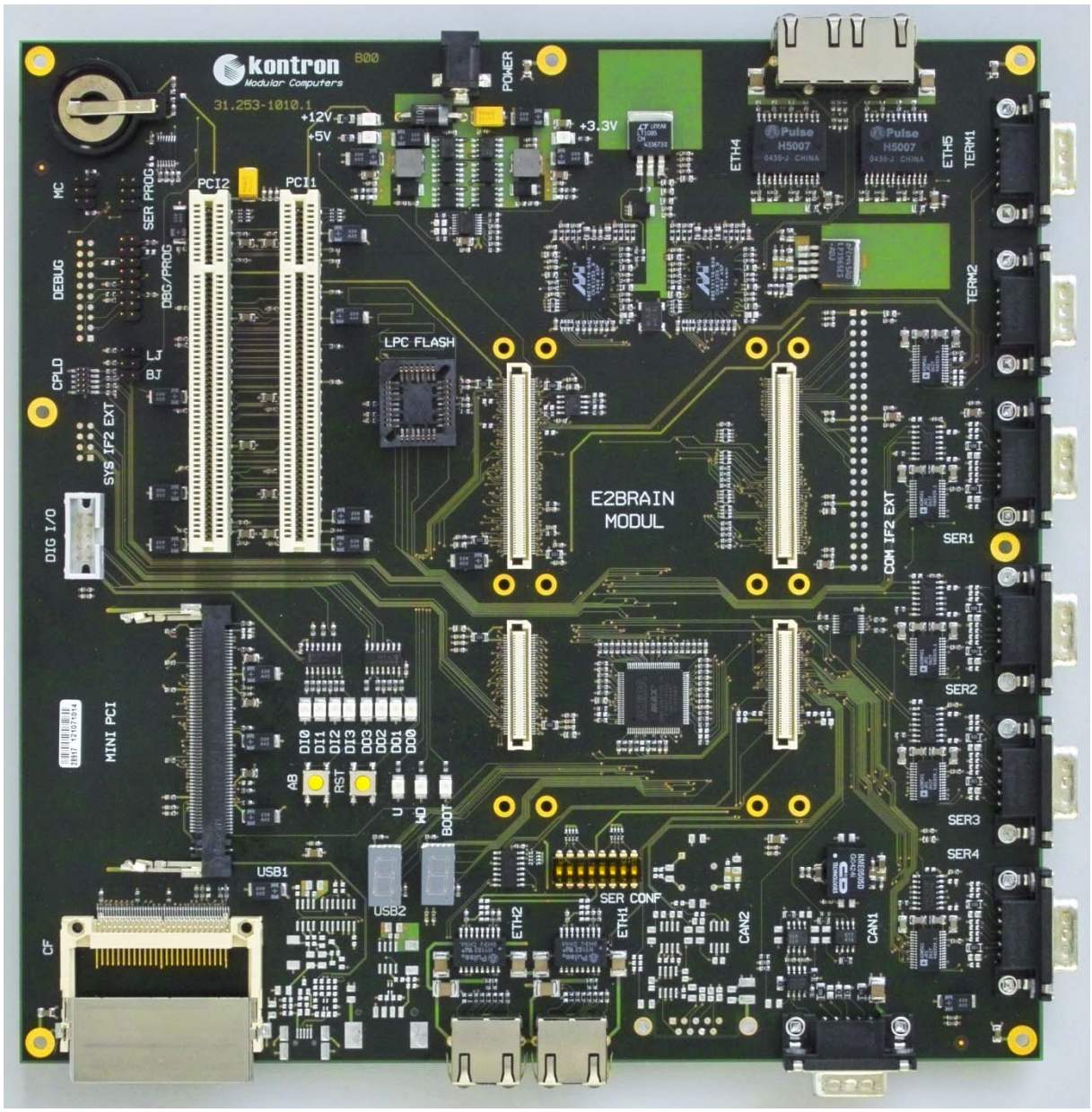
The J13 and J14 connectors are 3.3V coded. Only 3.3V or universally coded cards may be used with this connector. Do not attempt to install 5V coded cards as this will result in damage to the PCI card, the EBC2, or the E²Brain™ module itself.

The EBC2 is configured for 3.3V V(I/O) operation which supports currently available E²Brain™ modules. The EBC2 is not configurable for 5V V(I/O).


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**Figure 1-5: EBC2 Board Variant for E²Brain™ Module EB8540**




The population of various connectors and other corresponding interfacing components on the EBC2 is a function of the E²Brain™ module to be used with the EBC2. The figure above is illustrative of an EBC2 which is configured for the EB8540 module.


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**Table 1-3: EBC2 Interfaces and MC Elements**

| IF / MCE | ALIAS | DESCRIPTION |
|---|---|---|
| BT1 | | Backup battery for RTC, SRAM, etc. |
| D2 | 12V | LED, green, indicates 12V input power is applied |
| D4 | 5V | LED, green, indicates 5V power is applied |
| D5 | 3.3V | LED, green, indicates 3.3V power is applied |
| D9 | DIN0 | LED, green, indicates DIN(0) signal is asserted |
| D10 | DIN1 | LED, green, indicates DIN(1) signal is asserted |
| D11 | DIN2 | LED, green, indicates DIN(2) signal is asserted |
| D12 | DIN3 | LED, green, indicates DIN(3) signal is asserted |
| D13 | DOUT3 | LED, yellow, indicates DOUT(3) signal is asserted |
| D14 | DOUT2 | LED, yellow, indicates DOUT(2) signal is asserted |
| D15 | DOUT1 | LED, yellow, indicates DOUT(1) signal is asserted |
| D16 | DOUT0 | LED, yellow, indicates DOUT(0) signal is asserted |
| D17 | GPIO | LED, red, general purpose IO signal, when on signal is asserted (MC11) |
| D18 | WDOG | LED, yellow, indication is a function of the E²Brain™ module Watchdog logic(MC7) |
| D19 | BOOT | LED, green, indication is a function of the NetBootLoader during system booting, is available to the application after booting is completed (MC6) |
| D20 | POST_HI | LED, seven segment, hexadecimal display, higher nibble of byte, used for indicating POST codes or application after system is booted |
| D21 | POST_LO | LED, seven segment, hexadecimal display, lowerer nibble of byte, used for indicating POST codes or application after system is booted |
| J1 | TSE[1, 2] | Connector, dual RJ45, three speed Ethernet interface, right connector is TSE1, left connector is TSE2 (as seen from front of connector - LEDs visible) |
| J2 | +12Supply | Connector, +12V main input power supply |
| J3 | TERM | Connector, serial interface for terminal operations |
| J4 | M/C | Connector, external access to monitor and control signal lines |
| J5 | ATMEL | Connector, programming interface for E²Brain™ module logic configuration EEPROM |
| J6 | TP1 | Connector, test and programming interface for EB405 and EB8540 E²Brain™ modules |
| J7 | TP2 | Connector, test and programming interface for EB425 E²Brain™ module |
| J8 | CONS | Connector, serial interface for console operations |
| J9 | INT2 | Jumper, test interface, interrupt input source, active low |
| J10 | INT1 | Jumper, test interface, interrupt input source, active high |
| J11 | TP3 | Connector, programming interface for the EBC2 logic CPLD |
| J12 | F/LPCB | Jumper, selects boot code source: open = boot from E²Brain™ module Flash (default); set = boot from EBC2 LPC Flash |

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**Table 1-3: EBC2 Interfaces and MC Elements**

| IF / MCE | ALIAS | DESCRIPTION |
|---|---|---|
| J13 | PCI_SLOT2 | Connector, PCI interface, standard 32-bit, 3.3V V(I/O), slot number 2, 33 MHz |
| J14 | PCI_SLOT1 | Connector, PCI interface, standard 32-bit, 3.3V V(I/O), slot number 1, 33 MHz |
| J15 | LPCFLASH | Socket, Flash interface, PLCC, 32-pin, for LPC boot Flash |
| J16 | CIE_EX | Connector, X-BUS and DIO interfacing for EB425 |
| J17 | SIE_EX | Connector, GPIO interfacing for EB405 |
| J18 | SER1 | Connector, high speed serial interface 1 |
| J19 (P1) | SI | Connector, system interfacing to the E²Brain™ module, System Interface - SI |
| J20 (P4) | CIE | Connector, communications interfacing extension to the E²Brain™ module, Communications Interface Extension - CIE |
| J21 | DIO | Connector, general purpose digital input (4) and output (4) interfacing |
| J22 | SER2 | Connector, high speed serial interface 2 |
| J23 (P2) | SIE | Connector, system interfacing extension to the E²Brain™ module, System Interface Extension - SIE |
| J24 (P3) | CI | Connector, communications interfacing to the E²Brain™ module, Communications Interface - CI |
| J25 | PCI_MINI | Connector, PCI interface, 32-bit, Mini PCI, 33 MHz |
| J26 | SER3 | Connector, high speed serial interface 3 |
| J27 | SER4 | Connector, high speed serial interface 4 |
| J28 | CF_SOCKET | Connector, CompactFlash interface, Type I and II |
| J29 | USB2 | Connector, USB interface, USB 2.0, type A |
| J30 | FE2 | Connector, Fast Ethernet interface 2 |
| J31 | FE1 | Connector, Fast Ethernet interface 1 |
| J32 | USB1 | Connector, USB interface, USB 2.0, type mini AB |
| J33 | CAN2 | Connector, CAN interface 2 |
| J34 | CAN1 | Connector, CAN interface 1 |
| JP1 | | Jumper, TSE1 PHY low power mode select (open = default) |
| JP2 | | Jumper, TSE2 PHY low power mode select (open = default) |
| JP3 | | Jumper, SER1 120Ω termination for RS422/485 operation |
| JP4 | | Jumper, SER1 120Ω termination for RS422/485 operation |
| JP5 | | Jumper, SER2 120Ω termination for RS422/485 operation |
| JP6 | | Jumper, SER2 120Ω termination for RS422/485 operation |
| JP7 | | Jumper, SER3 120Ω termination for RS422/485 operation |

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**Table 1-3: EBC2 Interfaces and MC Elements**

| IF / MCE | ALIAS | DESCRIPTION |
|---|---|---|
| JP8 | | Jumper, SER3 120Ω termination for RS422/485 operation |
| JP9 | | Jumper, SER4 120Ω termination for RS422/485 operation |
| JP10 | | Jumper, SER4 120Ω termination for RS422/485 operation |
| JP11 | | Jumper, CAN2, galvanic isolation power ground (set = default) |
| JP12 | | Jumper, CAN1, galvanic isolation power ground (set = default) |
| JP13 | | Jumper, CAN2 120Ω termination (open = default) |
| JP14 | | Jumper, CAN2, galvanic isolation power ground (set = default) |
| JP15 | | Jumper, CAN2, galvanic isolation power 5V (set = default) |
| JP16 | | Jumper, CAN1 120Ω termination (open = default) |
| JP17 | | Jumper, CAN1, galvanic isolation power ground (set = default) |
| JP18 | | Jumper, CAN1, galvanic isolation power 5V (set = default) |
| SW1 | ABORT | Switch, when closed asserts the abort signal MC1 |
| SW2 | RESET | Switch, when closed asserts the reset signal MC0 |
| SW3 | MODESEL | Switch, 8-pole DIP, SER[1:4] operational mode select. RS232 / RS422 / RS485 |

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## 1.6 Technical Specifications

**Table 1-4: EBC2 Main Specifications**

| | DESIGNATOR | TYPE | Specifications |
|---|---|---|---|
| Mezzanine Modules | EB405 (currently available) | | High Performance PowerPC™ Processor E²Brain™ Module based on IBM's 405EP Integrated Processor PowerPC |
| | EB425 (currently available) | | High Performance XScale Processor E²Brain™ Module based on the Intel™ IXP425 |
| | EB8540 (currently available) | | High Performance PowerPC™ Processor E²Brain™ Module based on Motorola's MPC8540 Integrated Processor PowerPC |
| Onboard Controller | Logic Controller | | CPLD controller, Altera EPM3128, for digital I/O and seven segment LED display, LPC-bus interface, HSS interfaces operational control |
| Embedded Module Interfaces | J19 (P1) | System Interface (SI) | E²Brain™ System Interface, 140-pin HIROSE connector |
| | J23 (P2) | System Interface Extension (SIE) | E²Brain™ System Interface Extension, 80-pin HIROSE connector |
| | J24 (P3) | Communications Interface (CI) | E²Brain™ Communications Interface, 80-pin HIROSE connector |
| | J20 (P4) | Communications Interface Extension (CIE) | E²Brain™ Communications Interface Extension, 140-pin HIROSE connector |
| System Interfaces | PCI INTERFACES | | |
| | J19 (P1) (internal) | PCI-bus | Standard PCI bus, 32-bit, 33 MHz (Can be supplied for 66 MHz or PCI_X) |
| | J13 | PCI Slot 2 | Single standard PCI expansion slot interface, 124-pin connector |
| | J14 | PCI Slot 1 | Single standard PCI expansion slot interface, 124-pin connector |
| | J25 | Mini PCI | Mini PCI expansion interface, 124-pin connector |
| | LPC INTERFACES | | |
| | J19 (P1) (internal) | LPC-bus | Standard LPC-bus, but no DMA support |
| | J15 | PLCC32 Socket | 32-pin PLCC socket, supports LPC Flash for system booting, jumper configurable |
| | I²C INTERFACES | | |
| | J19 (P1) (internal) | I²C-bus | Standard I²C-bus<br>The only device on this bus is an EEPROM which is provided for application development of I²C functionality. |


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**Table 1-4: EBC2 Main Specifications (Continued)**

| | DESIGNATOR | TYPE | Specifications |
|---|---|---|---|
| System Interfaces | COMPACTFLASH INTERFACES | | |
| | J28 | CompactFlash | Standard CompactFlash device interface, 50-pin, male, dual pinrow, shrouded connector |
| | J23 (P2) (internal) | CompactFlash | CompactFlash interface routed from J23 (P2) to J28 to allow for direct interfacing between the E²Brain™ module and a CompactFlash |
| | TERMINAL / CONSOLE INTERFACES | | |
| | J3 | RS232 | TERM, terminal serial port (no HW handshake), 9-pin, male, D-Sub connector |
| | J8 | RS232 | CONS, console serial port (no HW handshake), 9-pin, male, D-Sub connector |
| | USB INTERFACES | | |
| | J29 | USB 1.1, USB 2.0 | USB2, host port, type A receptacle connector |
| | J32 | USB 1.1, USB 2.0 | USB1, device port, mini USB, type AB receptacle connector |
| | DIGITAL INPUT AND OUTPUT (DIO) INTERFACES | | |
| | J17 | GPIO | Six general purpose digital input / output channels, individually configurable for either input or output<br>This interface is only supported by the EB405 module. |
| | J21 | Digital Input / Output | Four channels of digital input and four channels of digital output non-opto-isolated signals on 10-pin, male, shrouded, dual pinrow connector (DI 0, 1, 2, 3 and DO 0, 1, 2, 3) |
| Communications Interfaces | HIGH SPEED SERIAL INTERFACES | | |
| | J18 | RS232 / 422 / 485 | SER1, configurable serial port, 9-pin, male, D-Sub connector |
| | J22 | RS232 / 422 / 485 | SER2, configurable serial port, 9-pin, male, D-Sub connector |
| | J26 | RS232 / 422 / 485 | SER3, configurable serial port, 9-pin, male, D-Sub connector |
| | J27 | RS232 / 422 / 485 | SER4, configurable serial port, 9-pin, male, D-Sub connector |
| | ETHERNET INTERFACES | | |
| | J30 | Fast Ethernet | 10 / 100 Mbit Fast Ethernet interface (channel 2), auto-negotiation |
| | J31 | Fast Ethernet | 10 / 100 Mbit Fast Ethernet interface (channel 1), auto-negotiation |
| | J1 | Giga Ethernet (TSE) | Three speed Ethernet interface, 10 / 100 / 1000 Mbit, dual RJ45 connector, TSE1 is routed to right connector, auto-negotiation |

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**Table 1-4: EBC2 Main Specifications (Continued)**

| | DESIGNATOR | TYPE | Specifications |
|---|---|---|---|
| Communications Interfaces | CAN INTERFACES | | |
| | J33 | CAN | CAN interface (CAN2), 9-pin, male, D-Sub connector, opto-isolated |
| | J34 | CAN | CAN interface (CAN1), 9-pin, male, D-Sub connector, opto-isolated |
| | OTHER INTERFACES | | |
| | J16 | GPIO | General purpose interface, supports EB425 X-Bus and DIO, shrouded, 50-pin, male, dual pinrow connector |
| Monitor and Control (M/C) Interfaces | SWITCH INTERFACES | | |
| | SW1 | Switch | Abort switch, generates abort input (interrupt request) |
| | SW2 | Switch | Reset switch, generates reset input |
| | SW3 | Switch | HSS operational mode control, selects RS232/422/485 for SER[1:4] |
| | LED INTERFACES | | |
| | D2 | LED | Indicates 12V input power is applied |
| | D4 | LED | Indicates 5V power is applied |
| | D5 | LED | Indicates 3.3V power is applied |
| | D9 | LED | Indicates DIN(0) signal is asserted |
| | D10 | LED | Indicates DIN(1) signal is asserted |
| | D11 | LED | Indicates DIN(2) signal is asserted |
| | D12 | LED | Indicates DIN(3) signal is asserted |
| | D13 | LED | Indicates DOUT(3) signal is asserted |
| | D14 | LED | Indicates DOUT(2) signal is asserted |
| | D15 | LED | Indicates DOUT(1) signal is asserted |
| | D16 | LED | Indicates DOUT(0) signal is asserted |
| | D17 | LED | General purpose IO signal, when on signal is asserted (MC11) |
| | D18 | LED | Indication is a function of the E²Brain™ module Watchdog logic(MC7) |
| | D19 | LED | Indication is a function of the NetBootLoader during system booting, is available to the application after booting is completed (MC6) |
| | D20 | LED | Seven segment, hexadecimal display, higher nibble of byte, used for indicating POST codes or application after system is booted |


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**Table 1-4: EBC2 Main Specifications (Continued)**

| | DESIGNATOR | TYPE | Specifications |
|---|---|---|---|
| Monitor and Control (M/C) Interfaces | D21 | LED | Seven segment, hexadecimal display, lowerer nibble of byte, used for indicating POST codes or application after system is booted |
| | FE1LG | LED | FE channel 1 link speed indicator, green, integrated in J31 |
| | FE1LY | LED | FE channel 1 link status indicator, yellow, integrated in J31 |
| | FE2LG | LED | FE channel 2 link speed indicator, green, integrated in J30 |
| | FE2LY | LED | FE channel 2 link status indicator, yellow, integrated in J30 |
| | TSE1_ACT | LED | TSE channel 1 link activity indicator, green, integrated in J1B |
| | TSE1_SPEED | LED | TSE channel 1 link speed indicator, green/yellow, integrated in J1B |
| | TSE2_ACT | LED | TSE channel 2 link activity indicator, green, integrated in J1A |
| | TSE2_SPEED | LED | TSE channel 2 link speed indicator, green/yellow, integrated in J1A |
| | SIGNAL INTERFACES ON J4 | | |
| | MC2 | M/C | Specific use of these signals is function of application and E²Brain™ module employed<br>J4 is a 6-pin, male, dual pinrow header connector |
| | MC3 | M/C | |
| | MC5 | M/C | |
| | MC9 | M/C | |
| | MC10 | M/C | |
| | GND | Ground | |
| Test and Programming (T/P) Interfaces | J6 | JTAG / DEBUG | EB8540 and EB405 T / P interface, 16-pin, male, dual pinrow header connector |
| | J7 | JTAG / DEBUG | EB425 T / P interface, 20-pin, male, dual pinrow header connector |
| | J11 | JTAG | EBC2 Logic programming interface, 10-pin, male, dual pinrow, miniature header connector |
| | J5 | ATMEL | E²Brain™ module logic configuration EEPROM programming interface, 6-pin, male, dual pinrow header connector |

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**Table 1-4: EBC2 Main Specifications (Continued)**

| | DESIGNATOR | TYPE | Specifications |
|---|---|---|---|
| Power Interfaces | J2 | + 12 V | Main input power interface to EBC2 board, 2-pin female receptacle |
| | J19 (P1) | + 3.3 V, V(IO) | Input power interface to E²Brain™ module, 140-pin HIROSE connector |
| | J23 (P2) | + 3.3 V, V(IO) | Input power interface to E²Brain™ module, 80-pin HIROSE connector |
| | Battery socket | AUX Power | Battery input power interface to E²Brain™ modules for power backup of RTC and SRAM memory devices<br>Battery voltage range: 2.8 to 3.6 volts |
| | DC / DC | Power converter (onboard) | + 12 V DC to + 3.3 V DC and + 5 V DC converter, distribution of power to EBC2 board and board connectors |
| General | Mechanical | | Conforms with Kontron Modular Computers' "E²Brain™ Module Specification" |
| | Electrical | | Main board input power voltage: + 12 V DC<br>Onboard voltages: + 3.3 V DC<br>+ 5 V DC<br>+ 12 V DC<br>+ 2.5 V DC (for EB8540)<br>+ 1.5 V DC (for EB8540) |
| | Power Consumption | | Output rating of the onboard DC / DC converter is 30 W |
| | Temperature Range | | Operational: 0ºC to +55ºC Standard<br>Storage: -55ºC to +125ºC |
| | Humidity | | 93% relative humidity at 40°C non-condensing |
| | Dimensions | | 244 mm x 244 mm, micro ATX |
| | Board Weight | | Approximately 300 g (minimum configuration and no E²Brain™ module installed) |


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## 1.7 Applied Standards

The Kontron Modular Computers' E²Brain™ modules comply with the requirements of the following standards:

**Table 1-5: Applied Standards**

| | TYPE | STANDARD |
|---|---|---|
| CE | Emission | EN55022 |
| | Immunity, Industrial Environment | EN61000-6-2 |
| | Immunity, IT Equipment | EN55024 |
| | Electrical Safety | EN60950<br>Note:<br>The EBC2 is specified I/O only for: SELV and EVL.<br>It is **NOT SPECIFIED** for "Hazardous" |
| MECHANICAL | Mechanical Dimensions | IEEE 1101.1 |
| ENVIRONMENTAL TESTS | Vibration, Sinusoidal | IEC 60068-2-6 |
| | Random Vibration, Broadband | IEC 60068-2-64 |
| | Bump | IEC 60068-2-29 |
| | Single Shock | IEC 60068-2-27 |
| | Temperature Tests A: Cold | IEC 60068-2-1 |
| | Temperature Tests B: Dry Heat | IEC 60068-2-2 |
| | Climatic Humidity | IEC 60068-2-78 |
| PRODUCT PACKAGING | Transport and Storage | IEC 61131-2 |
| | ESD Protection | IEC 61340-5-1 and IEC 61340-5-2 |

## 1.8 Related Publications

**Table 1-6: Related Publications**

| | ISSUED BY | DOCUMENT |
|---|---|---|
| PCI | PCI-SIG | PCI Local Bus Specification, R.2.2 |
| Mini PCI | PCI-SIG | Mini PCI Specification, Rev. 1.0 |
| LPC | Intel® | Intel® Low Pin Count (LPC) Interface Specification, Rev. 1.1 |
| I²C | Philips | I2C-BUS SPECIFICATION, Rev. 2.1 |
| E²Brain™ | Kontron Modular Computers | E²Brain™ Module Specification |

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Chapter 2

# Functional Description

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# 2. Functional Description

The following chapters present more detailed, board level information about the EBC2 E²Brain™ SAI (Simplified Application Interface) whereby the board components and their basic functionality are discussed in general.

## 2.1 General Information

The EBC2 is comprised basically of the following:

- E²Brain embedded module interfaces
  - System Interface
  - System Interface Extension
  - Communications Interface
  - Communications Interface Extension
- Board system interfaces:
  - PCI expansion slots, Mini PCI socket
  - I²C bus
  - LPC interface
  - Terminal and Console (T/C) serial interfacing
  - Monitor and Control (M/C) interfacing
  - Test and Programming (T/P) interfacing
  - CompactFlash (CF) interface
  - Digital input and output interfacing
  - USB interfacing
  - LPC Boot Flash
  - DC/DC power supply
- Board communications interfaces:
  - High Speed Serial (HSS) communications
  - Fast Ethernet (FE)
  - CAN
  - Giga Ethernet (TSE)

### 2.1.1 Embedded Module Interfaces

The EBC2 E²Brain™ SAI is supplied with a comprehensive set of embedded module interfacing capabilities. The standard set of system interfaces is routed through the System Interface connector J19 (P1). An extended set of system interfacing is routed through the System Interface Extension connector J23 (P2). The standard set of communications interfaces is routed through the Communications Interface connector J24 (P3). In addition, the EBC2 is provided with the Communications Interface Extension connector J20 (P4).

The System Interface connector J19 (P1) provides interfacing for the following:

- PCI bus
- LPC bus
- I²C bus
- Terminal and Console (T/C) serial interfacing (TERM and CONS)
- Monitor and Control (M/C) interfacing
- Test and Programming (T/P) interfacing

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The System Interface Extension connector J23 (P2) provides interfacing for the following:

- CompactFlash (CF) interface
- GPIO interfacing (EB405 only)
- USB interfacing

The Communications Interface connector J24 (P3) provides interfacing for the following:

- High Speed Serial (HSS) interfacing (TTL level) (SER1, SER2, SER3, SER4)
- Fast Ethernet (MDI interface)
- CAN

The Communications Interface Extension connector J20 (P4) provides interfacing for the following:

- Giga Ethernet (GMII interface, Three Speed Ethernet)
- X-bus (EB425 only)
- GPIO (EB425 only)

### 2.1.2 Board System and Communications Interfaces

The EBC2 supports a very comprehensive sub-set of the E²Brain system and communications interfaces. Refer to the individual connector pinout descriptions for details.

## 2.2 Board-Level Interfacing Diagrams

The following five figures demonstrate the interfacing structure between the internal processing elements of the EBC2 and other major EBC2 components. The interfacing lines are shown in white where they are on board and in black for board external interfacing.

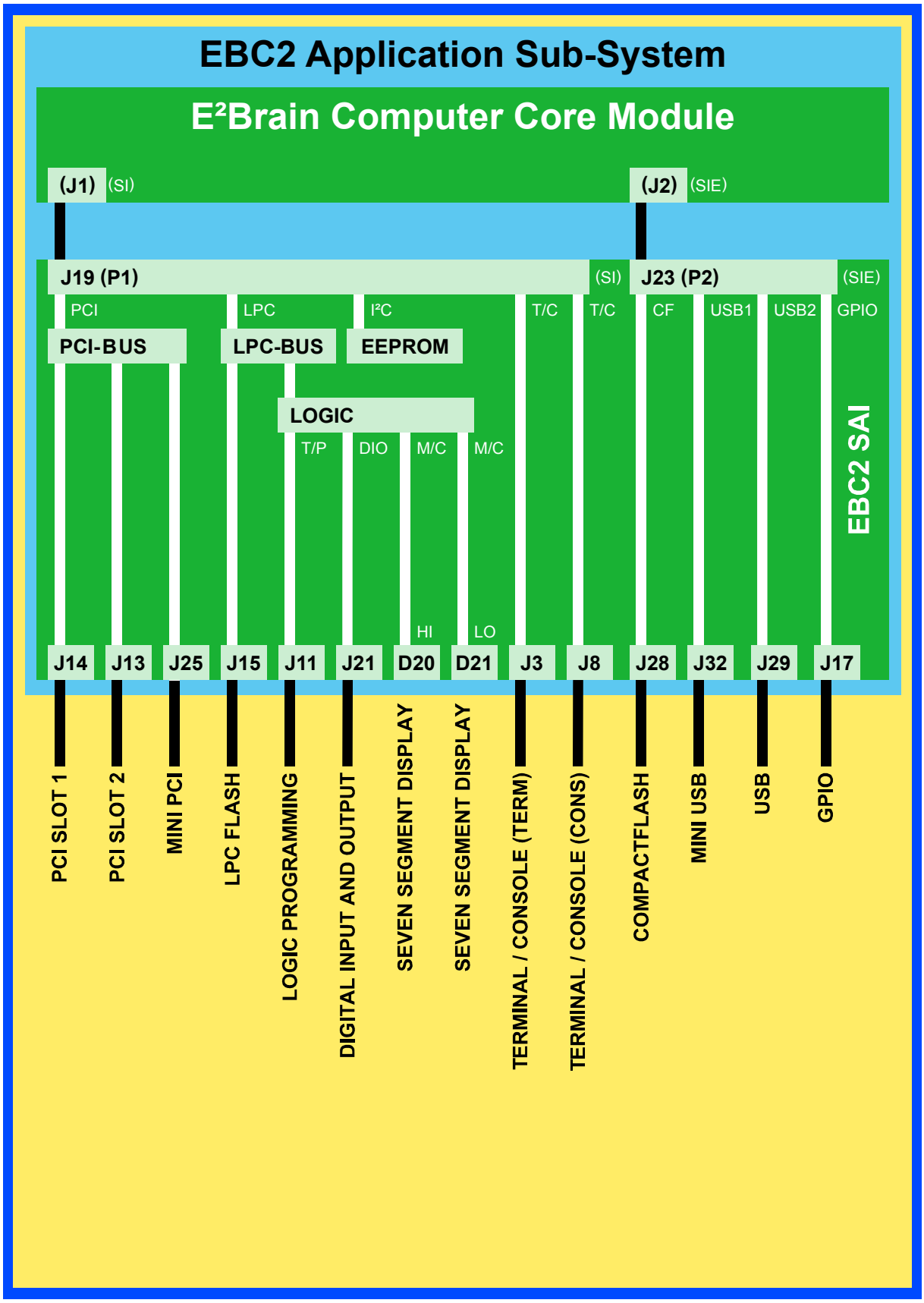
**Legend for Figures 2-1 thru 2-5:**

| | |
|---|---|
| **#** | Interfacing without switching |
| **(Jn)** | Connector designator from E²Brain specification |
| **(Pn)** | Connector designator from E²Brain specification |
| **BOOT** | Boot LED |
| **BT1** | Backup battery interface |
| **CAN** | Controller Area Network |
| **CF** | CompactFlash |
| **CI** | Communications Interface |
| **CIE** | Communications Interface Extension |
| **DC/DC** | DC to DC (converter) |
| **DIN** | Digital input indicator LED |
| **DIO** | Digital Input and Output |
| **Dnn** | LEDs 2, 4, 5 and 9 through 19 |
| **DOUT** | Digital output indicator LED |
| **FE** | Fast Ethernet |
| **G/GY** | Green and green/yellow LEDs |
| **GPIO** | General Purpose Input or Output (LED) |
| **HSS** | High Speed Serial interfacing |
| **I²C** | Inter-Integrated Circuit |
| **J1A** | TSE2 interace (left connector) |
| **J1B** | TSE1 interface (right connector) |
| **LDO** | Low dropout linear regulator |
| **LOGIC** | Logic controller |
| **LPC** | Low Pin Count |
| **M/C** | Monitor and Control |
| **MAG** | Magnetics |
| **nn** | Connector number nn (Jnn) |
| **O-I** | Opto-isolation |
| **PCI** | Peripheral Component Interface |
| **PHY** | Ethernet PHY |
| **SAI** | Simplified Application Interface |
| **SERn** | Serial interface n |
| **SI** | System Interface |
| **SIE** | System Interface Extension |
| **SWn** | Switches 1, 2, 3 |
| **T/C** | Terminal/Console (Serial Interface) |
| **T/P** | Test and Programming |
| **TXRX** | Transceiver |
| **USB** | Universal Serial Bus |
| **V_BAT** | Backup power input |
| **V(I/O)** | PCI signalling voltage |
| **WDOG** | Watchdog (LED) |
| **X** | Interfacing with switching |
| **YG** | Yellow and green LEDs |

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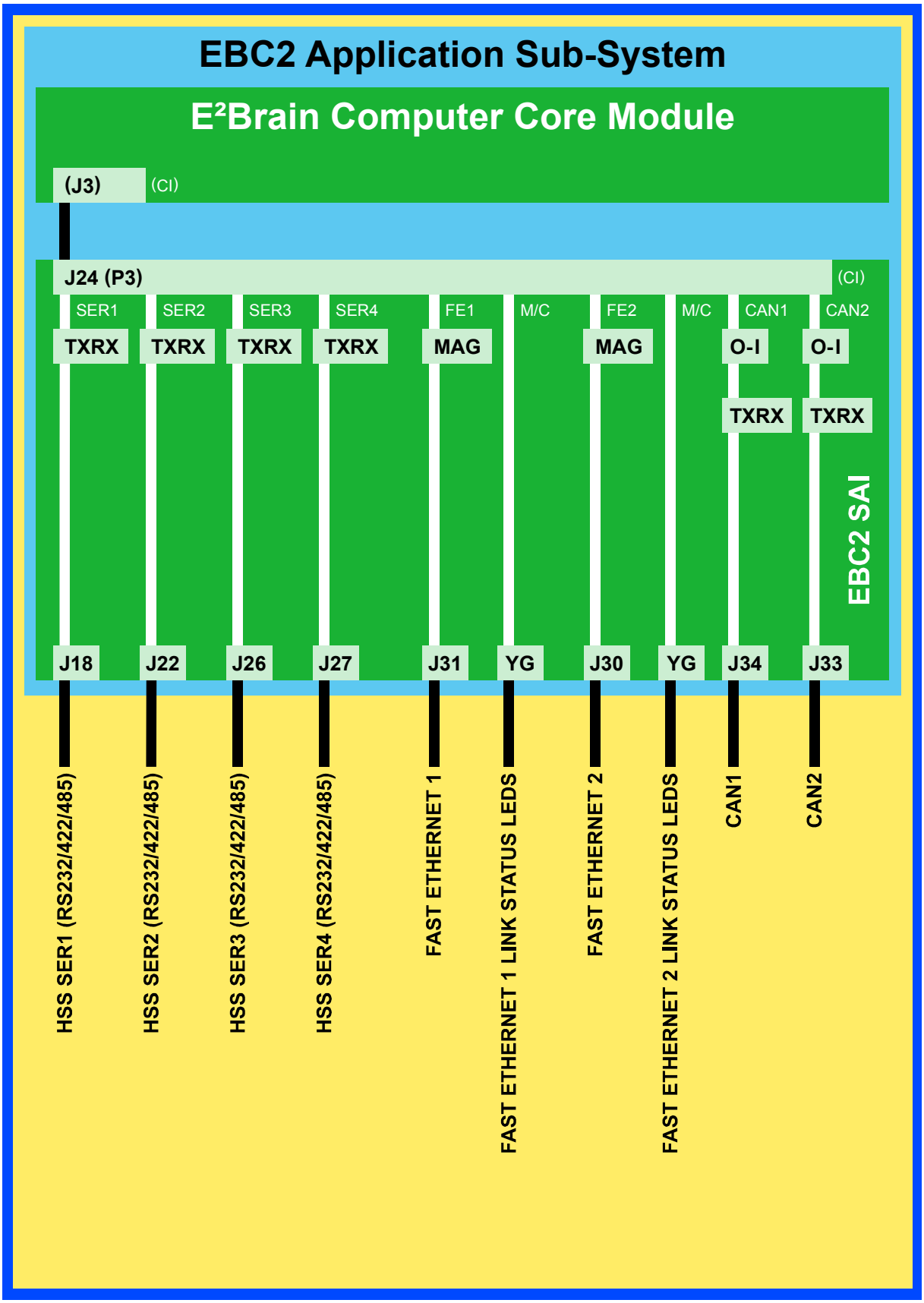
Figure 2-1: EBC2 Board Level Interfacing (1 of 5)





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Figure 2-2: EBC2 Board Level Interfacing (2 of 5)

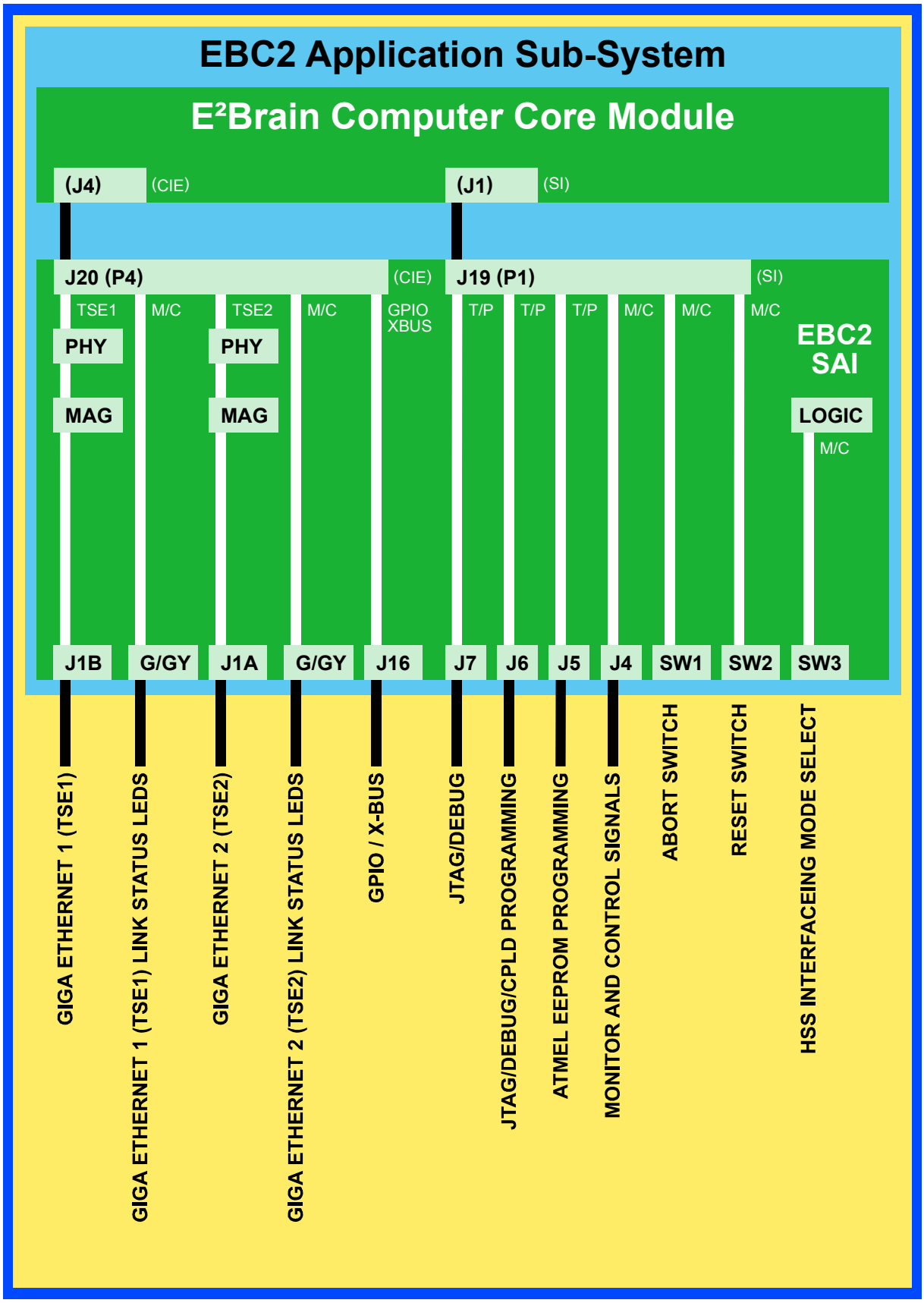




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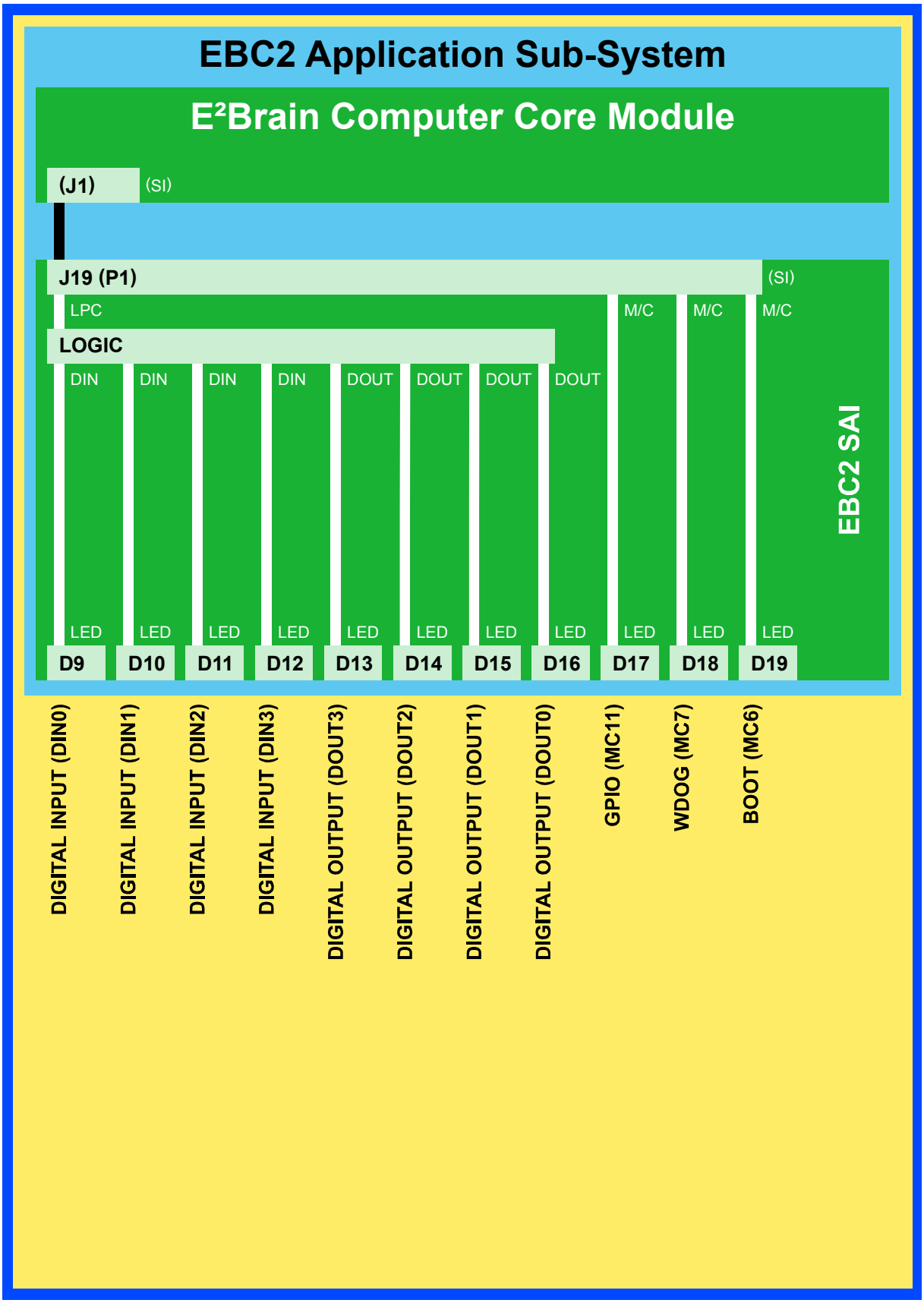
Figure 2-3: EBC2 Board Level Interfacing (3 of 5)





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Figure 2-4: EBC2 Board Level Interfacing (4 of 5)

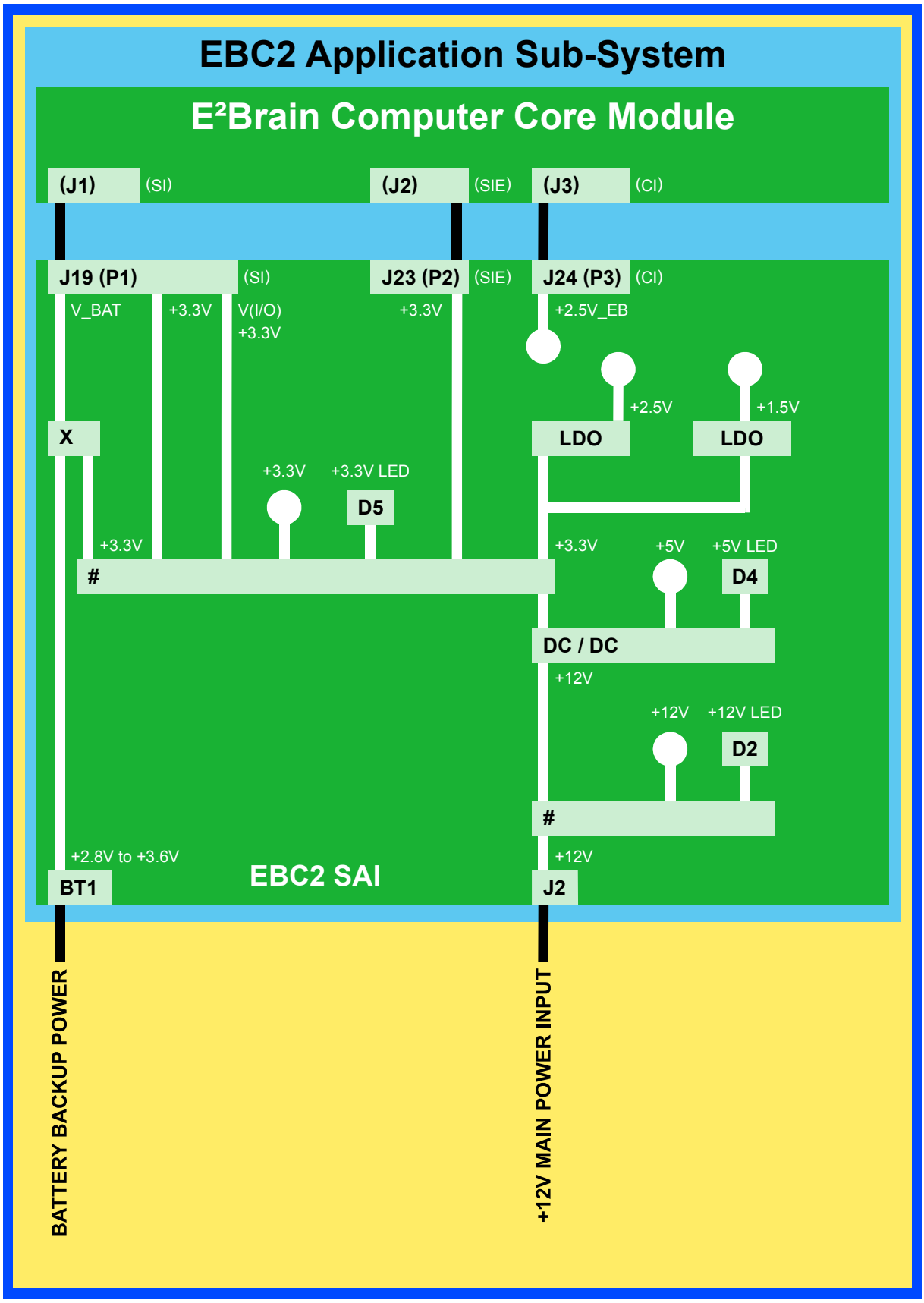




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Figure 2-5: EBC2 Board Level Interfacing (5 of 5)





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## 2.3 Embedded Module Interfaces

As the name implies, these interfaces provide the basic interfacing functionality required for the realization of E²Brain™ applications using the EBC2 as the development platform.

### 2.3.1 Embedded Module System Interface

The System Interface is realized using a 140-pin, HIROSE FX8C-140S-SV connector designated as J19 (P1). The following table provides an overview of the signal types and a brief description of the interfacing realized on this connector. The ensuing sections provide more detailed information concerning the signal specification for this interface.

**Table 2-1: System Interface J19 (P1) Signal Types**

| SIGNAL TYPE | DESCRIPTION |
|---|---|
| **POWER** | EBC2 E²Brain™ module input power, grounds, battery backup power, PCI signaling voltage V(I/O) |
| **MONITOR AND CONTROL (M/C)** | Monitor signals for LEDs and PCI operation. Control signals for E²Brain™ module operation |
| **TEST AND PROGRAMMING (T/P)** | JTAG, DEBUG, and system programming signals |
| **TERMINAL AND CONSOLE (T/C)** | Two serial interfaces: one for connecting a terminal and one for use as a console interface |
| **I2C** | One I2C standard interface for low speed, serial, inter-chip communications |
| **LPC** | One LPC standard interface for (GP)IOs and simple memory interfacing |
| **PCI** | One PCI standard interface for PCI-bus interfacing |

#### 2.3.1.1 J19 (P1) Connector Pinout

The following table provides signal pinouts along with information concerning signal characteristics for connector J19 (P1) of EBC2 E²Brain™ module.

**Figure 2-6: J19 - System Interface Connector (SI)**

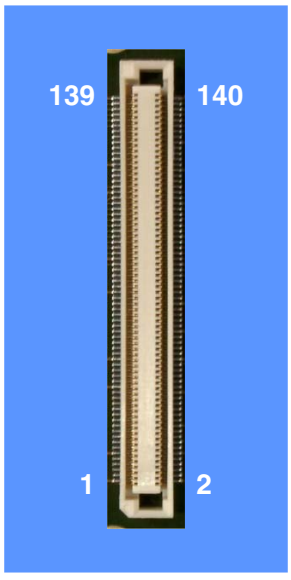



Table 2-2 notes:

1. Emulator VCC: is used to provide the applicable IO voltage to the emulator probe
2. Back-up power for the SRAM and RTC
3. Used in AGENT mode
4. DIR: signal direction is as viewed from the E²Brain™module.

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**Table 2-2: Pinout of J19 (P1) Connector**

| SIGNAL | DIR | SIGNAL GROUP | PIN | PIN | SIGNAL GROUP | DIR | SIGNAL |
|---|---|---|---|---|---|---|---|
| GND | I | POWER | 1 | 2 | POWER | I | AUX-Power (2 |
| SDA1 | I/O | I2C | 3 | 4 | I2C | I/O | SCL1 |
| MC6 | O | M/C | 5 | 6 | POWER | I | +3.3V |
| MC0 | I | M/C | 7 | 8 | M/C | O | MC7 |
| MC2 | I | M/C | 9 | 10 | M/C | I | MC1 |
| +3.3V | I | POWER | 11 | 12 | POWER | I | GND |
| MC3 | I | M/C | 13 | 14 | M/C | O | MC11 |
| MC4 | I | M/C | 15 | 16 | M/C | I | MC5 |
| MC9 | O | M/C | 17 | 18 | M/C | I | MC8 |
| GND | I | POWER | 19 | 20 | M/C | I/O | MC10 |
| LPCCLK | O | LPC | 21 | 22 | LPC | | RESERVED |
| LAD0 | I/O | LPC | 23 | 24 | LPC | I/O | LAD1 |
| LAD2 | I/O | LPC | 25 | 26 | POWER | I | +3.3V |
| LFRAME# | O | LPC | 27 | 28 | POWER | I | GND |
| SERIRQ# | I/O | LPC | 29 | 30 | LPC | I/O | LAD3 |
| TxD1 (TERM) | O | T/C | 31 | 32 | LPC | | RESERVED |
| +3.3V | I | POWER | 33 | 34 | T/C | O | TxD2 (CONS) |
| GND | I | POWER | 35 | 36 | T/C | I | RxD2 (CONS) |
| RxD1 (TERM) | I | T/C | 37 | 38 | T/P | I | CKSTP_IN |
| EMU_VCC (1 | O | T/P | 39 | 40 | T/P | I | COP-HRST/HRESET |
| CKSTP_OUT | O | T/P | 41 | 42 | POWER | I | GND |
| COP-SRST/SRESET | I | T/P | 43 | 44 | T/P | I | TMS |
| TRST | I | T/P | 45 | 46 | POWER | I | +3.3V |
| TCK | I | T/P | 47 | 48 | T/P | O | TDO |
| RESERVED | | I2C | 49 | 50 | T/P | I | TDI |
| GND | I | POWER | 51 | 52 | I2C | | RESERVED |
| PCI-CLK-OUT-0 | O | PCI | 53 | 54 | POWER | I | V(I/O) |
| +3.3V | I | POWER | 55 | 56 | PCI | I | PCI-CLK-IN (3 |
| PCI-CLK-OUT-1 | O | PCI | 57 | 58 | POWER | I | GND |
| PCI-RST# | I/O | PCI | 59 | 60 | PCI | O | PCI-CLK-OUT-2 |
| INTA# | I/O | PCI | 61 | 62 | PCI | I | INTC# |
| INTB# | I | PCI | 63 | 64 | PCI | I/O | GNT#1 |
| INTD# | I | PCI | 65 | 66 | POWER | I | +3.3V |
| GND | I | POWER | 67 | 68 | PCI-MASTER | O | GNT#2 |
| AD31 | I/O | PCI | 69 | 70 | PCI-MASTER | O | GNT#3 |


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**Table 2-2: Pinout of J19 (P1) Connector**

| SIGNAL | DIR | SIGNAL GROUP | PIN | PIN | SIGNAL GROUP | DIR | SIGNAL |
|---|---|---|---|---|---|---|---|
| AD29 | I/O | PCI | 71 | 72 | PCI | I/O | REQ#1 |
| AD27 | I/O | PCI | 73 | 74 | PCI-MASTER | I | REQ#2 |
| +3.3V | I | POWER | 75 | 76 | POWER | I | GND |
| AD25 | I/O | PCI | 77 | 78 | PCI-MASTER | I | REQ#3 |
| C/BE3# | I/O | PCI | 79 | 80 | PCI | I/O | AD30 |
| AD23 | I/O | PCI | 81 | 82 | PCI | I/O | AD28 |
| GND | I | POWER | 83 | 84 | PCI | I/O | AD26 |
| AD21 | I/O | PCI | 85 | 86 | PCI | I/O | AD24 |
| V(I/O) | I | POWER | 87 | 88 | POWER | I | +3.3V |
| AD19 | I/O | PCI | 89 | 90 | PCI | I/O | IDSEL |
| AD17 | I/O | PCI | 91 | 92 | POWER | I | GND |
| C/BE2# | I/O | PCI | 93 | 94 | PCI | I/O | AD22 |
| +3.3V | I | POWER | 95 | 96 | PCI | I/O | AD20 |
| IRDY# | I/O | PCI | 97 | 98 | PCI | I/O | AD18 |
| DEVSEL# | I/O | PCI | 99 | 100 | PCI | I/O | AD16 |
| GND | I | POWER | 101 | 102 | PCI | I/O | FRAME# |
| PCI-X-CAP | I/O | PCI | 103 | 104 | POWER | I | GND |
| LOCK# | I/O | PCI | 105 | 106 | PCI | I/O | TRDY# |
| PERR# | I/O | PCI | 107 | 108 | PCI | I/O | STOP# |
| SERR# | I/O | PCI | 109 | 110 | POWER | I | +3.3V |
| GND | I | POWER | 111 | 112 | PCI | I/O | PAR |
| C/BE1# | I/O | PCI | 113 | 114 | PCI | I/O | AD15 |
| AD14 | I/O | PCI | 115 | 116 | POWER | I | V(I/O) |
| AD12 | I/O | PCI | 117 | 118 | PCI | I/O | AD13 |
| AD10 | I/O | PCI | 119 | 120 | PCI | I/O | AD11 |
| +3.3V | I | POWER | 121 | 122 | PCI | I/O | AD9 |
| M66EN | I/O | PCI | 123 | 124 | POWER | I | GND |
| AD8 | I/O | PCI | 125 | 126 | PCI | I/O | C/BE0# |
| AD7 | I/O | PCI | 127 | 128 | PCI | I/O | AD6 |
| AD5 | I/O | PCI | 129 | 130 | POWER | I | +3.3V |
| GND | I | POWER | 131 | 132 | PCI | I/O | AD4 |
| AD3 | I/O | PCI | 133 | 134 | PCI | I/O | AD2 |
| AD1 | I/O | PCI | 135 | 136 | PCI | I/O | AD0 |
| ACK64# | I/O | PCI | 137 | 138 | PCI | I/O | REQ64# |
| +3.3V | I | POWER | 139 | 140 | POWER | I | GND |

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### 2.3.1.2 Power Interface

For the EBC2 E²Brain™ module, a single power supply voltage of 3.3 VDC is specified. The following table summarizes the power specifications.

**Table 2-3: EBC2 Power Interface Requirements**

| VOLTAGE | DESCRIPTION |
|---|---|
| + 3.3 VDC | Input voltage tolerance: +5% to -3%<br>Supply voltage ripple: 100 mV peak-to-peak |
| GND | Ground voltage reference input |
| AUX-Power | Optional auxiliary power input for battery backup of RTC and/or SRAM devices |
| V(I/O) | PCI signalling voltage selection. The EBC2 only supports 3.3V PCI signalling. |

### 2.3.1.3 Monitor and Control Interface

This interface is comprised of a set of twelve IO signals which can be used to facilitate system integration.

The following table provides a listing of Monitor and Control signals along with a brief description.

**Table 2-4: Monitor and Control Interface Signal Description**

| SIGNAL | PIN | DESCRIPTION |
|---|---|---|
| MC0 | 7 | Input (refer to the respective E²Brain™ module documentation for details) |
| MC1 | 10 | Input (refer to the respective E²Brain™ module documentation for details) |
| MC2 | 9 | Input (refer to the respective E²Brain™ module documentation for details) |
| MC3 | 13 | Input (refer to the respective E²Brain™ module documentation for details) |
| MC4 | 15 | Input (refer to the respective E²Brain™ module documentation for details) |
| MC5 | 16 | Input (refer to the respective E²Brain™ module documentation for details) |
| MC6 | 5 | Output (refer to the respective E²Brain™ module documentation for details) |
| MC7 | 8 | Output (refer to the respective E²Brain™ module documentation for details) |
| MC8 | 18 | Input (refer to the respective E²Brain™ module documentation for details) |
| MC9 | 17 | Output (refer to the respective E²Brain™ module documentation for details) |
| MC10 | 20 | Output (refer to the respective E²Brain™ module documentation for details) |
| MC11 | 14 | Output (refer to the respective E²Brain™ module documentation for details) |

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### 2.3.1.4 Test and Programming Interface

The Test and Programming interface supports JTAG/DEBUG and ISP operations. This interface can be used for connecting hardware emulators and debuggers (COP), and for “in system programming” (ISP) of programmable hardware as well as in system testing (JTAG). It is comprised of a set of six signals whereby some are common to all three interfaces and some are dedicated to only one.

The following table provides a listing of the Test and Programming interface signals and a brief description.

**Table 2-5: Test and Programming Interface Signal Description**

| SIGNAL | DESCRIPTION |
|---|---|
| TCK | Test Clock in for JTAG/ISP and emulator/debugger |
| TDI | Test Data In for JTAG/ISP and emulator/debugger |
| TDO | Test Data Out JTAG/ISP and emulator/debugger |
| TMS | Test Mode Select, input for JTAG/ISP and emulator/debugger |
| TRST | Test Reset, input for JTAG/ISP and emulator/debugger |
| COP_HRST/HRST | Hard Reset, emulator/debugger hard reset In |
| COP_SRST/SRESET | Soft Reset, emulator/debugger soft reset In |
| CKSTP_IN | Emulator/debugger specific signal |
| CKSTP_OUT | Emulator/debugger specific signal |
| EMU_VCC | Reference Voltage of the JTAG/DEBUG core |

### 2.3.1.5 Terminal and Console Interface

The EBC2 provides two serial interfaces for supporting a terminal port and a low speed communications interface (console) for firmware updating. These interfaces are realized using the CPU on-chip dual UART, and as such provide only a two wire interface without hardware handshake signals.

The following table provides a listing of the Terminal and Console interface signals and a brief description.

**Table 2-6: Terminal and Console Interface Signal Description**

| SIGNAL | DESCRIPTION |
|---|---|
| TxD1, TxD2 (TERM, CONS) | Serial Transmit Data outputs, channel 1 and 2 |
| RxD1, RxD2 (TERM, CONS) | Serial Receive Data signal inputs, channel 1 and 2 |

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### 2.3.1.6 I2C Interface

The EBC2 E²Brain™ module provides one I2C serial interface for supporting direct interfacing to the EBC2 carrier board devices. This interface is two signals wide and fully supports the I2C specification.

The following table provides a listing of the I2C interface signals and a brief description.

**Table 2-7: I2C Interface Signal Description**

| SIGNAL | DESCRIPTION |
|---|---|
| SCL1 | Serial Clock line, channel 1 |
| SDA1 | Serial Data line, channel 1 |

### 2.3.1.7 LPC Interface

One Low Pin Count (LPC) interface for supporting simple IOs, simple static memory devices, and IO controllers is available to the EBC2.

The controller is completely integrated in the E²Brain™ module and offers an 8-bit data access port to devices which use LPC IO or memory access protocols. I/O and memory area are selected using different address spaces.

The I/O address space is 64 kByte in size, whereas the memory area offers 16 MByte address space. For respective address mapping, refer to the corresponding E²Brain™module documentation.

In addition, a serial IRQ controller is also implemented in the E²Brain™ module, controlling and collecting the serial LPC IRQs and converting and processing them to IRQs for the CPU. DMA, however, is not supported by this interface.

The following table provides a listing of the LPC interface signals and a brief description.

**Table 2-8: LPC Interface Signal Description**

| SIGNAL | DESCRIPTION |
|---|---|
| LAD[0:3] | Multiplexed Command, Address, and Data lines |
| LFRAME# | Indicates start of a new cycle, termination of broken cycle |
| LPCCLK | 33 MHz clock |
| SERIRQ | Serialized IRQ, optional for peripherals that need interrupt |

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### 2.3.1.8 PCI Interface

In contrast to all other PCI based modules, the E²Brain™ modules are capable of both PCI Master mode and PCI Agent mode. PCI Agent mode can be selected by setting the AGENT signal on the System Interface to low.

In PCI Master mode (default by the EBC2), the E²Brain™ module operates as the host, initializing and controlling up three PCI devices on the EBC2, whereas, in the Agent mode, the E²Brain™ module itself operates as a PCI target.

The following table identifies the EBC2 PCI bus signals and provides a short description of each signal.

**Table 2-9: PCI Interface Signal Description**

| SIGNAL | DESCRIPTION |
|---|---|
| AD [0:31] | PCI multiplexed address and data bus |
| INT [A, B, C, D]# | PCI interrupt requests |
| C/BE [0:3]# | PCI multiplexed bus command and byte enable |
| IRDY# | Initiator Ready indicates the current bus master is ready to complete the current data phase. |
| TRDY# | Target Ready indicates the selected device is ready to complete the current data phase. |
| PCI-RST# | PCI Reset signal, is also used for LPC devices |
| PCI-CLK-OUT- [1:3] | PCI clock Outputs for up to 3 external bus mastering PCI devices. All PCI signals except PCI_RST#, and INT [A, B, C, D] # are sampled on the rising edge. (Consider routing guidelines for Carrier board) |
| FRAME# | Indicate the beginning and duration of a PCI access. |
| STOP# | Indicates the target is requesting the master to stop the current transaction |
| DEVSEL# | Device select generated by the target when cycle refers to its own address. |
| REQ [1:3]# | PCI Arbiter requests |
| GNT [1:3]# | PCI Arbiter grants |
| PAR | Calculated/Checked Parity |
| PERR# | Parity Error |
| LOCK# | PCI Lock resource signal |
| SERR# | System Error |
| REQ64# | PCI request for a 64-bit access |
| ACK64# | PCI grant for a 64-bit access |
| PCI-CLK-IN | PCI clock input, used in agent mode |
| AGENT | PCI-agent mode logic input, 0 -> PCI agent mode, 1 -> system controller |
| M66EN | 66 MHz enable |
| PCI-X-CAP | PCI-X capable |


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### 2.3.2 System Interface Extension

The System Interface Extension is realized using an 80-pin, HIROSE FX8C-80S-SV connector designated as J23 (P2), and it is used to provide CPU architecture specific system interfaces.

In the case of the EBC2, a CompactFlash interface, a GPIO interface (EB405), and two USB interfaces are available on the System Interface Extension. The following sections provide further information concerning these interfaces.

#### 2.3.2.1 J23 (P2) Connector Pinout

The following figure and table provide pinout information for J23 (P2).

**Figure 2-7: J23 - System Interface Extension Connector (SIE)**

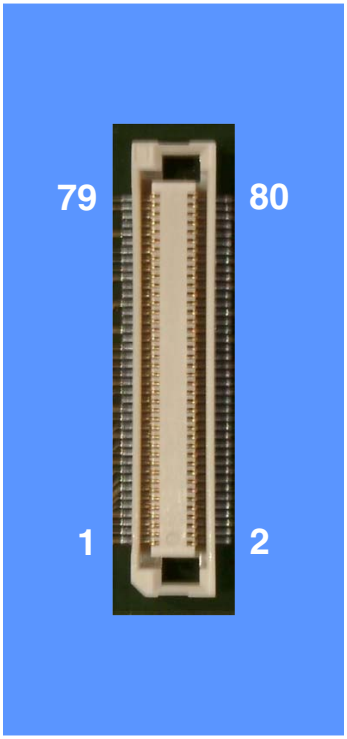



**Table 2-10: Pinout of J23 (P2) Connector**

| SIGNAL | PIN | PIN | SIGNAL | SIGNAL | PIN | PIN | SIGNAL |
|---|---|---|---|---|---|---|---|
| GND | 1 | 2 | CF_CD1 | CF_D9 | 41 | 42 | GND |
| CF_D3 | 3 | 4 | CF_D11 | V(I/O) | 43 | 44 | CF_CS16 |
| CF_D4 | 5 | 6 | +3.3V | CF_D10 | 45 | 46 | CF_CD2 |
| +3.3V | 7 | 8 | CF_D12 | ATA_ DMARQ | 47 | 48 | GND |
| CF_D5 | 9 | 10 | CF_D13 | +3.3V | 49 | 50 | ATA/DMACK |
| CF_D6 | 11 | 12 | GND | NC | 51 | 52 | NC |
| GND | 13 | 14 | CF_D14 | NC | 53 | 54 | GND |
| CF_D7 | 15 | 16 | CF_D15 | GND | 55 | 56 | NC |
| CF_CS0 | 17 | 18 | +3.3V | USB_OC | 57 | 58 | NC |
| GND | 19 | 20 | CF_CS1 | USB_PO | 59 | 60 | +3.3V |
| CF_RD | 21 | 22 | CF_WR | GND | 61 | 62 | GPIO(0) |
| CF_INTRQ | 23 | 24 | GND | GPIO(15) | 63 | 64 | GPIO(16) |
| GND | 25 | 26 | CF_RST | GPIO(14) | 65 | 66 | GND |
| CF_IORDY | 27 | 28 | CF_A2 | GPIO(30) | 67 | 68 | GPIO(31) |
| CF_A1 | 29 | 30 | GND | NC | 69 | 70 | USB1_OTG _EXVBO |
| +3.3V | 31 | 32 | CF_A0 | +3.3V | 71 | 72 | USB1_OTG _VBP |
| CF_DASP | 33 | 34 | CF_D0 | NC | 73 | 74 | USB1_OTG _VBUS |
| CF_PDIAG | 35 | 36 | +3.3V | USB1_OTG _ID | 75 | 76 | GND |
| GND | 37 | 38 | CF_D1 | USB1+ | 77 | 78 | USB2+ |
| CF_D8 | 39 | 40 | CF_D2 | USB1- | 79 | 80 | USB2- |


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### 2.3.2.2 CompactFlash Interface

The following table provides a summary of the CompactFlash signals implemented on the System Interface Extension connector.

**Table 2-11: CompactFlash Interface Signals**

| SIGNAL | DESCRIPTION |
|---|---|
| CF-D[0:15] | Compact Flash data bus – 16-bit wide |
| CF-CS[0:1] | Compact Flash chip select |
| CF-RD | Compact Flash IO read strobe |
| CF-WR | Compact Flash IO write strobe |
| CF-RST | Compact Flash reset, active low |
| CF-INTRQ | Compact Flash interrupt request, active high |
| CF-IORDY | Compact Flash IO ready |
| CF-A[0:2] | Compact Flash address lines |

The CompactFlash interface is realized as a true IDE interface (PIO mode). The PC CARD Memory Mode and the PC Card I/O Mode of the Compact Flash Specification are not supported. In addition, the pinout for the Compact Flash signals have been optimized for routing to a CompactFlash socket.

### 2.3.2.3 GPIO Interfacing

The EBC2 module provides a subset of six of the PPC405EP general purpose digital input/output signals on this connector. The signals GPIO[00, 14, 15, 16, 30, and 31] are available for applications requiring digital IO. These signals are implemented as 3.3V TTL for direct CPU interfacing.

**Table 2-12: GPIO Interface Signals**

| SIGNAL | DESCRIPTION | SIGNAL | DESCRIPTION |
|---|---|---|---|
| GPIO(0) | General purpose IO | GPIO(16) | General purpose IO |
| GPIO(14) | General purpose IO | GPIO(30) | General purpose IO |
| GPIO(15) | General purpose IO | GPIO(31) | General purpose IO |

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### 2.3.2.4 USB Interfaces

The following table provides a summary of the USB signals implemented on the System Interface Extension connector.

**Table 2-13: USB Interface Signals**

| SIGNAL | DESCRIPTION |
|---|---|
| USB1+ | Serial data + interface 1 |
| USB1- | Serial data - interface 1 |
| USB2+ | Serial data + interface 2 |
| USB2- | Serial data - interface 2 |
| USB_OC | Over current condition indicator for Host ports |
| USB_PO | Power ON/OFF control for Host ports |
| USB_OTG_EXVBO | ON/OFF control of external VBUS (5V) for OTG operation |
| USB_OTG_VBP | VBUS pulsing control for OTG operation |
| USB_OTG_VBUS | VBUS input for OTG operation |
| USB_OTG_ID | Connected to ID pin of the USB Mini AB connector (input for OTG opeation) |


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### 2.3.3 Communications Interface

The Communications Interface Connector J24 (P3), is used to provide a set of standard communications interfaces. In the case of the EBC2, there are three types of interfaces provided: four high speed serial interfaces, two Fast Ethernet interfaces, and two CAN interfaces.

All of these interfaces are provided on the Communications Interface J24 (P3) connector (an 80-pin, HIROSE FX8C-80S-SV connector).

The following figure and table provide pinout information for J24 (P3).

**Figure 2-8: J24 - Communications Interface Connector (CI)**

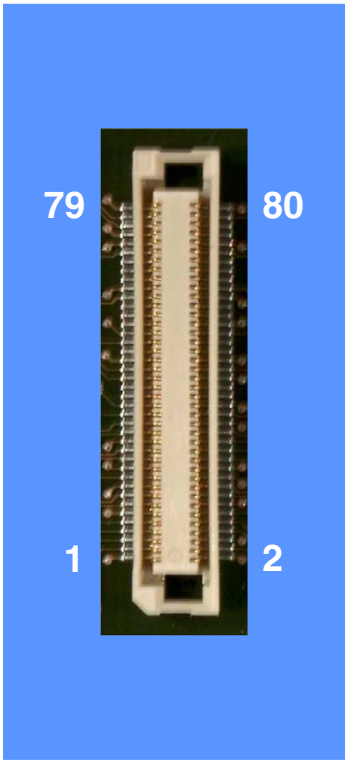



**Table 2-14: Pinout of J24 (P3) Connector**

| SIGNAL | PIN | PIN | SIGNAL | SIGNAL | PIN | PIN | SIGNAL |
|---|---|---|---|---|---|---|---|
| GND | 1 | 2 | GND | CAN1_TXD0 | 41 | 42 | CAN1_RXD0 |
| SER_DSR1/ TCLK1 | 3 | 4 | SER_RI1/ RCLK1 | CAN1_TXD1 | 43 | 44 | CAN1_RXD1 |
| SER_RTS1 | 5 | 6 | SER_CTS1 | GND | 45 | 46 | GND |
| SER_TXD1 | 7 | 8 | SER_RXD1 | NC | 47 | 48 | NC |
| SER_DTR1 | 9 | 10 | SER_CD1 | ETH2_LINK | 49 | 50 | NC |
| GND | 11 | 12 | SER_RI2/ RCLK2 | ETH2_ACT | 51 | 52 | ETH2_SPEED |
| SER_DSR2/ TCLK2 | 13 | 14 | SER_CTS2 | NC | 53 | 54 | GND |
| SER_RTS2 | 15 | 16 | SER_RXD2 | NC | 55 | 56 | NC |
| SER_TXD2 | 17 | 18 | SER_CD2 | NC | 57 | 58 | NC |
| SER_DTR2 | 19 | 20 | SER_RI3/ RCLK3 | ETH2_T- | 59 | 60 | ETH2_R- |
| SER_DSR3/ TCLK3 | 21 | 22 | GND | ETH2_T+ | 61 | 62 | ETH2_R+ |
| SER_RTS3/ TXFRAME3 | 23 | 24 | SER_CTS3/ RXFRAME3 | +2.5V_EB | 63 | 64 | +2.5V_EB |
| SER_TXD3 | 25 | 26 | SER_RXD3 | NC | 65 | 66 | NC |
| SER_DTR3 | 27 | 28 | SER_CD3 | NC | 67 | 68 | NC |
| SER_DSR4/ TCLK4 | 29 | 30 | SER_RI4/ RCLK4 | ETH1_T- | 69 | 70 | ETH1_R- |
| SER_RTS4/ TXFRAME4 | 31 | 32 | SER_CTS4/ RXFRAME4 | ETH1_T+ | 71 | 72 | ETH1_R+ |
| SER_TXD4 | 33 | 34 | SER_RXD4 | GND | 73 | 74 | NC |
| SER_DTR4 | 35 | 36 | SER_CD4 | ETH1_LINK | 75 | 76 | NC |
| CAN2_TXD0 | 37 | 38 | CAN2_RXD0 | ETH1_ACT | 77 | 78 | ETH1_SPEED |
| CAN2_TXD1 | 39 | 40 | CAN2_RXD1 | GND | 79 | 80 | GND |

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### 2.3.3.1 High Speed Serial Interfaces

Four, full modem, serial ports (SER1, 2, 3 and 4) are available on the EBC2 SAI. Depending on the E²Brain™ module employed with the EBC2 up to eight signals per port are provided to realize asynchronous or synchronous (EB425) high speed serial links interfaced using dedicated controlling/handshaking.

The following table provides a summary of the HSS signals implemented on the Communications Interface connector.

**Table 2-15: High Speed Serial Interface Signal Type and Description**

| SIGNAL | DESCRIPTION |
|---|---|
| TXD | Transmit data output |
| RXD | Receive data input |
| RTS/TXFRAME | Request to send output; transmit frame signal for synchronous transmission |
| CTS/RXFRAME | Clear to send input; receive frame signal for synchronous transmission |
| DTR | Data terminal ready output |
| CD | Carrier detect input |
| TCLK/DSR | Transmit clock for synchronous transmissions/Data set ready input |
| RCLK/RI | Receive clock for synchronous transmissions/Ring indicator input |

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### 2.3.3.2 Ethernet Interface

The EBC2 SAI provides two Fast Ethernet interfaces: FE1 and FE2.

For monitoring and control purposes, LED functionality is provided to indicate activity, link, and speed status information for the respective interfaces.

**Table 2-16: Ethernet Port Signal Type and Description**

| SIGNAL | DESCRIPTION |
|---|---|
| ETH1_T+, ETH2_T+ | Transmit pair in 10BaseT/100BaseTX configuration |
| ETH1_T-, ETH2_T- | |
| ETH1_R+, ETH2_R+ | Receive pair in 10BaseT/100BaseTX configuration |
| ETH1_R-, ETH2_R- | |
| ETH1_LINK, ETH2_LINK | Indicates that link is present<br>Asserted: link is present |
| ETH1_ACT, ETH2_ACT | Indicates that link is actively transmitting data<br>Asserted intermittently: traffic on link |
| ETH1_SPEED,<br>ETH2_SPEED | Indicates link speed<br>Not asserted: 10 Mb<br>Asserted: 100 Mb |

### 2.3.3.3 CAN Interface

The EBC2 SAI provides two Controller Area Network (CAN) interfaces. Defaultwise, CAN TXD/RXD0 is implemented on the EBC2. If CAN TXD/RXD1 is required, it must be specified when ordering the EBC2. In addition, the default configuration for this interface is with opto-isolation. If non-opto-isolation is required, it also must be specified when ordering.

The following table provides a summary of the CAN signals implemented on the Communications Interface connector.

**Table 2-17: CAN Port Signal Type and Description**

| SIGNAL | DESCRIPTION |
|---|---|
| CAN1_TXD0, CAN2_TXD0 | Transmit data output driver (default) |
| CAN1_RXD0, CAN2_RXD0 | Receive data input channel (default) |
| CAN1_TXD1, CAN2_TXD1 | Transmit data output driver |
| CAN1_RXD1, CAN2_RXD1 | Receive data input channel |

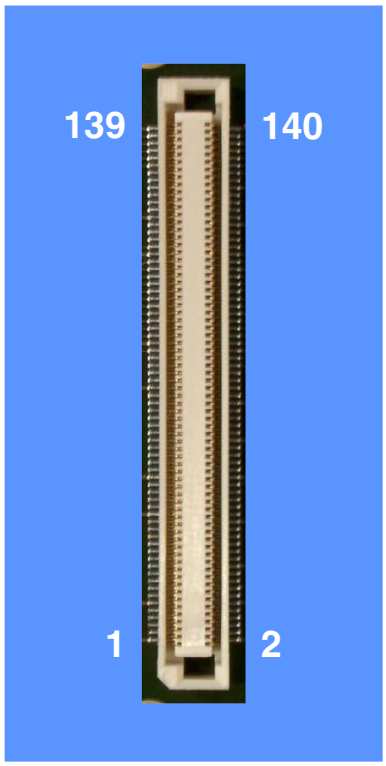
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### 2.3.4 Communications Interface Extension

The Communications Interface Extension is realized using a 140-pin, HIROSE FX8C-140S-SV connector designated as J20 (P4). The following table provides signal pinouts along with information concerning signal characteristics for connector J20 (P4) of the EBC2 SAI. The signal direction is as viewed from the E²Brain™ module.

**Figure 2-9: J20 - Communications Interface Extension Connector (CIE)**





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**Table 2-18: Pinout of J20 (P4) Connector**

| SIGNAL | DIR | SIGNAL GROUP | PIN | PIN | SIGNAL GROUP | DIR | SIGNAL |
|---|---|---|---|---|---|---|---|
| GND | I | POWER | 1 | 2 | POWER | I | GND |
| DIO0 | I/O | - | 3 | 4 | - | I/O | DIO1 |
| DIO2 | I/O | - | 5 | 6 | - | I/O | DIO3 |
| DIO4 | I/O | - | 7 | 8 | - | I/O | DIO5 |
| DIO6 | I/O | - | 9 | 10 | - | I/O | DIO7 |
| GND | I/O | POWER | 11 | 12 | POWER | I | GND |
| X_DATA7 | I/O | - | 13 | 14 | - | I/O | X_DATA6 |
| X_DATA5 | I/O | - | 15 | 16 | - | I/O | X_DATA4 |
| X_DATA3 | I/O | - | 17 | 18 | - | I/O | X_DATA2 |
| X_DATA1 | I/O | - | 19 | 20 | - | I/O | X_DATA0 |
| X_ADDR9 | O | - | 21 | 22 | POWER | I | GND |
| X_ADDR7 | O | - | 23 | 24 | - | O | X_ADDR8 |
| X_ADDR5 | O | - | 25 | 26 | - | O | X_ADDR6 |
| X_ADDR3 | O | - | 27 | 28 | - | O | X_ADDR4 |
| X_ADDR1 | O | - | 29 | 30 | - | O | X_ADDR2 |
| NC | - | - | 31 | 32 | - | O | X_ADDR0 |
| NC | - | - | 33 | 34 | POWER | I | GND |
| GND | I | POWER | 35 | 36 | - | - | NC |
| NC | - | - | 37 | 38 | - | - | NC |
| NC | - | - | 39 | 40 | - | - | NC |
| NC | - | - | 41 | 42 | - | - | NC |
| NC | - | - | 43 | 44 | - | - | NC |
| GND | I | POWER | 45 | 46 | POWER | I | GND |
| NC | - | - | 47 | 48 | - | - | NC |
| NC | - | - | 49 | 50 | - | - | NC |
| NC | - | - | 51 | 52 | - | - | NC |
| NC | - | - | 53 | 54 | - | - | NC |
| NC | - | - | 55 | 56 | POWER | I | GND |
| NC | - | - | 57 | 58 | - | - | NC |
| NC | - | - | 59 | 60 | - | - | NC |
| NC | - | - | 61 | 62 | - | - | NC |
| NC | - | - | 63 | 64 | - | - | NC |
| NC | - | - | 65 | 66 | POWER | I | GND |
| NC | - | - | 67 | 68 | - | - | NC |
| GND | I | POWER | 69 | 70 | - | - | NC |

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**Table 2-18: Pinout of J20 (P4) Connector**

| SIGNAL | DIR | SIGNAL GROUP | PIN | PIN | SIGNAL GROUP | DIR | SIGNAL |
|---|---|---|---|---|---|---|---|
| TSEC2_GTX_CLK | O | GMII2 | 71 | 72 | PHY2_CLK | I | EC_GTX2_CLK125 |
| NC | - | - | 73 | 74 | - | - | NC |
| EC_GTX1_CLK125 | I | PHY1_CLK | 75 | 76 | GMII2 | O | TSEC2_TXD[7] |
| NC | - | - | 77 | 78 | GMII2 | O | TSEC2_TXD[5] |
| TSEC2_TXD[6] | O | GMII2 | 79 | 80 | POWER | I | GND |
| GND | I | POWER | 81 | 82 | GMII2 | O | TSEC2_TXD[3] |
| TSEC2_TXD[4] | O | GMII2 | 83 | 84 | GMII2 | O | TSEC2_TXD[1] |
| TSEC2_TXD[2] | O | GMII2 | 85 | 86 | GMII2 | I | TSEC2_RXD[1] |
| TSEC2_TXD[0] | O | GMII2 | 87 | 88 | GMII2 | I | TSEC2_RXD[3] |
| TSEC2_RXD[0] | I | GMII2 | 89 | 90 | POWER | I | GND |
| TSEC2_RXD[2] | I | GMII2 | 91 | 92 | GMII2 | I | TSEC2_RXD[5] |
| TSEC2_RXD[4] | I | GMII2 | 93 | 94 | GMII2 | I | TSEC2_RXD[7] |
| TSEC2_RXD[6] | I | GMII2 | 95 | 96 | GMII2 | I | TSEC2_CRS |
| TSEC2_COL | I | GMII2 | 97 | 98 | GMII2 | O | TSEC2_TX_EN |
| TSEC2_TX_ER | O | GMII2 | 99 | 100 | GMII2 | I | TSEC2_RX_CLK |
| TSEC2_RX_DV | I | GMII2 | 101 | 102 | POWER | I | GND |
| EC_MDIO2 | I | PHY2_MANAGE | 103 | 104 | GMII2 | I | TSEC2_TX_CLK |
| GND | I | POWER | 105 | 106 | GMII2 | I | TSEC2_RX_ER |
| EC_MDC2 | O | PHY2_MANAGE | 107 | 108 | GMII1 | O | TSEC1_TXD[7] |
| TSEC1_TXD[6] | O | GMII1 | 109 | 110 | GMII1 | O | TSEC1_TXD[5] |
| TSEC1_TXD[4] | O | GMII1 | 111 | 112 | GMII1 | O | TSEC1_TXD[3] |
| TSEC1_TXD[2] | O | GMII1 | 113 | 114 | POWER | I | GND |
| GND | I | POWER | 115 | 116 | GMII1 | O | TSEC1_TXD[1] |
| TSEC1_TXD[0] | O | GMII1 | 117 | 118 | GMII1 | I | TSEC1_RXD[1] |
| TSEC1_RXD[0] | I | GMII1 | 119 | 120 | GMII1 | I | TSEC1_RXD[3] |
| TSEC1_RXD[2] | I | GMII1 | 121 | 122 | GMII1 | I | TSEC1_RXD[5] |
| TSEC1_RXD[4] | I | GMII1 | 123 | 124 | POWER | I | GND |
| TSEC1_RXD[6] | I | GMII1 | 125 | 126 | GMII1 | I | TSEC1_RXD[7] |
| TSEC1_COL | I | GMII1 | 127 | 128 | GMII1 | O | TSEC1_CRS |
| TSEC1_TX_ER | O | GMII1 | 129 | 130 | GMII1 | I | TSEC1_TX_EN |
| TSEC1_RX_DV | I | GMII1 | 131 | 132 | GMII1 | I | TSEC1_RX_ER |
| EC_MDIO1 | I/O | PHY1_MANAGE | 133 | 134 | GMII1 | I | TSEC1_RX_CLK |
| TSEC1_GTX_CLK | O | GMII1 | 135 | 136 | POWER | I | GND |
| EC_MDC1 | O | PHY1_MANAGE | 137 | 138 | GMII1 | O | TSEC1_TX_CLK |
| GND | I | POWER | 139 | 140 | POWER | I | GND |


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### 2.3.4.1 Gigabit Ethernet Interface

The E²Brain™ modules provide up to two three speed Ethernet (GMII) interfaces (TSEC1 and TSEC2) whose signals are already at TTL level. The EBC2 carrier board provides the PHY, galvanic isolation (magnetics) function, and the appropriate connector type for each Ethernet interface.

**Table 2-19: Gigabit Ethernet Signal Type and Description**

| SIGNAL | I/O | DESCRIPTION |
|---|---|---|
| TSECn_COL | I | Collision |
| TSECn_CRS | I | Carrier sense |
| TSECn_GTX_CLK | O | Transmit clock |
| EC_GTX_CLK125 | I | Oscillator source for GMII |
| EC_MDC | O | Management clock |
| EC_MDIO | I/O | Management data |
| TSECn_RX_CLK | I | Receive clock |
| TSECn_RX_DV | I | Receive data valid |
| TSECn_RXD[7:0] | I | Receive data bits 7:0 |
| TSECn_RX_ER | I | Receive error |
| TSECn_TX_CLK | I | Transmit clock |
| TSECn_TXD[7:0] | O | Transmit data bits 7:0 |
| TSECn_TX_EN | O | Transmit data valid |
| TSECn_TX_ER | O | Transmit error |

## 2.3.5 Monitor and Control (M/C)

Monitor and Control functions are divided essentially into Pre-operation and Operation. Pre-operation M/C deals with board configuration and system requirements. Operation M/C covers direct operational interfaces.

### 2.3.5.1 Pre-Operation M/C

Pre-operation M/C is a direct function of the application and the system requirements. These requirements dictate the EBC2 configuration as well as the overall system integration. Overall system integration and compliance with its requirements is beyond the scope of this manual.

### 2.3.5.2 Operation M/C

Operation M/C is primarily a function of the E²Brain™ module driver software and the application. M/C signals are available, and, if implemented as part of the application, the operator as well as application software has access to these functions.

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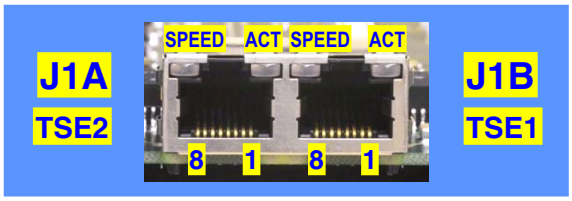
## 2.4 Board Interfaces

The following sections provide detailed information regarding the connector layout and pinout of the various board interfaces of the EBC2. The section ordering is by the connector designator.

### 2.4.1 J1 - Dual Giga Ethernet Connector

This connector provides interfacing for E²Brain™ modules which support the three speed Ethernet channels TSE1 and TSE2. This is a dual RJ45 connector with LEDs to indicate the status of the links.

**Figure 2-10: J1 - Dual Giga Ethernet Connector**




**LED OPERATION:**

| | | |
|---|---|---|
| ACT | OFF: | link not active |
| | GREEN: | link active |
| | GREEN BLINKING: | activity on link |
| SPEED | OFF: | 10 Mbps |
| | GREEN: | 100 Mbps |
| | YELLOW: | 1000 Mbps |

**Table 2-20: Pinouts of J1A and J1B Based on the Implementation**

| MDI / Standard Ethernet Cable | | | | | | PIN | MDIX / Crossed Ethernet Cable | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 10BASE-T | | 100BASE-TX | | 1000BASE-T | | | 10BASE-T | | 100BASE-TX | | 1000BASE-T | |
| I/O | SIGNAL | I/O | SIGNAL | I/O | SIGNAL | | I/O | SIGNAL | I/O | SIGNAL | I/O | SIGNAL |
| O | TX+ | O | TX+ | I/O | BI_DA+ | 1 | I | RX+ | I | RX+ | I/O | BI_DB+ |
| O | TX- | O | TX- | I/O | BI_DA- | 2 | I | RX- | I | RX- | I/O | BI_DB- |
| I | RX+ | I | RX+ | I/O | BI_DB+ | 3 | O | TX+ | O | TX+ | I/O | BI_DA+ |
| - | - | - | - | I/O | BI_DC+ | 4 | - | - | - | - | I/O | BI_DD+ |
| - | - | - | - | I/O | BI_DC- | 5 | - | - | - | - | I/O | BI_DD- |
| I | RX- | I | RX- | I/O | BI_DB- | 6 | O | TX- | O | TX- | I/O | BI_DA- |
| - | - | - | - | I/O | BI_DD+ | 7 | - | - | - | - | I/O | BI_DC+ |
| - | - | - | - | I/O | BI_DD- | 8 | - | - | - | - | I/O | BI_DC- |



***Note ...***

The Gigabit PHYs on the EBC2 support automatic MDI/MDIX crossover at all speeds of operation. Therefore both standard as well as crossed Ethernet cables can be used with these interfaces.


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### 2.4.2 J2 - 12V DC Power Input Connector

This connector is used for providing main input power to the EBC2 E²Brain™.

**Figure 2-11: J2 - 12V DC Power Input Connector**

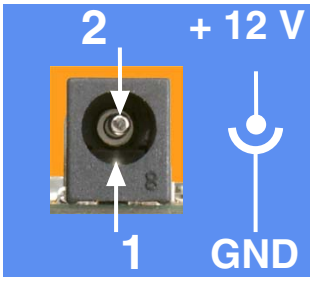



**Table 2-21: Pinout of J2**

| PIN | DESCRIPTION |
|---|---|
| 1 | GND |
| 2 | + 12 V DC |

### 2.4.3 J3 - TERM T/C Connector

This connector is used to provide serial terminal or console interfacing without hardware hand-shaking. This is a standard 9-pin, male, D-Sub connector.

**Figure 2-12: J3 - TERM T/C Connector**

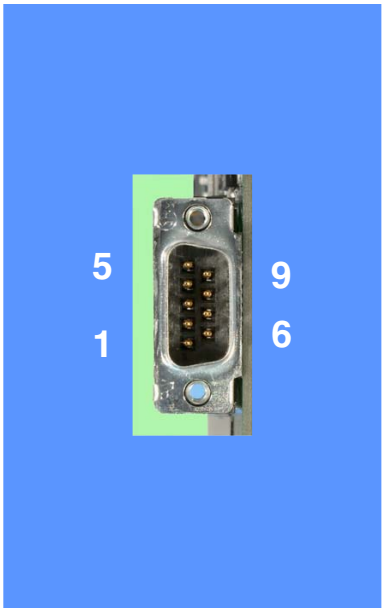



**Table 2-22: Pinout of J3**

| PIN | SIGNAL | DESCRIPTION |
|---|---|---|
| 1 | NC | Not connected |
| 2 | RXD | Receive data |
| 3 | TXD | Transmit data |
| 4 | RS232+ | RS232 positive voltage level |
| 5 | GND | Ground |
| 6 | NC | Not connected |
| 7 | RS232+ | RS232 positive voltage level |
| 8 | NC | Not connected |
| 9 | NC | Not connected |

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### 2.4.4 J4 - Monitor and Control Signal Connector

This connector is used for providing selected monitor and control signal interfacing. It is a 6-pin, male, dual pinrow, header connector.

**Figure 2-13: J4 - Monitor and Control Signal Connector**

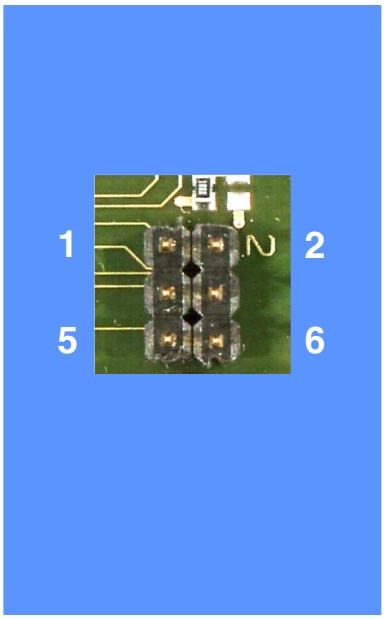



**Table 2-23: Pinout of J4**

| PIN | SIGNAL | DESCRIPTION |
|---|---|---|
| 1 | MC5 | Refer to the respective E²Brain™ module documentation for details |
| 2 | MC10 | Refer to the respective E²Brain™ module documentation for details |
| 3 | MC2 | Refer to the respective E²Brain™ module documentation for details |
| 4 | MC3 | Refer to the respective E²Brain™ module documentation for details |
| 5 | MC9 | Refer to the respective E²Brain™ module documentation for details |
| 6 | GND | Ground |

### 2.4.5 J5 - ATMEL Programming Connector

This connector is used for providing a programming interface for the ATMEL configuration EEPROM used with the E²Brain™ module FPGA logic controller. It is a 6-pin, male, dual pinrow, header connector.

**Figure 2-14: J5 - Logic Programming Connector**

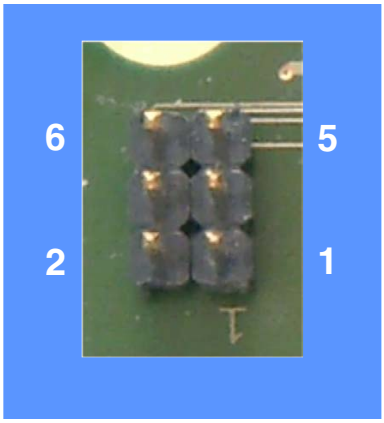



**Table 2-24: Pinout of J5**

| PIN | SIGNAL |
|---|---|
| 1 | DI |
| 2 | GND |
| 3 | AACK |
| 4 | DCLK |
| 5 | SER_EN |
| 6 | GND |


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### 2.4.6 J6 - DEBUG and Programming Connector

This connector is used for providing MPC8540 and PPC405EP debugging interfacing. It is a 16-pin, male, dual pinrow, header connector. When used with the EB405, it also can be used to programm the CPLD. Refer to the EB405 E²Brain™ module manual for the JTAG configuration requirements.

**Figure 2-15: J6 - Debug and Programming Connector**

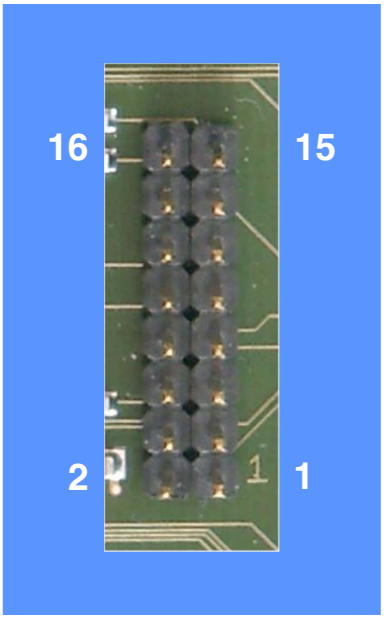



**Table 2-25: Pinout of J6**

| PIN | SIGNAL |
|---|---|
| 1 | TDO |
| 2 | NC |
| 3 | TDI |
| 4 | TRST |
| 5 | Pull up 10 kΩ to +3.3V |
| 6 | TARGET_VCC |
| 7 | TCK |
| 8 | CHKSTP_IN |
| 9 | TMS |
| 10 | NC |
| 11 | SRST / HALT |
| 12 | NC |
| 13 | HRST |
| 14 | KEY (NC) |
| 15 | CHKSTP_OUT |
| 16 | GND |

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### 2.4.7 J7 - IXP425 Debug Connector

This connector is used for providing IXP425 debugging interfacing. It is a 20-pin, male, dual pinrow, header connector.

**Figure 2-16: J7 - IXP425 Debug Connector**

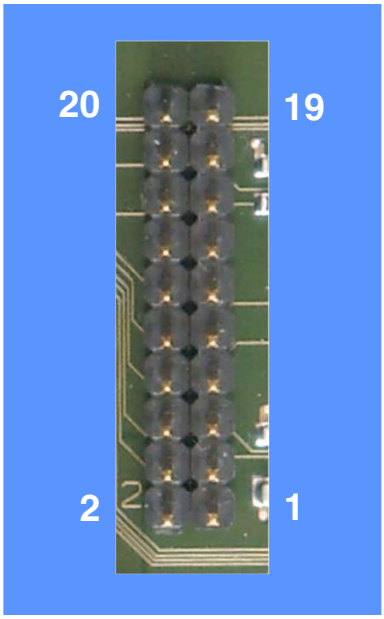



**Table 2-26: Pinout of J7**

| PIN | SIGNAL |
|---|---|
| 1 | TARGET_VCC |
| 2 | NC |
| 3 | TRST |
| 4 | NC |
| 5 | TDI |
| 6 | NC |
| 7 | TMS |
| 8 | GND |
| 9 | TCK |
| 10 | GND |
| 11 | NC |
| 12 | NC |
| 13 | TDO |
| 14 | NC |
| 15 | HRST |
| 16 | NC |
| 17 | NC |
| 18 | NC |
| 19 | NC |
| 20 | NC |

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### 2.4.8 J8 - CONS T/C Connector

This connector is used to provide serial terminal or console interfacing without hardware handshaking. This is a standard 9-pin, male, D-Sub connector.

**Figure 2-17: J8 - CONS T/C Connector**

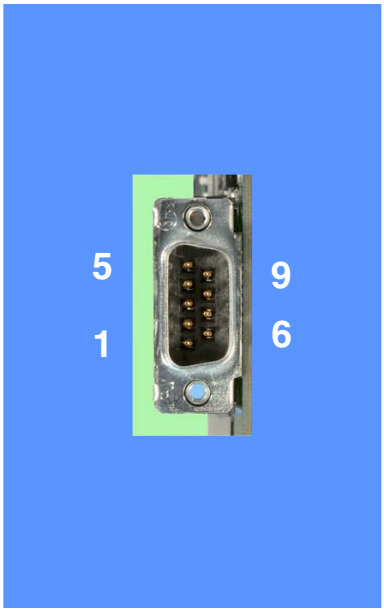



**Table 2-27: Pinout of J8**

| PIN | SIGNAL | DESCRIPTION |
|---|---|---|
| 1 | NC | Not connected |
| 2 | RXD | Receive data |
| 3 | TXD | Transmit data |
| 4 | RS232+ | RS232 positive voltage level |
| 5 | GND | Ground |
| 6 | NC | Not connected |
| 7 | RS232+ | RS232 positive voltage level |
| 8 | NC | Not connected |
| 9 | NC | Not connected |

### 2.4.9 J9 - INT2 T/P Interface

This jumper provides polarity control for SERIRQ testing. It is read in from and transferred inside the CPLD logic to the SERIRQ4 position of the SERIRQ signal. When set, the polarity is low, otherwise, it is high. This is a 2-pin, male, header connector.

### 2.4.10 J10 - INT1 T/P Interface

This jumper provides polarity control for SERIRQ testing. It is read in from and transferred inside the CPLD logic to the SERIRQ3 position of the SERIRQ signal. When set, the polarity is high, otherwise, it is low. This is a 2-pin, male, header connector.

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### 2.4.11 J11 - Logic Programming Connector

This connector is used for providing a programming interface for the EBC2 logic controller. It is a 10-pin, male, dual pinrow, header connector.

**Figure 2-18: J11 - Logic Programming Connector**

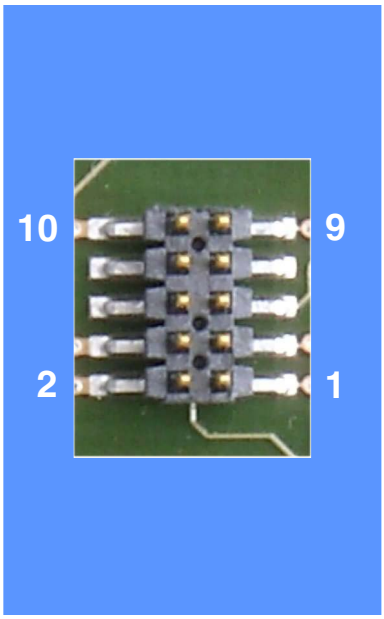



**Table 2-28: Pinout of J11**

| PIN | SIGNAL |
|---|---|
| 1 | LTCK |
| 2 | GND |
| 3 | LTDO |
| 4 | +3.3V |
| 5 | LTMS |
| 6 | NC |
| 7 | NC |
| 8 | NC |
| 9 | LTDI |
| 10 | GND |

### 2.4.12 J12 - F/LPCB Boot Select Interface

This jumper is used to select the source of the NetBootLoader boot software. When open, the source is the E²Brain™ module boot Flash. When set, the source is the EBC2 LPC Flash. This is a 2-pin, male, header connector.


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### 2.4.13 J13 - PCI Expansion Slot 2 Connector

This connector is used for providing interfacing for one standard PC PCI board. The factory setting for V(I/O) is +3.3 V. J13 is a standard 124-pin, 3.3V coded, PC PCI expansion slot connector. Only universally or +3.3V coded PCI cards may used with this connector.

**Figure 2-19: J13 - PCI Expansion Slot 2 Connector**

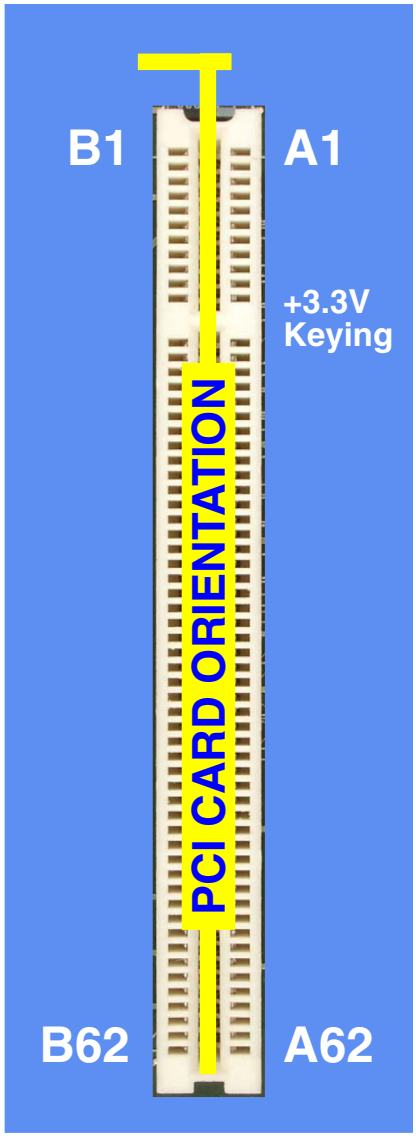



**Table 2-29: Pinout of J13**

| SIGNAL | PIN | PIN | SIGNAL | SIGNAL | PIN | PIN | SIGNAL |
|---|---|---|---|---|---|---|---|
| RES | A1 | B1 | NC | AD16 | A32 | B32 | AD17 |
| +12V | A2 | B2 | RES | +3.3V | A33 | B33 | C/BE2# |
| RES | A3 | B3 | GND | FRAME# | A34 | B34 | GND |
| RES | A4 | B4 | NC | GND | A35 | B35 | IRDY# |
| +5V | A5 | B5 | +5V | TRDY# | A36 | B36 | +3.3V |
| INTA# | A6 | B6 | +5V | GND | A37 | B37 | DEVSEL# |
| INTC# | A7 | B7 | INTB# | STOP# | A38 | B38 | GND |
| +5V | A8 | B8 | INTD# | +3.3V | A39 | B39 | LOCK# |
| NC | A9 | B9 | NC | NC | A40 | B40 | PERR# |
| V(I/O) | A10 | B10 | NC | NC | A41 | B41 | +3.3V |
| NC | A11 | B11 | NC | GND | A42 | B42 | SERR# |
| Key | A12 | B12 | Key | PAR | A43 | B43 | +3.3V |
| Key | A13 | B13 | Key | AD15 | A44 | B44 | C/BE1# |
| V_BAT | A14 | B14 | NC | +3.3V | A45 | B45 | AD14 |
| RST# | A15 | B15 | GND | AD13 | A46 | B46 | GND |
| V(I/O) | A16 | B16 | CLK | AD11 | A47 | B47 | AD12 |
| GNT# | A17 | B17 | GND | GND | A48 | B48 | AD10 |
| GND | A18 | B18 | REQ# | AD9 | A49 | B49 | GND |
| NC | A19 | B19 | V(I/O) | GND | A50 | B50 | GND |
| AD30 | A20 | B20 | AD31 | GND | A51 | B51 | GND |
| +3.3V | A21 | B21 | AD29 | C/BE0# | A52 | B52 | AD8 |
| AD28 | A22 | B22 | GND | +3.3V | A53 | B53 | AD7 |
| AD26 | A23 | B23 | AD27 | AD6 | A54 | B54 | +3.3V |
| GND | A24 | B24 | AD25 | AD4 | A55 | B55 | AD5 |
| AD24 | A25 | B25 | +3.3V | GND | A56 | B56 | AD3 |
| IDSEL | A26 | B26 | C/BE3# | AD2 | A57 | B57 | GND |
| +3.3V | A27 | B27 | AD23 | AD0 | A58 | B58 | AD1 |
| AD22 | A28 | B28 | GND | V(I/O) | A59 | B59 | V(I/O) |
| AD20 | A29 | B29 | AD21 | REQ64# | A60 | B60 | ACK64# |
| GND | A30 | B30 | AD19 | +5V | A61 | B61 | +5V |
| AD18 | A31 | B31 | +3.3V | +5V | A62 | B62 | +5V |


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### 2.4.14 J14 - PCI Expansion Slot 1 Connector

This connector is used for providing interfacing for one standard PC PCI board. The factory setting for V(I/O) is +3.3 V. J14 is a standard 124-pin, 3.3V coded, PC PCI expansion slot connector. Only universally or +3.3V coded PCI cards may used with this connector.

**Figure 2-20: J14 - PCI Expansion Slot 1 Connector**

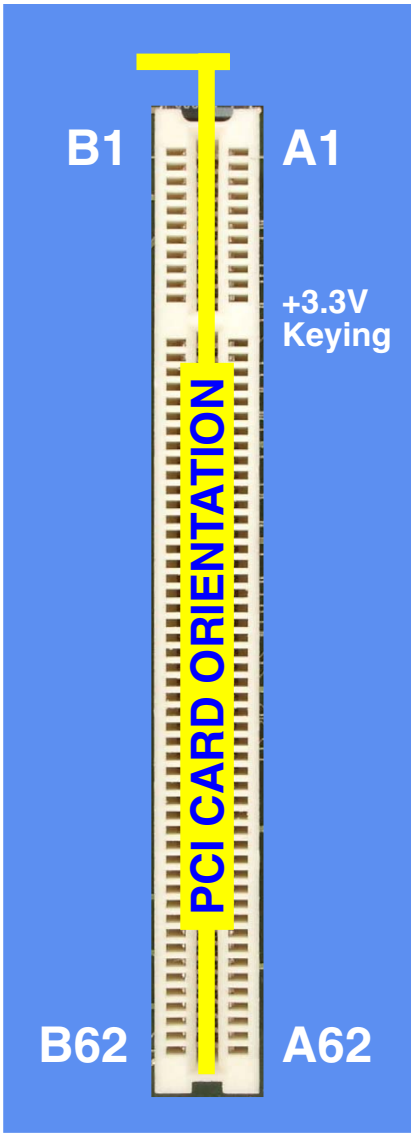



**Table 2-30: Pinout of J14**

| SIGNAL | PIN | PIN | SIGNAL | SIGNAL | PIN | PIN | SIGNAL |
|---|---|---|---|---|---|---|---|
| RES | A1 | B1 | NC | AD16 | A32 | B32 | AD17 |
| +12V | A2 | B2 | RES | +3.3V | A33 | B33 | C/BE2# |
| RES | A3 | B3 | GND | FRAME# | A34 | B34 | GND |
| RES | A4 | B4 | NC | GND | A35 | B35 | IRDY# |
| +5V | A5 | B5 | +5V | TRDY# | A36 | B36 | +3.3V |
| INTA# | A6 | B6 | +5V | GND | A37 | B37 | DEVSEL# |
| INTC# | A7 | B7 | INTB# | STOP# | A38 | B38 | GND |
| +5V | A8 | B8 | INTD# | +3.3V | A39 | B39 | LOCK# |
| NC | A9 | B9 | NC | NC | A40 | B40 | PERR# |
| V(I/O) | A10 | B10 | NC | NC | A41 | B41 | +3.3V |
| NC | A11 | B11 | NC | GND | A42 | B42 | SERR# |
| Key | A12 | B12 | Key | PAR | A43 | B43 | +3.3V |
| Key | A13 | B13 | Key | AD15 | A44 | B44 | C/BE1# |
| V_BAT | A14 | B14 | NC | +3.3V | A45 | B45 | AD14 |
| RST# | A15 | B15 | GND | AD13 | A46 | B46 | GND |
| V(I/O) | A16 | B16 | CLK | AD11 | A47 | B47 | AD12 |
| GNT# | A17 | B17 | GND | GND | A48 | B48 | AD10 |
| GND | A18 | B18 | REQ# | AD9 | A49 | B49 | GND |
| NC | A19 | B19 | V(I/O) | GND | A50 | B50 | GND |
| AD30 | A20 | B20 | AD31 | GND | A51 | B51 | GND |
| +3.3V | A21 | B21 | AD29 | C/BE0# | A52 | B52 | AD8 |
| AD28 | A22 | B22 | GND | +3.3V | A53 | B53 | AD7 |
| AD26 | A23 | B23 | AD27 | AD6 | A54 | B54 | +3.3V |
| GND | A24 | B24 | AD25 | AD4 | A55 | B55 | AD5 |
| AD24 | A25 | B25 | +3.3V | GND | A56 | B56 | AD3 |
| IDSEL | A26 | B26 | C/BE3# | AD2 | A57 | B57 | GND |
| +3.3V | A27 | B27 | AD23 | AD0 | A58 | B58 | AD1 |
| AD22 | A28 | B28 | GND | V(I/O) | A59 | B59 | V(I/O) |
| AD20 | A29 | B29 | AD21 | REQ64# | A60 | B60 | ACK64# |
| GND | A30 | B30 | AD19 | +5V | A61 | B61 | +5V |
| AD18 | A31 | B31 | +3.3V | +5V | A62 | B62 | +5V |

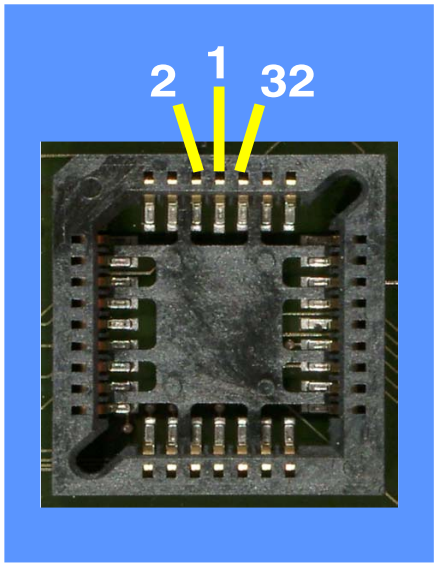
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### 2.4.15 J15 - LPC Flash Socket

This PLCC socket connector is used to provide interfacing for one standard PLCC 32-pin Flash device. The EBC2 provides the capability of either booting from the onboard E²Brain™ module Flash or from the EBC2 onboard LPC Flash. The setting of the jumper J12 controls the selection of the source for the boot software.

**Figure 2-21: J15 - LPC Flash Socket**





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### 2.4.16 J16 - CIE Extension Connector

This connector is used for providing interfacing for GPIO and X-Bus signals for the EB425 module. It is a 50-pin, male, dual pinrow, shrouded connector.

**Figure 2-22: J16 - CIE Extension Connector**

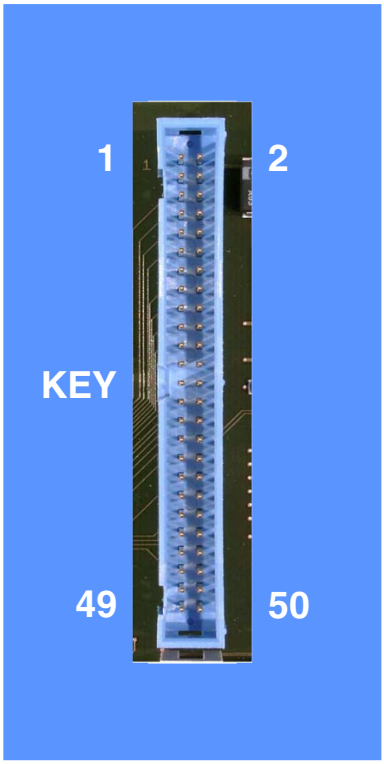



**Table 2-31: Pinout of J16**

| SIGNAL | PIN | PIN | SIGNAL |
|---|---|---|---|
| 3.3V | 1 | 2 | 3.3V |
| DIO0 | 3 | 4 | DIO1 |
| DIO2 | 5 | 6 | DIO3 |
| DIO4 | 7 | 8 | DIO5 |
| DIO6 | 9 | 10 | DIO7 |
| GND | 11 | 12 | GND |
| X_DATA7 | 13 | 14 | X_DATA6 |
| X_DATA5 | 15 | 16 | X_DATA4 |
| X_DATA3 | 17 | 18 | X_DATA2 |
| X_DATA1 | 19 | 20 | X_DATA0 |
| VCC | 21 | 22 | VCC |
| X_ADDR9 | 23 | 24 | X_ADDR8 |
| X_ADDR7 | 25 | 26 | X_ADDR6 |
| X_ADDR5 | 27 | 28 | X_ADDR4 |
| X_ADDR3 | 29 | 30 | X_ADDR2 |
| X_ADDR1 | 31 | 32 | X_ADDR0 |
| GND | 33 | 34 | GND |
| NC | 35 | 36 | NC |
| 3.3V | 37 | 38 | 3.3V |
| NC | 39 | 40 | NC |
| NC | 41 | 42 | NC |
| GND | 43 | 44 | GND |
| NC | 45 | 46 | NC |
| NC | 47 | 48 | 3.3V |
| VCC | 49 | 50 | NC |

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### 2.4.17 J17 - SIE Extension Connector

This connector is used for providing GPIO interface for the EB405 E²Brain™EBC2 module. It is a 8-pin, male, dual pinrow, header connector.

**Figure 2-23: J17 - SIE Extension Connector**

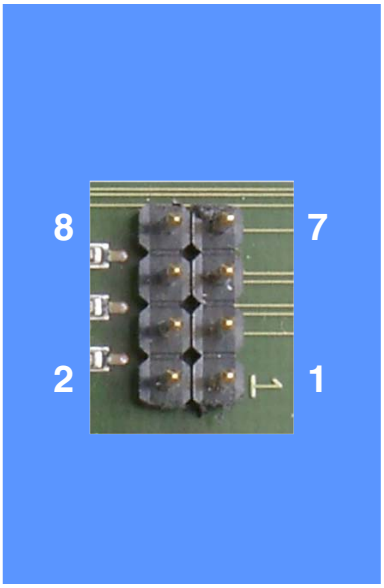



**Table 2-32: Pinout of J17**

| PIN | SIGNAL |
|---|---|
| 1 | 3.3V |
| 2 | GPIO15 |
| 3 | GPIO16 |
| 4 | GPIO14 |
| 5 | GPIO30 |
| 6 | GPIO31 |
| 7 | GPIO0 |
| 8 | GND |

### 2.4.18 J18 - SER1 HSS Connector

This connector is used to provide high speed RS232 full modem or RS422/RS485 serial interfacing. This is a standard 9-pin, male, D-Sub connector.

**Figure 2-24: J18 - SER1 HSS Connector**

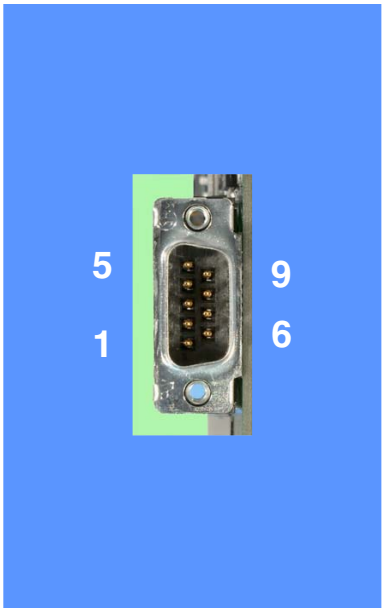



**Table 2-33: Pinout of J18**

| PIN | RS232 | RS422 | RS485 |
|---|---|---|---|
| 1 | DCD | RXD+ | NC |
| 2 | RXD | NC | NC |
| 3 | TXD | TXD+ | TRXD+ |
| 4 | DTR | NC | NC |
| 5 | GND | GND | GND |
| 6 | DSR/TCLK | RXD- | NC |
| 7 | RTS | NC | NC |
| 8 | CTS | TXD- | TRXD- |
| 9 | RI/RCLK | NC | NC |

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### 2.4.19 J21 - DIO Connector

This connector is used for providing four digital input and four digital output interfaces via the EBC2 logic controller. It is a 10-pin, male, dual pinrow, shrouded header connector.

Both the four inputs and the four outputs are defined as +3.3V TTL signalling GPIO, whereby the inputs accept 5V signal levels (up to a maximum of +5.5V DC). The digital outputs have a drive capacity of a maximum of 24mA, reduced to 12mA to guarantee the TTL output levels (0.4V Low and 2.4V High).

The digital general purpose I/O can be accessed via read/write cycles in the LPC IO-Space (offset address digital inputs: 0x00; offset address digital outputs: 0x01).

**Figure 2-25: J21 - DIO Connector**

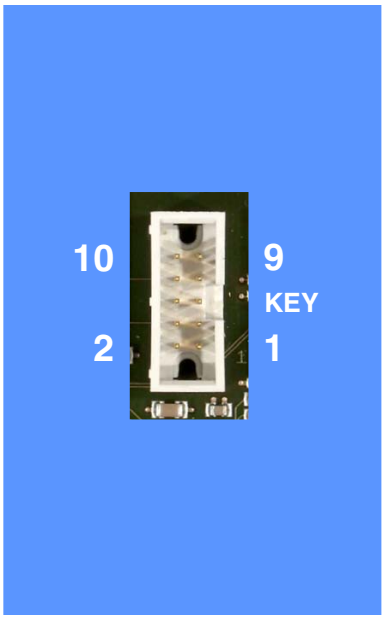



**Table 2-34: Pinout of J21**

| PIN | SIGNAL |
|---|---|
| 1 | DO0 |
| 2 | DI0 |
| 3 | DO1 |
| 4 | DI1 |
| 5 | DO2 |
| 6 | DI2 |
| 7 | DO3 |
| 8 | DI3 |
| 9 | +3.3V |
| 10 | GND |


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### 2.4.20 J22 - SER2 HSS Connector

This connector is used to provide high speed RS232 full modem or RS422/RS485 serial interfacing. This is a standard 9-pin, male, D-Sub connector.

**Figure 2-26: J22 - SER2 HSS Connector**

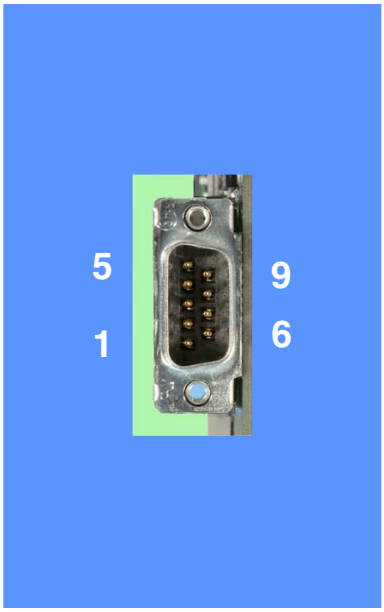



**Table 2-35: Pinout of J22**

| PIN | RS232 | RS422 | RS485 |
|---|---|---|---|
| 1 | DCD | RXD+ | NC |
| 2 | RXD | NC | NC |
| 3 | TXD | TXD+ | TRXD+ |
| 4 | DTR | NC | NC |
| 5 | GND | GND | GND |
| 6 | DSR/TCLK | RXD- | NC |
| 7 | RTS | NC | NC |
| 8 | CTS | TXD- | TRXD- |
| 9 | RI/RCLK | NC | NC |

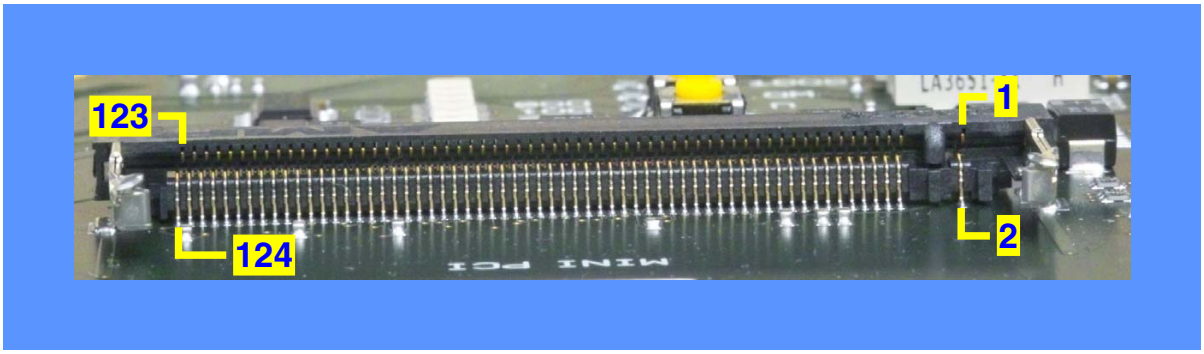
### 2.4.21 J25 - Mini PCI Connector

The EBC2 has one, 32-bit, 33 MHz, standard 124-pin Mini-PCI socket which accepts all type III Mini PCI boards. This interface supports a wide range of available Mini-PCI modules.

The Mini-PCI connector is a 124-pin card edge type connector that is similar to the SO-DIMM type. In the Mini-PCI specification this connecter is defined as “Type III”.

The maximum permitted height for the Mini PCI connector and the Mini PCI module is 8 mm.

**Figure 2-27: J25 - Mini PCI Connector**




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**Table 2-36: Pinout of J25**

| SIGNAL | PIN | PIN | SIGNAL |
|---|---|---|---|
| NC | 1 | 2 | NC |
| NC | 3 | 4 | NC |
| NC | 5 | 6 | NC |
| NC | 7 | 8 | NC |
| NC | 9 | 10 | NC |
| NC | 11 | 12 | NC |
| NC | 13 | 14 | NC |
| NC | 15 | 16 | RESERVED |
| INTB# | 17 | 18 | +5V |
| 3.3V | 19 | 20 | INTA# |
| RESERVED | 21 | 22 | RESERVED |
| GND | 23 | 24 | 3.3VAUX |
| CLK | 25 | 26 | RST# |
| GND | 27 | 28 | 3.3V |
| REQ# | 29 | 30 | GNT# |
| 3.3V | 31 | 32 | GND |
| AD[31] | 33 | 34 | NC |
| AD[29] | 35 | 36 | RESERVED |
| GND | 37 | 38 | AD[30] |
| AD[27] | 39 | 40 | 3.3V |
| AD[25] | 41 | 42 | AD[28] |
| NC | 43 | 44 | AD[26] |
| C/BE[3]# | 45 | 46 | AD[24] |
| AD[23] | 47 | 48 | IDSEL |
| GND | 49 | 50 | GND |
| AD[21] | 51 | 52 | AD[22] |
| AD[19] | 53 | 54 | AD[20] |
| GND | 55 | 56 | PAR |
| AD[17] | 57 | 58 | AD[18] |
| C/BE[2]# | 59 | 60 | AD[16] |
| IRDY# | 61 | 62 | GND |

| SIGNAL | PIN | PIN | SIGNAL |
|---|---|---|---|
| 3.3V | 63 | 64 | FRAME# |
| CLKRUN# | 65 | 66 | TRDY# |
| SERR# | 67 | 68 | STOP# |
| GND | 69 | 70 | 3.3V |
| PERR# | 71 | 72 | DEVSEL# |
| C/BE[1]# | 73 | 74 | GND |
| AD[14] | 75 | 76 | AD[15] |
| GND | 77 | 78 | AD[13] |
| AD[12] | 79 | 80 | AD[11] |
| AD[10] | 81 | 82 | GND |
| GND | 83 | 84 | AD[09] |
| AD[08] | 85 | 86 | C/BE[0]# |
| AD[07] | 87 | 88 | 3.3V |
| 3.3V | 89 | 90 | AD[06] |
| AD[05] | 91 | 92 | AD[04] |
| RESERVED | 93 | 94 | AD[02] |
| AD[03] | 95 | 96 | AD[00] |
| +5V | 97 | 98 | NC |
| AD[01] | 99 | 100 | NC |
| GND | 101 | 102 | GND |
| NC | 103 | 104 | GND |
| NC | 105 | 106 | NC |
| NC | 107 | 108 | NC |
| NC | 109 | 110 | NC |
| NC | 111 | 112 | RESERVED |
| GND | 113 | 114 | GND |
| NC | 115 | 116 | NC |
| GND | 117 | 118 | GND |
| GND | 119 | 120 | NC |
| NC | 121 | 122 | RESERVED |
| RESERVED | 123 | 124 | 3.3VAUX |


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### 2.4.22 J26 - SER3 HSS Connector

This connector is used to provide high speed RS232 full modem or RS422/RS485 serial interfacing. This is a standard 9-pin, male, D-Sub connector.

**Figure 2-28: J26 - SER3 HSS Connector**

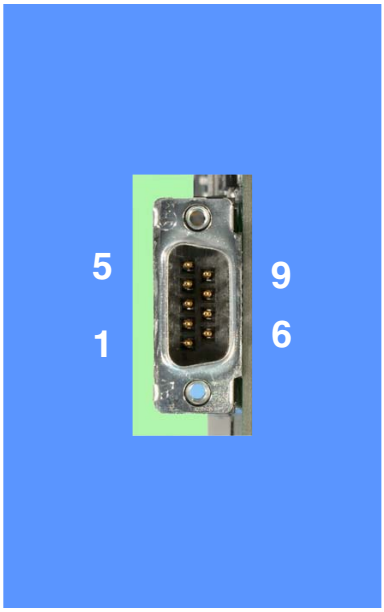



**Table 2-37: Pinout of J26**

| PIN | RS232 | RS422 | RS485 |
|---|---|---|---|
| 1 | DCD | RXD+ | NC |
| 2 | RXD | NC | NC |
| 3 | TXD | TXD+ | TRXD+ |
| 4 | DTR | NC | NC |
| 5 | GND | GND | GND |
| 6 | DSR/TCLK | RXD- | NC |
| 7 | RTS/TXFRAME | NC | NC |
| 8 | CTS/RXFRAME | TXD- | TRXD- |
| 9 | RI/RCLK | NC | NC |

### 2.4.23 J27 - SER4 HSS Connector

This connector is used to provide high speed RS232 full modem or RS422/RS485 serial interfacing. This is a standard 9-pin, male, D-Sub connector.

**Figure 2-29: J27 - SER4 HSS Connector**

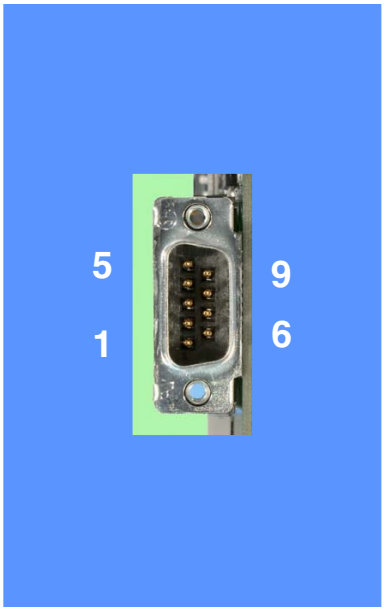



**Table 2-38: Pinout of J27**

| PIN | RS232 | RS422 | RS485 |
|---|---|---|---|
| 1 | DCD | RXD+ | NC |
| 2 | RXD | NC | NC |
| 3 | TXD | TXD+ | TRXD+ |
| 4 | DTR | NC | NC |
| 5 | GND | GND | GND |
| 6 | DSR/TCLK | RXD- | NC |
| 7 | RTS/TXFRAME | NC | NC |
| 8 | CTS/RXFRAME | TXD- | TRXD- |
| 9 | RI/RCLK | NC | NC |

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### 2.4.24 J28 - CompactFLASH Type II Connector

This connector is used for providing interfacing for CompactFLASH Type II devices. The E²Brain™ modules that are supported by the EBC2 all provide a direct CF interface without a bridging device. It is a standard Type II CompactFLASH connector assembly with a 50-pin, male, dual pinrow connector.

**Figure 2-30: J28 - CompactFlash Connector**

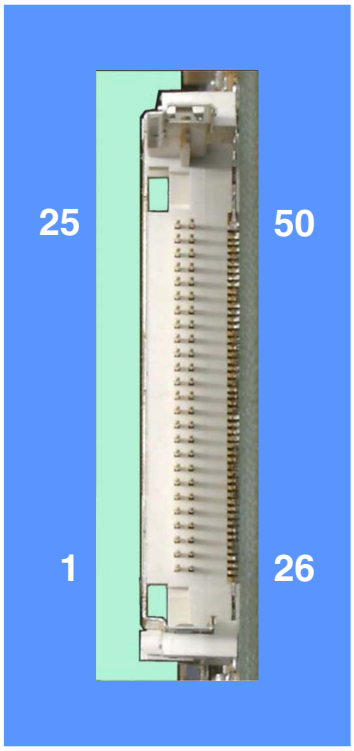



**Table 2-39: Pinout of J28**

| SIGNAL | PIN | PIN | SIGNAL |
|---|---|---|---|
| GND | 1 | 26 | CF_CD1 |
| CF_D3 | 2 | 27 | CF_D11 |
| CF_D4 | 3 | 28 | CF_D12 |
| CF_D5 | 4 | 29 | CF_D13 |
| CF_D6 | 5 | 30 | CF_D14 |
| CF_D7 | 6 | 31 | CF_D15 |
| CF_CS0 | 7 | 32 | CF_CS1 |
| GND | 8 | 33 | GND |
| GND | 9 | 34 | CF_RD |
| GND | 10 | 35 | CF_WR |
| GND | 11 | 36 | +3.3V |
| GND | 12 | 37 | CF_IRQ |
| +3.3V | 13 | 38 | +3.3V |
| GND | 14 | 39 | GND |
| GND | 15 | 40 | NC |
| GND | 16 | 41 | CF_RST |
| GND | 17 | 42 | CF_IORDY |
| CF_A2 | 18 | 43 | CF_DMAREQ |
| CF_A1 | 19 | 44 | CF_DMAACK |
| CF_A0 | 20 | 45 | CF_DASP |
| CF_D0 | 21 | 46 | CF_PDIAG |
| CF_D1 | 22 | 47 | CF_D8 |
| CF_D2 | 23 | 48 | CF_D9 |
| CF_CS16 | 24 | 49 | CF_D10 |
| CF_CD2 | 25 | 50 | GND |


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### 2.4.25 J29 - USB2 Connector

This connector is used for providing a host USB 2.0 interface for E²Brain™ modules. It is a standard USB type A receptacle connector.

**Figure 2-31: J29 - USB2 Connector**

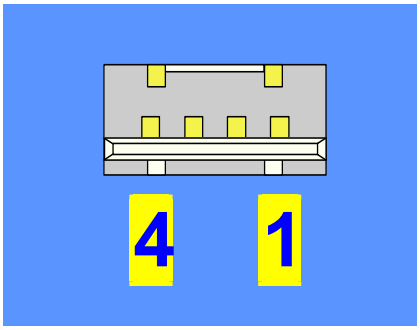


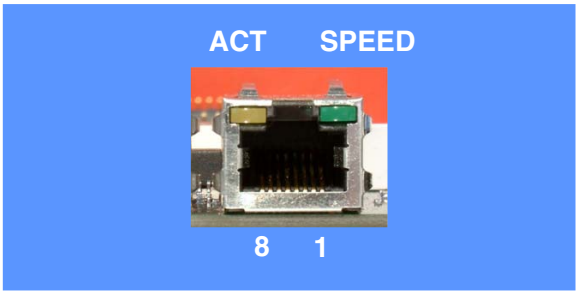

**Table 2-40: Pinout of J29**

| PIN | SIGNAL |
|---|---|
| 1 | VCC |
| 2 | DATA- |
| 3 | DATA+ |
| 4 | GND |

### 2.4.26 J30 - FE2 Fast Ethernet Connector

This connector is used to provide Fast Ethernet interfacing. This is an 8-pin, RJ45 type connector which has link status LEDs integrated in the connector housing.

**Figure 2-32: J30 - FE2 Fast Ethernet Connector**




**LED OPERATION:**

| | | |
|---|---|---|
| ACT | OFF: | link not active |
| | YELLOW: | link active |
| | YELLOW BLINKING: | activity on link |
| SPEED | OFF: | 10 Mbps |
| | GREEN: | 100 Mbps |

**Table 2-41: Pinout of J30**

| PIN | SIGNAL | DESCRIPTION |
|---|---|---|
| 1 | TDP2 | Transmit data + |
| 2 | TDN2 | Transmit data - |
| 3 | RDP2 | Receive data + |
| 4 | NC | |
| 5 | NC | |
| 6 | RDN2 | Receive data - |
| 7 | NC | |
| 9 | NC | |

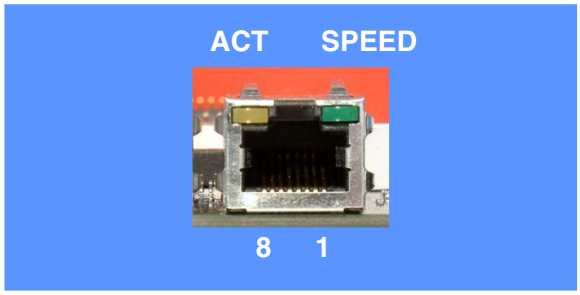
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### 2.4.27 J31 - FE1 Fast Ethernet Connector

This connector is used to provide Fast Ethernet interfacing. This is an 8-pin, RJ45 type connector which has link status LEDs integrated in the connector housing.

**Figure 2-33: J31 - FE1 Fast Ethernet Connector**




**LED OPERATION:**

| | | |
|---|---|---|
| ACT | OFF: | link not active |
| | YELLOW: | link active |
| | YELLOW BLINKING: | activity on link |
| SPEED | OFF: | 10 Mbps |
| | GREEN: | 100 Mbps |

**Table 2-42: Pinout of J31**

| PIN | SIGNAL | DESCRIPTION |
|---|---|---|
| 1 | TDP2 | Transmit data + |
| 2 | TDN2 | Transmit data - |
| 3 | RDP2 | Receive data + |
| 4 | NC | |
| 5 | NC | |
| 6 | RDN2 | Receive data - |
| 7 | NC | |
| 9 | NC | |

### 2.4.28 J32 - USB1 Connector

This connector is used for providing a host, device, or OTG USB 2.0 interface for E²Brain™ modules. It is a standard USB type mini AB receptacle connector.

**Figure 2-34: J32 - USB1 Connector**

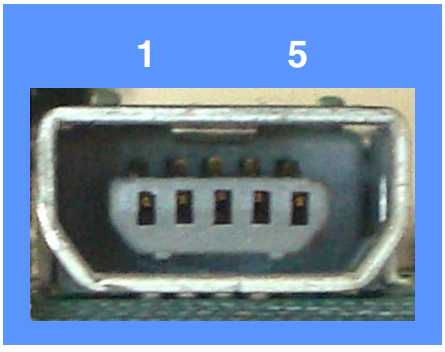



**Table 2-43: Pinout of J32**

| PIN | SIGNAL |
|---|---|
| 1 | VCC |
| 2 | DATA- |
| 3 | DATA+ |
| 4 | ID |
| 5 | GND |


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### 2.4.29 J33 - CAN2 Connector

This connector is used to provide Controller Area Network (CAN) interfacing. The default configuration for this interface is with opto-isolation. If non-opto-isolation is required, it must be specified when ordering. This is a standard 9-pin, male, D-Sub connector.

**Figure 2-35: J33 - CAN2 Connector**

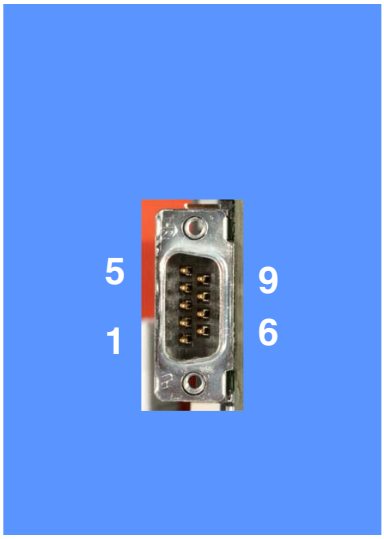



**Table 2-44: Pinout of J33**

| PIN | SIGNAL | DESCRIPTION |
|---|---|---|
| 1 | NC | |
| 2 | CAN2_L | CAN low |
| 3 | GND | Ground (isolated) |
| 4 | NC | |
| 5 | NC | |
| 6 | GND | Ground (isolated) |
| 7 | CAN2_H | CAN high |
| 8 | NC | |
| 9 | VCC | +5V isolated (max. 90 mA) |

### 2.4.30 J34 - CAN1 Connector

This connector is used to provide Controller Area Network (CAN) interfacing. The default configuration for this interface is with opto-isolation. If non-opto-isolation is required, it must be specified when ordering. This is a standard 9-pin, male, D-Sub connector.

**Figure 2-36: J34 - CAN1 Connector**

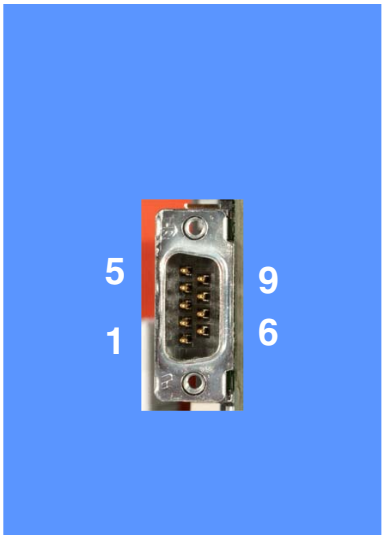



**Table 2-45: Pinout of J34**

| PIN | SIGNAL | DESCRIPTION |
|---|---|---|
| 1 | NC | |
| 2 | CAN1_L | CAN low |
| 3 | GND | Ground (isolated) |
| 4 | NC | |
| 5 | NC | |
| 6 | GND | Ground (isolated) |
| 7 | CAN1_H | CAN high |
| 8 | NC | |
| 9 | VCC | +5V isolated (max. 90 mA) |

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## 2.5 Monitor and Control Interfaces

The following sections provide detailed information regarding the monitor and control functions available on the EBC2.

### 2.5.1 Operational Status Indicators - LEDs

There are 16 operational status indicators available on the EBC2 for monitoring of the board operation. In addition to these indicators, each of the Ethernet connectors has two LEDs which provide link status information which has been described along with the connectors.The following table provides an overview of these indicators.

**Table 2-46: EBC2 Operational Status Indicators (LEDs)**

| DES. | NAME | COLOR | DESCRIPTION |
|---|---|---|---|
| D2 | 12V | GREEN | When on is general indication that +12V supply is functioning |
| D4 | 5V | GREEN | When on is general indication that +5V supply is functioning |
| D5 | 3.3V | GREEN | When on is general indication that +3.3V supply is functioning |
| D9 | DIN0 | GREEN | Indicates DIN(0) signal is asserted |
| D10 | DIN1 | GREEN | Indicates DIN(1) signal is asserted |
| D11 | DIN2 | GREEN | Indicates DIN(2) signal is asserted |
| D12 | DIN3 | GREEN | Indicates DIN(3) signal is asserted |
| D13 | DOUT3 | YELLOW | Indicates DOUT(3) signal is asserted |
| D14 | DOUT2 | YELLOW | Indicates DOUT(2) signal is asserted |
| D15 | DOUT1 | YELLOW | Indicates DOUT(1) signal is asserted |
| D16 | DOUT0 | YELLOW | Indicates DOUT(0) signal is asserted |
| D17 | GPIO | RED | General purpose indicator |
| D18 | WDOG | YELLOW | Used to indicate the status of the E²Brain™ module watchdog<br>Is a function of the application. If not used, remains off. |
| D19 | BOOT | GREEN | General purpose indicator<br>Used by bootloader to indicate boot status. After bootup is completed, is available for application use.<br>At start of bootup, is flashing to indicate that bootup may be interrupted by pressing SW1. Refer to the corresponding E²Brain™ product documentation for further information. |
| D20 | 7SHN | RED | Seven segment LED, most significant nibble<br>General purpose indicator for POST codes and application |
| D21 | 7SLN | RED | Seven segment LED, least significant nibble<br>General purpose indicator for POST codes and application |


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### 2.5.2 Operator Switches - SW1, SW2, SW3

There are three operator switches available on the EBC2 for interaction with the system. SW2 can be used to invoke a system reset, and SW1 can be used to invoke a system abort. SW1 is used during the boot operation to cause the E²Brain™ module to abort the boot operation and allow command line inputs to the bootloader. Refer to the E²Brain™ module manual for further information.

SW3 is an eight pole DIP switch which is used to select the operational mode of each of the HSS serial interfaces: SER[1:4]. The following table provides information for configuring these switches.

**Table 2-47: HSS Serial Mode Configuration**

| | SER1 | | SER2 | | SER3 | | SER4 | |
|---|---|---|---|---|---|---|---|---|
| | DIP Switch Pole | | DIP Switch Pole | | DIP Switch Pole | | DIP Switch Pole | |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
| RS232 (default) | Off | Off | Off | Off | Off | Off | Off | Off |
| RS422 (4wire) | Off | On | Off | On | Off | On | Off | On |
| RS485 (2wire) with Local Echo | On | Off | On | Off | On | Off | On | Off |
| RS485 (2wire) without Local Echo | On | On | On | On | On | On | On | On |

### 2.5.3 M / C Signals

In addition to the above mentioned interfaces, there are monitor and control signals available for application development and usage. Refer to sections 2.3.1.3, 2.4.4, and the E²Brain™ module product documentation for further information.

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Chapter 3

# Installation

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# 3. Installation

The EBC2 has been designed for easy installation. However, the following standard precautions, installation procedures, and general information must be observed to ensure proper installation and to preclude damage to the board or injury to personnel.

## 3.1 Hardware Installation

The product described in this manual is designed for use only with E²Brain™ modules that comply with Kontron's E²Brain™specification. For installation of E²Brain™ modules refer to the applicable E²Brain™ module documentation.

### 3.1.1 Safety Requirements

The following electrical hazard precautions must be observed.



***Caution, Electric Shock Hazard!***

Ensure that the system main power is removed prior to installing or removing this board. Ensure that there are no other external voltages or signals being applied to this board or other boards within the system. Failure to comply with the above could endanger your life or health and may cause damage to this board or other system components including process-side signal conditioning equipment.



***ESD Equipment!***

This Kontron board contains electrostatic sensitive devices. Please observe the following precautions to avoid damage to your board:

Discharge your clothing before touching the assembly. Tools must be discharged before use.

Do not touch any on board components, connector pins, or board conductive circuits.

If working at an anti-static workbench with professional discharging equipment, ensure compliance with its usage when handling this product.

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### 3.1.2 Installation Procedures

To install the EBC2 proceed as follows:

1. Ensure that the safety requirements indicated in chapter 3.1.1 are observed.



***Warning!***

Failure to comply with the instruction below may cause damage to the board or result in improper system operation. Please refer to chapter 4 for configuration information.

2. Ensure that the board is properly configured for operation before installing.



***Note...***

Care must be taken when applying the procedures below to ensure that when the board is assembled along with the other application system components that it is not damaged through contact with the other components of the system.

3. Ensure that the associated E²Brain™ module is properly installed on the EBC2.



***Warning!***

The EBC2 is designed for use only with E²Brain™ modules that comply with Kontron's E²Brain™ specification. Use of any other type of E²Brain™ module with the EBC2 will result in improper operation and possibly cause damage to the E²Brain™ module as well as the EBC2.

4. Assemble the EBC2 within the application system as required. See appropriate system documentation for assembly procedures.

### 3.1.3 Removal Procedures

To remove the EBC2 proceed as follows:

1. Ensure that the safety requirements indicated in chapter 3.1.1 are observed.



***Warning!***

Care must be taken when applying the procedures below to ensure that when the board is removed it is not damaged through contact with other components in the system.

2. Disassemble the EBC2 within the application sub-system as required. See appropriate system documentation for disassembly procedures.

3. Dispose of the EBC2 as required observing applicable environmental regulations governing the handling and disposition of this type of product.

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Chapter 4

# Configuration

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# 4. Configuration

The following sections provide system integrators with detailed information for configuring the EBC2 module for operation

## 4.1 Jumper Settings

Prior to installation of the EBC2 board there are jumpers which must be configured appropriately to ensure proper operation of the board. Please refer to Figure 1-4 in section 1 for the location of the jumpers on the board.

### 4.1.1 Overview

The following table provides an overview of the EBC2 jumpers including a short description of the default settings.

**Table 4-1: EBC2 Jumper Settings Overview**

| JUMPER | FUNCTION | DEFAULT SETTING | SETTING DESCRIPTION |
|---|---|---|---|
| J12 | Select boot software source | open | Boot from E²Brain™ module Flash |
| JP1 | PHY1 low power mode select | open | PHY1 normal operation |
| JP2 | PHY2 low power mode select | open | PHY2 normal operation |
| JP3 | RS422/485 Line Termination | open | SER1 transmit differential pair termination (120 ohm) |
| JP4 | RS422/485 Line Termination | open | SER1 receive differential pair termination (120 ohm) |
| JP5 | RS422/485 Line Termination | open | SER2 transmit differential pair termination (120 ohm) |
| JP6 | RS422/485 Line Termination | open | SER2 receive differential pair termination (120 ohm) |
| JP7 | RS422/485 Line Termination | open | SER3 transmit differential pair termination (120 ohm) |
| JP8 | RS422/485 Line Termination | open | SER3 receive differential pair termination (120 ohm) |
| JP9 | RS422/485 Line Termination | open | SER4 transmit differential pair termination (120 ohm) |
| JP10 | RS422/485 Line Termination | open | SER4 receive differential pair termination (120 ohm) |
| JP11/14/15 | CAN2 Power Options | set | +5V isolated power supply |
| JP12/17/18 | CAN1 Power Options | set | +5V isolated power supply |
| JP13 | CAN2 Termination | open | CAN2 transmission lines not terminated with 120 ohm termination resistor |
| JP16 | CAN1 Termination | open | CAN1 transmission lines not terminated with 120 ohm termination resistor |

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### 4.1.2 Jumper Locations

The following figures illustrate the location of the various jumpers on the EBC2.

**Figure 4-1: J12 Jumper**

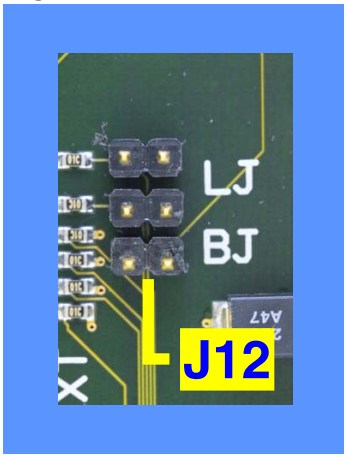



**Figure 4-2: JP1 and JP2 Jumpers**

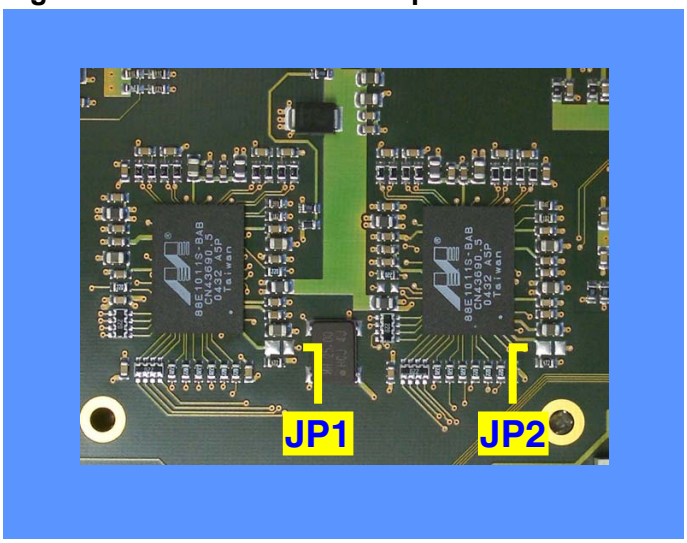
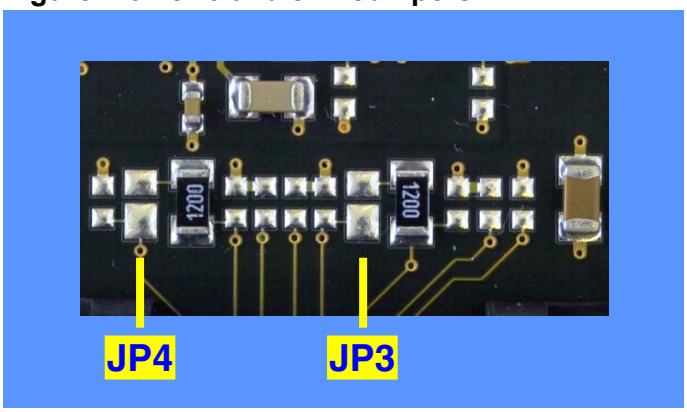



**Figure 4-3: JP3 and JP4 Jumpers**




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Figure 4-4: JP5 and JP6 Jumpers

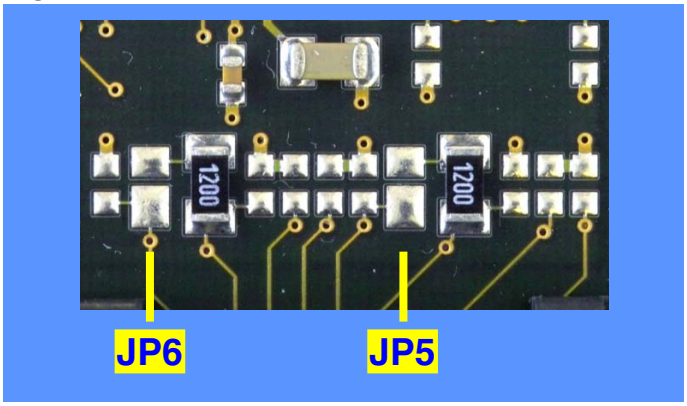



Figure 4-5: JP7 and JP8 Jumpers

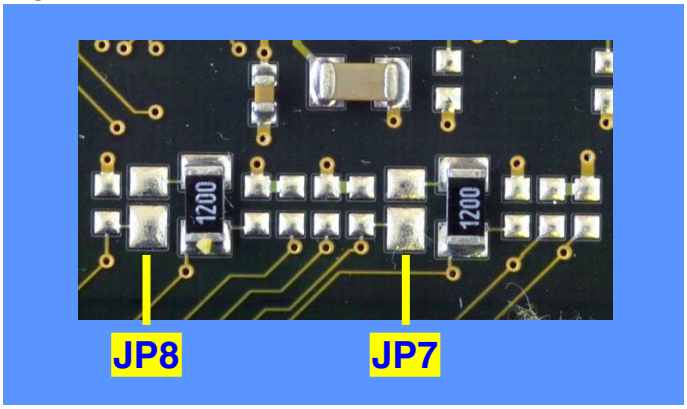
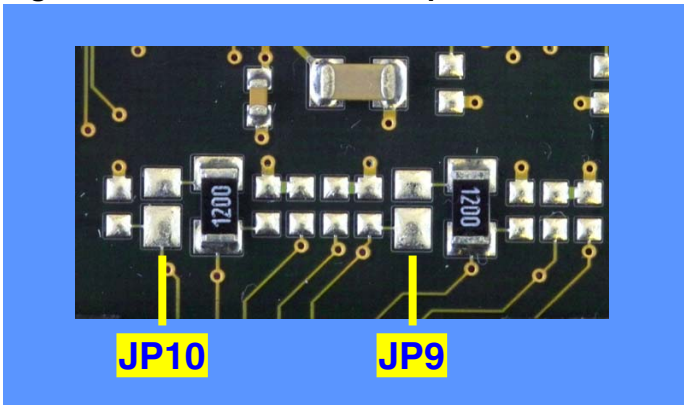



Figure 4-6: JP9 and JP10 Jumpers





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Figure 4-7: JP11, JP13, JP14 and JP15 Jumpers

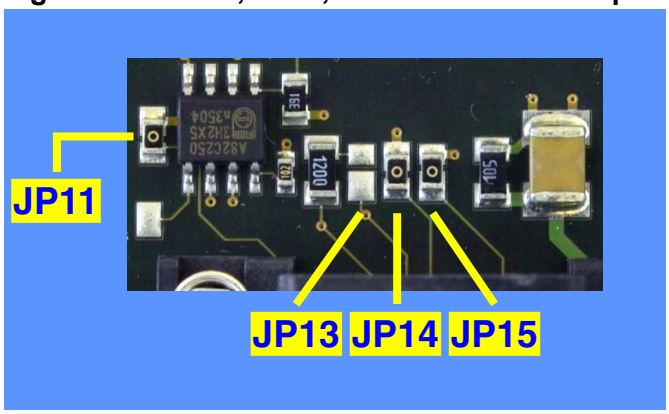
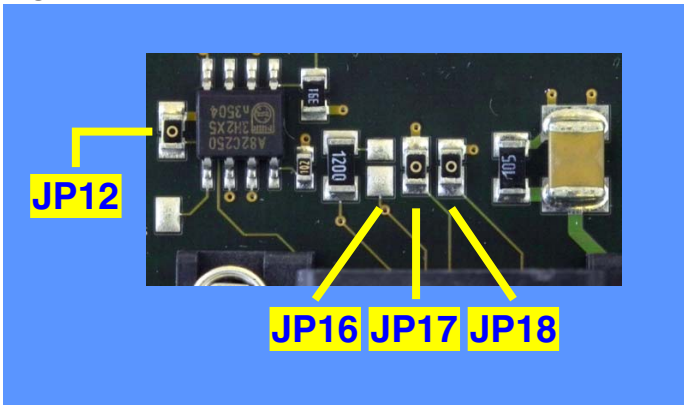



Figure 4-8: JP12, JP16, JP17 and JP18 Jumpers




## 4.2 V(I/O) Configuration

The EBC2 is configured for +3.3V V(I/O) operation and cannot be configured for +5V. Only universally coded or +3.3V coded PCI cards may be used with this board. The PCI connectors J13 and J14 are +3.3V key coded. Refer to sections 2.4.13 and 2.4.14 for orientation information for PCI expansion boards.

## 4.3 LPC Address Mapping

The following table indicates the LPC address mapping for access to the digital input, digital output, and POST code data.

Table 4-2: LPC Address Mapping

| REGISTER | LPC I/O ADDRESS OFFSET |
|---|---|
| DIN_DATA | 0x0000 0000 |
| DOUT_DATA | 0x0000 0001 |
| POST_CODE_DATA | 0x0000 0080 |

The address map describes the offset location for the LPC I/O area. The LPC I/O address itself is a function of the corresponding E²Brain™ module.

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## 4.4 PCI Bus IDSEL Mapping and IRQ Routing

The IRQ´s of the different PCI devices on the EBC2 must be distributed to the four PCI interrupts (INTA#, INTB#, INTC#, INTD#) of the E²Brain™ module. In the same manner, different PCI ADxx lines from the E²Brain™ module must be connected to the IDSEL input of the PCI devices on the EBC2.

The following table provides the realized routing on the EBC2 with the corresponding PCI device.

**Table 4-3: IDSEL Mapping and IRQ Routing**

| EBC2 PCI DEVICE | EBC2 IDSEL ← ADXX E²Brain™ MODULE | PCI INTERRUPT E²Brain™ MODULE |
|---|---|---|
| PCI connector slot 1, J14 | AD28 | |
| INTA# | | INTA# |
| INTB# | | INTB# |
| INTC# | | INTC# |
| INTD# | | INTD# |
| PCI connector slot 2, J13 | AD27 | |
| INTA# | | INTD# |
| INTB# | | INTA# |
| INTC# | | INTB# |
| INTD# | | INTC# |
| Mini PCI slot, J25 | AD26 | |
| INTA# | | INTC# |
| INTB# | | INTD# |

For further information concerning this subject, please contact Kontron Modular Computers.


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## 4.5 EBC2 Register Description

The following sections provide register descriptions for the:

- Digital Input Data Register
- Digital Output Data Register
- POST Code Data Register

### 4.5.1 Digital Input Data Register

The digital input data register indicates the status of the respective input signals.

Address Offset: 0x0000 0000
Format: Byte
Access: Read
Value after reset: 0x00 (if inputs are left open)

Digital input channels 0 to 3 are active, channels 4 to 7 are not used.

**Table 4-4: Digital Input Data Register**

| REGISTER NAME | | Digital Input Data Register | | | | | | ACCESS | |
|---|---|---|---|---|---|---|---|---|---|
| ADDRESS | | 0x0000 0000 (offset) | | | | | | R | |
| BIT POSITION | | MSB 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 LSB |
| CONTENT | | DIN_ DATA_7 | DIN_ DATA_6 | DIN_ DATA_5 | DIN_ DATA_4 | DIN_ DATA_3 | DIN_ DATA_2 | DIN_ DATA_1 | DIN_ DATA_0 |
| DEFAULT | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | DIN_ DATA_0 | 0 | Input signal is low or open | | | | | | |
| | | 1 | Input signal is high | | | | | | |
| 1 | DIN_ DATA_1 | 0 | Input signal is low or open | | | | | | |
| | | 1 | Input signal is high | | | | | | |
| 2 | DIN_ DATA_2 | 0 | Input signal is low or open | | | | | | |
| | | 1 | Input signal is high | | | | | | |
| 3 | DIN_ DATA_3 | 0 | Input signal is low or open | | | | | | |
| | | 1 | Input signal is high | | | | | | |
| 4 | DIN_ DATA_4 | 0 | Channel not used | | | | | | |
| | | 1 | | | | | | | |
| 5 | DIN_ DATA_5 | 0 | Channel not used | | | | | | |
| | | 1 | | | | | | | |
| 6 | DIN_ DATA_6 | 0 | Channel not used | | | | | | |
| | | 1 | | | | | | | |
| 7 | DIN_ DATA_7 | 0 | Channel not used | | | | | | |
| | | 1 | | | | | | | |


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### 4.5.2 Digital Output Data Register

The digital output data register controls the digital output port or indicates the status of the respective output signals in the case of a read access.

Address Offset: 0x0000 0001
Format: Byte
Access: Read and write
Value after reset: 0x00

The bits 0 to 3 set the outputs according to the programmed value and reflect the status of the respective digital output channel in the case of a read access. The bits 4 to 7 are reserved.

**Table 4-5: Digital Output Data Register**

| REGISTER NAME | | Digital Output Data Register | | | | | | ACCESS | |
|---|---|---|---|---|---|---|---|---|---|
| ADDRESS | | 0x0000 0001 (offset) | | | | | | R | W |
| BIT POSITION | | MSB 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 LSB |
| CONTENT | | DOUT_ DATA_7 | DOUT_ DATA_6 | DOUT_ DATA_5 | DOUT_ DATA_4 | DOUT_ DATA_3 | DOUT_ DATA_2 | DOUT_ DATA_1 | DOUT_ DATA_0 |
| DEFAULT | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | DOUT_ DATA_0 | 0 | TTL signal level 0 | | | | | | |
| | | 1 | TTL signal level 1 | | | | | | |
| 1 | DOUT_ DATA_1 | 0 | TTL signal level 0 | | | | | | |
| | | 1 | TTL signal level 1 | | | | | | |
| 2 | DOUT_ DATA_2 | 0 | TTL signal level 0 | | | | | | |
| | | 1 | TTL signal level 1 | | | | | | |
| 3 | DOUT_ DATA_3 | 0 | TTL signal level 0 | | | | | | |
| | | 1 | TTL signal level 1 | | | | | | |
| 4 | DOUT_ DATA_4 | 0 | Channel not used | | | | | | |
| | | 1 | | | | | | | |
| 5 | DOUT_ DATA_5 | 0 | Channel not used | | | | | | |
| | | 1 | | | | | | | |
| 6 | DOUT_ DATA_6 | 0 | Channel not used | | | | | | |
| | | 1 | | | | | | | |
| 7 | DOUT_ DATA_7 | 0 | Channel not used | | | | | | |
| | | 1 | | | | | | | |

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### 4.5.3 POST Code Data Register

The POST code data register is used to control the seven segment LED displays and to indicate the status of the respective display in the case of a read access.

Address Offset: 0x0000 0080
Format: Byte
Access: Read and write
Value after reset: 0x5F (indicates that the boot process has been completed)

LED D20 indicates the value of the higher nibble of the register, whereas, LED D21 indicates the value of the lower nibble of the register.

**Table 4-6: POST Code Data Register**

| REGISTER NAME | | POST Code Data Register | | | | | | ACCESS | |
|---|---|---|---|---|---|---|---|---|---|
| ADDRESS | | 0x0000 0080 (offset) | | | | | | R | W |
| BIT POSITION | | MSB 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 LSB |
| CONTENT | | POST_ CODE_ DATA_7 | POST_ CODE_ DATA_6 | POST_ CODE_ DATA_5 | POST_ CODE_ DATA_4 | POST_ CODE_ DATA_3 | POST_ CODE_ DATA_2 | POST_ CODE_ DATA_1 | POST_ CODE_ DATA_0 |
| DEFAULT | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | POST_ CODE_ DATA_0 | 0 | Register lower nibble: display indicates in hexadecimal value:<br>**BITS 3 2 1 0** **HEX** **DISPLAY: D21**<br>0 0 0 0 0x0 0<br>•<br>•<br>•<br>1 1 1 1 0xF F | | | | | | |
| | | 1 | | | | | | | |
| 1 | POST_ CODE_ DATA_1 | 0 | | | | | | | |
| | | 1 | | | | | | | |
| 2 | POST_ CODE_ DATA_2 | 0 | | | | | | | |
| | | 1 | | | | | | | |
| 3 | POST_ CODE_ DATA_3 | 0 | | | | | | | |
| | | 1 | | | | | | | |
| 4 | POST_ CODE_ DATA_4 | 0 | Register higher nibble: display indicates in hexadecimal value:<br>**BITS 7 6 5 4** **HEX** **DISPLAY: D20**<br>0 0 0 0 0x0 0<br>•<br>•<br>•<br>1 1 1 1 0xF F | | | | | | |
| | | 1 | | | | | | | |
| 5 | POST_ CODE_ DATA_5 | 0 | | | | | | | |
| | | 1 | | | | | | | |
| 6 | POST_ CODE_ DATA_6 | 0 | | | | | | | |
| | | 1 | | | | | | | |
| 7 | POST_ CODE_ DATA_7 | 0 | | | | | | | |
| | | 1 | | | | | | | |

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