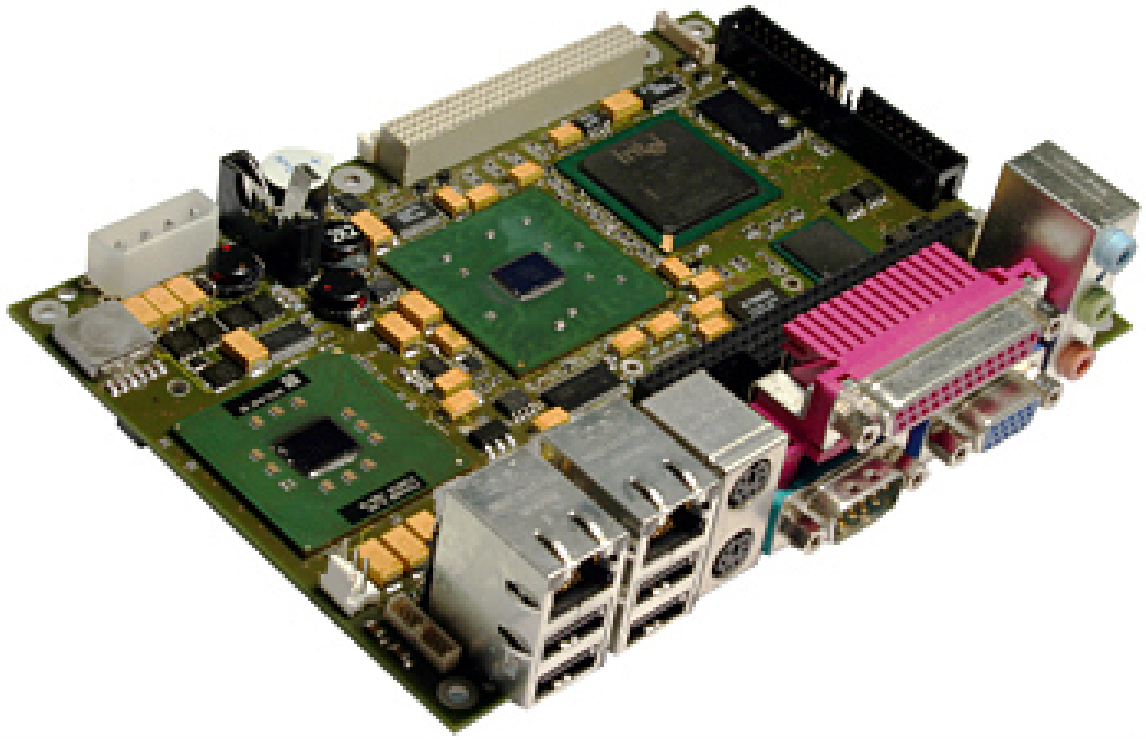
Kontron User's Guide



EPIC/PM

Document Revision 1.16

Table of Contents

1 User Information 9

1.1 About This Document 9
1.2 Copyright Notice 9
1.3 Trademarks 9
1.4 Standards 9
1.5 Warranty 9
1.6 Technical Support 10

2 Introduction 11

2.1 EPIC/PM 11
2.2 The EPIC Family 11

3 Getting started 12

4 Specifications 13

4.1 Functional Specifications 13
4.2 Mechanical Specifications 15
4.2.1 PC/104 Bus Connector (ISA part) 15
4.2.2 PC/104-Plus Bus Connector (PCI part) 15
4.2.3 Height on Top 15
4.2.4 Height on Bottom 15
4.2.5 Weight 15
4.3 Electrical Specifications 16
4.3.1 Supply Voltages 16
4.3.2 Supply Voltage Ripple 16
4.3.3 Supply Current (typical) 16
4.3.4 Supply Current (maximum) 17
4.3.5 Real-time Clock (RTC) Battery 18
4.4 MTBF 19
4.5 Environmental Specifications 19
4.5.1 Temperature 19
4.5.2 Humidity 19

5 CPU, Chipset and Super I/O 20

5.1 CPU 20
5.2 Chipset 20
5.2.1 GMCH (855GME Chipset) 20
5.2.2 ICH4 (82801DB) 21
5.3 Super I/O 22
5.4 CPU, Chipset and Super-I/O Configuration 22

6 System Memory 23

7 ISA and PCI Bus Expansion 24

7.1 PC/104 Bus (ISA part) 24
7.1.1 PC/104 Connectors 24
7.1.2 PC/104 Configuration 24
7.2 PC/104-Plus (PCI part) 25
7.2.1 PC/104-Plus Connector 25
7.2.2 PC/104-Plus Configuration 25

8 Keyboard and Mouse Interface 26

8.1 PS/2-Keyboard Connector 26
8.1.1 PS/2-Keyboard Configuration 26
8.2 PS/2-Mouse Connector 26
8.2.1 PS/2-Mouse Configuration 27

9 USB INTERFACES 28

9.1 Front Connectors (USB 0 to USB 3) 28
9.2 Internal Connectors (USB 4 and USB 5) 28
9.2.1 Limitations of USB Ports 4 and 5 29
9.3 Configuration 29

10 Ethernet Interface 30

10.1 First Ethernet Controller 30
10.2 Second Ethernet Controller 30
10.3 Connectors 31
10.4 Configuration 31
10.5 Ethernet Technical Support 32

11 Graphic Interfaces 33

11.1 Video Controller 33
11.2 CRT Connector 33
11.3 DVO Connector 34
11.4 Flat Panel LVDS Interface (JILI) Connector 35
11.5 Display Power Considerations 35
11.6 Connecting a LCD Panel 35
11.7 Configuration 36
11.8 Graphics Technical Support 36
11.9 Available Video Modes 36
11.9.1 Standard IBM-Compatible VGA Modes 36
11.9.2 Extended VESA VGA Modes 37

12 Serial-Communication Interfaces 38

12.1 Serial Ports COMA to COMD 38
12.2 Onboard RS-232 Connector 38
12.3 RS-485 Connector 39
12.4 Configuration 39

13 Parallel-Port Interface 40

13.1 Connector 40
13.2 Configuration 40

14 IDE-Interfaces 41

14.1 Connector 41
14.2 CompactFlash Socket 42
14.3 Configuration 42

15 Floppy Interface 43

15.1 Connector 43
15.1.1 Connector Diagram 44
15.2 Configuration 44

16 Sound Interface 45

16.1 Connectors 45
16.1.1 Jack Connector 45
16.1.2 Line-In/Rear Speakers Connector 46
16.2 Configuration 47
16.3 Technical Support for Sound 47

17 General Purpose I/O 48

17.1 Connector 48
17.2 Programming 48
17.2.1 16-Bit Operating Systems 49
17.2.2 32-Bit Operating Systems 49
17.2.3 Register Description: 49
17.2.4 Output Waveforms 52
17.3 SMBus Interface 52

18 Fan Interface 53

18.1 CPU Fan Connector 53
18.2 CPU Fan Configuration 53
18.3 Chassis Fan Connector 53
18.4 Chassis Fan Configuration 54

19 Power Interface 55

19.1 Power Interface Connectors 55
19.1.1 ATX Connector Version 55
19.1.2 AT Connector Version 56
19.1.3 Configuration 56
19.2 ATX/Reset/2LED Interface 56
19.2.1 Configuration 57

20 Watchdog Timer 58

20.1 Configuration 58
20.2 Programming 58
20.2.1 Initialization 58
20.2.2 Trigger 58

21 Hardware Monitor 59

21.1 Configuration 59

22 Important Technology Information 60

22.1 Max CPU Frequency setting 60
22.2 Thermal Monitor and Catastrophic Thermal Protection 60
22.2.1 Thermal Monitor 60
22.2.2 Catastrophic Thermal Protection 61
22.3 Processor Performance Control 61
22.4 Thermal Management 62
22.4.1 Processor Clock Throttling 62
22.5 I/O APIC vs. 8259 PIC Interrupt mode 63
22.6 Native vs. compatible IDE mode 63
22.6.1 Compatible IDE Mode 63
22.6.2 Native Mode 63
22.6.3 Native Mode Configuration 64

23 Appendix A: System-Resource Allocation 65

23.1 Interrupt Request (IRQ) Lines 65
23.2 Direct Memory Access (DMA) Channels 66
23.3 Memory Map 67
23.3.1 Using Expanded Memory Managers 67
23.4 I/O Address Map 68
23.5 Peripheral Component Interconnect (PCI) Devices 69

24 Appendix B: BIOS Operation 70

24.1 Determining the BIOS Version 70
24.2 Configuring the System BIOS 70

24.2.1 Start Phoenix BIOS Setup Utility 71
24.2.2 General Information 71
24.3 Main Menu 72
24.3.1 Master or Slave Submenus 73
24.4 Advanced Menu 74
24.4.1 Advanced Chipset Control Submenu 74
24.4.2 PCI/PNP Configuration Submenu 74
24.4.3 PCI Device, Slot #x Submenu 75
24.4.4 PCI/PNP ISA IRQ Resource Exclusion Submenu 75
24.4.5 Memory Cache Submenu 76
24.4.6 I/O Device Configuration Submenu 77
24.4.7 USB Options 77
24.4.8 LAN Options 78
24.4.9 SIO Options 79
24.4.10 Keyboard Features Submenu 80
24.4.11 Hardware Monitor Submenu 80
24.4.12 Watchdog Settings Submenu 80
24.4.13 Display Control Submenu 81
24.4.14 Miscellaneous Submenu 81
24.5 Security Menu 83
24.6 Power Menu 84
24.6.1 ACPI Resume Events 85
24.6.2 ACPI Control Submenu 86
24.7 Boot Menu and Utilities 86
24.7.1 MultiBoot XP 86
24.7.2 Boot First Function 87
24.8 Exit Menu 88
24.9 Kontron BIOS Extensions 88
24.9.1 JIDA BIOS extension 88
24.9.2 Remote Control Client Extension 89
24.9.3 LAN PXE ROM 89
24.10 Updating or Restoring BIOS Using PhoenixPhlash 90
24.10.1 Flashing a BIOS 90
24.10.2 Preventing Problems When Updating or Restoring BIOS 91

25 Appendix C: Block Diagram 92

26 Appendix D: Mechanical Dimensions 93

26.1 Top View 93
26.2 Front View 94

27 Appendix E: Connector Layout 95

27.1 Top Side 95

27.2 Bottom Side 96
27.3 Connector Functions and Interface Cables 97
27.4 Pin-out Table 99

28 Appendix F: PC Architecture Information 102

28.1 Buses 102
28.1.1 ISA, Standard PS/2 - Connectors 102
28.1.2 PCI 102
28.2 General PC Architecture 102
28.3 Ports 103
28.3.1 RS-232 Serial 103
28.3.2 ATA 103
28.3.3 USB 103
28.4 Programming 103

29 Appendix G: Document Revision History 104

1 User Information

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1.4 Standards

Kontron Embedded Modules GmbH is certified to ISO 9000 standards.

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Technicians and engineers from Kontron Embedded Modules GmbH and/or its subsidiaries are available for technical support. We are committed to making our product easy to use and will help you use our products in your systems.

Before contacting Kontron Embedded Modules GmbH technical support, please consult our Web site at http://www.kontron-emea.com/emd for the latest product documentation, utilities, and drivers. If the information does not help solve the problem, contact us by telephone or email.

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2 Introduction

2.1 EPIC/PM

The EPIC/PM hosts an Intel® Pentium® M processor in combination with an Intel® 855GME chipset with an integrated graphic memory controller hub. Celeron M versions of this board are possible, too. Two DDR-SDRAM-SODIMM sockets for up to 2 GB allows you to use standard DDR SODIMM memory modules. Six USB 2.0 ports and two 10/100 MBit Ethernet interface extend the standard connectivity of four serial, one parallel and a PS/2 mouse/keyboard interface besides 5.1 sound jackplugs.

The EPIC/PM is designed in the EPIC (Embedded Platform for Industrial Computing) form factor, which is an international standard of the PC/104 Consortium and can be extended with standard PC/104 and PC/104-Plus extension modules. This provides a flexible, space-saving and cost-optimized industrial computer solution.

2.2 The EPIC Family

Each EPIC is a member of the EPIC family of Kontron Embedded Modules GmbH.

Each EPIC module has the same front connectivity for Reset/ATX feature, 4xUSB ports, 2 LAN interfaces, PS/2 Keyboard, PS/2 Mouse connector, Compact-Flash socket, VGA, LPT and one serial port. These family features allow the use of the same chassis over the whole product line and maximize design reuse.

EPIC modules allow the use of standard notebook SODIMM memory modules and full ATX power supplies. An optional 5V-only version is available, too. These homogeneous features facilitate easy upgrades within the EPIC product family.

Display connections are simplified when using the onboard standard DVO and JILI Interface (JUMPtec® Intelligent LVDS Interface). JILI automatically recognizes which display is connected and independently sets all video parameters. All EPIC modules are plug-and-work enabled to further reduce time-to-market.

As part of the standard features package, all EPIC modules come with a JUMPtec Intelligent Device Architecture (JIDA) interface, which is integrated into the BIOS. This interface enables hardware-independent access to EPIC features that cannot be accessed via standard APIs. Functions such as watchdog timer, brightness and contrast of LCD backlight, and user bytes in the EEPROM can be configured with ease by taking advantage of this standard EPIC module feature.

The EPIC line products support the PC/104-Plus (PCI) and the PC/104 (ISA) standard via Kontron's own, special PCI-to-ISA bridge. Because of the availability of both extension buses, all past and future PC/104 expansion assemblies with state-of-the-art processor performance can be accommodated.

3 Getting started

Getting started with the EPIC/PM is very easy. For location of the connectors, see Appendix E: Connector Layout.

Take the following steps:

1. Turn off the power supply.
2. Connect the power supply to the EPIC's power supply connector. The board is available in a 10-pin ATX version.
3. Plug a memory module(s) into the memory socket(s) of the EPIC.
4. Connect the CRT monitor to the CRT interface or a LCD panel to the JILI interface by using a corresponding adapter cable.
5. Plug the keyboard and the mouse to the PS/2 connectors or use USB keyboard or mouse.
6. Connect the floppy drive cable to the EPIC's floppy interface. Attach the floppy drive to the connector at the opposite end of the cable.
7. Connect the power supply to the floppy's power connector.
8. Plug a hard-drive data cable to the EPIC's hard-disk interface.
9. Attach the hard disk to the connector at the opposite end of the cable.
10. If necessary, connect the power supply to the hard disk's power connector.
11. If required, plug a PC/104 or PC/104+ extension card
12. Make sure all your connections have been made correctly.
13. Turn on power.
14. Enter the BIOS by pressing the F2 key during boot-up. Make all changes in the BIOS setup. See the BIOS chapter of this manual for details.

4 Specifications

4.1 Functional Specifications

Processor

- Intel® Pentium®-M 1.8GHz CPU
- Intel® Celeron®-M 1.0GHz ULV
- Intel® ZeroCache CPU 0.8GHz ULV
- CPU socket supports all Pentium®-M in PGA package
- Further processor support planned

Chipset

- Intel® 855GME Chipset graphics memory controller hub

Power Supply

- Full ATX power supply support
- +5V-single supply (5V and 5Vstb)

Super I/O

- SMSC SCH3114

Cache

- On-die second level cache between 512KB and 2MB depending on used CPU

Memory

- Two 200-pin SODIMM unbuffered DDR SDRAM, each up to 1 GB

Four Serial Ports (COM A to COM D)

- 3 RS232C serial ports (1 DSUB9 at the front, 3 internal, 10-pin headers)
- 16550 compatible
- COM D configurable as RS422/485

One Parallel Port (LPT1)

- Enhanced Parallel Port (EPP) and Extended Capabilities Port (ECP) with bi-directional capability

Floppy Interface

Intelligent Drive Electronics (IDE)

- One UDMA Peripheral Component Inter-connect (PCI) Bus Master IDE port (up to two devices)
- One Compact Flash Type 1 as EIDE Secondary Master

Compact Flash Socket

System Monitor Controller for Temperature, Fan and Chassis Fan

Universal Serial Bus (USB)

- 6 USB 2.0 ports (4 at the front, 2 internal via 4-pin headers
- USB legacy keyboard support
- USB-boot support

Ethernet

- Integrated Intel® 82562 10/100BASE-T LAN
- Additional Intel® 82551ER 10/100BASE-T LAN
- Follows the common criteria of the embedded technology market segment

Onboard Video Graphics Array (VGA)

- Intel® 855GM/GME Chipset graphics memory controller hub with Intel® Extreme Graphics 2 technology
- CRT (Cathode Ray Tube) and LCD flat panel LVDS interface (JILI)
- LCD (Liquid Crystal Display) flat panel 2x24bit LVDS interface that uses JILI

Audio

- Integrated in Intel® SoundBlaster™ AC97
- Windows Sound System™ compatible
- 3 jack plugs (Line-in/Line-out/Mic).
- Extra standard Line-in connector (Motherboard-like)
- 5.1 Sound compatible

Phoenix BIOS, 1024KB Flash BIOS

NV-EEPROM for CMOS Setup Retention without Battery

PS/2 Keyboard Controller

PS/2 Mouse Controller

Watchdog timer (WDT)

Real Time Clock (RTC) with Onboard Battery Supply

15 General Purpose Input/Outputs (GPIOs)

4.2 Mechanical Specifications

4.2.1 PC/104 Bus Connector (ISA part)

One 2 X 32 pin stackthrough and one 2 X 20 pin stackthrough connector

4.2.2 PC/104-Plus Bus Connector (PCI part)

One 4 x 30 pin 2mm downward connector

4.2.3 Height on Top

Max 32mm (1.26”)

Height is depending upon CPU cooler/fan.

4.2.4 Height on Bottom

Maximum 9.7mm (0.38”)

4.2.5 Weight

About 320g (full featured version with passive CPU cooler, without DDR SDRAM)

4.3 Electrical Specifications

4.3.1 Supply Voltages

EPIC -PM boards are equipped with a 10 pin ATX power- connector. The EPIC-PM board requires at least +5V and +5V standby. The voltages +3.3V, +12V, -12V and –5V are not required for the operation of the EPIC itself. Varying voltages may be required for peripheral devices such as backlight inverters or PC/104 and PC/104-Plus extension modules.

- +5V DC +/- 5%
- +5V DC Standby +/- 5%
- +3,3V DC (required for 3.3V PC/104-Plus extension cards)
- +12V DC (required for some PC/104, PC/104-Plus extension cards or for JILI cables)
- -12V DC (required for some PC/104, PC/104-Plus extension cards)

4.3.2 Supply Voltage Ripple

- 100mV peak to peak 0 - 20MHz

4.3.3 Supply Current (typical)

The EPIC/PM is equipped with power-saving features. Different power-consumption tests were executed to give an overview of the electrical conditions for several operational states. The board used a 512MB DDR SDRAM module. The attached hard disk was not supplied through the measurement path and no extension module was mounted on the system.

- EPIC/PM 0.8GHz (ZeroCache CPU)

Operation State	Power Supply	
	+5V	+5V stby
DOS Prompt		
DOS Standby		
Windows Idle		
Windows Standby		
Windows 100% CPU Load		

- EPIC/PM 1.0GHz (Celeron-M®)

Operation State	Power Supply	
	+5V	+5Vstby
DOS Prompt		
DOS Standby		
Windows Idle		
Windows Standby		
Windows 100% CPU Load		

➤ EPIC/PM 1.8GHz

Operation State	Power Supply	
	+5V	+5VStby
DOS Prompt	[redacted]	[redacted]
DOS Standby	[redacted]	[redacted]
Windows Idle	[redacted]	[redacted]
Windows Standby	[redacted]	[redacted]
Windows 100% CPU Load	[redacted]	[redacted]

4.3.4 Supply Current (maximum)

Board	Power Supply	
	+5V	+5VStby
EPIC/PM 0.8GHz	[redacted]	[redacted]
EPIC/PM 1.0GHz	[redacted]	[redacted]
EPIC/PM 1.8GHz	[redacted]	[redacted]

(calculated theoretical values from all components maximum supply currents)

4.3.5 Real-time Clock (RTC) Battery

- Voltage range: 1.8V - 4.0V (typ 3.0V)
- Quiescent current: max. 3,5uA@ 3.0 V

English:

CAUTION ! Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.

Deutsch:

VORSICHT ! Explosionsgefahr bei unsachgemäßem Austausch der Batterie. Ersatz nur durchden selben oder einen vom Hersteller empfohlenen gleichwertigen Typ. Entsorgung gebrauchter Batterien nach Angaben des Herstellers.

French:

ATTENTION ! Risque d'explosion avec l'échange inadéquat de la batterie. Remplacement seulement par le même ou un type équivalent recommandé par le producteur. L'évacuation des batteries usagées conformément à des indications du fabricant.

Danish:

ADVARSEL ! Lithiumbatteri – Eksplosionsfare ved fejlagtig Håndtering. Udskifting må kun skemed batteri af samme fabrikant og type. Lever det brugte batteri tilbage til leverand□ren.

Finnish:

VAROITUS ! Paristo voi räjähtää, jos se on virheellisesti asennettu. Vaihda paristo ainoastaan laltevalmistajan suosittelmaan tyyppiln. Havita kaytetty paristo valmistajan ohjeiden mukaisesti.

Spanish:

Precaución ! Peligro de explosión si la batería se sustituye incorrectamente. Sustituya solamente por el mismo o tipo equivalente recomendado por el fabricante. Disponga las baterías usadas según las instrucciones del fabricante.

The battery of this product is not considered to be accessible by the end user. Safety instructions are given only in English, German, French, Danish, Finish and Spanish. If the battery is accessible by the end user, it is in the responsibility of the customer to give the corresponding safety instructions in the required language(s).

4.4 MTBF

The following MTBF (Mean Time Between Failure) values were calculated using a combination of manufacturer's test data, if the data was available, and a Bellcore calculation for the remaining parts. The Bellcore calculation used is "Method 1 Case 1". In that particular method the components are assumed to be operating at a 50 % stress level in a 40° C ambient environment and the system is assumed to have not been burned in. Manufacturer's data has been used wherever possible. The manufacturer's data, when used, is specified at 50° C, so in that sense the following results are slightly conservative. The MTBF values shown below are for a 40° C in an office or telecommunications environment. Higher temperatures and other environmental stresses (extreme altitude, vibration, salt water exposure, etc.) lower MTBF values.

- System MTBF (hours) : (171.636) TBD

Notes: *Fans usually shipped with Kontron Embedded Modules GmbH products have 50,000-hour typical operating life. The above estimates assume no fan, but a passive heat sinking arrangement.*
Estimated RTC battery life (as opposed to battery failures) is not accounted for in the above figures and need to be considered for separately. Battery life depends on both temperature and operating conditions. When the Kontron unit has external power; the only battery drain is from leakage paths.

4.5 Environmental Specifications

4.5.1 Temperature

The Intel® Mobile Pentium-M is specified for proper operation when junction temperature is within the specified range of 0 °C to 100 °C.

The Intel® 855GM/GME Chipset temperature and the Intel® ICH4 I/O Controller Hub 4 (82801DB) case temperature are maximum 110C.

- Operating: 0 to +65 °C (*) (with appropriate airflow)
- Non-operating: -10 to +85 C (non-condensing)

Note: *(*) The maximum operating temperature is the maximum measurable temperature on any spot on the module's surface. You must maintain the temperature according to the above specification.*

4.5.2 Humidity

- Operating: 10% to 90% (non-condensing)
- Non-operating: 5% to 95% (non-condensing)

5 CPU, Chipset and Super I/O

5.1 CPU

The EPIC/PM is available with an Intel® Mobile Pentium®-M or Celeron®-M central processing unit (CPU) from 0.8GHz up to 1.8GHz or 1.8GHz. However, other GHz as well as Celeron®-M versions (half cache size, no SpeedStep® technology) of this board are available.

Intel® Mobile Pentium®-M CPU features include:

- Supports Intel® Architecture with Dynamic Execution
- High performance, low-power core
- On-die, primary 32-kbyte instruction cache and 32-kbyte write-back data cache
- On-die, up to 2-MByte (depends on CPU) second level cache with Advanced Transfer Cache Architecture
- Advanced Branch Prediction and Data Prefetch Logic
- Streaming SIMD Extensions 2 (SSE2)
- 400-MHz, Source-Synchronous processor system bus
- Advanced Power Management features, including Enhanced Intel SpeedStep® technology (only for Pentium® M processors)

5.2 Chipset

The chipset of the EPIC/PM consists of the Intel® 855GME chipset GMCH (Graphics and Memory Controller Hub) and the Intel ® 82801DB ICH-4 (I/O Controller Hub 4).

5.2.1 GMCH (855GME Chipset)

Processor/Host Bus Support

- Intel® Pentium® M and Celeron® M processors
- Supports system bus at 400MHz
- Supports Enhanced Intel® SpeedStep® technology

Memory System

- Directly supports one DDR SDRAM channel, 64-bits wide
- Supports 200/266-MHz DDR SDRAM devices with double-sided SO-DIMMs (four rows populated) with unbuffered PC1600/PC2100 DDR SDRAM.
- Supports 128-Mbit, 256-Mbit, and 512-Mbit technologies providing maximum capacity of 1 GB with x16 devices
- All supported devices have four banks

Internal Graphics Features

- Up to 32MB of dynamic video memory allocation
- Display image rotation
- Graphics core frequency
- Display core frequency at 133MHz or 200MHz
- Render core frequency at 100MHz,133MHz, 200MHz
- 2D graphics engine
- 3D graphics engine
- Single- or dual-channel LVDS panel support up to UXGA panel resolution with frequency range from 25MHz to 112MHz (single channel/dual channel)

Video Stream Decoder

- Improved hardware motion compensation for MPEG2
- Software DVD at 60 Fields/second and 30 frames/second full screen
- Support for standard definition DVD (i.e. NTSC pixel resolution of 720x480, etc.)
- quality encoding at low CPU utilization

Power Management

- APM 1.2 compliant power management
- ACPI 1.0b, 2.0 support
- Enhanced Intel® SpeedStep Technology support

5.2.2 ICH4 (82801DB)

PCI 2.2 Bus interface at 33MHz

Integrated LAN controller

- WfM 2.0 and IEEE802.3 compliant with 10/100 Mbit/s Ethernet support

USB

Three UHCI USB 1.1 or one EHCI high speed USB 2.0 host controller(s)

Supporting up to 6 ports (4 available on EPIC board's front, 2 on internal pin headers)

AC-Link for AC'97 support

Integrated IDE controller

- Ultra ATA/100/66/33 and PIO mode support
- Two channels for up to 3 devices with independent timing

- Support of “Native Mode” register and interrupts

Interrupt Controller

- Two cascade 83C59 with 15 interrupts
- Integrated I/O APIC capability with 24 interrupts

Enhanced DMA

- Two cascaded 8237 controllers
- Supports PC/PCI DMA and LPC DMA
- Supports DMA collection buffers

Timers based on 82C54

Power Management Logic

- ACPI 2.0 compliant
- Supports PCI PME#

Low Pin Count (LPC) Interface

SM Bus 2.0 interface (System Management Bus)

5.3 Super I/O

The super I/O device is a SMSC SCH3114 that is connected to the LPC (Low Pin Count) Bus. This device provides the following additional features:

- Four serial ports (one RS232 available on EPIC board’s front as DSUB connector and three ports on internal pin headers with one port capable of RS422/RS485 functionality)
- One Multi-Mode Parallel Port at board front plate
- Floppy Disk Controller
- PS/2-Keyboard Controller and PS/2-Mouse Interface at board front plate
- 5V CPU Fan and 12V Chassis Fan

5.4 CPU, Chipset and Super-I/O Configuration

See the Advanced Menu and its submenus section of the Appendix B: BIOS chapter for information on possible settings.

6 System Memory

The EPIC/PM supports 200-pin SODIMM DDR-SDRAM memory modules. Two sockets are available for 2.5V (power level), unbuffered double data rate synchronous dynamic random access memory (DDR-SDRAM) each up to 1024MB following Intel's DDR266/PC2100 Specification.

The supported devices on the DDR-SDRAM module must be 128-Mbit, 256-Mbit or 512-Mbit technologies chips. All modules validated by Intel with the 845 chipset and minimum DDR266 speed are electrical ready with the 855 chipset (A similar memory interface is used on the two chipsets.)

Notes: Some older modules and modules out of specification are designed for 2.7V (power level). These modules may not work well at the EPIC/PM.

The total amount of memory available on the DDR-SDRAM modules is used for main memory and graphics memory on the EPIC/PM. Unified Memory Architecture (UMA) manages the sharing of the system memory between the graphics controller and processor. Full system memory size is not available for software applications. Up to 32MB of system memory are used for graphics memory.

Notes: When the lower Memory socket will be used, then must be used following Memory RAM Modules

97007-1024-00-0EPBA	*for 1GByte*	*Memory RAM*	*(K-SDN12864S4B52MT-60CR)*
97007-2560-00-0EPBA	*for 256MByte*	*Memory RAM*	*(K-SDN0326403B41MT-60CR)*
97007-5120-00-0EPBA	*for 512MByte*	*Memory RAM*	*(K-SDN0646403B42MT-60CR)*

7 ISA and PCI Bus Expansion

The design of the EPIC/PM follows the standard EPIC (Embedded Platform for Industrial Computing) form factor and offers ISA- and PCI-bus signals. The PC/104-Plus standard is downward compatible with PC/104 and enables the use of standard PC/104 and PC/104-Plus adapter cards as on-top modules.

7.1 PC/104 Bus (ISA part)

The PC/104 bus consists of two connectors that use 104 pins in total.

- XT bus connector (64 pins)
- AT bus connector (40 pins, which is optional for 16-bit, data-bus system)

The pin-out of the PC/104 bus connectors corresponds to the pin-out of the ISA bus connectors with some added ground pins. The two PC systems with different form factors are electrically compatible.

The XT bus connector, Row A and B.

The corresponding 64-pin female header (ISA bus = 62pins) has two added ground pins at the end of the connector (Pin A32 and Pin B32). The pin-out between PC/104 bus and XT ISA bus is identical between A1 - A31 and B1 - B31.

The AT bus extension connector, Row C and D.

The corresponding 40-pin female header (ISA bus = 36 pins) has four added ground pins, including two on each side of the connector. To avoid confusion, the first two pins are defined as Pin C0 and Pin D0. The additional ground pins at the end of the connector are defined as C19 and D19. The pin-out between PC/104 bus and AT ISA bus is identical between C1 - C18 and D1 - D18.

7.1.1 PC/104 Connectors

The EPIC/PM features the XT bus and AT bus extension on two, dual-row socket connectors with a 2.54mm x 2.54mm grid (0.1" x 0.1").

The PC-104 bus is available through Connectors X10B and X12A.

A description of the signals, including electrical characteristics and timings is beyond the scope of this document. Please refer to the official ISA bus and PC/104 specifications for more details.

7.1.2 PC/104 Configuration

When using add-on boards on the PC/104 bus, make sure that there are no resource conflicts in the system. Carefully choose hardware interrupts, DMA channels, memory- and I/O address ranges to avoid resource conflicts, which are often the reason for a board or a feature not functioning correctly. See Appendix A: System Resource Allocation for information about the resources already used by the EPIC/PM.

7.2 PC/104-Plus (PCI part)

The EPIC/PM offers the PC/104-Plus bus on a quad-row female connector with a 2mm x 2mm (0.79" x 0.79") pitch. This connector implements the standard 32-bit PCI bus signals.

7.2.1 PC/104-Plus Connector

You can only use PC/104-Plus adapter boards on top of an EPIC/PM.

The PC/104-Plus bus is available through Connector X9.

A description of signals, including electrical characteristics and timings, is beyond the scope of this document. Please refer to the official PCI bus and PC/104-Plus specifications for more details.

7.2.2 PC/104-Plus Configuration

Add-on boards on the PC/104-Plus bus have to be associated to a "PCI-slot." Make sure that there are no resource conflicts in the system. Carefully choose PCI interrupts, REQ/GNT pairs, and IDSEL for the add-on board. See the technical manual of the add-on board for more details.

The EPIC/PM's PCI bus can be configured to optimize your system. See the PCI Configuration Submenu in Appendix B: BIOS for more information on configuration.

8 Keyboard and Mouse Interface

The EPIC/PM offers a PS/2-keyboard and PS/2-mouse interface on Connector X18. The upper interface is for the Mouse and the lower interface for the Keyboard connection. To find the location of the keyboard and mouse connector, please see the Appendix E: Connector Layout chapter.

8.1 PS/2-Keyboard Connector

The following table shows the pin-out of the PS/2-keyboard connector on the front.

Header	Pin	Signal Name	Function
	1	KBDAT	PS/2 Keyboard data (bi-directional I/O)
	2	NC	Not connected
	3	GND	Ground
	4	VCC *	+5V (max. current 500mA, shared with PS/2 Mouse Con)
	5	KBCLK	PS/2 Keyboard clock (bi-directional I/O)
	6	NC	Not connected

Notes: (*) To protect the external power lines of peripheral devices, make sure that:
-- the wires have the right diameter to withstand the maximum available current
-- the enclosure of the peripheral device fulfils the fire-protecting requirements of IEC/EN 60950.

8.1.1 PS/2-Keyboard Configuration

Refer to the Keyboard Features submenu and the I/O Device Configuration submenu in the Appendix B: BIOS Operation chapter for information on configuration.

8.2 PS/2-Mouse Connector

The following table shows the pin-out of the PS/2-Mouse connector on the front.

Header	Pin	Signal Name	Function
	1	MSDAT	Mouse data (bi-directional I/O)
	2	NC	Not connected
	3	GND	Ground
	4	VCC *	+5V (max. current 500mA, shared with PS/2 Keyboard Con)
	5	MSCLK	Mouse clock (bi-directional I/O)
	6	NC	Not connected

Notes: (*) To protect the external power lines of peripheral devices, make sure that:
-- the wires have the right diameter to withstand the maximum available current
-- the enclosure of the peripheral device fulfils the fire-protecting requirements of IEC/EN 60950.

8.2.1 PS/2-Mouse Configuration

You can set the PS/2 mouse to enabled, disabled or auto-detect from the BIOS Setup. If you enable the mouse, IRQ12 is used as the interrupt and is no longer available for other devices. Please refer to the

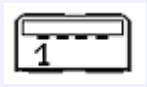
Miscellaneous Submenu in the Appendix B: BIOS Operation chapter for additional information on configuration.

9 USB INTERFACES

The EPIC/PM offers 6 USB ports. These ports are driven by either three UHCI USB 1.1 or one EHCI USB 2.0 controller(s). Four of the 6 USB ports are available on the EPIC/PM front, and two more ports are available on internal connectors. You can expand the ports for up to 127 USB peripherals by using external USB hubs.

9.1 Front Connectors (USB 0 to USB 3)

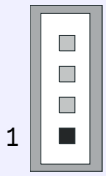
The four USB interfaces on the front are available through the multi-functional Connectors X5 and X21. To find the location of the USB connectors, please see the Appendix E: Connector Layout chapter. The following table shows the pin-out of these USB interfaces.

Header	Pin	Signal Name	Function
	1	USB_5V *	USB-supply (max. 500mA)
	2	USB-	Universal serial bus port (-)
	3	USB+	Universal serial bus port (+)
	4	USB_GND	USB Ground

Notes: (*) To protect the external power lines of peripheral devices, make sure that:
-- the wires have the right diameter to withstand the maximum available current
-- the enclosure of the peripheral device fulfils the fire-protecting requirements of IEC/EN 60950.
-- The USB power lines are protected with a resetable fuse and are limited to 500mA

9.2 Internal Connectors (USB 4 and USB 5)

The two internal USB interfaces are available through the Connectors X20 and X25 (4 pins). The following table shows the pin-out of these additional USB interfaces.

Header	Pin	Signal Name	Function
	1	VCC *	USB supply (max. 500mA)
	2	USB-	USB port (-)
	3	USB+	USB port (+)
	4	GND	USB Ground

Notes: (*) To protect the external power lines of peripheral devices, make sure that:
-- the wires have the right diameter to withstand the maximum available current
-- the enclosure of the peripheral device fulfils the fire-protecting requirements of IEC/EN 60950.
-- The USB power lines are not protected. An additional resetable fuse is recommended.

9.2.1 Limitations of USB Ports 4 and 5

The power contacts for USB devices on Pin 1 and Pin 4 are not protected. They are suitable to supply connected USB devices with a maximum of 500mA power dissipation. Do not supply external USB devices with higher power dissipation through these pins. Always use a fuse when powering external USB devices through these pins, otherwise a defective USB device may damage the EPIC/PM. Kontron recommends using a resettable fuse, which follows the USB 1.1 specification, for power on external USB connectors.

9.3 Configuration

You can enable or disable the three USB UHCI Host Controllers in the BIOS Setup Utility for support of USB 1.1 devices. USB Host Controller 1 serves the two USB Ports 0 and 1 on the front. USB host Controller 2 serves the USB Ports 2 and 3 on the front. USB Controller 3 only needs to be enabled for the use of two more internal ports.

For high-speed USB 2.0 support of all 6 available ports, enable the USB EHCI Host Controller.

You also can enable or disable the legacy USB support. Legacy support is required for a USB keyboard and a USB Mouse when used with non USB aware operating systems such as Unix or DOS. It also is required to boot from USB mass storage devices. For more information, see the I/O Device Configuration Submenu section in Appendix B: BIOS Operation.

You can download available drivers or get driver download support information from the Kontron Web site. Kontron offers the latest Kontron-tested drivers, which can differ from newer ones. For further technical questions, contact your local support or get support information and downloadable software updates from Intel®.

Notes: *1. Some operating systems without USB 2.0 support do not work well with EHCI controller enabled. If you install such an OS at the EPIC/PM please disable the EHCI controller in the Setup Utility before installation.*
2. For operating systems not listed on our Web site please contact your OS distributor for an USB 2.0 driver. We are not allowed by law to ship USB 2.0 drivers.

10 Ethernet Interface

The EPIC/PM comes with two Ethernet interfaces. The first Ethernet interface uses the ICH4's integrated 32-bit PCI LAN controller in combination with the Intel® 82562 platform LAN connect device. The second Ethernet interface uses the Single Chip Fast Ethernet NIC Controller Intel 82551ER.

The two network controllers support a 10/100Base-T interface. The devices auto-negotiate the use of a 10Mbit/sec or 100Mbit/sec connection.

All major network-operating systems and several real-time and embedded operating systems support the interface.

Note: For safe date transfer with the 82551ER the maximum cable length should not be longer than 70m. With the 82562EZ the maximum cable length is 85m. For detailed values see test report

10.1 First Ethernet Controller

The Intel® 82562 features are:

- IEEE 802.3 10Base-T/100Base-TX compliant physical layer interface
- IEEE 802.3u Auto-Negotiation support
- IEEE 802.3x Full Duplex Flow Control standard
- Digital Adaptive Equalization control
- Link status interrupt capability
- 10Base-T auto-polarity correction
- Platform LAN connect interface support
- Diagnostic loopback mode
- 1:1 transmit transformer ratio support
- Low power (less than 300mW in active transmit mode)
- Reduced power in "unplugged mode"

Note: The Ethernet interface works according to the common criteria of the embedded technology market segment.

10.2 Second Ethernet Controller

The Intel® 82551ER features are:

- TCP, UDP, IPv4 Checksum Offload
- Received Checksum Verification
- Multiple Priority Transmit Queues
- Integrated IEEE 802.3 10BASE-T and 100BASE-TX compatible PHY
- ACPI and PCI Power Management standards compliance
- Improved dynamic transmit chaining with multiple priorities transmit queues

- Backward compatible software to 82559ER controller
- Full Duplex support at 10 and 100 Mbps
- IEEE 802.3u Auto-Negotiation support
- 3 Kbyte transmit and receive FIFOs
- Fast back-to-back transmission support with minimum interframe spacing
- IEEE 802.3x 100BASE-TX Flow Control support
- Advanced Power Management capabilities
- Improved Bit Error Rate performance
- HWI support

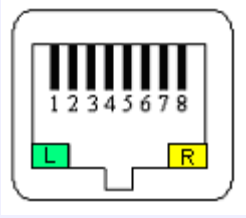
Note: The Ethernet interfaces work according to the common criteria of the embedded technology market segment.

10.3 Connectors

The 10/100Base-T interfaces are standard 8-pin RJ45 jacks. They are available at the front of the EPIC/PM through the multi-functional Connector X21 (Intel® 82562) and Connector X5 (Intel® 82551ER).

To find the location of the Ethernet interfaces, please see the Appendix E: Connector Layout chapter.

The following table shows the pin-out of the Ethernet connector.

Header	Pin	Signal Name	Function	In/Out
	1	TXD+	100/10BASE-T Transmit	Differential Output
	2	TXD-	100/10BASE-T Transmit	Differential Output
	3	RXD+	100/10BASE-T Receive	Differential Input
	4	NC **	For internal use only	
	5	NC **	For internal use only	
	6	RXD-	100/10BASE-T Receive	Differential Input
	7	NC **	For internal use only	
	8	NC **	For internal use only	
	L	Left LED	Link	Green/Orange
	R	Right LED	Activity	Yellow

NOTE: (**) Do not connect anything to these pins!

10.4 Configuration

The onboard LAN controller can be enabled or disabled in the BIOS Setup Utility. Additionally it is possible to enable the onboard LAN PXE boot ROM to allow the system to boot up via a network connection from a PXE boot server. Refer to the I/O Device Configuration Submenu in the Appendix B: BIOS Operation chapter for additional information on configuration.

You can download available drivers from the Kontron Web site. For further information read the read-me file or contact technical support.

10.5 Ethernet Technical Support

If any problems occur, you can solve some of them by using the latest drivers for the Intel® LAN controller. Kontron provides you with the latest Kontron-tested drivers, which can differ from newer ones. For further technical support, contact either Kontron or get support information and downloadable software updates from Intel®.

11 Graphic Interfaces

11.1 Video Controller

The EPIC/PM uses the graphics accelerator integrated in the Intel® 855GM/GME chipset, which delivers high-performance 2D, 3D and video capabilities. With its interface to UMA (Unified Memory Architecture) up to 32MB of system memory are used as video memory.

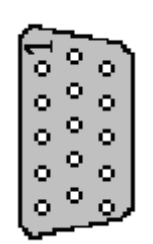
The controller can drive four interfaces with its two graphic engines on the EPIC/PM:

- Cathode Ray Tube (CRT) interface
- Low Voltage Differential Signaling (LVDS) interface
- 2 Digital Video Output (DVO) ports

11.2 CRT Connector

The CRT (Cathode Ray Tube) interface is available through a standard DSUB15 connector, which is part of the multi-function Connector X1 on the front.

The following table shows the pin-out of the CRT connector:

Header	Pin	Signal Name	Function
	1	RED	Red Video
	2	GRN	Green Video
	3	BLU	Blue Video
	4	NC	Not connected
	5	GND	Ground
	6	GND	Ground
	7	GND	Ground
	8	GND	Ground
	9	NC	Not connected
	10	GND	Ground
	11	NC	Not connected
	12	DDA	DDC Serial Data Line
	13	HSYNC	Horizontal Sync
	14	VSYNC	Vertical Sync
	15	DCK	DDC Data Clock Line

To find the location of the CRT interface, please see the Appendix E: Connector Layout chapter.

11.3 DVO Connector

The DVO (Digital Video Output) interface is available on Connector X4, a 50-pin, flat-foil connector on the bottom side of the board. To find the location of the DVO interface, please see the Appendix E: Connector Layout chapter. DVO interface usage excludes LVDS interface usage.

The following table shows the pin-out of the DVO connector.

Pin	Signal Name	Function	Pin	Signal Name	Function
1	DVOCD0	Channel-C / Data 0	2	DVOBD0	Channel-B / Data 0
3	DVOCD1	Channel-C / Data 1	4	VCC	+5V Power
5	DVOBD1	Channel-B / Data 1	6	DVOCD2	Channel-C / Data 2
7	DVOBD2	Channel-B / Data 2	8	VCC	+5V Power
9	DVOCD3	Channel-C / Data 3	10	DVOBD3	Channel-B / Data 3
11	DVOCD4	Channel-C / Data 4	12	GND	Ground
13	DVOBD4	Channel-B / Data 4	14	DVOCD5	Channel-C / Data 5
15	DVOBD5	Channel-B / Data 5	16	GND	Ground
17	DVOCD6	Channel-C / Data 6	18	DVOBD6	Channel-B / Data 6
19	DVOCD7	Channel-C / Data 7	20	GND	Ground
21	DVOBD7	Channel-B / Data 7	22	DVOCD8	Channel-C / Data 8
23	DVOBD8	Channel-B / Data 8	24	GND	Ground
25	DVOCD9	Channel-C / Data 9	26	DVOBD9	Channel-B / Data 9
27	DVOCD10	Channel-C / Data 10	28	GND	Ground
29	DVOBD10	Channel-B / Data 10	30	DVOCD11	Channel-C / Data 11
31	DVOBD11	Channel-B / Data 11	32	GND	Ground
33	DVOBCLK	Channel-B / Clock Out 0	34	DVOBCLK# (*)	Channel-B / Clock Out 1
35	GND	Ground	36	DVOCCLK	Channel-C / Clock Out 0
37	DVOCCLK# (*)	Channel-C / Clock Out 1	38	GND	Ground
39	DVOBVSYNC	Channel-B Vertical Sync	40	DVOBHSYNC	Channel-B Horiz. Sync
41	DVOBBLANK#	Channel-B Flicker Blank	42	DVOBFLDSTL	Channel-B Field Stall
43	DVOCVSYNC	Channel-C Vertical Sync	44	DVOCHSYNC	Channel-C Horiz. Sync
45	DVOCBLANK#	Channel-C Flicker Blank	46	DVOCFLDSTL	Channel-C Field Stall
47	DVOINT	LCD Interrupt	48	LTVDAT	LCD/TV Data
49	LTVCLK	LCD/TV Clock	50	VREF	Reference Voltage

(*) optional

11.4 Flat Panel LVDS Interface (JILI) Connector

The interface for the LCD Panel is available through the X26 connector (40 pins) on the top side of the board. This connector represents the JILI interface (JUMPtec Intelligent LVDS Interface). The implementation of this subsystem complies with the JILI Specification of Kontron Embedded Modules GmbH. The EPIC/PM already supports the JILI3 implementation. A variety of cables for different display types are available from Kontron. Please refer to the cable list on the Kontron Web site for part numbers and cable names. A detailed description of the JILI interface standard also is available in a separate document JILIM???.PDF. The three question marks represent the document's revision number. You can download the document from the Kontron Web site, or contact your local Kontron technical support to receive it.

To find the location of the LCD Panel interface connector, please see the Appendix E: Connector Layout chapter.

11.5 Display Power Considerations

When using a LCD Panel, additional voltages may be required to drive the display's logic and to supply the backlight converter and the display's contrast voltage.

The display logic may require +5V for standard or +3.3V for low-power LCDs. Contrast voltages for passive displays are normally very different and can range from –30V to +30V. Backlight converters usually are +5V or +12V types. When using a Kontron JILI cable, you do not need to determine such configurations. Display logic voltage and contrast voltage come pre-configured on the JILI cable. On occasion, backlight voltage has to be adjusted on the cable.

Even though the EPIC/PM is also available as a +5V-only board, you need to supply the +12V for the backlight converter additionally when using such a converter type.

The onboard 3.3V-circuitry of the EPIC/PM and the +3.3V logic voltage of low-voltage panels are powered by separate voltage regulators. The one for the LCD is mounted on the JILI adapter cable.

11.6 Connecting a LCD Panel

To determine whether your panel display is supported, check the Kontron Web site for panel lists. We regularly update the list of panels that have been tested with our boards.

Many panel adapters for a wide spread variety of displays are available through Kontron. If you use one of those adapters supplied by Kontron, configuration is easy:

1. Check whether you have the correct adapter and cable for the panel you plan to use. Inspect the cable for damages.
2. Disconnect the power from your system.
3. Connect the panel adapter to the LCD Panel connector (JILI) on the EPIC/PM.
4. Connect the other end of the cable to your display.
5. Connect the backlight converter.
6. Supply power to your system.

7. If no image appears on your display, connect a CRT monitor to the CRT connector.
8. If necessary program the EEPROM on the JILI cable with the matching configuration data.
9. If you still do not see improvement, consider contacting the dealer for technical support.

11.7 Configuration

You can set the general configuration for the graphic controller in the BIOS setup utility. Refer to the Advanced Chipset Control submenu and the Display Control submenu in the Appendix B: BIOS Operation chapter for more configuration information.

You can download drivers for the graphics controller from the Kontron Web site. For further information, read the read-me or help files or contact technical support.

11.8 Graphics Technical Support

If problems occur, you can solve some of them by using the latest drivers for the graphics controller. Kontron provides you with the latest tested drivers, which can differ from newer ones. For further technical support, contact either Kontron, or obtain support information and downloadable software updates from Intel®.

11.9 Available Video Modes

The following list shows the video modes supported by the graphics controller with maximum frame buffer size. When configured for smaller frame buffers and/or using a LCD panel on the JILI interface, not all of the video modes listed below may be available. Capability depends on system configuration and on display capabilities. Different operating systems also may not support all listed modes by the available drivers.

11.9.1 Standard IBM-Compatible VGA Modes

Video Mode	Type	Characters/Pixels	Colors/Gray val.
00h/01h	Text	40x25	16
02h/03h	Text	80x25	16
04h/05h	Graphics	320x200	4
06h	Graphics	640x200	2
0Dh	Graphics	320x200	16
0Eh	Graphics	640x200	16
0Fh	Graphics	640x350	Mono
10h	Graphics	640x350	16
11h	Graphics	640x480	2
12h	Graphics	640x480	16
13h	Graphics	320x200	256

11.9.2 Extended VESA VGA Modes

VESA	Display	Pixels	Colors
101h	Graphics	640x480	256
103h	Graphics	800x600	256
105h	Graphics	1024x768	256
107h	Graphics	1280x1024	256
111h	Graphics	640x480	64K
112h	Graphics	640x480	16M
114h	Graphics	800x600	64K
115h	Graphics	800x600	16M
117h	Graphics	1024x768	64K
118h	Graphics	1024x768	16M
11Ah	Graphics	1280x1024	64K
11Bh	Graphics	1280x1024	16M
13Ah	Graphics	1600x1200	256
13Ch	Graphics	1920x1440	256
14Bh	Graphics	1600x1200	64K
14Dh	Graphics	1920x1440	64K
15Ah	Graphics	1600x1200	16M
15Ch	Graphics	1920x1440	16M

12 Serial-Communication Interfaces

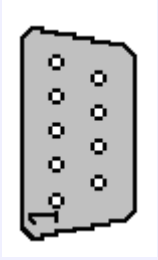
12.1 Serial Ports COMA to COMD

Four fully functional serial ports (COM A, COM B, COM C, and COM D) provide asynchronous serial communications. The serial ports support RS-232 operation modes and are compatible with the serial-port implementation used on the IBM Serial Adapter. You also can use COM D for RS-422/485 communications. The ports are 16550 high-speed UART compatible and support 16-byte FIFO buffers for transfer rates up to 115.2Kbaud. COM A is available on a standard DSUB9 connector on the front while the other COM ports are available on internal connectors.

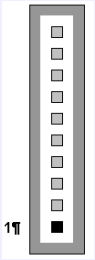
COM A is available through the standard DSUB9 connector, which is part of the multi-function Connector X1 on the front. COM B to COM D are available through Connectors X15, X16 and X17 (10 pins in line). To find the location of the serial ports on the board, please see the Appendix E: Connector Layout chapter.

12.2 Onboard RS-232 Connector

The following table shows the pin-out of COMA available at the front of the EPIC/PM board.

Header	Pin	Signal Name	Function	In / Out
	1	DCD1	Data Carrier Detect	In
	2	SIN1	Receive Data	In
	3	SOUT1	Transmit Data	Out
	4	DTR1	Data Terminal Ready	Out
	5	GND	Signal Ground	--
	6	DSR1	Data Set Ready	In
	7	RTS1	Request to Send	Out
	8	CTS1	Clear to Send	In
	9	RI1	Ring Indicator	In

COM B to COM D are available through Connectors X15, X16 and X17 (10 pins in line). To have the signals available on the standard serial interface connectors DSUB9 or DSUB25, an adapter cable is required. A 9-pin DSUB cable is available from Kontron (KAB-DSUB9-3, Part Number 96061-0000-00-0).

Header	Pin	Signal Name	Function	In / Out	DSUB-25	DSUB-9
	1	/DCD	Data Carrier Detect	In	8	1
	2	/DSR	Data Set Ready	In	6	6
	3	SIN	Receive Data	In	3	2
	4	/RTS	Request to Send	Out	4	7
	5	SOUT	Transmit Data	Out	2	3
	6	/CTS	Clear to Send	In	5	8
	7	/DTR	Data Terminal Ready	Out	20	4
	8	/RI	Ring Indicator	In	22	9
	9	GND	Signal Ground	--	7	5
	10	VCC (*)	+5V	--	--	--

Notes: (*) To protect the external power lines of peripheral devices, make sure that:
-- the wires have the right diameter to withstand the maximum available current
-- the enclosure of the peripheral device fulfils the fire-protecting requirements of IEC/EN 60950.

To find the location of the serial ports on the board, please see the Appendix E: Connector Layout chapter.

12.3 RS-485 Connector

You can use Connector X19 (COM D) for RS422/485 purposes.

Header	Pin	Signal Name	Function
	1	485_1RXD+	Channel A positive terminal
	2	485_1RXD-	Channel A negative terminal
	3	GND	Ground
	4	485_1TXD+	Channel B positive terminal
	5	485_1TXD-	Channel B negative terminal

The serial port COM D can only be used either as RS232 (Connector X17) or as RS422/RS485 (Connector X19).

12.4 Configuration

From the BIOS set-up utility, you can set the serial input/output interfaces to enabled, disabled or auto. The base I/O-addresses 3F8h, 2F8h, 3E8h, or 2E8h can be configured when enabled, as well as the interrupts IRQ3, IRQ4, IRQ10 and IRQ11. COM D can be set to the RS232 or RS485 interface. Refer to the I/O Device Configuration submenu in the Appendix B: BIOS Operation chapter for information on configuration.

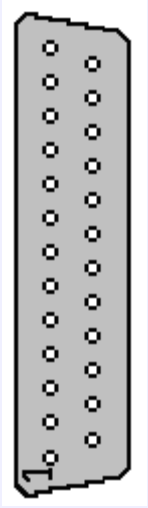
13 Parallel-Port Interface

The EPIC/PM incorporates an IBM XT/AT compatible parallel port. It supports uni-directional, bi-directional, EPP and ECP operating modes.

13.1 Connector

The parallel port is available through the standard DSUB25 connector which is part of the multifunctional Connector X1 on the front. To find the location of the parallel port, please see the Appendix E: Connector Layout chapter.

The following table shows the pin-out of the connector.

Header	Pin	Signal Name	Function	In / Out
	1	/STB	Strobe	Out
	2	PD0	Data 0	I/O
	3	PD1	Data 1	I/O
	4	PD2	Data 2	I/O
	5	PD3	Data 3	I/O
	6	PD4	Data 4	I/O
	7	PD5	Data 5	I/O
	8	PD6	Data 6	I/O
	9	PD7	Data 7	I/O
	10	/ACK	Acknowledge	In
	11	/BUSY	Busy	In
	12	PE	Paper out	In
	13	/SLCT	Select out	In
	14	/AFD	Autofeed	Out
	15	/ERR	Error	In
	16	/INIT	Init	Out
	17	/SLIN	Select in	Out
	18 - 25	GND	Signal Ground	--

Notes: (*) To protect the external power lines of peripheral devices, make sure that:
-- the wires have the right diameter to withstand the maximum available current
-- the enclosure of the peripheral device fulfils the fire-protecting requirements of IEC/EN 60950.

To find the location of the parallel port, please see the Appendix E: Connector Layout chapter.

13.2 Configuration

The parallel-port mode, I/O addresses, and IRQs are changeable from the BIOS Setup Utility. You can program the base I/O-address 378h (default), 3BCh or 278h. You can set the parallel port mode to disable, enable or AUTO (default). You can choose IRQ5 or IRQ7 as the parallel-port interrupt.

Refer to the I/O Device Configuration Submenu in the Appendix B: BIOS Operation chapter for additional information on configuration.

14 IDE-Interfaces

PCI-bus devices serve as primary and secondary IDE hosts on the EPIC/PM. The controller supports:

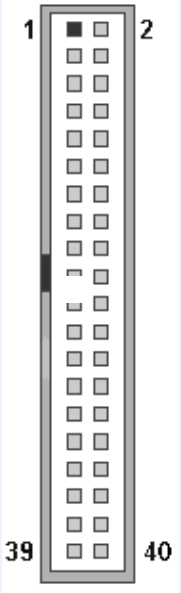
- Up to Ultra DMA 100 mode
- Up to PIO mode 4 timing
- Multiword DMA mode 1 and 2 with independent timing

The controller also supports IDE legacy and IDE native mode configuration. The EPIC/PM features one IDE interface that can drive two hard disks and one CompactFlash socket. When two IDE devices share a single adapter, they are connected in a master/slave, daisy-chain configuration. If only one drive is in the system, you must set it as the master. The CompactFlash socket is implemented through the secondary host as master.

14.1 Connector

The IDE interface is available through Connector X22 (39 pins).

This interface is designed in 0.1" grid for optimal connectivity to a 3.5" hard drive. The following table shows the pin-out of the IDE connector.

Header	Pin	Signal Name	Function
	1	/HDRST	Reset
	2	GND	Ground
	3-18	PIDE_D1..D15	Primary IDE ATA data bus
	19	GND	Ground
	21	PIDE_DRQ	Primary IDE DMA Request for IDE master
	22	GND	Ground
	23	/PIDE_IOW	Primary IDE IOWJ Command
	24	GND	Ground
	25	/PIDE_IOR	Primary IDE IORJ Command
	26	GND	Ground
	27	PIDE_RDY	Primary IDE ready
	28	PIDE_PD1	IDE1 Cable Select (470Ω to Ground)
	29	/PIDE_AK	Primary IDE DACK for IDE master
	30	GND	Ground
	31	PIDE_IRQ	IDE IRQ Primary
	32	NC	Not connected
	33	PIDE_A1	Primary IDE ATA address bus
	34	PIDE_ATAD	UDMA detection
	35	PIDE_A0	Primary IDE ATA address bus
	36	PIDE_A2	Primary IDE ATA address bus
	37	/PIDE_CS1	IDE chipselect 1 for primary channel 0
	38	/PIDE_CS3	IDE chipselect 2 for primary channel 1
	39	PIDE_ACT	Drive Activity
	40	GND	Ground

To find the location of IDE interface, please see the Appendix E: Connector Layout chapter.

14.2 CompactFlash Socket

The CompactFlash socket X13 for commercial CompactFlashes (Type I) is integrated on the bottom side of the EPIC/PM board.

Because the signals of the socket are connected to the secondary IDE, the socket is not a hot-plug capable interface. Turn off power to the system before adding or removing a CompactFlash card.

The following table shows the pin-out of the CompactFlash socket.

Pin	Signal Name	Function	Pin	Signal Name	Function
1	GND	Ground	2	D3	Data 3
3	D4	Data 4	4	D5	Data 5
5	D6	Data 6	6	D7	Data 7
7	CS1#	Chip select 1	8	GND	Ground
9	GND	Ground	10	GND	Ground
11	GND	Ground	12	GND	Ground
13	VCC	+5V	14	GND	Ground
15	GND	Ground	16	GND	Ground
17	GND	Ground	18	SA2	Addr. 2
19	SA1	Addr. 1	20	SA0	Addr. 0
21	D0	Data 0	22	D1	Data 1
23	D2	Data 2	24	NC	Not connected
25	GND	Ground	26	GND	Ground
27	D11	Data 11	28	D12	Data 12
29	D13	Data 13	30	D14	Data 14
31	D15	Data 15	32	CS3#	Chip select 3
33	GND	Ground	34	IOR#	I/O read
35	IOW#	I/O write	36	VCC	+5V
37	IRQ	Interrupt	38	VCC	+5V
39	GND	Ground	40	NC	Not connected
41	RESET#	Reset	42	IOCHRDY	Ready
43	DRQ#	DMA Request	44	DACK#	DMA Ack
45	SIDE_ACT	Drive Activity	46	NC	Not connected
47	D8	Data 8	48	D9	Data 9
49	D10	Data 10	50	GND	Ground

To find the location of the socket, please see the Appendix E: Connector Layout chapter.

14.3 Configuration

The IDE interfaces offer several configuration settings. Refer to the Main Menu, the ACPI Control submenu, the I/O Device Configuration Submenu and the Master or Slave Submenu in the Appendix B: BIOS Operation chapter for additional information on configuration.

Notes: *1. Use an UDMA flat-ribbon cable (80 lines) to drive UDMA66 or UDMA100 devices*
2. When using a standard ribbon cable (40 lines) with UDMA66 or UDMA100 devices, you have to disable the Ultra DMA Mode in the BIOS Setup Utility.

15 Floppy Interface

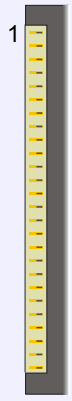
The floppy-drive interface of the EPIC/PM uses a 2.88MB super I/O floppy-disk controller and can support one floppy disk drive with densities that range from 360kB to 2.88MB.

15.1 Connector

The floppy disk interface is available on the flat-foil connector X2 (26 pins). This type of connector is often internally used in notebooks to connect a slim-line floppy drive.

Accessories are available for this interface from Kontron. To connect a standard 3.5" floppy drive, use an adapter cable (ADA-FLOPPY-2, Part Number 96001-0000-00-0). If you have a slim-line 3.5" floppy drive, you may need a flat foil cable (KAB-FLOPPY/MOPS-1, Part Number 96019-0000-00-0). It also is possible to get a slim line 3.5" floppy drive with cable from Kontron (FLOPPY-MOPS-1, Part Number 96010-0000-00-0).

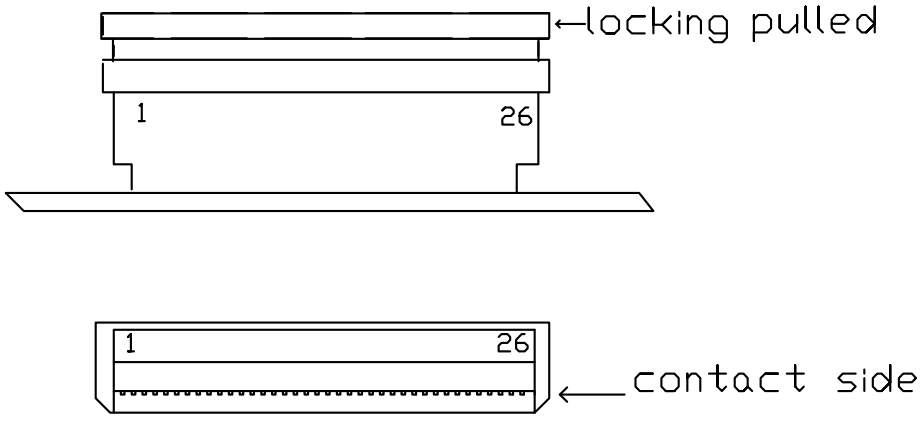
The following table shows the connector pin-out.

Header	Pin	Signal Name	Function	Pin	Signal Name	Function
	1	VCC *	+5V	2	/IDX	Index
	3	VCC *	+5V	4	/DR0	Drive Select 0
	5	VCC *	+5V	6	/DSKCHG	Disk Change
	7	NC	Not connected	8	NC	Not connected
	9	NC	Not connected	10	/MTR0	Motor on 0
	11	NC	Not connected	12	/FDIR	Direction Select
	13	NC	Not connected	14	/STEP	Step
	15	GND	Ground	16	/WDATA	Write Data
	17	GND	Ground	18	/WGATE	Write Gate
	19	GND	Ground	20	/TRK0	Track 00
	21	GND	Ground	22	/WRTPRT	Write Protect
	23	GND	Ground	24	/RDATA	Read Data
	25	GND	Ground	26	/HDSEL	Side One Select

To find the location of floppy-drive interface on the EPIC/PM board, please see the Appendix E: Connector Layout chapter.

Notes: (*) To protect the external power lines of peripheral devices, make sure that:
-- the wires have the right diameter to withstand the maximum available current
-- the enclosure of the peripheral device fulfils the fire-protecting requirements of IEC/EN 60950.

15.1.1 Connector Diagram



15.2 Configuration

You can configure the floppy disk interface in the BIOS Setup Utility. You can choose the 3.5" (common) or 5.25" drive types with densities of 360kB, 720kB, 1.2MB, 1.25MB, 1.44MB or 2.88MB. Refer to the Main Menu section of the Appendix B: BIOS Operation chapter for more information on configuring the floppy drive.

You also can disable the floppy-disk interface in the I/O Device Configuration Submenu.

16 Sound Interface

The EPIC/PM uses a Realtek ALC650 sound codec. The ALC650 is an 18-bit, full duplex AC'97 2.2 compatible stereo audio CODEC designed for PC multimedia systems, including host/soft audio and AMR/CNR based designs. The ALC650 incorporates proprietary converter technology to achieve a high SNR, greater than 90 dB.

All major operating systems support the interface.

The ALC650 features:

- High-performance CODEC with high S/N ratio (>90 dB)
- 18-bit ADC and 20-bit DAC resolution
- Compliant with AC'97 2.2 Specifications
- 18-bit stereo full-duplex CODEC with independent and variable sampling rate
- One analog line-level stereo input with 5-bit volume control: LINE_IN, (CD_IN is possible)
- Stereo Output with 5-bit volume control
- MIC input
- Power-management capabilities
- Embedded 50mW/20ohm OP at front LINE output
- 6 Channel output for multi-channel applications

16.1 Connectors

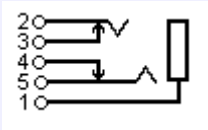
The EPIC/PM offers two connectors related to the Sound feature. One is the jack connector on the front of the board and one is an internal connector.

16.1.1 Jack Connector

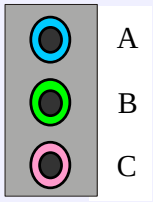
The standard 3 position jack connector (X23) complies with the standard pin-out used in many commercially available motherboards.

To find the location of the connector on the EPIC/PM board, please see the Appendix E: Connector Layout chapter. A special version of the EPIC/PM may only be equipped with a 2 position jack connector (for applications with mechanical restrictions). In this case only jacks „B" and „C" are available. The signals for Jack „A" are available on the internal connector X14.

The following table shows the general connection of each single audio jack.

Jack	Pin	Signal	Description
	1	ASGND	Analog Sound Ground
	2	XX	See Next Table
	3	NC	Not connected
	4	NC	Not connected
	5	XX	See Next Table

The individual pin-out of each jack connector is shown in the following table. (The configuration for multi-channel applications is described in Italics)

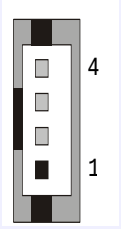
Header	Jack	Pin	Signal Name	Function
	A	2	AUXAL_C/ *REAR_L*	Line-input left. *Left Rear Speaker output for multi-channel applications*
		5	AUXAR_C/ *REAR_R*	Line-input right. *Right Front Speaker output for multi-channel applications*
	B	2	LEFT/ *FRONT_L*	Line-level stereo output left. *Left Front Speaker output for multi-channel applications*
		5	RIGHT/ *FRONT_R*	Line-level stereo output right. *Right Front Speaker output for multi-channel applications*
	C	2	MIC_C/ *CENTER*	Mono Microphone input. *Center Speaker output for multi-channel applications.*
		5	*LFE*	*Low Frequency output for multi-channel applications.*

16.1.2 Line-In/Rear Speakers Connector

Line-In or Rear Speaker signals (depending on the configuration) are always available on Connector X14. To find the location of the connector on the EPIC/PM board, please see the Appendix E: Connector Layout chapter.

If using these signals as Line-In, a CDROM can be connected using a standard CDROM Audio cable.

The pin-out of this connector complies with the standard pin-out used in many commercially available motherboards and it is shown in the following table.

Header	Pin	Signal Name	Function
	4	AUXAL_C/ *REAR_L*	Auxiliary A input left. Normally intended for connection to an internal or external CD-ROM analog output. *Left Rear Speaker output for multi channel applications*
	3	ASGND	Analog ground.
	2	AUXAR_C/ *REAR_R*	Auxiliary A input right. Normally intended for connection to an internal or external CD-ROM analog output. *Right Rear Speaker output for multi channel applications*
	1	ASGND	Analog ground.

16.2 Configuration

From the BIOS Setup Utility you can set the onboard legacy AC97 audio controller to Disabled or Enabled (default). Refer to I/O Device Configuration submenu in the Appendix B: BIOS Operation for more details.

You can download available drivers for the sound controller from the Kontron Web site or use the drivers provided by the manufacturer Realtek. Search for ALC650 drivers for the required operating system and instructions on how to enable multi-channel support.

16.3 Technical Support for Sound

If problems occur, you can solve some of them by using the latest drivers for the Sound controller. Kontron provides you with the latest tested drivers, which can differ from newer ones. For further technical support, contact either Kontron, or obtain support information and downloadable software updates from Realtek.

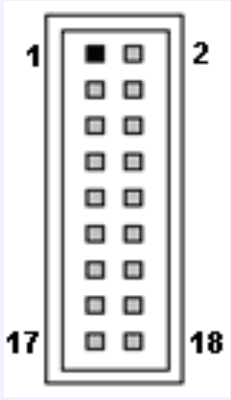
17 General Purpose I/O

The EPIC/PM Board comes with 15 General Purpose Input/Outputs (GPIOs). Each pin is individually configurable as an input or output. One pin is configurable as Interrupt output. All output pins have at least 12mA drive strength. (See the connector table in Appendix E for detailed information on each pin).

17.1 Connector

The GPIOs are available on the 2mm grid 2 row connector X11 (16 pins). To find the location of the Connector on the EPIC/PM board, please see the Appendix E: Connector Layout chapter.

The following table shows the pin-out of the connector.

GPIO	Pin	Connector Top View	Pin	GPIO
GP17*(12tu)	1		2	GND
GP16*(12tu)	3		4	GP26/INT*(12t)
GP15*(12tu)	5		6	GP25*(12tu)
GP14*(12tu)	7		8	GP24*(12tu)
GP13*(12tu)	9		10	GP23*(12tu)
GP12*(12tu)	11		12	GP22*(24td)(1)
GP11*(12tu)	13		14	GP21*(24td) (1)
GP10*(12tu)	15		16	GP20*(24td) (1)
SMB_DATA	17		18	SMB_CLK

Notes: *(12t) TTL level bi-directional pin and open-drain output with 12mA sink capability
*(12tu) TTL level bi-directional pin with internal pull up resistor and open-drain output with 12mA sink capability
*(24td) TTL level bi-directional pin with weak internal pull down resistor and 24mA source/sink capability
*(1) leave pin floating or pull low during reset. This pin must not be pulled high within 50ms after PCIRESET# signal goes inactive.
All of these signals are not galvanically isolated from the board. To ensure that the EPIC/PM Board is protected from electrical damage, implement external protection circuitry such as optocouplers at each signal.

17.2 Programming

You cannot configure the GPIOs from the BIOS Setup utility.

The GPIO controller can be accessed on I2C address 30h for write operations and 31h for read operations.

17.2.1 16-Bit Operating Systems

The 15 GPIOs are driven by the onboard Winbond W83601R controller connected to the I2C bus.

The controller's registers are accessible by the BIOS extension JIDA (JUMPtec Intelligent Device Architecture). Additional Information on how to work with JIDA for 16-Bit Operating Systems can be found on the Kontron Web site.

17.2.2 32-Bit Operating Systems

Kontron Embedded Modules GmbH offers a 32bit API (JIDA32), which also includes protected mode functions to read and write the GPIOs. This programmer's interface is available for the major 32-bit operating systems and can be downloaded from the Kontron Web site.

Detailed programming information about JIDA32 is beyond the scope of this document. Please refer to the JIDA32 documentation and the sample code, which is part of the JIDA32 package on the Kontron Web site.

17.2.3 Register Description:

Here is a brief overview of the controller's register set.

Index	R/W	Default	Register Description
00	R	-	GP Port 1: Input Port Data Register
01	R/W	00	GP Port 1: Output Port Data Register
02	R/W	F0	GP Port 1: Polarity Inversion Register
03	R/W	FF	GP Port 1: Input/Output Configuration Register
04	R/W	00	GP Port 1: Output style control Register
05	R	-	GP Port 1: Input Latched Data Register
08	R	-	GP Port 2: Input Port Data Register
09	R/W	00	GP Port 2: Output Port Data Register
0A	R/W	70	GP Port 2: Polarity Inversion Register
0B	R/W	7F	GP Port 2: Input/Output Configuration Register
0C	R/W	00	GP Port 2: Output style control Register
0D	R	-	GP Port 2: Input Latched Data Register
11	R	00	GP Port 2: Interrupt Status Register
13	R/W	00	GP Port 2: Interrupt Enable Register
14	R/W	00	Mode Configuration Register

CR00 - GP Port 1: Input Port Data Register

Bit 7 ... 0 → Pins GP17 ... GP10

This register is a data port for input only. It reflects the incoming logic levels of the pins whether the pins are defined as an input mode by CR03. It will be inverted data by CR02.

CR01 - GP Port 1: Output Port Data Register

Bit 7 ... 0 → Pins GP17 ... GP10

This register is a data port for output only. It reflects the outgoing logic levels of the pins whether the pins are defined as an output mode by CR03. This register will reflect the value of output Flip-flop while read access. The output data will be inverted or changed output style by CR02 or CR04.

CR02 - GP Port 1: Polarity Inversion Register

Bit 7 ... 0 → Pins GP17 ... GP10

This register enables polarity inversion of pins defined as input or output by CR03.

When set to a "1", the incoming/outgoing port value is inverted.

When set to a "0", the incoming/outgoing port value is the same as in data register.

CR03 - GP Port 1: Input/Output Configuration Register

Bit 7 ... 0 → Pins GP17 ... GP10

This register selects Input or Output mode of pins.

When set to a "1", respective GPIO port is programmed as an input port.

When set to a "0", respective GPIO port is programmed as an output port.

CR04 - GP Port 1: Output style control Register

Bit 7 ... 0 → Pins GP17 ... GP10

When set to a "1", respective GPIO port is programmed as a pulse signal.

When set to a "0", respective GPIO port is programmed as a level signal.

CR05 - GP Port 1: Input Latched Data Register

Bit 7 ... 0 → Pins GP17 ... GP10

This register will latch Port 1 data while power on or RST# pin low, which is controlled by CR14h bit 0.

CR08 - GP Port 2: Input Port Data Register

Bit 6 ... 0 → Pins GP26 ... GP20

Bit 7 → Reserved

This register is a data port for input only. It reflects the incoming logic levels of the pins whether the pins are defined as an input mode by CR0B. It will be inverted data by CR0A.

CR09 - GP Port 2: Output Port Data Register

Bit 6 ... 0 → Pins GP26 ... GP20

Bit 7 → Reserved

This register is a data port for output only. It reflects the outgoing logic levels of the pins whether the pins are defined as an output mode by CR0B. This register will reflect the value of output Flip-flop while read access. The output data will be inverted or changed output style by CR0A or CR0C.

CR0A - GP Port 2: Polarity Inversion Register

Bit 6 ... 0 → Pins GP26 ... GP20

Bit 7 → Reserved

This register enables polarity inversion of pins defined as input or output by CR0B.

When set to a "1", the incoming/outgoing port value is inverted.

When set to a "0", the incoming/outgoing port value is the same as in data register.

CR0B - GP Port 2: Input/Output Configuration Register

Bit 6 ... 0 → Pins GP26 ... GP20

Bit 7 → Reserved

This register selects Input or Output mode of pins.

When set to a "1", respective GPIO port is programmed as an input port.

When set to a "0", respective GPIO port is programmed as an output port.

CR0C - GP Port 2: Output style control Register

Bit 6 ... 0 → Pins GP26 ... GP20

Bit 7 → Reserved

When set to a "1", respective GPIO port is programmed as a pulse signal.

When set to a "0", respective GPIO port is programmed as a level signal.

CR0D - GP Port 2: Input Latched Data Register

Bit 6 ... 0 → Pins GP26 ... GP20

Bit 7 → Reserved

This register will latch Port 1 data while power on or RST# pin low, which is controlled by CR14h bit 0.

Bit 2...0 reflect the I2C bus address bits A2...A0.

CR11 - GP Port 2: Interrupt Status Register

Bit 6 ... 0 → 1 if a transition occurs at pin GP26 ... GP20.

Bit 7 → Reserved

If GP26/INT is selected as interrupt function, bit 6 of this register will always be 0.

A read to this register will clear this register.

CR13 - GP Port 2: Interrupt Enable Register

Bit 5 ... 0 → 0 to disable GP26-GP20 interrupt output when interrupt function is selected.

Bit 7 ... 6 → Reserved

CR14 - GP Port 2: Mode Configuration Register

Bit 7 → 1, Set GP/INT pin as INT function. 0, set GP/INT pin as GP function.

Bit 6 → 1, Set INT function at GP26(pin 12). 0, Set INT function at GP17(pin 18).

Bit 5 → 1, Set INT output pin as pulse mode. 0, set INT output pin as level mode.

Bit 4 → 1, Set INT out pin polarity is 1 (normal high). 0, set INT out pin polarity is 0 (normal low).

Bit 3 → 1, Port 2 (CR09h-CR0Ch,CR11h,CR13h) registers can be reset to default data during PCIRESET#. 0, Port 2 (CR09h-CR0Ch) can not be reset during PCIRESET#.

Bit 2 → 1, Port 1 (CR01h-CR04h,CR10h,CR12h) registers can be reset to default data during PCIRESET#. 0, Port 1 (CR01h-CR04h) can not be reset during PCIRESET#.

Bit 1 → 1, Port 2 CR0Dh can be latched not only by PCIRESET# but also power-on period. 0, Port 2 CR0Dh can only be latched by power-on period.

Bit 0 → 1, Port 1 CR05h can be latched not only by PCIRESET# but also power-on period.

0, Port 1 CR05h can only be latched by power-on period.

17.2.4 Output Waveforms

Depending on the register settings following output waveforms are possible on the GPIO pins.

GPO Output Style	Polarity	Output Port Register	Output Value at Pin	Wave
Level	0	0	0	
		1	1	
	1	0	1	
		1	0	
Pulse	0	write 1	Active	
	1	write 1	Active	

INT Output Mode	Polarity	Output	Wave
Level	0(normal low)	1	
	1(normal high)	0	
Pulse	0(normal low)	High Pulse	
	1(normal high)	Low Pulse	

17.3 SMBus Interface

Pins 17 (SMB_DATA) and 18 (SMB_CLK) represent the SMBus interface of the System.

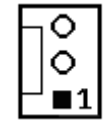
Use these pins to communicate with the Smart Battery module if connected. Otherwise these pins must be left unconnected.

18 Fan Interface

The EPIC/PM is normally shipped with a CPU fan. If for any reason no CPU fan is mounted or a different fan has to be used, use this interface to connect a fan to cool the CPU. The connector and onboard system controller support the speed monitoring of the fan. This connector supports 5V fans, only. A second fan is supported by the EPIC/PM which is intended for chassis cooling. For this 12V fan speed monitoring is also supported.

18.1 CPU Fan Connector

The CPU fan interface is available on connector X24 (3 pins).

Header	Pin	Signal Description	Function
	1	Sense	Speed Monitoring
	2	VCC *	+5V
	3	GND	Ground

Notes: (*) To protect the external power lines of peripheral devices, make sure that:
-- the wires have the right diameter to withstand the maximum available current
-- the enclosure of the peripheral device fulfils the fire-protecting requirements of IEC/EN 60950.

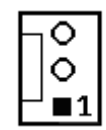
For the location of the CPU fan connector see Appendix E: Connector Layout.

18.2 CPU Fan Configuration

You can set the active trip point to a value from 40°C up to 100°C in the ACPI Control submenu of the BIOS Setup Utility. The fan will automatically turn on whenever this trip point temperature value is reached. Setting this item to disabled means the fan will always run, except when the operating system takes control over it.

18.3 Chassis Fan Connector

The Chassis fan interface is available on connector X28 (3 pins).

Header	Pin	Signal Description	Function
	1	Sense	Speed Monitoring
	2	VCC *	+12V
	3	GND	Ground

Notes: (*) To protect the external power lines of peripheral devices, make sure that:
-- the wires have the right diameter to withstand the maximum available current
-- the enclosure of the peripheral device fulfils the fire-protecting requirements of IEC/EN 60950.

For the location of the Chassis fan connector see Appendix E: Connector Layout.

18.4 Chassis Fan Configuration

You can set the active trip point to a value from 40°C up to 100°C in the ACPI Control submenu of the BIOS Setup Utility. The fan will automatically turn on whenever this trip point temperature value is reached. The temperature measured can be either the CPU temperature or the system temperature which is measured within the SCH3114 controller. Setting this item to disabled means the fan will always run, except when the operating system takes control over it.

19 Power Interface

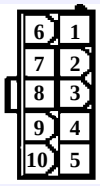
19.1 Power Interface Connectors

19.1.1 ATX Connector Version

This power connector is available through Connector X7 (10 pins). To find the location of this connector see Appendix E: Connector Layout.

The EPIC/PM requires +5V and +5V Standby. The +3.3V for the EPIC/PM's circuitry is generated onboard. The onboard generated +3.3V is not connected to the PC/104-Plus bus. The +3.3V pin of the ATX connector is connected to the PC/104-Plus bus and provides power up to 6A for PC/104-Plus extension modules.

Additionally, some peripherals such as LCD panel backlight inverters, disk drives, and PC/104 as well as PC/104-Plus add-on cards may need more voltages (+12V, -12V, +3.3V). These voltages are not generated onboard the EPIC/PM and need to be supplied, too, as soon as peripheral devices require these voltages. We recommend that you use an ATX power supply with this type of EPIC/PM, even though not all voltages are required. An adapter cable to connect a standard ATX power supply to this connector is available from Kontron (KAB-ATX-20TO10, Part Number 96072-0000-00-0). The following table shows the pin-out of the ATX connector.

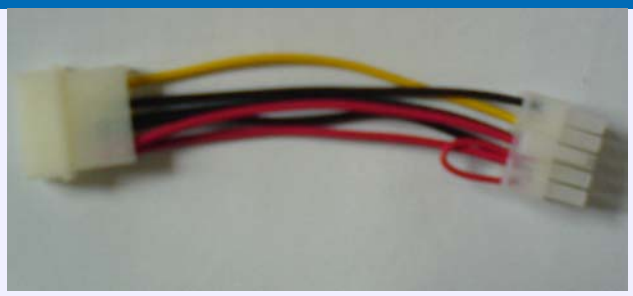
Header	Pin	Signal Name	Function	Pin	Signal Name	Function
	1	PS_ON (**)	Power On	6	+5V_SB (*)	5V Standby
	2	GND	Ground	7	+5V (*)	+5V
	3	GND	Ground	8	+5V (*)	+5V
	4	+12V (*)	+12V	9	-12V (*)	-12V
	5	+3.3V (*)	+3.3V external (PC/104-Plus)	10	GND	Ground

Notes: (*) To protect the external power lines of peripheral devices, make sure that:
-- the wires have the right diameter to withstand the maximum available current
-- the enclosure of the peripheral device fulfils the fire-protecting requirements of IEC/EN 60950.
The current on these pins is limited to 6A/pin.

To find the location of this connector see Appendix E: Connector Layout.

19.1.2 AT Connector Version

By using a cable adapter **KAB-5V-ATX10** a 4 pin AT power connector can be adapted.



X1 Pin	X2 Pin	Signal name	Cable color
1	4	+12V	Yellow
2	2	COM	Black
2	3	COM	Black
3	10	COM	Black
4	8	+5V	Red
4	7	+5V	Red
4	6	+5VSB	Purple

The following table shows the pin-out of the AT connector.

Header	Pin	Signal Description	Function
	1	V5S *	+5V
	2	GND	Ground
	3	GND	Ground
	4	VCC12 *	+12V

Notes: (*) To protect the external power lines of peripheral devices, make sure that:
-- the wires have the right diameter to withstand the maximum available current
-- the enclosure of the peripheral device fulfils the fire-protecting requirements of IEC/EN 60950.
The current of the pins on this connector is limited to 13A/pin.

19.1.3 Configuration

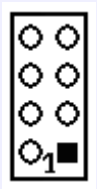
The EPIC/PM comes with a power-management system that supports APM 1.2 and ACPI 2.0 features. You can configure lots of options for power-saving states such as standby state with partial power reduction and suspend state with full-power reduction. Please refer to the Power menu section in the Appendix B: BIOS Operation chapter for more information on saving power.

19.2 ATX/Reset/2LED Interface

This interface on the EPIC/PM is an 8-pin female (Connector X6). For the location of this connector see Appendix E: Connector Layout. The interface's functions include:

- Power Button
- Reset Button
- Hard Disk LED
- CompactFlash LED

The following table shows the pin-out of the connector.

Header	Pin	Signal Description	Function
	1	HDLED *	Hard Disk LED (cathode)
	2	CFLED *	CompactFlash LED (cathode)
	3	VCC	+5V (anode)
	4	VCC	+5V (anode)
	5	/RESIN	Reset Input (low active)
	6	GND	Ground
	7	/PWRBTN	Power Button (low active)
	8	GND	Ground

Notes: (*) This signal has an onboard 470 Ohm resistor. Directly connect the cathode of the LED to HDLED/CFLED and the anode to VCC.

19.2.1 Configuration

The function of the power button can be set to either “power off” or “sleep” mode from the BIOS set-up utility. When set to “power off” the power button offers an On/Off function and when set to “Sleep” it offers a Sleep/Wake function. Please refer to the Power menu section in the Appendix B: BIOS Operation chapter for more information about power savings.

20 Watchdog Timer

The watchdog timer is integrated in the onboard SMSC SCH3114 controller of the EPIC/PM and can issue a reset to the system or generate a non-maskable interrupt (NMI). The watchdog timer circuit has to be triggered within a specified time by the application software. If the watchdog is not triggered because proper software execution fails or a hardware malfunction occurs, it will reset the system or generate the NMI.

20.1 Configuration

You can set the watchdog timer to disabled, reset or NMI mode. You can specify the delay time and the timeout (trigger period) from 1 second to 30 minutes. The delay time is the time after first initialization before the trigger period starts. The timeout is the time the watchdog has to be triggered within. You can make the initialization settings in the BIOS setup. Refer to the Watchdog Settings Submenu in the Appendix B: BIOS Operation chapter for information on configuration.

20.2 Programming

20.2.1 Initialization

You can initialize the watchdog timer from the BIOS setup. You also can set up the initialization from the application software with help of the JIDA (Jumptec Intelligent Device Architecture) programmer's interface.

20.2.2 Trigger

The watchdog needs to be triggered out of the application software within a specified timeout period. You can only do this in the application software with help of the JIDA programmer's interface.

For information about the JIDA programmer's interface refer to the JIDA BIOS extension section in the Appendix B: BIOS Operation and separate documents available in the JIDA software packages on the Kontron Web site.

21 Hardware Monitor

The SMSC SCH3114 controller monitors several critical hardware parameters of the system, including power-supply voltages, fan speed and CPU temperature, which are very important for a high-end computer system to remain stable and properly. This controller is connected via the system management (SM) bus to the south bridge.

The following parameters are monitored:

- +3.3V from onboard DC/DC
- CPU core voltage
- +5V standby voltage
- Battery voltage
- CPU temperature with on-die diode
- CPU fan speed
- Chassis fan speed

21.1 Configuration

You can use the Hardware Monitor submenu in the BIOS Setup Utility to obtain information on voltages, fan speed and to check the temperature of the CPU die. For more information on this submenu, see the Appendix B: BIOS Operation chapter in this manual.

To monitor the parameters of this feature from your operating system, Kontron recommends that you use the 32-bit protected mode JUMPtec's Intelligent Device Architecture 32-bit driver (JIDA 32) with the test and demo application for Windows 95/98/ME/NT/2000/XP, which is available on the Kontron Web site.

22 Important Technology Information

The following technological information is designed to give you a better understanding of some of the features offered by the EPIC/PM. This information can be referenced when reading the Appendix A: System Resource Allocations and Appendix B: BIOS Operation sections that follow. There also are references to additional documentation that will help you develop a better understanding of the technical information. They are listed in the Appendix F: PC-Architecture Information.

22.1 Max CPU Frequency setting

Kontron Embedded Modules currently offers four variants of the EPIC/PM. They are the 600MHz, 800Mhz and 1000MHz Celeron®-M versions and a 1800MHz Pentium® M version. Additional processor support is planned. These variants use a smart BIOS with the capability of identifying the CPU that the module is equipped with. Another feature of the BIOS is its ability to offer the user the option to set the maximum CPU frequency based on the Intel® SpeedStep® technology.

Notes: Celeron® M processors do not support this feature.

The different Max CPU frequency settings available for the different modules are as follows:

- 600MHz: 600MHz
- 800MHz: 800MHz
- 1000MHz: 1000MHz
- 1800MHz: 600, 800, 1000, 1200, 1400, 1600, 1800MHz (def)

Notes: Selecting frequencies higher then the default may cause the system to reach "Critical Trip Point" and shutdown if a proper cooling solution is not used. Always ensure that you use a proper cooling when selecting higher frequency settings.

Refer to the Power Menu section in the Appendix B: BIOS Operation chapter of this manual for more information.

22.2 Thermal Monitor and Catastrophic Thermal Protection

22.2.1 Thermal Monitor

The Thermal Monitor within the Pentium M processor helps to control the processor temperature by activating the TCC (Thermal Control Circuit) when the processor silicon reaches its maximum operating temperature. The temperature at which the Intel Thermal Monitor activates the TCC is not user-configurable and is not software visible.

The Thermal Monitor controls the processor temperature by modulating (starting and stopping) the CPU core clocks at a 50% duty cycle (TM1) or by initiating an Enhanced Intel SpeedStep® technology

transition (TM2*) when the processor silicon reaches its maximum operating temperature. The mode is selectable in the BIOS Setup Utility.

➤ Maximum operating temperature activating TCC: 100°C

Notes:(*) TM2 is the recommended mode for the Intel Pentium M processor.
TM2 is not supported on boards with Celeron® M processor.

Thermal Monitor supports two modes to activate the TCC: Automatic and On-Demand mode. The Intel Thermal Monitor Automatic Mode must be enabled via BIOS for the processor to be operating within specification. Automatic mode does not require any additional hardware, software drivers, or interrupt handling routines.

22.2.2 Catastrophic Thermal Protection

The Intel Pentium M processor supports the THERMTRIP# signal for catastrophic thermal protection.

In the event of a catastrophic cooling failure, the processor will automatically shut down when the silicon has reached the absolute maximum temperature. At this point the system BUS signal THERMTRIP# will go active. THERMTRIP# activation is independent of processor activity and does not generate any bus cycles. The system will immediately shut down.

➤ Absolute maximum temperature activating THERMTRIP#: 125°C

For more details, see Chapter 5.1.2 of the Intel Pentium M Processor Datasheet.

22.3 Processor Performance Control

The Pentium M processor can run in different performance states (multiple frequency/voltage operating points). The CPU performance can be altered while the computer is functioning. This allows the processor to run at different core frequencies and voltages depending on CPU thermal state and OS policy.

Microsoft Windows XP includes built-in processor performance control to operate the processor more efficiently when it is not fully utilized. Win2k, WinME and Win9x do not support processor performance control. Special software is required for Operating Systems that are not capable of processor performance control.

In Windows, the processor performance control policy is linked to the Power Scheme setting in the control panel power option applet.

Notes: Windows always runs at the highest performance state when the "Home/Office" or the "Always On" power scheme is selected. For more detailed information about processor performance control, see:
- Chapter 8 of the ACPI Specification Revision 2.0c
- Windows platform design notes

22.4 Thermal Management

ACPI allows the OS to play a role in the thermal management of the system. With the OS in control of the operating environment, cooling decisions can be made based on the application load on the CPU and the thermal heuristics of the system.

The ACPI thermal solution on EPIC/PM supports three cooling policies and their trip points:

Active Trip Point

Active cooling devices typically consume power and produce noise but are able to cool a thermal zone without limiting system performance. The active cooling trip point declares the temperature threshold OS uses to start/stop active cooling devices (fan).

Passive Cooling Trip Point

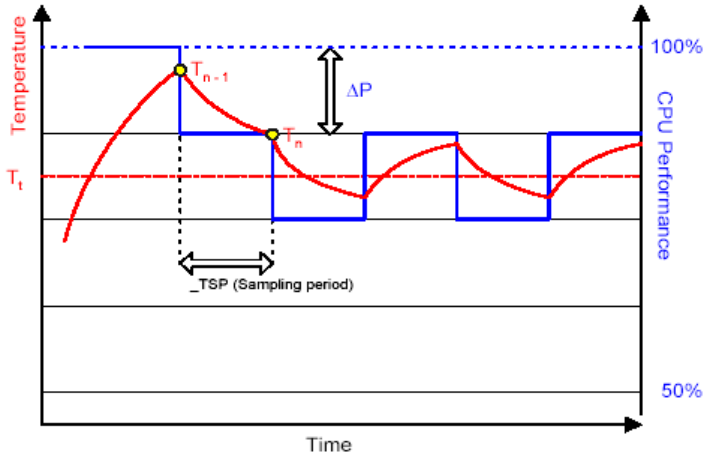
Passive cooling devices produce no noise, but may not be effective enough to cool the thermal zone. The passive cooling trip point declares the temperature threshold in which the OS will start or stop passive cooling. In this case it throttles the processor.

Critical Trip Point

The OS performs an orderly, but critical, shutdown of the system when the temperature reaches the critical trip point.

22.4.1 Processor Clock Throttling

The ACPI OS assesses the optimum CPU performance change necessary to lower the temperature using the following equation:



$$\Delta P[\%] = TC1(Tn-Tn-1) + TC2(Tn-Tt)$$

ΔP is the performance delta, Tt is the target temperature = critical trip point. The two coefficients TC1 and TC2 and the sampling period TSP are hardware dependent constants that you must supply. (See the setup options in the ACPI Control Submenu section in the BIOS Operation chapter).

It is up to you to set the cooling preference of the system by setting the appropriate trip points in the BIOS setup.

Notes: For more detailed information see Chapter 12 of the ACPI Specification.

22.5 I/O APIC vs. 8259 PIC Interrupt mode

The I/O APIC (Advanced Programmable Interrupt Controller) handles interrupts differently than the 8259 PIC. Enable the I/O APIC mode in the BIOS Setup Utility, if your operating system supports it.

The following information explains these differences to the standard 8259 PIC mode:

Method of interrupts transmission

The I/O APIC transmits interrupts through the system bus and interrupts are handled without the needs for the processor to run an interrupt acknowledge cycle.

Interrupt priority

The priority of interrupts in the I/O APIC is independent of the interrupt number.

More interrupts

The I/O APIC in the chipset of the EPIC/PM supports a total of 24 interrupts.

Notes: The APIC is not supported by all operating systems. Only Windows XP supports APIC.
The APIC mode must be enabled in the BIOS setup before the OS installation.
APIC only works in ACPI mode.
For more detailed information about APIC, see Chapter 8 of the IA-32 Intel Architecture Software Developer's Manual, Volume 3.

22.6 Native vs. compatible IDE mode

22.6.1 Compatible IDE Mode

The ATA controller emulates a legacy IDE controller, which is a non-standard extension of the ISA-based IDE controller. In compatible mode, the controller requires two ISA IRQs (14 and 15) that cannot be shared with other devices.

22.6.2 Native Mode

The ATA controller acts as a true PCI device that does not require dedicated legacy resources and can be configured anywhere in the system. ATA controllers running in native mode use their PCI interrupt for both channels and can share this interrupt pin with other devices in the system, like any other PCI device.

By requiring only one shareable interrupt instead of two non-shareable ones, native-mode controllers significantly decrease the likelihood that a user will install a device that cannot work because no interrupts are available.

Enable Native IDE Support in the BIOS Setup Utility if your OS supports this mode.

Notes: The Native Mode is not supported by all operating systems.
The Native mode must be enabled in the BIOS setup before the OS installation.
Native Mode only works in ACPI mode.
For more information see: Microsoft Windows platform design notes about Native-mode ATA.

22.6.3 Native Mode Configuration

Windows XP SP1 and Windows Server 2003 will switch a native-mode-capable ATA controller from compatible to native mode if the BIOS indicates that the controller can be switched, the controller supports native mode and the appropriate registry entry is set.

You must add a DWORD VALUE called EnableNativeModeATA under

HKEY_LOCAL_MACHINE/System/CurrentControlSet/Control/PnP/PCI/

and set 1 as the value.

23 Appendix A: System-Resource Allocation

23.1 Interrupt Request (IRQ) Lines

In 8259 PIC mode (I/O APIC mode is disabled)

IRQ #	Use	Available	Comment
0	Timer0	No	
1	Keyboard	No	
2	Slave 8259	No	
3	COM2	No	Note (1)
4	COM1	No	Note (1)
5	Sound	No	Note (1), Note (2)
6	FDC	No	Note (1)
7	LPT1	No	Note (1)
8	RTC	No	
9	SCI	Yes	Note (3)
10	COM4	No	Note (1)
11	COM3	No	Note (1)
12	PS/2 Mouse	No	Note (1)
13	FPU	No	
14	IDE0	No	Note (1)
15	CompactFlash IDE1	No	Note (1)

Notes: *(1)* *If the „used for"-device is disabled in setup, the corresponding interrupt is available for other devices.*

(2) *Possible setting for LPT1. IRQ7 is the default setting.*

(3) *Available in default configuration. IRQ 9 is used as SCI, if ACPI is enabled.*

In I/O APIC mode

IRQ #	Use	Available	Comment
0	Timer0	No	
1	Keyboard	No	
2	Slave 8259	No	
3	COM2	No	Note (1)
4	COM1	No	Note (1)
5	Sound	No	Note (1), Note (2)
6	FDC	No	Note (1)
7	LPT1	No	Note (1)
8	RTC	No	
9	SCI	Yes	Note (3)
10	COM4	No	Note (1)
11	COM3	No	Note (1)
12	PS/2 Mouse	No	Note (1)
13	FPU	No	
14	IDE0	No	Note (1), Note (5)
15	CompactFlash IDE1	No	Note (1), Note (5)
16	PIRQ[A]	For PCI	
17	PIRQ[B]	For PCI	
18	PIRQ[C]	For PCI	
19	PIRQ[D]	For PCI	
20	PIRQ[E]	No	
21	PIRQ[F]	No	
22	PIRQ[G]	No	
23	PIRQ[H]	No	

Notes: (1) If the „used for"-device is disabled in setup, the corresponding interrupt is available for other devices.
(2) Possible setting for LPT1. IRQ7 is the default setting.
(3) Available in default configuration. IRQ 9 is used as SCI, if ACPI is enabled.
(5) Available if IDE controller is in Native Mode.

23.2 Direct Memory Access (DMA) Channels

DMA #	Use	Available	Comment
0		Yes	
1	Sound	No	Note (1), (2)
2	FDC	No	Note (1)
3		Yes	Note (2)
4	Cascade	No	
5		Yes	
6		Yes	
7		Yes	

Notes: (1) If the „used for"-device is disabled in setup, the corresponding DMA channel is available for other devices.
(2) Possible setting for LPT1 if configured for ECP mode.

23.3 Memory Map

The EPIC/PM processor modules can support up to 2048MB of memory. The first 640KB of DDR-SDRAM are used as main memory.

Using DOS, you can address 1MB of memory directly. Memory area above 1MB (high memory, extended memory) is accessed under DOS via special drivers such as HIMEM.SYS and EMM386.EXE, which are part of the operating system. Please refer to the operating system documentation or special textbooks for information about HIMEM.SYS and EMM386.EXE.

Other operating systems (Linux or Windows versions) allow you to address the full memory area directly.

Upper Memory	Use	Available	Comment
A0000h – BFFFFh	VGA Memory	No	Mainly used by graphic adapter cards. If a PCI graphic card is in the system this memory area is mapped to the PCI bus.
C0000h – CFFFFh	VGA BIOS, RPL/PXE ROM	No	
D0000h – DFFFFh		Yes	Free for LPC bus or shadow RAM in standard configurations. If JRC software is used, a 16K block is shadowed for BIOS extension, starting with first free area at D0000h, D4000h, D8000hor DC000h. (BIOS extensions do not use the whole shadow block.).
E0000h – F0000h	System BIOS, USB legacy support	No	

23.3.1 Using Expanded Memory Managers

EPIC/PM extension BIOSes may be mapped to an upper memory area. (See the previous table). Some add-on boards also have optional ROMs or use drivers that communicate with their corresponding devices via memory mapped I/O such as dual-ported RAM. These boards have to share the upper memory area with the Expanded Memory Manager's EMS frame. This often causes several problems in the system.

Most EMMs scan the upper memory area for extension BIOSes (optional ROMs) and choose a free memory area for their frame if it is not explicitly set. Normally, they are not always capable of detecting special memory-mapped I/O areas. You need to tell the EMM which memory areas are not available for the EMS frames, which is most of the time done by using special exclusion parameters.

If the Expanded Memory Manager you use cannot detect extension BIOSes (optional ROMs), make sure you excluded all areas in the upper memory, which are used by extension BIOSes, too. Your instruction in the CONFIG.SYS concerning the Expanded Memory Manager should look like this: (question marks symbolize the location of extension BIOS).

MS-DOS Example

```
DEVICE=EMM386.EXE X=????-???? X=E000-FFFF
```

Note: When booting up your system using this configuration under MS-DOS, the exclusion of area F000 to FFFF causes a warning. Microsoft reports that this message will always appear when the F000 segment lies in the shadow RAM. This is a bug of EMM386, not of the EPIC/PM.

Please read the technical manuals of add-on cards used with the EPIC/PM for the memory areas they use. If necessary, exclude their memory locations to avoid a conflict with EMM386.

23.4 I/O Address Map

The I/O-port addresses of the EPIC/PM are functionally identical with a standard PC/AT. All addresses not mentioned in this table should be available. We recommend that you do not use I/O addresses below 0110hex with additional hardware for compatibility reasons, even if available.

Address (h)	Use	Available	Comment
0000 – 001F	DMA Controller 1	No	Fixed
0020 – 003D	Interrupt Controller 1	No	Fixed
0040 – 0053	Timer, Counter	No	Fixed
0060 – 0067	Keyboard controller	No	Fixed
0070 – 0077	Real Time Clock and CMOS Registers	No	Fixed
0080 – 008F	DMA Page Register	No	Fixed
0090 – 009F	DMA Control	No	Fixed
0092	Reset Generator	No	Fixed
00A0 00BF	Interrupt Controller 2	No	Fixed
00C0 – 00DF	DMA Controller 2	No	Fixed
00F0	Math. Coprocessor	No	Fixed
0100 – 010F	General Purpose I/O	No	Kontron Control Port, Fixed
0170 – 0177	Hard Disk Drive (Secondary)	No	Available if IDE port 2 is disabled or in native IDE mode
01F0 – 01F7	Hard Disk Drive (Primary)	No	Available if IDE port 1 is disabled or in native IDE mode
0220 – 0227	COM3	Yes	Possible address for COM
0228 – 022F	COM4	Yes	Possible address for COM
0274 – 0277	ISA PNP Data	No	Fixed
0278 – 027F	LPT	Yes	Possible address for LPT
02F8 – 02FF	COM2	Yes	Possible address for COM
0330 – 0331			
0376	IDE Controller	No	Available if IDE port 2 is disabled or in native IDE mode
0378 – 037F	LPT	No	Available if LPT is disabled
03BC – 03C3	LPT	Yes	Possible address for LPT
03B0 – 03DF	Graphic Subsystem	No	Fixed
03F6	IDE Controller	No	Available if IDE port 2 is disabled or in native IDE mode
03F0 – 03F7	Floppy Controller	No	Available if floppy controller is disabled
03F8 – 03FF	COM1	No	Available if COM is disabled
0400 – 047F	SIO Runtime Regs	No	Fixed
04D0 – 04D1	Interrupt Select	No	Fixed
0CF8 – 0CFF	PCI Configuration	No	Fixed
1000 – 107F	System Resources	No	Fixed
1180 – 11BF	System Resources	No	Fixed
1454	System Resources	No	Fixed
14D4	System Resources	No	Fixed
1500 – 157F	System Resources	No	Fixed
1800 – 1807	Graphic Subsystem	No	Fixed
1C00 – 1C1F	USB Host Controller 1	No	Fixed
2000 – 201F	USB Host Controller 2	No	Fixed
2400 – 240F	Ultra ATA Storage Controller	No	Fixed
2800 – 281F	SM-Bus Controller	No	Fixed
4000 – 403F	Ethernet Controller 2	No	Set at runtime
4400 – 443F	Ethernet Controller 1	No	Set at runtime

23.5 Peripheral Component Interconnect (PCI) Devices

All devices follow the PCI 2.1 specification. The BIOS and OS control memory and I/O resources. Please refer to the PCI 2.1 specification for details.

PCI Device (IDSEL)	PCI IRQ	REQ/ GNT	Comment
AGP Graphic	-	-	Separate Bus, integrated in Intel chipset
Ethernet (AD24)	INTE#	Discrete channel	
AC97 Sound	INTB#		Separate Bus, integrated in Intel chipset
1st UHCI USB Controller	INTA#	-	Separate Bus, integrated in Intel chipset
2nd UHCI USB Controller	INTD#	-	Separate Bus, integrated in Intel chipset
EHCI USB Controller	INTH#	-	Separate Bus, integrated in Intel chipset
PCI to ISA bridge (AD18)	-	REQ#4/GNT#4	
82551ER Ethernet Controller (AD17)	INTC#	REQ#3/GNT#3	

24 Appendix B: BIOS Operation

The EPIC/PM comes with Phoenix BIOS 4.0, Release 6.1, which is located in the onboard Flash EEPROM in compressed form. The device has an 8-bit access. The shadow RAM feature offers faster access (16 bit). You can update the BIOS using a Flash utility. For complete Phoenix BIOS 4.0 information, visit the Phoenix Technologies Web site.

24.1 Determining the BIOS Version

To determine the BIOS version of the EPIC/PM, immediately press the <Pause/Break> key on your keyboard as soon as you see the following text display in the upper left corner of your screen:

PhoenixBIOS 4.0 Release 6.1
Copyright 1985-2005 Phoenix Technology Ltd.
All Rights Reserved
Kontron(R) BIOS Version <EPBAR110>
Copyright 2002-2006 Kontron Embedded Modules GmbH

Whenever you contact technical support about BIOS issues, providing a BIOS version <EPBAR???> is especially helpful.

The system BIOS provides additional information about the board's serial number, CPU, and memory information by displaying information similar to the following:

S/N: E05350002

CPU = Mobile Genuine IntelI processor 1600MHz
503M System RAM Passed
1024K Cache SRAM Passed
System BIOS shadowed
Video BIOS shadowed
UMB upper limit segment address: E4EC

The board's serial number has value to technical support. EPIC/PM serial numbers always start with E0 and are followed by six or seven digits. The first digit represents the year of manufacturing, the next two digits stand for the lot number, and the last three or four digits are the number of the board in that lot.

In the example above, the board with the serial number E05350002 was manufactured in year 2005, lot 35 of that year, and is board number 2 of that lot.

24.2 Configuring the System BIOS

The Phoenix BIOS setup utility allows you to change system behavior by modifying the BIOS configuration. Setup-utility menus allow you to make changes and turn features on or off.

BIOS setup menus represent those found in most models of the EPIC/PM. The BIOS setup utility for specific models can differ slightly.

Note: Selecting incorrect values can cause system boot failure. Load setup-default values to recover by pressing <F9>.

24.2.1 Start Phoenix BIOS Setup Utility

To start the Phoenix BIOS Setup Utility, press the <F2> key when the following string appears during boot up.

Press <F2> to enter Setup

The Main Menu then appears.

24.2.2 General Information

The Setup Screen is composed of several sections:

Setup Screen	Location	Function
Menu Bar	Top	Lists and selects all top-level menus.
Legend Bar	Bottom	Lists setup navigation keys.
Item Specific Help Window	Right	Help for selected item.
Menu Window	Left Center	Selection fields for current menu.
General Help Window	Overlay (center)	Help for selected menu.

Menu Bar

The menu bar at the top of the window lists different menus. Use the left/right arrow keys to make a selection.

Legend Bar

Use the keys listed in the legend bar on the bottom to make your selections or exit the current menu. The table below describes the legend keys and their alternates.

Key	Function
<F1> or <Alt-H>	General Help window.
<Esc>	Exit menu.
← or → Arrow key	Select a menu.
↑ or ↓ Arrow key	Select fields in current menu.
<Tab> or <Shift-Tab>	Cycle cursor up and down.
<Home> or <End>	Move cursor to top or bottom of current window.
<PgUp> or <PgDn>	Move cursor to next or previous page.
<F5> or <->	Select previous value for the current field.
<F6> or <+> or <Space>	Select next value for the current field.
<F9>	Load the default configuration values for this menu.
<F10>	Save and exit.
<Enter>	Execute command or select submenu.
<Alt-R>	Refresh screen.

Selecting an Item

Use the ↓ or ↑ key to move the cursor to the field you want. Then use the + and – keys to select a value for that field. Save Value commands in the Exit menu save the values displayed in all menus.

Displaying Submenus

Use the ← or → key to move the cursor to the submenu you want. Then press <Enter>. A pointer (►) marks all submenus.

Item Specific Help Window

The Help window on the right side of each menu displays the Help text for the selected item. It updates as you move the cursor to each field.

General Help Window

Pressing <F1> or <Alt-F1> on a menu brings up the General Help window that describes the legend keys and their alternates. Press <Esc> to exit the General Help window.

24.3 Main Menu

Feature	Option	Description
System Time	HH:MM:SS	Sets system time. Press <Enter> to move to MM or SS.
System Date	MM/DD/YYYY	Sets the system date. Press <Enter> to move to DD or YYYY.
Legacy Diskette A	360 Kb, 5 ¼ " 1.2 MB, 5 ¼ " 720 Kb, 3 ½ " **1.44/1.25 MB, 3 ½ "** 2.88 MB, 3 ½ " Disabled	Select the type of floppy disk drive.
Legacy Diskette B	360 Kb, 5 ¼ " 1.2 MB, 5 ¼ " 720 Kb, 3 ½ " 1.44/1.25 MB, 3 ½ " 2.88 MB, 3 ½ " **Disabled**	Select the type of floppy disk drive.
‣ Primary Master	Autodetected drive	Displays result of PM autotyping.
‣ Primary Slave	Autodetected drive	Displays result of PS autotyping.
‣ Compact Flash	Autodetected drive	Displays result of CF autotyping.
Smart Device Monitoring	Disabled **Enabled**	Turns on Self-Monitoring Analysis-Reporting Technology, which monitors the condition of the hard drive and reports when a catastrophic IDE failure is about to happen.
System Memory	N/A	Displays amount of conventional memory detected during bootup.
Extended Memory *	N/A	Displays amount of extended memory detected during bootup.

Notes: In the Option column, bold shows default settings.
(*) Extended Memory = capacity of memory module – selected frame buffer memory size.

24.3.1 Master or Slave Submenus

Feature	Option	Description
Type	None User **Auto** CD-ROM IDE Removable ATAPI Removable Other ATAPI	None = Autotyping is not able to supply the drive type or end user has selected None, disabling any drive that may be installed. User = End user supplies hdd information. Auto = Autotyping. The drive itself supplies the information. CD-ROM = CD-ROM drive. ATAPI Removable = Read- and writeable media e.g. LS120 and USB-ZIP Other ATAPI = for ATAPI devices not supported by other HDD features.
Cylinders	1 to 65,536	Number of cylinders.
Heads	1 to 256	Number of read/write heads.
Sectors	1 to 63	Number of sectors per track.
Maximum Capacity	N/A	Displays the calculated size of the drive in CHS.
Total Sectors	N/A	Number of total sectors in LBA mode.
Maximum Capacity	N/A	Displays the calculated size of the drive in LBA.
Multi-Sector Transfer	**Disabled** 2 sectors 4 sectors 8 sectors 16 sectors	Any selection except Disabled determines the number of sectors transferred per block. The standard is one sector per block.
LBA Mode Control	**Disabled** Enabled	Enabling LBA causes Logical Block Addressing to be used in place of CHS.
32-Bit I/O	**Disabled** Enabled	Enables 32-bit communication between CPU and IDE card. Requires PCI or local bus.
Transfer Mode	**Standard** Fast PIO 1 Fast PIO 2 Fast PIO 3 Fast PIO 4 FPIO 3 / DMA 1 FPIO 4 / DMA 2	Selects the method for transferring the data between the hard disk and system memory.
Ultra DMA Mode *	Disabled MOD0 MOD1 MOD2 MOD3 MOD4 MOD5	Selects the UDMA mode to move data to/from the drive. Autotype the drive to select the optimum transfer mode. This feature is autodetected.
SMART Monitoring	Disabled Enabled	Shows whether a disk supports SMART.

Note: In the Option column, bold shows default settings.
(*) The CompactFlash IDE interface is not capable of running UDMA modes. On the 40 pin IDE interface an 80line UDMA 100 cable is required for proper operation in modes UDMA 3 and higher.

24.4 Advanced Menu

Feature	Option	Description
▸ Advanced Chipset Control	Sub menu	Opens Advanced Chipset Control sub menu.
▸ PCI/PNP Configuration	Sub menu	Opens PCI/PNP Config sub menu.
▸ Memory Cache	Sub menu	Opens Cache Control sub menu.
▸ I/O Device Configuration	Sub menu	Opens Peripheral Config sub menu.
▸ Keyboard Features	Sub menu	Opens Keyboard Features sub menu.
▸ Hardware Monitor	Sub menu	Shows hardware monitor current state.
▸ Watchdog Settings	Sub menu	Opens Watchdog Config sub menu.
▸ Display Control	Sub menu	Opens Display Control sub menu
▸ Miscellaneous	Sub menu	Opens sub menu with miscellaneous options.

24.4.1 Advanced Chipset Control Submenu

Feature	Option	Description
Enable Memory gap	**Disabled** Enabled	Allows enabling a 1MB memory gap for add-on cards at 15MB
Graphics Engine 1	Disabled **Enabled**	Enable/Disable Internal Graphics Device.
Graphics Engine 2	Disabled **Enabled**	Enabled/Disabled Function 1 of the Internal Graphics Device
Graphics Memory	UMA = 1MB, **8MB**, 16MB, 32MB	Select the amount of main memory that the Internal Graphics Device will use.

Note: In the Option column, bold shows default settings.

24.4.2 PCI/PNP Configuration Submenu

Feature	Option	Description
Plug & Play OS	No **Yes**	If your system has a PnP OS (e.g. Win9x) select Yes to let the OS configure PnP devices not required for booting. No allows the BIOS to configure them.
Reset Configuration Data *	**No** Yes	Yes erases all configuration data in ESCD, which stores the configuration settings for plug-in devices. Select Yes when required to restore the manufacturer's defaults.
Secured Setup Configuration	**Yes** No	Yes prevents a Plug and Play OS from changing system settings.
▸ PCI Device, Slot #x	Sub menu	Opens sub menu to configure slot x PCI device
PCI IRQ line 1 PCI IRQ line 2 PCI IRQ line 3 PCI IRQ line 4 Onboard LAN IRQ line Onboard USB EHCI IRQ line	Disabled **Auto Select** IRQ3, 4, 5, 7, 9, 10, 11, 12, 14,15	Select IRQs for external PIC interrupts A/B/C/D and the onboard LAN and USB2.0 host controller. Select Auto to let the BIOS assign the IRQ.
▸ PCI/PNP ISA IRQ Resource Exclusion	Sub menu	Opens IRQ Exclusion sub menu.
Default Primary Video Adapter	AGP **PCI**	In a system with an AGP and a PCI video adapter end user can select the adapter which will be initialized by the BIOS.

Notes: In the Option column, bold shows default settings.
(*) Setting this option to "yes", under certain circumstances, may help to recover from system boot failure or a resource conflict.

24.4.3 PCI Device, Slot #x Submenu

Feature	Option	Description
Option ROM Scan	Disabled **Enabled**	Initialize device expansion ROM.
Enable Master	**Disabled** Enabled	Enables device in slot as a PCI bus master, not every device can function as a master. Check device documentation.
Latency Timer	**Default**, 20h, 40h, 60h, 80h, A0h, C0h, E0h	Minimum guaranteed time slice allocated for bus master in units of PCI bus clocks. A high-priority, high-throughput device may benefit from a greater value.

Note: In the Option column, bold shows default settings.

24.4.4 PCI/PNP ISA IRQ Resource Exclusion Submenu

Feature	Option	Description
IRQ3	**Available** Reserved	Reserves the specified IRQ for use by legacy ISA devices.
IRQ4	**Available** Reserved	See above.
IRQ5	**Available** Reserved	See above.
IRQ7	**Available** Reserved	See above.
IRQ9 *	**Available** Reserved	See above.
IRQ10	**Available** Reserved	See above.
IRQ11	**Available** Reserved	See above.
IRQ12	**Available** Reserved	See above.
IRQ14 **	**Available** Reserved	See above.
IRQ15 **	**Available** Reserved	See above.

Notes: In the Option column, bold shows default settings.
(*) IRQ9 is used for SCI in ACPI mode. Do not use IRQ9 for legacy ISA devices when ACPI enabled.
(**) Entry is only visible when primary IDE or secondary IDE is disabled.

24.4.5 Memory Cache Submenu

Feature	Option	Description
Memory Cache	Disabled **Enabled**	Enables or Disables L2 cache.
Cache System BIOS area	Uncached **Write Protected**	Controls caching of System BIOS area.
Cache Video BIOS area	Uncached **Write Protected**	Controls caching of Video BIOS area.
Cache Base 0-512K	Uncached Write Through Write Protected **Write Back**	Controls caching of base memory up to 512KB.
Cache Base 512-640K	Uncached Write Through Write Protected **Write Back**	Controls caching of base memory above between 512 and 640KB.
Cache Extended Memory area	Uncached Write Through Write Protected **Write Back**	Controls caching of system memory above 1MB.
D000 – D3FF D400 – D7FF D800 – DBFF DC00 – DFFF	**Disabled** Write Through Write Protected Write Back	Disabled: block is not cached. Write-Through: Write are cached and sent to main memory at once. Write-Protect: Writes are ignored. Write-Back: Writes are cached but not sent to main memory until necessary.

Note: In the Option column, bold shows default settings.

24.4.6 I/O Device Configuration Submenu

Feature	Option	Description
Local Bus IDE adapter	Disabled Primary Secondary **Both**	Enables onboard PCI IDE device.
USB Options	Sub menu	Opens USB Config sub menu.
AC97 Audio Controller	**Disabled** Enabled	Enables the AC97 Audio device.
Lan Options	Sub menu	Opens LAN Config sub menu.
SIO Options	Sub menu	Opens Super-IO Config sub menu.
Floppy disk controller	Disabled **Enabled**	Enable / Disable the onboard FDC controller.
Serial port A	Disabled Enabled **Auto**	Disabled turns off the port. Enabled requires end user to enter the base I/O address and the IRQ. Auto makes the BIOS configure the port.
Serial port B	**Disabled** Enabled Auto	Disabled turns off the port. Enabled requires end user to enter the base I/O address and the IRQ. Auto makes the BIOS configure the port.
Mode	**Normal**, IR	Set the mode for Serial Port B.
Base I/O address	3F8h, 2F8h, 3E8h, 2E8h	Select I/O base of port.
IRQ (port A and B)	IRQ 3, IRQ 4	Select IRQ of Port A and B

24.4.7 USB Options

Feature	Option	Description
USB UHCI Host Controller 1	**Enabled** Disabled	Enable / Disable UHCI 1 Host Controller for USB ports 0 and 1 (EPIC front).
USB UHCI Host Controller 2	Enabled **Disabled**	Enable / Disable UHCI 2 Host Controller for USB ports 2 and 3 (EPIC front).
USB EHCI Host Controller *	Disabled **Enabled**	Controls USB 2.0 functionality.
Legacy USB Support **	Disabled **Enabled**	Enable support for USB keyboard and mice and boot from USB mass storage devices.

Notes: In the Option column, bold shows default settings.
(*) The USB ports are multiplexed between UHCI and EHCI. Ports are routed to EHCI if an USB 2.0 high-speed device is connected and an EHCI driver is loaded.
(**) If you want to use the USB boot feature, enable USB BIOS Legacy Support. A 16kb UMB area (most likely DC000h-DFFFFh) is used for USB BIOS Legacy Support.

24.4.8 LAN Options

Feature	Option	Description
LAN 1		
LAN MAC address		Displays adapter's MAC address
Onboard LAN Controller	Disabled **Enabled**	Enables the ICH4 internal LAN controller.
Onboard LAN PXE ROM	**Disabled** Enabled	Enables the remote boot BIOS extension for the onboard LAN controller.
Enable WOL	**Disabled** Enabled	Enables the wake on LAN BIOS extension for the onboard LAN controller.
LAN 2		
LAN MAC address		Displays adapter's MAC address
Onboard LAN Controller	Disabled **Enabled**	Enables the ICH4 internal LAN controller.
Onboard LAN PXE ROM	**Disabled** Enabled	Enables the remote boot BIOS extension for the onboard LAN controller.
Enable WOL	**Disabled** Enabled	Enables the wake on LAN BIOS extension for the onboard LAN controller.

24.4.9 SIO Options

Feature	Option	Description
Floppy disk controller	Disabled **Enabled**	Enable / Disable the onboard FDC controller.
Serial port A	Disabled Enabled **Auto**	Disabled turns off the port. Enabled requires end user to enter the base I/O address and the IRQ. Auto makes the BIOS configure the port.
Serial port B	Disabled Enabled **Auto**	Disabled turns off the port. Enabled requires end user to enter the base I/O address and the IRQ. Auto makes the BIOS configure the port.
Mode	**Normal**, IR	Set the mode for Serial Port B.
Serial port C	**Disabled** Enabled Auto	Disabled turns off the port. Enabled requires end user to enter the base I/O address and the IRQ. Auto makes the BIOS configure the port.
Serial port D	**Disabled** Enabled Auto	Disabled turns off the port. Enabled requires end user to enter the base I/O address and the IRQ. Auto makes the BIOS configure the port.
Interface	**RS232**, RS485	Set the mode for Serial Port D.
Base I/O address	3F8h, 2F8h, 3E8h, 2E8h, 220h, 228h	Select I/O base of port.
IRQ	IRQ 3, IRQ 4, IRQ10, IRQ11	Select IRQ
Parallel Port	Disabled Enabled **Auto**	
Mode	Output only **Bi-directional** EPP ECP EPP & ECP	Set the mode for Parallel Port
Base I/O address	**378h**, 278h, 3BCh	Select I/O base of port.
Interrupt	IRQ 5, **IRQ 7**	Select IRQ
DMA channel	DMA1, **DMA3**	Set the DMA channel for the parallel port in ECP mode

Note: In the Option column, bold shows default settings.

24.4.10 Keyboard Features Submenu

Feature	Option	Description
Numlock	Auto **On** Off	On or Off turns NumLock on or off at boot up. Auto turns NumLock on if it finds a numeric key pad.
Key Click	**Disabled** Enabled	Turns audible key click on.
Keyboard auto-repeat rate	**30/sec**, 26.7/sec, 21.8/sec, 18,5/sec, 13.3/sec, 10/sec, 6/sec, 2/sec	Sets the number of times to repeat a keystroke per second if you hold the key down.
Keyboard auto-repeat delay	¼ sec, **½ sec**, ¾ sec, 1 sec	Sets the delay time after the key is held down before it begins to repeat the keystroke.

Note: In the Option column, bold shows default settings.

24.4.11 Hardware Monitor Submenu

This submenu shows the current voltages, temperatures and the fan speed of the system.

Voltage/Temperature/Fan	Explanation
VCC 3.3V Voltage	3.3V power plane
CPU Core Voltage	CPU core voltage
5Vsb Voltage	5V-Standby voltage
Battery Voltage	Battery voltage
CPU Temperature	CPU Temperature in °C and °F
CPU Fan Speed	CPU fan speed in rpm

24.4.12 Watchdog Settings Submenu

Feature	Option	Description
Mode	**Disabled** Reset NMI	Select watchdog operation mode.
Delay	1s, 5s, 10s, **30s**, 1min, 5.5min, 10.5min, 30.5min	The time until the watchdog counter starts counting. Useful to handle longer boot times.
Timeout	1s, 5s, 10s, **30s**, 1min, 5.5min, 10.5min, 30.5min	Max. trigger period.

Note: In the Option column, bold shows default settings.

24.4.13 Display Control Submenu

Feature	Option	Description
Display Mode	CRT only LFP only **CRT+LFP**	Select the display mode.
JDA Revision	x.x	Displays the revision of the JILI data area image.
Flat Panel Type	VGA * SVGA * XGA * XGA2 * SXGA * UXGA * Enter PAID Enter FPID **Auto**	Select Auto to let the BIOS automatically detect the panel type or use one of the predefined fixed panel types. Choose Enter PAID or Enter FPID to manually set JILI3 ID values.
PAID/FPID **	0 – FFFF, default **0**	Enter the JILI3 ID.
Flat Panel Scaling	Centered **Stretched**	Stretched expands a low resolution video mode to full screen on a higher flat panel resolution.
Flat Panel Backlight ***	0 – 255, default **128**	Enter a value to adjust backlight of the LCD.
Flat Panel Contrast ****	0 – 63, default **32**	Enter a value to adjust contrast of the LCD.

Note: In the Option column, bold shows default settings.
(*) Standard timings for VGA to UXGA panels cannot drive all available displays of that type that are on the market. Use a JILI cable whenever possible.
(**) Only visible if Enter PAID or Enter FPID is selected.
(***) Only visible if the panel adapter is equipped with a MAX5362 DAC for backlight control.
(****) Only visible if the panel adapter is equipped with a Xicore X9429 digital potentiometer for contrast control.

24.4.14 Miscellaneous Submenu

Feature	Option	Description
Floppy Check	**Disabled** Enabled	Enabled verifies floppy type on boot; disabled speeds boot.
Summary Screen	**Disabled** Enabled	If enabled, a summary screen is displayed just before booting the OS to let the end user see the system configuration.
QuickBoot Mode	Disabled **Enabled**	Allows the system to skip certain tests while booting. This will decrease the time needed to boot the system.
Extended Memory Testing	Normal * **Just zero it** None	Determines which type of tests will be performed on memory above 1MB.
Dark Boot	**Disabled** Enabled	If enabled, system comes up with a blank screen instead of the diagnostic screen during bootup.
Halt On Errors	**Yes**	Determines if post errors cause the system to halt.

	No	
PS/2 Mouse	**Auto Detect** Enabled Disabled	Selecting Disabled prevents any installed PS/2 mouse from functioning but frees up IRQ12. Selecting Autodetect frees IRQ12 if a mouse is not detected.
Spread Spectrum	**Disable** Enable	Controls the spread spectrum feature of the clock generator
Large Disk Access Mode	**DOS** Other	Select DOS if you have DOS. Select Other if you have another OS such as UNIX. A large disk is one that has more than 1024 cylinders, more than 16 heads or more than 63 sectors per track.

Note: In the Option column, bold shows default settings.
(*) The option normal is not visible when QuickBoot is enabled.

Dark Boot

After you turn on or reset the computer, Dark Boot displays a graphical logo (default is a blank screen) instead of the text based POST screen, which displays a number of PC diagnostic messages.

The graphical logo stays up until just before the OS loads unless:

- You press <Esc> to display the POST screen
- You press <F2> to enter Setup
- POST issues an error message
- The BIOS or an option ROM requests keyboard input

24.5 Security Menu

Feature	Option	Description
Supervisor Password is	**Clear** Set	Displays whether password is set.
User Password is	**Clear** Set	Displays whether password is set.
Set User Password *	Up to seven alphanumeric characters	Pressing <Enter> displays the dialog box for entering the user password. In related systems, this password gives restricted access to setup.
Set Supervisor Password *	Up to seven alphanumeric characters	Pressing <Enter> displays the dialog box for entering the user password. In related systems, this password gives full access to setup.
Diskette access	User **Supervisor**	Enabled requires supervisor password to access floppy disk.
Fixed disk boot sector	**Normal** Write protected	Write protect the boot sector on the hard disk for virus protection. Requires a password to format or Fdisk the hard disk.
Virus check reminder	**Disabled** Daily Weekly Monthly	Displays a message during bootup asking (Y/N) if you backed up the system or scanned for viruses. Message returns on each boot until you respond with Y. Daily displays the message on the first boot of the day, Weekly on the first boot after Sunday, and monthly on the first boot of the month.
System backup reminder	**Disabled** Daily Weekly Monthly	Displays a message during bootup asking (Y/N) if you backed up the system or scanned for viruses. Message returns on each boot until you respond with Y. Daily displays the message on the first boot of the day, Weekly on the first boot after Sunday, and monthly on the first boot of the month.
Password on boot	**Disabled** Enabled	Enabled requires a password on boot. Requires prior setting of the supervisor password. If supervisor password is set and this option is disabled, BIOS assumes user is booting.

Notes: In the Option column, bold shows default settings.
(*) Enabling Supervisor Password requires a password for entering Setup.
Passwords are not case sensitive. User and Supervisor passwords are related. A User password is possible only if a Supervisor password exists.

24.6 Power Menu

In the BIOS Setup Utility, you can set up an Advance Power Management system (APM 1.2) to reduce the amount of energy used after specified periods of inactivity. The setup menu supports:

- Full On State
- Standby State with Partial Power Reduction
- Suspend State with Full Power Reduction

In addition you can enable an ACPI 1.0 support in the BIOS setup utility, if you intend to use an operating system supporting the Advanced Configuration and Power Management Interface. For logical reasons it is required to use an ATX power supply with the ACPI feature.

The following states are supported from the system:

- S0 (Working)
- S1 (Sleeping with processor context maintained)
- S5 (Soft off)

The state S2 (sleeping with processor context not maintained) and S3 (Save to RAM) is not supported. The state S4 (Save to Disk) is a matter of the used operating system.

24.6.1 ACPI Resume Events

The following events resume the system from S1:

- Power button
- PME#
- PS/2 keyboard and mouse
- USB keyboard and mouse activity
- USB resume event

Feature	Option	Description
Enable ACPI *	No **Yes**	Enables/Disables ACPI BIOS (Advanced Configuration and Power Interface). IRQ9 is used for SCI (System Control Interrupt).
‣ ACPI Control	sub menu	Opens the ACPI sub menu
Max CPU frequency **	1800MHz 1600MHz 1400MHz **1200MHz** 1000MHz 800MHz 600MHz	Warning! Selecting frequencies higher then the default may cause the system to reach "critical trip point" and shut down if a proper cooling solution is not used. Always ensure that you use proper cooling when selecting higher frequency settings.
Automatic Thermal Monitor Control Circuit **	Disabled TM1 **TM2 *** **	Enables the thermal control circuit (TCC) of the thermal monitor feature of the Pentium-M CPU. TM1 = 50% duty cycle TM2 = Geyserville III **Automatic TTC must be enabled to ensure that the processor operates within specification.**
Hard Disk Timeout	**Disabled**, 10 sec – 15 min	Inactivity period of hard disk required before standby (motor off).
Video Timeout	**Disabled**, 10 sec – 15 min	Inactivity period of user input device before the screen is turned off.
Resume on Modem Ring	**Off** On	Enabled wakes the system on incoming calls detected by mode (RI).
Resume on Time	**Off** On	Enabled wakes the system at a specific time.
Resume Time	00:00:00	Specifies the time when the system is to wake.
Power supply	**ATX** AT	Specifies whether an ATX or an AT power supply is used.
Power Button Function	Power Off **Sleep**	Determines if the system enters suspend or soft off when the power button is pressed.

Notes: In the Option column, bold indicates default setting.
(*) Disable ACPI support whenever you are using an operating system without ACPI capability.
(**) See the chapter "Important Technology Information of this user's guide for more details about these features.
(***) EPIC/PM with Celeron M processor does not support TM2.

24.6.2 ACPI Control Submenu

Feature	Option	Description
Active Trip Point *	Disabled 40 C – 100 C	Determines the temperature of the ACPI Active Trip Point, the point at which the OS will turn on/off the CPU fan.
Passive Trip Point *	Disabled 40 C – 100 C	Determines the temperature of the ACPI Passive Trip Point, the point at which the OS will turn on/off CPU clock throttling.
Critical Trip Point *	40 C – 110 C	This value controls the temperature of the ACPI Critical Trip Point- the point at which the OS will shut the system off.
APIC – IO APIC Mode *	Disabled Enabled	This item is valid only for Windows XP. Also, a fresh install of the OS must occur when APIC Mode is desired. Test the IO APIC by setting an item to Enabled. The APIC Table will then be pointed to by the RSDT, the Local APIC will be initialized, and the proper enable bits will be set in IHC4M. See section I/O APIC vs. 8259 PIC Interrupt mode
Native IDE Support *	Disabled Enabled	Enable Native IDE support for WINXP by setting this item. The NATA Package will be created if this item is set to Enabled. Changing this item will have no effect in WIN98, WINME, or WIN2K. See section Native vs. compatible IDE mode for more details.

Notes: In the Option column, bold indicates default setting.
(*) See the chapter "Important Technology Information of this user's guide for more details about these features.

24.7 Boot Menu and Utilities

MultiBoot is a boot utility integrated in the PhoenixBIOS 4.0. The EPIC/PM provides the MultiBoot XP version with integrated Boot First function.

24.7.1 MultiBoot XP

MultiBoot XP comes with a complete new look of the Boot Device Priority submenu. This submenu is now separated into two sections:

- Boot Priority Order
- Excluded from Boot Order

MultiBoot XP can display the setup menus by each kind of device type and arrange the boot priority order with any sequence of devices. MultiBoot XP meets the requirements of PC 98 and accommodates more devices that are bootable. It employs a boot scheme that is generic and flexible enough to boot from any current device. You can select your boot device in Setup, or you can choose a different device each time you boot by selecting your boot device in the Boot First function.

An available bootable device can be easily switched between the two sections by just highlighting the device and then pressing <X>. To change the order, select the device to change and press <-> to decrease or <+> to increase priority. You can also choose between four default configurations for the boot order <1>-<4>.

Boot Priority Order

This section shows eight configuration entries for up to eight devices that can be arranged in boot priority order (1: highest priority, 8: lowest priority).

Excluded from Boot Order

This section shows all devices that are excluded from the boot order. Any device listed here will never be used as boot device and not appear in the Boot First function.

The following table shows a list of supported devices:

Device	Description
IDE 0	Primary master IDE hard drive
IDE 1	Primary slave IDE hard drive
IDE 2	Secondary master IDE hard drive
IDE 3	Secondary slave IDE hard drive
IDE CD	IDE compatible CD-ROM drive
Legacy Floppy Drives	Standard Legacy Diskette Drive
USB KEY	USB Stick
USB FDC	USB Diskette Drive
USB HDD	USB Hard Drive and memory sticks that follow MMS specification
USB CDROM	USB CD-ROM Drive
USB ZIP	USB ZIP Drive
USB LS120	USB LS120 Drive
PCI BEV	Ethernet Controller on the PCI Bus with LAN Boot ROM
PCI SCSI	SCSI Controller on the PCI Bus with SCSI BIOS ROM

24.7.2 Boot First Function

Display the Boot First function by pressing <Esc> during POST. In response, the BIOS displays the message Entering Boot Menu and then displays the Boot Menu at the end of POST. With the MultiBoot XP feature only devices detected during boot up are displayed.

Use the menu to select a following option:

- Override the existing boot sequence (for this boot only) by selecting another boot device. If the specified device does not load the OS, the BIOS reverts to the previous boot sequence.
- Enter Setup.
- Press <Esc> to continue with the existing boot sequence.

24.8 Exit Menu

The following sections describe the five options in Exit Menu. Pressing <Esc> does not exit this menu. You must select an item from the menu to exit.

Feature	Option	Description
Exit Saving Changes	Saves selections and exits setup. The next time the system boots, the BIOS configures the system according to the Setup selection stored in CMOS.	Exit saving changes.
Exit Discarding Changes	Exits Setup without storing in CMOS any new selections you may have made. The selections previously in effect remain in effect.	Exit discarding changes.
Load Setup Defaults	Displays default values for all the Setup menus.	Load setup defaults.
Discard Changes	If, during a Setup session, you change your mind about changes you have made and have not yet saved the values to CMOS, you can restore the values you saved to CMOS.	Discard changes.
Save Changes	Saves all the selection without exiting Setup. You can return to the other menus to review and change your selection.	Save changes.

24.9 Kontron BIOS Extensions

Besides the Phoenix System BIOS, the EPIC/PM comes with a few BIOS extensions that support special features. All extensions are located in the onboard flash EEPROM. Some extensions are permanently available; some are loaded if required during boot up. Supported features include:

- JIDA standard
- Remote Control (JRC)
- Onboard LAN RPL ROM

All enabled BIOS extensions require shadow RAM. They will be loaded into the same 32K shadowed memory block, if possible. However, if the system memory cannot find free memory space because all the memory is already used for add-on peripherals, the BIOS extensions do not load.

24.9.1 JIDA BIOS extension

The JUMPtec Intelligent Device Architecture (JIDA) BIOS extension is not a true extension BIOS. It is part of the system BIOS and is located in the system BIOS segments after boot up. It is permanently available and supports the JIDA 16-bit and JIDA 32-bit standard.

The JIDA 16-bit standard is a software interrupt 15hex driven programmers interface and offers lots of board information functions. For detailed information about programming, refer to the JIDA specification and a source code example (JIDAI???.ZIP), which you can find at the Kontron Web site. The three question marks represent the revision number of the file. You also can contact technical support for this file.

For other operating systems, special 32-bit drivers (JIDAIA??.ZIP) are available. You can download the zip file from the Kontron Web site.

24.9.2 Remote Control Client Extension

You can remotely control the EPIC/PM using software available from Kontron (JRC-1, Part Number 96047-0000-00-0). This software tool can communicate with the board via one of the serial ports. During boot-up, the system BIOS scans the serial ports for an available JRC connection. If detected, it loads the JRC client BIOS extension into the memory. With the JRC client loaded into the first detected free memory location between C0000hex and DFFFFhex, a 16K block is shadowed.

For more information on the Remote Control usage, refer to the JRC-1 technical manual or Application Note JRCUsage_E???.PDF, which you can find on the Kontron Web site.

24.9.3 LAN PXE ROM

If the onboard LAN PXE ROM is enabled in the system BIOS setup, a special optional ROM for the Ethernet controller loads into memory during boot up. This optional ROM allows you to boot the EPIC/PM over an Ethernet connection. A server with Intel PXE boot support is required on the other side of the Ethernet connection. The setup and configuration of the server, including PXE support, is not the responsibility of Kontron.

The PXE ROM extension is loaded into the first free memory area between C0000hex and DFFFFhex and a 16K block of memory is shadowed.

24.10 Updating or Restoring BIOS Using PhoenixPhlash

PhoenixPhlash allows you to update the BIOS by using a floppy disk without having to install a new ROM chip. PhoenixPhlash is a utility used to flash a BIOS to the Flash ROM installed on the EPIC/PM.

Use PhoenixPhlash to:

- Update the current BIOS with a newer version
- Restore a corrupt BIOS

24.10.1 Flashing a BIOS

Use the following procedure to update or restore a BIOS.

1. Download the Phoenix Phlash compressed file, CRDxEPBA.ZIP, from the KONTRON Embedded Modules Web site or contact your local technical support for it. It contains the following files:

File	Purpose
MAKEBOOT.EXE	Creates the custom boot sector on the Crisis Recovery Diskette.
CRISBOOT.BIN	Serves as the Crisis Recovery boot sector code.
MINIDOS.SYS	Allows the system to boot in Crisis Recovery Mode.
PHLASH16.EXE	Programs the flash ROM.
WINCRIS.EXE	Creates the Crisis Recovery Diskette from Windows.
WINCRIS.HLP	Serves as the help file of WINCRISES.EXE.
CRISDISK.BAT	Batch file for crisis disk.
BIOS.WPH	Serves as the actual BIOS image to be programmed into Flash ROM.

2. Install Phoenix Phlash on a hard disk by unzipping the content of CRDxEPBA.ZIP into a local directory such as C:\PHLASH.
3. Create a Crisis Recovery Diskette by inserting a blank diskette into Drive A: or B: and execute WINCRISIS.EXE. This at least copies three files onto the diskette.

File	Purpose
MINIDOS.SYS	Allows the system to boot in Crisis Recovery Mode.
PHLASH16.EXE	Programs the flash ROM.
BIOS.ROM	Serves as the actual BIOS image to be programmed into Flash ROM.

4. If the BIOS image (BIOS.ROM) changes due to an update or bug fix, copy the new BIOS onto the diskette and name it BIOS.ROM.

   Phoenix Phlash runs in either command line mode or crisis recovery mode.

5. Use the command line mode to update or replace a BIOS. To execute Phlash in this mode, move to the Crisis Recovery Disk and type:

   PHLASH16 <bios name> (Example: PHLASH16 EPBAR110.WPH)

PhoenixPhlash will update the BIOS. PhoenixPhlash can fail if the system uses memory managers. If this occurs, the utility displays the following message:

Cannot flash when memory manager are present.

If you see this message after you execute Phlash, disable the memory manager or use parameter /x for Phlash16.exe.

24.10.2 Preventing Problems When Updating or Restoring BIOS

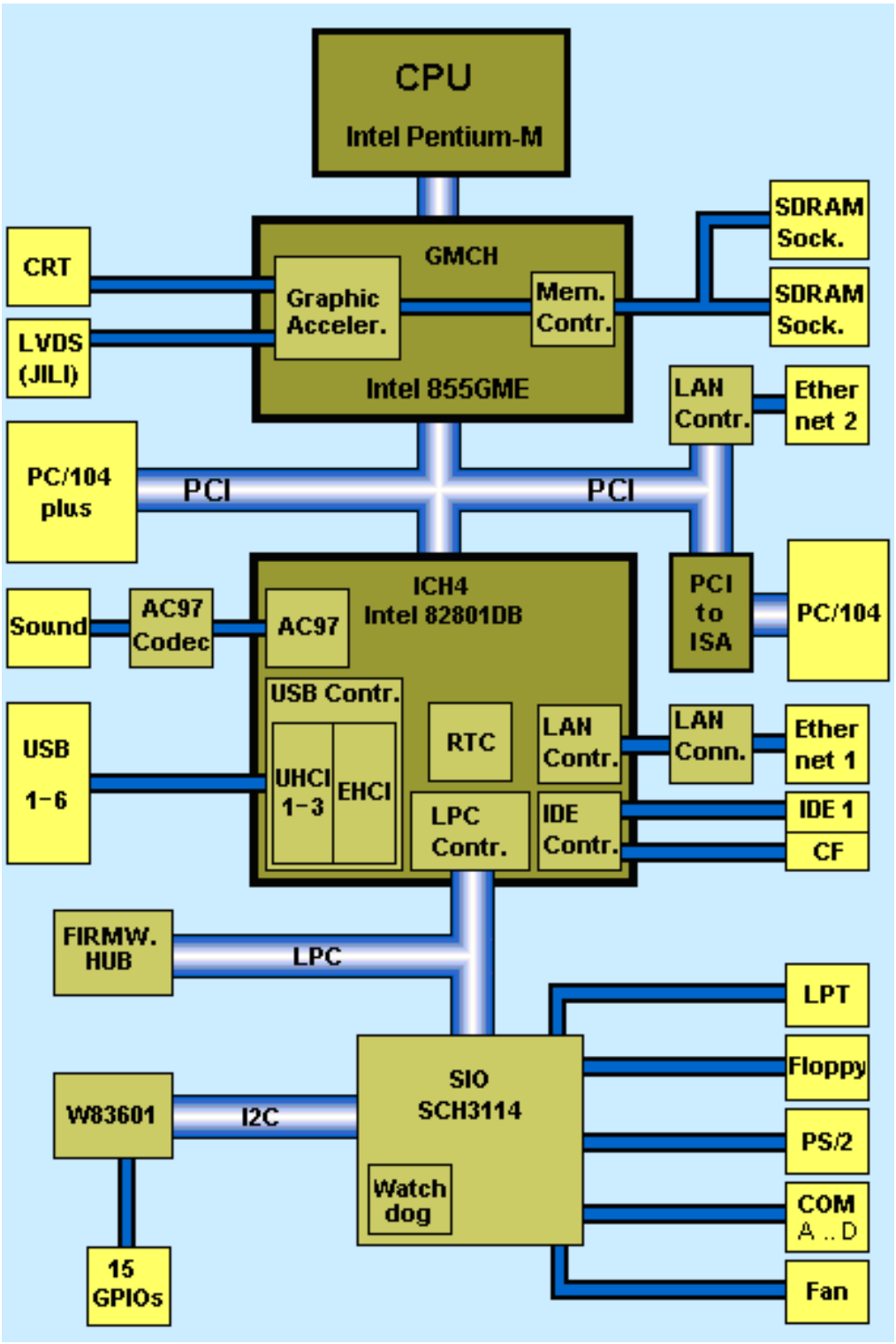
Updating the BIOS represents a potential hazard. Power failures or fluctuations can occur when you update the Flash ROM can damage the BIOS code, making the system unbootable.

To prevent this hazard, many systems come with a boot-block Flash ROM. The boot-block region contains a fail-safe recovery routine. If the boot-block code finds a corrupted BIOS (checksum fails), it boots into the crisis recovery mode and loads a BIOS image from a crisis diskette (see above).

Additionally, the end user can insert an update key into the parallel port (LPT) to force initiating the boot block recovery routine.

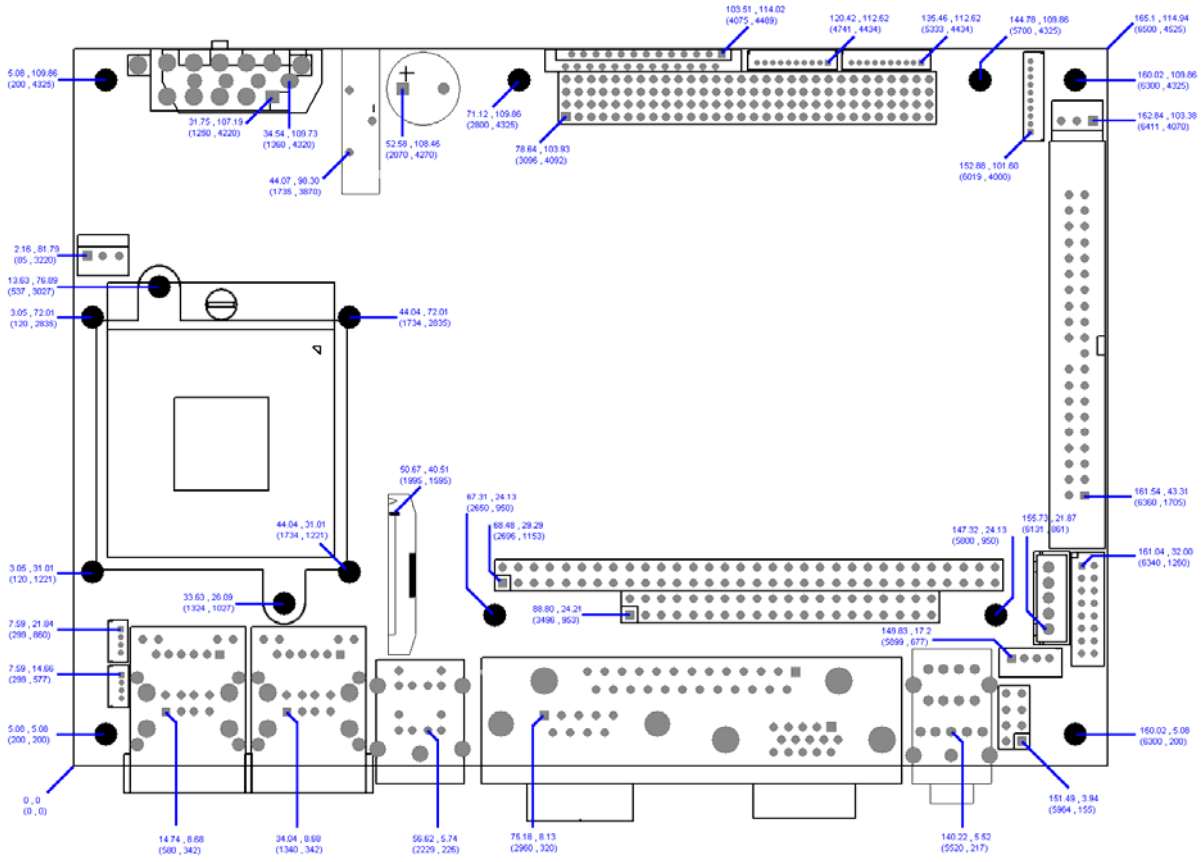
For further information on the update key and the crisis diskette, see the Application Note PHLASH_SCE???, which is available from the KONTRON Embedded Modules Web site. The three question marks stand for the revision number of the file.

25 Appendix C: Block Diagram



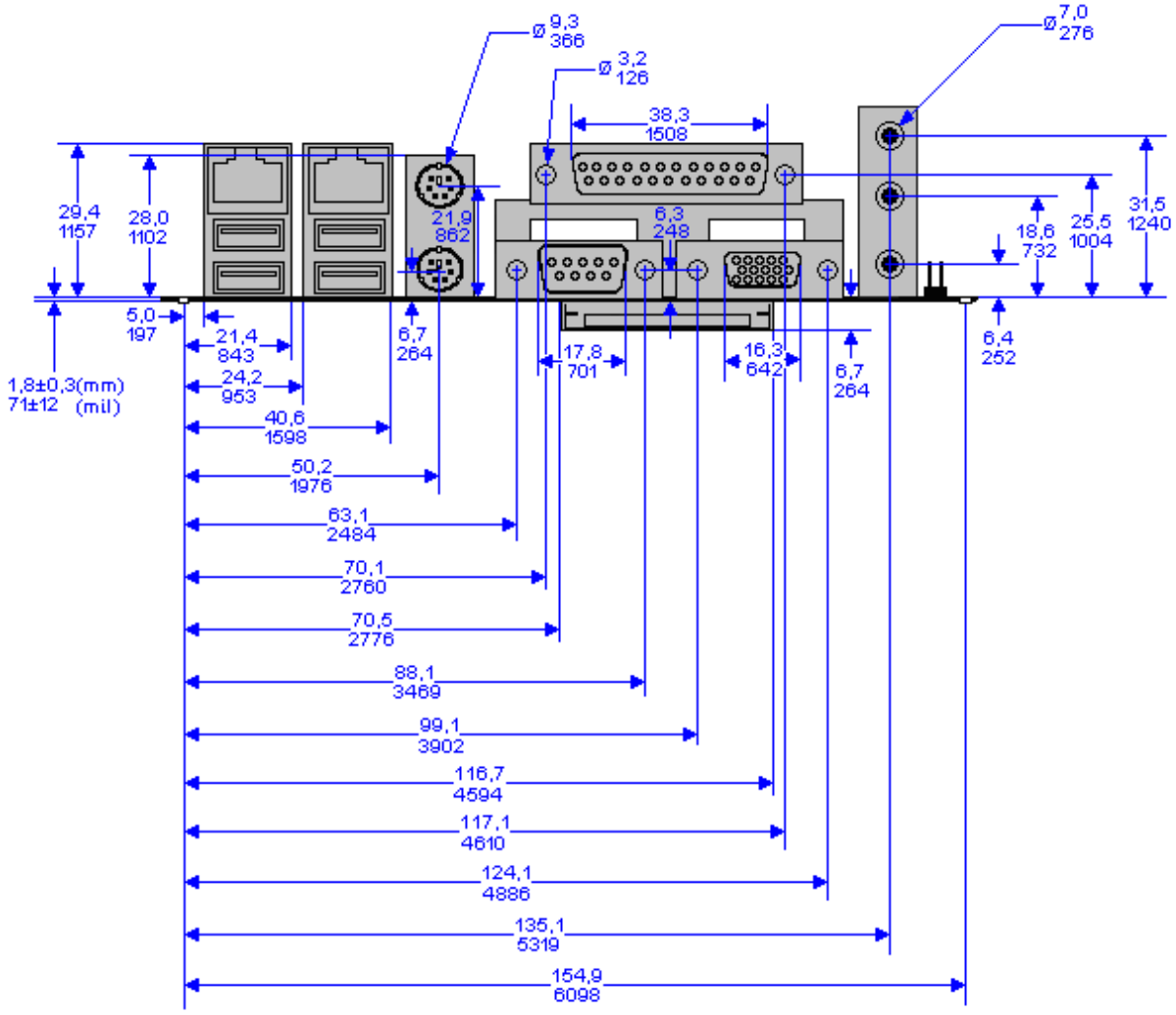
26 Appendix D: Mechanical Dimensions

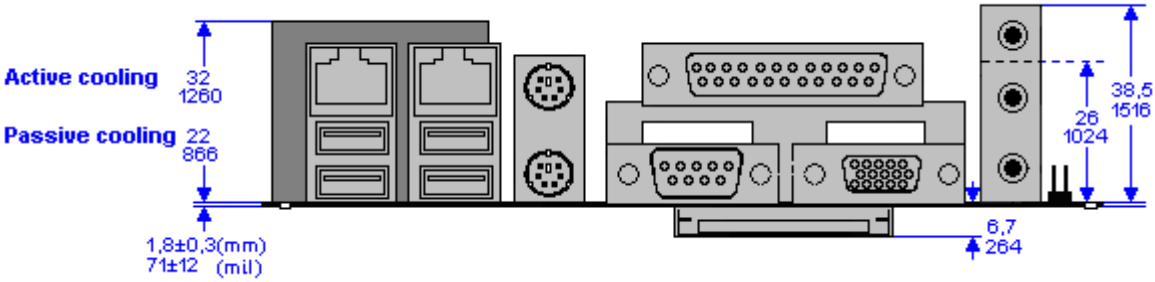
26.1 Top View



Dimensions on Mounting Holes and Pin 1 of each connector given in mm (mil)

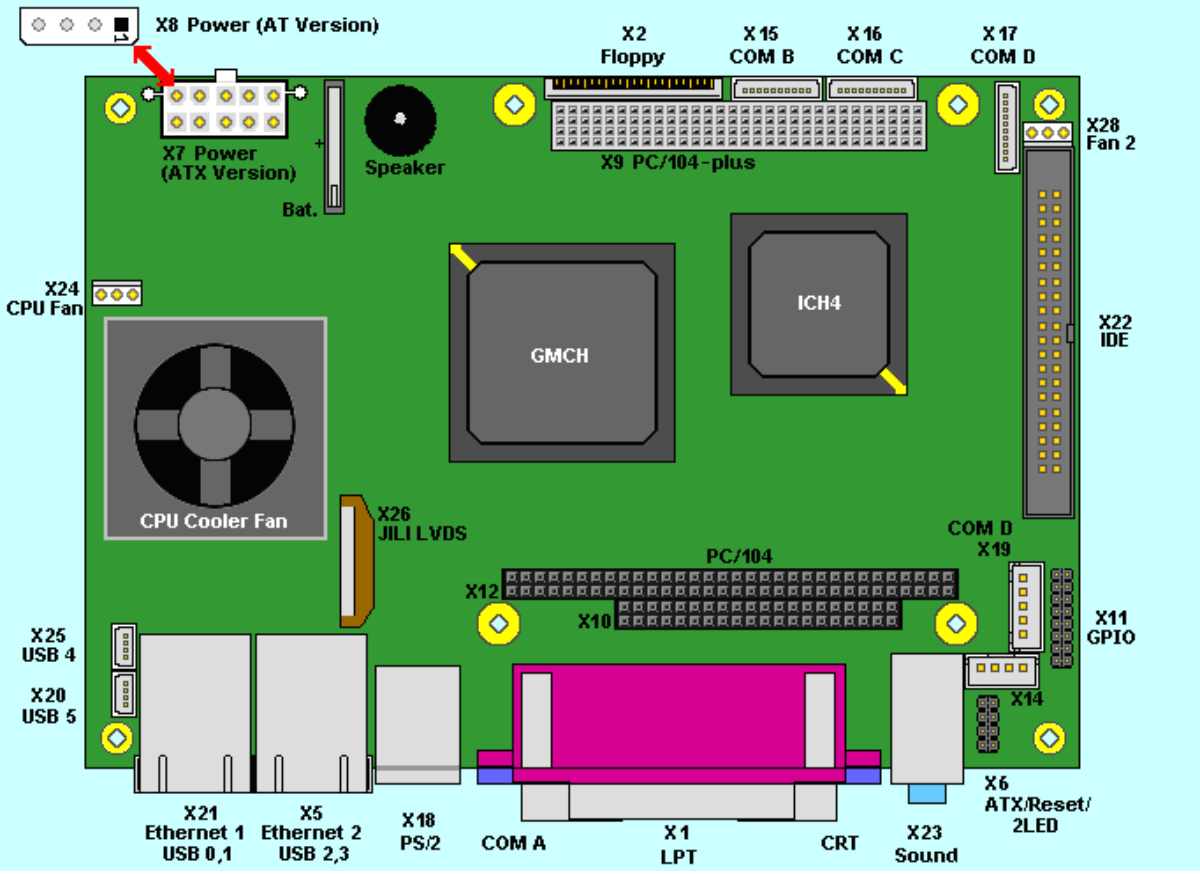
26.2 Front View





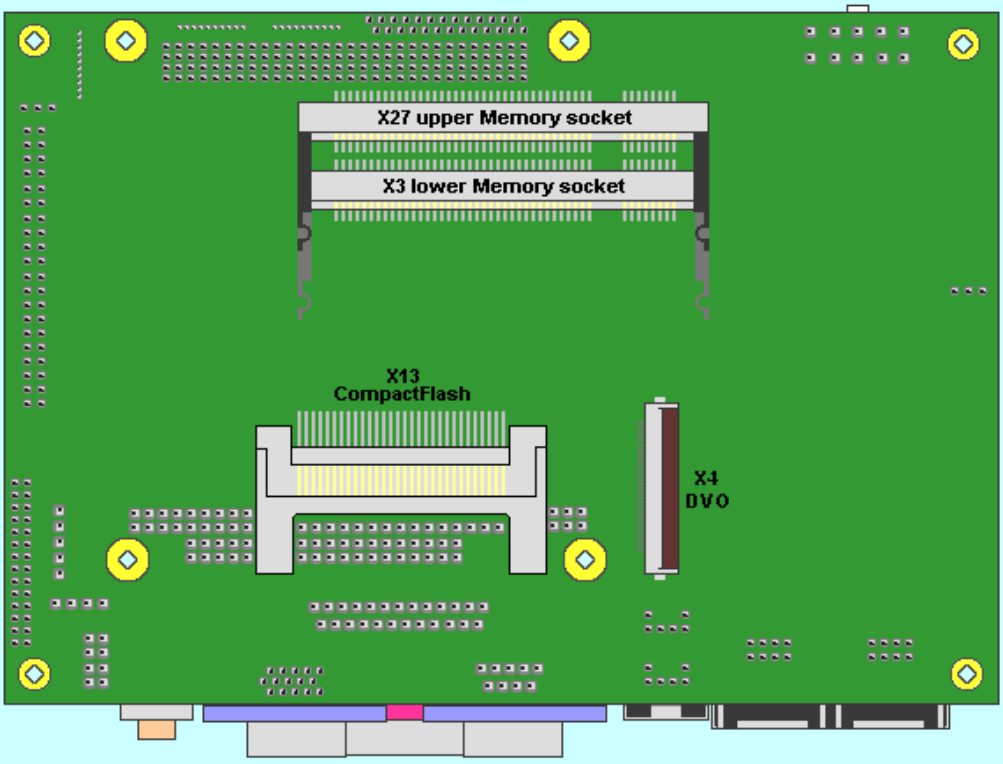
27 Appendix E: Connector Layout

27.1 Top Side



Notes: The position of Pin 1 of each connector can be seen in the previous chapter.

27.2 Bottom Side



27.3 Connector Functions and Interface Cables

The table notes connector functions, as well as mating connectors and available cables.

Connector	Function	Mating Connector	Available Cable or Accessory	Description
X1	CRT Connector	Standard DSUB15 male plug		For CRT monitor connection
	Serial Interface Connectors (COM A)	Standard DSUB9 female plug.		For DSUB9 RS232 connection
	Parallel Interface LPT Connector	Standard DSUB25 male plug.		For DSUB 25 LPT connection
X2	Floppy Drive Interface Connector		ADA-FLOPPY-2 (PN 96001-0000-00-0) or KAB-FLOPPY/MOPS-1 (PN 96019-0000-00-0)	For 3.5" floppy or slim-line floppy.
X3	DDR SDRAM SODIMM socket 1			
X4	DVO Connector			For DVO interfacing
X5	2 USB Connectors	Standard USB plug		For USB device connection
	Ethernet Connector	Standard RJ45 plug		For Ethernet connection
X6	ATX/Reset/2LED Connector	2.54mm 8 pos. female header		For power and reset button
X7	ATX Power Connector	AMP DUAC Connector or compatible	KAB-ATX-20T010 (PN 96072-0000-00-0)	For power connection
	AT Power Connector	Mate-N-Lok Connector (AMP 1-480424-0 or compatible)	**KAB-5V-ATX10 required**	For power connection
X9	PC/104-Plus Bus (PCI part)	2mm 120pos. (EPT 264-60303-12)		
X10	PC/104 Bus (AT-Bus part)	2.54mm 40 pos. (EPT 962-60203-12 or compatible for board to board connection)		
X11	GPIO Connector	2mm 28 pos. female header		For general purpose I/O usage
X12	PC/104 Bus (XT-Bus part)	2.54mm 64 pos. (EPT 962-60323-12 or compatible for board to board connection)		
X13	CompactFlash Connector			For CompactFlash IDE storage devices.
X14	Line-In Connector	2mm 4 pos. (Molex 87369-0400 or compatible)		For internal line-in connection
X15, X16, X17	Serial Interface	1.25mm 10 pos.	KAB-DSUB9-3	For DSUB 9

	Connectors	(Molex 51021-1000 or compatible)	(PN 96061-0000-00-0)	adaptation.
X18	PS/2 Keyboard and Mouse Interfaces	Standard PS/2 plugs		For PS/2 Mouse and Keyboard
X19	Serial Interface Connector COM D	2.5mm 5 pos. (JST XHP-5 or compatible)		For RS485 connection
X20, X25	USB interface connector	1.25mm 4 pos. (Molex 51021-0400 or compatible)	KAB-USB-1 (PN 96054-0000-00-0)	For standard USB adoption
X21	2 USB Connectors	Standard USB plug		For USB device connection
	Ethernet Connector	Standard RJ45 plug		For Ethernet connection
X22	Primary IDE Hard Disk Interface Connector	2.54mm 40 pos. (AMP 4-215882-0 or compatible)	KAB-IDE-1 (PN 96022-0000-00-0)	For 3.5" HDD
X23	Sound Interface	Standard audio plugs		For audio interfacing
X24	CPU Fan Interface	2.54mm 3 pos. (AMP MTA-100 3-640440-3 or compatible)		For CPU fan connection
X26	JILI LVDS Interface		KAB-JILI-?????? (see separate cable list)	For JILI interface cables
X27	DDR SDRAM SODIMM socket 2			
X28	Chassis Fan Interface	2.54mm 3 pos. (AMP MTA-100 3-640440-3 or compatible)		For Chassis fan connection

27.4 Pin-out Table

Pin	COM A	COM B-D	COM D RS485	LPT	Floppy	Primary IDE	Compact Flash	ATX/ Reset/ 2LED	CRT
	X1	X15–X17	X19	X1	X2	X22	X13	X6	X1
1	/DCD1	/DCD	RXD+	/STB	VCC *	/HDRST	GND	HDLED	RED
2	SIN1	/DSR	RXD-	PD0	/IDX	GND	D3	CFLED	GRN
3	SOUT1	SIN	GND	PD1	VCC *	PIDE_D7	D4	VCC	BLU
4	/DTR1	/RTS	TXD+	PD2	/DR0	PIDE_D8	D5	VCC	NC
5	GND	SOUT	TXD-	PD3	VCC *	PIDE_D6	D6	/RESIN	GND
6	/DSR1	/CTS		PD4	/DSKCHG	PIDE_D9	D7	GND	GND
7	/RTS1	/DTR		PD5	NC	PIDE_D5	/CS1	/PWRBTN	GND
8	/CTS1	/RI		PD6	NC	PIDE_D10	GND	GND	GND
9	RI1	GND		PD7	NC	PIDE_D4	GND		NC
10		VCC *		/ACK	/MTR0	PIDE_D11	GND		GND
11				/BUSY	NC	PIDE_D3	GND		NC
12				PE	/FDIR	PIDE_D12	GND		DDDA
13				/SLCT	NC	PIDE_D2	VCC		HSYNC
14				/AFD	/STEP	PIDE_D13	GND		VSYNC
15				/ERR	GND	PIDE_D1	GND		DDCK
16				/INIT	/WDATA	PIDE_D14	GND		
17				/SLIN	GND	PIDE_D0	GND		
18				GND	/WGATE	PIDE_D15	SA2		
19				GND	GND	GND	SA1		
20				GND	/TRK0	NC	SA0		
21				GND	GND	PIDE_DRQ	D0		
22				GND	/WRTPRT	GND	D1		
23				GND	GND	/PIDE_IOW	D2		
24				GND	/RDATA	GND	IOCS16		
25				GND	GND	/PIDE_IOR	GND		
26					/HDSEL	GND	GND		
27						PIDE_RDY	D11		
28						PIDE_PD1	D12		
29						/PIDE_AK	D13		
30						GND	D14		
31						PIDE_IRQ	D15		
32						NC	/CS3		
33						PIDE_A1	GND		
34						PIDE_ATAD	/IOR		
35						PIDE_A0	/IOW		
36						PIDE_A2	VCC		
37						/PIDE_CS1	IRQ		
38						/PIDE_CS3	VCC		
39						PIDE_ACT	GND		
40						GND	NC		
41							/RESET		
42							IOCHRDY		
43							DRQ		
44							DACK		
45							SIDE_ACT		
46							ATADET		
47							D8		
48							D9		
49							D10		
50							GND		

Pin	Ethernet	PS/2 Keyboard	PS/2 Mouse	USB	Line-In	GPIO	Power ATX	Power AT	Fan
	X5, X21	X18	X18	X5, X20, X21, X25	X14	X11	X7	X8	X24, X28
1	TXD+	KBDAT	MSDAT	VCC * ***	AUXL_C/REAR_L	GP_17	PS_ON	V5S *	Sense
2	TXD-	NC	NC	USB-	ASGND	GND	GND	GND	VCC *
3	RXD+	GND	GND	USB+	AUXR_C/ REAR_R	GP_16	GND	GND	GND
4	NC **	VCC *	VCC *	GND	ASGND	GPINT26	+12V *	VCC12 *	
5	NC **	KBCLK	MSCLK			GP_15	+3.3V *		
6	RXD-	NC	NC			GP_25	+5V_SB		
7	NC **					GP_14	+5V		
8	NC **					GP_24	+5V		
9						GP_13	-12V		
10						GP_23	GND		
11						GP_12			
12						GP_22			
13						GP_11			
14						GP_21			
15						GP_10			
16						GP_20			

Notes: *(*)* *To protect the external power lines of peripheral devices, make sure that:*
-- the wires have the right diameter to withstand the maximum available current
-- the enclosure of the peripheral device fulfils the fire-protecting requirements of IEC/EN 60950.

(**) *Do not connect anything to these signals.*

(***) *The internal USB ports 4 and 5 are not protected on the power lines. An additional resetable fuse is recommended.*

Pin	PC104 (A)	PC104 (B)	PC104 (C)	PC104 (D)	PC/104 Plus (A)	PC/104 Plus (B)	PC/104 Plus (C)	PC/104 Plus (D)
	X10, X12				X9			
0			GND	GND				
1	/IOCHCK	GND	/SBHE	/MEMCS16	GND	Reserved	VCC (**)	AD00
2	SD7	RESETDRV	LA23	/IOCS16	VCC (**)	AD02	AD01	AD03
3	SD6	VCC (**)	LA22	IRQ10	AD05	GND	AD04	AD03
4	SD5	IRQ9	LA21	IRQ11	C/BE0	AD07	GND	AD06
5	SD4	-5V (**)	LA20	IRQ12	GND	AD09	AD08	GND
6	SD3	DRQ2	LA19	IRQ15	AD11	VCC (**)	AD10	GND
7	SD2	-12V (**)	LA18	IRQ14	AD14	AD13	GND	AD12
8	SD1	/0WS	LA17	/DACK0	VCC3 (**)	C/BE1	AD15	VCC3 (**)
9	SD0	+12V (**)	/MEMR	DRQ0	SERR	GND	SB0	PAR
10	IOCHRDY	GND (*)	/MEMW	/DACK5	GND	PERR	VCC3 (**)	SDONE
11	AEN	/SMEMW	SD8	DRQ5	STOP	VCC3 (**)	LOCK	GND
12	SA19	/SMEMR	SD9	/DACK6	VCC3 (**)	TRDY	GND	DEVSEL
13	SA18	/IOW	SD10	DRQ6	FRAME	GND	IRDY	VCC3 (**)
14	SA17	/IOR	SD11	/DACK7	GND	AD16	VCC3 (**)	C/BE2
15	SA16	/DACK3	SD12	DRQ7	AD18	VCC3 (**)	AD17	GND
16	SA15	DRQ3	SD13	VCC (**)	AD21	AD20	GND	AD19
17	SA14	/DACK1	SD14	/MASTER	VCC3 (**)	AD23	AD22	VCC3 (**)
18	SA13	DRQ1	SD15	GND	IS0 (AD20)	GND	IS1 (AD21)	IS2 (AD22)
19	SA12	/REFRESH	GND	GND	AD24	C/BE3	VI/O	IS3 (AD23)
20	SA11	SYSCLK			GND	AD26	AD25	GND
21	SA10	IRQ7			AD29	VCC (**)	AD28	AD27
22	SA9	IRQ6			VCC (**)	AD30	GND	AD31
23	SA8	IRQ5			REQ0	GND	REQ1	VI/O
24	SA7	IRQ4			GND	REQ2	VCC (**)	GNT0
25	SA6	IRQ3			GNT1	VI/O	GNT2	GND
26	SA5	/DACK2			VCC (**)	CLK0	GND	CLK1
27	SA4	T/C			CLK2	VCC (**)	CLK3	GND
28	SA3	BALE			GND	INTD	VCC (**)	RST
29	SA2	VCC (**)			+12V (**)	INTA	INTB	INTC
30	SA1	OSC			-12V (**)	Reserved	Reserved	Reserved
31	SA0	GND						
32	GND	GND						

Notes: (*) Key pin for PC/104; GND for PC/104+ specification

(**) To protect the external power lines of peripheral devices, make sure that:

- the wires have the right diameter to withstand the maximum available current

- the enclosure of the peripheral device fulfils the fire protecting requirements of IEC/EN 60950.

28 Appendix F: PC Architecture Information

The following sources of information can help you better understand PC architecture.

28.1 Buses

28.1.1 ISA, Standard PS/2 - Connectors

- AT Bus Design: Eight and Sixteen-Bit ISA, E-ISA and EISA Design, Edward Solari, Annabooks, 1990, ISBN 0-929392-08-6
- AT IBM Technical Reference Vol 1&2, 1985
- ISA & EISA Theory and Operation, Edward Solari, Annabooks, 1992, ISBN 0929392159
- ISA Bus Specifications and Application Notes, Jan. 30, 1990, Intel
- ISA System Architecture, Third Edition, Tom Shanley and Don Anderson, Addison-Wesley Publishing Company, 1995, ISBN 0-201-40996-8
- Personal Computer Bus Standard P996, Draft D2.00, Jan. 18, 1990, IEEE Inc
- Technical Reference Guide, Extended Industry Standard Architecture Expansion Bus, Compaq 1989

28.1.2 PCI

- PCI SIG: The PCI-SIG provides a forum for its ~900 member companies, who develop PCI products based on the specifications that are created by the PCI-SIG. You can search for information about the SIG on the Web.
- PCI & PCI-X Hardware and Software Architecture & Design, Fifth Edition, Edward Solari and George Willse, Annabooks, 2001, ISBN 0-929392-63-9.
- PCI System Architecture, Tom Shanley and Don Anderson, Addison-Wesley, 2000, ISBN 0-201-30974-2.

28.2 General PC Architecture

- Embedded PCs, Markt&Technik GmbH, ISBN 3-8272-5314-4 (German)
- Hardware Bible, Winn L. Rosch, SAMS, 1997, 0-672-30954-8
- Interfacing to the IBM Personal Computer, Second Edition, Lewis C. Eggebrecht, SAMS, 1990, ISBN 0-672-22722-3
- The Indispensable PC Hardware Book, Hans-Peter Messmer, Addison-Wesley, 1994, ISBN 0-201-62424-9
- The PC Handbook: For Engineers, Programmers, and Other Serious PC Users, John P. Choisser and John O. Foster, Annabooks, 1997, ISBN 0-929392-36-1

28.3 Ports

28.3.1 RS-232 Serial

- EIA-232-E standard
- The EIA-232-E standard specifies the interface between (for example) a modem and a computer so that they can exchange data. The computer can then send data to the modem, which then sends the data over a telephone line. The data that the modem receives from the telephone line can then be sent to the computer. You can search for information about the standard on the Web.
- RS-232 Made Easy: Connecting Computers, Printers, Terminals, and Modems, Martin D. Seyer, Prentice Hall, 1991, ISBN 0-13-749854-3
- National Semiconductor
- The Interface Data Book includes application notes. Type “232” as a search criteria to obtain a list of application notes. You can search for information about the data book on National Semiconductor’s Web site.

28.3.2 ATA

AT Attachment (ATA) Working Group.

This X3T10 standard defines an integrated bus interface between disk drives and host processors. It provides a common point of attachment for systems manufacturers and the system. You can search for information about the working group on the Web.

We recommend you also search the Web for information on 4.2 I/O cable, if you use hard disks in a DMA3 or PIO4 mode.

28.3.3 USB

USB Specification

USB Implementers Forum, Inc. is a non-profit corporation founded by the group of companies that developed the Universal Serial Bus specification. The USB-IF was formed to provide a support organization and forum for the advancement and adoption of Universal Serial Bus technology. You can search for information about the standard on the Web.

28.4 Programming

- C Programmer’s Guide to Serial Communications, Second Edition, Joe Campbell, SAMS, 1987, ISBN 0-672-22584-0
- Programmer's Guide to the EGA, VGA, and Super VGA Cards, Third Edition, Richard Ferraro, Addison-Wesley, 1990, ISBN 0-201-57025-4
- The Programmer’s PC Sourcebook, Second Edition, Thom Hogan, Microsoft Press, 1991, ISBN 1-55615-321-X
- Undocumented PC, A Programmer’s Guide to I/O, CPUs, and Fixed Memory Areas, Frank van Gilluwe, Second Edition, Addison-Wesley, 1997, ISBN 0-201-47950-8

29 Appendix G: Document Revision History

Version	Date	Edited by	Changes
EPBAM110	25.04.2006	BAJ	Official release.
EPBAM111	03.04.2007	SMI	Update of Chapter 19.1 .
EPBAM112	30.07.2007	SMI	Updated Hyperlinks
EPBAM113	17.12.2007 29.02.2008	GUL ZDA	Updated to current Kontron Layout Released for web
EPBAM114	10.04.2008	ZDA	Ethernet restriction
EPBAM115	30.04.2008	ZDA	Memory RAM restriction
EPBAM116	22.08.2008	ZDA	Spread Spectrum option