» Kontron User's Guide «



ETXexpress®-PC-XT

Document Revision: v 1.4

» Table of Contents «

1 User Information 1

1.1 About This Document 1

1.2 Copyright Notice 1

1.3 Trademarks 1

1.4 Standards 1

1.5 Warranty 1

1.6 Technical Support 2

2 Introduction 3

2.1 ETXexpress®-PC-XT 3

2.2 Naming clarification 3

2.3 Understanding ETXexpress®-PC-XT functionality 3

2.4 COM Express™ Documentation 4

2.5 COM Express™ Benefits 4

3 Specification 6

3.1 Available modules of ETXexpress-PC-XT® 6

3.2 Functional Specification 6

3.3 Block Diagram 8

3.4 Meachnical Specification 8

3.5 Electical Specification 8

3.5.1 Supply Voltage 8

3.5.2 Supply Current (Windows XP SP3) 9

3.6 Environmental Specification 10

3.7 MTBF 10

4 ETXexpress®-PC-XT Connectors 12

4.1 Connector Locations 12

4.2 Pin-out List 13

4.3 Connector Pin-out 14
4.3.1 Connector X1A (Signal Levels A1-A55) 14
4.3.2 Connector X1A (Signal Levels A56-A110) 15
4.3.3 Connector X1A (Signal Levels B1-B55) 18
4.3.4 Connector X1A (Signal Levels B56-B110) 20
4.3.5 Connector X1B (Signal Levels C1-C55) 22
4.3.6 Connector X1B (Signal Levels C56-C110) 23
4.3.7 Connector X1B (Signal Levels D1-D55) 25
4.3.8 Connector X1B (Signal Levels D56-D110) 26
4.4 Alternative pinout of HDMI 28
4.5 Alternative Pinout of Display Port 29
4.6 Signal Description 30
4.6.1 PCI Express x1 lanes 30
4.6.2 USB 30
4.6.3 SATA 30
4.6.4 Audio 30
4.6.5 Serial IRQ 31
4.6.6 VGA Output 31
4.6.7 LVDS Flat Panel Interface (JILI) 31
4.6.8 PCIexpress Graphics 31
4.6.9 SDVO 31
4.6.10 HDMI 32
4.6.11 Displayport 32
4.6.12 Ethernet 32
4.6.13 Power Control 32
4.6.14 Power Management 32
4.6.15 Miscellaneous Circuits 33
4.6.16 PCI Bus 33
4.6.17 IDE Port 34

5 Special Features 35

5.1 S5 Eco Mode 35
5.2 GPIO - General Purpose Input and Output 36
5.3 Usage of Different Graphic interfaces 37
5.3.1 Available Graphic interfaces 37
5.4 Speedstep Technology 38
5.5 Flash Backup Feature 40

5.6 Dynamic FSB Frequency Switching 41
5.7 Enhanced Intel Dynamic Acceleration Technology 41
5.8 VID-x 42

6 Design Consideration 43

6.1 Module Drill Hole Dimension 43
6.1.1 38011-XXXX-XX-X 43
6.2 Thermal Management 44
6.3 Heatspreader Dimension 44
6.4 ETXexpress®-PC-XT onboard fan connector 44
6.4.1 Location and pin-out of fan connector 45
6.4.2 BIOS settings for fan control 45
6.4.3 Electrical Characteristics 46

7 System Resources 48

7.1 Interrupt Request lines 48
7.1.1 In 8259 PIC mode 48
7.1.2 In APIC mode 49
7.2 Direct Memory Access (DMA) Channels 50
7.3 Memory Area 50
7.4 I/O Address Map 50
7.5 External Inter-IC (I2C) Bus 50
7.6 System Management (SM) Bus 50
7.7 JILI-I2C Bus 51
7.8 SDVO-I2C Bus 51
7.9 CRT-I2C Bus 51
7.10 K-Station / JIDA32 resources 51
7.10.1 I2C 51
7.10.2 Storage 51
7.10.3 GPIO 51
7.10.4 Hardware Monitor 52

8 BIOS Operation 53

8.1 Determining the BIOS Version 53

8.2 Setup Guide 53
8.2.1 Start AMI® BIOS Setup Utility 53
8.3 BIOS Setup 55
8.3.1 Main Menu 55
8.3.2 Module Info 55
8.3.3 Advanced Menu 59
8.3.4 PCIPnP Menu 87
8.3.5 Boot 88
8.3.6 Security 90
8.3.7 Chipset 91
8.3.8 Exit Menu 97
9 Appendix A: JIDA Standard 98
9.1 JIDA Information 98
10 Appendix B: Architecture Information 99
10.1 Buses 99
10.1.1 ISA, Standard PS/2 – Connectors 99
10.1.2 PCI/104 99
10.2 General PC Architecture 99
10.3 Ports 100
10.3.1 RS-232 Serial 100
10.3.2 Serial ATA 100
10.3.3 USB 100
10.4 Programming 100
11 Appendix C: Document Revision History 101

1 User Information

1.1 About This Document

This document provides information about products from Kontron and/or its subsidiaries. No warranty of suitability, purpose, or fitness is implied. While every attempt has been made to ensure that the information in this document is accurate, the information contained within is supplied “as-is” and is subject to change without notice.

For the circuits, descriptions and tables indicated, Kontron assumes no responsibility as far as patents or other rights of third parties are concerned.

1.2 Copyright Notice

Copyright © 2003-2009 Kontron

All rights reserved. No part of this document may be reproduced, transmitted, transcribed, stored in a retrieval system, or translated into any language or computer language, in any form or by any means (electronic, mechanical, photocopying, recording, or otherwise), without the express written permission of Kontron.

DIMM-PC®, PISA®, ETX®, ETXexpress®, microETXexpress™, X-board®, DIMM-IO® and DIMM-BUS® are trademarks or registered trademarks of Kontron. Kontron is trademark or registered trademark of Kontron AG.

1.3 Trademarks

The following lists the trademarks of components used in this board.

- IBM, XT, AT, PS/2 and Personal System/2 are trademarks of International Business Machines Corp.
- Microsoft is a registered trademark of Microsoft Corp.
- Intel is a registered trademark of Intel Corp.
- All other products and trademarks mentioned in this manual are trademarks of their respective owners.

1.4 Standards

Kontron is certified to ISO 9000 standards.

1.5 Warranty

This Kontron product is warranted against defects in material and workmanship for the warranty period from the date of shipment. During the warranty period, Kontron will at its discretion decide to repair or replace defective products.

Within the warranty period, the repair of products is free of charge as long as warranty conditions are observed.

The warranty does not apply to defects resulting from improper or inadequate maintenance or handling by the buyer, unauthorized modification or misuse, operation outside of the product's environmental specifications or improper installation or maintenance.

Kontron will not be responsible for any defects or damages to other products not supplied by Kontron that are caused by a faulty Kontron product.

1.6 Technical Support

Technicians and engineers from Kontron and/or its subsidiaries are available for technical support. We are committed to making our product easy to use and will help you use our products in your systems.

Please consult our Web site at http://www.kontron.com/support for the latest product documentation, utilities, drivers and support contacts. Consult our customer section http://emdcustomersection.kontron.com for the latest BIOS downloads, Product Change Notifications and additional tools and software. In any case you can always contact your board supplier for technical support.

2 Introduction

2.1 ETXexpress®-PC-XT

The ETXexpress®-PC-XT module unifies the 45 nm generations of Intel® Core™ 2 Duo processors with the new SSE4 instruction set and the chipset Intel® GS45, GM45 and GL40. This combination really sets new standards in many terms: more performance than ever on COM Express™ form factor, outstanding performance-power-ratio, fast DDR3 SO-DIMM memory up to 8 GB and L2 cache up to 6 MB, the module really opens up new application fields.

ETXexpress®-PC-XT is available with Intel® small form factor package: for instance, the ICH9M was shrunk from 961 mm² to 256 mm². Thus, valuable space for further features is gained: among others two stacked SO-DIMM sockets for dual channel memory. On top of that, Intel® small form factor package processors allow operations in ultra low voltage for best energy-efficiency. The bigger Intel® performance package offer high performance for bargain pricing.

Especially, its 4 Serial ATA ports and the native RAID support establish the ETXexpress®-PC-XT perfectly for heavy data sensitive applications. On top of all that, DirectX® 10 supports Windows Vista® perfectly.

Like all Kontron ETXexpress® modules, it is strictly compliant to the COM Express™ standard. Therefore, upgrading existing carrier boards gets so easy and minimizes redesign efforts.

2.2 Naming clarification

COM Express™ defines a Computer-On-Module, or COM, with all components necessary for a bootable host computer, packaged as a super component. Interfaces will provide a smooth transition path from legacy parallel interfaces to LVDS (Low Voltage Differential Signaling) interfaces. These include the PCI bus and parallel ATA and PCI Express and Serial ATA.

- » ETXexpress® modules are Kontron's COM Express™ modules in basic form factor (125mm x 95mm)
- » microETXexpress® modules are Kontron's COM Express™ modules in compact form factor (95mm x 95mm)
- » nanoETXexpress modules are Kontron's COM Express™ modules in the future ultra form factor (55mm x 84mm)

2.3 Understanding ETXexpress®-PC-XT functionality

All Kontron ETXexpress® and microETXexpress® modules contain two connectors; each of it has two rows. The primary connector has two rows called Row A and Row B. The secondary connector has two rows called Row C and Row D.

The primary connector (Row A and Row B) feature the following legacy-free functionality:

- » Ethernet
- » Serial ATA (SATA)

- USB 2.0
- LVDS/VGA and dual display video
- Intel High Definition Audio (Azalia)
- LPC (low pin count) Bus

The secondary connector (Row C and Row D) provides support for the following buses and I/O:

- PCI Express
- PCI
- IDE

2.4 COM Express™ Documentation

This product manual serves as one of three principal references for a COM Express™ design. It documents the specifications and features of ETXexpress®-PC-XT. The other two references, which are available from your Kontron Support or from PICMG®, include:

- The COM Express Specification defines the COM Express™ module form factor, pinout, and signals. This document is available from the PIGMG website by filling out the order form.
- The COM Express™ Design Guide by PICMG serves as a general guide for baseboard design, with a focus on maximum flexibility to accommodate a wide range of COM Express™ modules.

Note:	Some of the information contained within this product manual applies only to certain product revisions (CE: xxx). If certain information applies to specific product revisions (CE: xxx) it will be stated. Please check the product revision of your module to see if this information is applicable.

2.5 COM Express™ Benefits

Computer on modules express (COM Express) modules in compact formfactor are very compact (95 x 95 mm, 12mm thick), highly integrated computers. All (micro)ETXexpress® modules feature a standardized form factor and a standardized connector layout that carry a specified set of signals. Each microETXexpress® module is based on connector type 2 of the COM Express specification. This standardization allows designers to create a single-system baseboard that can accept present and future (micro)ETXexpress® modules.

microETXexpress® modules include common personal computer (PC) peripheral functions such as:

- Graphics
- USB ports
- Ethernet
- Sound
- IDE (and SATA)

The baseboard designer can optimize exactly how each of these functions implements physically. Designers can place connectors precisely where needed for the application on a baseboard designed to optimally fit a system's packaging.

A peripheral PCI bus can be implemented directly on the baseboard rather than on mechanically unwieldy expansion cards. The ability to build a system on a single baseboard using the computer as one plug-in component simplifies packaging, eliminates cabling, and significantly reduces system-level cost.

A single baseboard design can use a range of ETXexpress®, microETXexpress® and nanoETXexpress modules. This flexibility can differentiate products at various price/performance points, or to design future proof systems that have a built-in upgrade path. The modularity of a COM Express™ solution also ensures against obsolescence as computer technology evolves. A properly designed COM Express™ baseboard can work with several successive generations of COM Express® modules.

A COM Express™ baseboard design has many advantages of a custom, computer-board design but delivers better obsolescence protection, greatly reduced engineering effort, and faster time to market.

3 Specification

3.1 Available modules of ETXexpress-PC-XT®

ETXexpress-PC-XT® is available in different variants to cover the demand of different performance, price and power. The following table shows the different combinations of ETXexpress-PC-XT®

Article Number	Processor	MCH	IO Controller
38011-0000-12-1	Celeron® M722	GS45	ICH9M-SFF
38011-0000-12-2	SU9300	GS45	ICH9M-SFF
38011-0000-19-2	SL9400	GS45	ICH9M-SFF

3.2 Functional Specification

Processor: Intel® Core2Duo, Celeron® (Penryn)

Processor	Number of Cores	Core	Processor Base Frequency	L2 Cache	FSB Speed	VT-x	Trusted Execution	Intel® 64	EIST
Celeron® M722	1	45nm	1.2 GHz	3MB	800 MHz	No	No	Yes	No
SU9300	2	45nm	1.2 GHz	3MB	800 MHz	Yes	Yes	Yes	Yes
SL9400	2	45nm	1.86 GHz	6MB	1066 MHz	Yes	Yes	Yes	Yes

Chipset Memory Controler Hub: Intel® GS45

MCH	Supported FSB	PCIe x16	DVI, HDMI, Displayport
GS45	800 / 1066 MHz	Yes	Yes

Note: If only one RAM module is used, it must be plugged into the lower socket if it is a board with GS45. In any other case a single RAM module must be plugged in the upper RAM socket. Otherwise there might be issues with the management engine, which lead to several problems.

Chipset Southbridge: Intel® ICH9M-SFF

IO Controller	USB	5x PCIe x1 (x4 possible)	Intel® HDA	PCI Bus	iTPM
ICH9M-SFF	8x USB 1.1/2.0	Yes	Yes	32 bit/ 33 MHz / 4 devices	Yes

Integrated graphics: Intel® GMAX4500

- Graphics Memory: up to 1024 MByte
- Features: HDTV/HD capable, Decoder for MPEG2(HD) / H.264, DirectX®10.0, OpenGL 2.0,

Pixelshader 4.0

MCH	GPU Speed
GS45	320 / 533 MHz

Display Interfaces

- » CRT: maximum resolution up to QXGA (2048x1536)
- » Flat Panel: dual channel 18bit and 24bit (with dithering) up to UXGA (1600x1200)
- » Digital Display: 2 SDVO channels (muxed with PEG) supporting external SDVO components (HDMI, DVI,

  LVDS, TV-out)
- » DVI
- » HDMI
- » DisplayPort

Storage

- » SATA: 3 SATA ports up to 300 MB/s supporting NCQ, Hotplug, Staggered Spinup, eSATA, PortMultiplier

MCH	Raid 0	Raid 1	Raid 5	Raid 10	Matrix Raid
GS45	Yes	Yes	No	No	No

- » IDE: One Channel (master only) SATA2PATA Bridge (88SA8052)

Onboard Devices:

- » Ethernet:Intel® 82567 10/100/1000 Phy
- » TPM: TPM 1.2, integrated in IO Controller (not in ICH9M)
- » Watchdog: onboard CPLD with integrated Watchdog functionality

Additional Interfaces:

- » LPC: Yes
- » SMBus: Yes
- » I2C: Yes
- » GPIO: 8, Fixed to 4 GPI or 4 GPO via JIDA interface

Power Management & Misc

- » JIDA support: Yes
- » MARS support: Yes

» HWM: Temperature Monitoring for CPU and Board Temperature

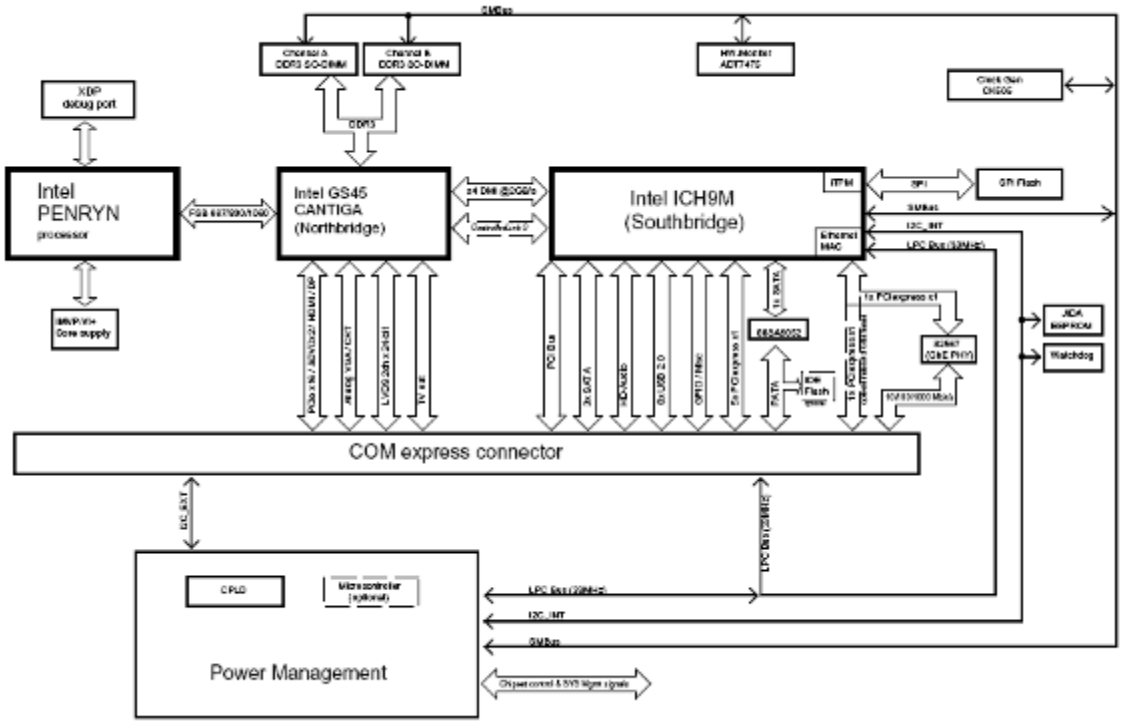
» Passive Cooling: Active, Passice and Critical Trip Point

» ACPI: ACPI 1.0 / 2.0 / 3.0

» S-States: S0, S3, S4, S5

» Input Voltage: Single supply support with wide range input 8.5 V - 18 V

3.3 Block Diagram



3.4 Meachnical Specification

» 95.0 mm x 125.0 mm

» Height approx. 12 mm (0.4”)

3.5 Electical Specification

3.5.1 Supply Voltage

» VCC: 12V DC +/- 5% or

» 8.5 V to 18 V DC in single supply mode

» 12V + 5VSB ±5% in ATX mode

Note:	It is not possible to use E2 rated boards with wide range input!

Note:	It is recommended to follow the ATX specification for voltage rise times which claims: "The output voltage shall rise from ≤ 10% of nominal to within the regulation ranges … within 0.1ms to 20ms".

Power Supply Risetime

» The input voltages shall rise from ≤10% of nominal to within the regulation ranges within 0.1ms to 20ms.

» There must be a smooth and continuous ramp of each DC input voltage from 10% to 90% of its final set-point following the ATX specification

Supply Voltage Ripple

» Maximum 100 mV peak to peak 0-20MHz

3.5.2 Supply Current (Windows XP SP3)

The tested boards were mounted on a Kontron Evaluation Board (Article number: 38100-0000-00-0), a mouse and a keyboard were connected. The Power-consumption tests were executed during Windows XP SP3 by using a tool to stress the CPU (100 % load). The power measurements values were acquired after 15 min full load and a stable CPU die temperature. To ensure a stable die temperature a corresponding heatsink was used to hold the temperature under the critical trip point.

All boards were equipped with 1024MB of memory. The Modules were tested using maximum CPU frequency.

ETXexpress®-PC-XT SL9400

Mode	[A] 12V	[A] 5VSB	[W]
Full Load	2.44	0.06	29.58
Idle	0.65	0.06	8.13
Standby S3	0.0	0.28	1.39
Soft Off S5	0.0	0.26	1.30

ETXexpress®-PC-XT SU9300

Mode	[A] 12V	[A] 5VSB	[W]
Full Load	1.40	0.06	17.10
Idle	0.62	0.06	7.78
Standby S3	0.0	0.28	1.42

Soft Off S5	0.0	0.27	1.37

ETXexpress®-PC-XT CM722

Mode	[A] 12V	[A] 5VSB	[W]
Full Load	1.09	0.06	13.32
Idle	0.63	0.06	7.89
Standby S3	0.0	0.28	1.40
Soft Off S5	0.0	0.26	1.28

3.6 Environmental Specification

Temperature

Operating: (with Kontron heat-spreader plate assembly):

- Ambient temperature: -40 to +85 °C
- Maximum heatspreader-plate temperature: -40 to +85 °C (*)

Non-operating: -40 to +85 °C

Note: *The maximum operating temperature with the heatspreader plate is the maximum measurable temperature on any spot on the heatspreader's surface. You must maintain the temperature according to the above specification.

Operating (without Kontron heat-spreader plate assembly):

- Maximum operating temperature: -40 to +85 °C (**)

Non operating: -40 to +85 °C

Note: **The maximum operating temperature is the maximum measurable temperature on any spot on a module's surface. You must maintain the temperature according to the above specification.

Humidity

- Operating: 10% to 90% (non condensing)
- Non operating: 5% to 95% (non condensing)

3.7 MTBF

The following MTBF (Mean Time Between Failure) values were calculated using a combination of manufacturer's test data, if the data was available, and a Bellcore calculation for the remaining parts. The Bellcore calculation used is "Method 1 Case 1". In that particular method the components are assumed to be operating at a 50 % stress level

in a 40° C ambient environment and the system is assumed to have not been burned in. Manufacturer's data has been used wherever possible. The manufacturer's data, when used, is specified at 50° C, so in that sense the following results are slightly conservative. The MTBF values shown below are for a 40° C in an office or telecommunications environment. Higher temperatures and other environmental stresses (extreme altitude, vibration, salt water exposure, etc.) lower MTBF values.

» System MTBF (hours) : 184428 @ 40°C

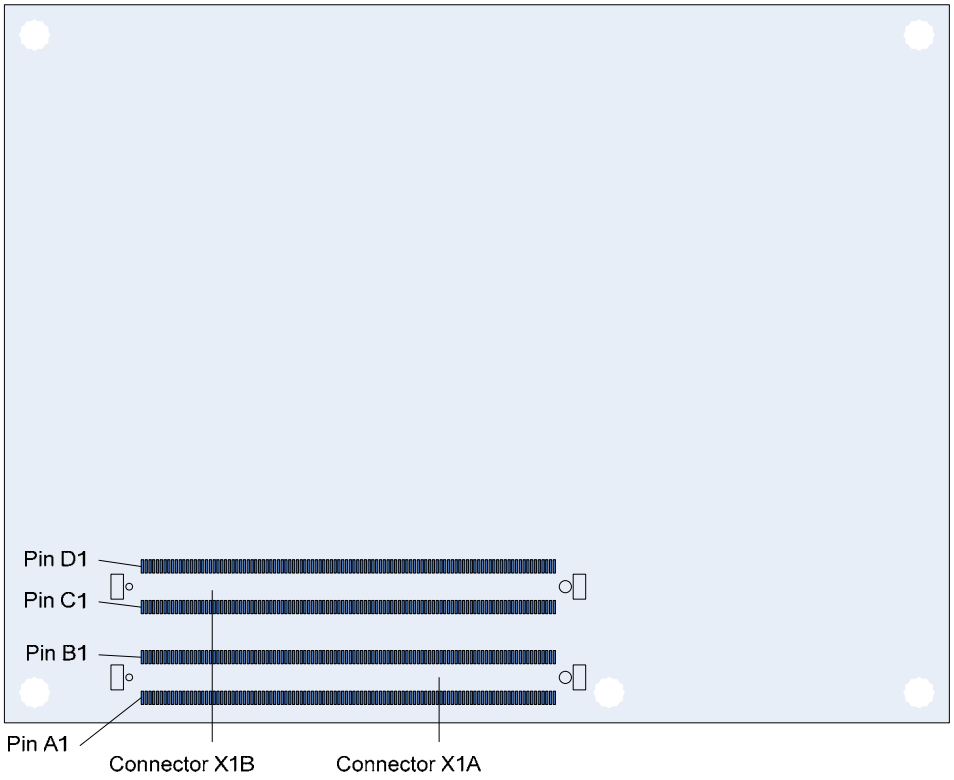
Notes: Fans usually shipped with Kontron products have 50,000-hour typical operating life. The above estimates assume no fan, but a passive heat sinking arrangement Estimated RTC battery life (as opposed to battery failures) is not accounted for in the above figures and need to be considered for separately. Battery life depends on both temperature and operating conditions. When the Kontron unit has external power; the only battery drain is from leakage paths.

4 ETXexpress®-PC-XT Connectors

4.1 Connector Locations

There are two connectors on the basic sized module. Connector X1A and Connector X1B are shown in the following drawing. It is a top layer view and the connectors are seen "through" the PCB.

Each connector consist s of two connector rows. Connector X1A has rows A and B and connector X1B has rows C and D.



4.2 Pin-out List

Type	Description
I/O-3.3	Bi-directional 3,3 V IO-Signal
I/O-5T	Bi-dir. 3,3V I/O (5V Tolerance)
I/O-5	Bi-directional 5V I/O-Signal
I-3,3	3,3V Input
I/OD	Bi-directional Input/Output Open Drain
I-5T	3,3V Input (5V Tolerance)
OA	Output Analog
OD	Output Open Drain
O-1.8	1,8V Output
O-3.3	3,3V Output
O-5	5V Output
DP-I/O	Differential Pair Input/Output
DP-I	Differential Pair Input
DP-O	Differential Pair Output
PU	Pull-Up Resistor
PD	Pull-Down Resistor
PWR	Power Connection

Notes: To protect external power lines of peripheral devices, make sure that: the wires have the right diameter to withstand the maximum available current the enclosure of the peripheral device fulfils the fire-protection requirements of IEC/EN60950

4.3 Connector Pin-out

4.3.1 Connector X1A (Signal Levels A1-A55)

Pin	Signal	Description	Type	Termination	Comment
A1	GND	Power Ground	PWR	-	-
A2	GBE0_MDI3-	GBE0_MDI3_N | Ethernet Receive Data -	DP-I	-	-
A3	GBE0_MDI3+	GBE0_MDI3_P | Ethernet Receive Data -	DP-I	-	-
A4	GBE0_LINK100#	GBE0_LINK100# | Ethernet Speed LED	O-3.3	-	-
A5	GBE0_LINK1000#	GBE0_LINK1000# | Ethernet Speed LED	O-3.3	-	-
A6	GBE0_MDI2-	GBE0_MDI2_N | Ethernet Receive Data	DP-I	-	-
A7	GBE0_MDI2+	GBE0_MDI2_P | Ethernet Receive Data -	DP-I	-	-
A8	GBE0_LINK#	GBE0_LINK# | LAN Link LED	OD	-	-
A9	GBE0_MDI1-	GBE0_MDI1_N | Ethernet Receive Data -	DP-I	-	-
A10	GBE0_MDI1+	GBE0_MDI1_P | Ethernet Receive Data +	DP-I	-	-
A11	GND	Power Ground	PWR	-	-
A12	GBE0_MDI0-	GBE0_MDI0_N | Ethernet Transmit Data -	DP-O	-	-
A13	GBE0_MDI0+	GBE0_MDI0_P | Ethernet Transmit Data +	DP-O	-	-
A14	GBE0_CTREF	GBE0_CTREF	O-1.8	-	on a power rail controlled by Intels ME
A15	SUS_S3#	PM_SLP_S3_EXT#	O-3.3	PU 10k 3,3V (S5)	-
A16	SATA0_TX+	SATA_TX0_P | SATA 0 Transmit Data +	DP-O	-	-
A17	SATA0_TX-	SATA_TX0_N | SATA 0 Transmit Data -	DP-O	-	-
A18	SUS_S4#	PM_SLP_S4_EXT#	O-3.3	-	-
A19	SATA0_RX+	SATA_RX0_P | SATA 0 Receive Data +	DP-I	-	-
A20	SATA0_RX-	SATA_RX0_N | SATA 0 Receive Data -	DP-I	-	-
A21	GND	Power Ground	PWR	-	-
A22	SATA2_TX+	SATA_TX2_P | SATA 2 Transmit Data +	DP-O	-	-
A23	SATA2_TX-	SATA_TX2_N | SATA 2 Transmit Data -	DP-O	-	-
A24	SUS_S5#	PM_SLP_S#5	O-3.3	-	-
A25	SATA2_RX+	SATA_RX2_P | SATA 2 Receive Data +	DP-I	-	-
A26	SATA2_RX-	SATA_RX2_N | SATA 2 Receive Data -	DP-I	-	-
A27	BATLOW#	PM_BATLOW# | Battery Low	I-3.3	PU 8k25 3,3V (S5)	-
A28	ATA_ACT#	ATA_LED# | SATA LED	O-3.3	PU 10k 3,3V (S0)	int. PU 15k in ICH9

A29	AC_SYNC	HDA_SYNC | HD Audio Sync	O-3.3	-	opt. for x4: PU 1k 3,3V(S0)
A30	AC_RST#	HDA_RST# | HD Audio Reset	O-3.3	-	int. PD 20k in ICH9
A31	GND	Power Ground	PWR	-	-
A32	AC_BITCLK	HDA_BITCLK | HD Audio Clock	O-3.3	int. PD 20k	active only in S3
A33	AC_SDOUT	HDA_SDOUT | HD Audio Data	O-3.3	int. PD 20k	=> PU 1k 3,3V(S0) for x4
A34	BIOS_DISABL	BIOS_DISABLE#	I-3.3	-	-
A35	THRMTRIP#	EXT_THRMTRIP#	O-3.3	PU 10k 3,3V (S0)	-
A36	USB6-	USB6_N | USB Data – Port6	DP-I/O	-	int. PD 15k in ICH9 | 5V tolerant
A37	USB6+	USB6_P | USB Data + Port6	DP-I/O	-	int. PD 15k in ICH9 | 5V tolerant
A38	USB_6_7_OC#	USB_67_OC# | USB OverCurrent Port 6/7	I-3.3	PU 10k 3,3V (S5)	-
A39	USB4-	USB4_N | USB Data - Port4	DP-I/O	-	int. PD 15k in ICH9 | 5V tolerant
A40	USB4+	USB4_P | USB Data + Port4	DP-I/O	-	int. PD 15k in ICH9 | 5V tolerant
A41	GND	Power Ground	PWR	-	-
A42	USB2-	USB2_N | USB Data - Port2	DP-I/O	-	int. PD 15k in ICH9 | 5V tolerant
A43	USB2+	USB2_P | USB Data + Port2	DP-I/O	-	int. PD 15k in ICH9 | 5V tolerant
A44	USB_2_3_OC#	USB_23_OC# | USB OverCurrent Port 2/3	I-3.3	PU 10k 3,3V (S5)	-
A45	USB0-	USB0_N | USB Data - Port0	DP-I/O	-	int. PD 15k in ICH9 | 5V tolerant
A46	USB0+	USB0_P | USB Data + Port0	DP-I/O	-	int. PD 15k in ICH9 | 5V tolerant
A47	VCC_RTC	V_BAT	PWR 3V	-	-
A48	EXCD0_PERST#	EXCD0_PERST#|Express card reset	O-3.3	-	-
A49	EXCD0_CPPE#	EXCD0_CPPE#| capable c. request	I-3.3	PU 10k 3,3V (S5)	-
A50	LPC_SERIRQ	LPC_SERIRQ | Serial Interrupt Request	IO-3.3	PU 10k 3,3V (S0)	-
A51	GND	Power Ground	PWR	-	-
A52	PCIE_TX5+	opt. PCI Express lane 5 + Transmit	Nc	-	just available if no GbEthernet PHY
A53	PCIE_TX5-	opt. PCI Express lane 5 - Transmit	Nc	-	just available if no GbEthernet PHY
A54	GPI0	EXT_GPI0 | General Purpose Input 0	I-3.3	PU 10k 3,3V (S0)	-
A55	PCIE_TX4+	PCI Express lane 4 + Transmit	DP-O	-	-

4.3.2 Connector X1A (Signal Levels A56-A110)

Pin	Signal	Description	Type	Termination	Comment
A56	PCIE_TX4-	PCI Express lane 4 - Transmit	DP-O	-	-
A57	GND	Power Ground	PWR	-	-
A58	PCIE_TX3+	PCI Express lane 3 + Transmit	DP-O	-	-
A59	PCIE_TX3-	PCI Express lane 3 - Transmit	DP-O	-	-

A60	GND	Power Ground	PWR	-	-
A61	PCIE_TX2+	PCI Express lane 2 + Transmit	DP-O	-	-
A62	PCIE_TX2-	PCI Express lane 2 - Transmit	DP-O	-	-
A63	GPI1	EXT_GPI1 | General Purpose Input 1	I-3.3	PU 10k 3,3V (S0)	-
A64	PCIE_TX1+	PCI Express lane 1 + Transmit	DP-O	-	-
A65	PCIE_TX1-	PCI Express lane 1 - Transmit	DP-O	-	-
A66	GND	Power Ground	PWR	-	-
A67	GPI2	EXT_GPI2 | General Purpose Input 2	I-3.3	PU 10k 3,3V (S0)	-
A68	PCIE_TX0+	PCI Express lane 0 + Transmit	DP-O	-	-
A69	PCIE_TX0-	PCI Express lane 0 - Transmit	DP-O	-	-
A70	GND	Power Ground	PWR	-	-
A71	LVDS_A0+	LVDS_A_DATA0_P | LVDS Channel A Data0+	DP-O	-	-
A72	LVDS_A0-	LVDS_A_DATA0_N | LVDS Channel A Data0-	DP-O	-	-
A73	LVDS_A1+	LVDS_A_DATA1_P | LVDS Channel A Data1+	DP-O	-	-
A74	LVDS_A1-	LVDS_A_DATA1_N | LVDS Channel A Data1-	DP-O	-	-
A75	LVDS_A2+	LVDS_A_DATA2_P| LVDS Channel A Data2+	DP-O	-	-
A76	LVDS_A2-	LVDS_A_DATA2_N | LVDS Channel A Data2 -	DP-O	-	-
A77	LVDS_VDD_EN	LVDS_VDD_EN | LVDS Panel Power Control	O-3.3	PD 100k	-
A78	LVDS_A3+	LVDS_A_DATA3_P | LVDS Channel A Data3+	DP-O	-	-
A79	LVDS_A3-	LVDS_A_DATA3_N | LVDS Channel A Data3-	DP-O	-	-
A80	GND	Power Ground	PWR	-	-
A81	LVDS_A_CK+	LVDS_A_CLK_P | LVDS Channel A Clock+	DP-O	-	-
A82	LVDS_A_CK-	LVDS_A_CLK_N | LVDS Channel A Clock-	DP-O	-	-
A83	LVDS_I2C_CK	LVDS_DDC_CLK | JILI I2C Clock	I/O-3.3	PU 2k21 3,3V (s0)	-
A84	LVDS_I2C_DAT	LVDS_DDC_DATA | JILI I2C Data	I/O-3.3	PU 2k21 3,3V (s0)	-
A85	GPI3	EXT_GPI3 | General Purpose Input 3	I-3.3	PU 10k 3,3V (S0)	-
A86	KBD_RST#	KBD_RST# | Keyboard Reset	I-3.3	PU 10k 3,3V (S0)	-
A87	KBD_A20GATE	KBD_A20GATE	I-3.3	PU 10k 3,3V (S0)	-
A88	PCIE0_CK_REF+	CLK_PCIE_CON_P	DP-O	-	-
A89	PCIE0_CK_REF-	CLK_PCIE_CON_N	DP-O	-	-
A90	GND	Power Ground	PWR	-	-
A91	RSVD	n.c.	Nc	-	-
A92	RSVD	n.c.	Nc	-	-

A93	GPO0	EXT_GPO0 | General Purpose Output 0	O-3.3	PD 10k	-
A94	RSVD	n.c.	Nc	-	-
A95	RSVD	n.c.	Nc	-	
A96	GND	Power Ground	PWR	-	-
A97	VCC_12V	12V VCC	PWR 8.5-	-	-
A98	VCC_12V	12V VCC	PWR 8.5-	-	-
A99	VCC_12V	12V VCC	PWR 8.5-	-	-
A100	GND	Power Ground	PWR	-	-
A101	VCC_12V	12V VCC	PWR 8.5-	-	-
A102	VCC_12V	12V VCC	PWR 8.5-	-	-
A103	VCC_12V	12V VCC	PWR 8.5-	-	-
A104	VCC_12V	12V VCC	PWR 8.5-	-	-
A105	VCC_12V	12V VCC	PWR 8.5-	-	-
A106	VCC_12V	12V VCC	PWR 8.5-	-	-
A107	VCC_12V	12V VCC	PWR 8.5-	-	-
A108	VCC_12V	12V VCC	PWR 8.5-	-	-
A109	VCC_12V	12V VCC	PWR 8.5-	-	-
A110	GND	Power Ground	PWR	-	-

4.3.3 Connector X1A (Signal Levels B1-B55)

Pin	Signal	Description	Type	Termination	Comment
B1	GND	Power Ground	PWR	-	-
B2	GBE0_ACT	Ethernet Activity LED	O-3.3	-	-
B3	LPC_FRAME#	LPC_FRAME# | LPC Frame Indicator	I-3.3	-	-
B4	LPC_AD0	LPC_AD0 | LPC Adress & DATA Bus	I/O-3.3	-	int. PU 20k in ICH9
B5	LPC_AD1	LPC_AD1 | LPC Adress & DATA Bus	I/O-3.3	-	int. PU 20k in ICH9
B6	LPC_AD2	LPC_AD2 | LPC Adress & DATA Bus	I/O-3.3	-	int. PU 20k in ICH9
B7	LPC_AD3	LPC_AD3 | LPC Adress & DATA Bus	I/O-3.3	-	int. PU 20k in ICH9
B8	LPC_DRQ0#	LPC_DRQ#0 | LPC Request 0	I-3.3	PU 10k 3,3V (S0)	int. PU 20k in ICH9
B9	LPC_DRQ1#	LPC_DRQ#1 | LPC Request 1	I-3.3	PU 10k 3,3V (S0)	int. PU 20k in ICH10
B10	LPC_CLK	CLK_LPC_33M_EXT |33MHz LPC clock	O-3.3	-	-
B11	GND	Power Ground	PWR	-	-
B12	PWRBTN#	EXT_PWRBTN# | Power Button	I-3.3	PU 20k 3,3V (S5)	-
B13	SMB_CK	SMB_CLK_EXT | SMBUS Clock	O-3.3	PU 2k2 3,3V (S5)	-
B14	SMB_DAT	SMB_DATA_EXT | SMBUS Data	IO-3.3	PU 2k2 3,3V (S5)	-
B15	SMB_ALERT#	SMB_ALERT# | SMBUS Interrupt	IO-3.3	PU 1k0 3,3V (S5)	-
B16	SATA1_TX+	SATA_TX1_P | SATA 1 Transmit Data +	DP-O	-	-
B17	SATA1_TX-	SATA_TX1_N | SATA 1 Transmit Data -	DP-O	-	-
B18	SUS_STAT#	PM_SUS_STAT#	O-3.3	-	-
B19	SATA1_RX+	SATA_RX1_P | SATA 1 Receive Data +	DP-I	-	-
B20	SATA1_RX-	SATA_RX1_N | SATA 1 Receive Data -	DP-I	-	-
B21	GND	Power Ground	PWR	-	-
B22	SATA3_TX+	Not Connected	n.c.	-	Not supported
B23	SATA3_TX-	Not Connected	n.c.	-	Not supported
B24	PWR_OK	EXT_PWR_OK | Power OK	I-3.3	-	-
B25	SATA3_RX+	Not Connected	n.c.	-	Not supported
B26	SATA3_RX-	Not Connected	n.c.	-	Not supported
B27	WDT	WDT | Watch Dog Timer	O-3.3	-	-
B28	AC_SDIN2	HDA_SDIN2_ICH| HD Audio Serial Input Data 2	I-3.3	-	int. PD 20k in ICH9
B29	AC_SDIN1	HDA_SDIN1_ICH| HD Audio Serial Input Data 1	I-3.3	-	int. PD 20k in ICH9

B30	AC_SDIN0	HDA_SDIN0_ICH| HD Audio Serial Input Data 0	I-3.3	-	int. PD 20k in ICH9
B31	GND	Power Ground	PWR	-	-
B32	SPKR	HDA_SPKR | Speaker	O-3.3	-	int. PD 20k in ICH9
B33	I2C_CK	I2C_CLK_EXT | I2C clock	O-3.3	PU 2k21 3,3V (S0)	-
B34	I2C_DAT	I2C_DATA_EXT | I2C data	I/O-3.3	PU 2k21 3,3V (S0)	-
B35	THRM#	PM_THRM# | Over Temperature	I-3.3	PU 8k25 3,3V (S0)	-
B36	USB7-	USB7_N | USB Data – Port7	DP-I/O	-	int. PD 15k in ICH9 | 5V tolerant
B37	USB7+	USB7_P | USB Data + Port7	DP-I/O	-	int. PD 15k in ICH9 | 5V tolerant
B38	USB_4_5_OC#	USB_45_OC# | USB OverCurrent Port 4/5	I-3.3	PU 10k 3,3V (S5)	-
B39	USB5-	USB5_N | USB Data – Port5	DP-I/O	-	int. PD 15k in ICH9 | 5V tolerant
B40	USB5+	USB5_P | USB Data + Port5	DP-I/O	-	int. PD 15k in ICH9 | 5V tolerant
B41	GND	Power Ground	PWR	-	-
B42	USB3-	USB3_N | USB Data – Port3	DP-I/O	-	int. PD 15k in ICH9 | 5V tolerant
B43	USB3+	USB3_P | USB Data + Port3	DP-I/O	-	int. PD 15k in ICH9 | 5V tolerant
B44	USB_0_1_OC#	USB_01_OC# | USB OverCurrent Port 0/1	I-3.3	PU 10k 3,3V (S5)	-
B45	USB1-	USB1_N | USB Data – Port1	DP-I/O	-	int. PD 15k in ICH9 | 5V tolerant
B46	USB1+	USB1_P | USB Data + Port1	DP-I/O	-	int. PD 15k in ICH9 | 5V tolerant
B47	EXCD1_PERST#	EXCD1_PERST# | Express card reset	O-3.3	-	-
B48	EXCD1_CPPE#	EXCD1_CPPE# | capable c. request	I-3.3	PU 10k 3,3V (S5)	-
B49	SYS_RESET#	EXT_SYS_RESET# | Reset Input	I-3.3	PU 10k 3,3V (S5)	-
B50	CB_RESET#	CB_RESET# | Carrier board Reset	O-3.3	-	-
B51	GND	Power Ground	PWR	-	-
B52	PCIE_RX5+	opt. PCI Express lane 5 + Recieve	Nc	-	just available if no GB Phy
B53	PCIE_RX5-	opt. PCI Express lane 5 - Recieve	Nc	-	just available if no GB Phy
B54	GPO1	EXT_GPO1 | General Purpose Output 1	O-3.3	PD 10k	-
B55	PCIE_RX4+	PCI Express lane 4 + Recieve	DP-I	-	-

4.3.4 Connector X1A (Signal Levels B56-B110)

Pin	Signal	Description	Type	Termination	Comment
B56	PCIE_RX4-	PCI Express lane 4 - Recieve	DP-I	-	-
B57	GPO2	EXT_GPO2 | General Purpose Output 2	O-3.3	PD 10k	-
B58	PCIE_RX3+	PCI Express lane 3 + Recieve	DP-I	-	-
B59	PCIE_RX3-	PCI Express lane 3 - Recieve	DP-I	-	-
B60	GND	Power Ground	PWR	-	-
B61	PCIE_RX2+	PCI Express lane 2 + Recieve	DP-I	-	-
B62	PCIE_RX2-	PCI Express lane 2 - Recieve	DP-I	-	-
B63	GPO3	EXT_GPO3 | General Purpose Output 3	O-3.3	PD 10k	-
B64	PCIE_RX1+	PCI Express lane 1 + Recieve	DP-I	-	-
B65	PCIE_RX1-	PCI Express lane 1 - Recieve	DP-I	-	-
B66	WAKE0#	PCIE_WAKE#	IO-3.3	PU 1k0 3,3V	-
B67	WAKE1#	WAKE1#	I-3.3	PU 10k 3,3V	-
B68	PCIE_RX0+	PCI Express lane 0 + Recieve	DP-I	-	-
B69	PCIE_RX0-	PCI Express lane 0 - Recieve	DP-I	-	-
B70	GND	Power Ground	PWR	-	-
B71	LVDS_B0+	LVDS_B_DATA0_P | LVDS Channel B Data0+	DP-O	-	-
B72	LVDS_B0-	LVDS_B_DATA0_N | LVDS Channel B Data0-	DP-O	-	-
B73	LVDS_B1+	LVDS_B_DATA1_P | LVDS Channel B Data1+	DP-O	-	-
B74	LVDS_B1-	LVDS_B_DATA1_N | LVDS Channel B Data1-	DP-O	-	-
B75	LVDS_B2+	LVDS_B_DATA2_P| LVDS Channel B Data2+	DP-O	-	-
B76	LVDS_B2-	LVDS_B_DATA2_N | LVDS Channel B Data2 -	DP-O	-	-
B77	LVDS_B3+	LVDS_B_DATA3_P | LVDS Channel B Data3+	DP-O	-	-
B78	LVDS_B3-	LVDS_B_DATA3_N | LVDS Channel B Data3-	DP-O	-	-
B79	LVDS_BKLT_EN	LVDS_BKLT_CTRL | Panel Backlight ON	O-3.3	PD 100k	-
B80	GND	Power Ground	PWR	-	-
B81	LVDS_B_CK+	LVDS_B_CLK_P | LVDS Channel B Clock+	DP-O	-	-
B82	LVDS_B_CK-	LVDS_B_CLK_N | LVDS Channel B Clock-	DP-O	-	-
B83	LVDS_BKLT_CTRL	LVDS_BKLT_CTRL | Backlight Brightness Contr.	O-3.3	-	-
B84	VCC_5V_SBY	+V_STBY_ETX | 5V Standby	PWR 5V	-	-
B85	VCC_5V_SBY	+V_STBY_ETX | 5V Standby	PWR 5V	-	-
B86	VCC_5V_SBY	+V_STBY_ETX | 5V Standby	PWR 5V	-	-
B87	VCC_5V_SBY	+V_STBY_ETX | 5V Standby	PWR 5V	-	-

B88	RSVD	n.c.	nc	-	-
B89	VGA_RED	CRT_RED | Analog Video RGB-RED	OA	PD 150R	-
B90	GND	Power Ground	PWR	-	-
B91	VGA_GRN	CRT_GREEN | Analog Video RGB-GREEN	OA	PD 150R	-
B92	VGA_BLU	CRT_BLUE | Analog Video RGB-BLUE	OA	PD 150R	-
B93	VGA_HSYNC	CRT_HSYNC | Analog Video H-Sync	O-3.3	-	-
B94	VGA_VSYNC	CRT_VSYNC | Analog Video V-Sync	O-3.3	-	-
B95	VGA_I2C_CK	CRT_DDC_CLK | Display Data Channel Clock	I/O-5	PU 2k21 5V (S0)	-
B96	VGA_I2C_DAT	CRT_DDC_DATA | Display Data Channel Data	I/O-5	PU 2k21 5V (S0)	-
B97	TV_DAC_A	TV_DACA_CVBS | Composite CVBS	OA	PD 150R	-
B98	TV_DAC_B	TV_DADB_Y | TV Luminance Signal	OA	PD 150R	-
B99	TV_DAC_C	TV_DADC_C | TV Chrominance Signal	OA	PD 150R	-
B100	GND	Power Ground	PWR	-	-
B101	VCC_12V	12V VCC	PWR 8.5-18V	-	-
B102	VCC_12V	12V VCC	PWR 8.5-18V	-	-
B103	VCC_12V	12V VCC	PWR 8.5-18V	-	-
B104	VCC_12V	12V VCC	PWR 8.5-18V	-	-
B105	VCC_12V	12V VCC	PWR 8.5-18V	-	-
B106	VCC_12V	12V VCC	PWR 8.5-18V	-	-
B107	VCC_12V	12V VCC	PWR 8.5-18V	-	-
B108	VCC_12V	12V VCC	PWR 8.5-18V	-	-
B109	VCC_12V	12V VCC	PWR 8.5-18V	-	-
B110	GND	Power Ground	PWR	-	-

4.3.5 Connector X1B (Signal Levels C1-C55)

Pin	Signal	Description	Type	Termination	Comment
C1	GND	Power Ground	PWR	-	-
C2	IDE_D7	IDE Data Bus	I/O-5T	PD 10k	-
C3	IDE_D6	IDE Data Bus	I/O-5T	-	-
C4	IDE_D3	IDE Data Bus	I/O-5T	-	-
C5	IDE_D15	IDE Data Bus	I/O-5T	-	-
C6	IDE_D8	IDE Data Bus	I/O-5T	-	-
C7	IDE_D9	IDE Data Bus	I/O-5T	-	-
C8	IDE_D2	IDE Data Bus	I/O-5T	-	-
C9	IDE_D13	IDE Data Bus	I/O-5T	-	-
C10	IDE_D1	IDE Data Bus	I/O-5T	-	-
C11	GND	Power Ground	PWR	-	-
C12	IDE_D14	IDE Data Bus	I/O-5T	-	-
C13	IDE_IORDY	IDE I/O Ready	I/O-5T	PU 4k7 3,3V (S0)	-
C14	IDE_IOR#	IDE I/O Read	I/O-3.3	-	-
C15	PCI_PME#	PCI Power Management Event	I/O-3.3	-	int. PU 20k in ICH9
C16	PCI_GNT2#	PCI Bus Grant 2	O-3.3	-	int. PU 20k in ICH9 (if PCIRST#=0 AND PWROK=1)
C17	PCI_REQ2#	PCI Bus Request 2	I-5T	PU 8k2 3,3V (S0)	-
C18	PCI_GNT1#	PCI Bus Grant 1	O-3.3	-	int. PU 20k in ICH9 (if PCIRST#=0 AND PWROK=1)
C19	PCI_REQ1#	PCI Bus Request 1	I-5T	PU 8k2 3,3V (S0)	-
C20	PCI_GNT0#	PCI Bus Grant 0	O-3.3	PD 1k0	int. PU 20k in ICH9 (if PCIRST#=0 AND PWROK=1)
C21	GND	Power Ground	PWR	-	-
C22	PCI_REQ0#	PCI Bus Reqest 0	I-5T	PU 8k2 3,3V (S0)	-
C23	PCI_RST#	PCI Bus Reset	O-3.3	-	-
C24	PCI_AD0	PCI Adress & Data Bus line	I/O-5T	-	-
C25	PCI_AD2	PCI Adress & Data Bus line	I/O-5T	-	-
C26	PCI_AD4	PCI Adress & Data Bus line	I/O-5T	-	-
C27	PCI_AD6	PCI Adress & Data Bus line	I/O-5T	-	-
C28	PCI_AD8	PCI Adress & Data Bus line	I/O-5T	-	-
C29	PCI_AD10	PCI Adress & Data Bus line	I/O-5T	-	-
C30	PCI_AD12	PCI Adress & Data Bus line	I/O-5T	-	-
C31	GND	Power Ground	PWR	-	-
C32	PCI_AD14	PCI Adress & Data Bus line	I/O-5T	-	-

C33	PCI_C/BE1#	PCI Bus Command and Byte enables 1	I/O-5T	-	-
C34	PCI_PERR#	PCI Bus Grant Error	I/O-5T	PU 8k2 3,3V (S0)	-
C35	PCI_LOCK#	PCI Bus Lock	I/O-5T	PU 8k2 3,3V (S0)	-
C36	PCI_DEVSEL#	PCI Bus Device Select	I/O-5T	PU 8k2 3,3V (S0)	-
C37	PCI_IRDY#	PCI Bus Bus Initiator Ready	I/O-5T	PU 8k2 3,3V (S0)	-
C38	PCI_C/BE2#	PCI Bus Command and Byte enables 2	I/O-5T	-	-
C39	PCI_AD17	PCI Adress & Data Bus line	I/O-5T	-	-
C40	PCI_AD19	PCI Adress & Data Bus line	I/O-5T	-	-
C41	GND	Power Ground	PWR	-	-
C42	PCI_AD21	PCI Adress & Data Bus line	I/O-5T	-	-
C43	PCI_AD23	PCI Adress & Data Bus line	I/O-5T	-	-
C44	PCI_C/BE3#	PCI Bus Command and Byte enables 3	I/O-5T	-	-
C45	PCI_AD25	PCI Adress & Data Bus line	I/O-5T	-	-
C46	PCI_AD27	PCI Adress & Data Bus line	I/O-5T	-	-
C47	PCI_AD29	PCI Adress & Data Bus line	I/O-5T	-	-
C48	PCI_AD31	PCI Adress & Data Bus line	I/O-5T	-	-
C49	PCI_IRQA#	PCI Bus Interrupt Request A	I-5T	PU 8k2 3,3V (S0)	-
C50	PCI_IRQB#	PCI Bus Interrupt Request B	I-5T	PU 8k2 3,3V (S0)	-
C51	GND	Power Ground	PWR	-	-
C52	PEG_RX0+	PCIexpress Graphics Recieve + (0)	DP-I	-	-
C53	PEG_RX0-	PCIexpress Graphics Recieve - (0)	DP-I	-	-
C54	TYPE0#	n.c. for type 2 module	nc	-	-
C55	PEG_RX1+	PCIexpress Graphics Recieve + (1)	DP-I	-	-

4.3.6 Connector X1B (Signal Levels C56-C110)

Pin	Signal	Description	Type	Termination	Comment
C56	PEG_RX1-	PCIexpress Graphics Recieve - (1)	DP-I	-	-
C57	TYPE1#	n.c. for type 2 module	nc	-	-
C58	PEG_RX2+	PCIexpress Graphics Recieve + (2)	DP-I	-	-
C59	PEG_RX2-	PCIexpress Graphics Recieve - (2)	DP-I	-	-
C60	GND	Power Ground	PWR	-	-
C61	PEG_RX3+	PCIexpress Graphics Recieve + (3)	DP-I	-	-
C62	PEG_RX3-	PCIexpress Graphics Recieve - (3)	DP-I	-	-
C63	RSVD	n.c.	nc	-	-

C64	RSVD	n.c.	nc	-	-
C65	PEG_RX4+	PCIexpress Graphics Recieve + (4)	DP-I	-	-
C66	PEG_RX4-	PCIexpress Graphics Recieve - (4)	DP-I	-	-
C67	RSVD	n.c.	nc	-	-
C68	PEG_RX5+	PCIexpress Graphics Recieve + (5)	DP-I	-	-
C69	PEG_RX5-	PCIexpress Graphics Recieve - (5)	DP-I	-	-
C70	GND	Power Ground	PWR	-	-
C71	PEG_RX6+	PCIexpress Graphics Recieve + (6)	DP-I	-	-
C72	PEG_RX6-	PCIexpress Graphics Recieve - (6)	DP-I	-	-
C73	SDVO_DATA	SDVO_CTRLDATA	I/O-3.3	-	opt. PU 2k21 3,3V (S0) - enable SDVO/HDMI/DP
C74	PEG_RX7+	PCIexpress Graphics Recieve + (7)	DP-I	-	-
C75	PEG_RX7-	PCIexpress Graphics Recieve - (7)	DP-I	-	-
C76	GND	Power Ground	PWR	-	-
C77	RSVD	n.c.	nc	-	-
C78	PEG_RX8+	PCIexpress Graphics Recieve + (8)	DP-I	-	-
C79	PEG_RX8-	PCIexpress Graphics Recieve - (8)	DP-I	-	-
C80	GND	Power Ground	PWR	-	-
C81	PEG_RX9+	PCIexpress Graphics Recieve + (9)	DP-I	-	-
C82	PEG_RX9-	PCIexpress Graphics Recieve - (9)	DP-I	-	-
C83	RSVD	n.c.	nc	-	-
C84	GND	Power Ground	PWR	-	-
C85	PEG_RX10+	PCIexpress Graphics Recieve + (10)	DP-I	-	-
C86	PEG_RX10-	PCIexpress Graphics Recieve - (10)	DP-I	-	-
C87	GND	Power Ground	PWR	-	-
C88	PEG_RX11+	PCIexpress Graphics Recieve + (11)	DP-I	-	-
C89	PEG_RX11-	PCIexpress Graphics Recieve – (11)	DP-I	-	-
C90	GND	Power Ground	PWR	-	-
C91	PEG_RX12+	PCIexpress Graphics Recieve + (12)	DP-I	-	-
C92	PEG_RX12-	PCIexpress Graphics Recieve - (12)	DP-I	-	-
C93	GND	Power Ground	PWR	-	-
C94	PEG_RX13+	PCIexpress Graphics Recieve + (13)	DP-I	-	-
C95	PEG_RX13-	PCIexpress Graphics Recieve - (13)	DP-I	-	-
C96	GND	Power Ground	PWR	-	-
C97	RSVD	n.c.	nc	-	-
C98	PEG_RX14+	PCIexpress Graphics Recieve + (14)	DP-I	-	-

C99	PEG_RX14-	PCIexpress Graphics Recieve - (14)	DP-I	-	-
C100	GND	Power Ground	PWR	-	-
C101	PEG_RX15+	PCIexpress Graphics Recieve + (15)	DP-I	-	-
C102	PEG_RX15-	PCIexpress Graphics Recieve -	DP-I	-	-
C103	GND	Power Ground	PWR	-	-
C104	VCC_12V	12V VCC	PWR	-	-
C105	VCC_12V	12V VCC	PWR	-	-
C106	VCC_12V	12V VCC	PWR	-	-
C107	VCC_12V	12V VCC	PWR	-	-
C108	VCC_12V	12V VCC	PWR	-	-
C109	VCC_12V	12V VCC	PWR	-	-
C110	GND	Power Ground	PWR	-	-

4.3.7 Connector X1B (Signal Levels D1-D55)

Pin	Signal	Description	Type	Termination	Comment
D1	GND	Power Ground	PWR	-	-
D2	IDE_D5	IDE Data Bus	I/O-5T	-	-
D3	IDE_D10	IDE Data Bus	I/O-5T	-	-
D4	IDE_D11	IDE Data Bus	I/O-5T	-	-
D5	IDE_D12	IDE Data Bus	I/O-5T	-	-
D6	IDE_D4	IDE Data Bus	I/O-5T	-	-
D7	IDE_D0	IDE Data Bus	I/O-5T	-	-
D8	IDE_REQ	IDE Data Bus	I/O-5T	PD 5k62	-
D9	IDE_IOW#	IDE IO Write	O-3.3	-	-
D10	IDE_ACK#	IDE DMA Acknowledge	O-3.3	-	-
D11	GND	Power Ground	PWR	-	-
D12	IDE_IRQ	IDE Interrupt Request	I-5T	PD 10k	-
D13	IDE_A0	IDE Adress Bus	O-3.3	-	-
D14	IDE_A1	IDE Adress Bus	O-3.3	-	-
D15	IDE_A2	IDE Adress Bus	O-3.3	-	-
D16	IDE_CS1#	IDE Chip Select Channel 0	O-3.3	-	-
D17	IDE_CS3#	IDE Chip Select Channel 1	O-3.3	-	-
D18	IDE_RESET#	IDE Hard Drive Reset	O-3.3	-	int. PU 31k in PATA bridge | not 5V tolerant
D19	PCI_GNT3#	PCI Bus Grant 3	O-3.3	-	int. PU 20k in ICH9 (if PCIRST#=0 AND PWROK=1)
D20	PCI_REQ3#	PCI Bus Reqest 0	I-5T	PU 8k2 3,3V (S0)	-
D21	GND	Power Ground	PWR	-	-
D22	PCI_AD1	PCI Adress & Data Bus line	I/O-5T	-	-
D23	PCI_AD3	PCI Adress & Data Bus line	I/O-5T	-	-
D24	PCI_AD5	PCI Adress & Data Bus line	I/O-5T	-	-
D25	PCI_AD7	PCI Adress & Data Bus line	I/O-5T	-	-
D26	PCI_C/BE0#	PCI Bus Command and Byte enables 0	I/O-5T	-	-
D27	PCI_AD9	PCI Adress & Data Bus line	I/O-5T	-	-
D28	PCI_AD11	PCI Adress & Data Bus line	I/O-5T	-	-

D29	PCI_AD13	PCI Adress & Data Bus line	I/O-5T	-	-
D30	PCI_AD15	PCI Adress & Data Bus line	I/O-5T	-	-
D31	GND	Power Ground	PWR	-	-
D32	PCI_PAR	PCI Bus Parity	I/O-5T	-	-
D33	PCI_SERR#	PCI Bus System Error	I/O-5T	PU 8k2 3,3V (S0)	-
D34	PCI_STOP#	PCI Bus Stop	I/O-5T	PU 8k2 3,3V (S0)	-
D35	PCI_TRDY#	PCI Bus Target Ready	I/O-5T	PU 8k2 3,3V (S0)	-
D36	PCI_FRAME#	PCI Bus Cycle Frame	I/O-5T	PU 8k2 3,3V (S0)	-
D37	PCI_AD16	PCI Adress & Data Bus line	I/O-5T	-	-
D38	PCI_AD18	PCI Adress & Data Bus line	I/O-5T	-	-
D39	PCI_AD20	PCI Adress & Data Bus line	I/O-5T	-	-
D40	PCI_AD22	PCI Adress & Data Bus line	I/O-5T	-	-
D41	GND	Power Ground	PWR	-	-
D42	PCI_AD24	PCI Adress & Data Bus line	I/O-5T	-	-
D43	PCI_AD26	PCI Adress & Data Bus line	I/O-5T	-	-
D44	PCI_AD28	PCI Adress & Data Bus line	I/O-5T	-	-
D45	PCI_AD30	PCI Adress & Data Bus line	I/O-5T	-	-
D46	PCI_IRQC#	PCI Bus Interrupt Request C	I-5T	PU 8k2 3,3V (S0)	-
D47	PCI_IRQD#	PCI Bus Interrupt Request D	I-5T	PU 8k2 3,3V (S0)	-
D48	PCI_CLKRUN#	PCI Clock Run	I-5T	PU 8k25 3,3V (S0)	-
D49	PCI_M66EN	n.c.	nc	-	-
D50	PCI_CLK	CLK_PCI_33M_EXT | PCI Clock 33MHz	O-3.3	-	-
D51	GND	Power Ground	PWR	-	-
D52	PEG_TX0+	PCIexpress Graphics Transmit + (0)	DP-O	-	-
D53	PEG_TX0-	PCIexpress Graphics Transmit - (0)	DP-O	-	-
D54	PEG_LANE_RV#	PCIexpress Graphics Lane Reversal	I-3.3	-	-
D55	PEG_TX1+	PCIexpress Graphics Transmit + (1)	DP-O	-	-

4.3.8 Connector X1B (Signal Levels D56-D110)

Pin	Signal	Description	Type	Termination	Comment
D56	PEG_TX1-	PCIexpress Graphics Transmit - (1)	DP-O	-	-
D57	TYPE2#	n.c. for type 2 module	nc	-	-
D58	PEG_TX2+	PCIexpress Graphics Transmit + (2)	DP-O	-	-
D59	PEG_TX2-	PCIexpress Graphics Transmit - (2)	DP-O	-	-
D60	GND	Power Ground	PWR	-	-

D61	PEG_TX3+	PCIexpress Graphics Transmit + (3)	DP-O	-	-
D62	PEG_TX3-	PCIexpress Graphics Transmit - (3)	DP-O	-	-
D63	RSVD	-	nc	-	
D64	RSVD	-	nc	-	
D65	PEG_TX4+	PCIexpress Graphics Transmit + (4)	DP-O	-	-
D66	PEG_TX4-	PCIexpress Graphics Transmit - (4)	DP-O	-	-
D67	GND	Power Ground	PWR	-	-
D68	PEG_TX5+	PCIexpress Graphics Transmit + (5)	DP-O	-	-
D69	PEG_TX5-	PCIexpress Graphics Transmit - (5)	DP-O	-	-
D70	GND	Power Ground	PWR	-	-
D71	PEG_TX6+	PCIexpress Graphics Transmit + (6)	DP-O	-	-
D72	PEG_TX6-	PCIexpress Graphics Transmit - (6)	DP-O	-	-
D73	SDVO_CLK	SDVO_CTRLCLK	IO-3.3	-	-
D74	PEG_TX7+	PCIexpress Graphics Transmit + (7)	DP-O	-	-
D75	PEG_TX7-	PCIexpress Graphics Transmit - (7)	DP-O	-	-
D76	GND	Power Ground	PWR	-	-
D77	IDE_CBLID	IDE_CBLID# | IDE cable type detect	I/0-3.3	-	opt. int. PU in IDE flash
D78	PEG_TX8+	PCIexpress Graphics Transmit + (8)	DP-O	-	-
D79	PEG_TX8-	PCIexpress Graphics Transmit - (8)	DP-O	-	-
D80	GND	Power Ground	PWR	-	-
D81	PEG_TX9+	PCIexpress Graphics Transmit + (9)	DP-O	-	-
D82	PEG_TX9-	PCIexpress Graphics Transmit - (9)	DP-O	-	-
D83	RSVD	n.c.	nc	-	-
D84	GND	Power Ground	PWR	-	-
D85	PEG_TX10+	PCIexpress Graphics Transmit + (10)	DP-O	-	-
D86	PEG_TX10-	PCIexpress Graphics Transmit - (10)	DP-O	-	-
D87	GND	Power Ground	PWR	-	-
D88	PEG_TX11+	PCIexpress Graphics Transmit + (11)	DP-O	-	-
D89	PEG_TX11-	PCIexpress Graphics Transmit - (11)	DP-O	-	-
D90	GND	Power Ground	PWR	-	-

D91	PEG_TX12+	PCIexpress Graphics Transmit + (12)	DP-O	-	-
D92	PEG_TX12-	PCIexpress Graphics Transmit - (12)	DP-O	-	-
D93	GND	Power Ground	PWR	-	-
D94	PEG_TX13+	PCIexpress Graphics Transmit + (13)	DP-O	-	-
D95	PEG_TX13-	PCIexpress Graphics Transmit - (13)	DP-O	-	-
D96	GND	Power Ground	PWR	-	-
D97	PEG_ENABLE #	PCIexpress Graphics Enable	I-3.3	PU 10k 3,3V (S0)	-
D98	PEG_TX14+	PCIexpress Graphics Transmit + (14)	DP-O	-	-
D99	PEG_TX14-	PCIexpress Graphics Transmit - (14)	DP-O	-	-
D100	GND	Power Ground	PWR	-	-
D101	PEG_TX15+	PCIexpress Graphics Transmit + (15)	DP-O	-	-
D102	PEG_TX15-	PCIexpress Graphics Transmit - (15)	DP-O	-	-
D103	GND	Power Ground	PWR	-	-
D104	VCC_12V	12V VCC	PWR	-	-
D105	VCC_12V	12V VCC	PWR	-	-
D106	VCC_12V	12V VCC	PWR	-	-
D107	VCC_12V	12V VCC	PWR	-	-
D108	VCC_12V	12V VCC	PWR	-	-
D109	VCC_12V	12V VCC	PWR	-	-
D110	GND	Power Ground	PWR	-	-

Note: The termination resistors in these tables are already mounted on the ETXexpress® board. Refer to the design guide for information about additional termination resistors.

4.4 Alternative pinout of HDMI

Pin Nr.	Pin Name PCIexpress	Pin Name HDMI	HDMI Pin Description
D61	PCIexpress Graphics Transmit + 3	TMDS_B_CLK	HDMI Port B Clock
D62	PCIexpress Graphics Transmit - 3	TMDS_B_CLK#	HDMI port B Clock complement
D58	PCIexpress Graphics Transmit + 2	TMDS_B_DATA0	HDMI port B Data0
D59	PCIexpress Graphics Transmit - 2	TMDS_B_DATA0#	HDMI port B Data0 complement
D55	PCIexpress Graphics Transmit + 1	TMDS_B_DATA1	HDMI port B Data1
D56	PCIexpress Graphics Transmit - 1	TMDS_B_DATA1#	HDMI port B Data1 complement
D52	PCIexpress Graphics Transmit + 0	TMDS_B_DATA2	HDMI port B Data2
D53	PCIexpress Graphics Transmit - 0	TMDS_B_DATA2#	HDMI port B Data2 complement
C61	PCIexpress Graphics Receive + 3	TMDS_B_HPD#	HDMI port B Hot-plug detect
D74	PCIexpress Graphics Transmit + 7	TMDS_C_CLK	HDMI port C Clock
D75	PCIexpress Graphics Transmit – 7	TMDS_C_CLK#	HDMI port C Clock complement
D71	PCIexpress Graphics Transmit + 6	TMDS_C_DATA0	HDMI port C Data0
D72	PCIexpress Graphics Transmit – 6	TMDS_C_DATA0#	HDMI port C Data0 complement

D68	PCIexpress Graphics Transmit + 5	TMDS_C_DATA1	HDMI port C Data1
D69	PCIexpress Graphics Transmit – 5	TMDS_C_DATA1#	HDMI port C Data1 complement
D65	PCIexpress Graphics Transmit + 4	TMDS_C_DATA2	HDMI port C Data2
D66	PCIexpress Graphics Transmit – 4	TMDS_C_DATA2#	HDMI port C Data2 complement
C74	PCIexpress Graphics Receive + 7	TMDS_C_HDP#	HDMI port C Hot-plug detect

4.5 Alternative Pinout of Display Port

Pin Nr.	Pin Name PCIexpress	Pin Name HDMI	HDMI Pin Description
D61	PCIexpress Graphics Transmit + 3	DPB_LANE3	Displayport B Lane3
D62	PCIexpress Graphics Transmit – 3	DPB_LANE3#	Displayport B Lane3 complement
D58	PCIexpress Graphics Transmit + 2	DPB_LANE2	Displayport B Lane2
D59	PCIexpress Graphics Transmit – 2	DPB_LANE2#	Displayport B Lane2 complement
D55	PCIexpress Graphics Transmit + 1	DPB_LANE1	Displayport B Lane1
D56	PCIexpress Graphics Transmit - 1	DPB_LANE1#	Displayport B Lane1 complement
D52	PCIexpress Graphics Transmit + 0	DPB_LANE0	Displayport B Lane0
D53	PCIexpress Graphics Transmit – 0	DPB_LANE0#	Displayport B Lane0 complement
C61	PCIexpress Graphics Receive + 3	DPB_HPD#	Displayport B Hot-plug detect
C58	PCIexpress Graphics Receive + 2	DPB_AUX	Displayport B Aux
C59	PCIexpress Graphics Receive – 2	DPB_AUX#	Displayport B Aux complement
D74	PCIexpress Graphics Transmit + 7	DPC_LANE3	Displayport C Lane3
D75	PCIexpress Graphics Transmit – 7	DPC_LANE3#	Displayport C Lane3 complement
D71	PCIexpress Graphics Transmit + 6	DPC_LANE2	Displayport C Lane2
D72	PCIexpress Graphics Transmit – 6	DPC_LANE2#	Displayport C Lane2 complement
D68	PCIexpress Graphics Transmit + 5	DPC_LANE1	Displayport C Lane1
D69	PCIexpress Graphics Transmit – 5	DPC_LANE1#	Displayport C Lane1 complement
D65	PCIexpress Graphics Transmit + 4	DPC_LANE0	Displayport C Lane0
D66	PCIexpress Graphics Transmit – 4	DPC_LANE0#	Displayport C Lane0 complement
C74	PCIexpress Graphics Receive + 7	DPC_HPD#	Displayport C Hot-plug detect
C71	PCIexpress Graphics Receive + 6	DPC_AUX	Displayport C Aux
C72	PCIexpress Graphics Receive – 6	DPC_AUX#	Displayport C Aus complement
D88	PCIexpress Graphics Transmit + 11	DPD_LANE3	Displayport D Lane3
D89	PCIexpress Graphics Transmit – 11	DPD_LANE3#	Displayport D Lane3 complement
D85	PCIexpress Graphics Transmit + 10	DPD_LANE2	Displayport D Lane2
D86	PCIexpress Graphics Transmit – 10	DPD_LANE2#	Displayport D Lane2 complement
D81	PCIexpress Graphics Transmit + 9	DPD_LANE1	Displayport D Lane1
D82	PCIexpress Graphics Transmit – 9	DPD_LANE1#	Displayport D Lane1 complement
D78	PCIexpress Graphics Transmit + 8	DPD_LANE0	Displayport D Lane0
D77	PCIexpress Graphics Transmit – 8	DPD_LANE0#	Displayport D Lane0 complement
C88	PCIexpress Graphics Receive + 11	DPD_HPD#	Displayport D Hot-plug detect
C85	PCIexpress Graphics Receive + 10	DPD_AUX	Displayport D Aux
C86	PCIexpress Graphics Receive – 10	DPD_AUX#	Displayport D Aus complement

4.6 Signal Description

4.6.1 PCI Express x1 lanes

The PCI Express x1 lanes is a fast connection interface for many different system devices, such as network controllers, I/O controllers or express card devices. The implementation of this subsystem complies with the ETXexpress® / COM Express Specification. Implementation information is provided in the ETXexpress® Design Guide. Refer to the documentation for additional information.

It is also possible to run the 1st 4 x1 lanes as 1 x4 lane. For that please pull-up the signal A33 and A29 to 3.3V on the baseboard.

Note:	Express Card hotplug functionality is only available, when in BIOS setup the PCIexpress lane is switched from [AUTO] which is default setting to [ENABLED]

4.6.2 USB

Eight USB ports (EHCI high-speed 2.0 controller) are on the Intel® ICH-9M south bridge device available. The USB controllers comply with both versions 1.1 and 2.0 of the USB standard and are backward compatible.

Configuration

The USB controllers are PCI bus devices. The BIOS allocates required system resources during configuration of the PCI bus.

4.6.3 SATA

The Intel® ICH-9M south bridge device offers the possibility to connect 3 SATA Harddisks according SATA with 150 MB/s per channel or SATA II with 300 MB/s per channel in AHCI mode.

Configuration

The SATA controller is a PCI bus device. The BIOS allocates required system resources during configuration of the PCI bus.

4.6.4 Audio

The ETXexpress®-PC-XT PCI HD audio controller is integrated in the Intel® ICH-9 Southbridge.

Warning:	Baseboards with AC'97 codec only are not supported.

Configuration

The audio controller is a PCI bus device. The BIOS allocates required system resources during configuration of the PCI device.

4.6.5 Serial IRQ

The serial IRQ pin offers a standardized interface to link interrupt request lines to a single wire.

Configuration

The serial IRQ machine is in “Continuous Mode”

4.6.6 VGA Output

The ETXexpress®-PC-XT graphics subsystem is integrated in the Intel® GS45 northbridge.

Configuration

The graphics controller requires the following resources:

- An IRQ
- Several I/O addresses
- Memory-address blocks in high memory

The BIOS allocates the resources during AGP configuration. Many resources are set for compatibility with industry-standard settings.

4.6.7 LVDS Flat Panel Interface (JILI)

The user interface for flat panels is the JUMPtec Intelligent LVDS Interface (JILI). The implementation of this subsystem complies with the ETXexpress® Specification. Implementation information is provided in the COM Express™ Design Guide. Refer to the documentation for additional information.

4.6.8 PCIexpress Graphics

The PCI express Graphics interface allows the connection of high performace graphics chips on a high bandwidth interface.

The implementation of this subsystem complies with the ETXexpress® / COM Express Specification. Implementation information is provided in the COM Express™ Design Guide. Refer to the documentation for additional information.

4.6.9 SDVO

The ETXexpress®-PC-XT Serial Digital Video Output port is integrated in the Intel® GS45 northbridge. It has the following features:

- Share its pins with the PEG interface
- Serial Digital Video Out Port (DVOB & DVOC) support
- Two 12-bit channels

» The SDVO B/C ports can drive a variety of SDVO devices (TV-Out Encoders, TMDS and LVDS transmitters, etc.)

The implementation of this subsystem complies with the COM Express Specification. Implementation information is provided in the COM Express™ Design Guide. Refer to the documentation for additional information.

4.6.10 HDMI

There is one HDMI port available shared together with PCIexpress Graphics, SDVO and Displayport.

4.6.11 Displayport

The display port is available shared together with PCIexpress Graphics, SDVO and HDMI.

4.6.12 Ethernet

The Ethernet interface offers 10 Mbit, 100Mbit or 1Gbit connection and is driven by the Intel® 82567 PCIexpress Gbit Ethernet controller.

Configuration

The Ethernet controller is a PCIexpress bus device. The BIOS allocates required system resources during configuration of the PCIexpress device.

4.6.13 Power Control

Power Good / Reset Input

The ETXexpress®-PC-XT provides an external input for a power-good signal or a manual- reset pushbutton. The implementation of this subsystem complies with the COM Express™ Specification. Implementation information is provided in the COM Express™ Design Guide. Refer to the documentation for additional information.

4.6.14 Power Management

ATX PS Control

The ETXexpress®-PC-XT can control the main power output of an ATX-style power supply. The implementation of this subsystem complies with the COM Express™ Specification. Implementation information is provided in the COM Express™ Design Guide. Refer to the documentation for additional information.

External SMI Interrupt

Contact Kontron technical support for information on this feature.

4.6.15 Miscellaneous Circuits

Speaker

The implementation of the speaker output complies with the COM Express™ Specification. Implementation information is provided in the COM Express™ Design Guide. Refer to the documentation for additional information.

Battery

The implementation of the battery input complies with the COM Express™ Specification. Implementation information is provided in the COM Express™ Design Guide. Refer to the documentation for additional information.

In compliance with EN60950, there are at least two current-limiting devices (resistor and diode) between the battery and the consuming component.

I2C Bus

You can access the I2C Bus via JUMPtec's Intelligent Device Architecture (JIDA) BIOS functions.

For additional information, refer to the COM Express™ Design Guide, I2C application notes and JIDA specifications which are available at the Kontron Web site.

SM Bus

System Management (SM) bus signals are connected to the SM bus controller, which is located in the Intel® ICH-9M device. For more information about the SM bus, please see the System Management (SM) Bus section in the Appendix A: System Resources chapter.

LPC Bus

The Low Pin Count Interface signals are connected to the LPC Bus bridge, which is located in the Intel® ICH-9M. The LPC low speed interface can be used for peripheral circuits such as an external Super I/O Controller, which typically combine legacy-device support into a single IC. The implementation of this subsystem complies with the COM Express™ Specification. Implementation information is provided in the COM Express™ Design Guide. Refer to the documentation for additional information.

4.6.16 PCI Bus

The implementation of this subsystem complies with the COM Express™ Specification. Implementation information is provided in the COM Express™ Design Guide. Refer to the documentation for additional information.

4.6.17 IDE Port

The IDE host adapter is capable of DMA-33/66/100 operation. The implementation of this subsystem complies with the ETXexpress® Specification. Implementation information is provided in the ETXexpress® Design Guide. Refer to those documents for additional information.

Configuration

The IDE host adapter is a SATA to IDE converter. It is configured by the BIOS during PCI device configuration. You can disable it in setup. Resources used by the SATA/IDE host adapter are compatible with the PC/AT.

5 Special Features

5.1 S5 Eco Mode

Kontron's new high-efficient power-off state S5 Eco enables lowest power-consumption in soft-off state – less than 1 mA compared to the regular S5 state this means a reduction by at least factor 200!

In the "normal" S5 mode the board is supplied by 5V_Stb and needs usually up to 300mA just to stay off. This mode allows to be switched on by power button, RTC event and WakeOnLan, even when it is not necessary. The new S5 Eco mode reduces the current tremendously.

The S5 Eco Mode can be enabled in BIOS Setup, when the BIOS supports this feature.

Following prerequesites and consequences occur when S5 Eco Mode is enabled

- The power button must be pressed at least for 200ms to switch on.
- Wake via Powerbutton only.
- "Power On After Power Fail": only "stay off" is possible
- In single supply mode the S5 Eco Mode must be switched off to enable the board to start immediately

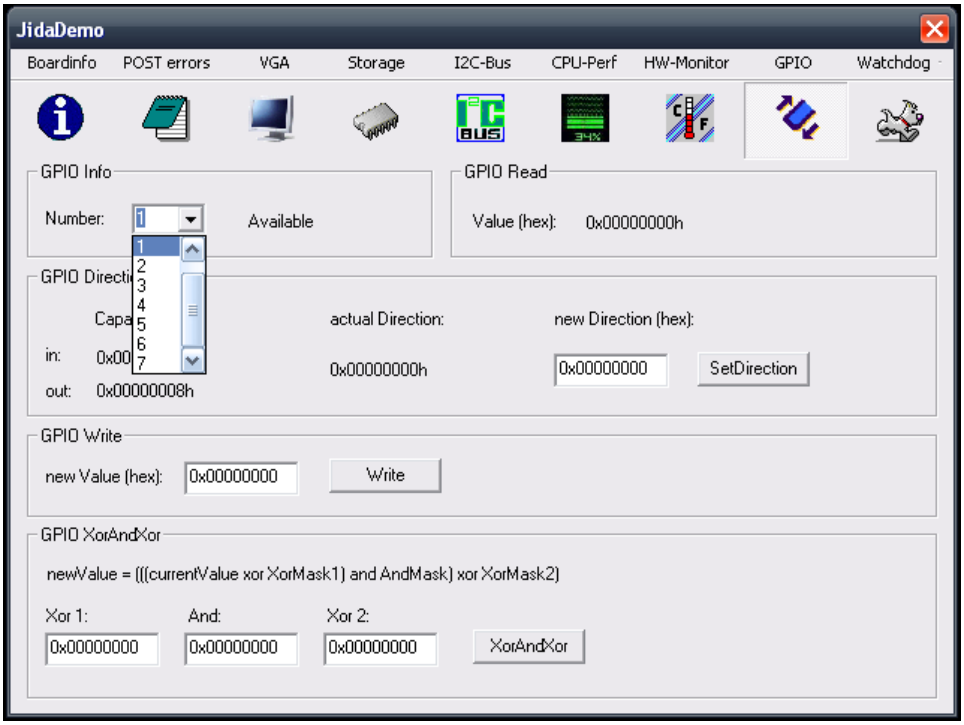
5.2 GPIO - General Purpose Input and Output

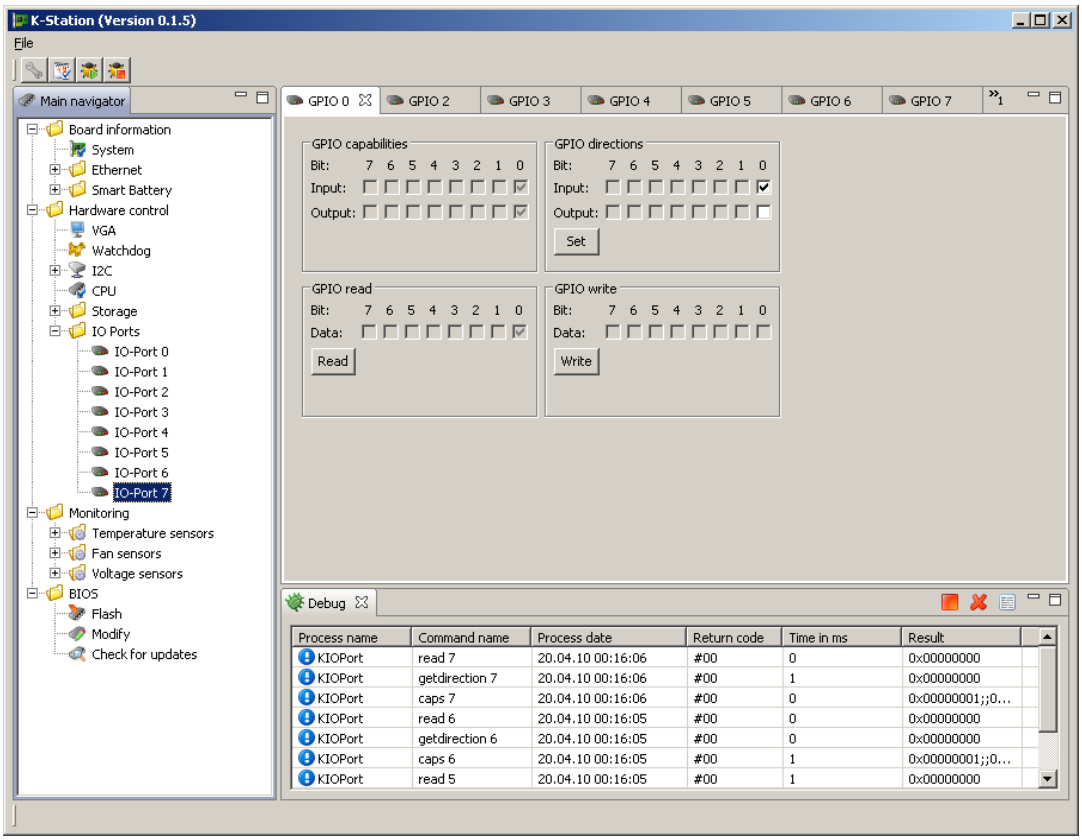
ETXexpress®-PC-XT offers 4 General Purpose Input (GPI) pins and 4 General Purpose Output (GPO) pins. On a 3.3V level digital in- and outputs are available.

Signal	Pin	Description
GPI0	A54	General Purpose Input 0
GPI1	A63	General Purpose Input 1
GPI2	A67	General Purpose Input 2
GPI3	A85	General Purpose Input 3
GPO0	A93	General Purpose Output 0
GPO1	B54	General Purpose Output 1
GPO2	B57	General Purpose Output 2
GPO3	B63	General Purpose Output 3

Configuration

The GPI and GPO pins can be configured via JIDA32. Please refer to the JIDA32 manual in the driver download packet on our website.



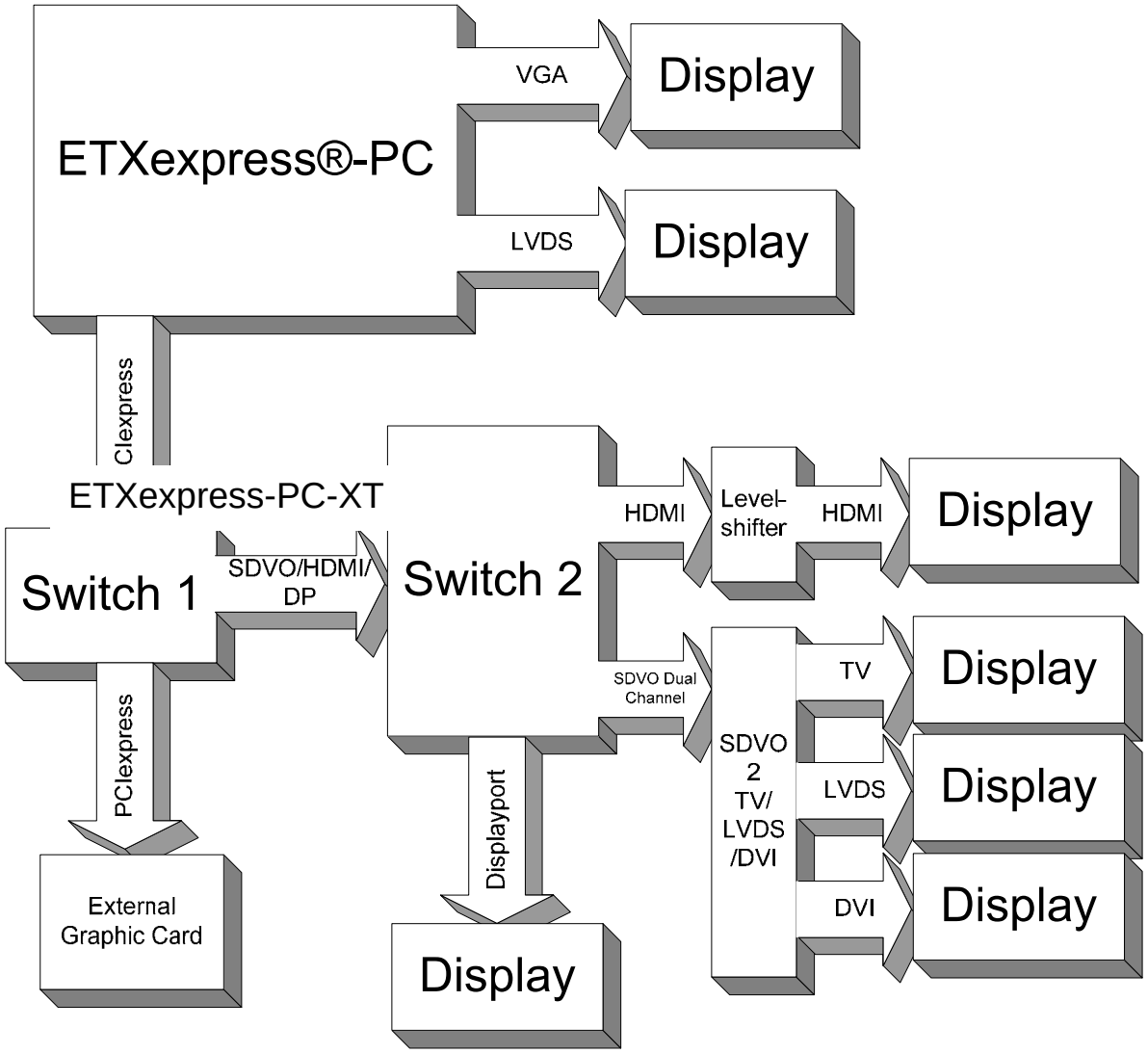


5.3 Usage of Different Graphic interfaces

5.3.1 Available Graphic interfaces

The ETXexpress®-PC-XT offers VGA, PCIexpress, LVDS, HDMI, SDVO and Displayport interfaces to connect graphical user interfaces. The usage of VGA, PCIexpress and SDVO complies with the current ETXexpress® Specification.

The principle of using them is shown in the next drawing.



VGA and LVDS interface is always available and can be used. The pins of PCIexpress Graphics either are used as PCIexpress Graphics or as HDMI/SDVO/DP, which is controlled by switch1.

Switch1 is the SDVO_SDA# line (C73). When this signal is high (2.5V), the SDVO/HDMI/DP output is enabled. Otherwise the lines can be used as PCIexpressGraphic.

The switch 2 to select HDMI, SDVO or Displayport consists of the devices detected on the regarding sense circuits. When there is an SDVO 2 TV/LVDS/DVI converter found on the SDVO_DATA and _CLK lines (C73; D73) then the output is switched to SDVO. When there is Displayport device found on the Displayport AUX lines (C71; C72) then it is Display port and in any other case the output is switched to HDMI.

Note:	PCIexpress Graphics, HDMI and Display Port is only supported by modules with GS45 and GM45

5.4 Speedstep Technology

The Intel® processors offer the Intel® Enhanced SpeedStep™ technology that automatically switches between maximum performance mode and battery-optimized mode, depending on the needs of the application being run. It

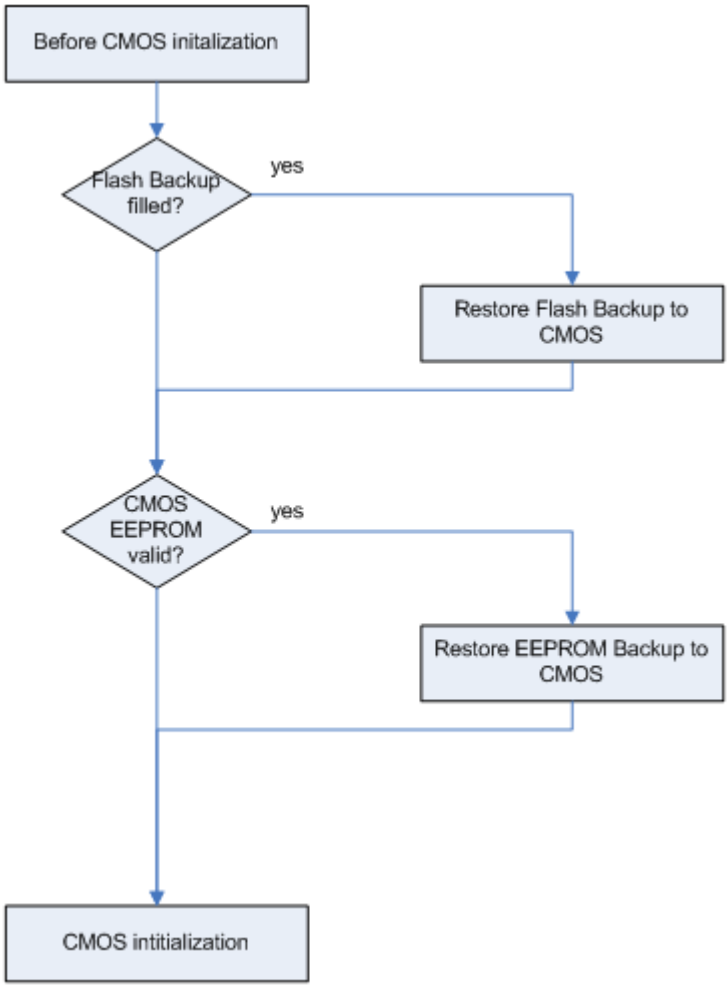
let you customize high performance computing on your applications. When powered by a battery or running in idle mode, the processor drops to lower frequencies (by changing the CPU ratios) and voltage, conserving battery life while maintaining a high level of performance. The frequency is set back automatically to the high frequency, allowing you to customize performance.

In order to use the Intel® Enhanced SpeedStep™ technology the operating system must support SpeedStep™ technology.

By disabling the SpeedStep feature in the BIOS, manual control/modification of CPU performance is possible. Setup the CPU Performance State in the BIOS Setup or use 3rd party software to control CPU Performance States.

5.5 Flash Backup Feature

The ETXexpress-PC-XT supports a new functionality called “Flash Backup”. This new feature allows saving custom defaults directly into the Flash. With invalid EEPROM data or without a CMOS EEPROM, the module will start up with these custom defaults. It’s possible to save this BIOS with changed defaults to an image and flash it on other modules.



To create a BIOS with custom defaults:

» Change your BIOS settings

» Save as custom defaults to RTC/Flash and Exit (module will now always start with these settings)

» Extract the BIOS including custom defaults with afudos or kflash utility for windows

Tool	Command
AFUDOS	`c:\>afudos.exe biosname.rom /O`
KFLASH	`c:\>kflash.exe backup biosname.rom`

Flash your BIOS with custom defaults: To flash a BIOS with customized defaults extracted like described above, use following options

Operating System	Command
Windows OS	`c:\>kflash.exe flash biosname.rom /bncr`
DOS	`c:\>afudos.exe biosname.rom /p /b /n /c` `c:\>jidacmos.exe eep /clean`

NOTE:	kflash.exe is a shell tool included in Kontron K-Station System Utility Package. jidacmos utility is included in the BIOS download packages at Kontron's customer section.

5.6 Dynamic FSB Frequency Switching

Dynamic FSB frequency switching effectively reduces the internal bus clock frequency in half to further decrease the minimum processor operating frequency from the Enhanced Intel SpeedStep Technology performance states and achieve the Super Low Frequency Mode (Super LFM). This feature is supported at FSB frequencies of 1066 MHz, 800 MHz and 667 MHz and does not entail a change in the external bus signal (BCLK) frequency. Instead, both the processor and GMCH internally lower their BCLK reference frequency to 50% of the externally visible frequency. Both the processor and GMCH maintain a virtual BCLK signal (VBCLK) that is aligned to the external BCLK but at half the frequency.

After a downward shift, it would appear externally as if the bus is running with a 133-MHz base clock in all aspects, except that the actual external BCLK remains at 266 MHz. See Figure 3 for details. The transition into Super LFM, a “down-shift,” is done following a handshake between the processor and GMCH. A similar handshake is used to indicate an “up-shift,” a change back to normal operating mode. Please ensure this feature is enabled and supported in the BIOS.

5.7 Enhanced Intel Dynamic Acceleration Technology

The processor supports Intel Dynamic Acceleration Technology mode. The Intel Dynamic Acceleration Technology feature allows one core of the processor to operate at a higher frequency point when the other core is inactive and the operating system requests increased performance. This higher frequency is called the opportunistic frequency and the maximum rated operating frequency is the ensured frequency. The processor includes a hysteresis mechanism that improves overall Intel Dynamic Acceleration Technology performance by decreasing unnecessary transitions of the cores in and out of Intel Dynamic Acceleration Technology mode. Normally, the processor would exit Intel Dynamic Acceleration Technology as soon as two cores are active. This can become an issue if the idle core is frequently awakened for a short periods (i.e., high timer tick rates). The hysteresis mechanism allows two cores to be active for a limited time before it transitions out of Intel Dynamic Acceleration Technology mode.

Intel Dynamic Acceleration Technology mode enabling requires:

» Exposure, via BIOS, of the opportunistic frequency as the highest ACPI P state

» Enhanced Multi-Threaded Thermal Management (EMTTM)

» Intel Dynamic Acceleration Technology mode and EMTTM MSR configuration via BIOS

5.8 VID-x

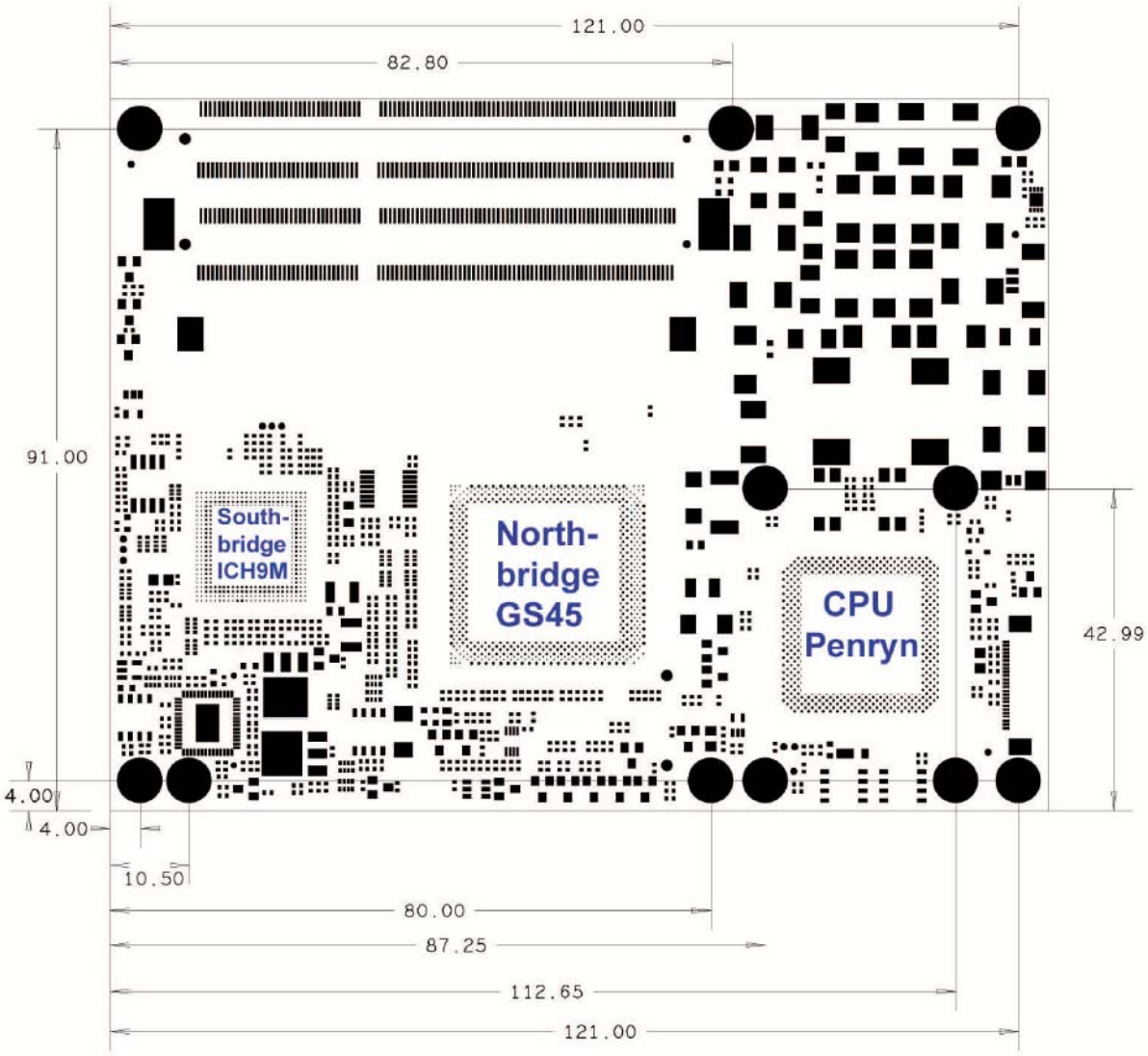
The processor implements the VID-x feature for improved control of core voltage levels when the processor enters a reduced power consumption state. VID-x applies only when the processor is in the Intel Dynamic Acceleration Technology performance state and one or more cores are in low-power state (i.e., CC3/CC4/CC6). VID-x provides the ability for the processor to request core voltage level reductions greater than one VID tick. The amount of VID tick reduction is fixed and only occurs while the processor is in Intel Dynamic Acceleration Technology mode. This improved voltage regulator efficiency during periods of reduced power consumption allows for leakage current reduction which results in platform power savings and extended battery life.

When in Intel Dynamic Acceleration Technology mode, it is possible for both cores to be active under certain internal conditions. In such a scenario the processor may draw a Instantaneous current (ICC_CORE_INST) for a short duration of tINST; however, the average ICC current will be lesser than or equal to ICCDES current specification.

6 Design Consideration

6.1 Module Drill Hole Dimension

6.1.1 38011-XXXX-XX-X



6.2 Thermal Management

A heat-spreader plate assembly is available from Kontron for the ETXexpress®-PC-XT. The heat-spreader plate on top of this assembly is NOT a heat sink. It works as an ETXexpress®-standard thermal interface to use with a heat sink or other cooling device.

External cooling must be provided to maintain the heat-spreader plate at proper operating temperatures. Under worst-case conditions, the cooling mechanism must maintain an ambient air and heat-spreader plate temperature of 60° C or less.

The aluminum slugs and thermal pads on the underside of the heat-spreader assembly implement thermal interfaces between the heat spreader plate and the major heat-generating components on the ETXexpress®-PC-XT. About 80 percent of the power dissipated within the module is conducted to the heat-spreader plate and can be removed by the cooling solution.

For 2266MHz modules, the heat dissipated into the plate ranges from 35 to 45 watts. Design a cooling solution to dissipate the heat load on a heat-spreader plate at a minimum of 45 watts to accommodate all ETXexpress®-PC-XT modules.

You can use many thermal-management solutions with the heat-spreader plates, including active and passive approaches. The optimum cooling solution varies, depending on the ETXexpress® application and environmental conditions. Please see the ETXexpress® Design Guide for further information on thermal management.

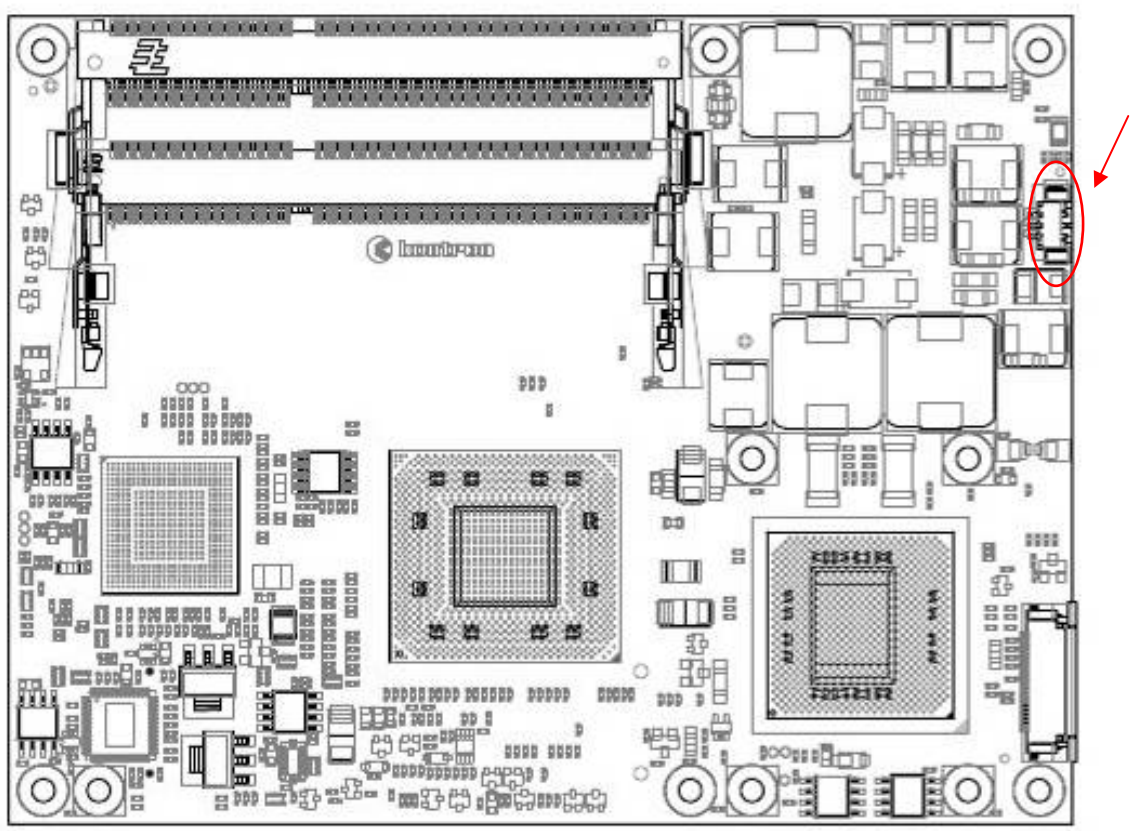
6.3 Heatspreader Dimension

Documentation of ETXexpress-PC-XT heatspreader and cooling solutions is provided at http://emdcustomersection.kontron.com. ETXexpress-PC-XT modules use the same heatsink and heatspreader plate solutions as the ETXexpress-PC SFF (38008-xxxx-xx-x) modules.

6.4 ETXexpress®-PC-XT onboard fan connector

This section describes how to connect a fan to the connector located directly on the ETXexpress®-PC-XT.

6.4.1 Location and pin-out of fan connector



The onboard fan connector (J5) can be found at the right side opposite of the DRAM.

Connector J5 has following specification:

- Part number (Molex) J8: 53261-0390
- Mates with: 51021-0300
- Crimp terminals: 50079-8100

The Pin assignment is:

- Pin1: Tacho
- Pin2: VCC
- Pin3: GND

6.4.2 BIOS settings for fan control

The fan can be controlled via the BIOS Settings "Advanced -> Hardware Health -> Module Hardware Health"



In general 4 modes are possible

- » Auto Fan Mode — Temperature Values can be selected to control the Fan
- » Fan Always On Full — Fan is always full on
- » Fan Disable Mode — Fan is disabled
- » Fan Manually Mode — A fixed PWM value (0…255) can be entered to run the fan at a selected speed

The used hardware monitor onboard is an ADT7475. For additional information please refer to the regarding datasheet.

6.4.3 Electrical Characteristics

Starting with revision 2.x.x there are 2 version of onboard fan control possible. Our standard modules have the simple version populated. For custom projects it is possible to populate a more sophisticated one. The differences are:

Features	Premium Fan	Base Fan
Input Voltage Range	8.5V - 18V	8.5V - 18V
Output Voltage	5V / 12V	Only 12V (switch in BIOS without function
Max. output current	1A	0.3A

Note: The premium fan option is only available on modules with GS45 MCH.

The fan voltage is in both versions VCC of the board and limited to 12V max.

The Fan out voltage output is not short circuit proof. If necessary the user has to ensure that the circuit is protected externally, for example by a fuse on the backplane.

With premium fan solution it is recommended to select the correct fan voltage first in BIOS setup and then connect the fan.

7 System Resources

7.1 Interrupt Request lines

Please be aware that an ACPI OS decides itself on resource usage. The tables below show only an example distribution.

7.1.1 In 8259 PIC mode

IRQ#	Used For	Available	Comment
0	Timer 0	No	
1	Keyboard	No	Note (4)
2	Slave 8259	No	
3		Yes	
4		Yes	
5		Yes	
6		Yes	
7		Yes	
8	RTC	No	
9	SCI	No	Note (3)
10		Yes	
11		Yes	
12	PS/2 Mouse	No	Note (5)
13	FPU	No	
14	IDE0	No	Note (1)(2)
15	IDE1	No	Note (1)(2)

Note: 1. If the “Used For” device is disabled in setup, the corresponding interrupt is available for other devices.

2. If the SATA controller is operating in legacy mode.

3. Unavailable in Advanced Configuration and Power Interface (ACPI) mode. Used as System Control Interrupt (SCI) in ACPI mode. Currently not free in Non-ACPI mode.

4. Used by legacy keyboard controller when available on carrier board.

5. Used by legacy ps/2 mouse controller when available on carrier board.

7.1.2 In APIC mode

IRQ#	Used For	Available	Comment
0	Timer 0	No	
1	Keyboard	No	
2	Slave 8259	No	
3		Yes	Note (4)
4		Yes	Note (4)
5		Yes	Note (4)
6		Yes	Note (4)
7		Yes	Note (4)
8	RTC	No	
9	SCI	No	Note (2)
10		Yes	Note (4)
11		Yes	Note (4)
12		Yes	Note (4)
13	FPU	No	
14	IDE0	No	Note (1)(3)
15	IDE1	No	Note (1)(3)
16	PIRQ[A]	For PCI	PCI IRQ line 1 + Graphics controller + HD Audio Controller + secondary IDE Note (4)
17	PIRQ[B]	For PCI	PCI IRQ line 2 + HD Audio controller Note (4)
18	PIRQ[C]	For PCI	PCI IRQ line 3 + USB UCHI controller #3 + SATA (native mode) Note (4)
19	PIRQ[D]	For PCI	PCI IRQ line 4 + USB UCHI controller #2 + IDE (native mode) Note (4)
20	PIRQ[E]	No	Lan Controller Note (4)
21	PIRQ[F]	No	Note (4)
22	PIRQ[G]	No	Note (4)
23	PIRQ[H]	No	USB EHCI controller, USB UCHI controller #1 Note (4)

Note: 1. If the “Used For” device is disabled in setup, the corresponding interrupt is available for other devices.

2. Unavailable in Advanced Configuration and Power Interface (ACPI) mode. Used as System Control Interrupt (SCI) in ACPI mode. Currently not free in Non-ACPI mode.

3. IRQs are available if IDE controller is either disabled in setup or if in Native IDE mode.

4. ACPI OS decides on particular IRQ usage.

7.2 Direct Memory Access (DMA) Channels

DMA#	Used For	Available	Comment
0		No	
1		No	
2		No	
3		No	
4	Cascade	No	
5		No	
6		No	
7		No	

7.3 Memory Area

Upper Memory	Used For	Available	Comment
C0000h-CFFFFh	VGA BIOS	No	
D0000h-DFFFFh		Yes	LPC Bus or Shadow RAM
E0000h-EFFFFh	System BIOS	No	

7.4 I/O Address Map

Upper Memory	Used For	Available	Comment
400h-41Fh	Chipset	No	Always used by chipset
4D0h-4D1h	Interrupt Controller	No	
500h-53Fh	Chipset	No	Always used by chipset
800h-87Fh	Chipset	No	Always used by chipset
1000h>	PCI	No	

7.5 External Inter-IC (I2C) Bus

I2C Address	Used For	Available	Comment	JIDA Bus Nr.
				2

7.6 System Management (SM) Bus

I2C Address	Used For	Available	Comment	JIDA Bus Nr.
10h	SMB Hoste	No	EEPROM for CMOS Data	1
12h	SMART_Charger	No	Only be used by a SMB Charger	1
14h	SMART_Selector	No	Only be used by a SMB Selector	1
16h	SMART_Battery	No	Only be used by a SMB Battery	1
2Eh	HW-Monitor	No		1
A0h	SPD	No		1
A2h	SPD	No		1
D2h	Clockgenerator	No		1

7.7 JILI-I2C Bus

I2C Address	Used For	Available	Comment	JIDA Bus Nr.
A0h	DDC	No	Display Data	6
62h	MAX6253	No	DAC for Backlight brightness	6

7.8 SDVO-I2C Bus

I2C Address	Used For	Available	Comment	JIDA Bus Nr.
A0h	DDC	No	Display Data	4

7.9 CRT-I2C Bus

I2C Address	Used For	Available	Comment	JIDA Bus Nr.
A0h	DDC	No	Display Data	5

JIDA Bus Nr. 0 and Bus Nr. 3 are for internal use only.

7.10 K-Station / JIDA32 resources

7.10.1 I2C

BUS	Function
I2C 0	Internal / JIDA I2C
I2C 1	SM-Bus
I2C 2	external I2C
I2C 3	internal watchdog
I2C 4	SDVO DDC
I2C 5	CRT DDC
I2C 6	JILI DDC

7.10.2 Storage

Device	Function
EEPROM 0	JIDA EEPROM Area1 with 32 Bytes (free to use)

7.10.3 GPIO

Port	Function
IO-Port 0	GPI 0
IO-Port 1	GPI 1
IO-Port 2	GPI 2
IO-Port 3	GPI 3

IO-Port 4	GPO 0
IO-Port 5	GPO 1
IO-Port 6	GPO 2
IO-Port 7	GPO 3

7.10.4 Hardware Monitor

Sensor	Function
Temp 0	CPU temperature
Temp 1	internal HWM temperature (inside ADT7475)
Temp 2	chipset temperature (Intel® 4 series chipset)
Temp 3	external carrier board SIO Winbond 83627 Temp Sensor 0
Temp 3	external carrier board SIO Winbond 83627 Temp Sensor 1
Temp 5	external carrier board SIO Winbond 83627 Temp Sensor 2
FAN 0	CPU fan controlled by ADT7475
FAN 1	external carrier board SIO Winbond 83627 FAN Sensor 0
FAN 2	external carrier board SIO Winbond 83627 FAN Sensor 1
FAN 3	external carrier board SIO Winbond 83627 FAN Sensor 2
Voltage 0	internal ADT7475 battery voltage: VBAT
Voltage 1	external SIO Winbond 83627 CPU core voltage sensor: V CoreA
Voltage 2	external SIO Winbond 83627 battery voltage Sensor: VBAT
Voltage 3	external SIO Winbond 83627 Voltage Sensor 3: +3.3V
Voltage 4	external SIO Winbond 83627 Voltage Sensor 4: +5V
Voltage 5	external SIO Winbond 83627 standby Voltage Sensor 5: +5V sb

8 BIOS Operation

The module is equipped with AMI® BIOS, which is located in an onboard SPI serial flash memory. You can update the BIOS using a Flash utility.

8.1 Determining the BIOS Version

To determine the AMI® BIOS version, immediately press the Pause key on your keyboard as soon as you see the following text display in the upper left corner of your screen:

- AMIBIOS © 2006 American Megatrends, Inc.
- BIOS Date: 06/16/08 10:52:49 Ver: 08.00.14
- Kontron® BIOS Version <CNXTRXXX>
- © Copyright 2002-2008 Kontron

8.2 Setup Guide

The AMIBIOS Setup Utility changes system behavior by modifying the BIOS configuration. The setup program uses a number of menus to make changes and turn features on or off.

Note:	Selecting incorrect values may cause system boot failure. Load setup default values to recover by pressing <F9>.

8.2.1 Start AMI® BIOS Setup Utility

To start the AMI® BIOS setup utility, press <DEL> when the following string appears during bootup.

Press <DEL> to enter Setup

The Info Menu then appears.

The Setup Screen is composed of several sections:

Setup Screen	Location	Function
Menu Bar	Top	Lists and selects all top level menus.
Legend Bar	Right side Bottom	Lists setup navigation keys.
Item Specific Help Window	Right side Top	Help for selected item.
Menu Window	Left Center	Selection fields for current menu.

Menu Bar

The menu bar at the top of the window lists different menus. Use the left/right arrow keys to make a selection.

Legend Bar

Use the keys listed in the legend bar on the bottom to make your selections or exit the current menu. The table below describes the legend keys and their alternates.

Key	Function
<F1> or <Alt-H>	General Help window.
<Esc>	Exit menu.
← or → Arrow key	Select a menu.
↑ or ↓ Arrow key	Select fields in current menu.
<Home> or <End>	Move cursor to top or bottom of current window.
<PgUp> or <PgDn>	Move cursor to next or previous page.
<F9>	Load the default configuration values for this menu.
<F10>	Save and exit.
<Enter>	Execute command or select submenu.
<Alt-R>	Refresh screen.

Selecting an Item

Use the ↑ or ↓ key to move the cursor to the field you want. Then use the + and – keys to select a value for that field. The Save Value commands in the Exit menu save the values displayed in all the menus.

Displaying Submenus

Use the ← or → key to move the cursor to the submenu you want. Then press <Enter>. A pointer (▸) marks all submenus.

Item Specific Help Window

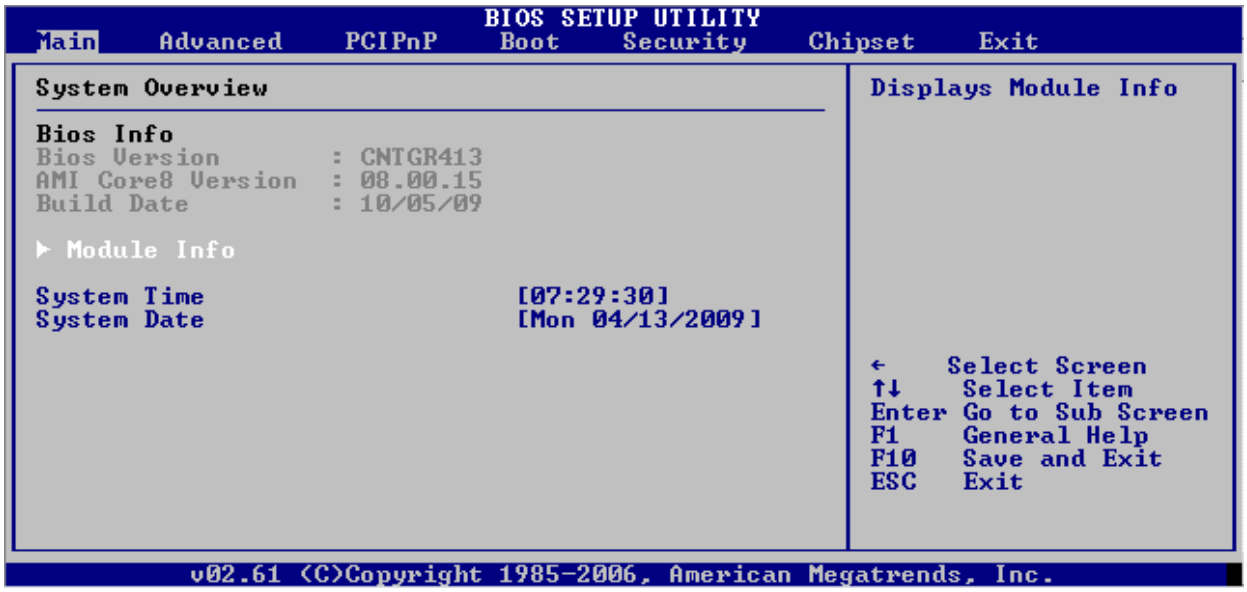
The Help window on the right side of each menu displays the Help text for the selected item. It updates as you move the cursor to each field.

General Help Window

Pressing <F1> or <Alt-F1> on a menu brings up the General Help window that describes the legend keys and their alternates. Press <Esc> to exit the General Help window.

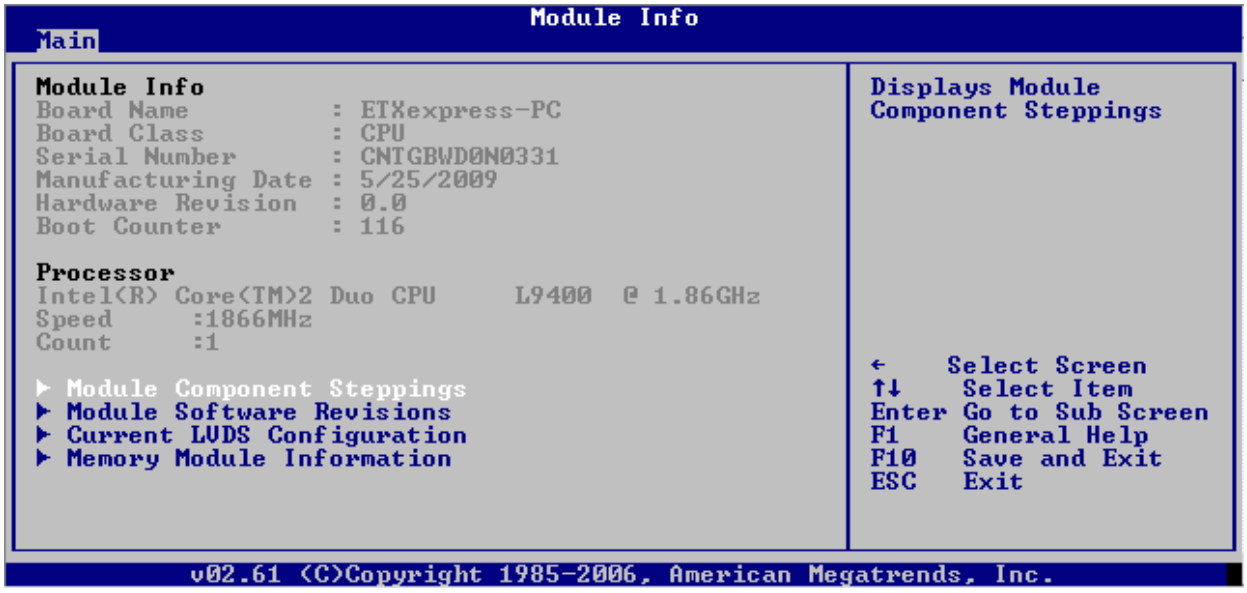
8.3 BIOS Setup

8.3.1 Main Menu

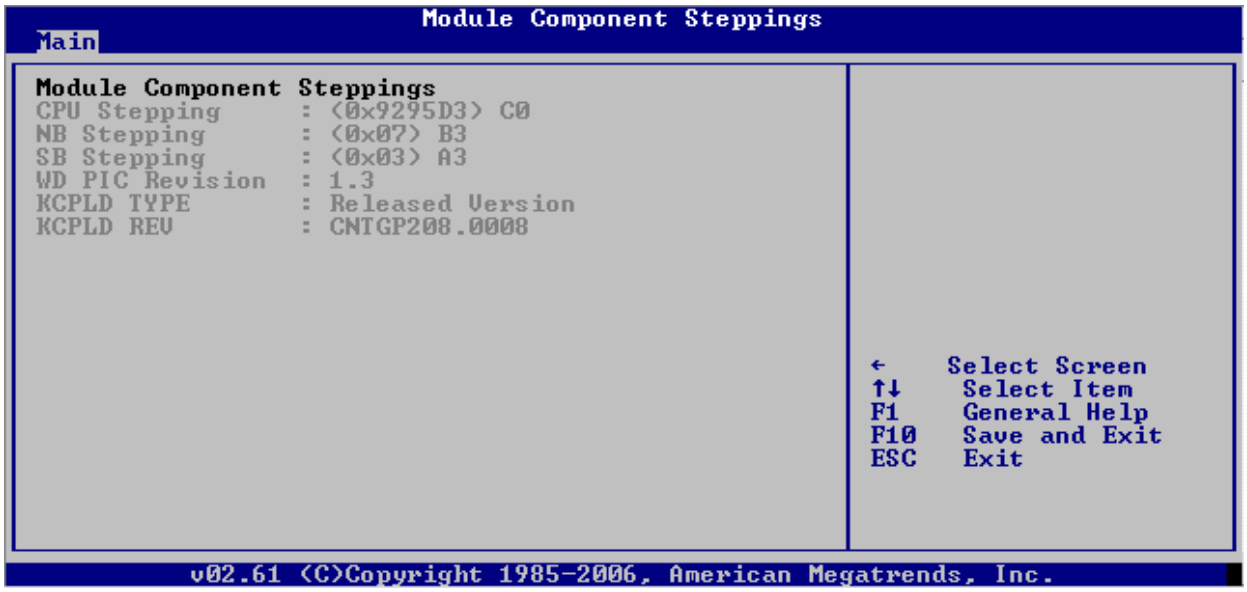


Feature	Option	Description
System Time	[hh:mm:ss]	<Tab>, <Shift-Tab>, or <Enter> selects field
System Date	[mm-dd-yyyy]	<Tab>, <Shift-Tab>, or <Enter> selects field

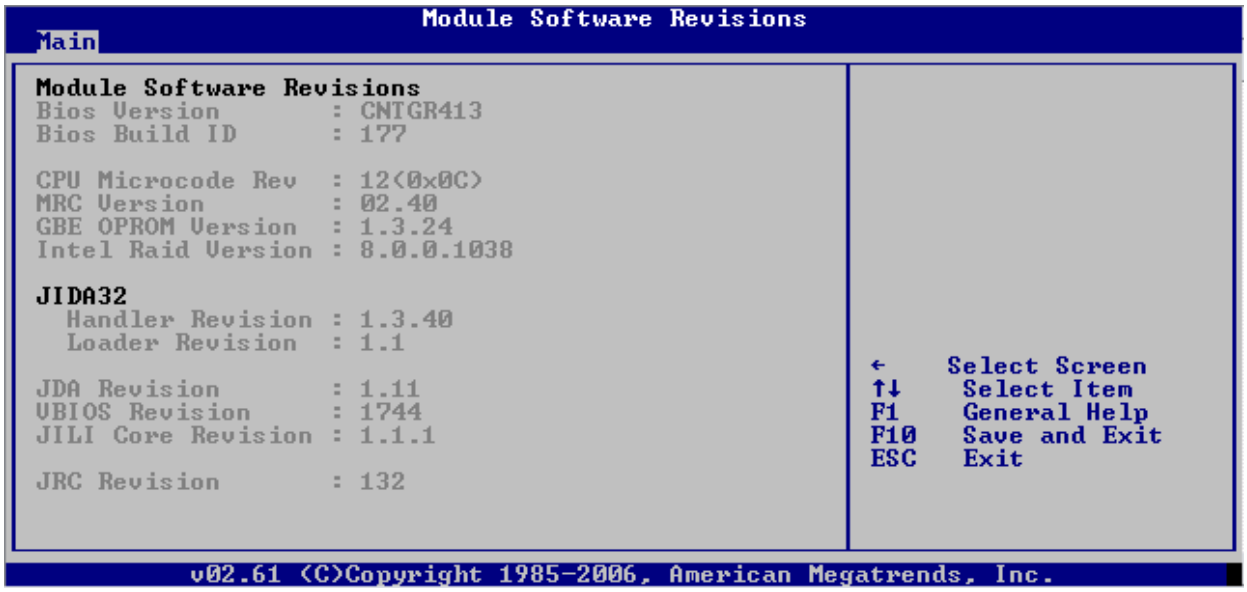
8.3.2 Module Info



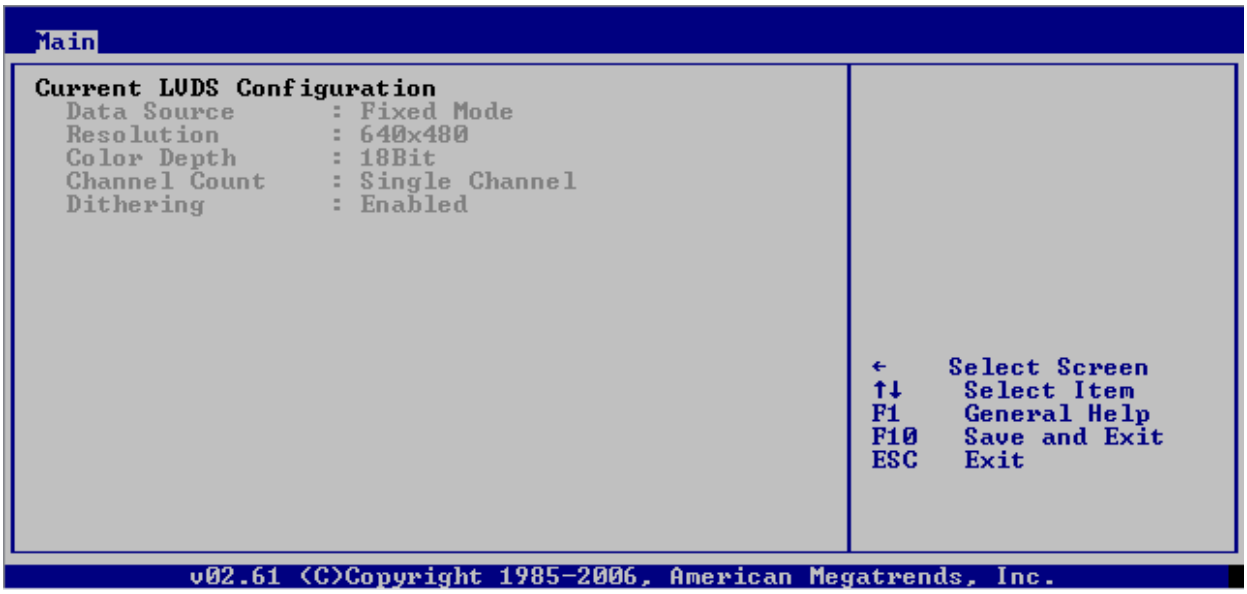
Module Component Steppings



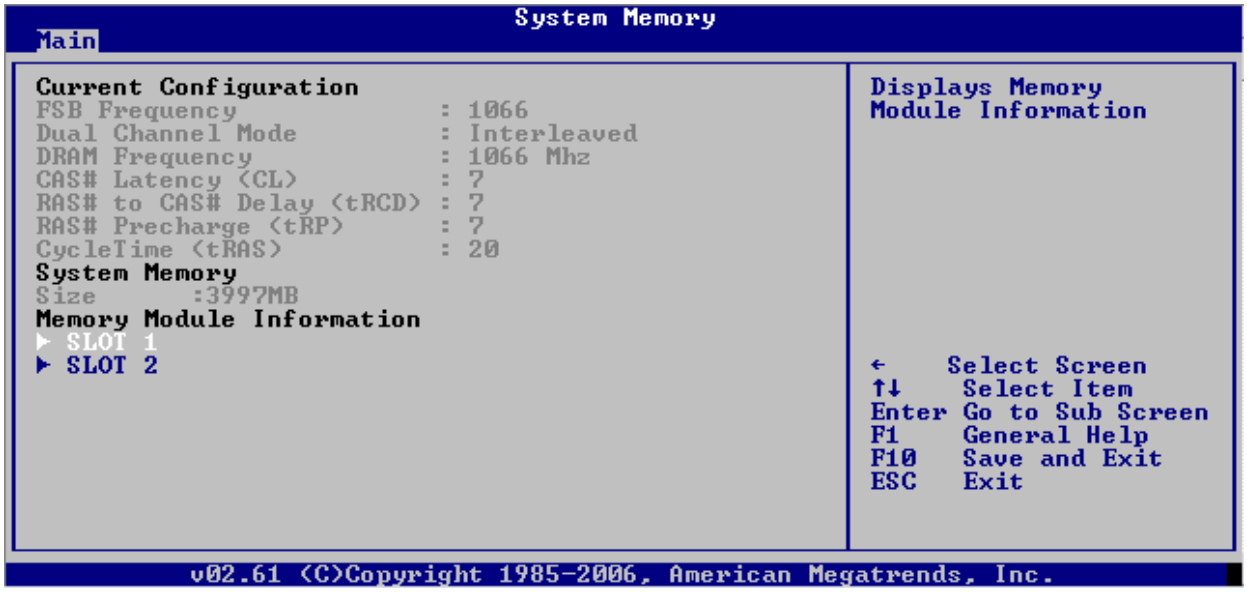
Module Software Revisions



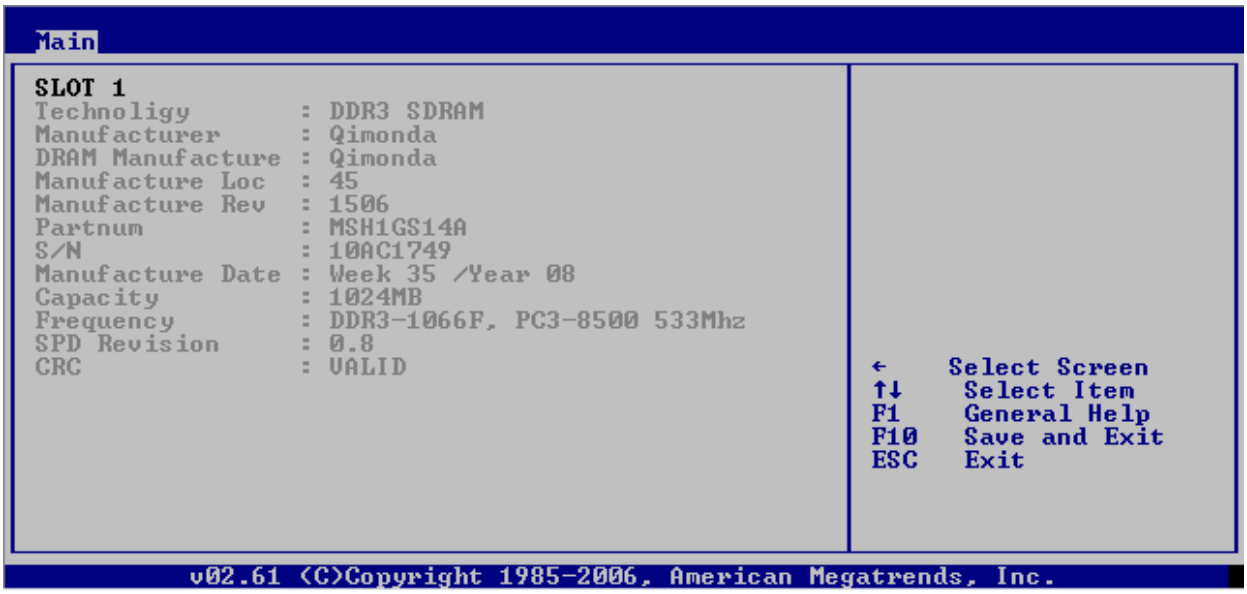
Current LVDS Configuration



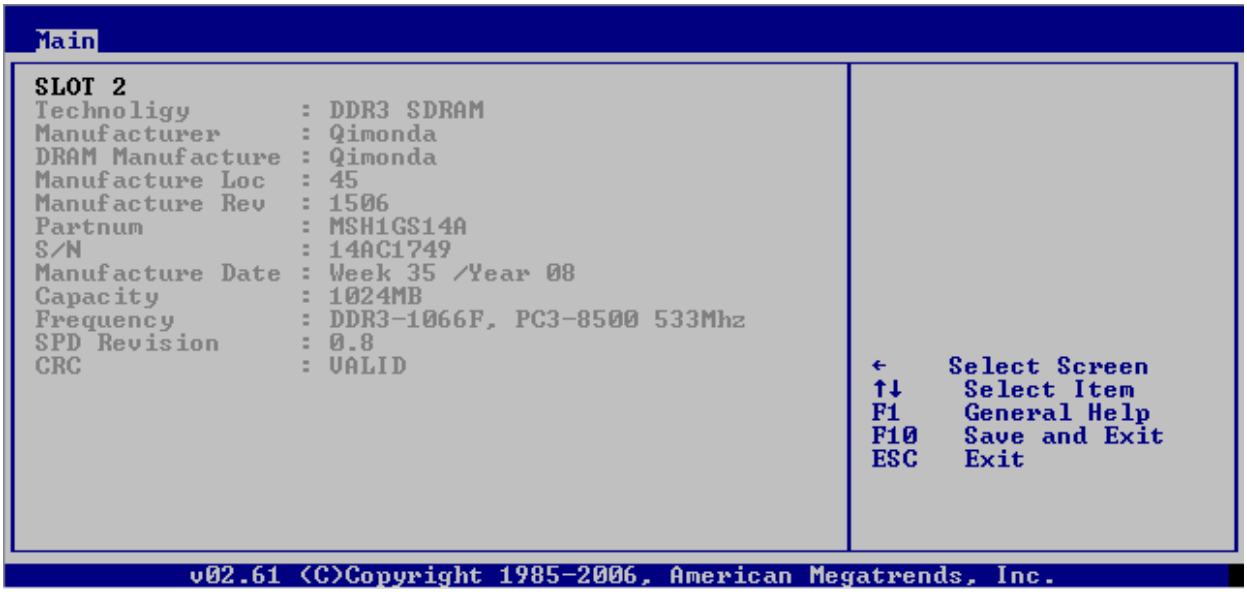
Memory Module Information



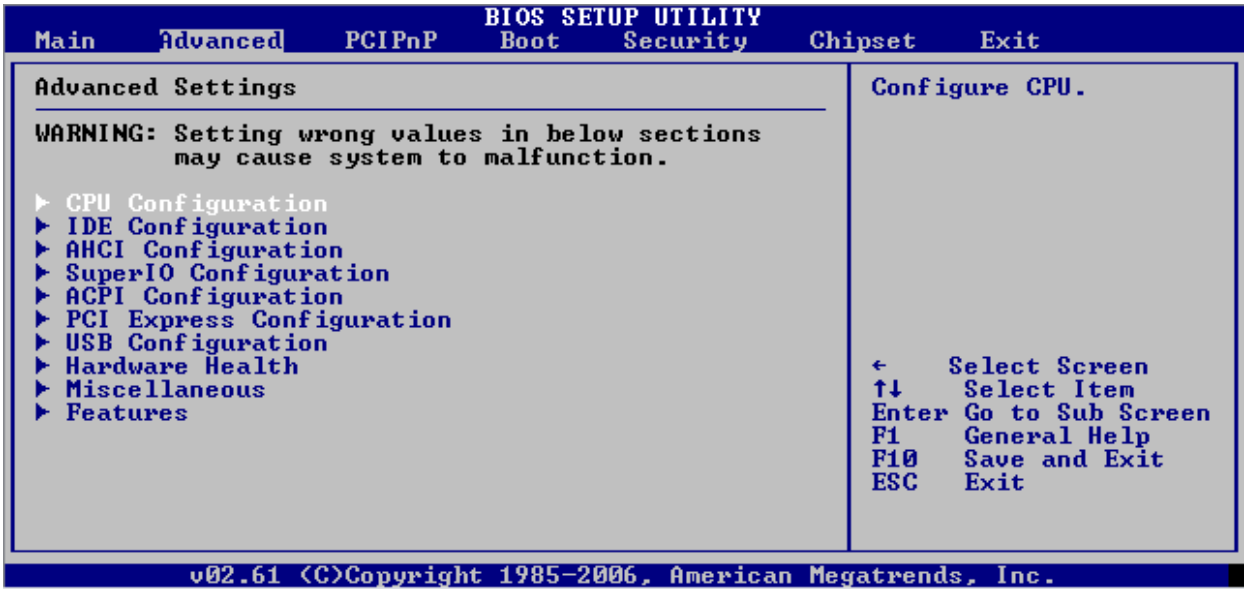
Slot 1


Main
SLOT 1
Technoligy : DDR3 SDRAM
Manufacturer : Qimonda
DRAM Manufacture : Qimonda
Manufacture Loc : 45
Manufacture Rev : 1506
Partnum : MSH1GS14A
S/N : 10AC1749
Manufacture Date : Week 35 /Year 08
Capacity : 1024MB
Frequency : DDR3-1066F, PC3-8500 533Mhz
SPD Revision : 0.8
CRC : VALID
← Select Screen
↑↓ Select Item
F1 General Help
F10 Save and Exit
ESC Exit
v02.61 (C)Copyright 1985-2006, American Megatrends, Inc.

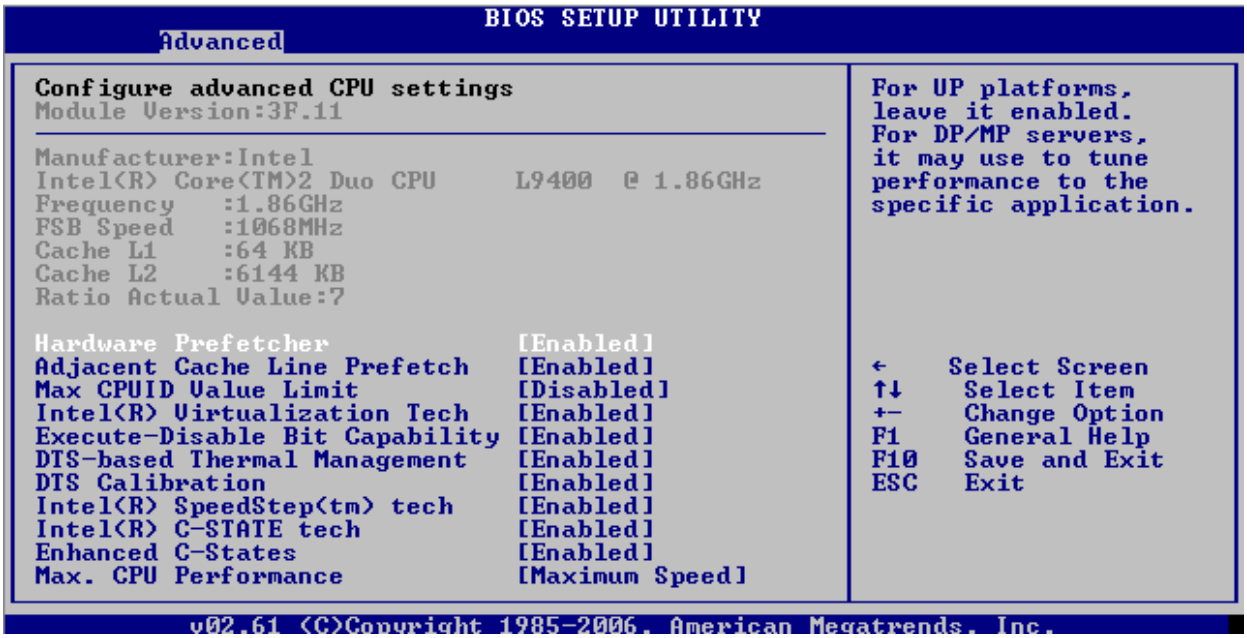
Slot 2


Main
SLOT 2
Technoligy : DDR3 SDRAM
Manufacturer : Qimonda
DRAM Manufacture : Qimonda
Manufacture Loc : 45
Manufacture Rev : 1506
Partnum : MSH1GS14A
S/N : 14AC1749
Manufacture Date : Week 35 /Year 08
Capacity : 1024MB
Frequency : DDR3-1066F, PC3-8500 533Mhz
SPD Revision : 0.8
CRC : VALID
← Select Screen
↑↓ Select Item
F1 General Help
F10 Save and Exit
ESC Exit
v02.61 (C)Copyright 1985-2006, American Megatrends, Inc.

8.3.3 Advanced Menu



CPU Configuration

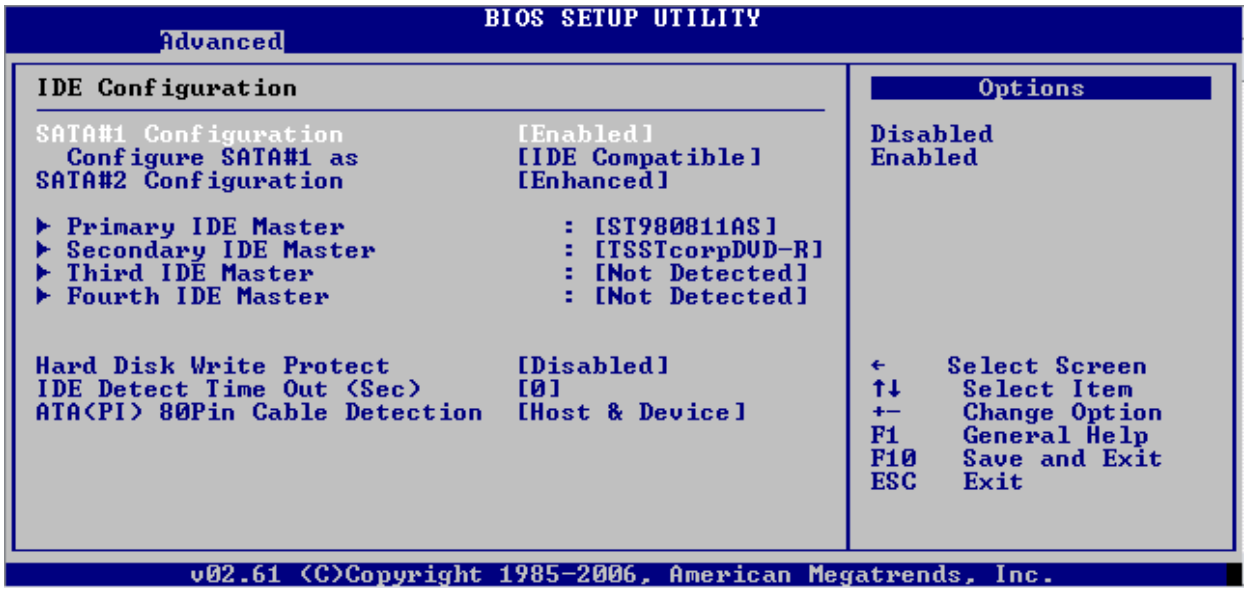


Feature	Option	Description
Hardware Prefetcher	**Enabled** Disabled	For UP platforms, leave it enabled. For DP/MP servers, it may use to tune performance to the specific application.
Adjacent Cache Line Prefetch	**Enabled** Disabled	For UP platforms, leave it enabled. For DP/MP servers, it may use to tune performance to the specific application.
Max CPUID Value Limit	**Disabled** Enabled	Disabled for WindowsXP
Intel® Virtualization Tech	**Enabled** Disabled	When enabled, a VMM can utilize the additional HW Caps, provided by Intel® Virtualization Tech. Note: A full reset is required to change the setting.
Execute-Disable Bit Capability	**Enabled** Disabled	When disabled, force the XD feature flag to always return 0
DTS-based Thermal Management	**Enabled** Disabled	Enable/Disable Thermal Management utilizing the CPU's Digital Thermal Sensor
DTS Calibration	**Enabled** Disabled	Enables and Disables the Calibration function of the CPU's Digital Thermal Sensor
Intel® SpeedStep™	**Enabled** Disabled	Enables and Disables the SpeedStep power management feature
Intel® C-State Technology	**Enabled** Disabled	Enables and Disables the C - States. If enabled, the CPU is set to C2 - C4 state in idle mode
Enhanced C-STATE Modes	**Enabled** Disabled	CPU idle is set to enhanced C-states
Max. CPU Performance	**High** Middle Low	Select CPU Performance after POST High: Highest Speed with enabled Intel® SpeedStep™ Middle: Middle Speed with disabled Intel® SpeedStep™ Low: Low Speed with disabled Intel® SpeedStep™

The CPU Performance relates to the used processor on the ETXexpress-PC-XT. The following table shows you the selected speed in the 3 performance stages.

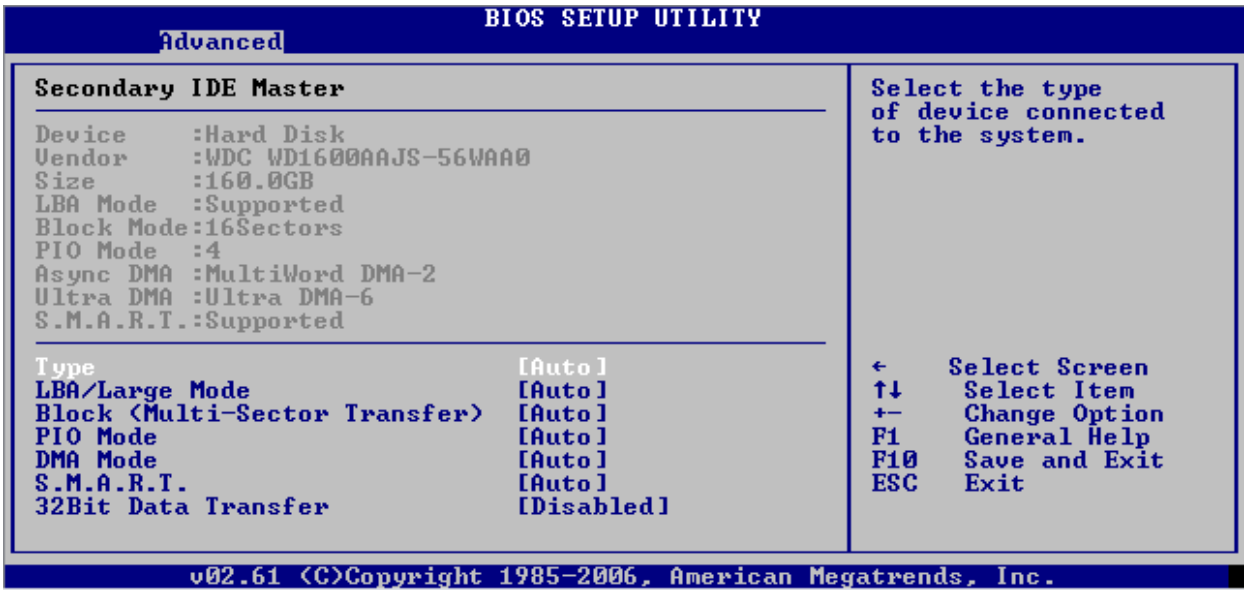
Product Number	Processor	High	Middle	Low
38011-0000-12-1	Celeron® M722	1.2 GHz	1.2 GHz	1.2 GHz
38011-0000-12-2	SU9300	1.2 GHz	1.2 GHz	1.2 GHz
38011-0000-19-2	SL9400	1.86 GHz	1.6 GHz	1.6 GHz

IDE Configuration



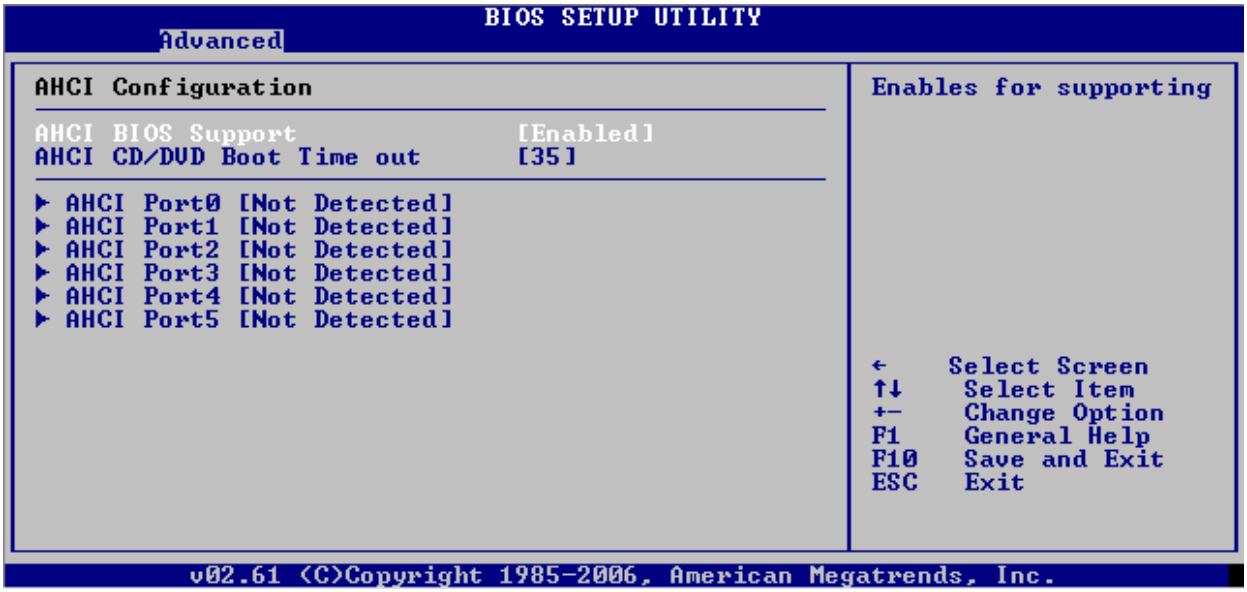
Feature	Option	Description
SATA #1 Configurationer	Disabled **Enabled**	Enables or disables the IDE interface of US15W SCH. This concerns the onboard SSD and PATA2SATA Bridge
Configure SATA#1 as	**IDE Compatible** RAID AHCI IDE Enhanced	Selects the mode for SATA#1 controller
SATA#2 Configuration	**Disabled** Enhanced	Controls the mode for the 2nd SATA controller in ICH-9
Hard Disk Write Protect	**Disabled** Enabled	Disables/enables device write protection. It will be effective only if device is accessed through BIOS functions.
IDE Detect Time Out (Sec.)	0, 5, 10, 15 20, 25, 30, 35	Selects the time out value for the detection of ATA/ ATAPI devices. From 0 to 35 sec.
ATA(PI) 80Pin Cable Detection	**Host & Device** Host Device	Selects the mechanism for detecting 80Pin ATA(PI) cables.

IDE Device Submenu



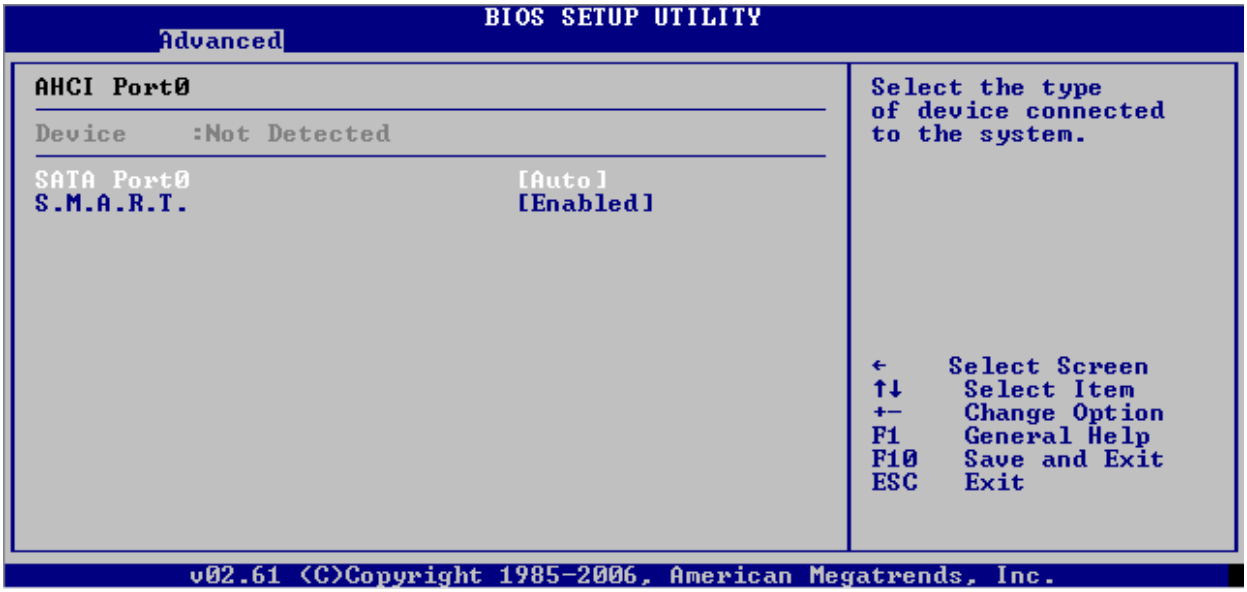
Feature	Option	Description
Type	Not Installed **Auto** CD/DVD ARMD	Selects the type of the IDE Devices connected to the system
LBA/Large Mode	Disabled **Auto**	Disables the LBA mode or enables it, when a device supports it
Block (Multi-Sector Transfer)	Disabled **Auto**	Disabled: The data transfer from and to the device occurs one sector ata atime Auto: The data transfer from and to the device occurs multiple sectors at a time if the device supports it
PIO Mode	**Auto** 0 1 2 3 4	(Auto) Configures the PIO Mode
DMA Mode	**Auto** SWDMAn MWDMAn UDMAn	SWDMA: Single Word DMA MWDMA: Multi Word DMA UDMA: Ultra DMA
S.M.A.R.T.	**Auto** Enabled Disabled	Disables, Enables or automatically enables the S.M.A.R.T feature (Self-Monitoring, Analysis and Reporting Technology)
32Bit Data Transfer	**Enabled** Disabled	Disables and Enables the 32Bit Data Transfer Mode

AHCI Configuration



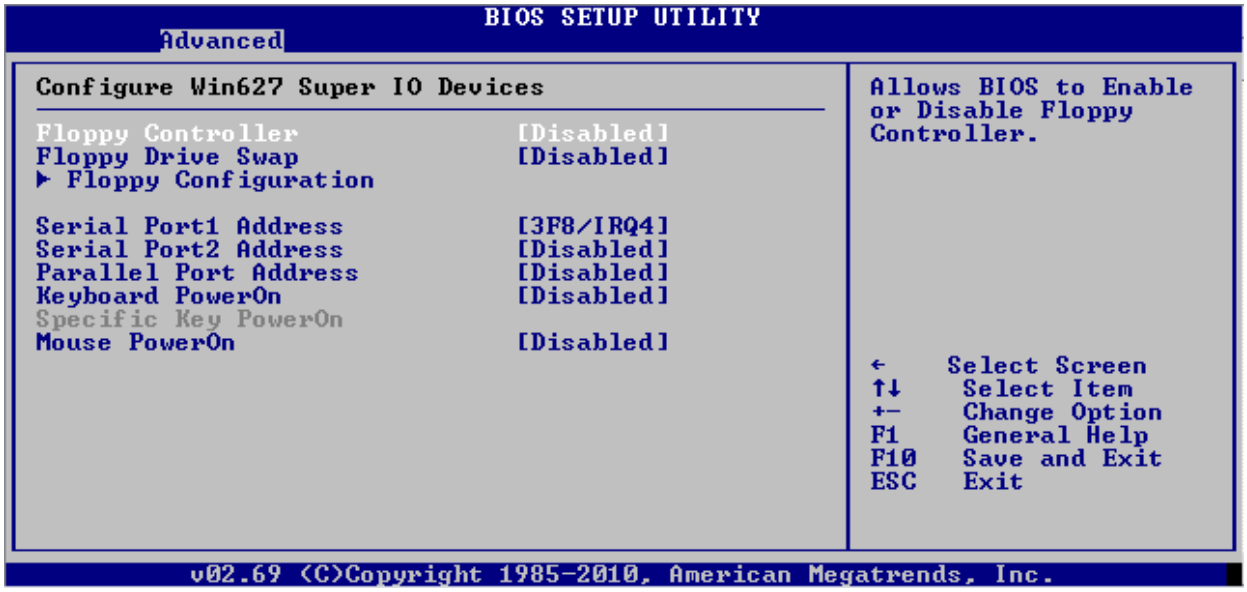
Feature	Option	Description
AHCI BIOS Support	**Enabled** Disabled	Enables / Disables the AHCI Support in BIOS
AHCI CD/DVD Boot Time out	0 5 10 … **35**	Selects the boot time out for AHCI CD/DVD devices

AHCI PortN Submenu



Feature	Option	Description
SATA Port 0	**Auto** Not installed	Enables / Disables the AHCI Support in BIOS
S.M.A.R.T.	Disabled **Enabled**	Enables and disables the SMART functionality.

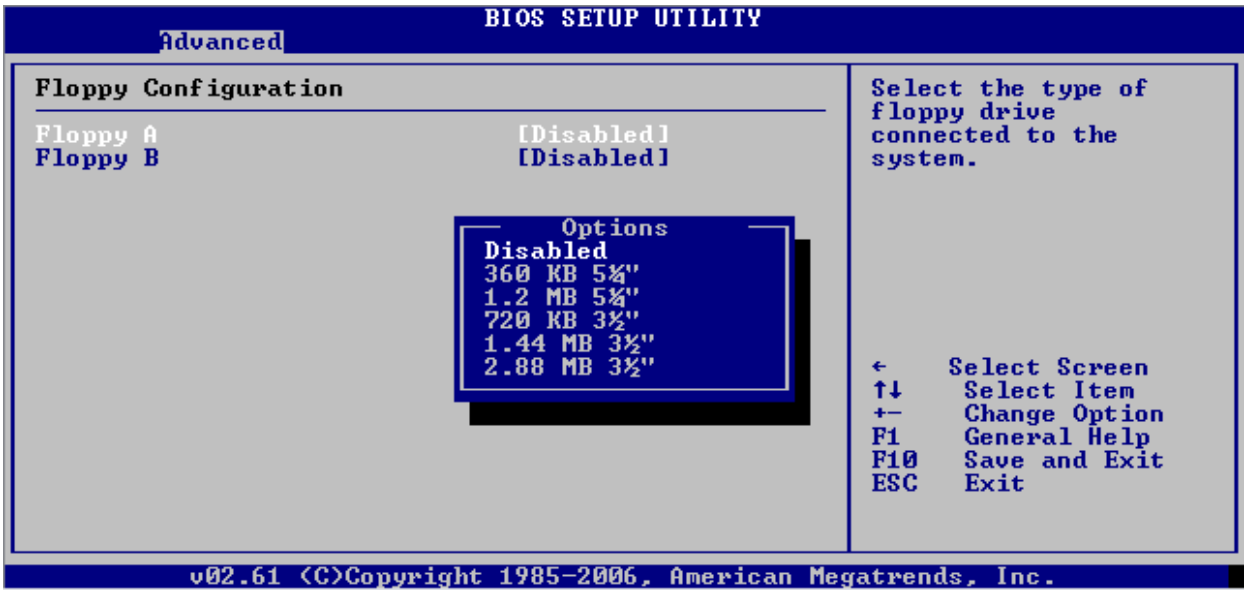
SuperIO Configuration



Feature	Option	Description
Floppy Controller	**Disabled** Enabled	Enables / Disables the AHCI Support in BIOS
Floppy Drive Swap	**Disabled** Enabled	If enabled floppy drive A and B are swapped.
Serial Port1 Address	Disabled **3F8/IRQ4** 2F8/IRQ3 3E8/IRQ4 2E8/IRQ3	Selects the Address of COM Port 1
Serial Port2 Address	**Disabled** 3F8/IRQ4 2F8/IRQ3 3E8/IRQ4 2E8/IRQ3	Selects the Address of COM Port 2
Parallel Port Address	**Disabled** 378 278 3BC	Selects the Address of the LPT Port
Parallel Port Mode	**SPP** Bi-Directional ECP EPP+SPP ECP+SPP	Allows BIOS to Select Parallel Port Mode. (Only visible when Parallel Port enabled.)
Parallel Port IRQ	IRQ5 **IRQ7**	Allows BIOS to Select Parallel Port IRQ. (Only visible when Parallel Port enabled.)
Keyboard PowerOn	**Disabled** Specific Key Any Key	Selects a key to wake up the system with a PS/2 keyboard.
Specific Key Power On	**[Enter Key]**	Only available when Specific Key is selected then „Enter

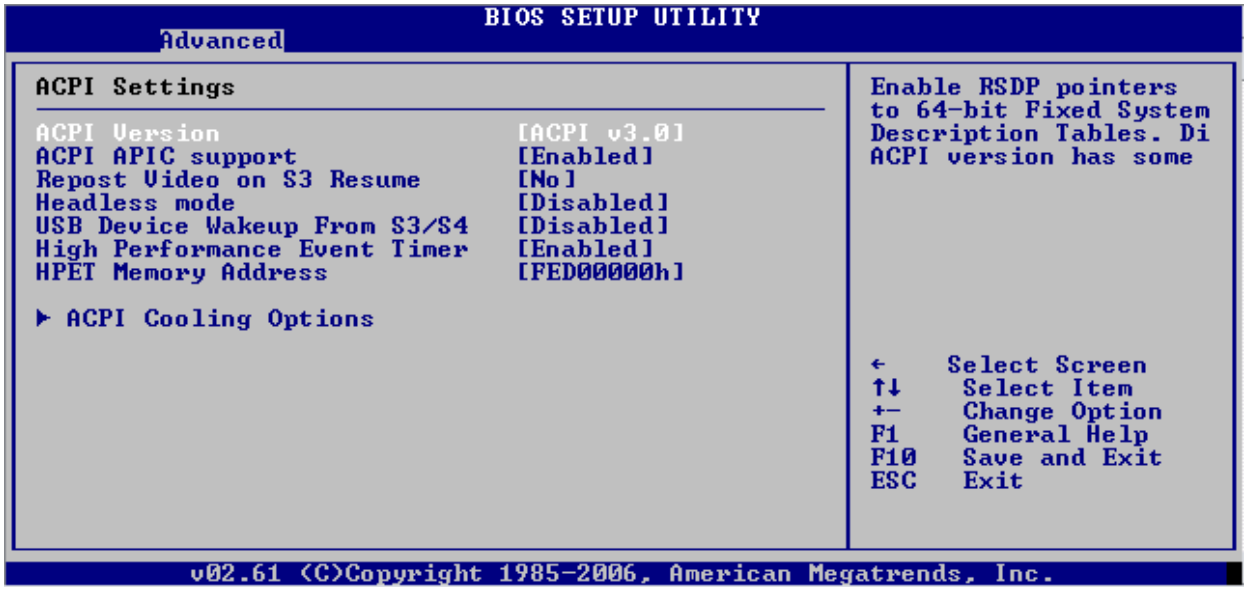
		New Password“ Pop Up appears
Mouse PowerOn	**Disabled** Left Button Right Button	Selects the mouse button of a PS/2 mouse to wake up the system.

Floppy Configuration Submenu



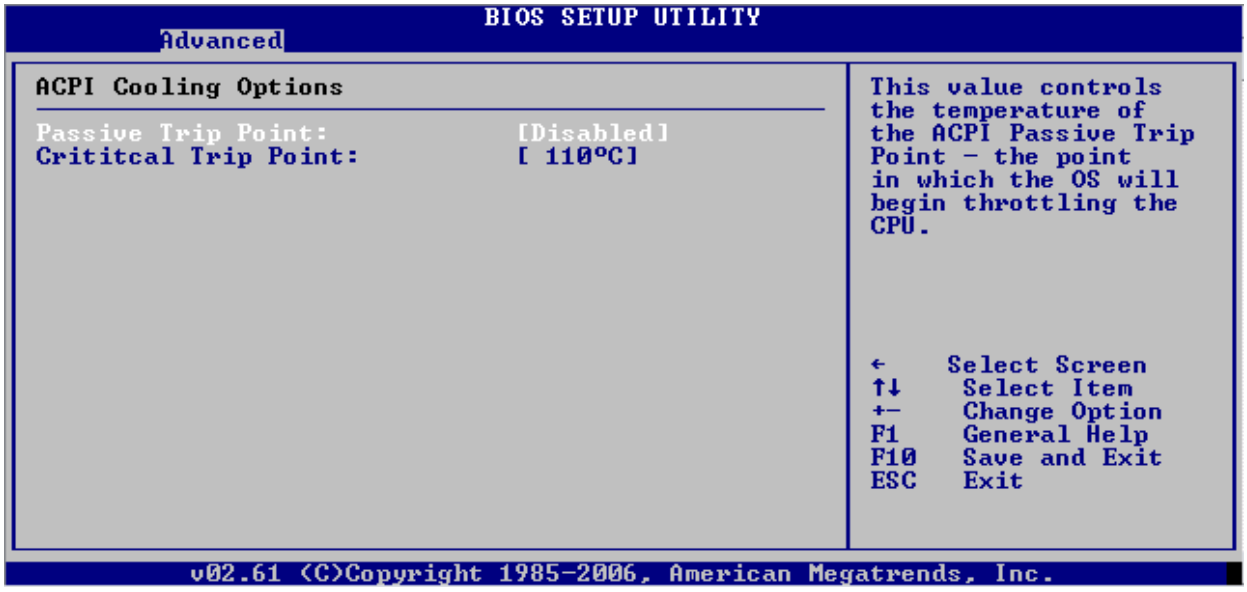
Feature	Option	Description
Floppy A	**Disabled** 360 KB 5 1/4" 1.2 MB 5 1/4" 720 KB 3 1/2" 1.44 MB 3 1/2" 2.88 MB 3 1/2"	Selects the Floppy Drive A
Floppy B	**Disabled** 360 KB 5 1/4" 1.2 MB 5 1/4" 720 KB 3 1/2" 1.44 MB 3 1/2" **2.88 MB 3 1/2"**	Selects the Floppy Drive B

ACPI Configuration



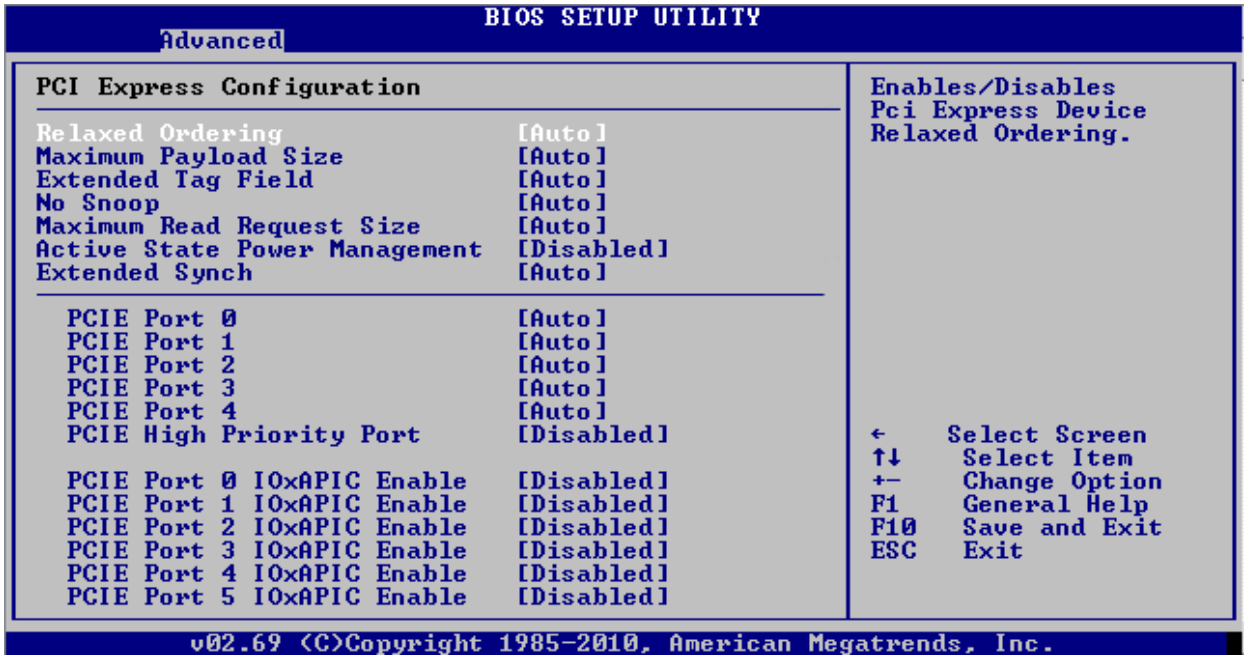
Feature	Option	Description
ACPI Version	**ACPI v.3.0** ACPI v.2.0 ACPI v.1.0	Selects the ACPI version
ACPI APIC support	**Enabled** Disabled	Include ACPI APIC table pointer to RSDT pointer list.
Repost Video on S3 Resume	**No** Yes	If yes, Videobios is reinitialized after S3 Resume
Headless Mode	**Disabled** Enabled	Enables / Disables headless mode through ACPI
USB Device Wakeup From S3/S4	**Disabled** Enabled	Enables / Disables the possibility to wake up via USB from S3 and S4
High Performance Event Timer	Disabled **Enabled**	Enables / Disables the High Performance Event Timer
HPET Memory Address	**FED00000h** FED01000h FED02000h FED03000h	Selects the Address of the High Performance Event Timer

ACPI Cooling Options



Feature	Option	Description
Passive Trip Point	**Disabled** 40°C 45°C 50°C … 110°C	This value controls the temperature of the ACPI Passive Trip Point - the point in which the OS will begin throttling the CPU.
Passive TC1 value	**1** 2 3 … 16	This value sets the TC1 value for the ACPI Passive Cooling Formula. (Only visible when Passive Trip Point is enabled.)
Passive TC2 value	1 2 … **5** … 16	This value sets the TC2 value for the ACPI Passive Cooling Formula. (Only visible when Passive Trip Point is enabled.)
Passive TSP value	2 4 … **10** … 30	This item sets the TSP value for the ACPI Passive Cooling Formula. It represents in tenths of a second how often the OS will read the temperature when Passive Cooling is Enabled.
Critical Trip Point	Disabled 40°C 45°C 50°C … **110°C**	This value controls the temperature of the ACPI Critical Trip Point - the point in which the OS will shut off the system.

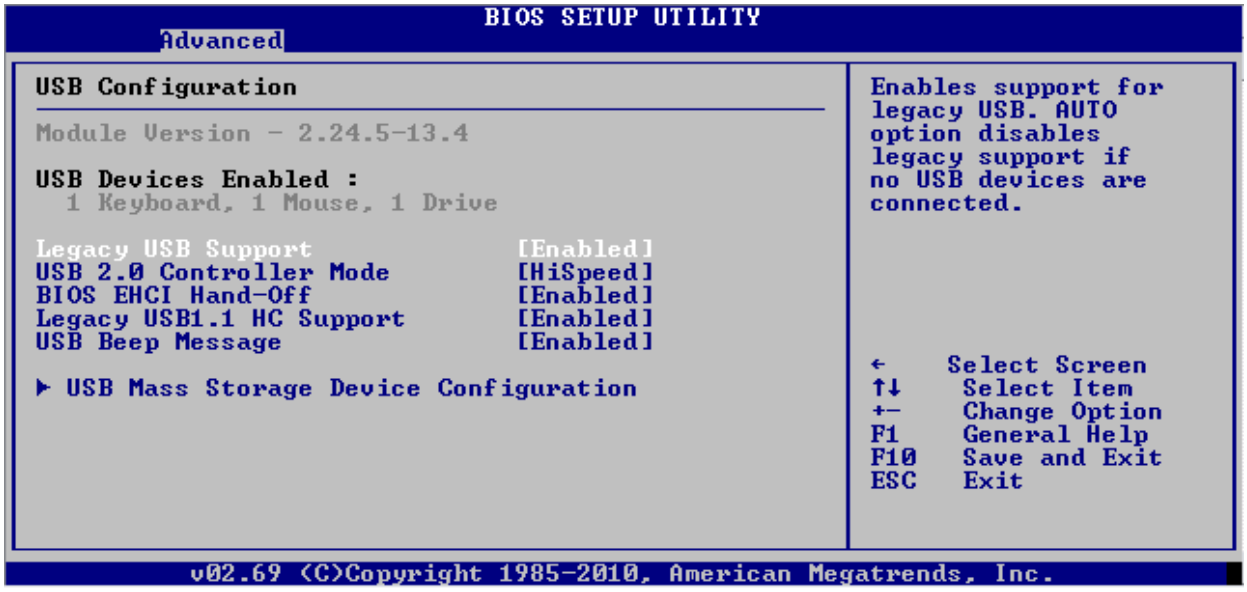
PCI Express Configuration



Feature	Option	Description
Relaxed Ordering	**Auto** Disabled Enabled	Enables and Disables PCI Express Device Relaxing Ordering
Maximum Payload Size	**Auto** 128 Bytes 256 Bytes … 4096 Bytes	Set Maximum Payload of PCI Express Device or allow system BIOS select the value
Extended Tag Field	**Auto** Disabled Enabled	If enabled allows device to use 8-bit TAG field as a requester
No Snoop	**Auto** Disabled Enabled	Enables and Disables PCI Express Device No Snoop option
Maximum Read Request Size	**Auto** 128 Bytes 256 Bytes … 4096 Bytes	Set Maximum Read Request Size of PCI Express Device or allow system BIOS select the value
Active State Power Management	**Disabled** Enabled	Enable/Disable PCI Express L0 and L1 link power states.
Extended Synch	**Auto** Disabled Enabled	If enabled allows generation of Extended Synchronisation patterns.
PCIE Port N	**Auto** Enabled Disabled	Enables/Disables or autoconfigures the PCIE Port N
PCIE High Priority Port	**Disabled**	Select the PCIE Port that gets higher priority than the

	Port 0 Port 1 Port 2 … Port 5	others.
PCIE Port N IOxAPIC Enable	**Disabled** Enabled	Enables/Disables the APIC Support for the PCIE Port N

USB Configuration



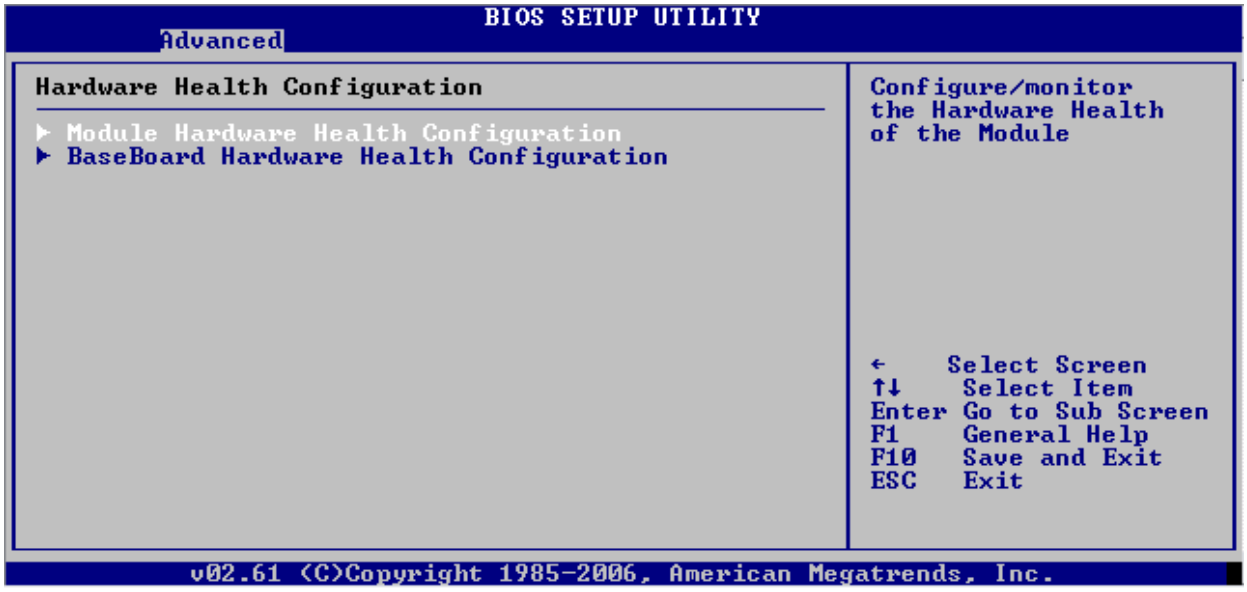
Feature	Option	Description
Legacy USB Support	Auto Disabled **Enabled**	Enables support for legacy USB. Auto option disables legacy support if no USB devices are connected.
USB 2.0 Controller Mode	FullSpeed **HiSpeed**	Configures the USB 2.0 controller in HiSpeed (480Mbps) or FullSpeed (12Mbps)
BIOS EHCI Hand-Off	Disabled **Enabled**	This is a workaround for an OS without EHCI hand-off support. The EHCI ownership change should claim by the EHCI driver
Legacy USB 1.1 HC Support	Disabled **Enabled**	Enables and Disables the legacy 1.1 host controller function
USB Beep Message	Disabled **Enabled**	Enables the beep during USB device enumeration

USB Mass Storage Device Configuration

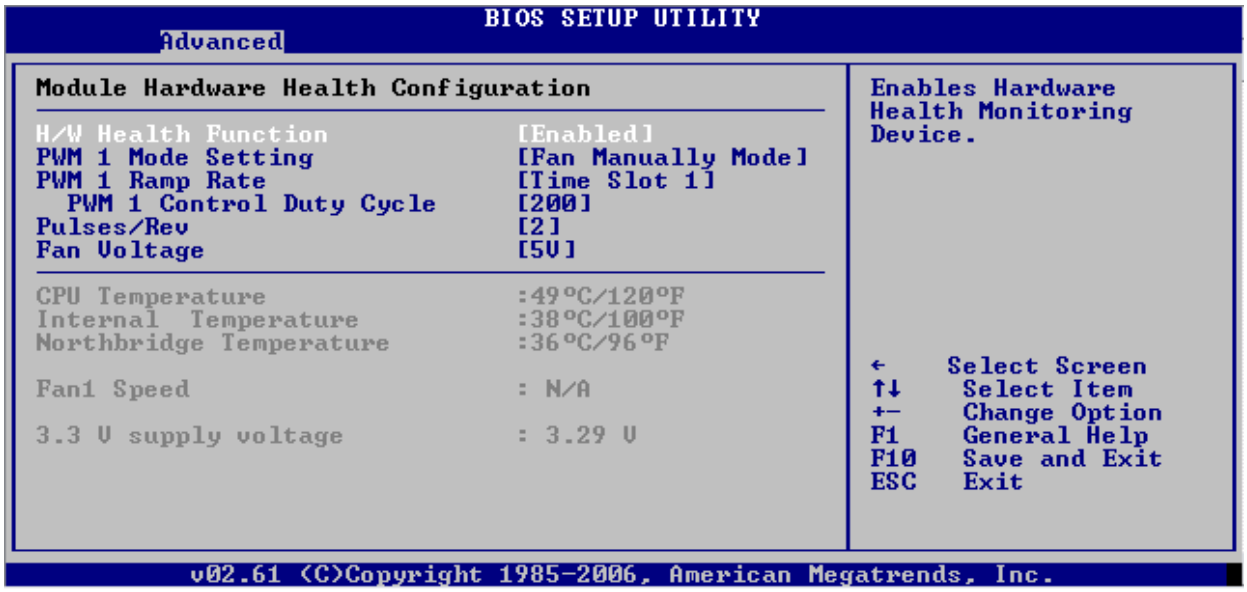


Feature	Option	Description
USB Mass Storage Reset Delay	10 Sec **20 Sec** 30 Sec 40 Sec	Number of seconds POST waits for the USB mass storage device after start unit command.
Emulation Type	**Auto** Floppy Forced FDD Hard Disk CDROM	If Auto USB devices with less than 530MB will be emulated as floppy and remaining as hard drive. Forced FDD option can be used to force a HDD formatted drive to boot as FDD (Ex. ZIP drive).

Hardware Health

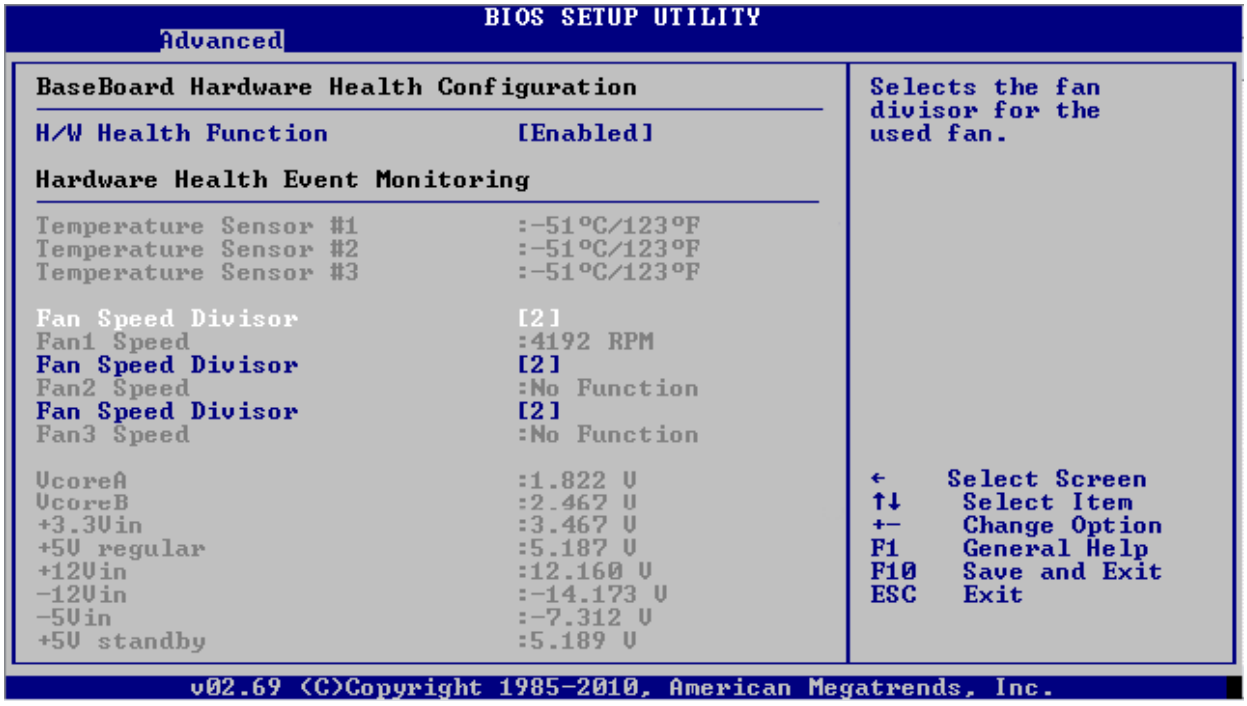


Module Hardware Health Configuration



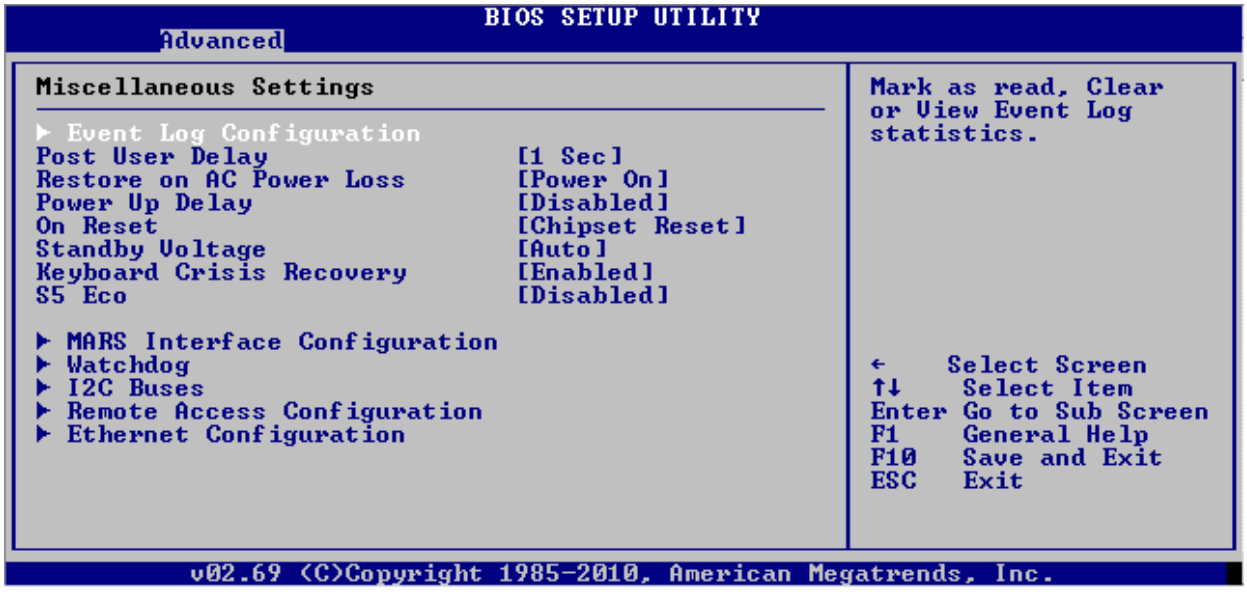
Feature	Option	Description
H/W Health Function	Disabled **Enabled**	Enables Hardware Health Monitoring Device.
PWM 1 Mode Setting	Auto Fan Mode Fan Always On Full Fan Disable Mode **Fan Manually Mode**	PWM Configuration Mode Setting
PWM 1 Ramp Rate	**Time Slot 1** Time Slot 2 Time Slot 3 Time Slot 4 Time Slot 8 Time Slot 12 Time Slot 24 Time Slot 48	
PWM 1 Control Duty Cycle	[0…255]	Controls the length of a PWM duty cycle.
Pulses/Rev	[1…4]	Selects the amount of ticks the fan creates per revolution.
Fan Voltage	12V **5V**	Selects the fan voltage. (only possible with premium fan hardware solution)

Baseboard Hardware Health Configuration



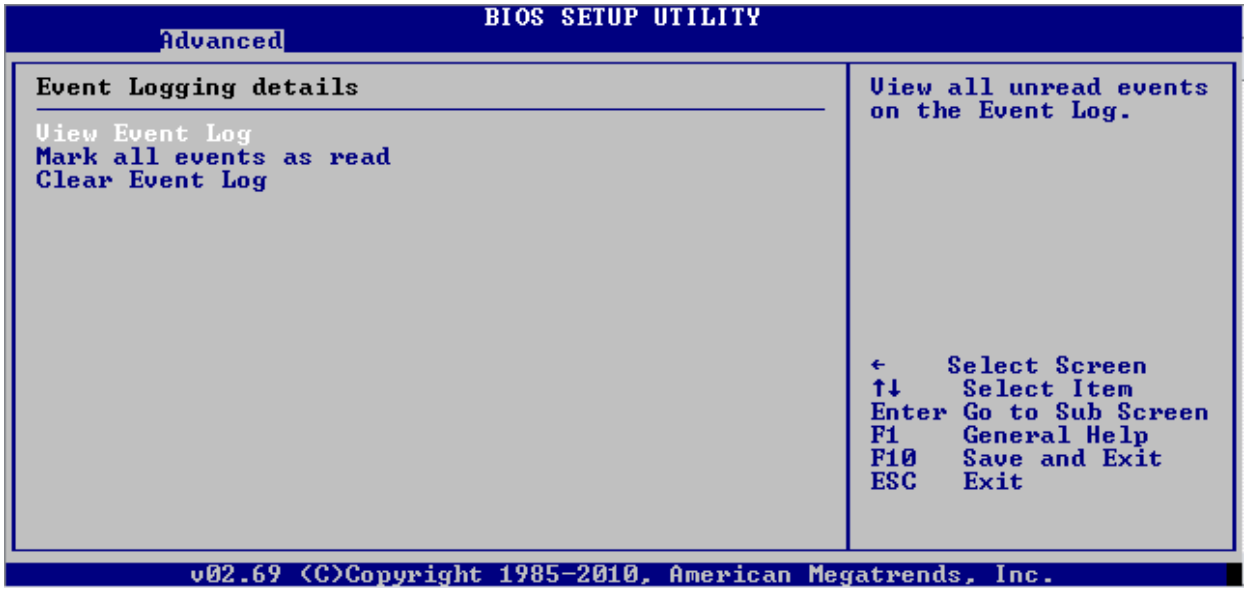
Feature	Option	Description
H/W Health Function	Disabled **Enabled**	Enables Hardware Health Monitoring Device.
Fan Speed Divisor 1	1 **2** 4 … 128	Sets the register setting for the baseboard winbond fan speed divisor for fan 1
Fan Speed Divisor 2	1 **2** 4 … 128	Sets the register setting for the baseboard winbond fan speed divisor for fan 2
Fan Speed Divisor 3	1 **2** 4 … 128	Sets the register setting for the baseboard winbond fan speed divisor for fan 3

Miscellaneous Settings



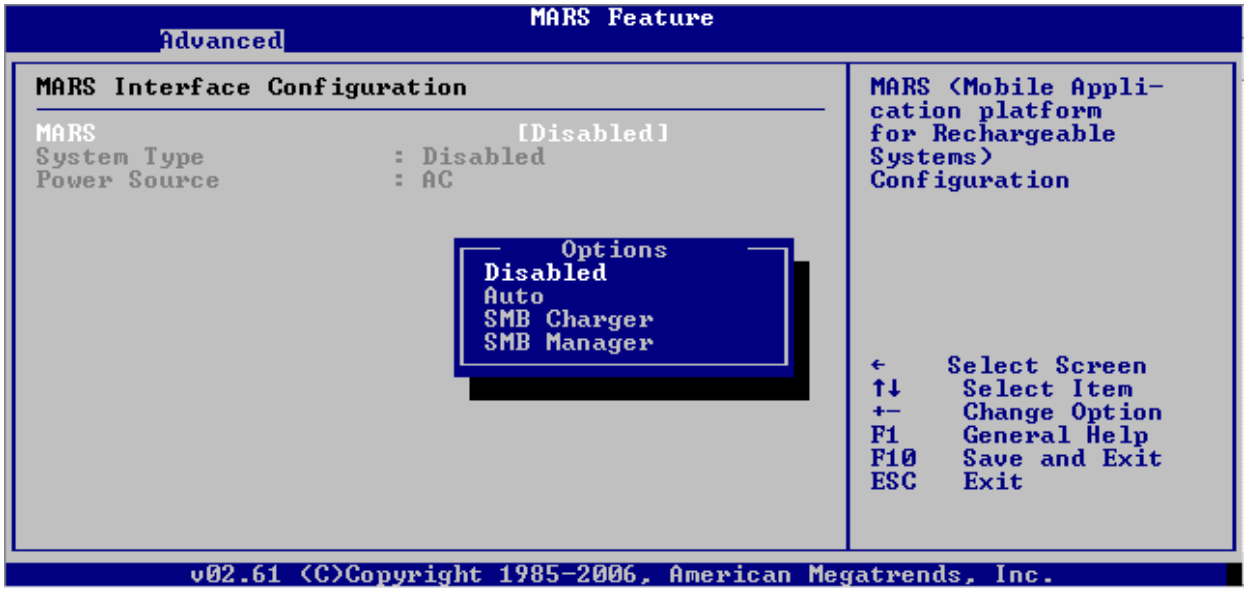
Feature	Option	Description
Post User Delay	None **1 Sec** 2 Sec … 10 Min	Delay to allow access to setup
Restore on AC Power Loss	Power Off **Power On**	Controls the behavior at Power Loss
Power Up Delay	**Disabled** 4 to 5 seconds 3 to 4 seconds 2 to 3 seconds 1 to 2 seconds	Delay after power up
On Reset	Chipset Reset Power Cycle	Controls the behavior in reset case.
Standby Voltage	5V Standby **Auto**	
Keyboard Crisis Recovery	**Enabled** Disabled	Disables and enables the keyboard crisis recovery feature
S5 Eco	Enabled **Disabled**	Enables and disables the S5 Eco feature

Event Log Configuration



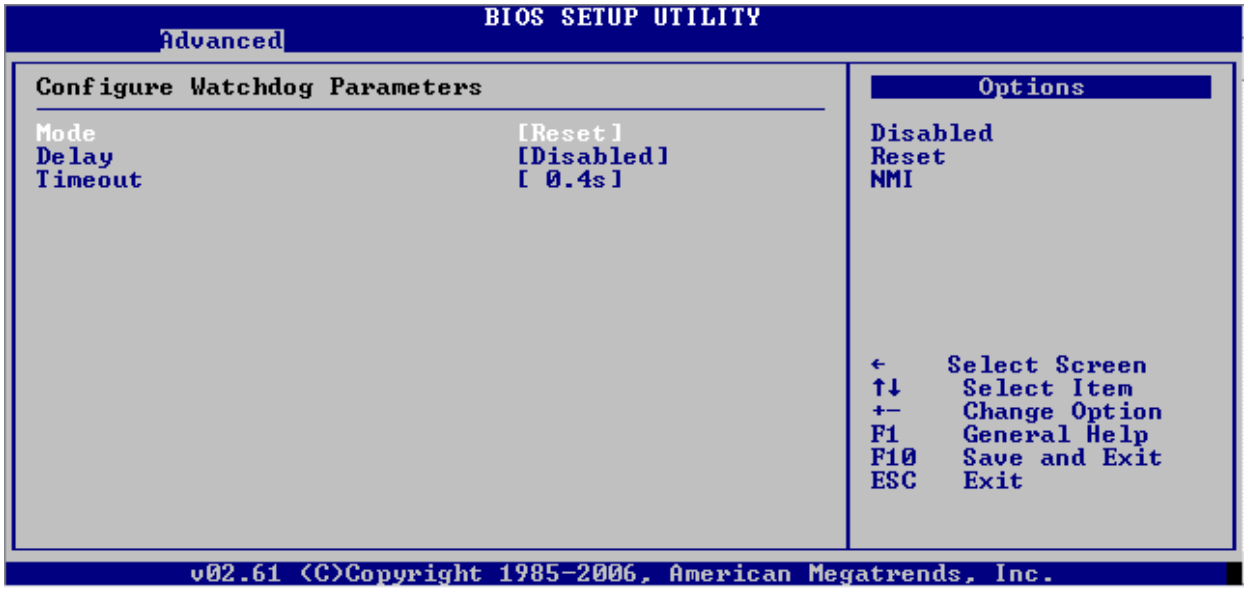
Feature	Option	Description
View Event Log		View All Unread Events in the Event Log
Mark all events as read		Mark All Unread Events as read
Clear Event Log		Discard All Unread Events in the Event Log

MARS Interface Configuration



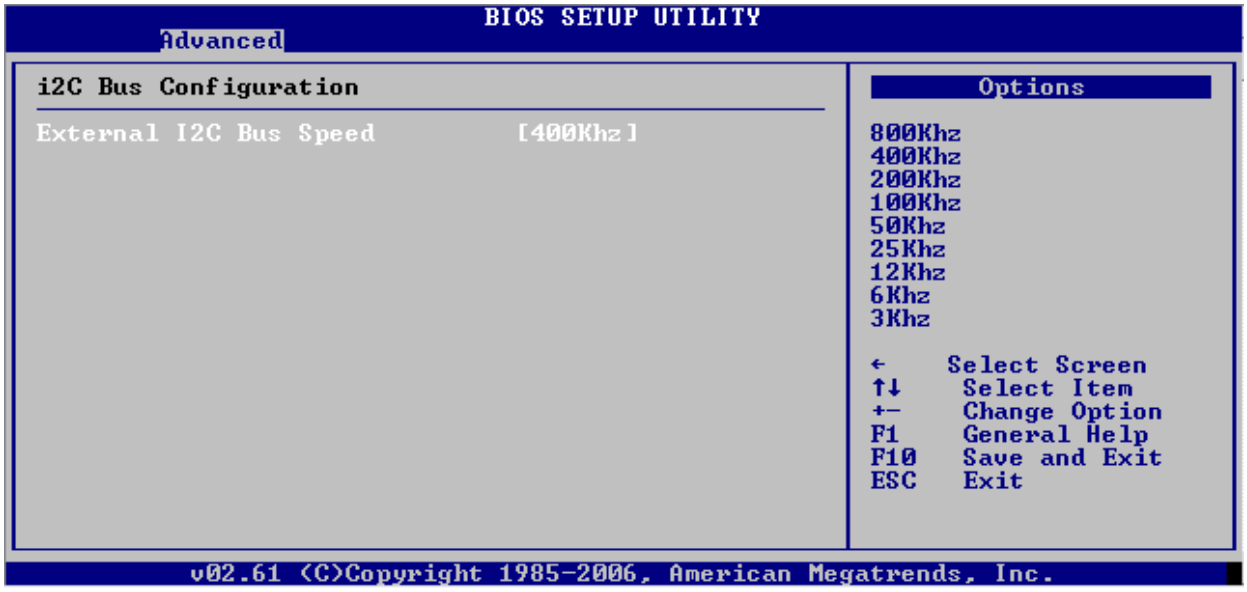
Feature	Option	Description
MARS	**Disabled** Auto SMB Charger SMB Manager	Enables the MARS function

Watchdog



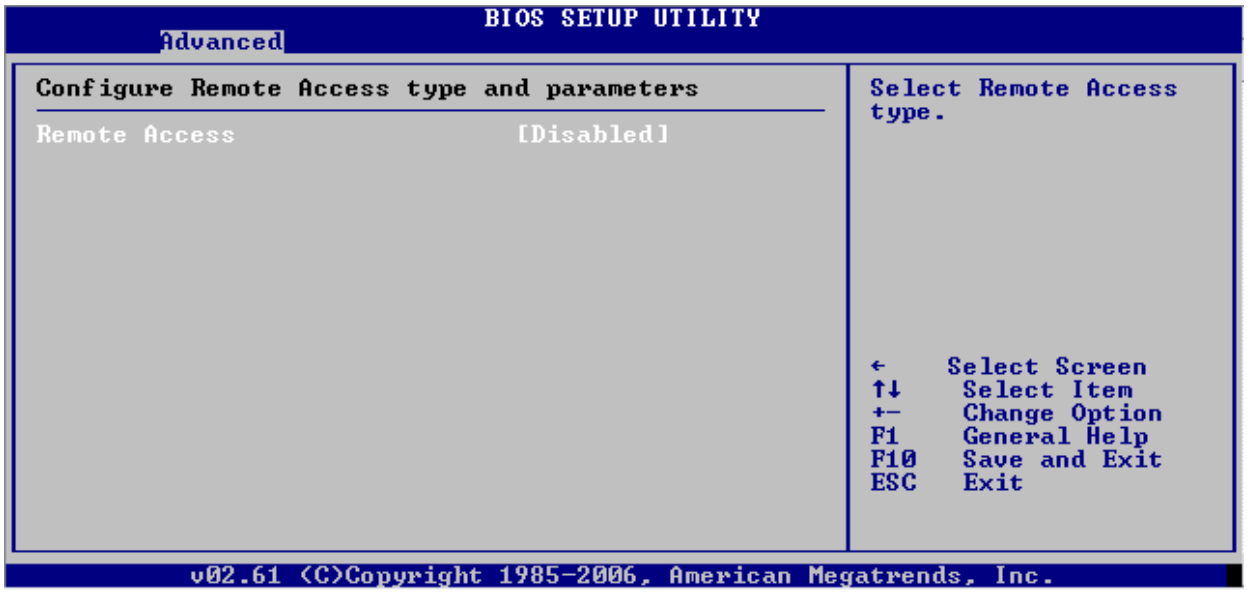
Feature	Option	Description
Mode	Reset **Disabled** NMI	Selects the mode of the watchdog
Delay	**Disabled** 1s 5s 10s 30s 1:00m 5:00m 10:00m 30:00m	Controls the delay after the watchdog is initialized
Timeout	**0.4s** 1s 5s 10s 30s 1:00m 5:00m 10:00m	Set the timout for Watchdog

I2C Busses



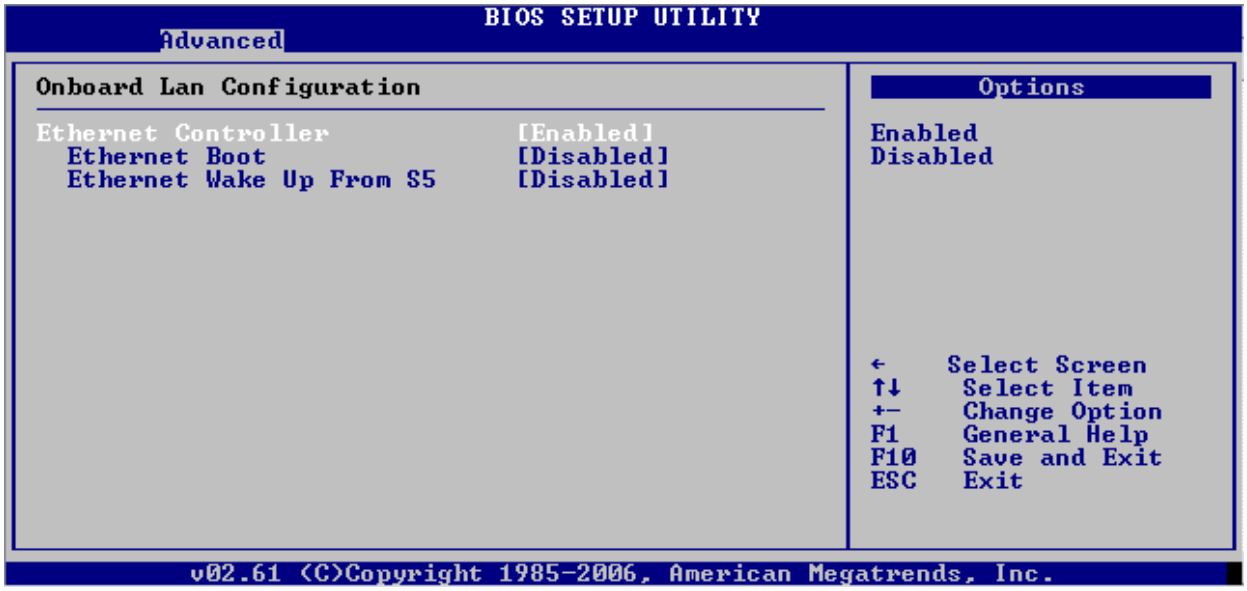
Feature	Option	Description
External I2C Bus Speed	800Khz **400Khz** 200Khz … 3Khz	Controls the Bus Speed of the external I2C bus

Remote Access Configuration



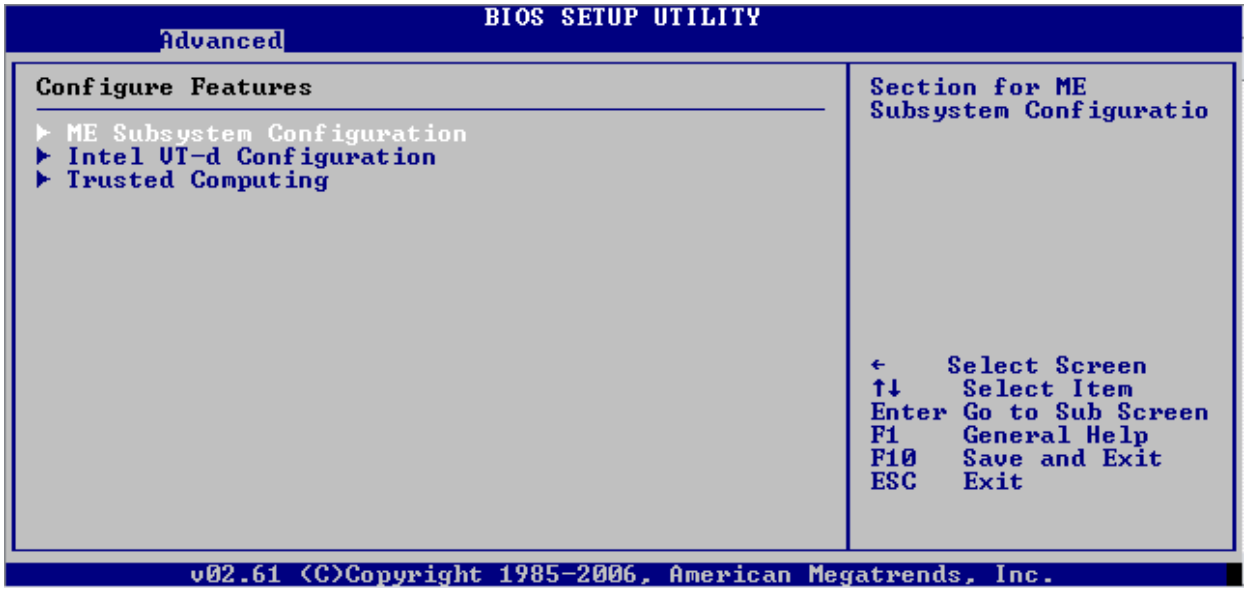
Feature	Option	Description
Remote Access	Enabled **Disabled**	Enables Remote Access via AMI Console Redirection

Ethernet Configuration

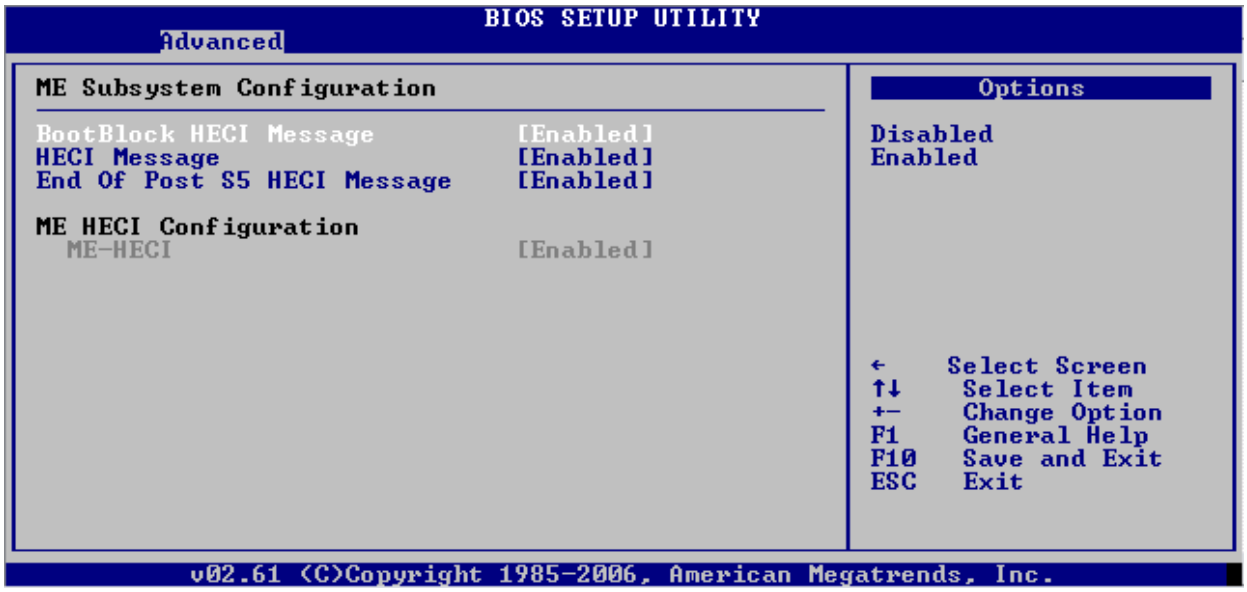


Feature	Option	Description
GbE LAN	Disabled **Enabled**	Disables / Enables the onboard Ethernet interface
GbE LAN Boot	**Disabled** Enabled	Disables / Enables the PXE Boot ROM
GbE Wake Up From S5	**Disabled** Enabled	Disables / Enables the WOL function from S5 ACPI state

Features



ME Subsystem Configuration



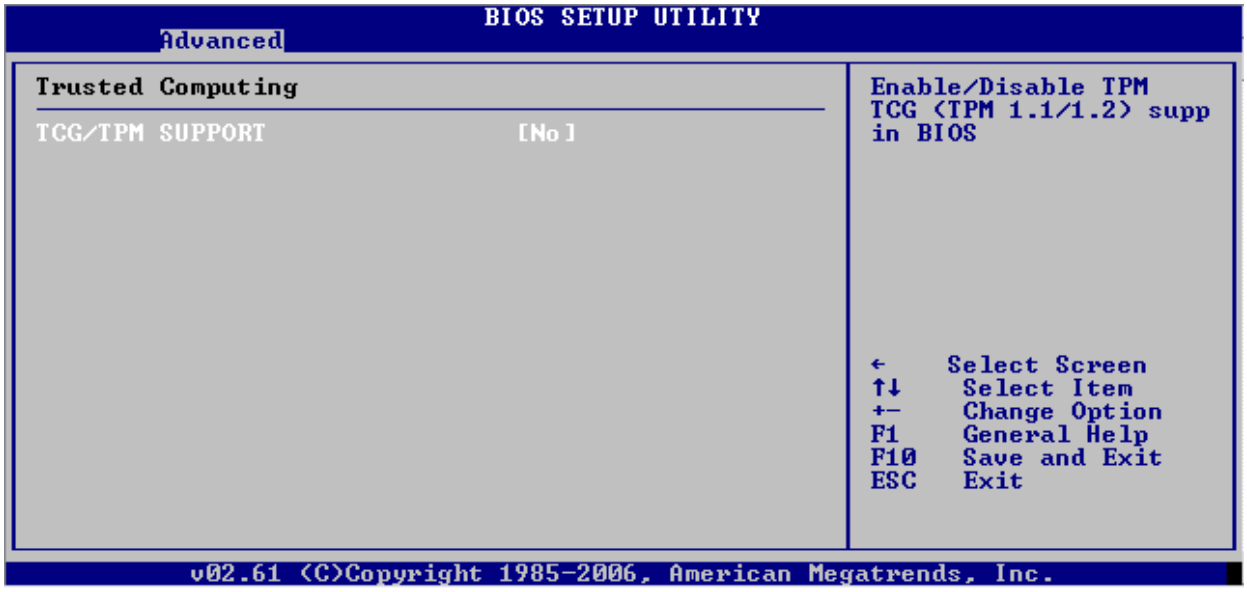
Feature	Option	Description
BootBlock HECI Message	**Enabled** Disabled	Selects the mode of the watchdog
HECI Message	**Enabled** Disabled	Enables / Disables the HECI Message
End of Post S5 HECI Message	**Enabled** Disabled	
ME-HECI	**Enabled** Disabled	

Intel VT-d Configuration



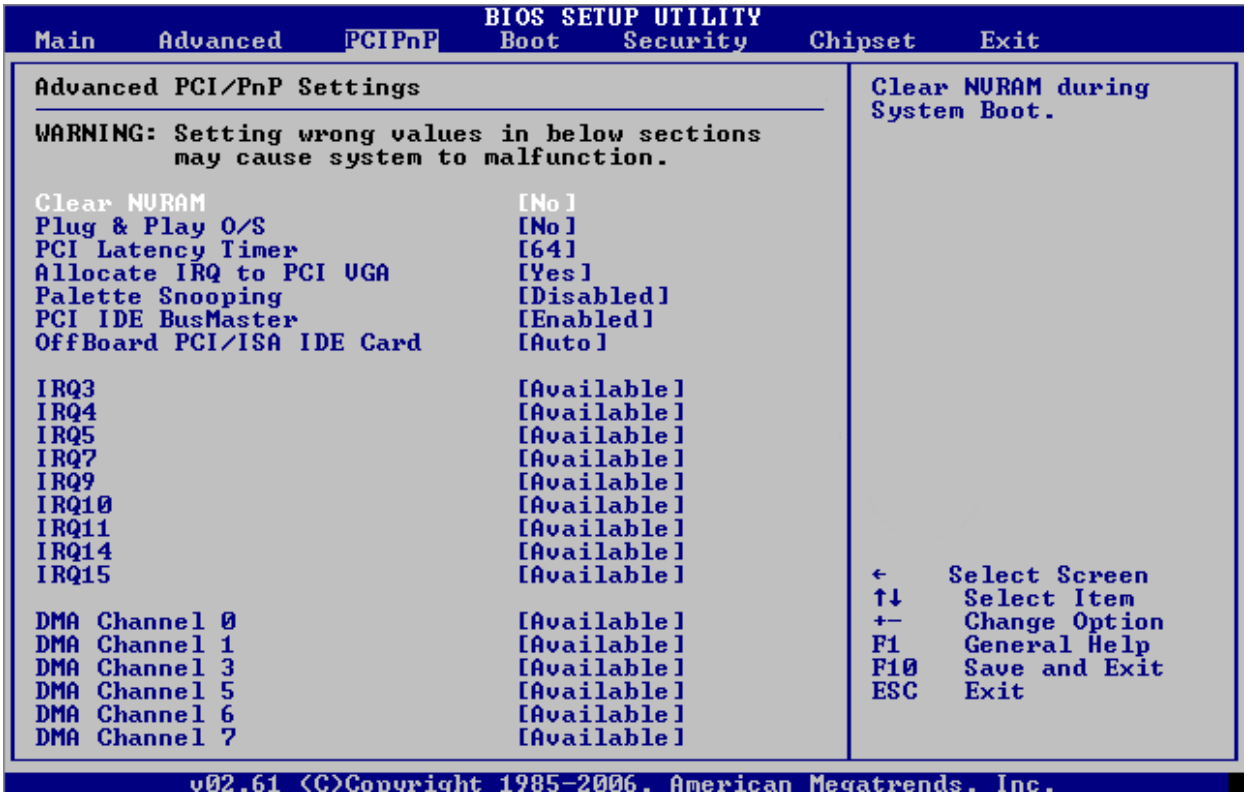
Feature	Option	Description
Intel VT-d	Enabled **Disabled**	Enables / Disables Intel Virtualisation Technology support

Trusted Computing



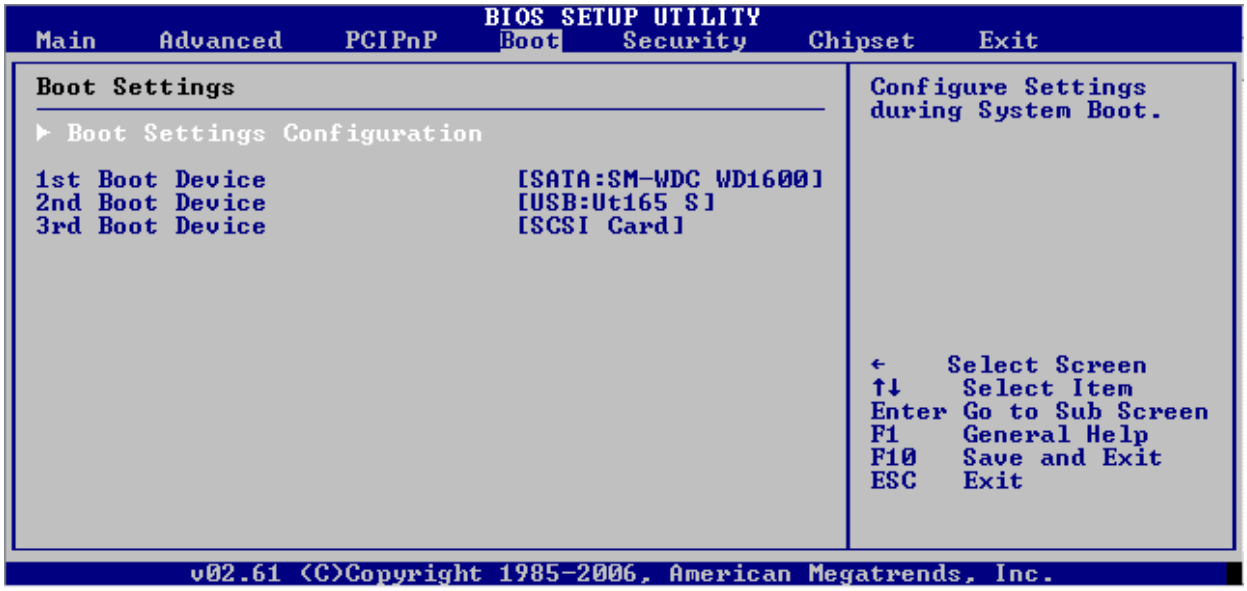
Feature	Option	Description
TCG/TPM Support	Yes **No**	Enables / Disables Trusted Computing and Trusted Platform Module

8.3.4 PCIPnP Menu



Feature	Option	Description
Clear NVRAM	**No** Yes	Clear NVRAM once during next system boot.
Plug & Play O/S	**No** Yes	No: all devices are initialized by BIOS Yes: OS has to initialize some devices
PCI Latency Timer	32 **64** … 248	Value in units of PCI clocks for PCI device latency register
Allocate IRQ to PCI VGA	**Yes** No	Decided if PCI VGA card does get an IRQ assigned if requested
Palette Snooping	**Disabled** Enabled	Disables and enables Palette Snooping
PCI IDE BusMaster	Disabled **Enabled**	Disables and enables PCI IDE Busmaster
OffBoard PCI/ISA IDE Card	**Auto** PCISlot 1 PCISlot 2 … PCISlot 6	Some IDE Cards needs this , with set to Auto it works with most cards
IRQ3 … IRQ15	**Available** Reserved	Available: IRQ useable by PCI/PnP devices Reserved: IRQ is reserved for ISA devices
DMA Channel 0 … DMA Channel 7	**Available** Reserved	Available: DMA useable by PCI/PnP devices Reserved: IRQ is reserved for ISA devices

8.3.5 Boot

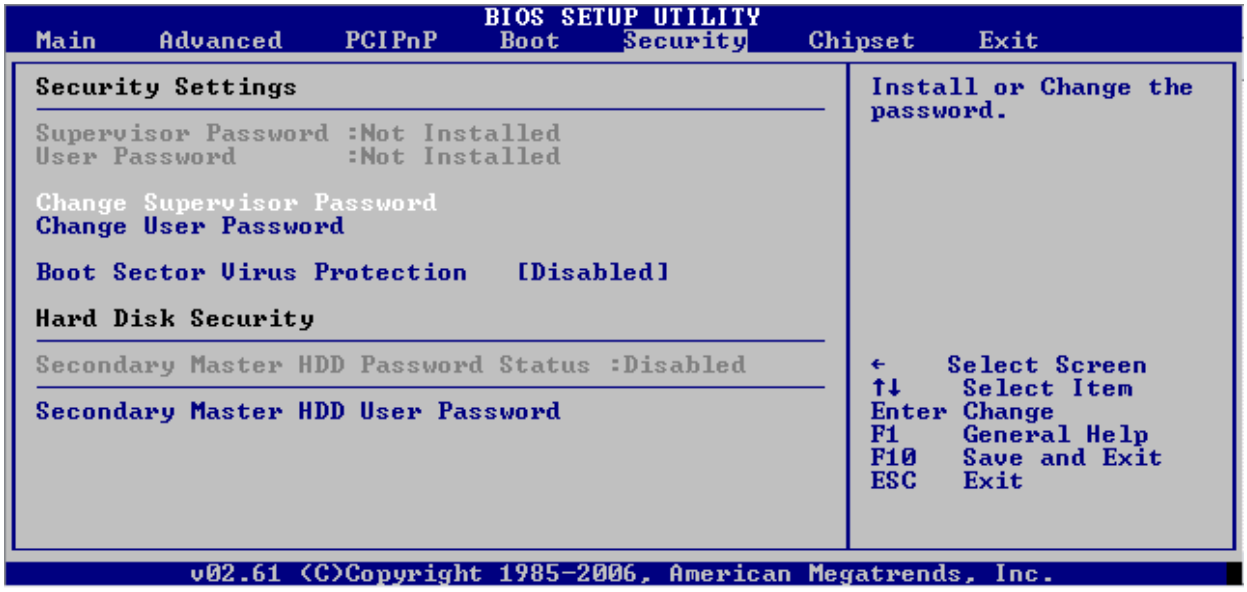

BIOS SETUP UTILITY
Main Advanced PCIPnP Boot Security Chipset Exit
Boot Settings
Boot Settings Configuration
1st Boot Device [SATA:SM-WDC WD1600]
2nd Boot Device [USB:Ut165 S]
3rd Boot Device [SCSI Card]
Configure Settings during System Boot.
← Select Screen
↑↓ Select Item
Enter Go to Sub Screen
F1 General Help
F10 Save and Exit
ESC Exit
v02.61 (C)Copyright 1985-2006, American Megatrends, Inc.

Boot Setting Configuration



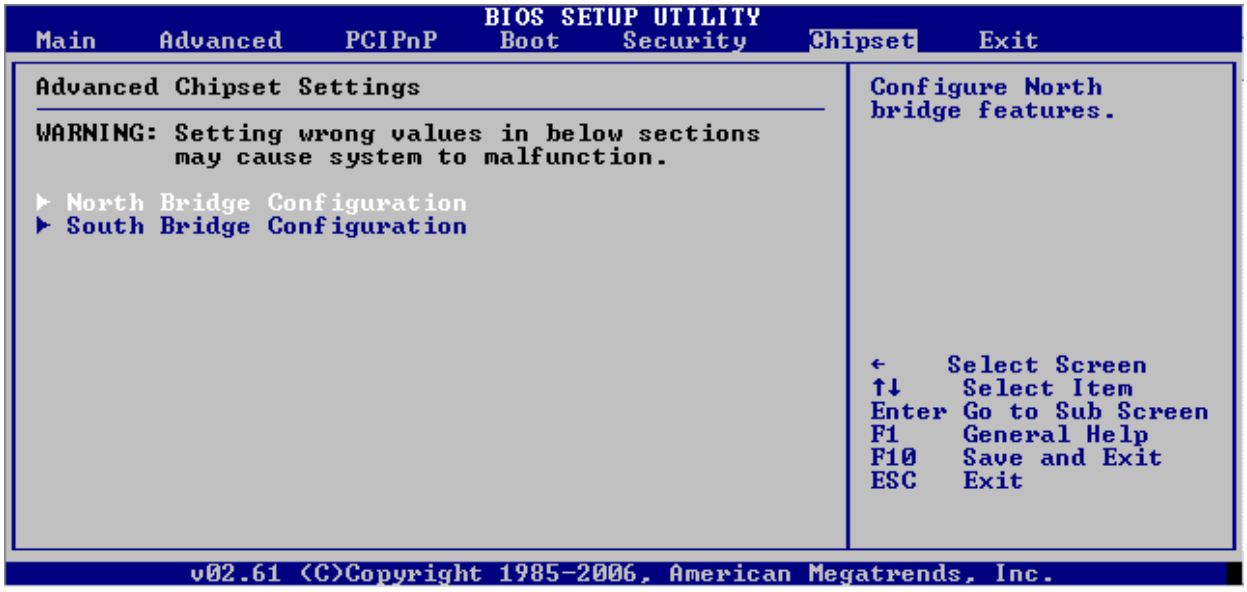
Feature	Option	Description
Quick Boot	**Enabled** Disabled	Disables or enables the quick boot feature
Quiet Boot	**Disabled** Enabled	Disabled: Shows normal POST messages Enabled: Shows OEM Logo during boot up
AddOn ROM Display Mode	**Force BIOS** Keep Current	Set Display Mode for Option ROM
Bootup Num-Lock	**On** Off	Select Power-On state for Num-Lock
PS/2 Mouse Support	**Auto** Disabled Enabled	Disables and enables or auto selects PS/2 Mouse Support
Wait For 'F1' If Error	**Disabled** Enabled	Wait for F1 key to be pressed, if error
Hit 'DEL' Message Display	**Enabled** Disabled	Displays: "Hit 'DEL' to run setup" during POST, if enabled
Boot USB HDD first	**Disabled** **Enabled**	If enabled, boots new attached USB HDD always first. If disabled, sets new attached USB HDD to last boot position
Interrupt 19 Capture	**Disabled** Enabled	Allows option ROMs to trap INT19h if enabled

8.3.6 Security

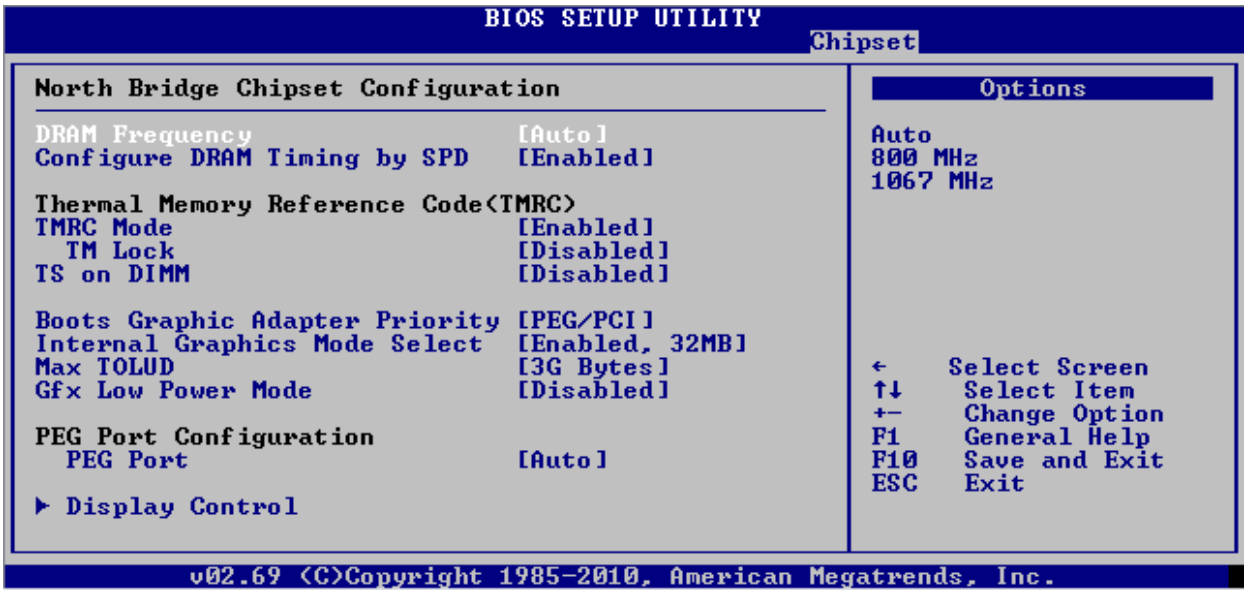


Feature	Option	Description
Change Supervisor Password	**Type in**	
Change User Password	**Type in**	
Boot Sector Virus Protection	**Disabled** Enabled	Enables or disables boot sector virus protection.

8.3.7 Chipset

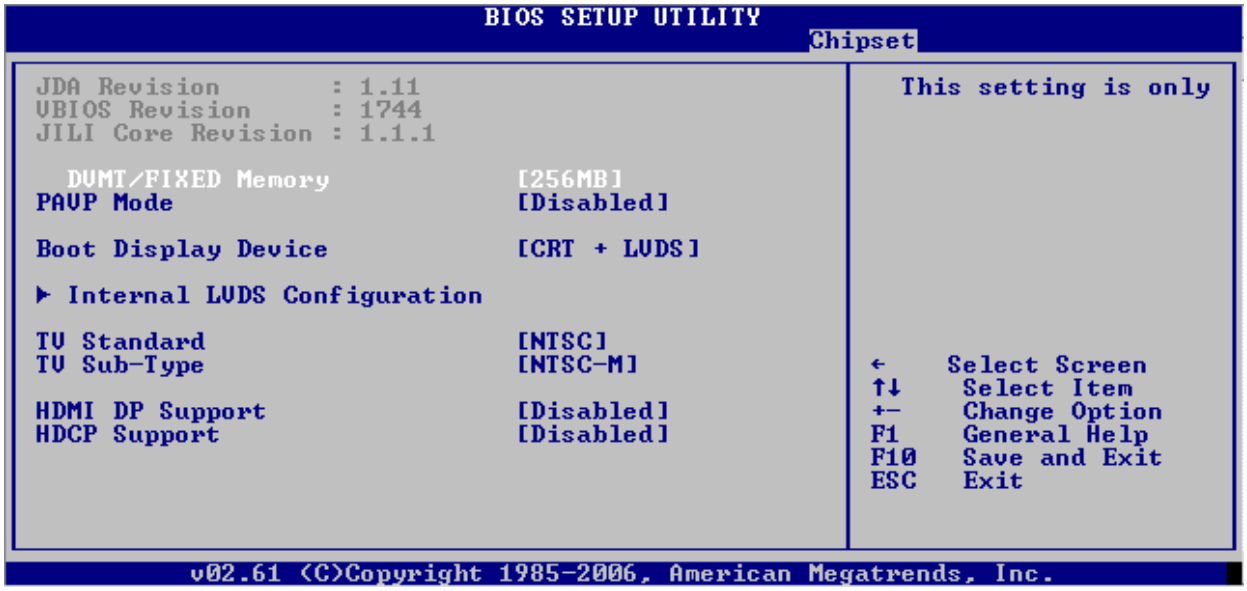

BIOS SETUP UTILITY
Main Advanced PCIPnP Boot Security Chipset Exit
Advanced Chipset Settings
WARNING: Setting wrong values in below sections may cause system to malfunction.
North Bridge Configuration
South Bridge Configuration
Configure North bridge features.
← Select Screen
↑↓ Select Item
Enter Go to Sub Screen
F1 General Help
F10 Save and Exit
ESC Exit
v02.61 (C)Copyright 1985-2006, American Megatrends, Inc.

North Bridge Configuration



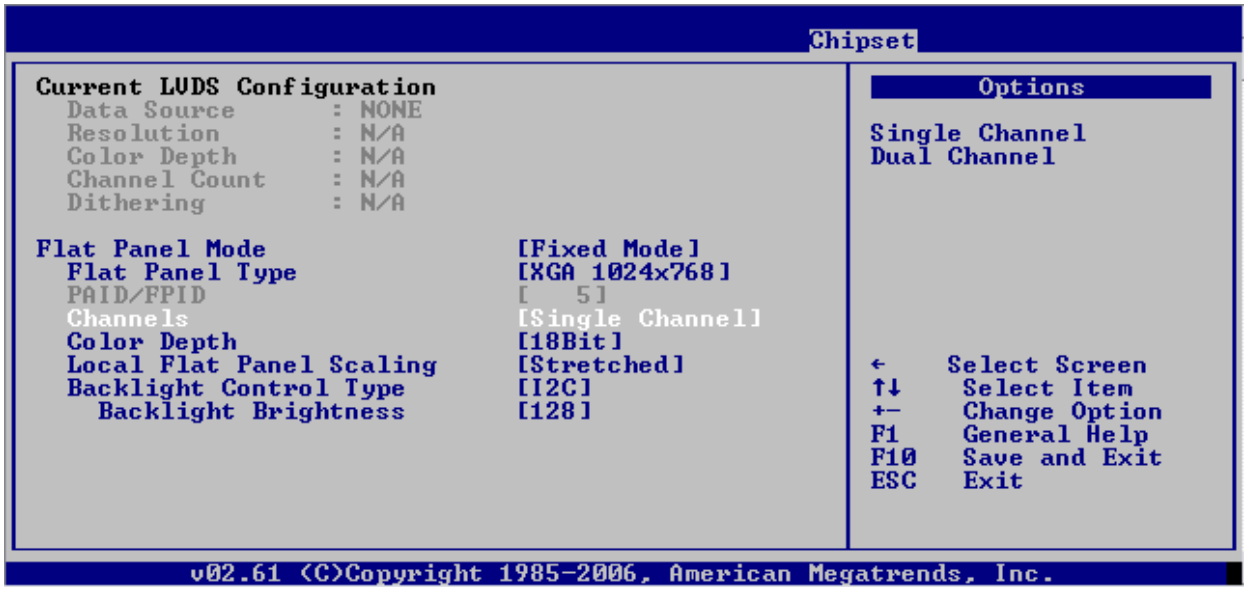
Feature	Option	Description
DRAM Frequency	**Auto** 800Mhz 1067Mhz	Selects the DRAM frequency
Configure DRAM Timing by SPD	Disabled **Enabled**	Disables and Enables automatic DRAM configuration via SPD EEPROM
TMRC Mode	Disabled **Enabled**	Disables and enables the Thermal Memory Reference Code
TM Lock	**Disabled** Enabled	Disables and enables the thermal sensor on lock
TS on DIMM	**Disabled** Enabled	Disables and enables the thermal sensor on DIMM
Boots Graphic Adapter Priority	IGD PCI/IGD PCI/PEG PEG/IGD **PEG/PCI**	Selects which graphics adapter is initialized during boot up and gets priority
Internal Graphics Mode Select	Disabled **Enabled, 32MB** Enabled, 64MB Enabled, 128MB	Select the mode for the interal graphicdevice
Max TOLUD	**3G Bytes** 2.5G Bytes 2G Bytes	Maximum value of "top of low usable DRAM"
Gfx Low Power Mode	**Disabled** Enabled	Disables and Enables the low power mode for the internal graphics device
PEG Port	**Auto** Disabled Enable PEG Port Always	Selects the initialization mode of the PCIexpress graphics port

Display Control



Feature	Option	Description
DVMT/FIXED Memory	128MB **256MB** Max DVMT	Configures the amount of memory for the Dynamic Video Memory Technology
PAVP Mode	**Disabled** Light High	Configures the Protected Audio Video Path
Boot Display Device	CRT TV SDVO CRT+SDVO LVDS **CRT+LVDS**	Selects the Boot Display Devices
TV Standard	**NTSC** PAL SECAM SMPTE240M ITU-R television SMPTE295M SMPTE296M EIA-770.2 EIA-770.3	Selects the regarding TV standard for TV out interface
TV Sub-Type	Depending on TV Standard	Selects the regarding TV Sub-Type
HDMI DP Support	**Disabled** Enabled	Enables and disables the HDMI DP Support
HDCP Support	**Disabled** Enabled	Enables and disables the HDCP Support

Internal LVDS Configuration



Feature	Option	Description
Flat Panel Mode	**Auto** Fixed Mode PAID FPID	Selects the Mode for the flat panel detection
Auto Fallback	**Disabled** Fixed Mode	Selects what happens, when there is no EEPROM detected (only when FPM: Auto)
Flat Panel Type	**VGA 640x480** … WXGA 1280x800	Selects the resolution of the LVDS display (only in FMP: Fixed Mode)
PAID/FPID	[X]	Selects the number of the PAID/FPID
Channels	**Single Channel** Dual Channel	Selects, if 1x or 2x LVDS signals are used (only in FPM: Fixed Mode)
Color Depth	**18bit** 24bit open LDI 24bit	Selects the Color Depth of the connected LVDS display (only in FPM: Fixed Mode)
Local Flat Panel Scaling	Centered **Stretched** Disabled	Selects the Scaling Options for the LVDS panel (only in FPM: Fixed Mode)
Backlight Control Type	None/External **I2C** PWM	Selects the mode for Backlight Control
Backlight Brightness	[0…255]	Selects the default setting for Backlight Brightness

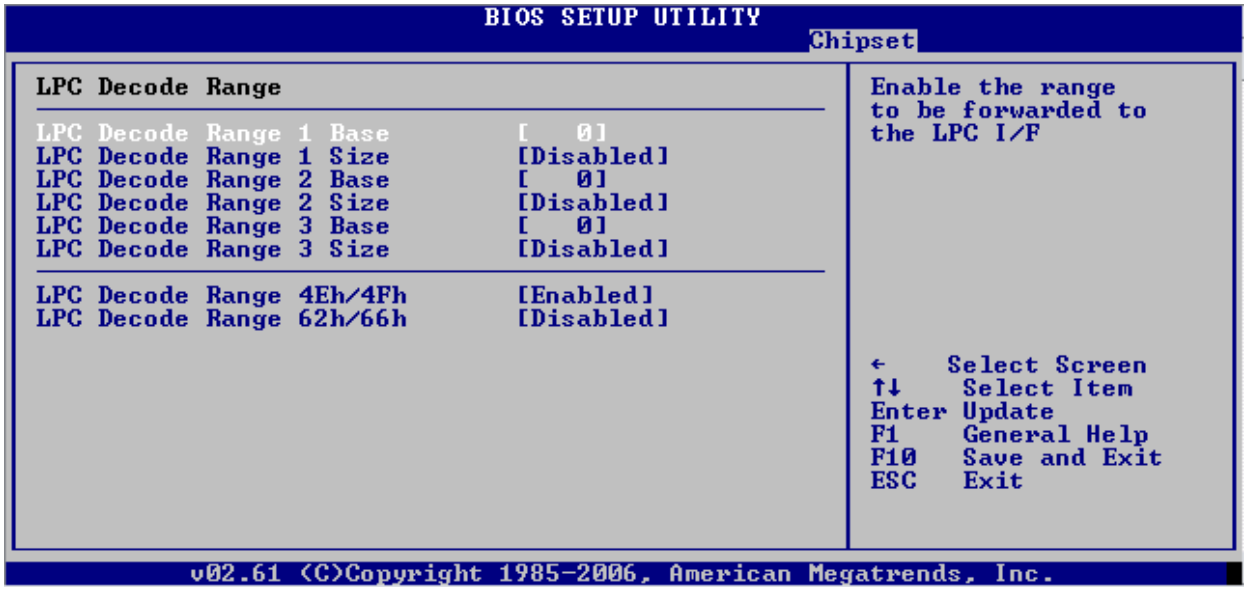
Southbridge Configuration



Feature	Option	Description
USB Functions	Disabled 2 USB Ports 4 USB Ports … 8 USB Ports + IDE	Enables / Disables USB ports*
USB Port Configure	**6+4 USB Ports** 8+2 USB Ports	Configures, how the ports are mapped internally to the USB controllers
USB 2.0 Controller	**Enabled** Disabled	Enables / Disables the USB 2.0 controller. (only available when there is USB2ATA port disabled)
Enable Lock Bit	Disabled **Enabled**	Enables Lock bit at end of POST. Only disable for debugging purposes.
Port 80h Output	**LPC** PCI	Selects the Inteface for Port 80h output during POST
Audio Controller	**Enabled** Disabled	Enables / Disables the HDA audio controller
SMBUS Controller	**Enabled** Disabled	Enables / Disables the SMBus controller

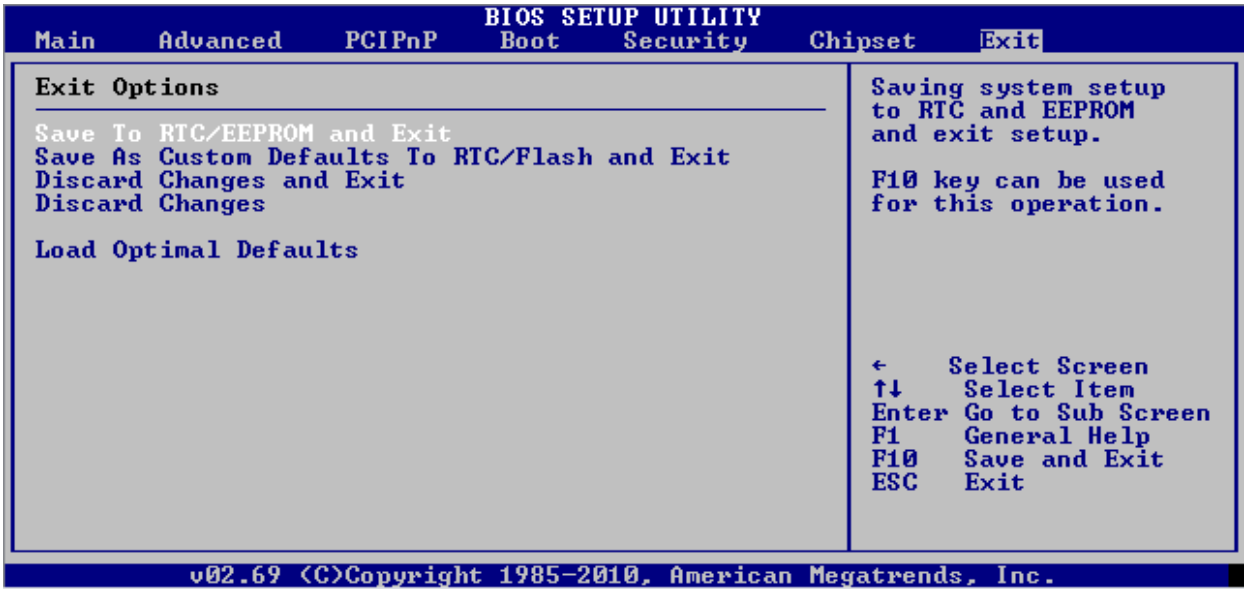
*Note: The parallel ATA channel is hosted by an USB2PATA bridge at the 9th USB port. Disabling this port will also disable parallel ATA!

LPC Decode Range



Feature	Option	Description
LPC Decode Range 1 Base	[0…FFFF]	Enter the Base Adress of the LPC decode range
LPC Decode Range 1 Size	**Disabled** 4 8 … 256	Size of the decode range in kB
LPC Decode Range 2 Base	[0…FFFF]	Enter the Base Adress of the LPC decode range
LPC Decode Range 2 Size	**Disabled** 4 8 … 256	Size of the decode range in kB
LPC Decode Range 3 Base	[0…FFFF]	Enter the Base Adress of the LPC decode range
LPC Decode Range 3 Size	**Disabled** 4 8 … 256	Size of the decode range in kB
LPC Decode Range 4Eh/4Fh	**Enabled** Disabled	Enables disables the LPC decode range at 4Eh/4Fh
LPC Decode Range 62h/66h	**Disabled** Enabled	Enables disables the LPC decode range at 62h/66h

8.3.8 Exit Menu



9 Appendix A: JIDA Standard

Every board with an on-board BIOS extension supports the following function calls, which supply information about the board. Jumptec Intelligent Device Architecture (JIDA) functions are called via Interrupt 15h. Functions include:

- AH=Eah
- AL=function number
- DX=4648h (security word)
- CL=board number (starting with 1)

The interrupt returns a CL□0 if a board with the number specified in CL does not exist. CL will equal 0 if the board number exists. In this case, the content of DX determines if the operation was successful. DX=6B6Fh indicates success; other values indicate an error.

9.1 JIDA Information

To obtain information about boards that follow the JIDA standard, use the following procedure.

- Call Get BIOS ID with CL=1. The name of the first device installed will be returned. If you see the result Board exists (CL=0), increment CL, and call Get BIOS ID again.
- Repeat until you see Board not present (CL□0). You now know the names of all boards within your system that follow the JIDA standard.
- You can find out more information about a specific board by calling the appropriate inquiry function with the board's number in CL.

Note:	Association between board and board number may change because of configuration changes. Do not rely on any association between board and board number. Always use the procedure described above to determine the association between board and board number.

Refer to the JIDA manual in the jidai1xx.zip folder, which is available from the Kontron Web site, for further information on implementing and using JIDA calls with C sample code.

10 Appendix B: Architecture Information

The following sources of information can help you better understand PC architecture.

10.1 Buses

10.1.1 ISA, Standard PS/2 – Connectors

- AT Bus Design: Eight and Sixteen-Bit ISA, E-ISA and EISA Design, Edward Solari, Annabooks, 1990, ISBN 0-929392-08-6
- AT IBM Technical Reference Vol 1&2, 1985
- ISA & EISA Theory and Operation, Edward Solari, Annabooks, 1992, ISBN 0929392159
- ISA Bus Specifications and Application Notes, Jan. 30, 1990, Intel
- ISA System Architecture, Third Edition, Tom Shanley and Don Anderson, Addison-Wesley Publishing Company, 1995, ISBN 0-201-40996-8
- Personal Computer Bus Standard P996, Draft D2.00, Jan. 18, 1990, IEEE Inc
- Technical Reference Guide, Extended Industry Standard Architecture Expansion Bus, Compaq 1989

10.1.2 PCI/104

- Embedded PC 104 Consortium
- The consortium provides information about PC/104 and PC/104-Plus technology. You can search for information about the consortium on the Web.
- PCI SIG
- The PCI-SIG provides a forum for its ~900 member companies, who develop PCI products based on the specifications that are created by the PCI-SIG. You can search for information about the SIG on the Web.
- PCI & PCI-X Hardware and Software Architecture & Design, Fifth Edition, Edward Solari and George Willse, Annabooks, 2001, ISBN 0-929392-63-9.
- PCI System Architecture, Tom Shanley and Don Anderson, Addison-Wesley, 2000, ISBN 0-201-30974-2.

10.2 General PC Architecture

- Embedded PCs, Markt&Technik GmbH, ISBN 3-8272-5314-4 (German)
- Hardware Bible, Winn L. Rosch, SAMS, 1997, 0-672-30954-8
- Interfacing to the IBM Personal Computer, Second Edition, Lewis C. Eggebrecht, SAMS, 1990, ISBN 0-672-22722-3
- The Indispensable PC Hardware Book, Hans-Peter Messmer, Addison-Wesley, 1994, ISBN 0-201-62424-9
- The PC Handbook: For Engineers, Programmers, and Other Serious PC Users, Sixth Edition, John P. Choisser and John O. Foster, Annabooks, 1997, ISBN 0-929392-36-1

10.3 Ports

10.3.1 RS-232 Serial

» EIA-232-E standard

» The EIA-232-E standard specifies the interface between (for example) a modem and a computer so that they can exchange data. The computer can then send data to the modem, which then sends the data over a telephone line. The data that the modem receives from the telephone line can then be sent to the computer. You can search for information about the standard on the Web.

» RS-232 Made Easy: Connecting Computers, Printers, Terminals, and Modems, Martin D. Seyer, Prentice Hall, 1991, ISBN 0-13-749854-3

» National Semiconductor: The Interface Data Book includes application notes. Type “232” as search criteria to obtain a list of application notes. You can search for information about the data book on National Semiconductor’s Web site.

10.3.2 Serial ATA

Serial AT Attachment (ATA) Working Group. This X3T10 standard defines an integrated bus interface between disk drives and host processors. It provides a common point of attachment for systems manufacturers and the system. You can search for information about the working group on the Web. We recommend you also search the Web for information on 4.2 I/O cable, if you use hard disks in a DMA3 or PIO4 mode.

10.3.3 USB

USB Specification

USB Implementers Forum, Inc. is a non-profit corporation founded by the group of companies that developed the Universal Serial Bus specification. The USB-IF was formed to provide a support organization and forum for the advancement and adoption of Universal Serial Bus technology. You can search for information about the standard on the Web.

10.4 Programming

» C Programmer’s Guide to Serial Communications, Second Edition, Joe Campbell, SAMS, 1987, ISBN 0-672-22584-0

» Programmer’s Guide to the EGA, VGA, and Super VGA Cards, Third Edition, Richard Ferraro, Addison-Wesley, 1990, ISBN 0-201-57025-4

» The Programmer’s PC Sourcebook, Second Edition, Thom Hogan, Microsoft Press, 1991, ISBN 1-55615-321-X

» Undocumented PC, A Programmer’s Guide to I/O, CPUs, and Fixed Memory Areas, Frank van Gilluwe, Second Edition, Addison-Wesley, 1997, ISBN 0-201-47950-8

11 Appendix C: Document Revision History

Revision	Date	Edited by	Changes
0.1	16-Mar-2010	CAV	Initial draft
0.2	2-July-2010	CAV	Various updates
1.0	19-July-2010	CAV	Added: MTBF and updated BIOS info
1.1	21-July-2010	CAV	Various updates
1.2	13-Sept-2010	CAV	Updated MTBF
1.3	13-Jan-2011	CAV	Updated table 7.10.4
1.4	8-April-2011	CAV	Updates throughout

Corporate Offices

Europe, Middle East & Africa

Oskar-von-Miller-Str. 1
85386 Eching/Munich
Germany
Tel.: +49 (0)8165/ 77 777
Fax: +49 (0)8165/ 77 219
info@kontron.com

North America

14118 Stowe Drive
Poway, CA 92064-7147
USA
Tel.: +1 888 294 4558
Fax: +1 858 677 0898
info@us.kontron.com

Asia Pacific

17 Building, Block #1,ABP.
188 Southern West 4th Ring
Beijing 100070, P.R.China
Tel.: + 86 10 63751188
Fax: + 86 10 83682438
info@kontron.cn