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Gamma7

Gamma7-CPU	**Nr. 000210**
Gamma7-VME	**Nr. 000211**
Gamma7-HDD	**Nr. 000215**
Gamma7-104AD	**Nr. 000216**

User's Manual

VMEbus-PC with PIII-CPU, Graphic and Net

Preface

The purpose of this manual is to explain and simplify the installation, the applications and the modification of the hardware/software documented in the following chapters.

If you have any problems when using this product, please try to reproducebly fix the error, then to check all DIP-switch settings, jumpers, connector pin assignments and all software setup parameters before calling.
Due to the versatility and complexity of the acquired product, it is possible that even one detail omitted causes uncorrect functioning of the product.

The information in this manual has been carefully checked and is believed to be entirely reliable. We would like to excuse ourselves for any inaccuracies due to translation. Please report any mistakes to Kontron Solutions.

Kontron Solutions reserves the right to make changes to both hardware and software, to improve the function or to facilitate the operation of the products. Those changes will not necessarily be documented.

Publishing, storage or processing in computer systems, as well as reprint, translation in whole, or in part of this manual need a written approval of Kontron Solutions.

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Andreas Huber

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Any changes to the manual are listed below in a brief description:

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0A	draft for correction	23.03.2000	A.H.	New design GAMMA7
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Symbols and Conventions

If not otherwise specified, groups of bits are written in binary notation, followed by a "b" - e.g.: 101b

If not otherwise specified, addresses and contents of registers are written in hexadecimal notation, followed by a "h". Hexadecimal digits are written in upper case - e.g.: EF002h

B is the short form of byte; b the short form of bit.

k means factor 400h (1 024 decimal).

M means factor 100 000h (1 048 576 decimal)



STOP. Important note. Skipping this material possibly causes errors or damage to the system.



Important note. Recommendation for proper function.



General hints for better understanding.

1. Introduction

The following “Introduction” provides an outline of the performance of the Gamma7 VMEbus PC and its specifications.

Chapter 2, “Functional Description”, describes the tasks and functions of the various Gamma7 components. This chapter provides a better understanding of the interrelated functions of the Gamma7 VMEbus PC prior to initial operation.

Chapter 3, “Safety Guidelines”, with regard to operation and maintenance, describes potential error sources. It is therefore essential that you read this chapter.

Chapter 4, “Installation”, contains the entire information essential for initial installation and subsequent configuration. A brief, clear overview provides setting options for configuring the modules for operation. Depending upon the module, steps that may be necessary for installing the driver are listed as well.
This chapter contains important instructions for the Gamma7 configuration and initial installation. It is therefore essential that you read this chapter prior to operating the Gamma7!

Chapter 5, “Programmer’s Reference”, describes the Gamma7 memory areas and registers and follows the PC architecture by examining the I/O area separately from the memory areas. Special attention should be paid to the description of the capability to also address VMEbus memory areas through PC I/O access.
This chapter is an essential reference for the software developer.

Chapter 6 provides several examples of commonly used kernel routines for initialization, data transfers and interrupt handling.

Chapter 7, “Error Corrections / Troubleshooting”, describes the troubleshooting methods, as well as tools and possible solutions.

Chapter 8 contains codes for new and additional orders. Use this information to check the correct delivery of your Gamma7.

The appendix provides a comprehensive reference. ***Literature*** provides recommended readings for reinforcing basic and special information. ***Abbreviations and Index*** is used to quickly locate specific terminology. Finally, a pre-formatted ***Error Report*** enables the fast processing of possible errors. ***Data Sheets*** of several programmable components provide supplemental information about using internal registers. The ***Board Layout*** is used as reference for the location of the jumper and solder bridge configuration elements.

Depending upon the configuration, the Gamma7 VMEbus PC consists of the following boards/modules:

- Gamma7-CPU
- Gamma7-VME
- Gamma7-HDD
- Gamma7-104AD
- VCPU486-ISA2

This manual describes the Gamma7 without the ISABUS adapter VCPU486-ISA2. A separate User's Manual exists for that module.

Due to the modular design of the Gamma7, each chapter contains a subchapter for the corresponding module.

1.1. General Description

Depending upon the model, the Gamma7 Industrial PC consists ***functionally*** of the following modules:

- CPU and memory
- PCI modules (internal)
  - VGA graphics
  - Ethernet controller
  - VMEbus interface
  - Ultra DMA/33 IDE interface (HDD)
  - USB
- ISABUS modules (internal)
  - I/O controller for serial ports, parallel port and FDD
  - Watchdog, NMI
- ISABUS adapter / PC/104 adapter

These functions are integrated on the following ***boards***:

- CPU and memory, I/O controller - Gamma7-CPU
  Ultra DMA/33 IDE interface,
  Watchdog, NMI timer,

- VGA graphics, network - Gamma7-VME
  and VMEbus interface

- Mass storage adapter - Gamma7-HDD
  Connection for FDD, HDD
  with 2.5“ HDD

- PC/104 adapter - Gamma7-104AD

- ISABUS adapter - VCPU486-ISA2

In a volume of less than 1000 cm^3, the Gamma7 (see Fig. 2: Gamma7 – Block Diagram) integrates all of the electronics components that are usually spread over motherboard, interface controller card, VGA card, and hard disk in typical PCs. In harsh environments, the Gamma7 can be equipped with a bootable silicon disk to avoid rotating storage media.



Fig. 1: Gamma7 - Overview

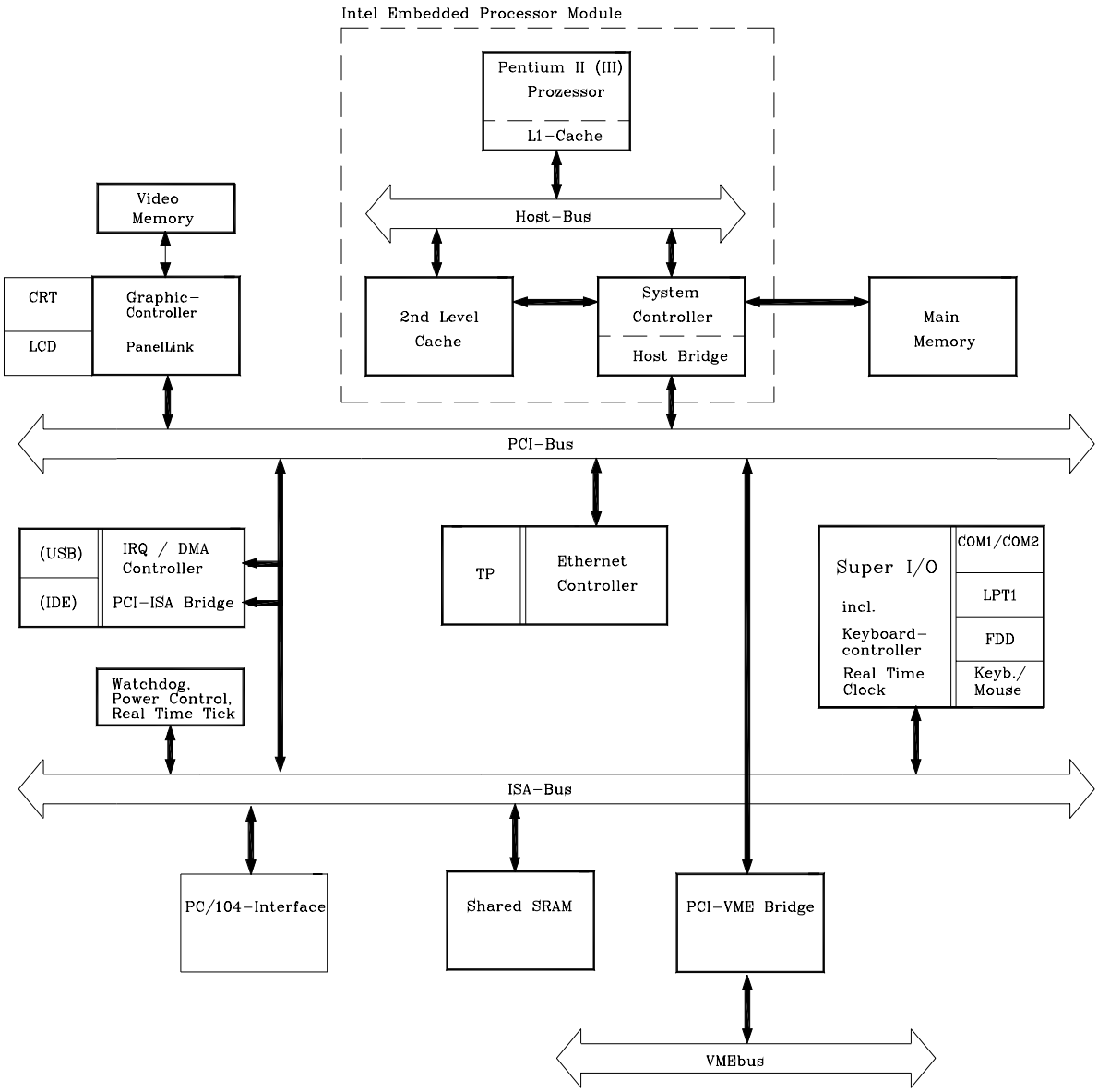


Fig. 2: Gamma7 – Block Diagram

1.2. Features

- Processor: Intel® Pentium® III Embedded Module, 500 MHz
- L1/L2 cache integrated on-board
- Up to 256 MB SDRAM on-board memory
- 3.3 V SDRAM DIMM modules with / w/o ECC
- Entire main memory is cacheable
- Intel‘s 82440BX AGPset: 82443BX Host Bridge Controller and 82371EB PCI ISA IDE Controller (PIIX4E)
- Super VGA with PCI interface, Lynx 3DM with 4/8 MB graphics memory
- CRT and LCD direct connection via DVI (Digital Video Interface) interface, simultaneous modes possible
- Ultra DMA/33 IDE interface for 2 IDE drives
- Mass storage:
  Hard disk with more than 3 GB
  Silicon disk with 32 MB flash memory, each IDE-compatible
- “General Software” – Bios, per software update
- USB interface
- VMEbus chip – Universe II® by Tundra Semiconductor Corporation
  - VME-to-PCI bus bridge
  - PCI 2.1 compliant
  - VME64 compliant
- Ethernet with 10Base-T and 100Base-Tx network connection, conforming to IEEE802.3, NE2100 compatible, LED for:
  - Active Link (AL)
  - Active Transmit (Tx)
  - Active Receive (Rx)
- Serial ports conforming to RS232 (COM1 and COM2); 16C550 compatible
- Parallel port (LPT1), ECP, EPP, SPP
- PS/2 keyboard and mouse
- FDD also as 2.88 MB drives
- Extensions via ISABUS or PC/104
- Watchdog timer function for monitoring local software and hardware
- NMI timer for real-time operation under Windows

- LED control displays for
  - enabled watchdog (WDG),
  - supply voltage (PWR), and
  - active hard disk (HDD)
- Real-time clock with calendar and alarm
- Reset from VMEbus via SYSRESET
- Keyboard reset also results in VMEbus interface reset

1.3. Technical Specification

1.3.1. Gamma7 (CPU / General)

CPU:	Intel Pentium III with 500 MHz, L1 cache 16 KB instructions and 16 KB data, L2 cache 256 KB, 256 MB cacheable
Main memory :	DIMM modules, available with 16 to 256 MB SDRAM
BIOS ROM:	8 Mbit FEPROM, 8 Bit common SYSTEM/VGA BIOS
Chipset:	Intel 440BX AGP set, consisting of: 82443BX Host Bridge/Controller and 82371AB (PIIX4) PCI / ISA Bridge
Real-time clock:	integrated in PIIX4 backup via battery or +5V STDBY from VMEbus

Mass storage:

- FDD: from standard to 2.88 and 4 MB drives,
  controller NEC uPD72065B compatible,
  connection on HDD adapter board: 34-pin
  standard contact strip for male IDC connector
- HDD: Local bus fast IDE interface
  for PIO-Mode 0-4 and Ultra DMA/33 drives
  connection on HDD adapter board:
  40-pin standard contact strip for male IDC connector
- Silicon flash disk

Network connection: AMD79C975
100Base-Tx connection conforming to IEEE 802.3

ISABUS interface: IEEE P996 compliant, available via adapter
VCPU486-ISA2

PC/104 interface: IEEE P996.1 compliant, available via adapter G7-104AD

I/O interfaces:

- EIA: RS232 compliant
  2 * serial: COM1 and COM2
  NS16650 compatible, 16 Bytes FIFOs,
  on front plate, 9-pin male DSUB connector

- IEEE1284-A compliant
  1 * parallel: LPT1
  ECP, EPP, Fast
  Centronics compatible
  128 Bytes FIFO, DMA capable
  on front plate, 25-pin female DSUB connector

- PS/2 compatible keyboard connection
  on front plate, 6-pin female Mini DIN connector

- Option: PS/2 mouse connection via Y cable

- USB according to Specification 1.1

Shared memory: 256 KB SRAM, battery-backed,

Watchdog: Trigger interval 400 ms
(reset triggered by time-out)
optical display in front plate (yellow LED), whether watchdog is enabled

Voltage monitoring: Reset signal for Vcc < 4.65 Volt
green LED Vcc > 4.85 Volt

Voltage supply +5V:

- Range: 4.875..5.25 Volt
- Ripple/Noise < 10 MHz: max. 50 mV (peak-peak)

- Power consumption: approx. 6 A (Version G7-4B0)

Mechanical system: 3 HE (height modules), 3 slots (without ISABUS extension)
6 HE (height modules) (with ISABUS extension)

Weight: approx. 0.5 kg

Operating temperature: 0..55 °C (when using hard disk)

1.3.2. Gamma7-VME

1.3.2.1. VMEbus Interface Functional Group

Local interface: PCI interface with Universe IIB

External interface: complete master/slave VMEbus interface
on VG96 connector, IEEE1014-1987 compliant, mailbox register

- Master: A24:D16, A16:D16, RMW
- Bus requester: (RWD, ROR, ROC, FAIR)
  Request level 0..3
- Slave: A24:D16, RMW (256 KB shared SRAM)
  A16:D08(O) (mailbox register)
- Interrupt handler: IH(1-7):D08 (each level is maskable)
- Interrupter: I(1-7):D08:ROAK, vectors are programmable
- All system controller functions:
  IACK daisy chain driver
  arbiter (SGL, PRI, RRS)
  system clock driver
  reset generator

1.3.2.2. VGA Graphics Adapter Functional Group

Graphics memory: 3D graphics controller SMI Lynx 3DM
PCI interface, 8 MB internal graphics memory

Refresh rate: Up to 85 Hz for 640 * 480, 32-bit colors

CRT: resolution up to 1280 * 1024 pixels for up to 24-bit colors

LCD: resolution up to 1600 * 1200 pixels for up to 24-bit colors
technologies LCD Single /Dual scan, TFT simultaneous
VGA/LCD display, Panel Link interface

1.3.2.3. Network Functional Group

Network controller: Am79C975 by AMD,
10/100 Mbit PCI Ethernet controller with Twisted Pair interface,
IEEE 802.3 compliant,
optional BootPROM support

LEDs: green LED – sending data
yellow LED – receiving data
red LED – active network connection

1.3.3. Gamma7-HDD

Integrated mass storage size:
32 MB to 1 GB silicon disk
or at least 3 GB HDD

External storage media: additional AT-IDE compatible storage medium
and 2 floppy disk drives connectable

Voltage supply: provided via module Gamma7-CPU,

1.3.4. Gamma7-104AD

Voltage supply: +5V, +12V provided via module Gamma7-CPU,
-12V for the PC/104 interface provided externally via
a separate male connector

2. Functional Description

2.1. Mechanical Construction

2.1.1. Boards

The standard Gamma7 model consists of 3 boards:

- Base board Gamma7-VME with VGA graphics, network and VMEbus interface
- Gamma7-CPU add-in board with all motherboard functions, incl. shared SRAM
- HDD add-in board as mass storage adapter

The boards Gamma7-CPU/Gamma7-VME are connected via an interface (Kontron Solutions PCIBUS) that corresponds electrically to a 3.3 V PCIBUS.

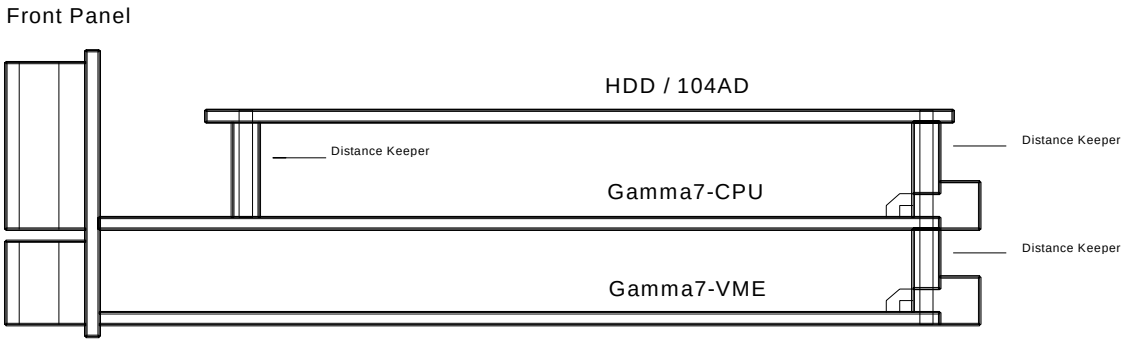


Fig. 3: Gamma7 - Construction

2.1.2. Front Plate

The width of the front plate is three slots (12 TE [depth modules] or 6.0 mm). The front plate is equipped with 2 serial ports (9-pin male DSUB connector) for COM1 and COM2, one parallel port (25-pin female DSUB connector) for LPT1, one USB interface for Series A connector, one female PS/2 connector for keyboard and mouse, one DVI interface for analog VGA monitors / digital LCDs and one female RJ45 connector for the network. The front plate also contains a momentary contact switch for RESET. This switch is recessed into the front plate and can only be operated with a tool (tip of a pen, small screw driver). The digital LCD interface (PanelLink) is trimmed using ADJ (PT1).

Six LEDs indicate status information:
Top left, yellow LED: HDD, active HDD
Top left, green LED: PWR, correct voltage supply > 4.85V
Top left, red LED: WDOG, enabled watchdog

Bottom left, yellow LED: Receive, receiving data packets
Bottom left, green LED: Transmit, sensing data packets
Bottom left, red LED: Active link, network connection exists

Two types of the Gamma7 front plate are available:

1. 3 HE (height modules) (see Figure 5, height approx. 13 cm) standard Gamma7 front plate
2. 6 HE (see Figure 4, height approx. 26 cm), allows for insertion of standard ISA cards (8 bit / 16 bit)

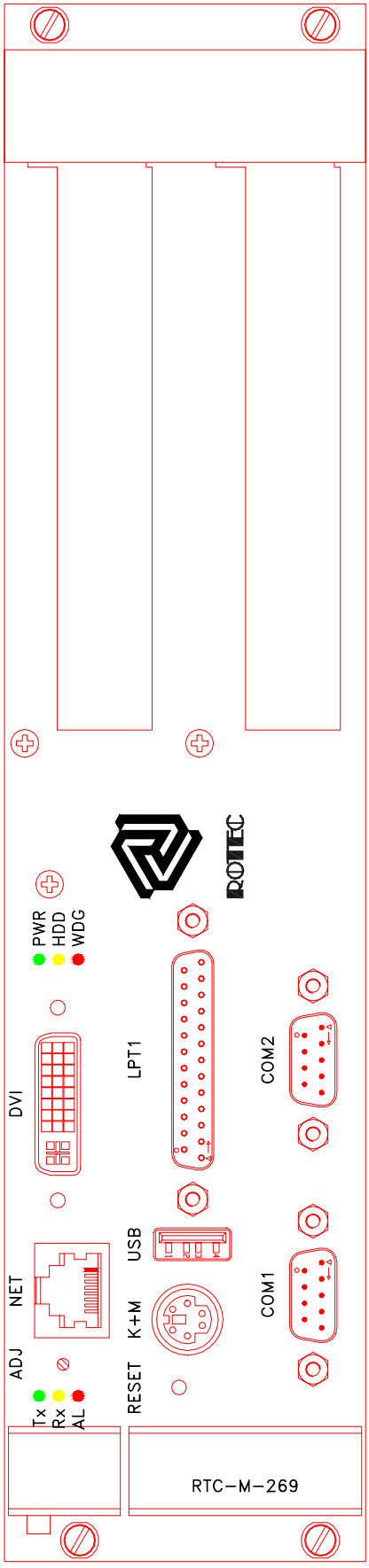


Fig. 4: Gamma7 (6 HE) - Front View

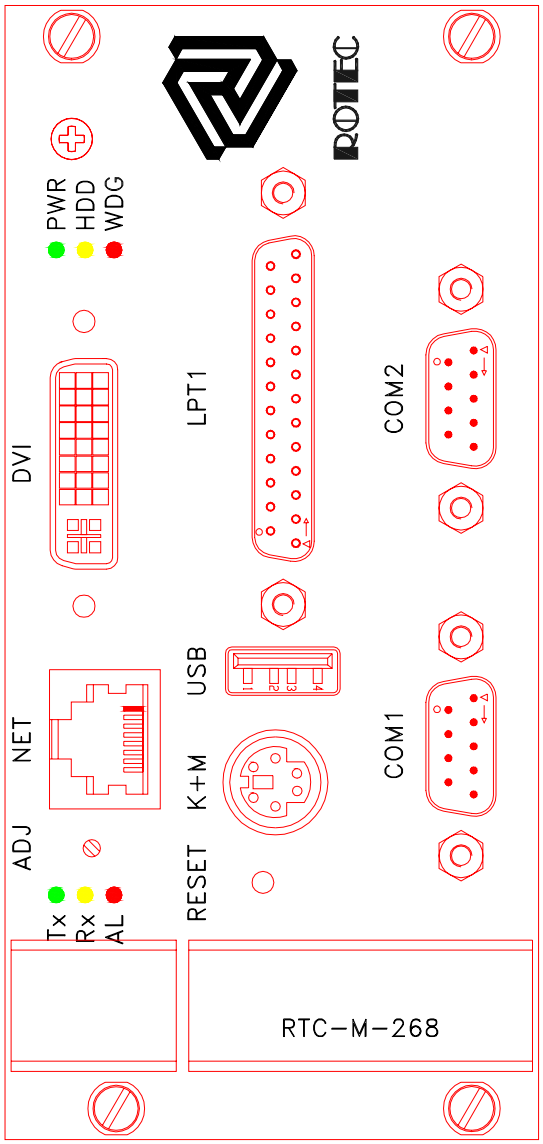


Fig. 5: Gamma7 (3 HE) - Front View

2.2. Gamma7-CPU

The Gamma7-CPU is designed as a complete PC motherboard. The Intel Pentium® III processor with 500 MHz is used and integrated on a mobile module, EMC-2 (Embedded Module Connector 2).

Two RS232 ports (COM1, COM2), one USB interface (USB) and one parallel port (LPT1) are integrated on-board as well as a connection for a PS/2 keyboard and PS/2 mouse.

Hard disks and floppy disk drives can be connected with standard connectors.

Watchdog, voltage monitoring and temperature monitoring are integrated as well as PC-standard extension capabilities. The Gamma7 functionality is extended with an ISABUS adapter for operating standard ISABUS boards (e.g., SCSI bus master). In addition, PC/104 boards can be used with another adapter. Common operation with both adapters is not possible.

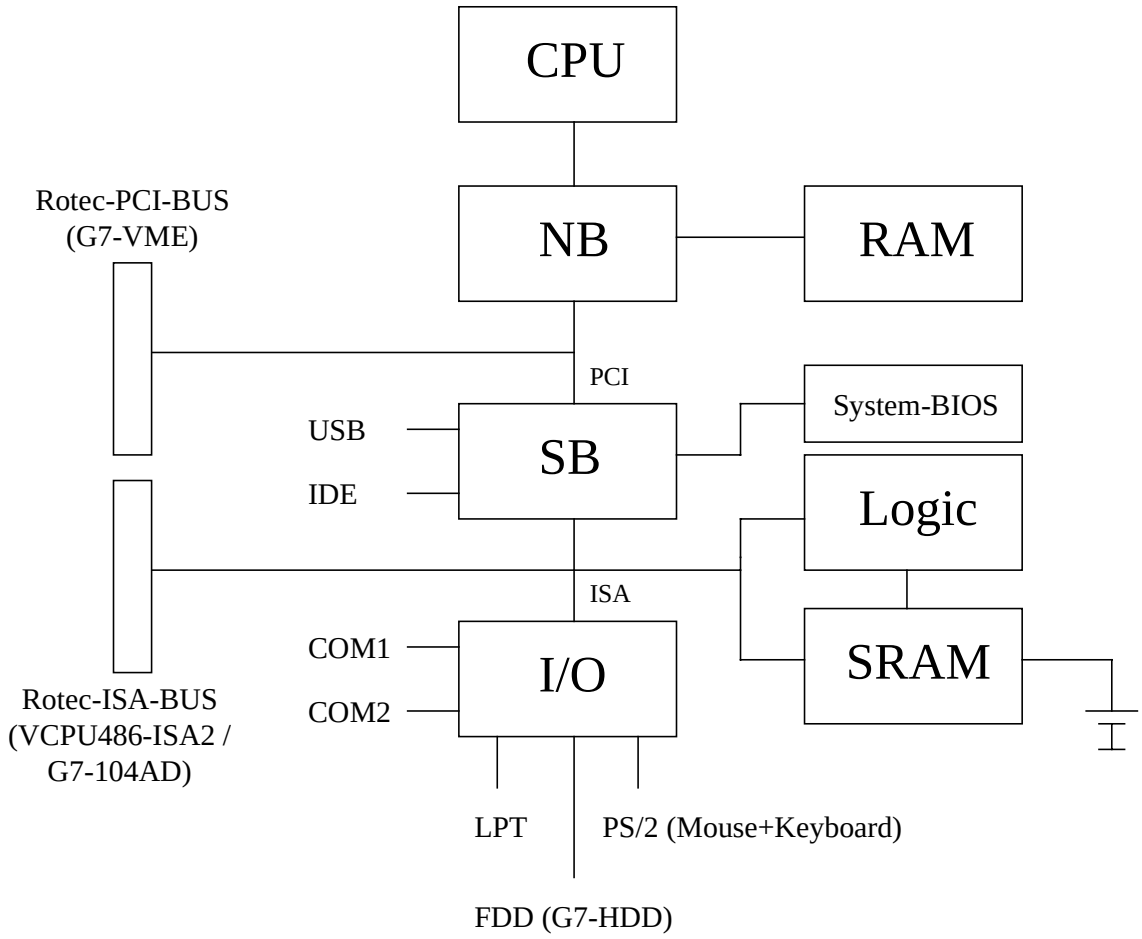


Fig. 6: G7-CPU - Functional Blocks

Functional Blocks of the Gamma7-CPU Board (Figure 6):

- CPU Pentium® III
- NB/SB Intel 440BX AGP set, consisting of:
  Host Bridge Controller 82443BX (NB - Northbridge)
  PCI ISA IDE Xcelerator 82371EB (PIIX4E, SB - Southbridge)
- I/O Super I/O Controller FDC37B78x (I/O)
- SRAM Battery-backed SRAM (max. 512 Kbyte)
- Logic Control of SRAM, NMI, etc.
- RAM 1 DIMM module, with up to 256 Mbyte PC100 SDRAM
- System BIOS FLASH component, BIOS UPDATES possible at any time
- Kontron Solutions-ISA-BUS ISA bus extension to VCPU486-ISA2 or G7-104AD
- Kontron Solutions-PCI-BUS PCI bus extension to Gamma7-VME board

2.2.1. Fast Access Memory

Gamma7 is equipped with fast access data memory (SRAM) and permits real-time storage of data being scanned at high speed. The 256 KB SRAM memory is battery-backed to prevent a loss of stored machine parameters after a power outage.

The fast access data memory can be accessed in two ways:

- **I/O Access**

  Access is handled via special IN/OUT CPU instructions. The PC address space is limited to 64 KB I/O ports, and only 16 address lines are activated.

  Since the SRAM covers a larger area (256 KB) and requires more than 16 address lines, an expansion of missing addresses is necessary. Four address lines (SAQ17..SAQ14) were expanded for the Gamma7. These can be used to select 2^4 = 16 windows. For each window, an I/O area of 16 KB can be addressed (C000h...FFFFh).

  (For details, see the description of the ADR register in Chapter 5, “Programmer’s Reference”.)

- **MEM Access**

  In PC architecture, general memory cycles (MEM access) must be differentiated with respect to REAL and PROTECTED mode addressing.

  REAL Mode:

  In REAL mode, an address space of only 1 MB can be addressed, and only 20 address lines are activated. The space reserved for expansions in the 1 MB address space is limited.

  Similar to I/O mode, addressing is also accomplished through 16 windows of 16 KB each. (The windows are addressed through the ADR register as well.) In REAL mode, the address space for mapping the window could be D0000h-D3FFFh.

  PROTECTED Mode:

  Theoretically, PROTECTED mode addressing provides all 32 bits. However, since the ISA bus contains only 24 address bits, the 16 MB of the ISA bus address space is mirrored 256 times (up to 256 MB of the low memory area is allocated to the memory and, hence, is not available for the ISA bus). The addresses are mapped 1:1, i.e., the SRAM is addressed directly by ISA bus addresses without using an intermediate address register.

2.2.2. Real Time Tick, NMI

The industrial PC includes an NMI timer for cyclical and deterministic hardware interrupts of the operating system. Time slices from 0.1 ms to 100 ms can be programmed.

In addition, the following events can be redirected to the NMI (non-maskable interrupt):

- Any ISA interrupt
- Real time tick (see above)

2.2.3. Watchdog

The watchdog increases system security by monitoring programs and detecting software errors, e.g. endless loops, that jeopardize the system's real-time capability. If the watchdog does not trigger within the hardware-configured time-out period, the watchdog "attacks" and triggers a reset.

Watchdog trigger time:

- Normal operation: t = 400 ms
- Immediately after reset: t = 1.6 s

The MAX691 watchdog ensures reliable processor operation, due to the integrated voltage-monitor function and dead man's circuit (watchdog). The red WDOG LED indicates whether the watchdog function is enabled. The watchdog is software-enabled (see "Programmer's Reference").

If the internal power supply drops below 4.65 Volt, the voltage monitor triggers a PC reset.

Recommended literature:
PC hardware basics [5], PC system programming [15], ISABUS in general [1] [2] [3], PC/104 [4], VMEbus in general [19] [20] [21], UniverseII VMEbus interface [22]

2.3. Gamma7-VME

Gamma7-VME is a complete technical redesign of the VMEbus interface for Gamma4 with graphics adapter. In addition to the VMEbus and graphics interface, the Gamma7-VME includes a 100 Mbit Ethernet interface. VMEbus, graphics and network are connected to the PCI bus, enabling fast data transfer.

The Gamma7-VME module includes the functional groups VGA graphics with CRT and LCD connection, network with RJ45 connection as well as the VMEbus interface.

The graphics and network components are active as soon as operating voltage is applied. The VMEbus component must be activated with a software protocol. The voltage is supplied through the male VG96 connector from the VMEbus, or for stand-alone operation without VMEbus, through a connector to the power supply.

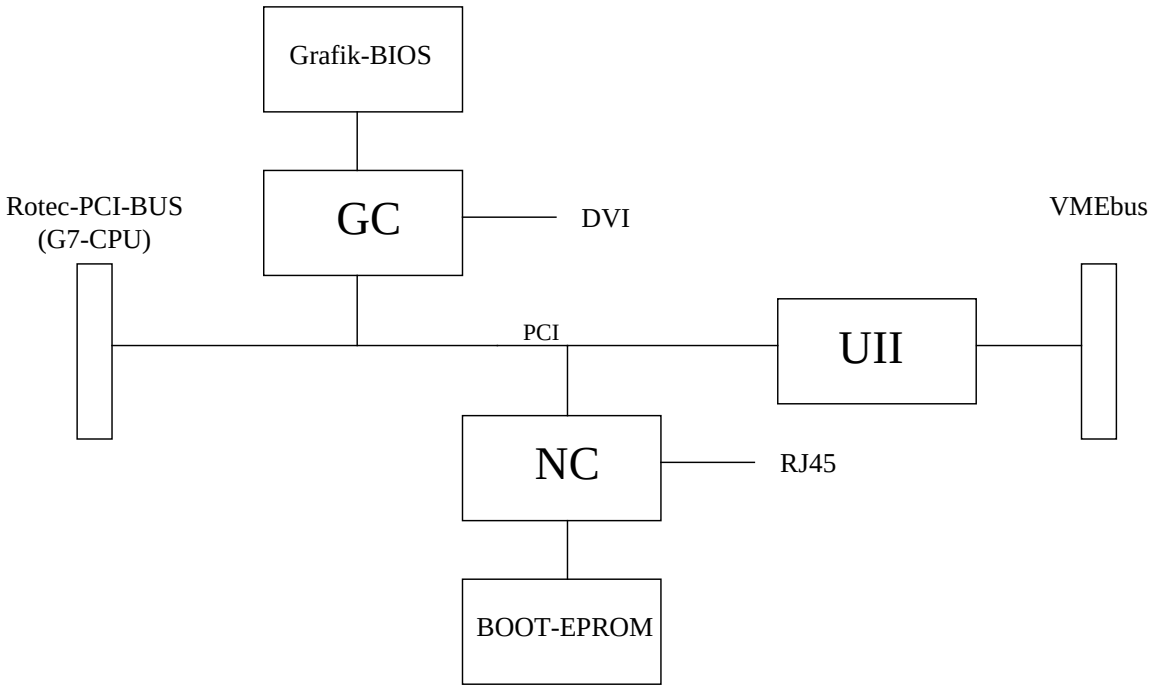


Fig. 7: G7-VME - Functional Blocks

Functional Blocks of the Gamma7-VME Board:

- GC — Lynx3DM graphics controller with up to 8 MB graphics memory
  DVI interface (VGA and PanelLink)
- Graphics BIOS — EEPROM, routines for graphics controller initialization
- NC — Am79C975 10/100 Mbit network controller by AMD
  Twisted Pair interface with RJ45 modular jacks
- BOOT EPROM — Gamma7 booting via the network
- UII — UniverseII by Tundra Semiconductor Corporation,
  VMEbus interface, PCI-to-VMEbus bridge

2.3.1. VGA Graphics Adapter

The ***graphics adapter*** with a 32-bit PCIBUS interface consists of the Lynx3DM graphics controller with an integrated DA converter for connecting a VGA monitor (200 MHz 24 bit RAMDAC) and a programmable color look-up table (CLUT) for display color space adjustment. In addition to the analog CRT interface, the graphics controller includes an LCD interface that is software/hardware-configurable and supports virtually all major LCD data formats for color models up to 24 bits. To ensure the reliable transmission of these digital signals over longer distances, a PanelLink® interface transmits LCD signals. The digital parallel signals are converted into differential serial signals. The PanelLink® interface can handle distances up to 10 m between display and computer. An additional advantage of PanelLink® is less wiring. PanelLink sends all control and data signals via three pairs of lines from the computer to the LCD. A fourth pair provides the required pixel clock for the LCD display. The analog (VGA) and digital (PanelLink®) signals are connected to the DVI (Digital Visual Interface) connector at the front. The Lynx3DM is 100% IBM VGA-compatible. It supports popular SVGA modes, such as 800 x 600, 1024 x 768 and 1280 x 1024 pixels, with ergonomic refresh rates of up to 85 Hz. The built-in hardware accelerator enables particularly fast frame rates in Windows applications. A hardware cursor further simplifies image management. In addition, the graphics controller is compatible with the 3D interfaces Direct3D and OpenGL.



The refresh rate is restricted to 60 Hz if an LCD is connected.

The graphics adapter supports power management for the CRT connection according to the VESA-DPMS standard.

2.3.2. VMEbus Adapter

The VMEbus adapter has a 32-bit PCI 2.1 compliant interface that is controlled by an ASIC. The ASIC includes the registers for VME-PCI bridge enabling and configuration. These registers are mapped in the PCIBUS I/O area. The link for buffered data transfer between PCI bus and VMEbus is a 256 KB SRAM bank with access from the PCI bus and VMEbus (shared SRAM).

A battery prevents data loss after a power outage.

The VME interface is controlled by the UniverseII component to implement in conformance with standards functions that are required according to VME specification for operation as system controller, VMEbus master, and VMEbus slave. These functions include arbiter, bus requester, bus timer, interrupter, interrupt handler, etc. Furthermore, the component provides advanced functions like VME mailbox and local interrupt controller. The component offers many registers for configuring the VMEbus interface, status information, and communication, including registers for triggering interrupts or resets on the VMEbus. These registers are mapped in the PCIBUS I/O area.

2.3.3. Network Adapter

The Am79C975 component by AMD is used as the Ethernet controller. It can be accessed in I/O mode or in memory mode. The initialization data are stored in a serial EEPROM, making switches and jumpers superfluous.

Factory-set default:

ISA interrupt IRQ10

I/O address 300h

2.4. Gamma7-HDD

The following mass storage can be connected to the VMEbus PC Gamma7 using the module HDD:

- up to 2 floppy disk drives 3.5" (using standard connector)
- up to 2 hard disk drives (using standard connector); in case of 2 drives, note master-slave jumpering of the HDDs.
  (alternately, one silicon disk and one additional hard disk drive)

The HDD add-in board can accommodate one of the following mass storage:

- 2.5" - HDD drive or alternative
- 2.5" - silicon disk

2.5. Gamma7-104AD

The 104AD is an adapter board providing a PC/104 interface acc. to IEEE-P996.1 for the Gamma7. This is an ISABUS extension with reduced form factor (9.1 x 9.6 cm). PC/104 cards are available with quite different functions (serial and parallel ports, ISDN, PC card, etc.).

8 TE (depth modules) additionally are required for PC/104 adapter installation in conjunction with a PC/104 card. Each additional PC/104 card requires only 4 TE. PC/104 interface extensions are limited by the PC architecture (IRQ, I/O ports) as well as the mechanical dimensions of the VMEbus rack.

Recommended literature:

VMEbus Interface Components Manual [x], Lynx3DM Databook [x], Am79C973/Am79C975 Databook [x], ISABUS in general [1] [2] [3], PC/104 [4], VMEbus in general [19] [20] [21]

3. Safety Guidelines

3.1. Handling

This module contains mechanically and electrically sensitive, high-quality electronics and should be carefully unpacked.

Thoroughly inspect the module for damage that might have occurred during shipment. In case of transport damage, do not install the module or apply power. Contact our technical support.

Electrostatic discharge can destroy components.

Avoid direct contact with integrated components and unprotected contacts. To avoid damages, the installation should only be made by trained personnel at a designated, static-free workplace.

Prior to installation, verify and correct, if necessary, the settings of jumpers and solder bridges.

Prior to installation in a rack or disassembly, disconnect all power to the rack and any connected components. Components must also be de-energized before connecting them to built-in interfaces.



Failure to comply with these safety precautions can destroy the module!

3.2. Circuitry

The Gamma7 is equipped with several independent safety features:

- **Voltage Monitoring**

  The PWR LED goes out when the external power supply drops below 4.85 V.

- **Program Run Time Monitoring**

  A watchdog timer monitors the CPU program run time. The watchdog must be software-enabled after booting.

  The WDG LED lights up, if the watchdog has been software-enabled.

- **Temperature Monitoring**

  A temperature sensor that is addressed by the SM bus is used for monitoring the CPU temperature. The temperature sensor monitors the CPU core temperature and activates its control output (software-enabled), if the temperature exceeds the permissible maximum value. The permissible maximum value is stored in a sensor register.

Safety advantages for you:

- **Potentially weak points of the system (e.g., overloaded or incorrect power supply) are recognized immediately through visual inspection.**

- **The watchdog trigger circuit stops (dangerous) processes triggered by software errors.**

- **An unintentionally disabled watchdog is detected through visual inspection.**

- **Destruction of modules due to excessive generation of heat is prevented.**

4. Installation

4.1. Important Installation Notes

It is essential that the following is adhered to during Gamma7 installation and operation:



Prior to connecting the Gamma7 PC to the VMEbus system, power to the entire system must be disconnected!



The Gamma7 must be sufficiently cooled for safe operation, which requires fans in the bottom of the VMEbus system. The Gamma7 must be cooled from below with an airflow rate of at least 170 m^3/h.

4.2. Quick Installation

The Gamma7 can be used directly as system controller in VMEbus slot 1 with the default setting.

The built-in hard disk is registered in the BIOS SETUP; however, an operating system is typically not pre-installed.

Connect a VGA monitor with the Gamma7 VGA output, and plug a keyboard into KEYBOARD.

Connect the floppy disk drive with the adapter board G7-HDD. The adapter board is the right board when looking directly at the front plate.

After applying power, the following message is displayed on the monitor:

1. Silicon Motion SM720 VGA BIOS Version x.xx.xx
   Copyright 2000, Silicon Motion Inc. – All Rights Reserved
   (VGA BIOS message)

2. General Software Pentium III Embedded BIOS ™ Version 4.3
   Copyright © 2000 General Software, Inc.
   Kontron Solutions GmbH
   BIOS – Version: G7_xx
   (SYSTEM BIOS message)

Pressing the key **<Delete>** calls SYSTEM BIOS SETUP.

4.3. Gamma7-CPU

4.3.1. Connection

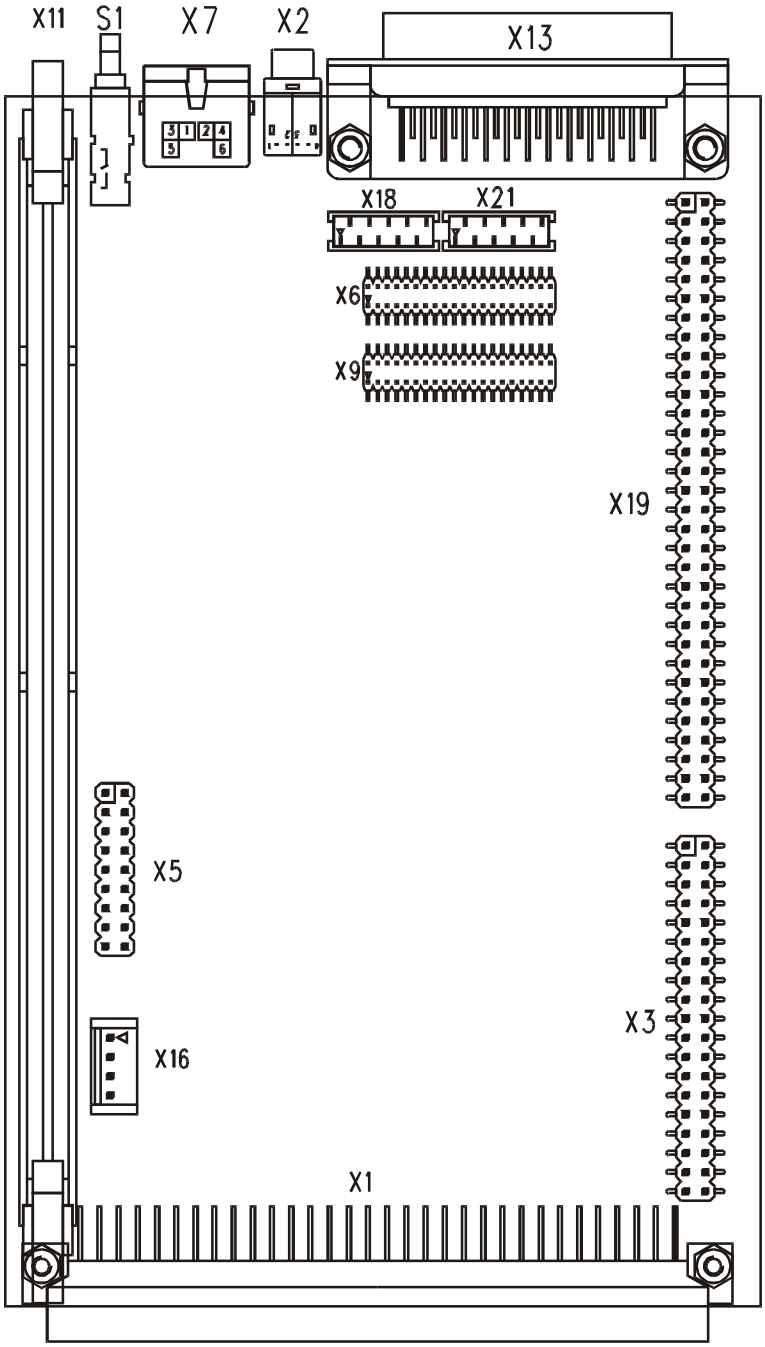


Fig. 8: Gamma7-CPU BS - Connections

X18	Serial port ("COM1" on the front plate)
X21	Serial port ("COM2" on the front plate)
X13	Parallel port
X9	HDD connection
X3, X19	Kontron SolutionsISA1Bus terminal strips, internal ISABUS modules
X6	FDD connection
X1	VMEbus VG connector for voltage supply
X11	Socket for SDRAM module
X7	PS/2 keyboard/mouse connection
X2	4.3.1.3.1. USB connection
X16	Voltage supply fan

Tab. 1: G7-CPU - Connections

4.3.2. Interfaces

4.3.2.4. Serial Ports

The Gamma7 includes two asynchronous serial ports with the following features:

- complete MS-DOS compatibility
- software-compatibility to 8250 and 16550 UARTs.

Standard address assignment:

- I/O 2F8h - 2FFh
- I/O 3F8h - 3FFh

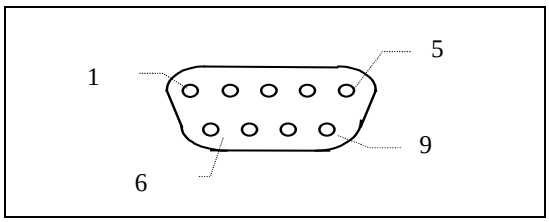


Fig. 9: DSUB COM1 and COM2 Connectors, Top View Front Plate

A ribbon cable connects the 10-pin socket connectors X18, X21 on the main board with the 9-pin DSUB connectors (COM1 and COM2) on the front plate. The pin assignment corresponds to the standard signal assignment for PCs.

COM1 / COM2		
Pin	Mnemonic	Signal Description
1	DCD	Data Carrier Detect
2	RxD	Receive Data
3	TxD	Transmit Data
4	DTR	Data Terminal Ready
5	GND	Ground
6	DSR	Data Set Ready
7	RTS	Ready To Send
8	CTS	Clear To Send
9	RI	Ring Indicator

Tab. 2: Pin Assignments for Serial Ports

4.3.2.5. Parallel Port

The Gamma7-CPU includes a complete MS-DOS-compatible parallel printer port.

Address assignment:

- I/O 278h - 27Fh or
- I/O 378h - 37Fh or
- I/O 3BCh - 3BEh

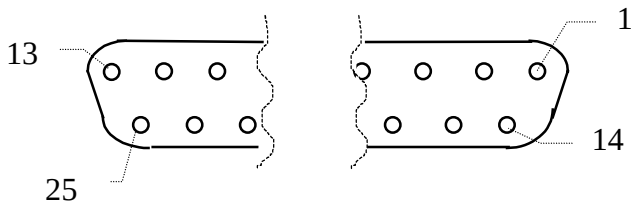


Fig. 10: DSUB LPT1 Connector, Top View Front Plate

The “LPT” DSUB connector assignment is listed in the following table:

LPT		
Pin	Mnemonic	Signal Description
1	/STB	Strobe
2	D0	Data Bit 0
3	D1	Data Bit 1
4	D2	Data Bit 2
5	D3	Data Bit 3
6	D4	Data Bit 4
7	D5	Data Bit 5
8	D6	Data Bit 6
9	D7	Data Bit 7
10	/ACK	Acknowledge
11	BUSY	Busy
12	PE	Paper End
13	SLCT	Select
14	/ALFD	Auto Feed
15	/ERROR	Error / Fault
16	/INIT	Printer Init
17	/SLCT IN	
18-25	GND	Ground

Tab. 3: Pin Assignments for Parallel LPT Port

4.3.2.6. Universal Serial Bus

Name : USB

Location : Front panel

Physical implementation : 4-pin contact strip

Universal Serial Bus		
Pin	Mnemonic	Signal Description
1	Vbus	+ 5 V Cable Power
2	D -	Data -
3	D +	Data +
4	GND	Cable Ground

Tab. 4: Pin Assignments for Universal Serial Bus

4.3.2.7. PS/2 Keyboard and Mouse Connection

Name : K+M

Location : Front panel

Physical implementation : 6-pin mini DIN connector (female)

Keyboard & Mouse		
Pin	Mnemonic	Signal Description
1	KBData	Keyboard Data
2	MData	Mouse Data
3	GND	Ground
4	VCC	+5 Volt
5	KBClk	Keyboard Clock
6	MClk	Mouse Clock

Tab. 5: Signal Assignments for 'K+M' Keyboard & Mouse Interface

Connecting

- a PS/2 mouse
- or a PS/2 keyboard and a PS/2 mouse (parallel operation)

requires a Y adapter (Part No. RTC-K-092).

A PS/2 keyboard can be connected directly.
An AT keyboard requires an off-the-shelf PS/2 adapter.

4.3.2.8. Power Supply

The VMEbus provides power to the Gamma7. +5 VDC are required (VMEbus). The Gamma7 is inserted in the 96-pin VG connector X1 on the VMEbus. The X1 VG connector assignment is listed in the following table:

Pin	Row A	Row B	Row C
9	GND		GND
11	GND		
15	GND		
17	GND		
19	GND		
20		GND	
23		GND	
31	-12V		+12V
32	+5V	+5V	+5V

Tab. 6: Pin Assignment for X1 Power Supply

4.3.3. Installation of the Internal ISABUS Modules

Two contact strips (X19, X3) with the complete ISABUS assignment are located at the upper edge of the board. This bus (Kontron SolutionsISA1Bus) connects the Gamma7-CPU and VCPU486-ISA2.

Up to 2 external 16-bit (slot bus) ISA cards can be connected using the ISABUS adapter VCPU486-ISA2.

However, this is only possible for the 6 HE version (order with VCPU486-ISA2). Therefore, only the signal assignment of the corresponding contact strips will be discussed.

The Gamma4-ISA2 bus adapter is exclusively factory-installed.
The contact strips X19/X3 are the signal interface to the ISABUS adapter VCPU486-ISA2.

These strips are assigned as follows:

Signal Name	Pin			Pin	Signal Name
	2	•	•	1	
LA23	4	•	•	3	/SBHE
LA21	6	•	•	5	LA22
LA19	8	•	•	7	LA20
LA17	10	•	•	9	LA18
/MEMW	12	•	•	11	/MEMR
SD09	14	•	•	13	SD08
SD11	16	•	•	15	SD10
SD13	18	•	•	17	SD12
SD15	20	•	•	19	SD14
/IOCS16	22	•	•	21	/MEMCS16
IRQ11	24	•	•	23	IRQ10
IRQ15	26	•	•	25	IRQ12
/DACK0	28	•	•	27	IRQ14.
/DACK5	30	•	•	29	DRQ0.
/DACK6	32	•	•	31	DRQ5
/DACK7	34	•	•	33	DRQ6
VCC	36	•	•	35	DRQ7
GND	38	•	•	37	/MASTER.

Tab. 7: X3 Connection Kontron SolutionsISA1Bus

Signal Name	Pin			Pin	Signal Name
VBAT-5V	2	•	•	1	
SD7	4	•	•	3	/IOCHCHK
SD5	6	•	•	5	SD6
SD3	8	•	•	7	SD4
SD1	10	•	•	9	SD2
IOCHRDY	12	•	•	11	SD0
SA19	14	•	•	13	AEN
SA17	16	•	•	15	SA18
SA15	18	•	•	17	SA16
SA13	20	•	•	19	SA14
SA11	22	•	•	21	SA12
SA9	24	•	•	23	SA10
SA7	26	•	•	25	SA8
SA5	28	•	•	27	SA6
SA3	30	•	•	29	SA4
SA1	32	•	•	31	SA2
GND	34	•	•	33	SA0
VCC	36	•	•	35	RESETDRV
N.C.	38	•	•	37	IRQ9
-12V	40	•	•	39	DRQ2
+12V	42	•	•	41	/ENDFXR
/SMEMW	44	•	•	43	GND
/IOW	46	•	•	45	/SMEMR
/DACK3	48	•	•	47	/IOR
/DACK1	50	•	•	49	DRQ3
/REFRESH	52	•	•	51	DRQ1
IRQ7	54	•	•	53	SYSCLK
IRQ5	56	•	•	55	IRQ6
IRQ3	58	•	•	57	IRQ4
TC	60	•	•	59	/DACK2
VCC	62	•	•	61	BALE
GND	64	•	•	63	OSC

Tab. 8: X19 - Kontron SolutionsISA1Bus

4.3.4. Installation of the Internal PCIBUS Modules

A female connector (X17) with almost complete PCIBUS assignment is located at the upper edge of the board on its solder side. This bus (Kontron SolutionsPCIBus) connects the Gamma7-CPU and Gamma7-VME. Graphics, network and VMEbus controller are connected to this PCIBus. The table below lists the Kontron SolutionsPCIBus signal assignments.

Signal Name	Pin			Pin	Signal Name
/P_GNT1	A1	•	•	B1	P_AD04
P_AD05	A2	•	•	B2	/P_REQ1
GND	A3	•	•	B3	GND
IDSEL VME	A4	•	•	B4	IDSEL NET
	A5	•	•	B5	/LRST
/P_INTA	A6	•	•	B6	P_AD06
/P_INTC	A7	•	•	B7	/P_INTB
	A8	•	•	B8	/P_INTD
ACTIVE_WDOG	A9	•	•	B9	ACTIV_HDD
	A10	•	•	B10	ACTIVE_POWER
/P_GNT2	A11	•	•	B11	GND
/P_REQ2	A12	•	•	B12	PCLK_VME
/P_RST	A13	•	•	B13	GND
	A14	•	•	B14	PCLK_NW
/P_GNT0	A15	•	•	B15	GND
GND	A16	•	•	B16	/P_REQ0
	A17	•	•	B17	
P_AD30	A18	•	•	B18	P_AD31
	A19	•	•	B19	P_AD29
P_AD28	A20	•	•	B20	GND
P_AD26	A21	•	•	B21	P_AD27
GND	A22	•	•	B22	P_AD25
P_AD24	A23	•	•	B23	
IDSEL VGA	A24	•	•	B24	/P_CBE03
	A25	•	•	B25	P_AD23
P_AD22	A26	•	•	B26	GND
P_AD20	A27	•	•	B27	P_AD21
GND	A28	•	•	B28	P_AD19

P_AD18	A29	•	•	B29	
P_AD16	A30	•	•	B30	P_AD17
	A31	•	•	B31	/P_CBE02
/P_FRAME	A32	•	•	B32	GND
GND	A33	•	•	B33	/P_IRDY
/P_TRDY	A34	•	•	B34	P_AD07
GND	A35	•	•	B35	/P_DEVSEL
/P_STOP	A36	•	•	B36	GND
P_AD02	A37	•	•	B37	/P_LOCK
P_SDONE	A38	•	•	B38	/P_PERR
/P_SBO	A39	•	•	B39	P_AD03
GND	A40	•	•	B40	/P_SERR
P_PAR	A41	•	•	B41	P_AD01
P_AD15	A42	•	•	B42	/P_CBE01
P_AD00	A43	•	•	B43	P_AD14
P_AD13	A44	•	•	B44	GND
P_AD11	A45	•	•	B45	P_AD12
GND	A46	•	•	B46	P_AD10
P_AD09	A47	•	•	B47	GND
GND	A48	•	•	B48	PCLK_VGA
GND	A49	•	•	B49	GND
/P_CBE00	A50	•	•	B50	P_AD08

Tab. 9: Kontron SolutionsPCIBus

4.3.5. Mass Storage Connection

The Gamma7-CPU includes the following mass storage interfaces via the HDD board:

- Fast IDE bus-compatible hard disk interface for up to 2 drives.

- MS-DOS-compatible floppy interface for up to 2 drives (3.5" and/or 5.25"). All major formats up to 4 MB are supported.

Basically two types are distinguished during installation:

- on-board mass storage system on HDD (2.5“ only)
- off-board mass storage system

For an off-board hard disk upgrade, master-slave jumpering is required (ask Kontron Solutions about the configured board on the HDD using the serial number of the Gamma7 VMEbus controller).

For a mass storage system, the add-in module HDD is installed. The required signals are sent to the HDD add-in board via two contact strip fields on the main board Gamma7-CPU (X6, X9).

4.3.5.9. Hard Disk Drives

Several mass storage types are supported for an on-board system. The hard disk used is dependent on market conditions.

Address assignment for the controller registers:

- I/O 1F0h - 1F7h
- I/O 3F6h - 3F7h

Connection details are listed in the HDD subchapter of this chapter.

4.3.5.10. Floppy Disk Drives

Up to two floppy disk drives can be connected when using the HDD add-in board.

For 3.5" drives, the format (normal or high density) is always detected through a mark on the floppy.

Address assignment:

- I/O 3F0h - 3F7h

4.4. Gamma7-VME

4.4.1. Connection

Figure 11 shows the plug-in connections of the Gamma7-VME module; not affected components are omitted for clarity. Table 10 explains the abbreviations.

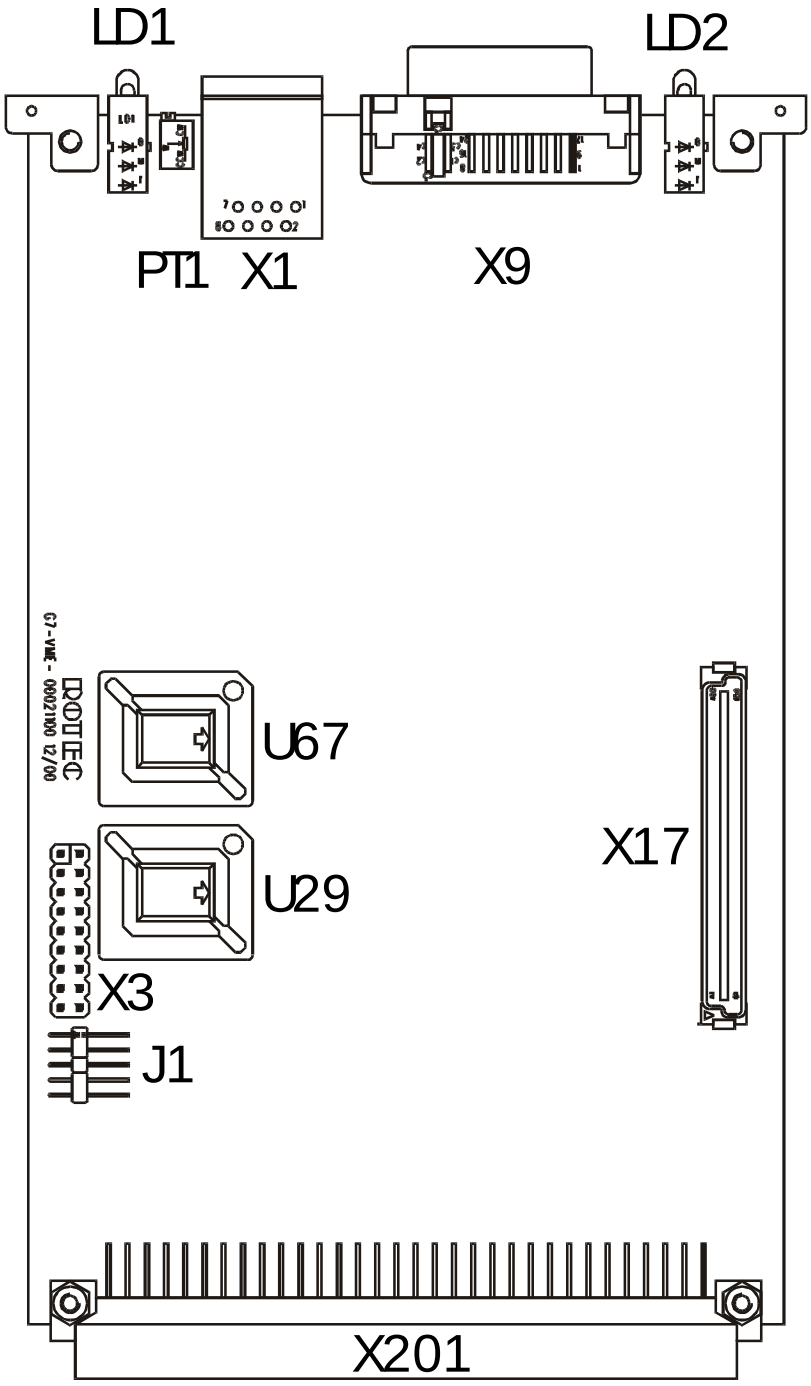


Fig. 11: G7-VME – Connections

X201	VMEbus VG connector
X17	PCI connector
J1	Jumper for configuration
X3	JTAG or boundary scan
U29	EPROM network
U67	EPROM graphics
LD1	Network controller LEDs
LD2	Hard disk, watchdog and power LEDs
X9	DVI connector
X1	4.4.1.10.1. 100Base-Tx connector
PT1	PanelLink trimming

Tab. 10: G7-VME - Connections

4.4.1.1. VMEbus Interface, X201

The 96-pin VG blade-connector strip X201, DIN 41612, type C, connects the Gamma7-VME with the VMEbus.

VMEbus Interface			
Pin	***Mnemonic, Row A***	***Mnemonic, Row B***	***Mnemonic, Row C***
1	D00	BBSY*	D08
2	D01	BCLR*	D09
3	D02	ACFAIL*	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	SYSCLK	BG3IN*	SYSFAIL*
11	GND	BG3OUT*	BERR*
12	DS0*	BR0*	SYSRESET*
13	DS1*	BR1*	LWORD*
14	WRITE*	BR2*	AM5
15	GND	BR3*	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*		A17
22	IACKOUT*		A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	-12V	+5V STDBY	+12V
32	+5V	+5V	+5V

Tab. 11: Pin Assignments for VMEbus Interface

Not listed pins are not connected on the board.

4.4.1.1.1. Start-Up Notes

1. For interrupt processing, check that the VMEbus IACK daisy chain exists as required (see VMEbus specification acc. to IEEE 1014-1987). The daisy chain must possibly be created using jumpers on the back of the VMEbus backplane. The same holds true for bus grant daisy chains in multiprocessor systems with several VMEbus masters.

2. Check the settings of, for example, the slave base address and system controller.



Prior to connecting the Gamma7 PC to the VMEbus system, power to the entire system must be disconnected!

4.4.1.2. Connection to Gamma7-CPU, X17

The connector X17 connects the Gamma7-VME board with the Gamma7-CPU board. Essentially, the signals correspond to the PCIBUS. In addition, several system-internal control pins are added. The connector pin assignment is described in Table 9 in Chapter 4.3.4.

4.4.1.3. Gamma7-VME Configuration through J1

The basic functions of the Gamma7-VMEbus board can be set through jumper block J1.

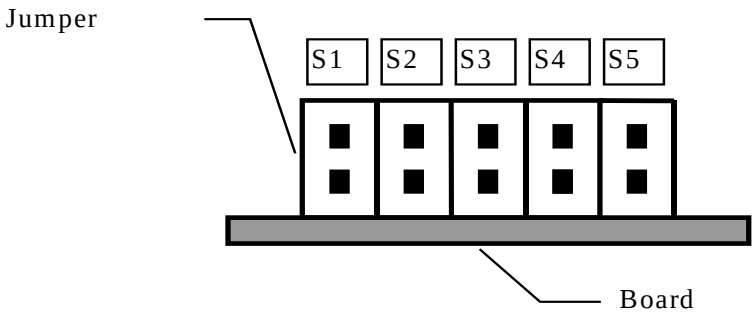


Fig. 12: Jumper Block J1

S1:

Jumper set	PCIBus address space of UII is in MEM area
Jumper not set	PCIBus address space of UII is in I/O area

S2:

Jumper set	after power-up, the VMEbus interface is in BUS-ISOLATION MODE, i.e., logically separated from the VMEbus. If the Gamma7 is started in this mode, each #SYSRESET or #RST results in a VMEbus interface switch to BI mode.
Jumper not set	BUS-ISOLATION MODE is deactivated

S3:

Jumper set	network controller is in sleep mode
Jumper not set	network controller is in normal mode

S4:

Jumper set	enable VMEbus Auto-ID acc. to UII
Jumper not set	disable VMEbus Auto-ID acc. to UII

S5:

Jumper set	enable VMEbus SYSRESET
Jumper not set	disable VMEbus SYSRESET

For a detailed description of the Universe see User's Manual.

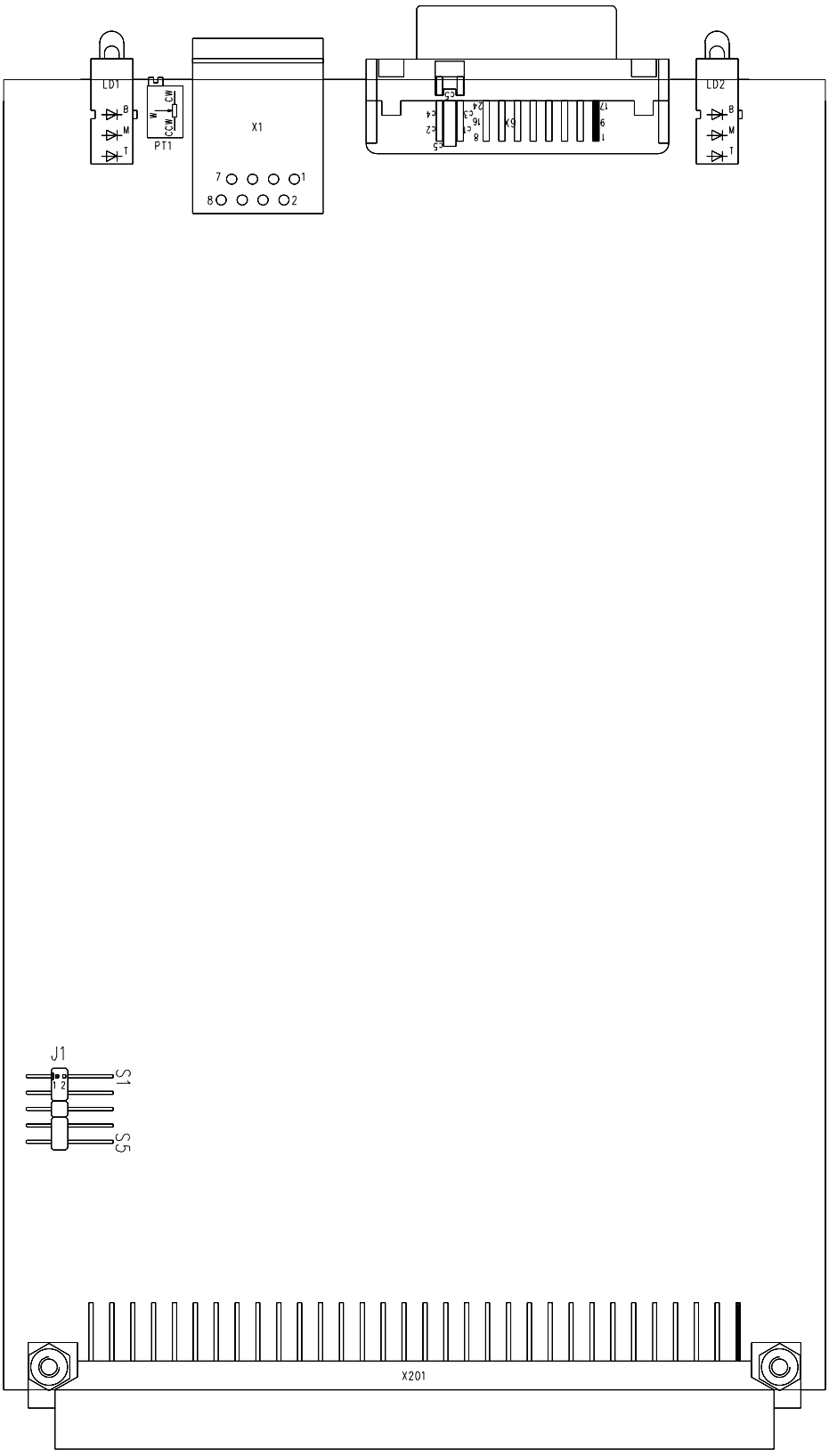


Fig. 13: Position of Jumper Block J1

4.4.1.4. Boundary Scan/JTAG Connector, X3

Test port for testing the function of the graphics or network controller and the PCI-to-VMEbus bridge. This connector is only of interest to the board manufacturer (Kontron Solutions).

4.4.1.5. Network Graphics BIOS, U 29, U67

The optional network BIOS is used as BOOT ROM. This can be used to create a “disk-less station”. Depending upon the network (e.g., TCP/IP or IPX) or function of the BOOT ROM, another ROM image is used. Several suppliers exist (see Appendix).

4.4.1.6. LEDs, LD1-LD2

See Chapter 2.1.2 for a description.

4.4.1.7. CRT/LCD Interface, X9

Name : DVI

Location : Front panel

Physical implementation :

Connector X9 is used to connect a monitor or LCD. This connector is completely compatible with the new DVI (**D**igital **V**isual **I**nterface) specification 1.0 ensuring the interface to new analog and digital display devices. For backward compatibility with older monitors/LCDs, an adapter (DVI -> 15-pin VGA, DVI -> RJ45) is available. All off-the-shelf TFT-LC-Displays with DVI interface can be connected to this connector X9.

Pin	Signal Assignment
1	TMDS DATA2-
2	TMDS DATA2+
3	TMDS DATA2/4 Shield
4	N.C.
5	N.C.
6	DDC CLOCK
7	DDC DATA
8	ANALOG VERTICAL SYNC
9	TMDS DATA1-
10	TMDS DATA1+
11	TMDS DATA1/3 Shield
12	N.C.
13	N.C.
14	VCC
15	GND
16	N.C.
17	TMDS DATA0-
18	TMDS DATA0+
19	TMDS DATA0/5 Shield
20	N.C.
21	N.C.
22	TMDS CLOCK Shield
23	TMDS CLOCK+
24	TMDS CLOCK-
C1	ANALOG RED
C2	ANALOG GREEN
C3	ANALOG BLUE
C4	ANALOG HORIZONTAL SYNC
C5	ANALOG GND

Tab. 12: DVI Pin Assignment

4.4.1.8. Network Connection (Twisted Pair), X1

Name : Net

Location : Front panel

Physical implementation : 8-pin RJ45 connector (female)

10Base-T / 100Base-TX		
Pin	Mnemonic	Signal Description
1	TD+	Transmit Data +
2	TD-	Transmit Data -
3	RD+	Receive Data +
4	n.c.	
5	n.c.	
6	RD-	Receive Data -
7	n.c.	
8	n.c.	

Tab. 13: Signal Assignment for 10Base-T / 100Base-TX

4.4.1.9. PanelLink Trimming Potentiometer, PT1

This potentiometer is used to trim the PanelLink transmission distance. Trimming is required for eliminating interferences on the LCD and can be done with a small screw driver.

4.5. Gamma7-HDD

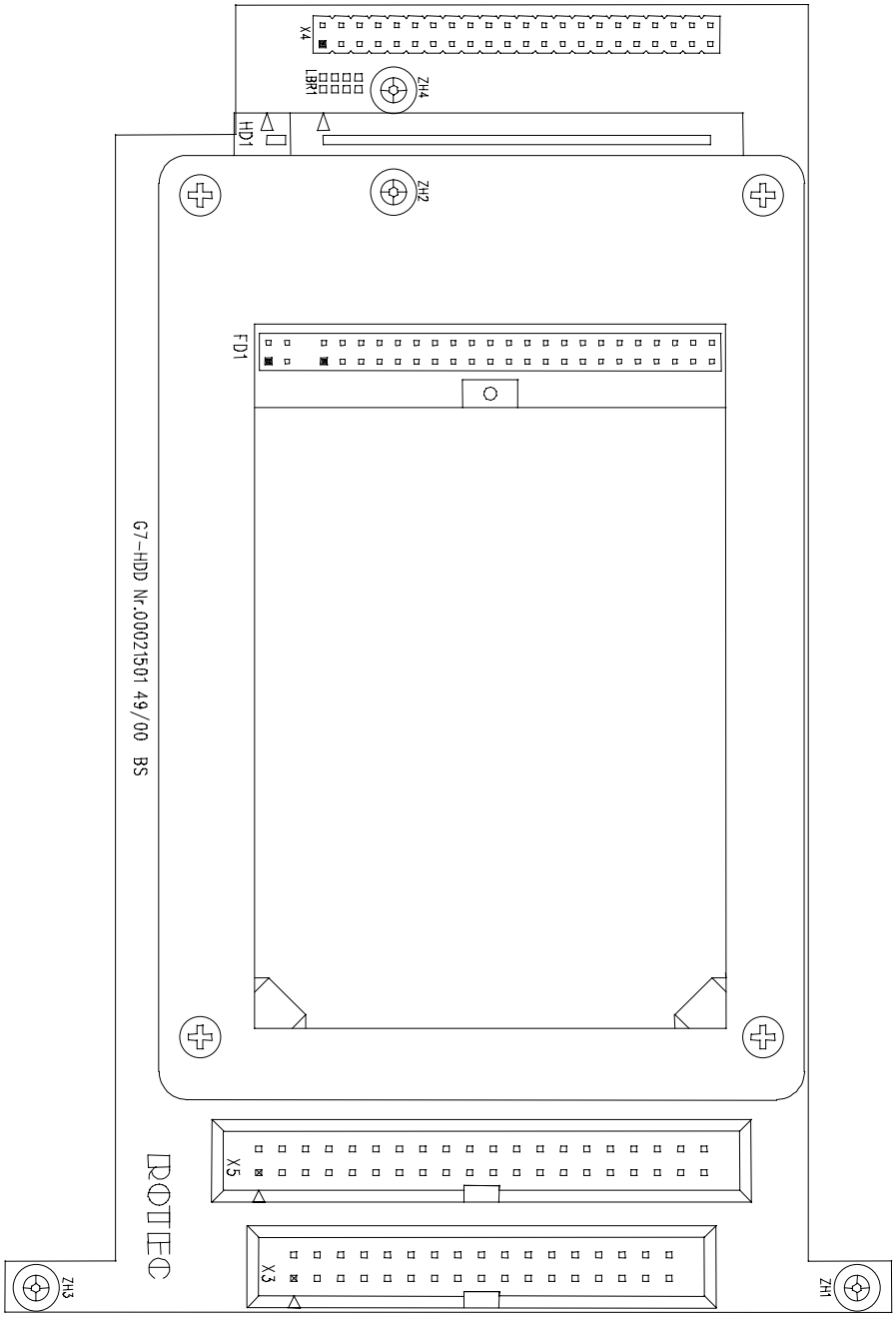


Fig. 14: Connector Assignment G7-HDD

X3	Connector 3,5“ Floppy-Disk-Dive
X4	Connector 2,5“ Hard-Disk-Drive
X5	Connector 3,5“ Hard-Disk-Drive/CDROM-Drive

Tab. 14: Connector Assignments G7-HDD

4.5.1. Floppy Disk Drive

The connector for FDD is a 34-pin 4-Wall Male Connector. The signal assignment corresponds to the following table.

X3			
Pin	Mnemonic	Signalname	I/O
2	RPM/LC	Density Select	I
6	DRATE0	Data Rate 0	O
8	#INDEX	Index	I
10	#MTR0	Motor Select 0	O
12	#DRV1	Drive Select 1	O
14	#DRV0	Drive Select 0	O
16	#MTR1	Motor Select 1	O
18	FDDIR	Direction Select	O
20	#STEP	Step	O
22	#WDATA	Write Data	O
24	#WGATE	Write Gate	O
26	#TRK0	Track 0	I
28	#WRTPRT	Write Protect	I
30	#RDATA	Read Data	I
32	HDSEL	Head Select	O
34	#DSKCHG	Disk Change	I
1, 4	NC	not connected	-
3, 5, 7...33	GND	Ground	-

Tab. 15: Signal Assignment X3

The power supply for the FDD must be separately connected (external) to the Drive!

Do not connect the FDD to the Gamma7 while the power is on. This could destroy the the device.

The following figure shows the configuration of the FDD ribbon cable.

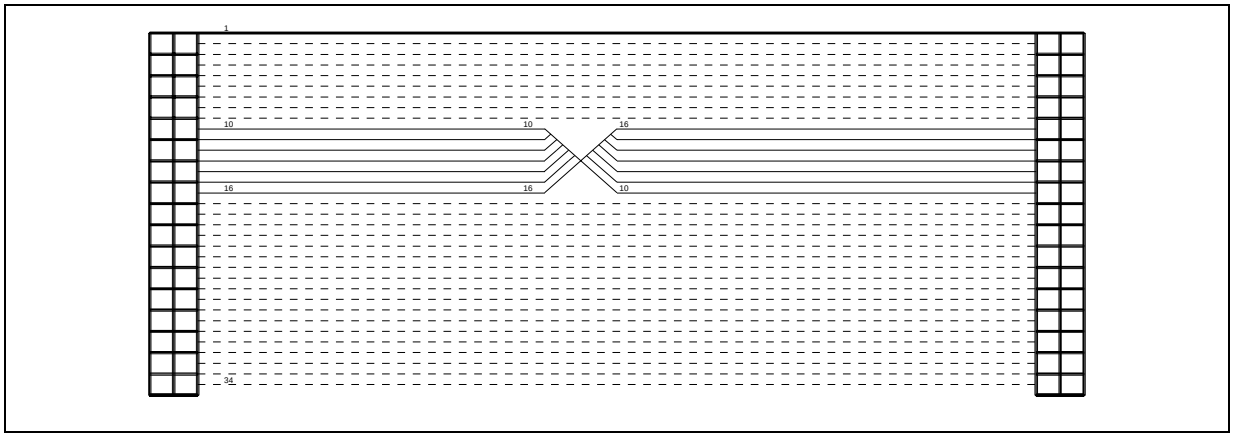


Fig. 15: Configuration of the ribbon cable for FDD

4.5.1.10. Settings

Depend on the used Floppy Disk Drive, it is necessary to configure the G7-HDD via the solder jumper LBR1.

Floppy Disk Drive	Closed connection in Solder Jumper Array LBR1
TEAC FD-05HF-030	1-2, 5-6

Fig. 16: Settings of the Solder Jumper LBR1

The settings are already configured in the factory. The user should not change these settings.

4.5.2. Hard Disk Drive X4

The connector for HDD is a 44-pin standard connector X4 (2mm Pitch). The signal assignment corresponds to the following table.

X4			
Pin	**Mnemonic**	**Signalname**	**I/O**
1	#SYSRESET	Reset DRV	O
3, 5, 7..17 4, 6, 8..18	IDE07...IDE00 IDE08...IDE15	Host Data Bus Bits 07...00 Host Data Bus Bits 08...15	I/O
23	#IDEIOW	I/O Write	O
25	#IDEIOR	I/O Read	O
27	I_IOCHRDY	I/O Channel Ready	I
28	SPSYNC	Spindel-Synchronisation	I/O
31	I_IRQ14	Interrupt Request	I
32	#I_IOCS16	I/O Chip Select 16	I
35, 33, 36	A0, A1, #I_SBHE	„Host“ Adress Bus (#I_SBHE ≅ A2)	O
34	#PDIAG	Passed Diagnostic	I/O
37	#IDECS0	HD Chip Select 0	O
38	#IDECS1	HD Chip Select 1	O
39	#IDEACT	Drive active / Slave present	I
20, 21, 29, 44	NC	not connected	-
41, 42	VCC	Power Supply	-
2, 19, 22, 24, 26, 30, 40, 43	GND	Ground	-

Fig. 17: Pin Assignment X4

Do not connect the HDD to the Gamma7 while the power is on. This could destroy the the device.

4.5.3. Hard Disk Drive X5

The connector for HDD (3,5'') is a 40-pin 4-Wall Male Connector. The signal assignment corresponds to the following table.

X5			
Pin	**Mnemonic**	**Signalname**	**I/O**
1	#SYSRESET	Reset DRV	O
3, 5, 7..17 4, 6, 8..18	IDE07...IDE00 IDE08...IDE15	Host Data Bus Bits 07...00 Host Data Bus Bits 08...15	I/O
23	#IDEIOW	I/O Write	O
25	#IDEIOR	I/O Read	O
27	I_IOCHRDY	I/O Channel Ready	I
28	SPSYNC	SPSYNC	I/O
31	I_IRQ14	Interrupt Request	I
32	#I_IOCS16	I/O Chip Select 16	I
35, 33, 36	A0, A1, #I_SBHE	„Host" Adress Bus (#I_SBHE ≅ A2)	O
34	#PDIAG	Passed Diagnostic	I/O
37	#IDECS0	HD Chip Select 0	O
38	#IDECS1	HD Chip Select 1	O
39	#IDEACT	Drive active / Slave present	I
20, 21, 29	NC	not connected	-
2, 19, 22, 24, 26, 30, 40	GND	Ground	-

Tab. 1: Pinbelegung von X5

The power supply for the HDD must be separately connected (external) to the Drive!

Do not connect the FDD to the Gamma7 while the power is on. This could destroy the the device.

4.6. Gamma7-104AD

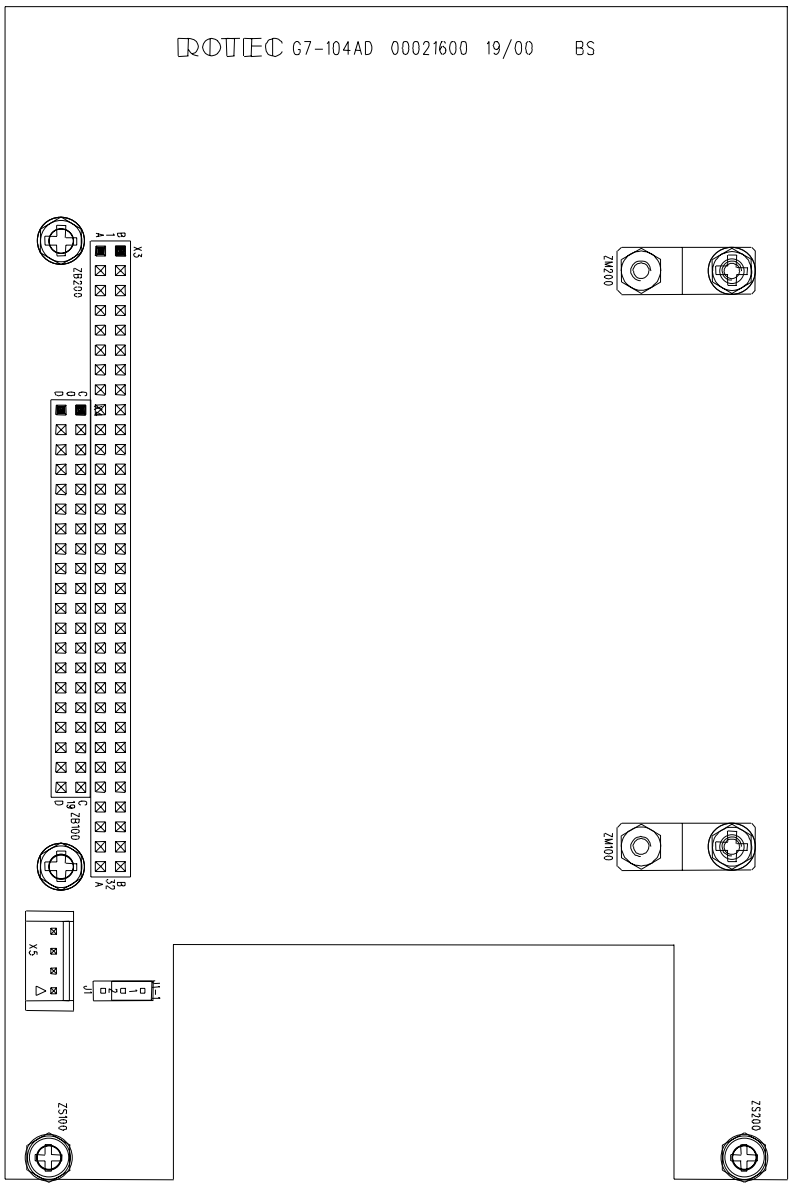


Fig. 18: Connector Assignment G7-104AD

X3	PC104-Receptable
X5	External Power Supply of the PC/104 Module
J1	Selection of the Power Supply

Tab. 16: Connector Assignment G7-104AD

4.6.1. Mounting of the G7-104AD

The modul G7-104AD is snaped on the CPU-Board of the Gamma7. The ISA-Bus signals for the PC/104-interface are available about the Kontron SolutionsISA1-Bus. The Power Supply for the PC/104-boards can provided either internal (G7-CPU) or external over X5. These selection were made with jumper J1.

4.6.2. Mounting of a PC/104 Module

PC/104 module is snaped on the G7-104AD and screwed on the other side over angle brackets. Two distance pieces were screwed on the G7-104AD to achieve the desired clearance.

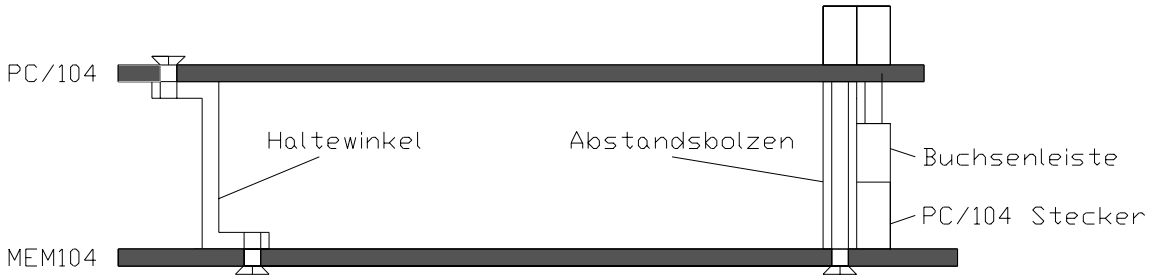


Abb. 1: Mounting of a PC/104-Module

4.6.3. Pin Assignment of X3 PC/104

The connector assignment for PC/104-modules corresponds to IEEE P996.1. PC/104-modules are plugged with the component side on top onto the G7-104AD-module. PC/104 corresponds to the connections X3.

Pin	Row C	Pin	Row D
0	GND	0	GND
1	/SBHE	1	/MEMCS16
2	LA23	2	/IOCS16
3	LA22	3	IRQ10
4	LA21	4	IRQ11
5	LA20	5	IRQ12
6	LA19	6	IRQ15
7	LA18	7	IRQ14
8	LA17	8	/DACK0
9	/MEMR	9	DRQ0
10	/MEMW	10	/DACK5
11	SD8	11	DRQ5
12	SD9	12	/DACK6
13	SD10	13	DRQ6
14	SD11	14	/DACK7
15	SD12	15	DRQ7
16	SD13	16	+5V
17	SD14	17	/MASTER
18	SD15	18	GND
19	n.c.	19	GND

Fig. 19: PC/104-Connection X3

Pin	Row A	Pin	Row B
1	/IOCHCHK	1	GND
2	SD7	2	RESETDRV
3	SD6	3	+5V
4	SD5	4	IRQ9
5	SD4	5	n.c.
6	SD3	6	DRQ2
7	SD2	7	-12V
8	SD1	8	/ENDXFR
9	SD0	9	+12V
10	IOCHRDY	10	n.c.
11	AEN	11	/SMEMW
12	SA19	12	/SMEMR
13	SA18	13	/IOW
14	SA17	14	/IOR
15	SA16	15	/DACK3
16	SA15	16	DRQ3
17	SA14	17	/DACK1
18	SA13	18	DRQ1
19	SA12	19	/REFRESH
20	SA11	20	SYSCLK
21	SA10	21	IRQ7
22	SA9	22	IRQ6
23	SA8	23	IRQ5
24	SA7	24	IRQ4
25	SA6	25	IRQ3
26	SA5	26	/DACK2
27	SA4	27	TC
28	SA3	28	BALE
29	SA2	29	+5V
30	SA1	30	OSC
31	SA0	31	GND
32	GND	32	GND

Fig. 20: PC/104-Connection X3

4.6.4. Pin Assignment X5

X5		
Pin	Mnemonic	Signal description
1,4	VCC	External Power Supply
2,3	GND	Ground

Fig. 21: Pin Assignment X5

4.6.4.11. Settings

The Power Supply for the PC/104-boards can provided either internal (G7-CPU) or external over X5. These selection were made with jumper J1.

J1	
Pin	Description
1-2	Internal Power Supply
2-3	External Power Supply

Fig. 22: Jumper J1

4.7. Settings

4.7.1. BIOS

The BIOS comprises numerous functions, including:

- Automatic detection of processor type
- Automatic detection and testing of main memory size and organization
- Automatic detection and testing of cache size and organization
- Support of non-standardized systems
- Support of several parallel and serial ports
- Password support
- Hard disk analysis
- Video and system BIOS shadowing



The BIOS Setup factory settings are correct and should normally not be modified by the customer!

The SYSTEM BIOS includes extensive SETUP capabilities.

The BIOS SETUP is accessed by pressing the **<del>** function key during boot-up. The parameter settings are self-explanatory.

It may be necessary to modify certain settings in order to configure the GAMMA7 according to customer requirements. It is necessary to take care when modifying configuration settings. Some configuration settings are factory settings and should not be modified by the customer.

4.8. Software Installation

4.8.1. Graphics Drivers

Graphics Driver Installation for Windows 9x:

The following steps are required to install the graphics drivers for Windows 95:

* In the Windows 95 „Start“ menu, select „Settings“ and then „Control Panel“.
* Select „Display“.
* In „Display“, select the submenu „Settings“ and click on the button „Change Configuration“.
* In the menu „Change Configuration“, click on „Change“ for the graphics card.
* In the window „Select Model“, click on „Have Disk“.
* Insert the diskette with the graphics drivers into the floppy disk drive. In the window „Install from disk“, click „OK“.
* In the menu „Select Model“, select the type „Silicon Motion“ and click „OK“.

The installation process is starting. The required files are copied to the hard disk.

After copying is completed, perform the following steps:

* Close the submenu „Change Configuration“.
* Close the menu „Display Properties“.

In order for the changes to take effect, reboot the computer after the installation process is completed.

For installation or reinstallation, Windows must be operated with a standard VGA driver.

The GAMMA7 graphics function works with the Windows drivers VGA 640x480x16 as well as with SVGA 800x600x16.

 For SVGA 800x600x16, the LCD panel must provide the required resolution for simultaneous or LCD stand-alone operation. However, this resolution is generally suited only for sole operation with a CRT monitor, since these panels are still rare.
The popular LCD panels with 640 x 480 may only be used with the VGA driver.

Higher resolutions require the SiliconMotion® driver that have been supplied. If the screen resolution is higher than can be displayed on the LCD panel, the highest displayable physical resolution is used. Invisible areas of the screen can be reached through panning. Panning is initiated by moving the mouse to the edge of the screen.

4.8.2. Ethernet Drivers

Ethernet Driver Installation for Windows 95:

The following steps are required to install the Ethernet drivers for Windows 95:

* In the Windows 95 „Start“ menu, select „Settings“ and then „Control Panel“.
* Select „Network“.
* In „Network“, select the submenu „Configuration“ and click on the button „Add“.
* In „Select Network Component“, select the setting „Network Card“ and the click on „Add“.
* Click on „Have Disk“.
* Insert the disk with the Ethernet drivers into the floppy disk drive and click „OK“(or specify the corresponding path).
* „Select Network Card“ is displayed. Select „AMD“ (manufacturer) and then „AMD PCNET Family Ethernet Adaptor PCI“ (network card). Click on „OK“.
* Close „Network“ by clicking „OK“.
* The corresponding files are copied to the hard disk (the corresponding source directories may have to set). During this installation, several Windows 95 installation files are required.
* In order for the changes to take effect, reboot the computer after successful installation.

5. Programmer's Reference

5.1. I/O Address Space

The CPU I/O address space is functionally divided into three areas:

- Standard PC I/O ports
- Special chipset registers
- Special I/O registers
- VMEbus register (Universe II)

Address	Mapping	Mnemonic
0000h – 000Fh	1st DMA controller	
0010h – 001Fh	Motherboard resources	
0020h – 0021h	1st Interrupt controller	
0022h – 003Fh	Motherboard resources	
0040h – 0043h	System timer	
0044h – 005Fh	Motherboard resources	
0060h	Keyboard controller	
0061h	NMI status and control	
0060h	Keyboard controller	
0062h – 0063h	Motherboard resources	
0064h	Keyboard controller	
0065h – 006Fh	Motherboard resources	
0070h – 0071h	RTC, NMI mask	
0072h – 0080h	Motherboard resources	
0081h – 0083h	DMA controller	
0084h – 0086h	Motherboard resources	
0087h	DMA controller	
0088h	Motherboard resources	
0089h – 008Bh	DMA controller	
008Ch – 008Eh	Motherboard resources	
008Fh	DMA controller	

0090h – 009Fh	Motherboard resources
00A0h – 00A1h	2nd Interrupt controller
00A2h – 00BFh	Motherboard resources
00C0h – 00DFh	2nd DMA controller
00E0h – 00EFh	Motherboard resources
00F0h – 00FFh	Coprocessor
0170h – 0177h	2nd IDE controller
01F0h – 01F7h	1st IDE controller
02F8h – 02FFh	COM2
0300h – 031Fh	Network controller
0376h	2nd IDE controller
0378h – 037Ah	LPT1
03B0h – 03BB	Graphics controller
03C0h – 03DF	Graphics controller
03F2h – 03F5h	Floppy
03F6h	1st IDE controller
03F8h – 03FFh	COM1
2000h – 2007h	1st IDE controller
2008h – 200Fh	2nd IDE controller
3900h – 391Fh	USB host controller
8000h – 8FFFh	UniverseII

Tab. 17: Gamma7 I/O Ports

The next table lists the chipset registers required for addressing the system management bus. (Refer also to the “82371AB PCI-TO-ISA/IDE Xcelerator” data sheet.)

Address	Mapping	Mnemonic
Base[1)] + (00h)	SMB Host Status Register	SMBHSTSTS
Base + (01h)	SMB Slave Status Register	SMBSLVSTS
Base + (02h)	SMB Host Control Register	SMBHSTCNT
Base + (03h)	SMB Host Command Register	SMBHSTCMD
Base + (04h)	SMB Host Address Register	SMBHSTADD
Base + (05h)	SMB Host Data 0 Register	SMBHSTDAT0
Base + (06h)	SMB Host Data 1 Register	SMBHSTDAT1
Base + (07h)	SMB Block Data Register	SMBBLKDAT
Base + (08h)	SMB Slave Control Register	SMBSLVCNT
Base + (09h)	SMB Shadow Command Reg.	SMBSHDWCMD
Base + (0Ah)	SMB Slave Event Register	SMBSLVEVT
Base + (0Ch)	SMB Slave Data Register	SMBSLVDAT

Tab. 18: Special Chipset Registers (SMBus I/O Registers)

[1)] For GAMMA7, the SMB base address was assigned to base = 10A0h (assignment through system BIOS)

Address	Mapping	Mnemonic
0300h – 031Fh	Ethernet	
03B0h – 03DFh	Graphics Controller	
4000h – 40FFh	Card/IOCHCK Enable	ENABLE
7000h – 70FFh	Address Register	ADR
7500h – 75FFh	Watchdog Trigger	WDOG
7600h – 76FFh	Configuration Port	KONFIG
7700h / 7701h	Reserved	
7900h – 79FFh	IRQx to NMI	IRQ_NMI
7B00h – 7BFFh	NMI Reason	NMI_RS
7D00h – 7DFFh	Real Time Tick	RTT
8000h – 8FFFh	PCI VMEbus Bridge	
C000h – FFFFh	SRAM	

Tab. 19: Special Gamma7 I/O Registers

The VMEbus functional group uses 4 KB PC I/O address space (8000h-8FFFh) which is subdivided as follows:

1. PCI configuration and status registers
2. UniverseII-specific registers
3. VMEbus configuration and status registers

Address	***Mapping***	***Mnemonic***
8000h – 830Ch	PCI configuration and status registers	
8310h – 8EFC	UniverseII-specific registers	
8F00h – 8FFC	VMEbus configuration and status registers	

Tab. 20: VME Functional Group I/O Areas

For a detailed PCI-to-VMEbus bridge register description refer to "Universe II™ User Manual", Appendix A, Registers. The manual can be downloaded from the Tundra Semiconductor Corporation Homepage (http://www.tundra.com).

5.2. Memory Address Space

The 4 GB CPU address space is structured as follows:

Address	Mapping	
0000.0000h – 0009.FFFFh	PC RAM	0K...640K
000A.0000h – 000F.FFFFh	ISA bus; shadow RAM; SRAM; video RAM; Ethernet	640K...1M
0010.0000h – 0FFF.FFFFh		1M...256M
00F0.0000h – 00FF.FFFFh	Optional MEMHOLE	15M...16M
1000.0000h – FEFF.FFFFh	No access allowed	
FF00.0000h – FFEF.FFFFh	Reserved	Top (16-1)M
FFF0.0000h – FFFF.FFFFh	System BIOS	Top 1M

Tab. 21: Gamma7 Address Space

5.3. Register Model

5.3.1. ADR

Address: 7000h-70FFh

The address register enables I/O (C000h-FFFFh) or MEM access to the SRAM (256 K sizes) in real mode (default: D0000h- D3FFFh). The address register sets 16 pages with 16 K each.

Read/write access:

X	X	X	X	X	X	A17	A16	A15	A14	X	X	X	X	X	X
D15							D08	D07							D00

Default state after system reset:

0000h

The SRAM memory map is listed in the following table:

Protected Mode	Initialization of Reg. ADR	I/O Access	Segm. Access
FBFFFFh FBC000h...	Page 15 : Value 03C0h	FFFFh C000h...	D3FFFh D0000h...
FBBFFFh FB8000h...	Page 14 : Value 0380h	FFFFh C000h...	D3FFFh D0000h...
FB7FFFh FB4000h...	Page 13 : Value 0340h	FFFFh C000h...	D3FFFh D0000h...
FB3FFFh FB0000h...	Page 12 : Value 0300h	FFFFh C000h...	D3FFFh D0000h...
FAFFFFh FAC000h...	Page 11 : Value 02C0h	FFFFh C000h...	D3FFFh D0000h...
FABFFFh FA8000h...	Page 10 : Value 0280h	FFFFh C000h...	D3FFFh D0000h...
FA7FFFh FA4000h...	Page 9 : Value 0240h	FFFFh C000h...	D3FFFh D0000h...
FA3FFFh FA0000h...	Page 8 : Value 0200h	FFFFh C000h...	D3FFFh D0000h...
F9FFFFh F9C000h...	Page 7 : Value 01C0h	FFFFh C000h...	D3FFFh D0000h...
F9BFFFh F98000h...	Page 6 : Value 0180h	FFFFh C000h...	D3FFFh D0000h...
F97FFFh F94000h...	Page 5 : Value 0140h	FFFFh C000h...	D3FFFh D0000h...
F93FFFh F90000h...	Page 4 : Value 0100h	FFFFh C000h...	D3FFFh D0000h...
F8FFFFh F8C000h...	Page 3 : Value 00C0h	FFFFh C000h...	D3FFFh D0000h...
F8BFFFh F88000h...	Page 2 : Value 0080h	FFFFh C000h...	D3FFFh D0000h...
F87FFFh F84000h...	Page 1 : Value 0040h	FFFFh C000h...	D3FFFh D0000h...
F83FFFh F80000h...	Page 0 : Value 0000h	FFFFh C000h...	D3FFFh D0000h...

Tab. 22: SRAM Memory Map

5.3.2. WDOG

Address: 7500h-75FFh

Read access:

Reading the WDOG register I/O activates the watchdog and sets the WD bit in the DIAG register.

When this condition is satisfied, the LED in the front panel lights for visual control.

Write access:

Writing to the WDOG register I/O deactivates the watchdog and clears the WD bit in the DIAG register.

For Gamma7, the watchdog must be constantly re-triggered within a 400 ms interval through read-access to the WDOG I/O address. If this trigger interval is exceeded, a system RESET is automatically triggered. The customer can set the watchdog trigger time.

5.3.3. KONFIG

Address: 7600h-76FFh

Register and SRAM access is enabled or disabled via the interface configuration register. KONFIG register access is possible prior to read access to 40xxh that is required for I/O register enabling.

Read access:

CRD	x	CS3	CS2	CS1	I/O	SEG	PRO	CRD	X	x	NMI EN	x	I/O	SEG	PRO
D15							D08	D07							D00

Write access:

X	x	CS3	CS2	CS1	x	x	x	CRD	X	x	NMI EN	x	I/O	SEG	PRO
D15							D08	D07							D00

CRD: Card Enable

CRD = 0: Register access (to special I/O registers) disabled

CRD = 1: Register access to special I/O registers enabled

CSx: Segment select bits 3..1 (segmented SRAM addressing)

CS3	CS2	CS1	Segment	
0	0	1	C8	
0	1	0	D0	Default
0	1	1	D8	
1	0	0	E0	
1	0	1	E8	

I/O: SRAM I/O access enable

I/O = 0: I/O access (to SRAM) disabled

I/O = 1: I/O access (to SRAM) enabled

SEG:SRAM segment access enable

SEG = 0: Segment access (to SRAM) disabled

SEG = 1: Segment access (to SRAM) enabled

PRO: SRAM access enable in protected mode

PRO = 0: SRAM access in protected mode disabled

PRO = 1: SRAM access in protected mode enabled

NMI EN: #IOCHCK enable

NMI EN = 0: NMI triggering globally disabled

NMI EN = 1: NMI triggering enabled

Default state after system reset:

1202h

5.3.4. IRQ_NMI

Address: 7900h-79FFh

The events triggering an NMI can be selected in register IRQ_NMI.

The following events can result in an NMI:

- ISA bus interrupt (“n out of m” selection)
- Drop in power (power failure)

Read access:

x	x	PFO	x	x	I15	I14	I12	I11	I10	I09	I07	I06	I05	I04	I03
D15							D08	D07							D00

Write access:

0	0	PFO	0	0	I15	I14	I12	I11	I10	I09	I07	I06	I05	I04	I03
D15							D08	D07							D00

PFO: Power failure

PFO = 0: Power failure has no effect on NMI

PFO = 1: Power failure results in NMI

Ix: ISA bus interrupt

Ix = 0: ISA bus interrupt Ix has no effect on NMI

Ix = 1: ISA bus interrupt Ix results in NMI

Default state after system reset:

0000h

5.3.5. NMI_RS

Address: 7B00h-7BFFh

The cause of the NMI can be determined by reading register NMI_RS (NMI reason). If the NMI was triggered by the timer or an ISA bus interrupt, the NMI is not disabled until after reading the NMI_RS register.

Read access:

x	x	PFO	x	RTT	I15	I14	I12	I11	I10	I09	I07	I06	I05	I04	I03
D15							D08	D07							D00

PFO: NMI triggered by power failure

PFO = 0: Power OK

PFO = 1: Power failure

RTT: NMI triggered by timer

RTT = 0: NMI not triggered by timer

RTT = 1: NMI triggered by timer

Ix: ISA bus interrupt

Ix = 0: NMI not triggered by ISA bus interrupt Ix

Ix = 1: NMI triggered by ISA bus interrupt Ix

Write access:

N/A

Default state after system reset:

0000h

5.3.6. RTT

Address: 7D00h-7DFFh

The time base for the tick is set to 0.1 ms via the RTT (real time tick) register. The tick set in RTT triggers an NMI only when bit 4 is set in register KONFIG (global NMI enabling). A tick that occurs during a disabled NMI is stored and triggers an NMI immediately after re-enabling.

Read access:

0	0	0	0	0	0	RT9	RT8	RT7	RT6	RT5	RT4	RT3	RT2	RT1	RT0
D15							D08	D07							D00

Write access:

x	x	x	x	x	x	RT9	RT8	RT7	RT6	RT5	RT4	RT3	RT2	RT1	RT0
D15							D08	D07							D00

RT9..0: Time base selection for tick

The tick is calculated as follows:

TICK = RT9..0 * 0.1 ms

Default state after system reset:

0000h

6. Applications

6.1. Enabling/Disabling the Watchdog

The code listed below contains extracts from a program for:

- Enabling and triggering the watchdog
- Disabling the watchdog

```
/*    Definition of constants                                    */
      #define ENABLE 0x4000
      #define WDOG 0x7500

/*    Enabling register access to special I/O registers*/
      inport (ENABLE);

/*    Enabling and triggering the watchdog                       */
      do
            {
            inport (WDOG);
            }
      while (?);              /* Triggering until event ? occurs      */

/*    Disabling the watchdog                                     */
      outport (WDOG, 0x0000);
```

6.2. SRAM Access through I/O Cycle

The following lists an example for a SRAM access through I/O cycle.

```
/*    Definition of constants                                          */
        #define ENABLE 0x4000
        #define ADR 0x7000
        #define KONFIG 0x7600

/*    Enabling register access to special I/O registers*/
      inport (ENABLE);

/*    Enabling SRAM access through I/O cycle                           */
      outportb (KONFIG, 0x87);

/*    Selection of page 1                                              */
/*    i.e., I/O address C000h corresponds to physical address F84000h  */
      outport (ADR, 0x0040)

/*    Reading a word from SRAM, ISA address F84002h                    */
          inport (0xC002)

/*    Selection of page 5                                              */
/*    i.e., I/O address C000h corresponds to physical address F94000h  */
      outport (ADR, 0x0140)

/*    Reading a word from SRAM, ISA address F94002h                    */
      inport (0xC002)
```

6.3. Initialization of the PCI-VMEbus-Bridge

The following code initialize the UniverseII of the PC-side (PCI-Bus). IO-Address of the bridge is 0x8000h.

```
/*************************************************************************
*      Header-File for UniverseII                                       *
*                                                                       *
*      A. Huber    24/06/2000      Address definition                   *
*                                                                       *
*************************************************************************/

/* IOBaseAddress Kontron Solutions 0x8000h */
#define UIIBAdr          0x8000          // Kontron Solutions specific IO-Base Address

#define PCI_ID       0x0000          // Device ID, Word Vendor ID
#define PCI_CSR      0x0004          // PCI Configuration Space Control and Status Register
#define PCI_CLASS 0x0008          // PCI Configuration Class Register
#define PCI_MISC0        0x000C          // PCI Configuration Miscellaneous 0 Register
#define PCI_BS0      0x0010          // PCI Configuration Base Address 0 Register
#define PCI_BS1      0x0014          // PCI Configuration Base Address 1 Register
#define PCI_MISC1  0x003C          // PCI Configuration Miscellaneous 1 Register
#define LSI0_CTL     0x0100          // PCI Target Image 0 Control
#define LSI0_BS      0x0104          // PCI Target Image 0 Base Address Register
#define LSI0_BD      0x0108          // PCI Target Image 0 Bound Address Register
#define LSI0_TO      0x010C          // PCI Target Image 0 Transl. Offset Register
#define LMISC        0x0184          // PCI Miscellaneous Register
#define U2SPEC       0x04FC          // UII and UIIB Specific Register
etc.
```

```
vmeinit()
{
        Value = IORead32 (UIIBAdr + PCI_ID);     // Read Device ID and Vendor ID
        if ( Value == 0x000010E3 )
                {
                printf("UniverseII is on the PCI-Bus\n");
                }

        /* global initialization */
        IOWrite32 (UIIBAdr + PCI_CSR, 0x00000007 );
                // Busmaster enable, Target Memory enable, 0 Target IO enable

        IOWrite32 (UIIBAdr + LMISC, 0x01000000 );
                // coupled window timer -> 16 PCI Clocks

        /* PCI Target Image 0 initialization */
        IOWrite32 (UIIBAdr + LSI0_BS, 0x80000000 );
                // Target Image Base Address, 2GB

        IOWrite32 (UIIBAdr + LSI0_BD,  0x80FFFFFF );
                // Target Image Bound Address, 2GB + 16MB

        IOWrite32 (UIIBAdr + LSI0_TO,  0x80800000 );
                // Target Image Translation Offset, VMEbus Address 0x800000

        IOWrite32 (UIIBAdr + LSI0_CTL, 0xC0411000 );
                // Image enable, Posted Write enable, 16 Bit VME data width
                // VME Address Space A24 enable, Supervisor enable

        /* UniverseII and UniverseIIB Specific initialization */
        IOWrite32 (UIIBAdr + U2SPEC, 0x00000200 );
                // READt27, VME Master Parameter t27 Control (Delay of DS* negation
                // after read), Bit9/8, 0/1 = Faster, 0/0 = Default, 1/0 = No Delay
}
```

7. Error Corrections / Troubleshooting

7.1. POST Codes

POST Code (hexadecimal)	Description
02	Verify Real Mode
04	Get CPU type
06	Initialize system hardware
08	Initialize chipset registers with initial POST values
09	Set in POST flag
0A	Initialize CPU registers
0B	Enable CPU cache
0C	Initialize caches to initial POST values
0E	Initialize I/O
0F	Initialize the local bus DIE
10	Initialize Power Management
11	Load alternate registers with initial POST values
12	Restore CPU control word during warm boot
14	Initialize keyboard controller
16	BIOS ROM checksum
18	8254 timer initialization
1A	8237 DMA controller initialization
1C	Reset Programmable Interrupt Controller
20	Test DRAM Refresh
22	Test 8742 Keyboard Controller
24	Set ES segment register to 4 GB
28	Autosize DRAM
2A	Clear 512K bawse RAM
2C	RAM failure on address line xxxx *
2E	RAM failure on data bits xxxx * of low byte of memory bus
30	RAM failure on data bits xxxx * of high byte of memory bus
32	Test CPU bus-clock frequency
34	Test CMOS RAM
35	Initialize alternate chipset register
36	Warm start shut down
37	Reinitialize the chipset /MB only‘)
38	Shadow system BIOS ROM
39	Reinitialize the cache (MB only)
3A	Autosize cache
3C	Configure advanced chipset registers
3D	Load alternate registers with CMOS values
40	Set Initial CPU speed
42	Initialize interrupt vectors
44	Initialize BIOS interrupts
46	Check ROM copyright notice
47	Initialize manager for PCI Option ROMs

48	Check video configuration against CMOS
49	Initialize PCI bus and devices
4A	Initialize all video adapters in system
4B	Display QuietBoot screen
4C	Shadow video BIOS ROM
4E	Display copyright notice
50	Display CPU type and speed
51	Initialize EISA board
52	Test keyboard
54	Set key click if enabled
56	Enable keyboard
58	Test for unexpected interrupts
5A	Display prompt “Press F2 to enter SETUP“
5C	Test RAM between 512 and 640K
60	Test extended memory
62	Test extended memory address lines
64	Jump to UserPatch1
66	Configure advanced cache register
68	Enable external and CPU caches
6A	Display external cache size
6C	Display shadow message
6E	Display non-disposable segments
70	Display error messages
72	Check for configuration errors
74	Test real-time clock
76	Check for keyboard errors
7A	Test for key lock on
7C	Set up hardware interrupt vectors
7E	Test coprocessor if present
80	Disable on-board I/O ports
82	Detect and install external RS232 ports
84	Detect and install external parallel ports
85	Initialize PC-compatible PnP ISA devices
86	Re-initialize onboard I/O ports
88	Initialize BIOS Data Area
8A	Initialize Extended BIOS Data Area
8C	Initialize floppy controller
90	Initialize hard disk controller
91	Initialize local-bus hard disk controller
92	Jump to UserPatch2
93	Build MPTABLE for multi-processor boards
94	Disable A20 address line
95	Install CD ROM for boot
96	Clear huge ES segment register
98	Search for option ROMs. One long, two short beeps on checksum failure
9A	Shadow option ROMs
9C	Set up Power Management
9E	Enable hardware interrupts
A0	Set time of day

A2	Check key lock
A4	Initialize typematic rate
A8	Erase F2 prompt
AA	Scan for F2 key stroke
AC	Enter SETUP
AE	Clear in-POST flag
B0	Check for errors
B2	POST done – prepare to boot operating system
B4	One short beep before boot
B5	-
B6	Check password (optional)
B8	Clear global descriptor table
BC	Clear parity checkers
BE	Clear screen (optional)
BF	Check virus and backup reminders
C0	Try to boot with INT 19
D0	Interrupt handler error
D2	Unknown interrupt error
D4	Pending interrupt error
D6	Initialize option ROM error
D8	Shutdown error
DA	Extended Block Move
DC	Shutdown error
The following are for boot block in Flash ROM	
E2	Initialize the chipset
E3	Initialize refresh counter
E4	Check for Forced Flash
E5	Check HW stats of ROM
E6	BIOS ROM is OK
E7 **Entry:**	Do a complete RAM test
E8	Do OEM initialization
E9	Initialize interrupt controller
EA	Read in the bootstrap code
EB	Initialize all vectors
EC	Boot the Flash program
ED	Initialize the boot device
EE	Boot code was read OK

- If the BIOS detects error 2C, 2E, or 30 (base 512K RAM error), it displays an additional word-bitmap (xxxx) indicating the address line or bits that failed. For example, “2C 0002“ means address line 1 (bit one set) has failed. “2E 1020“ means data bits 12 and 5 (bits 12 and 5 set) have failed in the lower 16 bits. Note that error 30 cannot occur on 386SX systems because they have a 16 rather than 32-bit bus. The BIOS also sends the bitmap to the port-80 LED display. It first displays the check point code, followed by a delay, the high order byte, another delay, and then the low order byte of the error. It repeats this sequence continuously.

8. Appendix

8.1. Literature

ISA-BUS

[1] A. Stiller — c't 11/1991, S.336ff "AT-Bus"
1991, Heise-Verlag

[2] A. Stiller — c't 12/1991, S.313ff "AT-Bus-Timing"
1991, Heise-Verlag

[3] E. Solari — AT BUS Design IEEE P996 Compatible
Anabooks San Diego

[4] — IEEE P996.1 Version 2.3
Juni 1996

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[5] E. Solari — PCI Hardware and Software, Architecture & Design
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[6] Tundra — VMEbus Interface Components Manual, Universe II™
Document: 9000000.MD304.01

[7] VITA — The VMEbus Specification Manual
1987

[8] Wade D. Peterson — The VMEbus Handbook, Second Edition
November 1990

[9] Wade D. Peterson — The VMEbus Handbook, Third Edition
September 1992

PC-Hardware

[10] H.-P. Messmer — PC-Hardwarebuch, Addison-Wesley

8.2. Component Mounting Diagrams

8.2.1. Gamma7-CPU

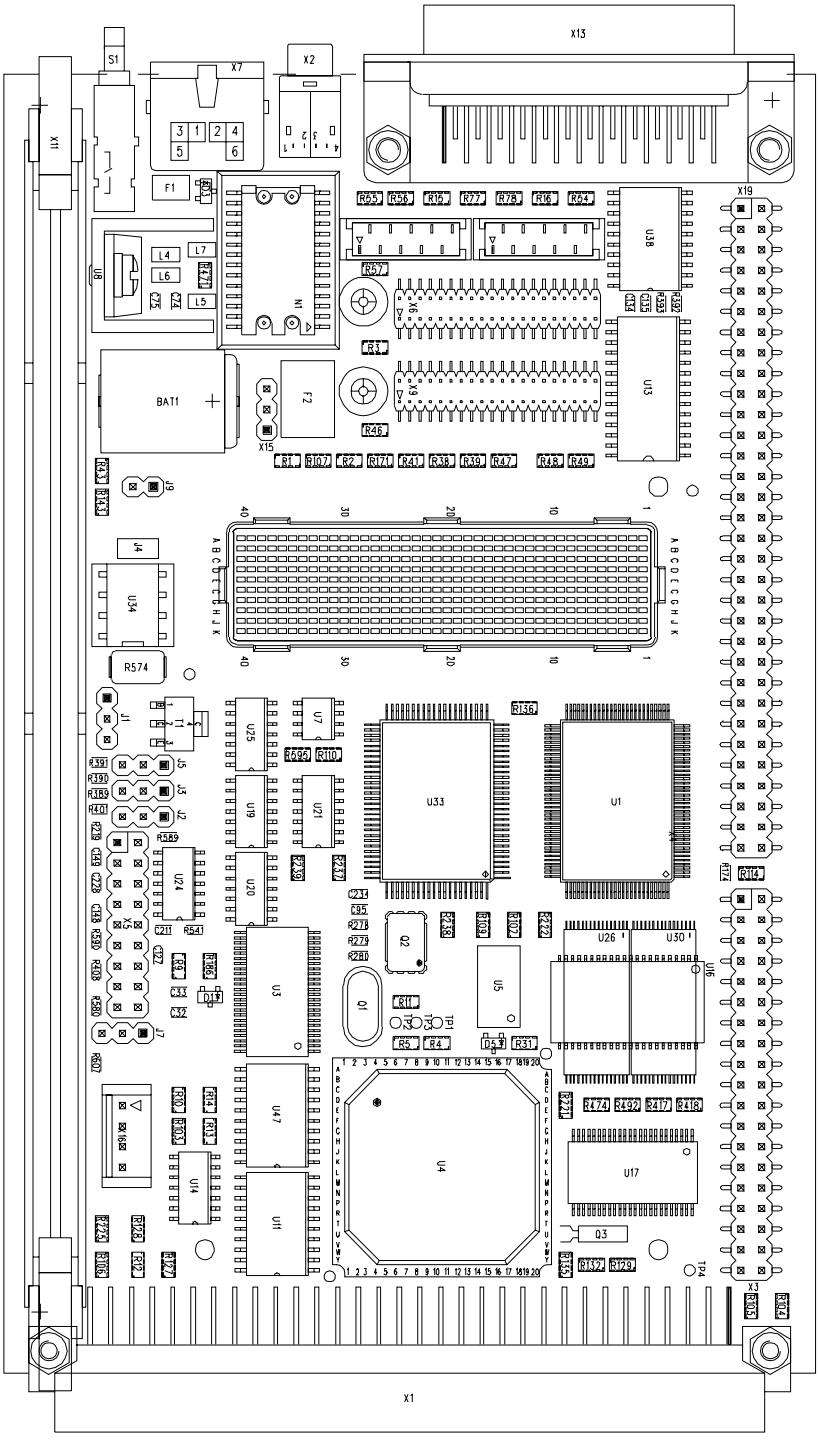


Fig. 23: Gamma7-CPU Component Side

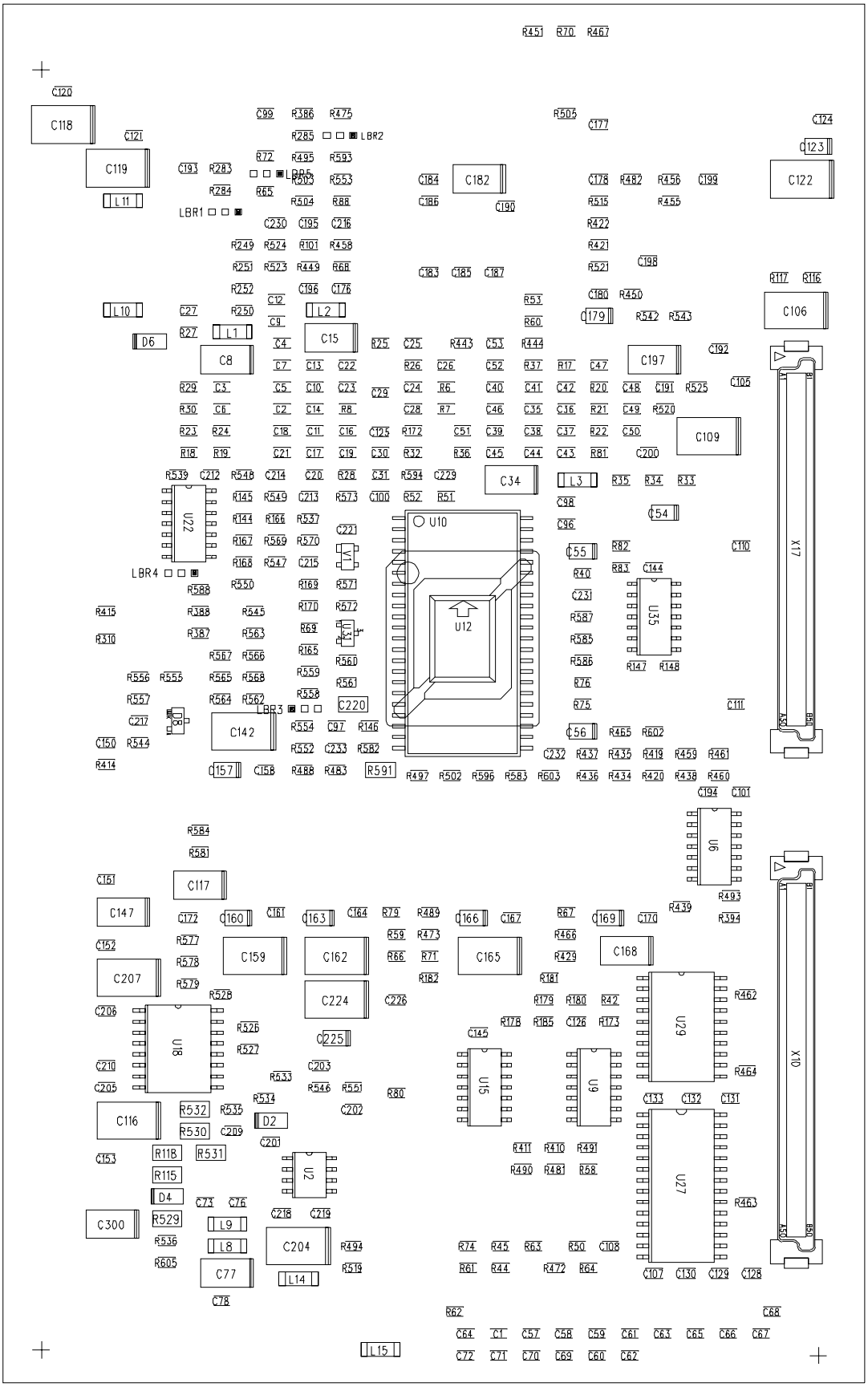


Fig. 24: Gamma7-CPU Solder Side

8.2.2. Gamma7-VME

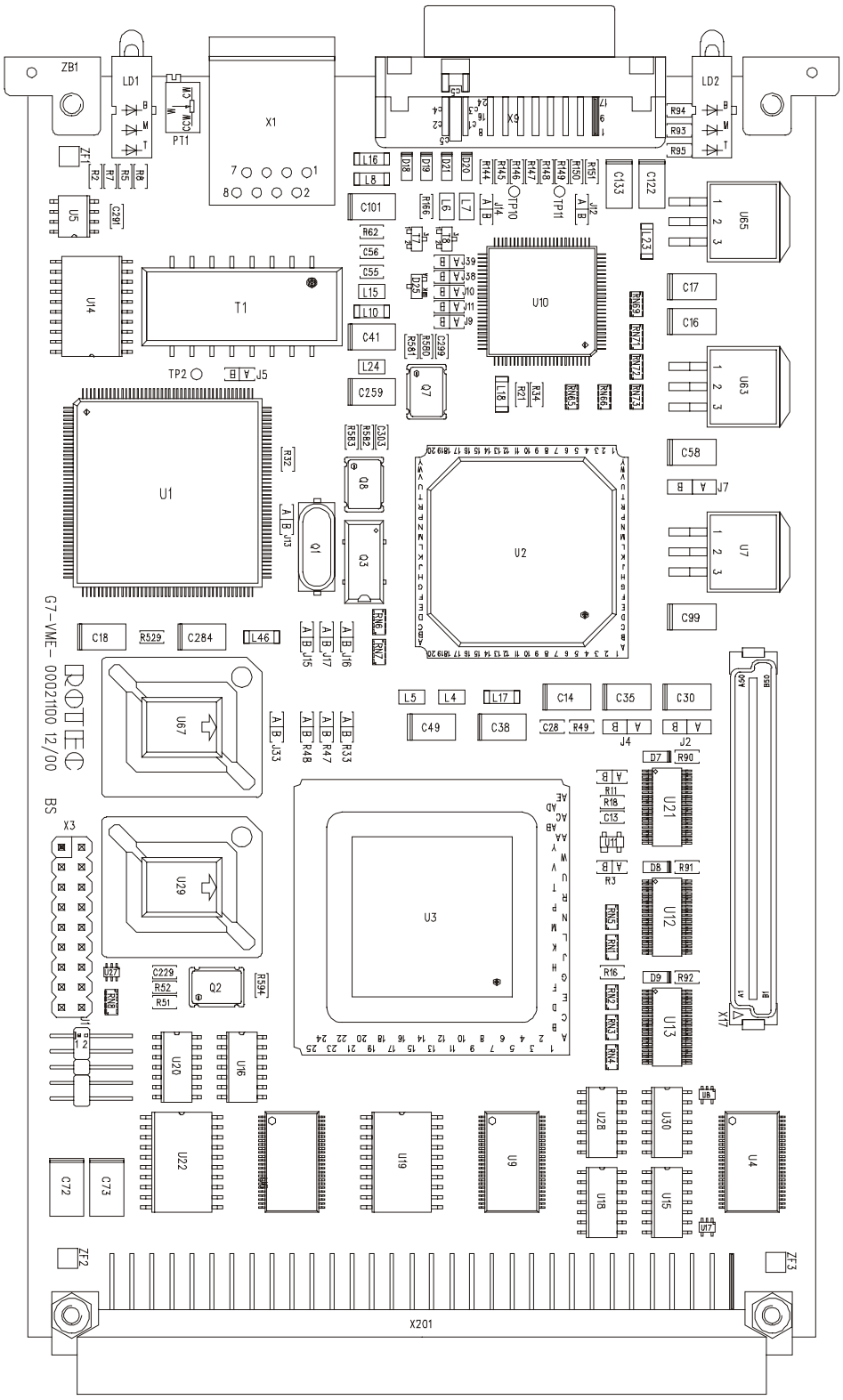


Fig. 25: Gamma7-VME Component Side

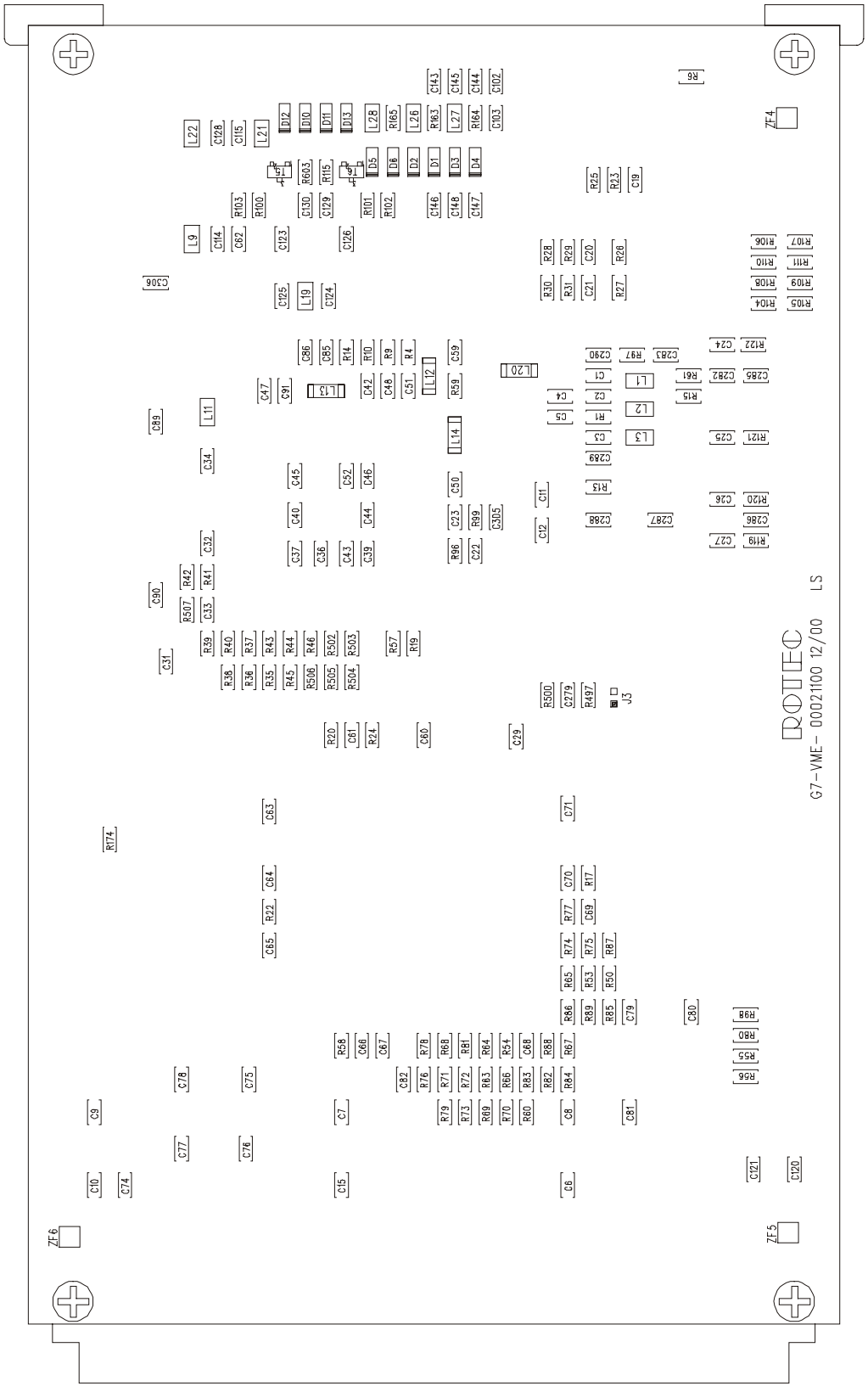


Fig. 26: Gamma7-VME Solder Side

8.2.3. Gamma7-HDD

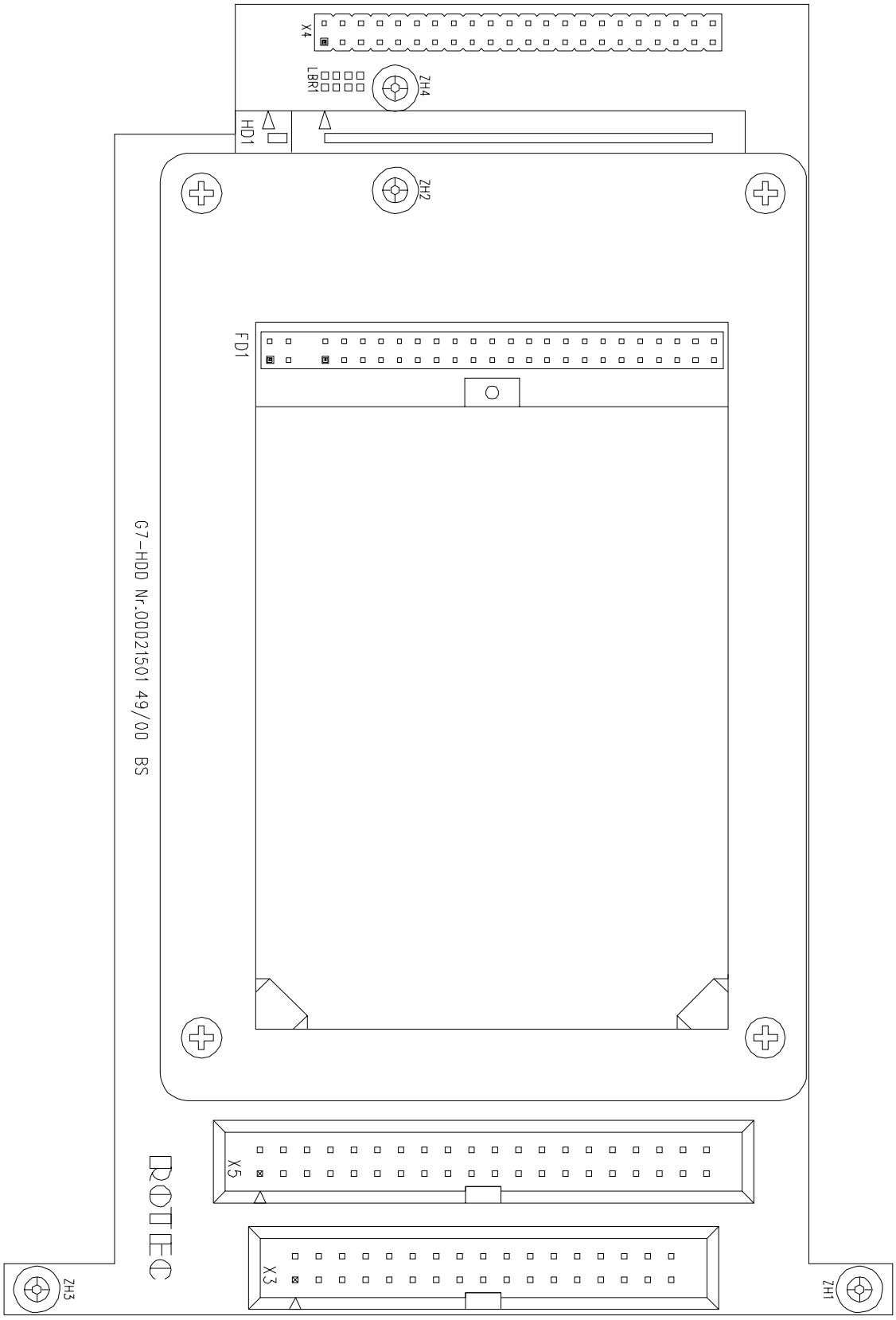


Fig. 27: Gamma7-HDD Component Side

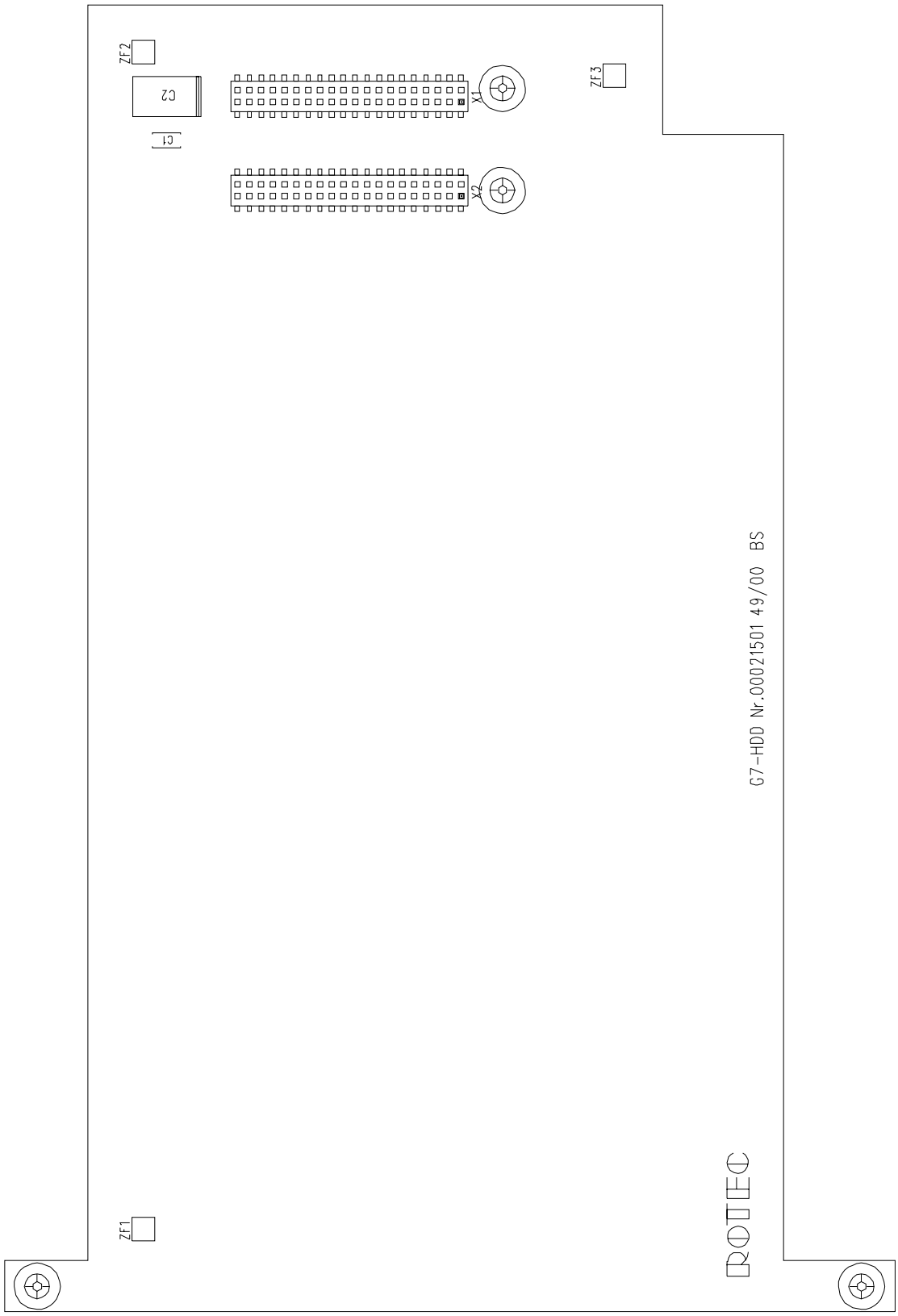


Fig. 28: Gamma7-HDD Solder Side

8.2.4. Gamma7-104AD

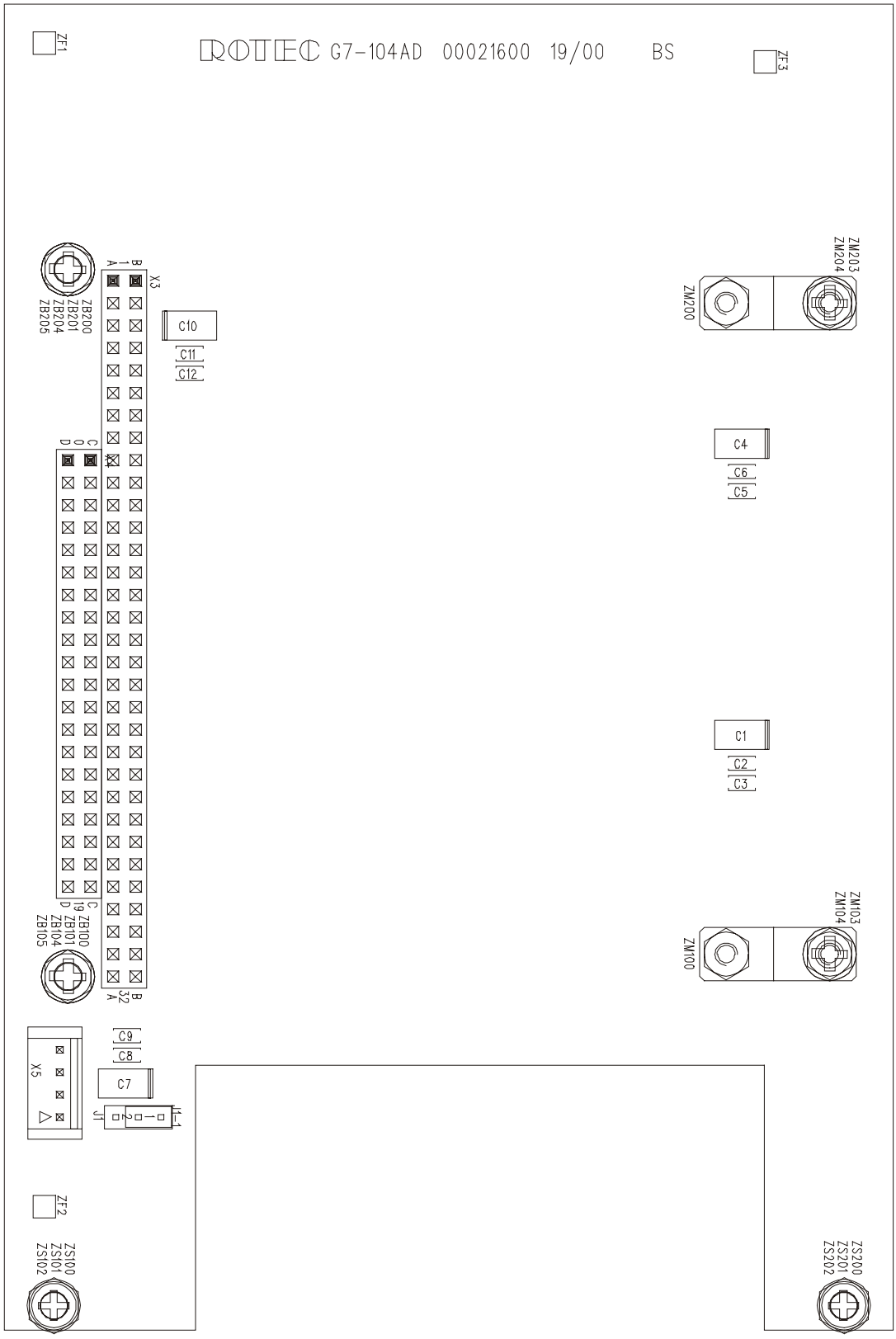


Fig. 29: Gamma7-104AD Component Side

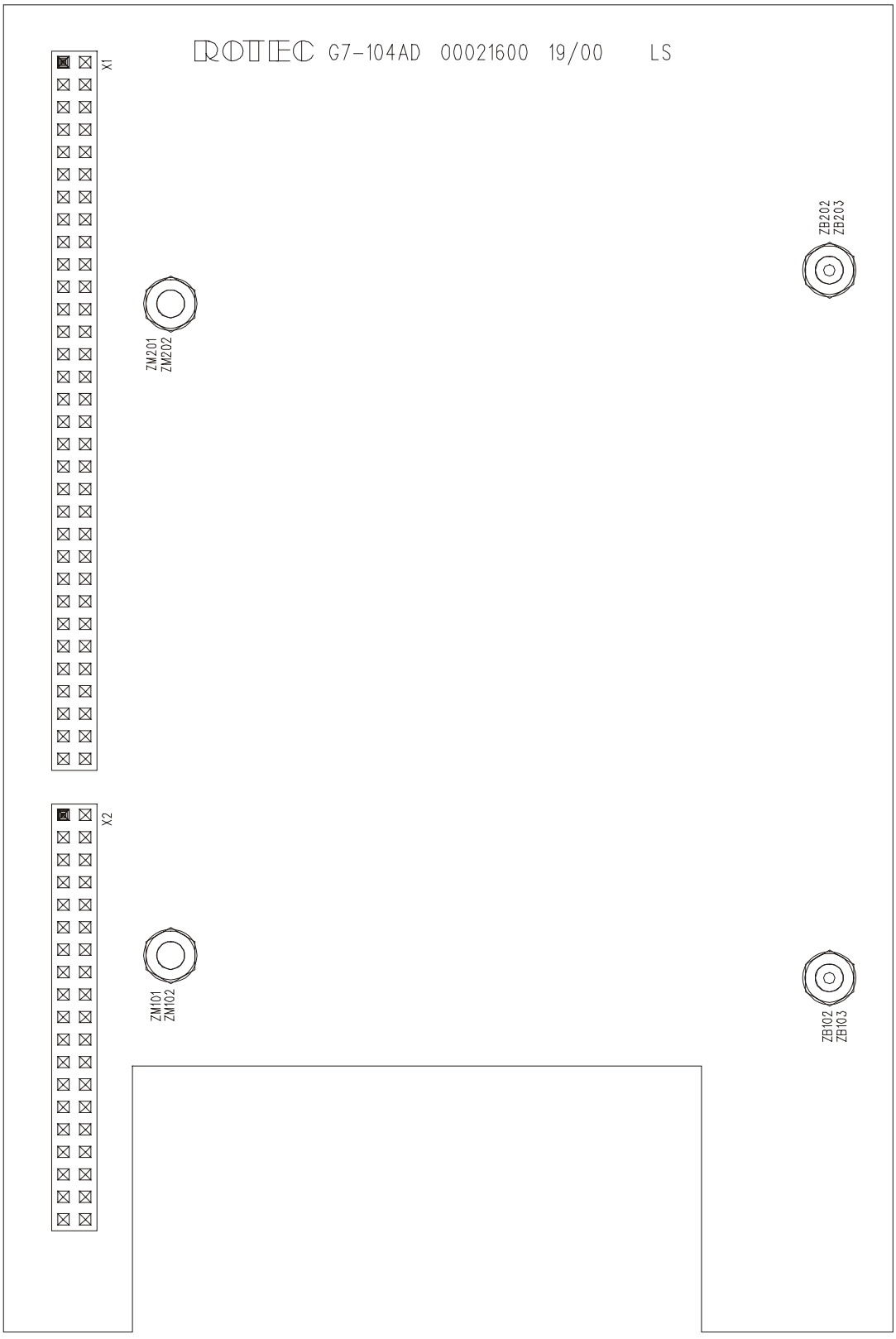


Fig. 30: Gamma7-104AD Solder Side