Modular Computers®

IUC860

(E)CXC Power PC Fast Ethernet/Serial Communications Controller

Manual ID: 22398, Rev. Index 01
November 2000

The product described in this manual is in compliance with all applied CE standards.

Revision History

Manual/Product Title:	IUC860		
Manual ID Number:	22398		
Rev. Index	**Brief Description of Changes**	**Board Index**	**Date of Issue**
01	Initial Issue	00	Nov 2000

Imprint

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This manual was realized by: **TPD/Engineering, PEP Modular Computers GmbH**.

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Preface

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Preface

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Explanation of Symbols



CE Conformity

This symbol indicates that the product described in this manual is in compliance with all applied CE standards. Please refer also to the section “Applied Standards” in this manual.



Caution, Electric Shock!

This symbol and title warn of hazards due to electrical shocks (> 60V) when touching products or parts of them. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your material.

Please refer also to the section “High Voltage Safety Instructions” on the following page.



Warning, ESD Sensitive Device!

This symbol and title inform that electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Please read also the section “Special Handling and Unpacking Instructions” on the following page.



Warning!

This symbol and title emphasize points which, if not fully understood and taken into consideration by the reader, may endanger your health and/or result in damage to your material.



Note...

This symbol and title emphasize aspects the reader should read through carefully for his or her own advantage.

PEP Advantage

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Serious electrical shock hazards can exist during all installation, repair and maintenance operations with this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing work.

Special Handling and Unpacking Instructions



ESD Sensitive Device!

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- Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.
- Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.
- It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory back-up, ensure that the board is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the board.

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- In order to maintain *PEP's* product warranty, this product must not be altered or modified in any way. Changes or modifications to the device, which are not explicitly approved by *PEP Modular Computers* and described in this manual or received from *PEP* Technical Support as a special handling instruction, will void your warranty.
- This device should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This applies also to the operational temperature range of the specific board version, which must not be exceeded. If batteries are present their temperature restrictions must be taken into account.
- In performing all necessary installation and application operations, please follow only the instructions supplied by the present manual.
- Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the board please re-pack it as nearly as possible in the manner in which it was delivered.
- Special care is necessary when handling or unpacking the product. Please, consult the special handling and unpacking instruction on the previous page of this manual.

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If the customer's eligibility for warranty has not been voided, in the event of any claim, he may return the product at the earliest possible convenience to the original place of purchase, together with a copy of the original document of purchase, a full description of the application the product is used on and a description of the defect. Pack the product in such a way as to ensure safe transportation (see our safety instructions).

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Chapter 1

Introduction

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1. Introduction

1.1 System Overview

The PEP Modular Computers product described in this manual is designed for use with the Controller eXtension Connector (CXC) bus architecture. In addition, this product also supports the enhanced CXC standard (ECXC). Both local mezzanine interface standards represent a streamlined variant of the VMEbus standard supplying a wide range of industrial I/O functions for industrial universal controllers. Some of the major advantages of the (E)CXC standard are:

- internationally accepted VITA standard;
- easier to setup and configure than VMEbus;
- optimized reliability achieved through reduced design complexity;
- compact application systems resulting from the reduced form factor.

Many system-relevant features that are specific for *PEP Modular Computers* CXC and Enhanced CXC systems can be found in the *PEP* CXC Reference Manual.

For detailled information concerning the (E)CXC modular package interface (MPI) standard, consult instead the VITA/*PEP* CXC MPI Specification which is available via the *VMEbus International Trade Association (VITA): http://www.vita.com*.

The CXC Reference Manual includes the following information:

- Functional description
- Slot assignments
- Schematics

The CXC MPI Specification includes the following information:

- Mechanical dimensions
- Electrical specifications
- Interface description
- ID Byte assignment

1.2 Product Overview

The IUC860 is a comprehensive single-height PowerQUICC™ computing platform which combines high computational performance with flexible I/O through use of (E)CXC bus interfaces and excellent communication ability afforded by the Motorola PowerQUICC™ RISC controller.

The IUC860 with its embedded PowerPC core (EPC) not only enables high computational performace but dispenses with the usual restrictions associated with serial communication using currently available off-the-shelf products. The PowerQUICC™ processor's internal Communications Processor Module (CPM) combined with the standard built-in Fast Ethernet interface makes the IUC860 ideally suited for data communication and networking applications.

The IUC860 employs an OS-independent boot loader that enables the loading of any operating system available for the PowerPC. This boot loader makes an update of the Flash contents and automatically downloads from Flash to DRAM before booting the OS. For performance reasons the OS and user programs are started from the DRAM.

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1.3 Board Overview

1.3.1 Board Introduction

The IUC860 is a 3U/4HP (Enhanced) CXC combined system and communications controller board based on Motorola's MPC860T PowerQUICC™ (Quad Integrated Communications Controller) microprocessor. This processor combines four high-speed multi-protocol serial I/O channels, two RS232 data input/terminal interfaces, and a Fast Ethernet controller to provide outstanding flexibility and computing power for advanced computer controlled communication applications. The IUC860 realizes the advantages of the MPC860T in a single board which provides two serial I/O channels and one Fast Ethernet interface on-board with additional expansion capability being provided by the CXCbus.

Some of the outstanding features of the product described in this manual are:

- (E)CXC system and communications controller board
- 32-bit Motorola MPC860T PowerQUICC™ microprocessor with integrated CPU, communications controller, and Fast Ethernet controller (FEC)
- 80 MHz CPU frequency
- CPU on-chip background debugging
- up to 64 MB DRAM
- up to 4 MB Flash memory
- 1 MB SRAM (backed-up)
- 2 kBit serial EEPROM
- up to 1 MB of on-board EPROM or up to 512 kB of on-board Flash memory
- real-time clock (backed-up)
- five different communication standards possible:
  - Serial I/O (RS232, RS485; RS422 on request)
  - Ethernet (10baseT or 100baseT Fast Ethernet)
- expandability through the external serial interface module CXM-SIO3
- Reset and Abort control (front panel buttons)
- front panel system status indicators:
  - two general purpose and one watchdog
  - three Fast Ethernet status indicators: ACT., LNK., and SPEED
- VxWorks® drivers

1.3.2 Board-Specific Information

The IUC860 mainboard is provided with the following standard connectors:

- two non-optoisolated RS232 serial interfaces on front panel, TERM (RJ12) and SER0 (RJ45)
- one Fast Ethernet interface on front panel (RJ45)
- one set of memory piggyback interface connectors (two 50-pin female connectors)
- one EPROM/Flash 32-pin DIP socket
- a background debug mode (BDM) interface (one 10-pin row male connector)
- a JTAG/ISP programming and testing interface (one 10-pin row male connector)
- an Enhanced CXC backplane interface (one 96-pin DIN 41612, style C male connector)

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Applications requiring further communication interfaces may be upgraded by means of an external CXM-SIO3 serial interface module which provides the following interface extension possibilities:

- RS232 serial interface connectors (non-optoisolated)
- Serial interface piggyback ports
- Serial communications piggyback port

Only one CXM-SIO3 module can be controlled by an IUC860 board. The CXM-SIO3 module provides access to internal communication signals of the base board that are transferred to the module via the CXC bus.

For a detailed list and description of the front panel interface and serial interface/communication piggybacks please refer to the CXM-SIO3 user's manual and its "Serial Communications Piggybacks" appendix respectively.

1.3.3 Main Memory and BootRom

IUC860 main memory and BootRom is provided using DM60x Memory Module piggybacks. By means of these piggybacks the following memory configurations are possible:

- up to 64 MB of DRAM
- up to 4 MB of Flash memory which can be used for the Bootstrap Loader and application.

For a detailled description of the memory piggybacks please refer to appendix A of this manual.

In addition to the Flash memory available on the DM60x Memory Modules there is a single 32- pin DIP socket on the IUC860 main board which accomodates up to 1 MB of EPROM or 512 kB of Flash memory which can be used for the Bootstrap Loader instead of the Flash memory located on the DM60x Memory Module

1.4 System Relevant Information

The following system relevant information is general in nature but should still be considered when developing applications using the IUC860.

Table 1-1: System Relevant Information

SUBJECT	INFORMATION
System Configuration	A IUC860-based system is made up of one system controller, and up to 7 other I/O boards can be located within one system.
Master / Slave Functionality	The IUC860 can operate only as a system controller.
Board Location in the System	The IUC860 board must be installed in the system controller slot of the CXC backplane.
Operating Systems	The IUC860 can operate under the following operating systems: VxWorks®

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1.4.1 System Configuration

As a combined CXC system and communications controller board the IUC860 must always have system controller function. Therefore, it is not possible to operate more than one IUC860 in one system, and the board must be always installed in the system controller slot.

The IUC860 can be installed in any CXC 3U rack. If a CXM-SIO3 or a CXM-SCSI module is used in combination with the IUC860, it must be placed immediately to the right of the system controller board.

1.4.2 Bootstrap Loader

Via the IUC860 front panel serial interface connectors the flash memory of the board's memory piggyback can be re-programmed by means of the Bootstrap Loader which is delivered already installed in the DM60x memory piggybacks. This standalone software has the capability of loading Flash memory from Motorola S-records or from any absolute address. If the downloaded image does not work properly, the Bootstrap Loader can be re-entered, the memory contents analyzed and a further programming cycle initiated



Warning!

To avoid damaging of your Bootstrap Loader and consequently leaving your board unusable, please read chapter 5 before resetting the flash contents of your IUC860 board.

1.4.3 Operating Systems

The IUC860 can operate under the following operating system:

- VxWorks®

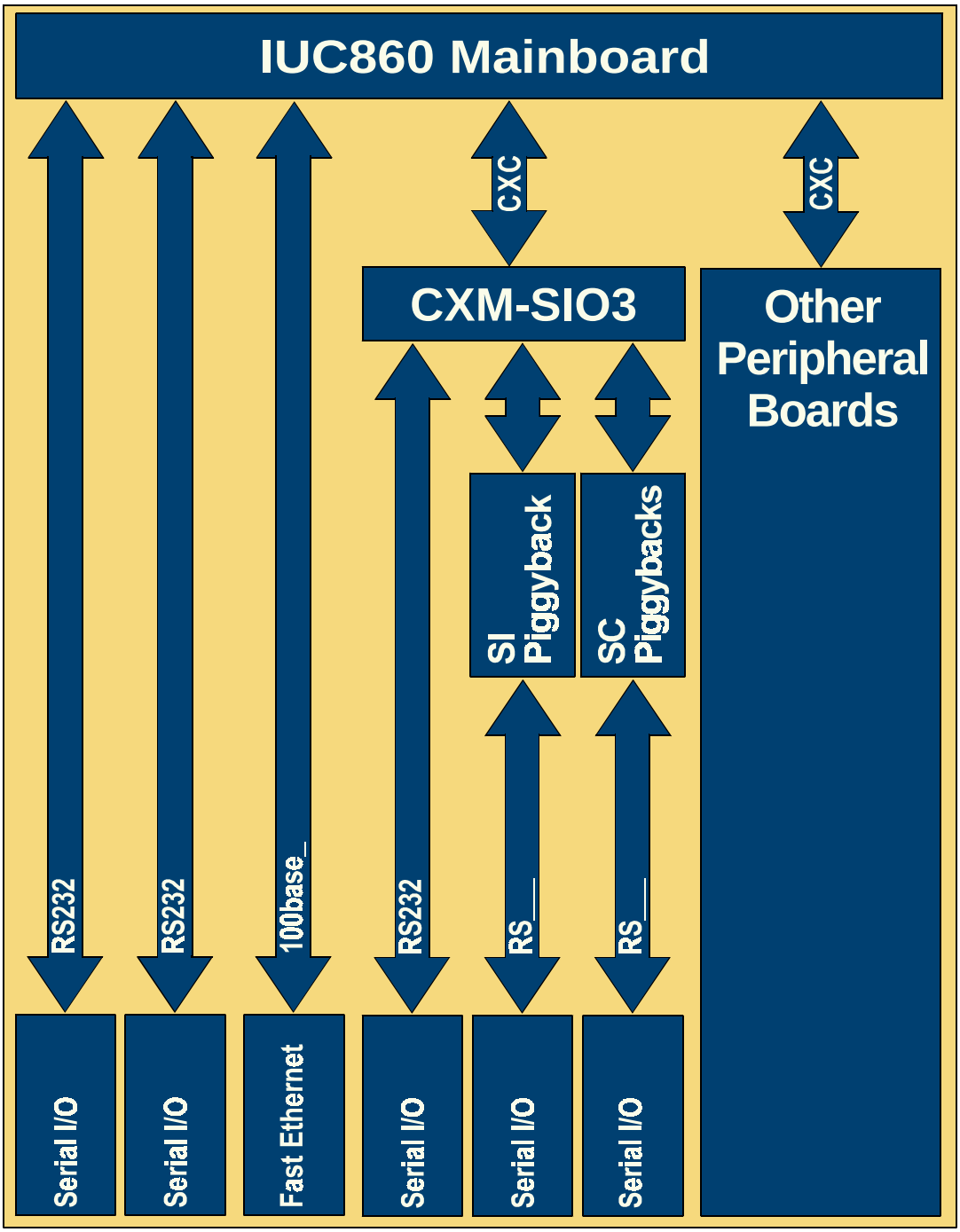
Porting to other operating systems can be done on request.

1.5 Board Diagrams

The following diagrams provide additional information concerning board functionality and component layout.

1.5.1 System Level Functional Block Diagram

Figure 1-1: IUC860 System-Level Functional Block Diagram



Legend:

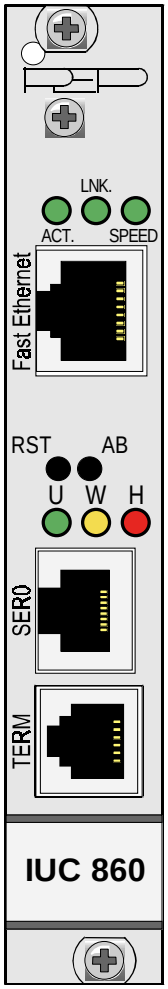
RS__: RS232 non-optoisolated or RS485 optoisolated

100base_: 10baseT or 100baseT Fast Ethernet

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1.5.2 Front Panel

Figure 1-2: IUC860 Front Panel



Legend:

LED1 Group

- Green (“ACT.”): Data send/receive
- Green (“LNK.”): Link established in both directions
- Green (“SPEED”): Data rate: on = 100 Mbps; off = 10 Mbps

Push Buttons:

- RST (left): Reset
- AB (right): Abort

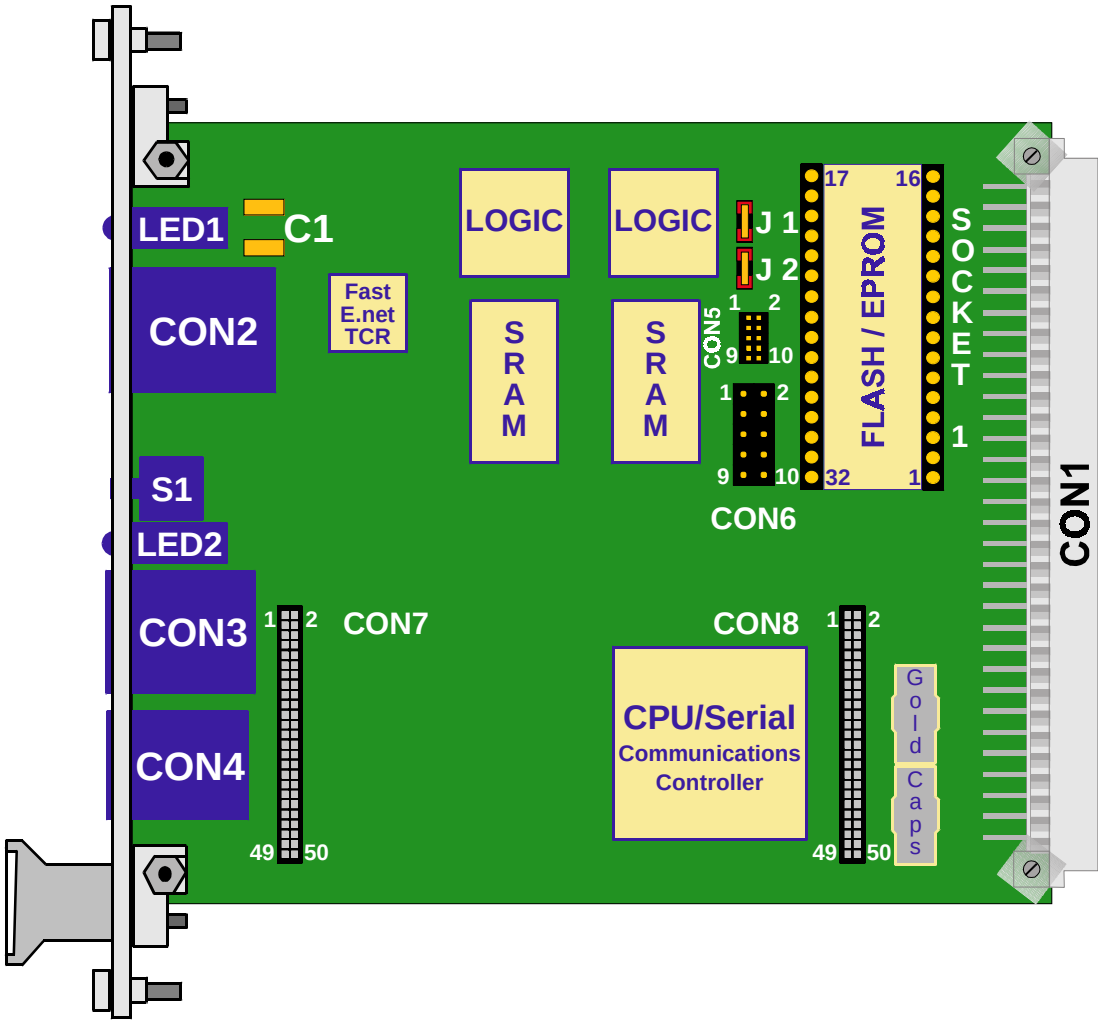
LED2 Group

- Green (“U”): General purpose
- Yellow (“W”): Watchdog
- Red (“H”): General purpose

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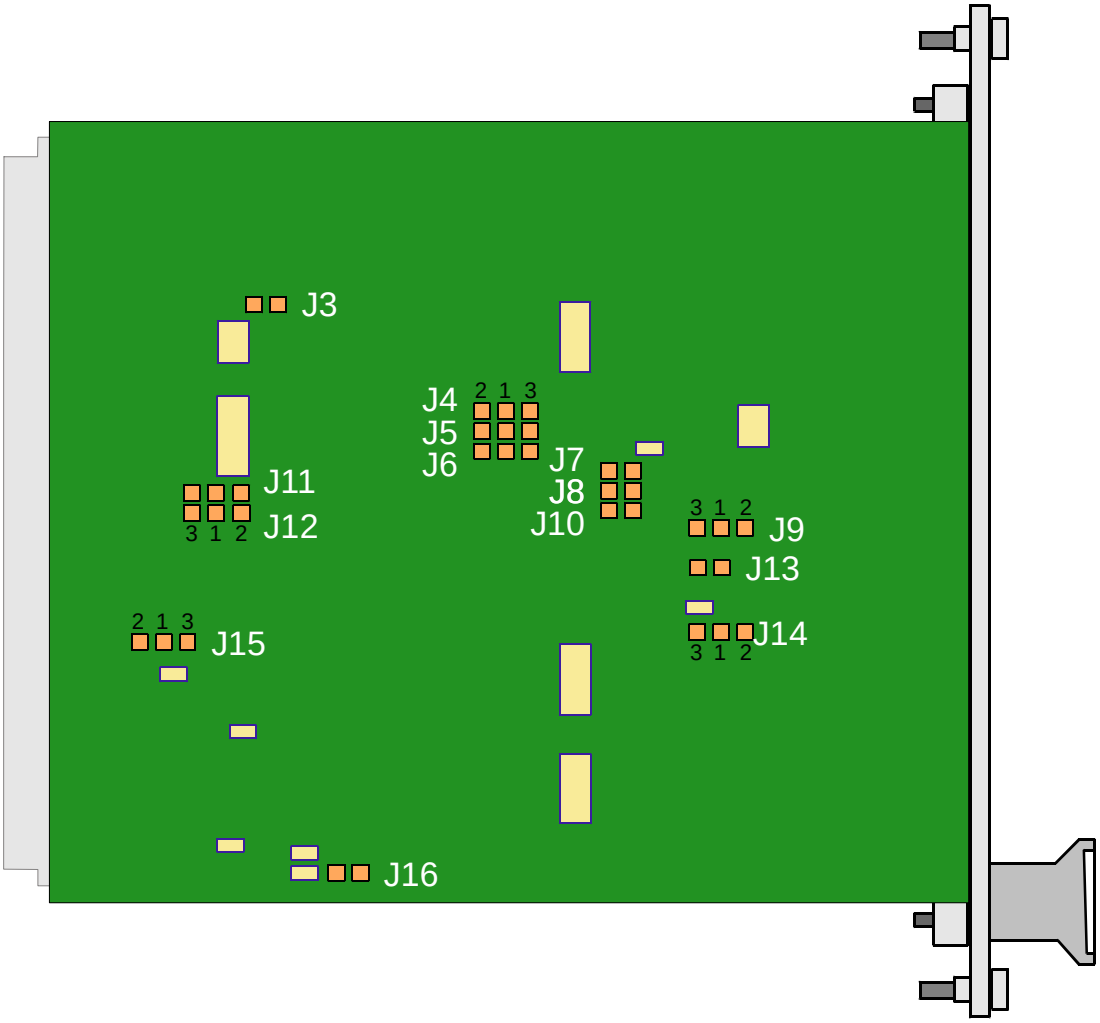
1.5.3 Board Layouts

Figure 1-3: IUC860 Board (Front View)



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Figure 1-4: IUC860 Board Diagram (reverse)



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1.6 Technical Specifications

Table 1-2: IUC860 Main Specifications

	IUC860	Specifications
Processor and Related	Processor	Motorola Power QUICC MPC860T, 80MHz
	Main Memory	Up to 64 MB of add-on DRAM via DM60x memory modules
	Cache Structure	4 KB instruction cache and 4 KB data cache
	FEC	Independent IEEE 802.3u compliant 10/100baseT Fast Ethernet Controller
	Watchdog	Watchdog generates a system reset
	RTC	Realtime clock, backed up using GoldCap with the data retention being typically about 6 to 7 days
Peripheral Memory	Soldered, Onboard	
	SRAM	1 MB, backed up using GoldCap with the data retention being typically about 6 to 7 days
	EEPROM (SPI)	2 kBit; 1 kBit for system and 1 kBit for applications (User EEPROM write protection possible)
	DM60x Memory Module	
	Flash	Up to 4 MB of Flash memory
	Memory Expansion Socket 1	
	EPROM/Flash	Up to 1 MB of EPROM or 512 kB of Flash memory
External Interfaces	Fast Ethernet	10BaseT / 100BaseTX via RJ45 connector
	Serial Ports	Two RS-232 ports on front panel:TERM:standard RS232 SER0:full modem RS232 Three RS-232/485 full modem ports to CXC: SCC2, SCC3, SCC4
	(E)CXC	(Enhanced) Controller eXtension Connector: CXC expansion bus
Internal Interfaces	Memory Sockets	Two 50-pin SMD connectors for one DM60x Memory Module, and one 32-pin DIP socket for EPROM or Flash memory
	Debug Interface	BDM 10-pin twin row connecter
	JTAG/ISP	JTAG/ISP 10-pin SMD connecter for programming and testing purposes
Indicators / Switches	LED's	3 LED's for indicating system status (two user programmable, one fixed); 3 LED's indicating the status of the Fast Ethernet link
	Switches, Front Panel	Two, non-latching, push-button type switches for resetting the system or accessing the bootstrap loader during booting of the operating system

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Table 1-2: IUC860 Main Specifications (Continued)

	IUC860	Specifications
General	Mechanical	Conforms with IEEE 1101.1
	Power Consumption	Typ. 6.2 watts at 5V (measured with DM600 Memory Module with 4 MB DRAM and 1 MB Flash)
	Temperature Range	0°C to +70°C Standard
	Humidity	0% to 95% non-condensing
	Dimensions	100 mm x 115 mm, 4 HP / 3U CXC format
	Board Weight	126 g without add-on memory 155 g with DM600 Memory Module
Software	Operating System Support	Initial boot loader with capability to load VxWorks operating system

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1.7 Applied Standards

1.7.1 CE Compliance

The *PEP Modular Computers'* (E)CXC systems comply with the requirements of the following CE-relevant standards:

- Emission EN50081-1
- Immission EN50082-2
- Electrical Safety EN60950

1.7.2 Mechanical Compliance

- Mechanical Dimensions IEEE 1101.1

1.7.3 Environmental Tests

- Vibration IEC68-2-6
- Random Vibration, Broadband IEC68-2-64 (3U boards)
- Permanent Shock IEC68-2-29
- Single Shock IEC68-2-27

1.8 Related Publications

1.8.1 CXC Systems/Boards

- *PEP Modular Computers* CXC Reference Manual (ID 16819)
- VITA/*PEP Modular Computers* CXC MPI Draft Specification, Rev. 3.10 (ID 12190)
- *PEP Modular Computers* CXM-SIO3 Manual (ID 14411)
- *PEP Modular Computers* CXM-SCSI Manual (ID 03545)

1.8.2 Manufacturers' Component Documentation

- Motorola: MPC860T Power QUICC User's Manual
- EM Microelectronic: V3021 1-Bit Real-Time Clock Datasheet
- XICOR: X25C02 SPI Serial EEPROM Datasheet

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Chapter 2

Functional Description

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2. Functional Description

The following chapters provide more detailed board information covering the following: board general information, memory, board interfaces, and special functions.

2.1 General Information

The IUC860 is a 3U/4HP (E)CXC combined system and communications controller board based on Motorola's MPC860T PowerQUICC™ (Quad Integrated Communications Controller) microprocessor. Because the MPC860T combines a CPU together with a serial communications controller and a Fast Ethernet controller, it is particularly well suited for system control functions in applications with demanding communications requirements such as LAN, WAN, or fieldbusses (CAN, LON, PROFIBUS).

The IUC860 provides up to six serial communications channels and one Fast Ethernet channel.

The serial channels of the IUC860 are configured in the following way:

- Two service/debug channels are extended to the front panel connectors TERM and SER0 providing standard RS232 (SMC2) and full modem RS232 (SCC1) support respectively.
- Three of the remaining channels: SCC2, SCC3, and SCC4 provide full modem, multi-protocol support and are routed to the CXC bus for use with CXM modules.
- The last channel, SMC1, which provides standard RS232 is available if required, but is not configured for use at the present.

The Fast Ethernet interface is extended to the front panel and provides 10/100baseT, 10/100 Mbps Ethernet support.

External serial interfacing can be achieved through the use of a CXM-SIO3 type external serial interface module with a variety of serial interface (SI) piggybacks and/or serial communications (SC) piggybacks which are available from *PEP.* The IUC860/ CXM-SIO3 tandem represents a really powerful and versatile communications system.

The IUC860 also allows for a variety of memory configurations: DRAM and flash memory located on special memory piggybacks, add-on Flash/EPROM on the DIP socket, gold cap backed-up SRAM, and EEPROM.

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2.2 Memory Configurations

Main memory (DRAM) and standard BootRom for the IUC860 is made available through the use of *PEP's* family of DM60x Memory Modules. The DM60x piggybacks provide between 1MB and 64MB of DRAM with 32-bit access and up to 4 MB of +5V flash memory. This special DRAM/Flash piggyback allows the user to take advantage of the on-board programming facility to produce low cost upgrades by simply overwriting existing stored data. This memory can be configured with different memory options allowing remarkable flexibility when customizing memory requirements for real-time applications.

In addition to the DM60x Memory Module there is a DIL socket located on the IUC860 mainboard which can accommodate an additional EPROM/Flash device. Up to 1 MB of EPROM or 512 kB of Flash can be installed. This memory is particularly suited for situations which require separation of the bootstrap loader and the application. The selection of the boot memory address to be used is achieved by hardware jumpering. See chapter 4 for configuration information.

Exchange and retention of system relevant data from the CXC bus to the CPU and peripheral boards is provided by means of a 16-bit wide 1 MB dual-ported SRAM which is backed-up by Gold Caps.

Configuration data are stored in a 2 kBit EEPROM. 1 kBit is used for factory-specific configuration purposes, and 1 kBit is available for application-specific configuration data.

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2.3 Serial Communications Control

Under the aspect of serial communications control, a major advantage of the MPC860T serial communications controller core is its compatibility with all important communication standards. A detailled description of all control functions is provided on the following pages.

For the mainboard interface connector pinouts refer also to the “Board Interfaces” section of this chapter. For a description and pinouts of the CXM-SIO3 frontpanel interface connectors please refer to the CXM-SIO3 user’s manual and its “Serial Communications Piggybacks” appendix.

2.3.1 Communication Standards and Protocols

Five communication standards are available with the IUC860:

- Serial I/O (RS232, RS485; RS422)
- Ethernet (10baseT, 100baseT)

Serial communications using the RS232 standard are available at the IUC860 mainboard front panel. In addition, RS232 communication is possible via a CXM-SIO3 external serial interface module. Communications using the PROFIBUS protocol are supported by an optoisolated, half-duplex RS485 serial I/O interface implemented on a dedicated piggyback to be connected to the SI Interface of the external serial interface module. RS422 is not commonly available on the IUC860 but can be supplied by *PEP Modular Computers* on special request.

The MPC860T processor also supports a full set of IEEE 802.3/Ethernet media access control and channel interface functions. The interface adapter and transceiver function are implemented on-board to support 10/100baseT.

2.3.2 Serial I/O Channelling

The IUC860 mainboard is provided with TxD and RxD signals by the controller’s SMC1 and SMC2 channels and supply RS232 interface software handshake (XON/XOFF) capability. TERM is configured for SMC2.

The full modem interface located on the front panel (SER0) supplies RxD, TxD, RTS, CTS, CD, DTR. The three full modem interfaces available via the CXM-SIO3 supply RXD, TXD, RTS, CTS, CD, DTR, RCLK, and TCLK. The SCC1 channel of the MPC860T provides the interface to the SER0 RJ45 connector of the IUC860. All other channels of the controller (SCC2, SCC3 and SCC4) are ported to the CXC interface.

Due to the fact that three out of the four SCC channels are routed to the CXC interface connector, a CXM-SIO3 external serial interface module can be installed in the system which therefore becomes a sort of “privileged” serial I/O extension of the IUC860 board itself. Only one CXM-SIO3 module can be controlled by an IUC860 board.

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The following table shows the availability of the various logical serial ports on the internal interfaces for configuration.

Table 2-1: IUC860 Serial Interface Channel Configurations

MPC860T RE-SOURCE	DEDICATED FUNCTION	CONFIGURED VIA	PHYSICAL STANDARDS	CONNECTOR	PORT NAME ON FRONT PANEL
SCC1	Serial I/O	ADM211 transceiver	RS232	CON3	SER0
SCC2	Serial I/O	CXM	RS232 RS485	CON1	not available
SCC3	Serial I/O	CXM	RS232 RS485	CON1	not available
SCC4	Serial I/O	CXM	RS232 RS485	CON1	not available
SMC1 (not used)	-	-	RS232	-	-
SMC2	Terminal Port	ADM211 transceiver	RS232	CON4	TERM

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To achieve flexibility, a full modem RS232 interface on the SER0 port, and to make use of the Fast Ethernet controller of the MPC860T the internal routing of the general purpose pins of the MPC860T has been realized in the following way.

Table 2-2: Serial Interface Routing

SERIAL I/O SIGNAL	MPC860T ROUTING SCC1	MPC860T ROUTING SCC2	MPC860T ROUTING SCC3	MPC860T ROUTING SCC4	MPC860T ROUTING SMC1	MPC860T ROUTING SMC2
TXD	PA14	PA12	PA10	PA8	PB25	PB21
RXD	PA15	PA13	PA11	PA9	PB24	PB20
CTS	PC11	PC9	PC7	PC5	-	-
RTS	PB19	PB18	PB17	PB16	-	-
CD	PC10	PC8	PC6	PC4	-	-
DTR	PA7	PB26	PB27	PB31	-	-
RCLK	PA7	PA6	PA2	PA0	-	-
TCLK	PA4	PA5	PA3	PA1	-	-

Notes: General purpose pin PA7 of the MPC860T can be used either as RCLK or DTR, but, however, on the IUC860 it must be configured as DTR because SCC1 is routed to the SER0 front panel interface where no clocks (RCLK or TCLK) are used.

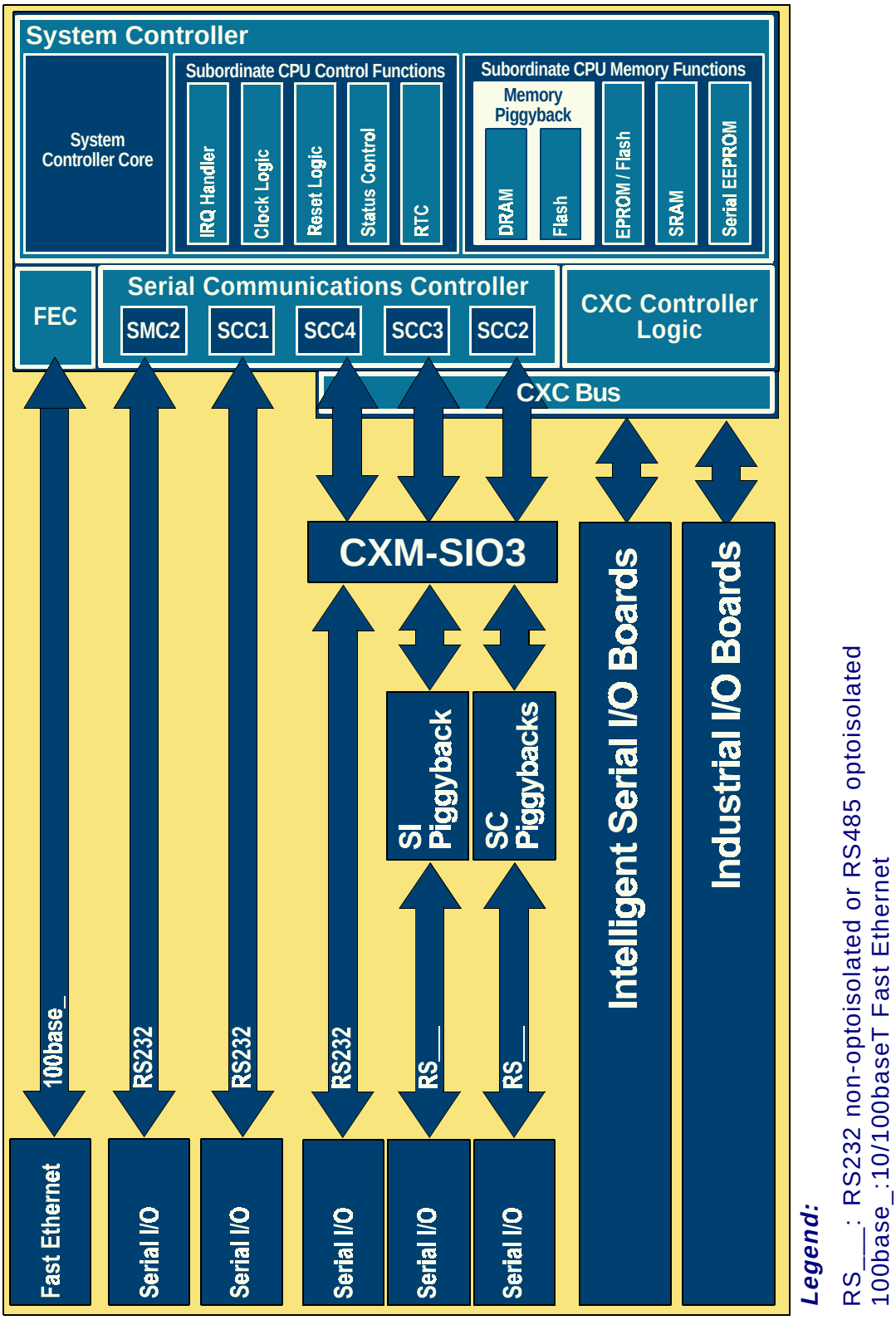
PB20, PB21, PB24 and PB25 are also routed to the CXC connector and connected to user defined pins.

- PB20 to C4
- PB21 to B11
- PB24 to C10
- PB25 to C1

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2.4 Functional Block Diagram

Figure 2-1: IUC860 Board-Level Functional Block Diagram



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2.5 Board Interfaces

The following section provides a description of the mainboard interface connectors and their pinouts.

2.5.1 TERM and SER0 Serial I/O Interfaces

The TERM front panel connector (CON4) is provided with TxD and RxD signals by the controller's SMC2 channel with software handshake (XON/XOFF) capability. It is configured for terminal use by default.

The SER0 front panel connector (CON3) is provided with TXD, RXD, RTS, CTS, CD, and DTR signals by the controller's SCC1 channel. As such it functions as a full modem interface.

The signal/pin assignments of these connectors are shown as follows.

Figure 2-2: TERM (CON4) and SER0 (CON3) Serial Interfaces

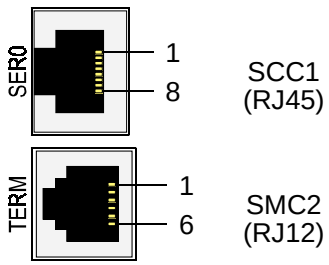


Table 2-3: TERM (CON4) Serial Interface Pinout

PIN	SIGNAL
1	N/C
2	GND
3	TXD
4	RXD
5	N/C
6	N/C

Table 2-4: SER0 (CON3) Serial Interface Pinout

PIN	SIGNAL
1	N/C
2	RTS
3	GND
4	TXD
5	RXD
6	CD
7	CTS
8	DTR

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2.5.2 Fast Ethernet Interface

The Fast Ethernet interface is based on the MPC860T on-chip Fast Ethernet Controller and the LXT970ATC PHY transceiver chip from LEVEL ONE.

The main features of the Fast Ethernet are as follows:

- full compliance with IEEE 802.3 standard for 10baseT and 100baseT,
- confgurable via MII or external control pins,
- configurable for DTE, repeater, or switch operation,
- full duplex support at both 10 and 100 Mbps,
- IEEE 802.3u auto-negotiation support,
- integrated FIFO's and bursting DMA.

The signal/pin assignments for this connector are as follows.

Figure 2-3: Fast Ethernet Connector (CON2)

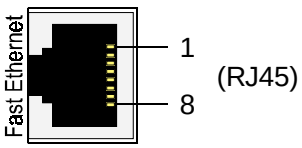


Table 2-5: Fast Ethernet Connector (CON2) Pinout

PIN NUMBER	SIGNAL
1	TX+
2	TX-
3	RX+
4	N/C
5	N/C
6	RX-
7	N/C
8	N/C

2.5.3 DM60x Memory Module Interface

The IUC860 is equipped with an interface for PEP's DM60x series of memory piggyback modules. Two 50-pin twin row connectors (CON7 and CON8) provide interfacing to one DM60x memory module. This allows for configurations of up to 64 MB of DRAM and 4 MB of Flash memory depending on the type of memory module installed. Addressing and jumper configuration information is provided in chapter 4, and Appendix A contains further details of the DM60x memory modules.

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2.5.4 Memory Expansion Connector

One 32-pin DIL memory expansion socket is provided for the addition of various types of memory expansion devices (up 1 MB EPROM or 512 kB Flash) with 8-bit wide data address. Use of this memory is controlled by jumper J2 which allows it to be used either as the bootstrap loader source or as additional memory if required. Jumpers J11 and J12 control the type of used device. Addressing and jumper configuration information is provided in chapter 4.

Figure 2-4: Memory Expansion Connector

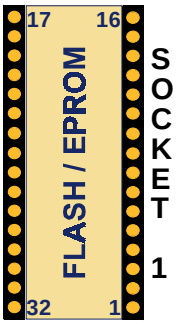


Table 2-6: Memory Devices Supported

DESCRIPTION		
DEVICE	**SPEED**	**SIZE**
EPROM 27C010	120 ns	128 kByte
EPROM 27C020	120 ns	256 kByte
EPROM 27C040	120 ns	512 kByte
EPROM 27C080	120 ns	1 MByte
FLASH 28F010	120 ns	128 kByte
FLASH 28F020	120 ns	256 kByte
FLASH 29F010	120 ns	128 kByte
FLASH 29F040	120 ns	512 kByte

2.5.5 (E)CXC Backplane Interface

The IUC860 is equipped with a (E)CXC backplane interface connector (CON1).

CXC and ECXC both contain a 16-bit data bus and eight decoded chip select lines. In total, there are eight control signals (CXC_CS0...CXC_CS7). The main difference between the two VITA standards is the amount of address space available for peripheral devices:

- CXC: 7 address lines, 8 x 128 words (256 bytes) per slot (address room available = 0x400 or 1024 bytes per slot with a total of 8192 bytes),
- ECXC: 23 address lines, 16 MB per slot, where 16 lines are multiplexed over the data bus (address room available = 0x1000 000 or 16 MB per slot with a total of 128 MB).

Furthermore, the CXC contains a 4-IRQ capability (4 edge-sensitive interrupt requests), DMA capability (1 channel, DREQ + DACK), serial ports (3 channels, Full MODEM) and a set of parallel port signals. These special CXC functions are based on the MPC860T controller resources.

For general CXC information including addressing, generic pinouts, and a cross reference to the MPC860T CPU pinouts refer to appendix B of this manual. For further details see the *PEP Modular Computers* CXC Reference Manual or the CXC Specification.

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2.6 IUC/IUC32-to-IUC860 System Upgrading

In the following the porting information required by customers wanting to upgrade their IUC-based systems to an IUC860 based one is supplied.

The CXC ports SER1, SER2 and SER3 of the MC68302/MC68360 are equivalent to ports SCC2, SCC3 and SCC4 respectively on the MPC860T controller chip.

With regard to special CXC capabilities, the CXC pinout on the IUC860 has been developed to provide maximum compatibility between the standard CXC functions.

Multifunction pins with incompatible functions with regard to the MC68302/MC68360 and MPC860T, which are called “user-defined” in the generic CXC Specification, are not part of the IUC860 CXC specification.

Although the SMC2 is configured on the mainboard, this port and the unused SMC1 port are also integrated on the CXC because of possible ISDN applications where SMC’s can be integrated and other protocols supported by the MPC860T.

Table 2-7: IUC/IUC32 -IUC860 Porting Information (Sheet 1 of 2)

CXC Function	Pin	MC68302/ MC68360 HW Comp.	MPC860T Port	Comment
IRQ_1	A1	Yes	PC12	—
IRQ_2	A2	Yes	PC13	—
IRQ_3	A3	Yes	PC14	—
IRQ_4	A4	Yes	PC15	—
DMA_ACK	C2	Yes	PB23	—
DMA_REQ	C3	Yes	PC15	—
SER1_RCLK	B1	Yes	PA6	If jumper J9 is set to 1-3. Cannot be used if jumper J9 set to 1-2.
SER1_TCLK	B2	Yes	PA5	—
SER1_TXD	B4	Yes	PA12	—
SER1_RXD	B10	Yes	PA13	—
SER1_RTS	B5	Yes	PB18	—
SER1_DTR	A13	Yes	PB26	—
SER1_CTS	B13	Yes	PC9	—
SER1_CD	B14	Yes	PC8	—
SER2_RCLK	C16	Yes	PA2	If jumper J14 is set to 1-3. Cannot be used if J14 is set to 1-2
SER2_TCLK	C15	Yes	PA3	—
SER2_TXD	C17	Yes	PA10	—
SER2_RXD	C18	Yes	PA11	—
SER2_RTS	C12	Yes	PB17	—

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Table 2-7: IUC/IUC32 -IUC860 Porting Information (Sheet 2 of 2)

CXC Function	Pin	MC68302/ MC68360 HW Comp.	MPC860T Port	Comment
SER2_DTR	A11	Yes	PB27	—
SER2_CTS	C13	Yes	PC7	—
SER2_CD	C11	Yes	PC6	—
SER3_RCLK	C6	Yes	PA0	—
SER3_TCLK	C5	Yes	PA1	—
SER3_TXD	C8	Yes	PA8	—
SER3_RXD	C9	Yes	PA9	—
SER3_RTS	B7	Yes	PB16	—
SER3_DTR	A12	Yes	PB31	—
SER3_CTS	B16	Yes	PC5	—
SER3_CD	B8	Yes	PC4	—
User-Defined	A5	No	PB14	If jumper J15 is set to 1-3. If J15 is set to 1-2, +5VSTDBY is connected to CXC pin A5.
	A6	No / Yes	PB30	SPI Clk: can be used if an ‘SPI SEL’ for example PB14 is used.
	A8	No / Yes	PB29	SPI TxD: can be used if an ‘SPI SEL’ for example PB14 is used.
	A9	No / Yes	PB28	SPI RxD: can be used if an ‘SPI SEL’ for example PB14 is used.
	A10	No	PB22	*See MPC860 User Manual*
	B11	No / Yes	PB21	Used on board SMC2 (Transmit)
	C1	No / Yes	PB25	SMC1 (Transmit)
	C4	No / Yes	PB20	Used on board SMC2 (Receive)
	C10	No / Yes	PB24	SMC1 (Receive)

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2.7 Special Board Functions

2.7.1 Real-Time Clock

The real-time clock V3021 is a 1-bit device which is accessible over the CS4 of the MPC860T. Its time-keeping features include as follows:

- seconds, minutes, hours, day of month, month, year, week day and week number in BCD format;
- leap year and week number correction;
- stand-by supply smaller than 1µA.

Short time data retention for the RTC is achieved through the use of two 0.22 F Gold Caps. Typically a backup time of 6 to 7 days should be possible with this configuration. For further information please refer to the EM Microelectronic V3021 data sheet.

2.7.2 EEPROM

The serial EEPROM is a 2 kBit device which is accessible over the three-wire Interchip SPI Interface of the MPC860T. 1 kBit of the EEPROM is reserved for factory data, including Board ID codes, Internet/Ethernet addresses, boot information etc. The rest of the EEPROM is available for the user. See also the Software Configuration chapter in this manual. For further information on the EEPROM refer also to the XICOR X25C02 data sheet.

2.7.3 Tick Generator

The MPC860T internal Periodic Interrupt Timer is used by the PEP supported real-time operating system as Tick generator.

For further information please refer also to the Motorola MPC860T User's Manual.

2.7.4 Bus Error Timer

The IUC860 provides an on-board bus error timer. An 128µs timeout timer monitors the cycle lengths of data transfers to and from locations beyond the CPU, including on-board I/O, CXC and SRAM. After a timeout occurs, it generates an on-board BERR signal for error termination. This timer is enabled/disabled via the BOARD_CON_STA_REG_1 register which also supplies a timeout status bit in order to identify bus errors generated by the on-board bus error timer.

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2.7.5 Watchdog Timer

A 512 ms watchdog timer triggers the on-board reset generator at timeout. Once enabled via the board control/status register, the watchdog timer cannot be reset by software. It must be re-triggered via the corresponding bit in the BOARD_CON_STA_REG_1 register periodically within the timeout period. 'Watchdog timer running' is a status that is displayed by the yellow front panel LED. At timeout the watchdog timer triggers the on-board system reset which also causes a reset to the CXC-bus.



Note...

The internal MPC860T watchdog timer is not used on the IUC860. Therefore, it should remain disabled (default setting).

2.7.6 Reset Sources

The IUC860 interacts with the following reset sources.

Table 2-8: IUC860 Reset Sources

MPC860T Reset Input	Reset Source
PORESET	Onboard Power Monitor Watchdog Front panel push button: RST Debug port (CON6, pin 2)

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2.8 Front Panel Functions

2.8.1 Reset/Abort

On the IUC860 front panel there are two push button switches for interacting with the system: RST for reset and AB for abort.

Pressing the RST button initiates an immediate hardware reset of the system.

During normal operation pressing the AB button causes a non-maskable interrupt (NMI) to be generated. Pressing the AB button during system startup when the green user LED (U) is blinking causes the bootstrap loader to enter interactive command mode. Commands can then be entered for processing by the bootstrap loader. Refer to chapter 5 for Bootstrap Loader information.

2.8.2 System Status Indicators

Six system status indicators divided into two groups of three LED's each are provided on the front panel of the IUC860. The first group (LED1) is dedicated to and controlled by the Ethernet interface whereas the second group (LED2) is application oriented. The table below provides an overview of the functionality associated with these indicators.

Table 2-9: System Status Indicators

G	FP DES.	COLOR	NAME	DESCRIPTION
LED1	ACT	GREEN	LED1AC	This LED indicates that data are being transmitted or received via the Ethernet link. It blinks when there is traffic on the link.
	LNK	GREEN	LED1LN	This LED indicates the integrity of the Ethernet link. When on the link is established in both directions.
	SPEED	GREEN	LED1SP	This LED indicates the data rate of the Ethernet link. When on the speed is 100 Mbps; off it is 10 Mbps.
LED2	U	GREEN	LED2G	This LED blinks during startup indicating that the system is being initialized (bootstrap loading in progress). After system initialization has been completed it is on steady and is available for use by the application program. Refer to chapter 4 (BOARD_CON_STA_REG_1 register) for setting of this LED.
	W	YELLOW	LED2Y	This LED is used to indicate the status of Watchdog Timer enabling. When on, the Watchdog Timer is enabled.
	H	RED	LED2R	This LED is available for general use and is application dependent. It is off if not used. Refer to chapter 4 (BOARD_CON_STA_REG_1register) for setting of this LED.

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2.9 RTC and SRAM Data Retention

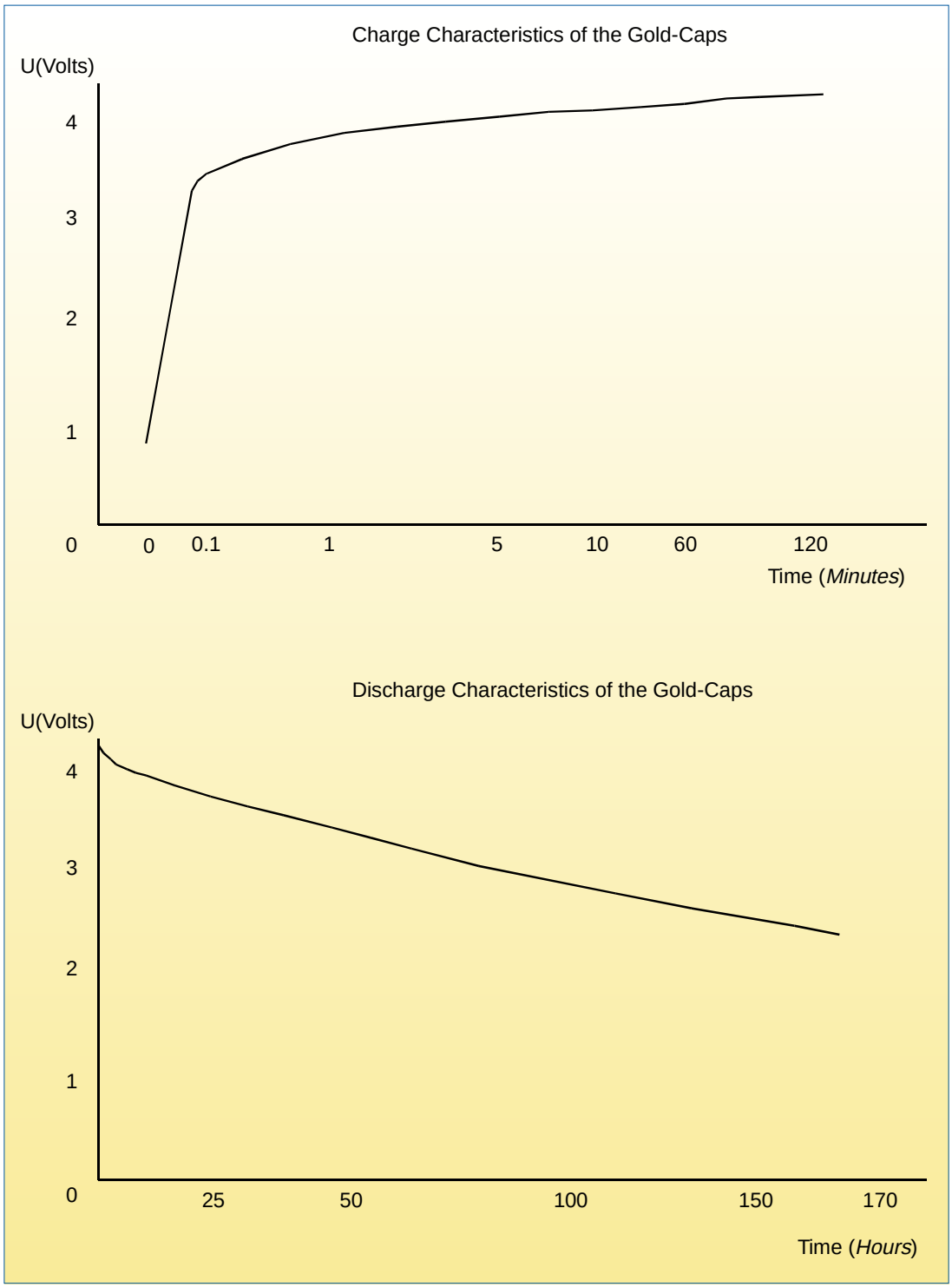
Short-term data retention for RTC and SRAM is gained with two Gold Caps, each with a value of 0.22 Farad. In contrast to Lithium cells, Gold Caps do not require servicing. This short-term backup is intended for short power failures or for reconfiguring systems. An empty Gold Cap needs approximately three hours to charge up, with backup times dependant on the temperature, memory size, and memory manufacturer tolerances. A well charged Gold Cap provides a minimum of 10 hours backup time.

Laboratory tests at *PEP* indicate a typical backup time of 1 week for 1MByte SRAM plus RTC (the typical on-board backup current is below 2µA). The charge and discharge behaviour of Gold Caps is documented on the following page.

For long-term data retention, 5V standby power supply could be provided via CXC pin A5 (user-defined line). This would require the setting of jumper J15 on the IUC860 board to 5V CXC backup and special wiring on the CXC backplane or a special CXC battery module.

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Figure 2-5: Gold-Cap Charge and Dischage Characteristics



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2.10 DEBUG Interface and Pinout

The MPC860T microprocessor has an integrated serial on-chip debug interface which is accessible on the IUC860 through a separate 10 pin connector pin row.

Figure 2-6: DEBUG Connector (CON6)

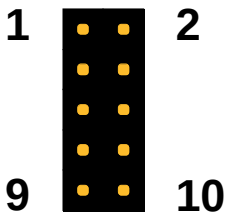


Table 2-10: DEBUG Connector (CON6) Pinout

SIGNAL	PIN	I / O	DESCRIPTION
VFLS0	1	O	MPC860 debug signal (visible history buffer flushes status)
RESETIN	2	I	Debug port reset input (leads to power on reset)
GND	3		
DSCK	4	I	Debug clock
GND	5		
VFLS1	6	O	MPC860 debug signal (visible history buffer flushes status)
RESETOUT	7	O	Debug port reset output (MPC860 is in reset state)
DSDI	8	I	Input serial data
VDD (3.3V)	9		
DSDO	10	O	Output serial data

2.11 JTAG/ISP Interface and Pinout

A JTAG/ISP interface is provided on the IUC860 for the manufacturer's use (logic programming, JTAG test).

Figure 2-7: JTAG Connector (CON5)

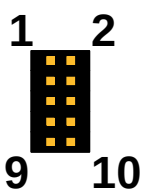


Table 2-11: JTAG Connector (CON5) Pinout

SIGNAL	PIN	PIN	SIGNAL
TCK	1	2	GND
TDO	3	4	VCC
TMS	5	6	GND
OE_CLKS	7	8	N/C
TDI	9	10	GND

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Chapter 3

Installation

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3. Installation

The IUC860 has been designed for easy installation. However, the following standard precautions and installation information/procedures must be observed to ensure proper installation and to preclude damage to the board or injury to personnel.

3.1 Hardware Installation

The board described in this manual can be installed in the system controller slot of any CXC or Enhanced CXC compatible computer. The board must be securely fastened to the chassis using the frontpanel retaining screws to avoid loosening of the board through vibration and to ensure proper grounding and operation of the board.



Caution, Electric Shock Hazard!

Switch off the (E)CXC system main power before installing the board. Ensure that there are no other external voltages being applied to system. Failure to comply with the above could endanger your life/health and may damage your board or system.



ESD Equipment!

Your (E)CXC board contains electrostatically sensitive devices. Please observe the necessary precautions to avoid damage to your board:

- Discharge your clothing before touching the assembly. Tools must be discharged before use.
- Do not touch components, connector pins, or conductive circuits.
- If working at an anti-static workbench with professional discharging equipment, please do not omit to use it.

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3.1.1 Installation/Removal Procedures

To install the board, please proceed as follows:

- Ensure that the safety requirements indicated above are observed.
- Ensure that the board is properly configured for operation before installing.



Warning!

Failure to comply with the above instruction could cause damage to the board or result in improper system operation. Please refer to chapter 4 for configuration information.

- Install the board in the appropriate slot and engage the retaining mechanism.
- Fasten the front panel retaining screws.
- Connect external interfacing cables to the board as required
- Ensure that the board and interfacing cables are properly secured.

To remove the board, please proceed as follows:

- Ensure that the safety requirements indicated above are observed.
- Disconnect any interfacing cables that may be connected to the board.
- Loosen the frontpanel retaining screws.
- Disengage the board retaining mechanism by pressing down on the board release handle disengaging the board from the backplane connector and pull the board out of the slot.

3.1.2 External Serial Interface Module

Being a combined system and serial communications controller board, the IUC860 is designed for a possible combined use together with the CXM-SIO3 external serial interface module. If such an interface module is used, all communication signals between the mainboard and the module are transmitted via the (E)CXC bus. For this purpose, the external interface module must be located in the next slot to the right of the IUC860.

3.2 Software Installation

Software installation is a function of the Bootstrap Loader and is described in chapter 5 of this manual.

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Chapter 4

Configuration

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4. Configuration

The following chapters provide information for configuring the IUC860 board jumpers and register addressing and usage.

4.1 Jumper Settings

Prior to installation of the IUC860 the board jumpers must be configured appropriately to ensure proper operation of the board. Two jumpers, J1 and J2, are wire bridge type jumpers, whereas the remaining jumpers, J3 to J16, are solder or 0 ohm resistor type jumpers. Please refer to Figures 1-3 and 1-4 in chapter 1 for the location of the jumpers on the board.

4.1.1 Overview

The following table provides an overview of the IUC860 jumpers including a short description of the default settings.

Table 4-1: IUC860 Jumper Settings Overview

JUMPER	FUNCTION	DEFAULT SETTING	SETTING DESCRIPTION
J1	(E)CXC mode select	open	CXC mode selected
J2	Boot device select	set	Boot from Flash on DM60x memory PB
J3	EEPROM write protection	open	Serial EEPROM not write protected
J4	SRAM size select	1 - 2	1 MByte of SRAM
J5	SRAM size select	1 - 2	1 MByte of SRAM
J6	SRAM data retention	1 - 3	Data retention on
J7	CPU clock speed select	open	Depends on processor type used
J8	CPU clock speed select	open	Depends on processor type used
J9	Baud rate clock	1 - 2	1.843 MHz clock connected to pin PA6 of the MPC860T
J10	CPU clock speed select	set	Depends on processor type used
J11	Installed ROM configuration	open	Depends on the ROM device installed
J12	Installed ROM configuration	open	Depends on the ROM device installed
J13	Layer bridge	set	Factory set, do not change
J14	24 MHz clock	1 - 2	24 MHz clock connected to pin PA2 of MPC860T
J15	CXC pin A5 use select	1 - 3	MPC860T pin PB14 connected to CXC pin A5
J16	Layer bridge	set	Factory set, do no change
C1	Connection of signal ground to chassis (ground)	open	Signal ground disconnected from chassis (ground)

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4.1.2 J1 - (E)CXC Mode Select

The purpose of the J1 jumper is to select either CXC mode or ECXC mode operation.

Table 4-2: J1 - (E)CXC Mode Select

JUMPER	SETTING	DESCRIPTION
J1	open	CXC mode operation enabled
	set	ECXC mode operation enabled

4.1.3 J2 - Boot Device Select

The purpose of the J2 jumper is to select the memory position from which the IUC860 fetches its boot code. It establishes the address location of the DM60x memory module Flash window and the memory expansion socket EPROM/Flash memory if installed.

Table 4-3: J2 - Boot Device Select

JUMPER	SETTING	DESCRIPTION
J2	open	IUC860 fetches boot code from memory expansion socket EPROM or Flash memory
	set	IUC860 fetches boot code from DM60x memory module Flash memory

4.1.4 J3 - EEPROM Write Protection

The purpose of the J3 jumper is to provide write protection for the serial EEPROM if required.

Table 4-4: J3 - EEPROM Write Protection

JUMPER	SETTING	DESCRIPTION
J3	open	Serial EEPROM not write protected
	set	Serial EEPROM write protected

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4.1.5 J4 and J5 - SRAM Size Select

The purpose of the J4 and J5 jumpers is to indicate the amount of SRAM installed on the IUC860 board. Both jumpers are required to be set together to properly indicate the amount of SRAM installed.

Table 4-5: J4 and J5 - SRAM Size Select

JUMPER	SETTING	DESCRIPTION
J4	1 - 2	1 MByte SRAM installed
	1 - 3	reserved
J5	1 - 2	1 MByte SRAM installed
	1 - 3	reserved

4.1.6 J6 - SRAM Data Retention

The purpose of the J6 jumper is to provide the ability to retain SRAM data if required.

Table 4-6: J6 - SRAM Data Retention

JUMPER	SETTING	DESCRIPTION
J6	1 - 2	SRAM data retention off
	1 - 3	SRAM data retention on

4.1.7 J7, J8, and J10 - CPU Clock Speed Select

The purpose of the J7, J8, and J10 jumpers is to select the CPU clock speed. As there is currently only one clock speed available, these jumpers are factory configured and may not be changed.

Table 4-7: J7, J8, and J10 - CPU Clock Speed Select

JUMPER	SETTING	DESCRIPTION
J7	open	Factory setting, do not change
	-	-
J8	open	Factory setting, do not change
	-	-
J10	-	-
	set	Factory setting, do not change

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4.1.8 J9 - Baud Rate Clock

The purpose of the J9 jumper is to select the source and frequency of the baud rate clock.

Table 4-8: J9 - Baud Rate Clock

JUMPER	SETTING	DESCRIPTION
J9	1 - 2	1.843 MHz clock connected to pin PA6 of the MPC860T
	1 - 3	CXC SER1RCLK connected to MPC860T PA6 pin

4.1.9 J11 and J12 - Installed ROM Configuration

The purpose of the J11 and J12 jumpers is to configure the IUC860 board with respect to the type of memory device installed in the memory expansion socket. If a memory device is installed, care must be taken to ensure the proper setting of jumpers J11 and J12 otherwise improper operation of the IUC860 may result. The J11/J12 jumpers are set to open/open at the factory if no memory device is installed. This is also the default setting.

Table 4-9: J11 and J12 - ROM Type and Size Select

SETTING		DESCRIPTION			
J11	J12	DEVICE	SPEED	ORG.	SIZE
open	open	EPROM 27C010	120 ns	128k x 8	128 kByte
open	open	EPROM 27C020	120 ns	256k x 8	256 kByte
open	1 - 3	EPROM 27C040	120 ns	512k x 8	512 kByte
1 - 2	1 - 3	EPROM 27C080	120 ns	1M x 8	1 MByte
open	open	FLASH 28F010 (read only)	120 ns	128k x 8	128 kByte
open	open	FLASH 28F020 (read only)	120 ns	256k x 8	256 kByte
open	1 - 2	FLASH 29F010 (read &write)	120 ns	128k x 8	128 kByte
1 - 3	1 - 2	FLASH 29F040 (read & write)	120 ns	512k x 8	512 kByte

4.1.10 J13 and J16 - Layer Bridge

The purpose of the J13 and J16 jumpers is to bridge layers in the IUC860 board. They are set at the factory and may not be changed.

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4.1.11 J14 - 24 MHz Clock

The purpose of the J14 jumper is to connect the 24 MHz clock to pin PA2 of the MPC860T.

Table 4-10: J14 - 24 MHz Clock

JUMPER	SETTING	DESCRIPTION
J14	1 - 2	24 MHz clock connected to pin PA2 of the MPC860T
	1 - 3	CXC SER2RCLK connected to MPC860T PA2 pin

4.1.12 J15 - CXC Pin A5 Use Select

The purpose of the J15 jumper is to select the usage of pin A5 of the CXC backplane.

Table 4-11: J15 - CXC Pin A5 Use Select

JUMPER	SETTING	DESCRIPTION
J15	1 - 2	+5VSTDBY connected to CXC pin A5
	1 - 3	MPC860T pin PB14 connected to CXC pin A5

4.1.13 C1 - Signal Ground Connection to Chassis (Ground)

The purpose of the C1 pads is to allow for various signal ground to chassis (ground) connections to satisfy different EMC/EMI requirements.

Table 4-12: C1 - Signal Ground Connection to Chassis (Ground)

JUMPER	SETTING	DESCRIPTION
C1	open	Signal ground disconnected from chassis (ground)
	set (wire bridge)	Signal ground connected directly to chassis (ground)
	set (capacitor)	Capacitive connection of signal ground to chassis (ground) through the use of a special high voltage capacitor

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4.2 Board Address Map

The following table and figure illustrate the address mapping of the IUC860. Whereas the table provides a detailed description, the figure provides an overall view of the mapping. The address map depends on the configuration of the IUC860 memory expansion socket and the requirements of the application.

Table 4-13: IUC860 Board Address Map

ADDRESS RANGE		MPC-860T CHIP SEL	AREA NAME	SIZE	DESCRIPTION
FROM	TO				
0x0000 0000	0x3FFF FFFF	CS2	DRAM	1 GB	Main memory (DM60x Module)
0x4000 0000	0x7FFF FFFF	CS1	reserved	1 GB	
0x8000 0000	0x89FF FFFF	CS4	reserved	160 MB	
0x8A00 0000	0x8AFF FFFF	CS4	RTC	16 MB	Realtime clock
0x8B00 0000	0x8BFF FFFF	CS4	BCS-REG	16 MB	Board control/status registers
0x8C00 0000	0x8FFF FFFF	CS4	reserved	64 MB	
0x9000 0000	0x9FFF FFFF	CS0	**J2 open** / SOCKET **J2 set** / DM60x	256 MB	Boot area
0xA000 0000	0xAFFF FFFF	CS3	**J2 open** / DM60x **J2 set** / SOCKET	256 MB	Additional memory area
0xB000 0000	0xB7FF FFFF	CS5	(E)CXC	128 MB	(E)CXC memory area
0xB800 0000	0xB8FF FFFF	CS7	SRAM	16 MB	SRAM memory area
0xB900 0000	0xBBFF FFFF		reserved	48 MB	
0xBC00 0000	0xBCFF FFFF	CS6	reserved	16 MB	
0xBD00 0000	0xBD00 FFFF		IMP (MPC-REG)	64 kB	IMMR register, 64 kBytes resolution
0xBD01 0000	0xBFFF FFFF		reserved	48 MB	
0xC000 0000	0xFFFF FFFF	CS1	reserved	1 GB	

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Figure 4-1: IUC860 Board Address Map

0xFFFF FFFF 0xC000 0000	CS1	reserved	1 GB
0xBD01 0000		reserved	48 MB
0xBD00 0000		**IMP**	64 kB
0xBC00 0000	CS6	reserved	16 MB
0xB900 0000		reserved	48 MB
0xB800 0000	CS7	**SRAM**	16 MB
0xB000 0000	CS5	**(E)CXC**	128 MB
0xA000 0000	CS3	**ADD MEM**	256 MB
0x9000 0000	CS0	**BOOT**	256 MB
0x8C00 0000	CS4	reserved	64 MB
0x8B00 0000	CS4	**BCS-REG**	16 MB
0x8A00 0000	CS4	**RTC**	16 MB
0x8000 0000	CS4	reserved	160 MB
0x4000 0000	CS1	reserved	1 GB
0x0000 0000	CS2	**DRAM**	1 GB

	J2 OPEN	J2 SET
	DM60x	**SOCKET**
	SOCKET	**DM60x**

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4.3 Board Registers

The IUC860 has two board registers available to the user which provide status information for controlling the operation of the board. The following chapters provide a basic overview of the registers. For more about the details of their functioning please refer to chapter 2.

4.3.1 Overview

The board registers may be accessed through byte-wide read and write operations to the address space 0x8B00 000x.

Table 4-14: Board Registers

REGISTER	ADDRESS	ACCESS	
		READ	WRITE
BOARD_CON_STA_REG1	0x8B00 0007	X	X
BOARD_CON_STA_REG2	0x8B00 0009	X	X (not all bits)

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4.3.2 BOARD_CON_STA_REG_1 Register

The BOARD_CON_STA_REG1 is a multi-purpose register which allows access to various on-board functions.

Table 4-15: BOARD_CON_STA_REG_1 Register

REGISTER NAME		BOARD_CON_STA_REG1						ACCESS	
ADDRESS		0x8B00 0007						R	W
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		res.	res.	BERRB	EN_ WDG	TR_ WDG	EN_ BERRB	LED_R	LED_G
DEFAULT		0	0	0	0	1	1	0	1
BIT	**NAME**	**VAL**	**DESCRIPTION**						
0	LED_G	0	Used to switch off the green general purpose front panel LED						
		1	Used to switch on the green general purpose front panel LED						
1	LED_R	0	Used to switch off the red general purpose front panel LED						
		1	Used to switch on the red general purpose front panel LED						
2	EN_ BERRB	0	Used to disable the on-board bus error timer						
		1	Used to enable the on-board bus error timer						
3	TR_ WDG	0	Used to indicate that the watchdog timer has not been re-triggered						
		1	Used to re-trigger the watchdog timer						
4	EN_ WDG	0	Used to indicate that the watchdog timer has not been enabled						
		1	Used to enable the watchdog timer						
5	BERRB	0	Used to indicate that the on-board bus error timer has not timed out						
		1	Used to indicate that the on-board bus error timer has timed out						
6		0	reserved						
		1	reserved						
7		0	reserved						
		1	reserved						

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4.3.3 BOARD_CON_STA_REG_2 Register

The BOARD_CON_STA_REG2 is a seond multi-purpose register which allows access to various on-board functions.

Table 4-16: BOARD_CON_STA_REG_2 Register

REGISTER NAME		BOARD_CON_STA_REG2						ACCESS	
ADDRESS		0x8B00 0009						R	W (bits 4, 5, 6 read only)
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		RMW	ECXC	CPUSP1	CPUSP0	res.	res.	res.	res.
DEFAULT		0	0	1	1	0	0	0	0
BIT	**NAME**	**VAL**	**DESCRIPTION**						
0		0	reserved						
		1							
1		0	reserved						
		1							
2		0	reserved						
		1							
3		0	reserved						
		1							
4	CPUSP0	0	Settings: Bit 5 Bit 4 1 1 40 MHz bus clock (80 MHz CPU clock) (This is the only valid setting for these bits.)						
		1							
5	CPUSP1	0							
		1							
6	ECXC	0	Used to indicate that the CXC bus protocol is being used						
		1	Used to indicate that the enhanced CXC ((E)CXC) bus protocol is being used						
7	RMW	0	Used to indicate normal read or write cycles						
		1	Used to generate an unsplittable read modify write (RMW) cycle						

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4.4 EEPROM

Access to the EEPROM is effected via the serial peripheral interface (SPI) of the MPC860T. Write protection however is achieved by installing jumper J3. For usage/configuration of the EEPROM refer to the documentation supplied with the board support package (BSP).

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Chapter 5

Bootstrap Loader

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5. Bootstrap Loader

5.1 Introduction

This manual contains a description of the Bootstrap Loader Software Package for the IUC860 and the VSBC-860.

The Bootstrap Loader is a stand-alone software located in the FLASH memory which allows the user to safely update the contents of the FLASH and delay the boot process for a specified time.

The Bootstrap Loader has the capability of programming FLASH memory from “MOTOROLA S-RECORDS” or from an absolute memory address. If the programmed image does not work, the Bootstrap Loader can be re-entered. The memory contents can be examined and another programming cycle initiated.

The Bootstrap Loader is delivered already installed in DM60x memory piggybacks.

Please read this user manual before reprogramming any FLASH memory.



Warning!

When programming FLASH memory, do not press the RESET button or switch off the mains power under any circumstances! Doing so may damage the Bootstrap Loader and would consequently leave the board unusable due to corrupt FLASH contents.

However, the ABORT button may be used to cancel a running operation safely.

5.2 Start-Up

After system reset, the Bootstrap Loader is started. It searches the FLASH memory area for a valid start key. If this start key is found, the Bootstrap Loader checks the 'BootWaitTime' from serial EEPROM. If the entry is valid, the continuation of the boot process is delayed for a period while the green front panel LED flashes to indicate that the system is alive but waiting for continuation. If the entry is not valid, a default of 5 seconds is used. After the BootWaitTime has passed, the program in FLASH is started.

The Bootstrap Loader has two modes of operation: non-interactive start mode as described above and the interactive command mode.

For normal board operation, only the non-interactive start mode is used to start a program in FLASH. This is done automatically without any user interaction. The interactive command mode is used to re-program the FLASH memory contents or change the BootWaitTime.

The serial term port operates at 9600 Baud, 8 bits / character, 1 stop bit and no parity.

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5.3 Entering the Command Mode

There are two possible reasons for entering the Bootstrap Loader command mode:

- If no valid start key is found the Bootstrap Loader command mode is entered automatically.
- If the user wants to enter the Bootstrap Loader manually, e.g. for re-programming the FLASH contents the ABORT button on the front panel must be used.



Note...

The ABORT button must not be pushed until the green LED appears, because this button generates an NMI, and the exception vector tables must be initialized correctly to serve this NMI.

However, the ABORT button must be pushed before the green LED stops flashing (BootWaitTime), since the system control is transferred to the downloaded binary image afterwards. The LED is cycled every 0.25 sec. so if 1 second is specified as BootWaitTime, the LED will only flash twice.

While in Command mode, CTRL-x deletes the complete input line and CTRL-a restores the last input line.

5.4 Programming a New Binary Image to FLASH Memory

5.4.1 Preparing the Image

The image must be compiled / linked to run from the FLASH base address 0x90000000 of the CPU. The image must contain executable PPC code at offset 0x100, as is usual for ROM/FLASH images.

A binary image must be converted to Motorola S-records or loaded to a CXM memory board with battery backup, FLASH or EPROM population.

5.4.2 Programming with Motorola S-Records

Programming is done with the *If* command.

The *If* command accepts S1, S2 and S3 records. Operation is terminated by the appropriate S9, S8 or S7 record. Other types of records are ignored.

The checksum of every record except end records is checked. Bad records are rejected by the Bootstrap Loader. The address range of every record is also checked; records that try to overwrite the Bootstrap Loader are rejected. Additionally, every record must match the programmable area exactly. To give the user an overview of the available ranges, the start-up banner includes address information.

If S1 or S2 record input is preferred, please note that these records only include 16 and 24-bit wide addresses. Therefore, in order to reach the FLASH area an address offset

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must be specified using the '-o=...' option of the *If* command. Additionally, it must be ensured that the code is not larger than the covered address range.



Note...

The 'If' command cannot be used to program Motorola S-records to RAM areas.

For sending programming data, the lower *(term)* or upper *(ser0)* front panel connectors can be used. The *ser0* port is preferable, because in this configuration it is possible to monitor the progress of the operation via the *term* port. In any case, the user LED flashes slowly while downloading to give feedback of the usual kind.

If not specified otherwise, sectors which are not touched by the programming operation are not erased. If you want to erase all sectors while programming, the '-c' option can be specified along with the *If* command. This is useful for software which searches memory during start-up and should not find any old modules, for example OS-9.

Make sure that the XON/XOFF protocol is used on the host side. This is a fixed setting and cannot be changed. Additionally, make sure that your host does not stop transmission after a number of lines (e.g. OS-9: use the 'nopause' attribute).

Serial parameters can be modified with the *pf* command.

5.4.3 Example Using OS-9 Development System

The host is assumed to be an OS-9 development system. A serial cable is used to connect the *ser0* port of the board to be programmed to the *t0* port of the development system. Additionally, we assume that we want to program a VxWorks bootrom image which is available as a file *'bootrom'* in a binary image format. The serial connection should run at 38400 Baud. The following steps must be performed:

Host

```
xmode /t0 baud=38400 nopause
iniz /t0
```

Target

```
pf ser0 38400
lf -u
```

Host

```
binex -s3 -a=90000000 bootrom >/t0
```

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5.5 Monitoring the Programming Progress

The programming can be monitored via the *term* port. The characters which are displayed have the following meaning:

- r Read S-record; valid and in range
- t Protected sector touched
- e Erase sector
- c Copy to buffer, program later
- p Program record

None of the above characters indicate an error. The first sector (which includes the first instruction to be executed) and the last sector (which includes the Bootstrap Loader itself) are protected. These sectors are not immediately programmed like the other sectors. The contents of these protected sectors are buffered in RAM and programmed at the end of the operation. This is done to limit the amount of time the Bootstrap Loader itself is not in FLASH or not startable, because if the Bootstrap Loader crashes during this critical period of time, it will not start again afterwards.



Warning!

When programming FLASH memory, please do not press the RESET button or switch off the mains power in any case! Doing so may damage the Bootstrap Loader and would consequently leave the board unusable due to corrupt FLASH contents.

However, the ABORT button may be used to cancel a running operation safely.

The parameter '-q' suppresses all messages and warnings except error messages.

Programming via the *term* port is also supported, but in this case programming of the loader is quiet by default. The propagation of the process cannot be monitored directly, since only the screen LED flashes while programming is in progress.

It is recommended that as a default the programming via the *ser0* port should be used.



Note...

If the process must be aborted, press the ABORT button and try again.

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5.6 Programming from an Absolute Address

The second way to program FLASH memory is to program it from an absolute address. The image to be programmed must be located in a visible address range, for example on the CXCbus. A memory card with battery-backup, FLASH or EPROM can be used to hold the image to program. If we assume that the image is located at 0x87000000 and is 0x123456 bytes large we must type the following at the command prompt of the Bootstrap Loader:

```
lf -m=87000000 -l=123456
```

The characters which are now displayed have the same meaning as if we are programming from S-records, but the time needed for each step to be completed may be longer because the loader tries to program with the largest possible block size that it can manage.

Again, '-c' can be used to clear untouched sectors.



Note...

Quiet operation is not supported, and also it is not possible to specify any offset.

Please note also that programming cannot be canceled with ABORT.

5.7 Boot Wait Time

The command *bw* can be used to display/change the current boot wait time. Available delays are 1-2-5-10-20-50 seconds.

The BootWaitTime is stored in the boot section of the serial EEPROM. This section is validated with a CRC code to avoid the setting of random parameters.



Note...

If the CRC of the Boot section is not valid, changing the BootWaitTime has no effect because the bw command does not validate an invalid CRC in order to avoid undesired side effects. In this case, a default timing of 5 seconds is always used.

To validate an invalid CRC, the appropriate utility from an operating system must be used or, alternatively, the line *bw -f* must be issued.



Note...

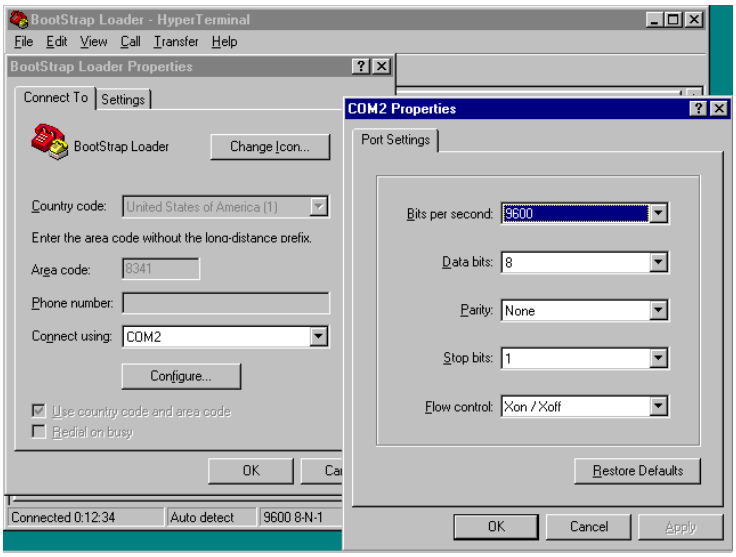
Please note that validation with the 'bw -f' command may validate invalid entries, thus causing undesired effects.

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5.8 Example Using Hyperterminal under Windows 95/Windows NT

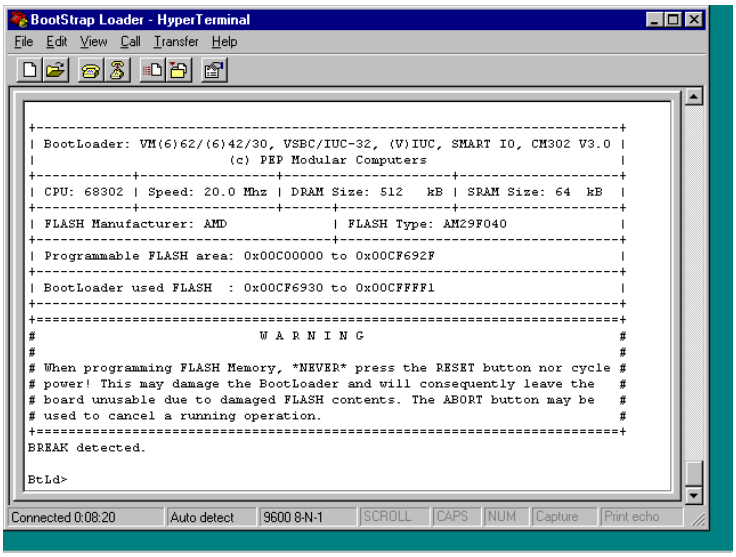
The host is assumed to be a PC with Windows 95 or Windows NT. A serial cable is used to connect the term port of the board to be programmed to COM2 of the PC. Additionally, we assume that we want to program a MOTOROLA S-record built for the FLASH address of the board. The serial connection runs at the default configuration of 9600 Baud with no parity and one stop bit. The properties should look like the following:

Figure 5-1: Setting of COM2 Properties



After entering the Command Mode the following screen should appear:

Figure 5-2: Screen after Entering the Command Mode



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Enter 'lf' on the target. The target now waits until the MOTOROLA S-records have been transferred over the term. Select **Transfer/Send Text File** dialogue box and select the file containing the MOTOROLA S-records.

Figure 5-3: Select Transfer/Send Text File Dialogue Box

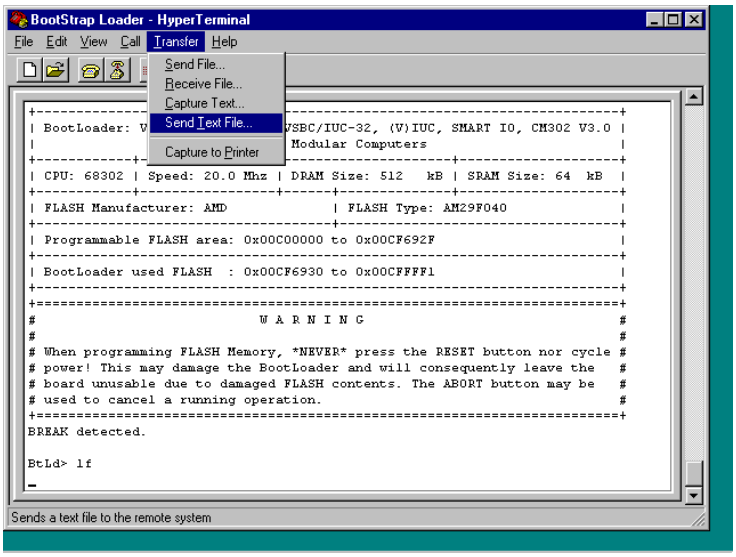
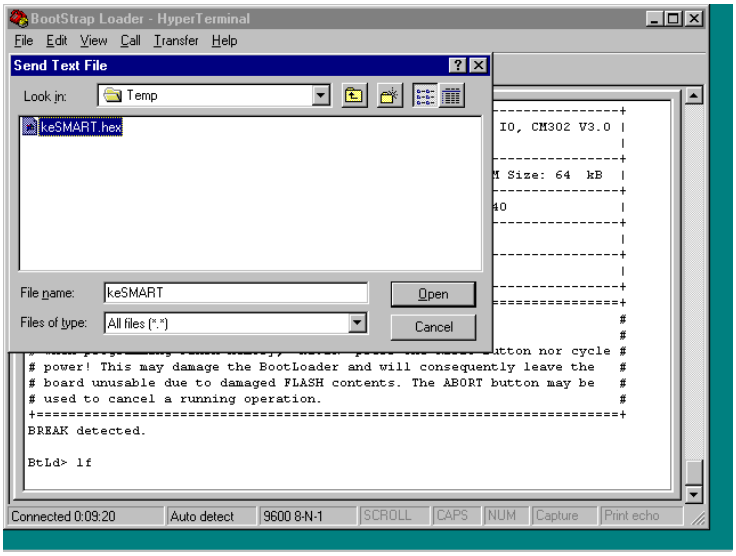


Figure 5-4: Selecting the MOTOROLA S-Records File



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After selecting **Open** the dialogue box disappears and the MOTOROLA S-records are transferred. As soon as the complete file is sent, the prompt of the Bootstrap Loader appears again.



Note...

No status information is displayed.

5.9 Command Reference

5.9.1 Boot Wait

Syntax

```
bw [<time>| -f]
```

Description

Without parameters, *bw* displays the current setting.

The parameter <time> may be set to 1, 2, 5, 10, 20 and 50, which signify the waiting time in seconds. No values other than these are supported, while the option '-f' has the following meaning:

- '-f' force CRC update.

5.9.2 Load Flash

Syntax

```
If [-o[=]<offset>] [-u] [-q] [-c] [-m[=]<adr> -l[=]<len>]
```

Description

Without parameters, the FLASH is loaded using S-records via the *term* port.

The parameter '<offset>' is a signed 32 bit offset which is added to every record and can be used to move the S-records to the FLASH position.



Note...

This option must always be used if the S1 or S2 records are used.

- '-u' must be used to download over *ser0.*
- '-q' suppresses all messages except error messages.
- '-c' clears all untouched sectors and leaves no old code fragments.

For a Load Flash from an absolute address, the -m / -l options must be used.

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5.9.3 Memory Display

Syntax

```
md [<adr>]
```

Description

Without parameters specified, the FLASH contents starting at the beginning of the programmable FLASH area are displayed. This function is not limited to FLASH and other address ranges can be specified.



Note...

The first instruction to be executed in FLASH is not identical to the one to be executed first from the programming source (S-records memory block).

5.9.4 Port Format

Syntax

```
pf [<port> [<baud>][/[<bitschar>][/[<parity>][/<stops>]]]]
```

Description

Without parameters specified, the current serial port settings are displayed.

- <port> specifies the serial port. Valid values are *term* or *ser0.*
- <baud> specifies the baud rate. The values 50, 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 7200, 9600, 19200, 38400 and 115200 Baud can be specified.
- <bitschar> specifies the bits / character. Valid values are 7 or 8.
- <parity> specifies if parity should be checked / generated. The value n specifies none, o for odd and e for even parity.
- <stops> specifies the stopbits which will be generated. Valid values are 1 or 2



Note..

No spaces are permitted between the options. Options must be separated with a slash. Not all options must be specified, but the '/' characters must be present to distinguish the different options from each other. The sequence can be aborted after every option.

Examples

Setting *term* to 300 Baud, 7 Bits/char, odd parity and 2 stopbits:

```
pf term 300/7/o/2
```

Set the bits / character field to 7 for *ser0* only:

```
pf ser0 /7
```

Set the stopbits field to 2 for *ser0*:

```
pf ser0 ///2
```


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5.9.5 Reset System

Syntax

`rs`

Description

This command exits the Bootstrap Loader and resets the system. It terminates the Bootstrap Loader command mode and resets the complete system, generating a system reset with the on-board watchdog.

5.9.6 Help

Syntax

`?` or `help`

Description

This command prints the online help page. The display of the help text varies between the different CPUs reflecting the difference of the CPUs.

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Appendix A

Memory Piggybacks

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A. Memory Piggybacks

A.1 General

The Memory Piggybacks described herein provide main memory capability for the storage of progam code and data either in DRAM or flash memory. Various configurations of DRAM and flash memory as indicated in the table below are available for a wide variety of PEP CPU boards. All configurations have 32-bit access and a maximum address range of 64 MB. In addition jumpers are available for providing write protection.

Table A-1: Memory Piggyback Types and Configurations

Type	Memory Configuration	
	DRAM	FLASH
DM600	4 MB	1 MB
		2 MB
		4 MB
DM601	16 MB	1 MB
		2 MB
		4 MB
DM602	1 MB	0 MB
		1 MB
		2 MB
DM603	32 MB	512 KB
		2 MB
		4 MB
DM604	8 MB	2 MB
		4 MB
DM605	64 MB	1 MB
		2 MB
		4 MB

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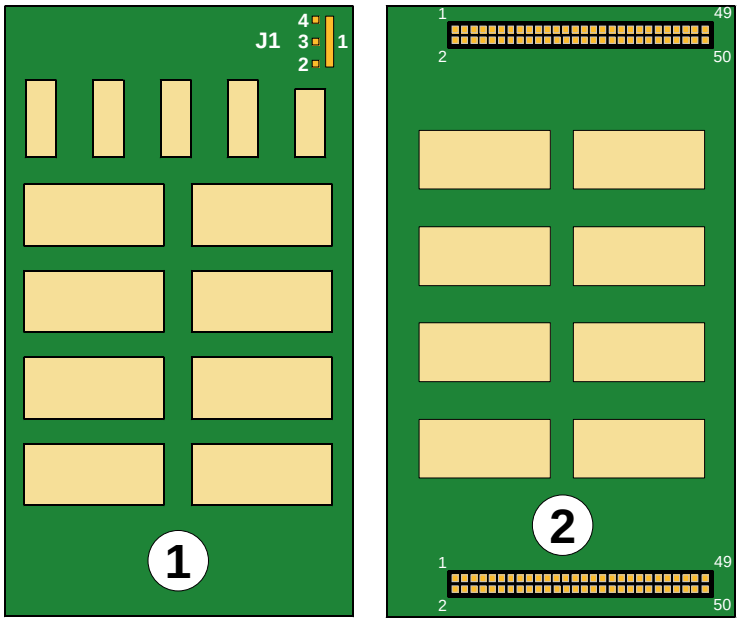
A.2 DM600

The DM600 is a memory piggyback fitted with:

- DRAM: 4 MB
- Flash Memory: 1, 2, or 4 MB

A.2.1 Board Layout and Jumper Location

Figure A-1: DM600 Memory Piggyback



Legend:

1. Flash Memory
2. DRAM

A.2.2 Jumper Description and Flash Addresses

Table A-2: Jumper: J1 Settings and Flash Memory Address Ranges

Setting	Description	1MB Flash	2MB Flash	4MB Flash
Open	All flash EPROM's write protected			
1 - 2	*No Protection*			
1 - 3	Flash Bank 1: Write protected Flash Bank 1: Address Range	Upper 512 KB 0x(9/A)0080000 - 0x(9/A)00FFFFF		Upper 2 MB 0x(9/A)0200000 - 0x(9/A)03FFFFF
1 - 4	Flash Bank 0: Write protected Flash Bank 0: Address Range	Lower 512 KB 0x(9/A)0000000 - 0x(9/A)007FFFF	 0x(9/A)0000000 - 0x(9/A)01FFFFF	Lower 2 MB 0x(9/A)0000000 - 0x(9/A)01FFFFF

Default settings are in italics.

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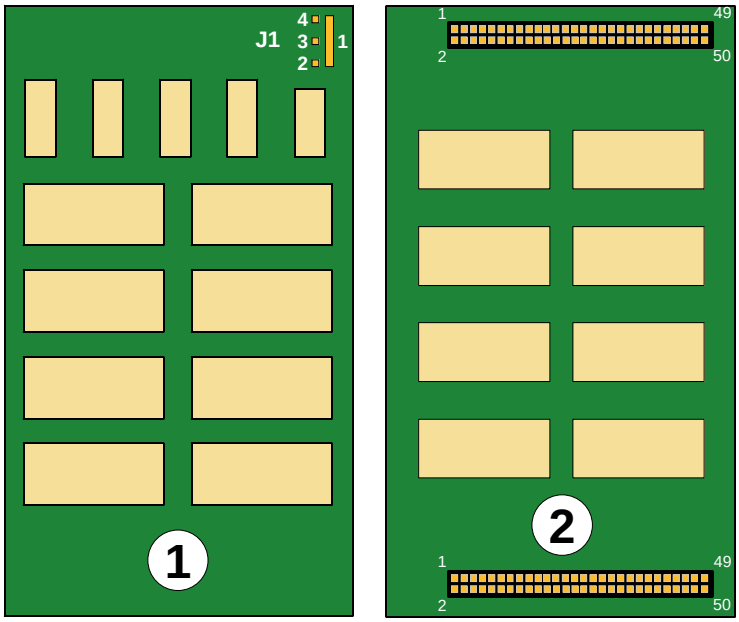
A.3 DM601

The DM601 is a memory piggyback fitted with:

- DRAM: 16 MB
- Flash Memory: 1, 2, or 4 MB

A.3.1 Board Layout and Jumper Location

Figure A-2: DM601 Memory Piggyback



Legend:

1. Flash Memory
2. DRAM

A.3.2 Jumper Description and Flash Addresses

Table A-3: Jumper: J1 Settings and Flash Memory Address Ranges

Setting	Description	1MB Flash	2MB Flash	4MB Flash
Open	All flash EPROM's write protected			
1 - 2	*No Protection*			
1 - 3	Flash Bank 1: Write protected Flash Bank 1: Address Range	Upper 512 KB 0x(9/A)0080000 - 0x(9/A)00FFFFF		Upper 2 MB 0x(9/A)0200000 - 0x(9/A)03FFFFF
1 - 4	Flash Bank 0: Write protected Flash Bank 0: Address Range	Lower 512 KB 0x(9/A)0000000 - 0x(9/A)007FFFF	 0x(9/A)0000000 - 0x(9/A)01FFFFF	Lower 2 MB 0x(9/A)0000000 - 0x(9/A)01FFFFF

Default settings are in italics.

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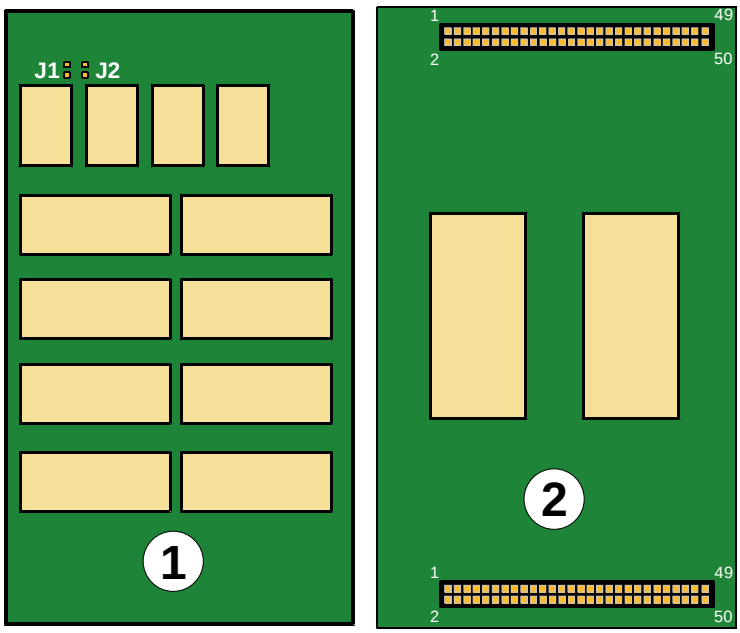
A.4 DM602

The DM602 is a memory piggyback fitted with:

- DRAM: 1 MB
- Flash Memory: 0, 1, or 2 MB

A.4.1 Board Layout and Jumper Location

Figure A-3: DM602 Memory Piggyback



Legend:

1. Flash Memory
2. DRAM

A.4.2 Jumper Description and Flash Addresses

Table A-4: Jumpers: J1 and J2 Settings and Flash Memory Address Ranges

Setting		Description	1MB Flash	2MB Flash
J1	*Set*	*No Protection*		
	Open	Flash Bank 1: Write protected Flash Bank 1: Address Range	Upper 512 KB 0x(9/A)0080000 - 0x(9/A)00FFFFF	
J2	*Set*	*No Protection*		
	Open	Flash Bank 0: Write protected Flash Bank 0: Address Range	Lower 512 KB 0x(9/A)0000000 - 0x(9/A)007FFFF	0x(9/A)0000000 - 0x(9/A)01FFFFF

Default settings are in italics.

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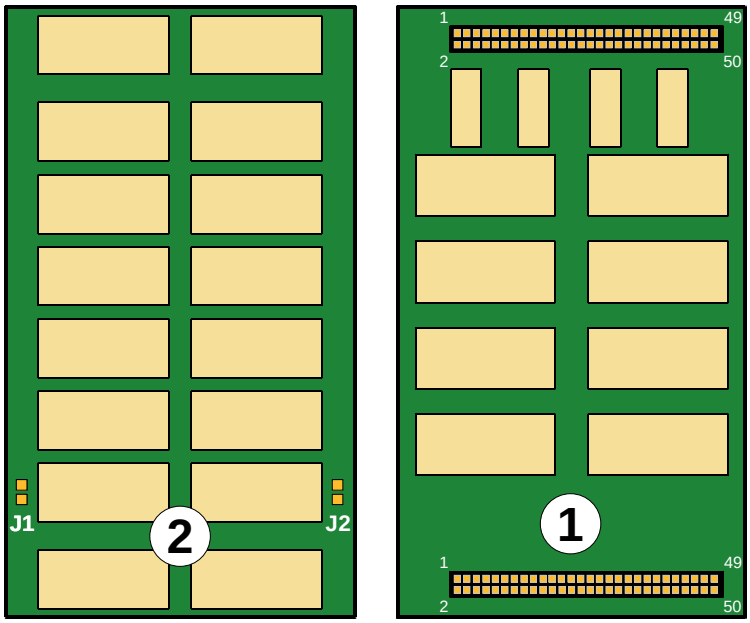
A.5 DM603

The DM603 is a memory piggyback fitted with:

- DRAM: 32 MB
- FLASH MEMORY: 0.5 (512 KB), 2, or 4 MB

A.5.1 Board Layout and Jumper Location

Figure A-4: DM603 Memory Piggyback



Legend:

1. Flash Memory
2. DRAM

A.5.2 Jumper Description and Flash Addresses

Table A-5: Jumpers: J1 and J2 Settings and Flash Memory Address Ranges

Setting		Description	512KB Flash	2MB Flash	4MB Flash
J1	*Set*	*No Protection*			
	Open	Flash Bank 0: Write protected			Lower 2 MB
		Flash Bank 0: Address Range	0x(9/A)0000000 - 0x(9/A)007FFFF	0x(9/A)0000000 - 0x(9/A)01FFFFF	0x(9/A)0000000 - 0x(9/A)01FFFFF
J2	*Set*	*No Protection*			
	Open	Flash Bank 1: Write protected			Upper 2 MB
		Flash Bank 1: Address Range			0x(9/A)0200000 - 0x(9/A)03FFFFF

Default settings are in italics.

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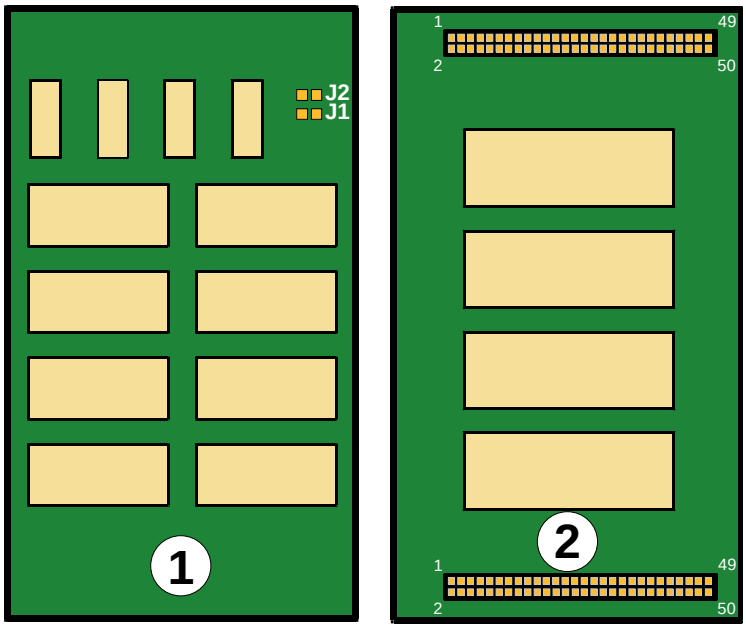
A.6 DM604

The DM604 is a memory piggyback fitted with:

- DRAM: 8 MB
- FLASH MEMORY:2 or 4 MB

A.6.1 Board Layout and Jumper Location

Figure A-5:DM604 Memory Piggyback



Legend:

1. Flash Memory
2. DRAM

A.6.2 Jumper Description and Flash Addresses

Table A-6: Jumpers: J1 and J2 Settings and Flash Memory Address Ranges

Setting		Description	2MB Flash	4MB Flash
J1	*Set*	*No Protection*		
	Open	Flash Bank 0: Write protected		Lower 2 MB
		Flash Bank 0: Address Range	0x(9/A)0000000 - 0x(9/A)01FFFFF	0x(9/A)0000000 - 0x(9/A)01FFFFF
J2	*Set*	*No Protection*		
	Open	Flash Bank 1: Write protected		Upper 2 MB
		Flash Bank 1: Address Range		0x(9/A)0200000 - 0x(9/A)03FFFFF

Default settings are in italics.

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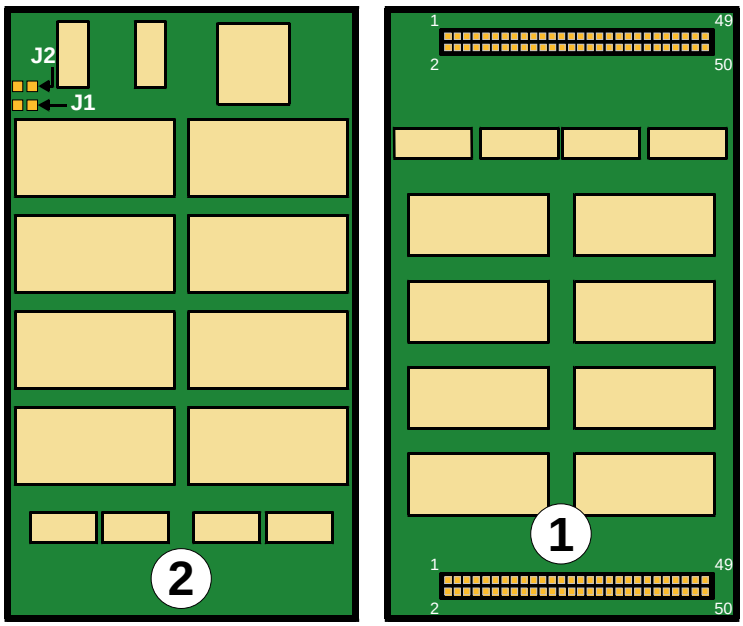
A.7 DM605

The DM605 is a memory piggyback fitted with:

- DRAM: 64 MB
- FLASH MEMORY:1, 2, or 4 MB

A.7.1 Board Layout and Jumper Location

Figure A-6: DM605 Memory Piggyback



Legend:

1. Flash Memory
2. DRAM

A.7.2 Jumper Description and Flash Addresses

Table A-7: Jumpers: J1 and J2 Settings and Flash Memory Address Ranges

Setting		Description	1MB Flash	2MB Flash	4MB Flash
J1	*Set*	*No Protection*			
	Open	Flash Bank 0: Write protected	Lower 512 KB		Lower 2 MB
		Flash Bank 0: Address Range	0x(9/A)0000000 - 0x(9/A)007FFFF	0x(9/A)0000000 - 0x(9/A)01FFFFF	0x(9/A)0000000 - 0x(9/A)01FFFFF
J2	*Set*	*No Protection*			
	Open	Flash Bank 1: Write protected	Upper 512 KB		Upper 2 MB
		Flash Bank 1: Address Range	0x(9/A)0080000 - 0x(9/A)00FFFFF		0x(9/A)0200000 - 0x(9/A)03FFFFF

Default settings are in italics.

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Appendix B

(E)CXC

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B. (E)CXC

The Controller eXtension Connector (CXC) is a local mezzanine interface. The CXC contains a 16-bit data bus, seven address lines, and eight decoded chip select lines. Addressing of the individual CXC backplane slots is achieved via the CS5 line of the MPC860T processor. The eight CXC chip selects (_CS0 to _CS7) make it possible to select the individual backplane slots.

Additionally, the CXC provides four IRQ's, DMA capability, three serial ports, and one set of parallel port signals.

B.1 (E)CXC Address Ranges

The following tables provide addressing information for both the CXC and ECXC operational modes for the CPU boards indicated. In the case of CXC mode operation, the address range is 256 bytes, whereas, in ECXC mode there are 16 MBytes addressable.

Table B-1: CXC Address Range

Slot	Chip Select	[V]IUC VSBC-4	VM30	VSBC-32 IUC32	VM(6)42 VM(6)62	VSBC-860 IUC860
BU2	CS0	0xF70000	0xC1F70000	0x0BF70000	0xCBF70000	0xB0000000
BU3	CS1	0xF70400	0xC1F70400	0x0BF70400	0xCBF70400	0xB0000400
BU4	CS2	0xF70800	0xC1F70800	0x0BF70800	0xCBF70800	0xB0000800
BU5	CS3	0xF70C00	0xC1F70C00	0x0BF70C00	0xCBF70C00	0xB0000C00
BU6	CS4	0xF71000	0xC1F71000	0x0BF71000	0xCBF71000	0xB0001000
BU7	CS5	0xF71400	0xC1F71400	0x0BF71400	0xCBF71400	0xB0001400
BU8	CS6	0xF71800	0xC1F71800	0x0BF71800	0xCBF71800	0xB0001800
BU0**	CS7	0xF71C00	0xC1F71C00	0x0BF71C00	0xCBF71C00	0xB0001C00

* *BU1 is the system slot*

** *On 5S, 8S, and 8ES for CXM-STAT1 only.*

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Table B-2: Enhanced CXC Address Range

Slot	Chip Select	VSBC-860 IUC860	VSBC-32 IUC32	VM642 VM662
BU2	CS0	0xB0000000	0x10000000	0x10000000
BU3	CS1	0xB1000000	0x11000000	0x11000000
BU4	CS2	0xB2000000	0x12000000	0x12000000
BU5	CS3	0xB3000000	0x13000000	0x13000000
BU6	CS4	0xB4000000	0x14000000	0x14000000
BU7	CS5	0xB5000000	0x15000000	0x15000000
BU8	CS6	0xB6000000	0x16000000	0x16000000
BU0*	CS7	0xB7000000	0x17000000	0x17000000

* *BU1 is the system slot*

** *On 5S, 8S, and 8ES for CXM-STAT1 only.*

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B.2 CXC Generic Pinouts

Table B-3: CXC Connector Pinouts

Pin	Signals		
	Row A	Row B	Row C
1	_IRQ_1[1)]	SER1_RCLK	User-defined
2	_IRQ_2[1)]	SER1_TCLK	_DMA_ACK[1)]
3	_IRQ_3[1)]	GND	_DMA_REQ[1)]
4	_IRQ_4[1)]	SER1_TXD	User-defined
5	User-defined	SER1_RTS	SER3_TCLK
6	User-defined	GND	SER3_RCLK
7	VCC	SER3_RTS	VCC
8	User-defined	SER3_CD	SER3_TXD
9	User-defined	GND	SER3_RXD
10	User-defined	SER1_RXD	User-defined
11	SER2_DTR	User-defined	SER2_CD
12	SER3_DTR	GND	SER2_RTS
13	SER1_DTR	SER1_CTS	SER2_CTS
14	VCC	SER1_CD	VCC
15	_CS-CXC[1)]	GND	SER2_TCLK
16	_AS[1)]	SER3_CTS	SER2_RCLK
17	R/_W[1)]	_SYSR[1)]	SER2_TXD
18	_UDS[1)]	GND	SER2_RXD
19	_LDS[1)]	_EDTACK[1)]	VCC
20	VCC	CXC-CLK	_CS2[1)]
21	A1	GND	_CS3[1)]
22	A2	_CS0[1)]	_CS4[1)]
23	A3	_CS1[1)]	_CS5[1)]
24	A4	GND	_CS6[1)]
25	A5	A6	_CS7[1)]
26	VCC	A7	VCC
27	D0	GND	D10
28	D1	D6	D11
29	D2	D7	D12
30	D3	GND	D13
31	D4	D8	D14
32	D5	D9	D15

1) *Normally active low (by R/_W, only _W).*

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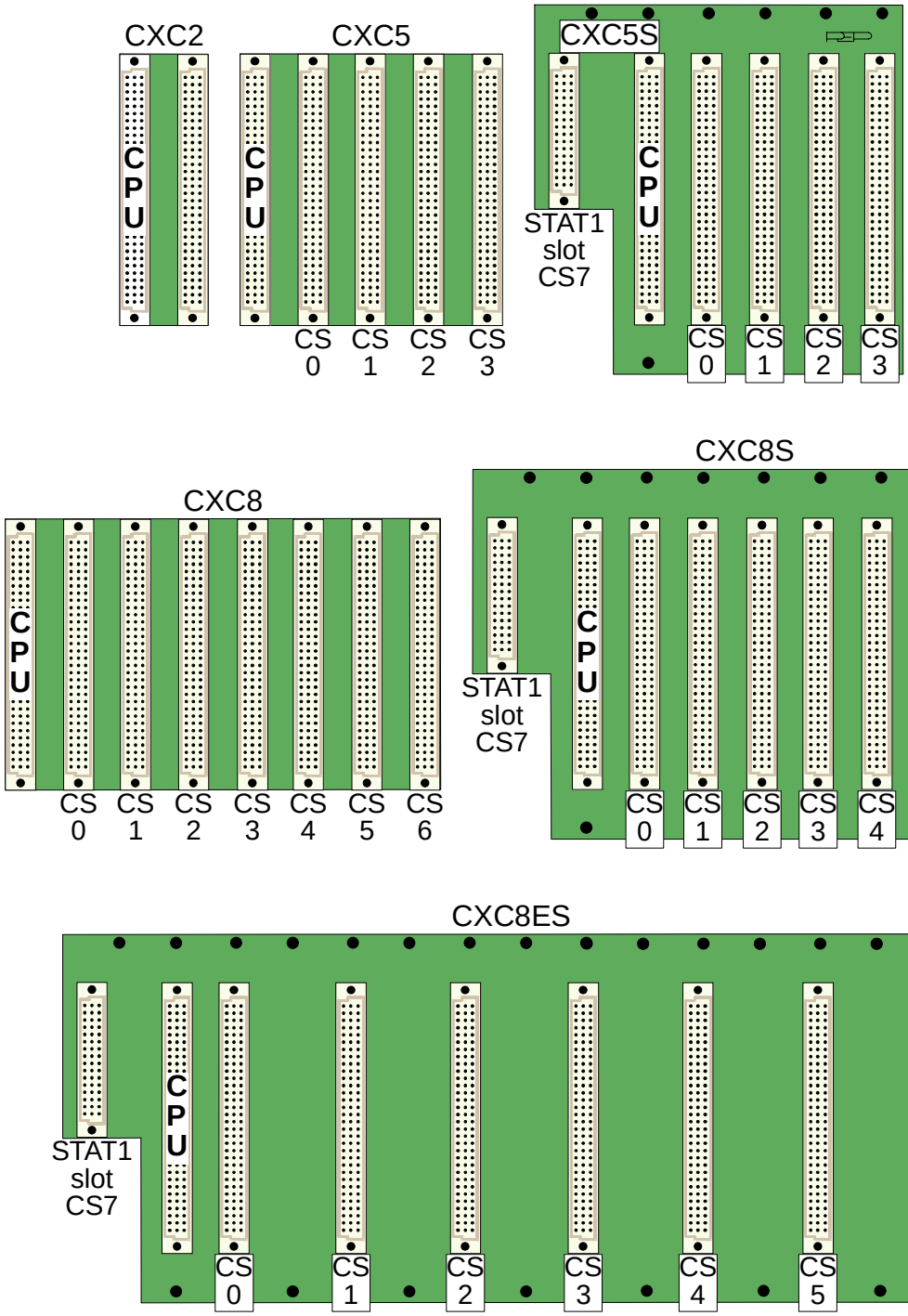
B.3 CXC Pinout Cross Reference to MPC860T

Table B-4: Cross Reference of CXC Signals to MPC860T

PIN	CXC SIGNALS	MPC860T
A1	IRQ_1	PC[12]
A2	IRQ_2	PC[13]
A3	IRQ_3	PC[14]
A4	IRQ_4	PC[15]
A5	User-defined	CXC A5 jumper J15 (PB[14] / +5VSTDBY)
A6	User-defined	PB30, SPICLK
A8	User-defined	PB29, SPITXD
A9	User-defined	PB28, SPIRXD
A10	User-defined	PB22
A11	SER2_DTR	PB[27]
A12	SER3_DTR	PB[31]
A13	SER1_DTR	PB[26]
B1	SER1_RCLK	SER1RCLK jumper J9 (open / PA[6])
B2	SER1_TCLK	PA[5]
B4	SER1_TXD	PA[12]
B5	SER1_RTS	PB[18]
B7	SER3_RTS	PB[16]
B8	SER3_CD	PC[4]
B10	SER1_RXD	PA[13]
B11	User-defined	PB[21]/SMC2TXD
B13	SER1_CTS	PC[9]
B14	SER1_CD	PC[8]
B16	SER3_CTS	PC[5]
C1	User-defined	PB[25]/SMC1TXD
C2	DMA_ACK	PB[23]
C3	DMA_REQ	PC[15]
C4	User-defined	PB[20]/SMC2RXD
C5	SER3_TCLK	PA[1]
C6	SER3_RCLK	PA[0]
C8	SER3_TXD	PA[8]
C9	SER3_RXD	PA[9]
C10	User-defined	PB[24]/SMC1RXD
C11	SER2_CD	PC[6]
C12	SER2_RTS	PB[17]
C13	SER2_CTS	PC[7]
C15	SER2_TCLK	PA[3]
C16	SER2_RCLK	SER2RCLK jumper J14 (open / PA[2])
C17	SER2_TXD	PA[10]
C18	SER2_RXD	PA[11]

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B.4 CXC Backplanes



Note:

When using an 8HP board on the CXC5 and CXC8 backplane, one slot is lost between each board and the next.

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