USER GUIDE



mITX-APL

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MITX-APL – USER GUIDE

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Revision History

Revision	Brief Description of Changes	Date of Issue	Author
1.0	Initial Issue	2018-Mar-08	hjs
1.1	added information in chapter 5.3	2018-Jul-12	hjs
1.2	added OS versions, chapter 6.24 changed	2018-Jul-24	hjs
1.3	Chapter 6.6: caution note added	2018-Oct-08	hjs
1.4	Layout modifications	2019-Jul-23	hjs
1.5	Added Caution limited power source	2020-Jun-18	cw

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Symbols

The following symbols may be used in this manual

⚠DANGER	DANGER indicates a hazardous situation which, if not avoided, will result in death or serious injury.
⚠WARNING	WARNING indicates a hazardous situation which, if not avoided, could result in death or serious injury.
⚠CAUTION	CAUTION indicates a hazardous situation which, if not avoided, may result in minor or moderate injury.
NOTICE	NOTICE indicates a property damage message.
	Electric Shock! This symbol and title warn of hazards due to electrical shocks (> 60 V) when touching products or parts of them. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your material. Please refer also to the "High-Voltage Safety Instructions" portion below in this section.
	ESD Sensitive Device! This symbol and title inform that the electronic boards and their components are sensitive to static electricity. Care must therefore be taken during all handling operations and inspections of this product in order to ensure product integrity at all times.
	HOT Surface! Do NOT touch! Allow to cool before servicing.
	Laser! This symbol inform of the risk of exposure to laser beam and light emitting devices (LEDs) from an electrical device. Eye protection per manufacturer notice shall review before servicing.
	This symbol indicates general information about the product and the user manual. This symbol also indicates detail information about the specific product configuration.
	This symbol precedes helpful hints and tips for daily use.

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1/ Introduction

This manual describes the Mini-ITX board with Apollo Lake CPU. This board will also be denoted mITX-APL within this Users Guide.

The use of this Users Guide implies a basic knowledge of PC hard- and software. This manual is focussed on describing the mITX-APL board's special features and is not intended to be a standard PC textbook.

New users are recommended to study the short installation procedure stated in the following chapter before switching-on the power.

All configuration and setup of the CPU board is either done automatically or manually by the user via the BIOS setup menus.

Latest revision of this manual, datasheet, thermal simulations, BIOS, drivers, BSPs (Board Support Packages) can be downloaded from Kontron Web Page.

2/ Description

The mITX-APL board is based on the Intel Apollo Lake System on Chip (SoC) and is mechanically compliant to the Mini-ITX (mITX) specification. The motherboard with Mini-ITX formfactor is designed for mobile processors with low power consumption. Board key features are:

- Intel Apollo Lake (APL) microprocessor supporting different speed grades from dual to quad core
- memory with one DDR3L 1333/1600/1867 SODIMM socket up to 8 GB
- Support for two independent high resolution graphic displays
- two Display Port (DP) Connectors
- one 24-bit dual-channel LVDS Transmitter
- two 10/100/1000 LAN RJ45 (rear)
- two USB 3.0 Double Stack Connector
- one SATA Gen3 (up to 6GB/s) vertical connector
- one RS232, one RS422 (Half-duplex), one RS485 (Half- and Full-duplex) through internal header
- SPI Interface for external fast IO support
- HD Audio with Stereo Line-in and Line-out (rear)
- Kontron Feature connector
- Temperature Sensor with active cooling solutions
- Wide range from 12 to 24 V DC Power Input or ATX 4-pin (12V)

Built with these functions, mITX-APL Mother Board is ideal for ATM, Automation, Kiosk applications, medical equipment, industrial automation, financial automation, process control, semiconductor equipment and network security markets.

2.1. Configurations

Table 1: Configurations

Product Name (Product Number)	Description	MTBF (hours)
N3350 (1060-7395)	Intel® Mobile Celeron® N3350 2C 2.3 GHz, 6 W, Commercial temp, Entry	1,454,122
E3930 (1060-7384)	Intel® Atom™ x5 E3930 2C 1.8 GHz, 6,5 W, Industrial temp, Entry	1,073,767
E3940 (1060-7396)	Intel® Atom™ x5 E3940 4C 1.8 GHz, 9,5 W, Industrial temp, Intermediate	1,084,363
E3950 (1060-7397)	Intel® Atom™ x7 E3950 4C 2.0 GHz, 12 W, Industrial temp, High	1,084,363

2.2. Accessories List

Table 2: List of Accessories

Connector (RefDes)	On-Board Connectors		Mating Connectors/Cables	
	Manufacturer	Part No.	Manufacturer	Part No.
FANCPU, FANSYS (J6, J5)	Molex	53047-0410	Molex	510210400
SATA 1 Straight	Lotes	ABA-SAT-010-K08	Molex	67489-8005

Connector (RefDes)	On-Board Connectors		Mating Connectors/Cables	
	Manufacturer	Part No.	Manufacturer	Part No.
(J15)			Kontron	821035 (kit)
SATA 2 Right Angle (J16)	Molex	47080-4001	Molex	67489-8005
			Kontron	821035 (kit)
SATA Power (J14)	Molex	22-23-2041	Molex	22.01.2045
	TE Connectivity	640456-4	TE Connectivity	1375820-4
ATX +12V -4p (J28)	Molex	39-28-1043	Molex	39-01-2045
	Foxconn	HM3502E		
	Lotes	ABA-POW-003-K04		
DC Jack (J32)	Singatron	2DC1003-010111	Singatron	2DP1505-000111
Headphone (J24)	Molex	53047-0410	Molex	51021-0400
LVDS (J3)	Samtec	SHF-120-01-L-D-SM-K-TR	Kontron	910000005
	Pinrex	53C-90-40GBE0	Kontron	821515 (kit) *
			Kontron	821515 (kit)
COM 1 RS232 (J30)	Foxconn	HL2205F	Molex	90635-1103
	Pinrex	510-90-10GB00	Kontron	821016 (kit)
	Cen Link	ZP91-014B1-10Y1	Kontron	821017 (kit) *
COM 2 RS485 (J4)	JST	B5B-PH-K-S(LF)(SN)(P)	JST	PHR-5
USB 2.0 (J26, FRONTPNL)	Pinrex	510-80-24GB05	Kontron	821401 (kit)
	Foxconn	HL2112V-P9		
USB 3.0 (J18)	Foxconn	HLL2107-CBC2D-4H		
SPI Hardflash (J2)	Pinrex	210-92-06GB01		
SPDIF –OUT (J30)	Molex	53047-0210	Molex	51021-0200
USB 2.0 (J26, FRONTPNL)	Pinrex	510-80-24GB05	Molex	90635-1243
	Foxconn	HL2112V-P9	Kontron	821042 (kit) *
FEATURE (J31)	Pinrex	52A-90-44GB00	Don Connex	A05c-44-B-G-A-1-G
	Molex	87831-4420	Kontron	1052-5885 (kit) *
CAN Bus (J11)	Molex	53047-0410	Molex	510210400
USB Client (J21)	Mill-Max	897-10-010-00-300002	Würth Electronics Inc.	692904100000
			FTDI	USB 3.0 A MICRO B CABLE

3/ Installation procedure

3.1. Packing Check List

The mITX-APL package includes the following basic items accompany with this manual.

- One mainboard
- One IO shield

Figure 1: Mainboard mITX-APL

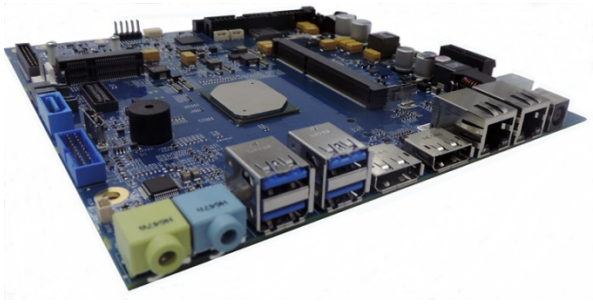
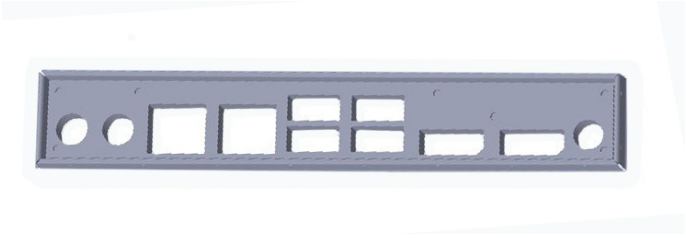


Figure 2: IO Shield (pattern)



If any of these items is damaged or missed, please contact your vendor and save all packing materials for future replacement and maintenance.

Note: The above packing list is for standard single box packing only.

3.2. Installing the Board



ESD Sensitive Device!

Electrostatic discharge (ESD) can damage equipment and impair electrical circuitry.

- Wear ESD-protective clothing and shoes
- Wear an ESD-preventive wrist strap attached to a good earth ground
- Check the resistance value of the wrist strap periodically (OK: 1 MΩ to 10 MΩ)
- Transport and store the board in its antistatic bag
- Handle the board at an approved ESD workstation
- Handle the board only by the edges

To get the board running follow these steps. If the board shipped from Kontron has already components like RAM and CPU cooler mounted, then relevant steps below can be skipped.

NOTICE

Only connect to a power supply delivering the specified input rating and complying with the requirements of Safety Extra Low Voltage (SELV) and Limited Power Source (L.P.S.) of IEC 60950-1 and the Energy sources (ES1) of IEC 62368-1.

1. **Turn off the PSU (Power Supply Unit)**

NOTICE

Turn off PSU (Power Supply Unit) completely (no mains power connected to the PSU) or leave the Power Connectors unconnected while configuring the board. Otherwise components (RAM, LAN cards etc.) might get damaged.

2. **Insert the memory module**
   Be careful to push it in the slot(s) before locking the tabs. For a list of approved memory modules contact your Distributor or FAE. See also chapter "System Memory Support". Use memory modules with the same density in all sockets!
3. **Connecting Interfaces**
   Insert all external cables for hard disk, keyboard etc. A monitor must be connected in order to change BIOS settings.
4. **Connect and turn on PSU**
   Connect PSU to the board by the ATX+12 V-4pin connector or alternatively connect a 12 V DC power adapter to the I/O power jack.
5. **BIOS Setup**
   Enter the BIOS setup by pressing the <F2> key during boot up.

   Enter "Exit Menu" and load Setup Defaults.

   Refer to the "BIOS Configuration / Setup" section of this manual for details on BIOS setup.

To clear all BIOS settings, including Password protection, activate "Load Default BIOS Settings" Jumper for > 10 sec (without power connected).

6. Mounting the board in chassis

NOTICE

When mounting the board to chassis etc. please notice that the board contains components on both sides of the PCB which can easily be damaged if board is handled without reasonable care. A damaged component can result in malfunction or no function at all.

When fixing the Motherboard on a chassis it is recommended to use screws with integrated washer and a diameter of > 7 mm. Do not use washers with teeth, as they can damage the PCB and cause short circuits.

3.3. Requirements IEC60950-1

Take care when designing chassis interface connectors in order to fulfil the IEC60950-1 standard. Users of mITX-APL must evaluate the end product to ensure compliance the requirements of the IEC60950-1 safety standard are met:

- The motherboard must be installed in a suitable mechanical, electrical and fire enclosure.
- The system in its enclosure must be evaluated for temperature and air flow considerations.
- The motherboard must be powered by a CSA or UL approved power supply that limits the maximum input current to 10 A via external barrel-type 12-24 VDC connector, and to 16 A via internal square 12 VDC ATX connector.

- For interfaces having a power pin such as external power or fan, ensure that the connectors and wires are suitably rated. All connections from/to the product shall be with SELV circuits only.
- Wires have suitable rating to withstand the maximum available power.
- The enclosure of the peripheral device fulfils the fire protecting requirements of IEC60950-1.

3.4. Lithium battery precautions

⚠CAUTION

Danger of explosion if the lithium battery is incorrectly replaced.

- Replace only with the same or equivalent type recommended by the manufacturer
- Dispose of used batteries according to the manufacturer's instructions

VORSICHT! Explosionsgefahr bei unsachgemäßem Austausch der Batterie.

- Ersatz nur durch denselben oder einen vom Hersteller empfohlenen gleichwertigen Typ
- Entsorgung gebrauchter Batterien nach Angaben des Herstellers

ATTENTION! Risque d'explosion avec l'échange inadéquat de la batterie.

- Remplacement seulement par le même ou un type équivalent recommandé par le producteur
- L'évacuation des batteries usagées conformément à des indications du fabricant

PRECAUCION! Peligro de explosión si la batería se sustituye incorrectamente.

- Sustituya solamente por el mismo o tipo equivalente recomendado por el fabricante
- Disponga las baterías usadas según las instrucciones del fabricante

ADVARSEL! Lithiumbatteri – Eksplosionsfare ved fejlagtig håndtering.

- Udskiftning må kun ske med batteri af samme fabrikat og type
- Levér det brugte batteri tilbage til leverandøren.

ADVARSEL! Eksplosjonsfare ved feilaktig skifte av batteri.

- Benytt samme batteritype eller en tilsvarende type anbefalt av apparatfabrikanten.
- Brukte batterier kasseres i henhold til fabrikantens instruksjoner

VARNING! Explosionsfara vid felaktigt batteribyte.

- Använd samma batterityp eller en ekvivalent typ som rekommenderas av apparattillverkaren.
- Kassera använt batteri enligt fabrikantens instruktion.

VAROITUS! Paristo voi räjähtää, jos se on virheellisesti asennettu.

- Vaihda paristo ainoastaan lalteval- mistajan suosittelemaan tyyppiln
- Hävitä käytetty paristo valmistajan ohjeiden mukaisesti

4/ System specifications

4.1. Component Main Data

The table below summarizes the features of the mITX-APL embedded motherboard.

Table 3: Component Main Data

Motherboard mITX-APL	
Form factor	Mini ITX (170.18 mm by 170.18 mm by 1.6 mm/LengthxWidthxThickness)
Processor	Onboard CPU variants Intel® Apollo Lake Processor line, 14 nm SoC ▶ Intel® Atom™ x7 E3950 4C 2.0 GHz, 12 W ▶ Intel® Atom™ x5 E3940 4C 1.8 GHz, 9.5 W ▶ Intel® Atom™ x5 E3930 2C 1.8 GHz, 6.5 W ▶ Intel® Mobile Celeron® N3350 2C 2.3 GHz, 6 W
BIOS	Winbond W25Q128FVSIG or Micron N25Q128A13ESE40F (128Mb) for System BIOS
Platform Controller Hub (PCH)	BGA-1296
Memory	A DDR3L 204-pin SODIMM memory module can be used, like ▶ DDR3L, 4 GB 1867 MHz, PC3-1867, non-ECC SODIMM ▶ DDR3L, 8 GB 1867 MHz, PC3-1867, non-ECC SODIMM ▶ DDR3L, 4 GB 1867MHz, PC3-1867, non-ECC, E2 SODIMM ▶ DDR3L, 8 GB 1867MHz, PC3-1867, non-ECC, E2 SODIMM
Flash Memory	The mITX-APL supports embedded embedded Multimedia Card (eMMC) interface 5.0 with a maximum bus speed of 400 MB/s. The board will also support a SD card interface UHS-I standard with a maximum bus speed of 104 MB/s. The eMMC chip is soldered on board. The microSD card interface is sharing a combo connector with the micro SIM card.
Storage	two SATA 3.0: While the first vertical SATA port is dedicated port from the SoC, the second right angle port is combined with mSATA.
Watchdog Timer	Watchdog timer will be supported by the MAX10 CPLD
Wake On	Wake on LAN, USB, Power button (S3 to S5)
Hardware Status Monitor	Monitoring CPU and system temperature, voltage status and fan speed
TPM	Infineon SLB9665 (option)
Power management	▶ ACPI System States support (S0, S3, S4 and S5) ▶ Processor Core/Package States support (C0, C1, C1E, C6, C7, C7L, C8, C9, C10) ▶ Processor Display States support (D0 to D5, and D9) ▶ Dynamic I/O power reduction (disabling sense amps on input buffers, tri-stating output buffers) ▶ Active power-down of display links
Battery	BR2032/CR2032 See Safety Instructions below this table!

Expansion	▶ one PCI-Express 2.0 x1 Slot ▶ one mPCIe/ mSATA with USB/UIM SIM interface
Operating System Support	Six different Board Support Packages are offered: ▶ BSP1: Windows 10 IOT Enterprise 64 bit, eMMC Boot ▶ BSP2: Windows 10 IOT Core, Redstone 64 bit ▶ BSP3: Windows 7, 64 bit, eMMC boot (optional) ▶ BSP4: Windows ES 7, 64 bit, eMMC boot (optional) ▶ BSP5: Linux 64 bit, Yocto ▶ BSP6: VxWorks 7.x or newer (optional) ▶ API: KEAPI 3 for all OS (except fo VxWorks)
External I/O	
LAN, USB3.0	two RJ-45 LAN Ports (with two LED indicators) + 2x dual USB3.0 + 2x dual USB2.0 (4 x USB)
Audio	two audio Jacks for Line-out (lime-color) and Line-input (blue-color)
Display Port (DP)	two Display Port connectors Version 1.2
Power	12 to 24 V DC-IN Power Connector
Internal I/O	
SATA	two connectors (straight and right angle) SATA3.0 (6 Gb/s) and one power connector +5 V and +12 V for external SATA drives
PC Buzzer	Standard PC buzzer on board
USB	two-port USB 3.0 Header on a 19-pin 2mm pitch dual row shrouded header, 1x microUSB 3.0 Type-B, Vertical
Serial Peripheral Interface (SPI)	one SPI on 10-pin (2x5) straight 2.54 mm pitch header
LVDS	one (2 x 20) 1.25 mm pin-header
Mini PCIe	one mPCIe/mSATA
Audio	one microphone, one headphone, one SPDIF
Serial	one RS232, one RS485
GPIO	one 2 x 22-pin header
Internal Header	
Power	two (1 x 4)-pin-header for CPU & System, Power connector +5 V and +12 V for external SATA drives, one 4-pin ATX Power
CMOS Clear	1 x (1 x 3) 2,54 mm pin-header (RTC Circuit)
Front Panel	1 x 24 pin connector, Pin 9 void
MicroSD/microSIM	one microSD & microSIM combo socket adapter

Display	
Graphics Controller	The mITX-APL board supports onboard graphics through two independent interfaces simultaneously: Two DP-Ports and the LVDS-Port. ▶ The two standard outputs in the rear are connected directly to Display Port connectors. ▶ The alternative output will be converted from Embedded DisplayPort (eDP) to LVDS. The LVDS conversion is done by NXP PTN3460BS DisplayPort to dual-channel 24-bit LVDS converter. Configuration for 1x18-, 1x24-, 2x18- and 2x24-bit / pixel can be selected by resistor option on board. The LVDS interface is provided on a standard 40-pin connector.
DP to LVDS Controller	NXP PTN3460I/PTN3460BS
Display Interface	two Display Ports and LVDS Note: Three (3) Independent Displays Max.
Resolution	DP/LVDS 4096x2304 @ 60 Hz, 24 bpp (One panel display)
Ethernet	
Controller	Intel GE WGI210IS/WGI211AT
Interface	IEEE 802.3 10BASE-T / 100BASE-TX / 1000BASE-T compliant
Audio	
Universal Audio Architecture (UAA)	The on-board Audio circuit implements six Channel High Definition Audio with UAA (Universal Audio Architecture), featuring three 24-bit stereo Digital-to-Analog converter (DACs) and two 24-bit stereo Analog-to-Digital Converter ADC.
Power	
Onboard Power Supply	All used power rails are generated internal by a highly integrated DC/DC power unit ☐ ▶ Voltage Ripple specification max ±5 % peak to peak 0 to 20 MHz ☐ ▶ Rise Time specification 2 to 20ms from input voltage <10% to nominal VCC
External Power Supply	The mITX-APL is operated by a single 12 to 24 V wide Input Voltage (VIN) DC supply from DC Jack on rear I/O Singatron 2DC1003-010111 or optionally 12 V DC supply through an internal ATX 4-pin header.

⚠CAUTION

Danger of explosion if the lithium battery is incorrectly replaced.

- Replace only with the same or equivalent type recommended by the manufacturer
- Dispose of used batteries according to the manufacturer's instructions

NOTICE

Only connect to a power supply delivering the specified input rating and complying with the requirements of Safety Extra Low Voltage (SELV) and Limited Power Source (L.P.S.) of IEC 60950-1 and the Energy sources (ES1) of IEC 62368-1.

NOTICE

The power supply used must comply with the requirements of the IEC 60950-1 or IEC 62368-1 standard or better. In the case of an unintentional temporary under voltage interruption use a power supply with an adequate holdup-time (brownout) and ensure the power supply has been fully tested to at least meet the minimum immunity of AC inputs requirements, as stipulated in IEC 55024. Including power supplies marketed with a separate AC/DC power converter.

NOTICE

After a brownout condition the power supply must remain in the “off state” long enough to allow all internal voltages to discharge sufficiently. Failure to observe this required “off state” time may mean that parts of the board or peripherals work incorrectly or suffer a reduction of MTBF. The minimum “off state” time, to allow internal voltages to discharge sufficiently, is dependent on the power supply and additional electrical factors. To determine the required “off state” time, each case must be considered individually. For more information, contact Kontron Support.

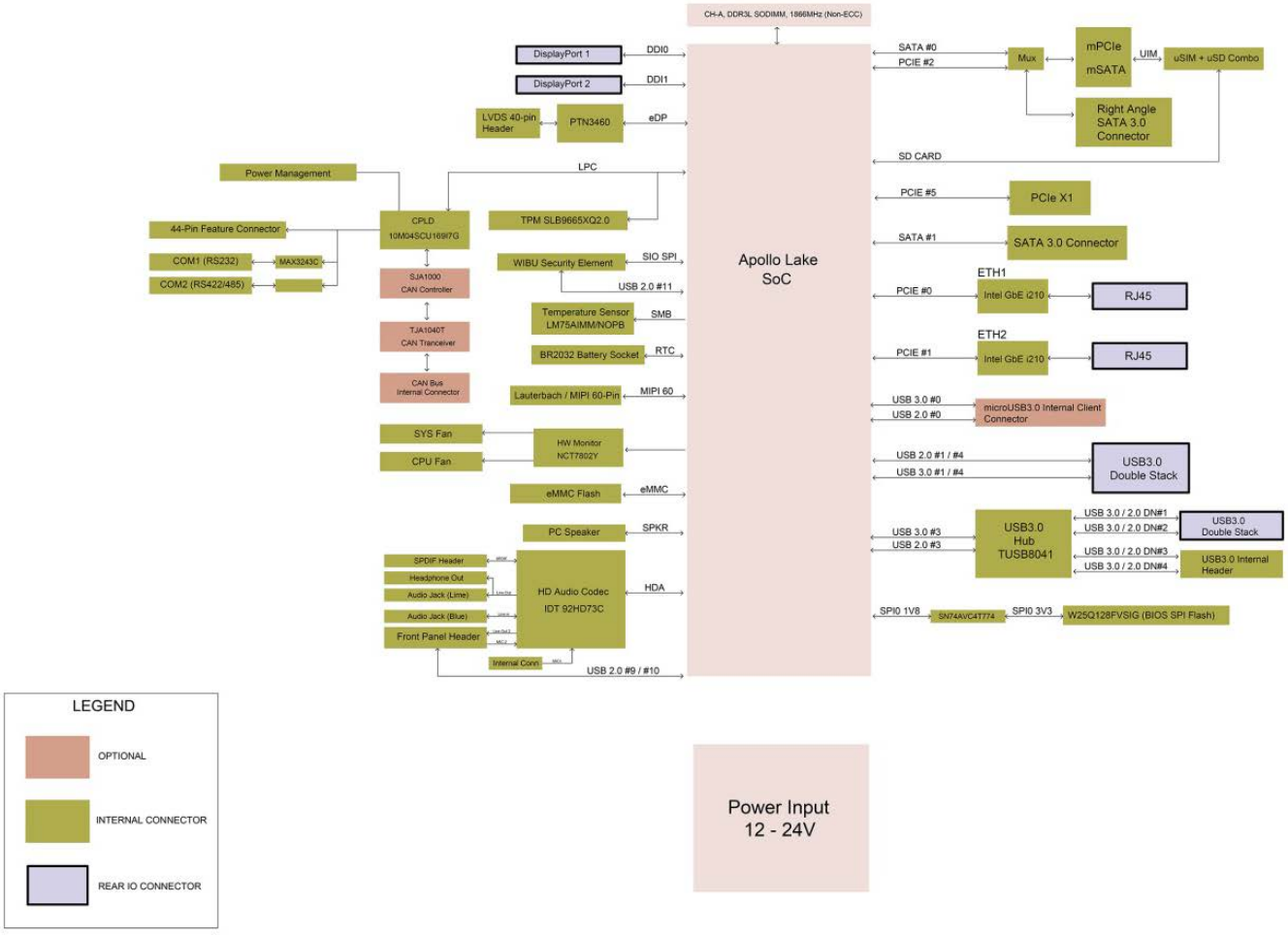
4.2. Environmental Conditions

Table 4: Environmental Conditions

Operating	The board has two temperature ranges: ▶ commercial grade: 0°C to +60°C (32°F~140°F) operating temperature (forced cooling). ▶ extended grade: -25°C to +75°C (-13°F~167°F) operating temperature It is the customer's responsibility to provide sufficient airflow around each of the components to keep them within allowed temperature range. Please refer to the thermal simulation report for information about airflow. 10% to 95% relative humidity (non-condensing)
Storage	-40°C to 85°C (-40°F to 185°F); lower limit of storage temperature is defined by specification restriction of on-board BR2032/CR2032 battery. Up to 95 % relative humidity (temperature 25°C to 30°C)
Radiated Emissions (EMI)	All Peripheral interfaces intended for connection to external equipment are EMI protected. ▶ EN55022 Class B radiated and conducted ▶ EN 61000-6-4:2007 (EMC) Generic emission standard Part 6-4: Emission standard for industrial environments ▶ EN 61000-6-2:2005 (EMC) – Generic standard – Immunity for industrial environmental ▶ Includes following tests accordingly ▶ IEC 61000 PT4-2, (EN 61000-4-2) Electrostatic discharge immunity ESD ▶ IEC 61000 PT4-3, (EN 61000-4-3 and ENV 50204) Radiated Field ▶ IEC 61000 PT4-4, (EN 61000-4-4) Electrical fast transient/burst (EFT) BURST ▶ IEC 61000 PT4-5, (EN 61000-4-5) Surge immunity test ▶ IEC 61000 PT4-6, (EN 61000-4-6) Immunity to conducted disturbances ▶ IEC 61000 PT4-8, (EN 61000-4-8) Immunity to magnetic fields (LOW) ▶ IEC 61000 PT4-11, (EN 61000-4-11) Testing and measuring techniques-voltage dips, short interruption, and voltage variations immunity tests
Safety	EN 60950-1:2006 +A11:2009 +A1:2010 +A12:2011: Safety for information technology equipment including electrical business equipment
Shock	Conducted in standard available ATX chassis. Test is following Standard IEC 60068-2-27, half-sine wave, Acceleration2g, Pulse duration ： 11ms. Number of shocks: 600 shocks (100 shocks for each face.)
Bump	IEC 60068-2-27: Half Sine Waveform Acceleration 2g; Pulse Duration 11ms. Number of shocks: 600 shocks (100 shocks for each face.)
Vibration	AW IEC 60068-2-64, test Fh, Random Vibration, 90 min per axis, 3 axes at 1.9 grms, with PSD: 10-20Hz: 0.05 g^2/Hz and 20-500Hz:- 3dB/octave.
Theoretical MTBF	1,073,767 to 1,454,122 hours depending on processor type at 30° C for the mITX-APL
Restriction of Hazardous Substances (RoHS II)	The product will comply to the European Council Directive on the approximation of the laws of the member states relating to Directive 20011/65/EU or the last status thereof.
Altitude	2000 m max.

4.3. Block Diagram

Figure 3: Block Diagram of mITX-APL



5/ Jumpers and Connectors

5.1. Hardware Configuration Setting

This chapter gives the definitions and shows the positions of jumpers, headers and connectors. All of the configuration jumpers on the board are in the proper position. The default settings shipped from factory are marked with an asterisk (*).

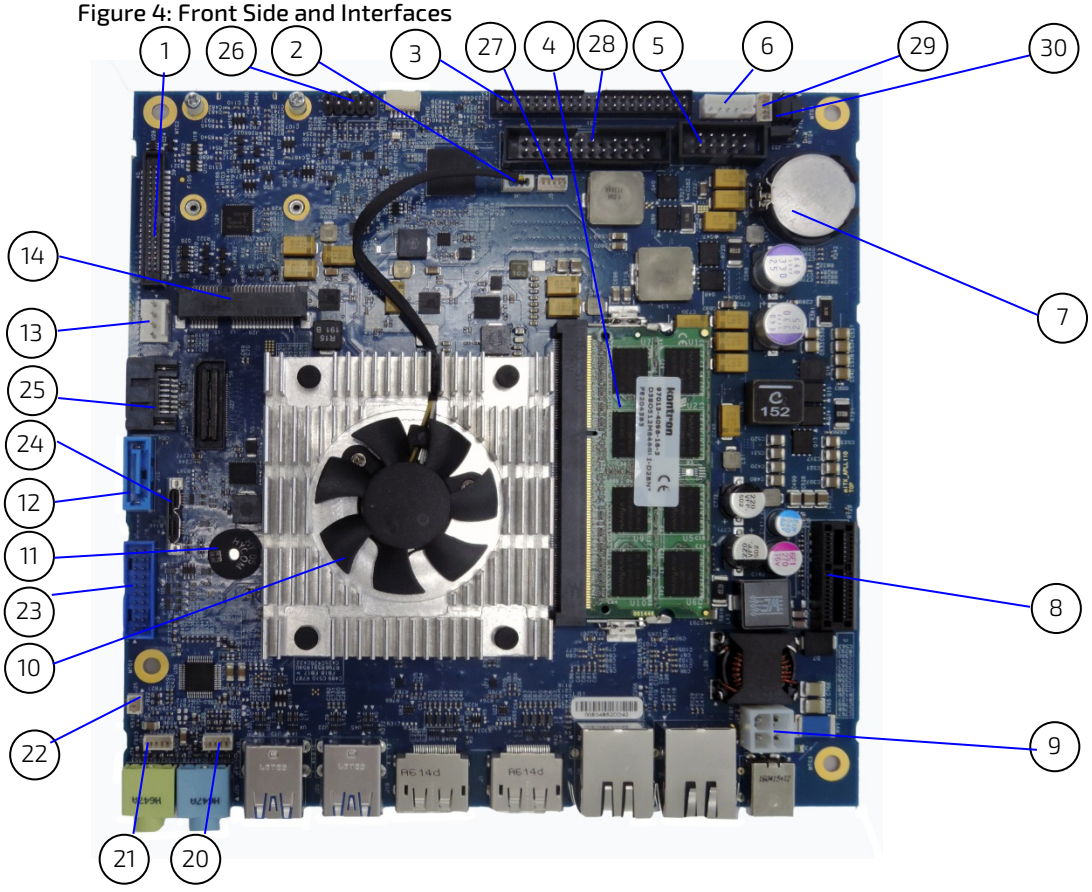
In general, jumpers on the board are used to select options for certain features. Some of the jumpers are designed to be user-configurable, allowing for system enhancement. The others are for testing purpose only and should not be altered. To select any option, cover the jumper cap over (SHORT) or remove (NC) it from the jumper pins according to the following instructions. Here, NC stands for "Not Connect".

5.1.1. Jumpers and Connectors

Jumpers	Function	Remark
CLR_CMOS (J36, J37)	Clear CMOS/RTC	2x 3-pin header
AUTOSTART (J33)	Always on	1 x 2 header
Connectors	**Function**	**Remark**
CPU_FAN1	CPU FAN Connector	1 x 4 wafer
SYS_FAN1	SYS FAN Connector	1 x 4 wafer
Front Panel (J26)	Front Panel Connector	2 x 5 header (pin9 void)
SPKR	Speaker Connector	1 x 4 wafer
LVDS (J27)	LVDS Connector	2 x 20 connector
ATX 4-pin	ATX Power Connector	2 x 2 connector
DC Jack	Power Connector	jack
MINI-PCIE (J29)	Mini PCIe Connector	2 x 26 connector
PCIEx1 (J17)	PCIe x1 Connector	2 x 18 connector
SPI_SOCKET	Bios Socket	2 x 5 connector
SATA	SATA3.0 Connector	Standard
SATA Port angle + Mux	SATA connector	
Battery	Battery Socket	BR2032/CR2032 compatible
SODIMM	Memory Socket	Slot
GPIO	GPIO connector	2 x 22 connector
USB3.0 (J18)	USB 3.0 Front Header	19-pin header
CAN Bus (J11, optional)	internal connector	4-pin connector
micro USB Client Port (optional)	internal USB connector	
RS232		2x 5-pin connector
RS485		5-pin connector
SATA Power		4-pin connector
SPDIF		2-pin connector
Mic		4-pin connector
Headphone		4-pin connector

5.2. Mainboard Placement and Rear I/O locations

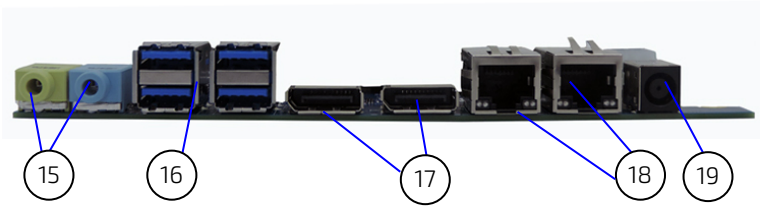
Figure 4: Front Side and Interfaces



1 LVDS connector
2 CPU and Sys Fan connector
3 GPIO (44-Pin connector)
4 Memory with connector
5 RS232
6 RS485
7 Battery
8 PCIe X1 connector
9 ATX-Four-Pin Power connector
10 CPU with fan
11 Speaker
12 SATA connector (straight and right-angle)
13 Power connector for SATA drives
14 mPCIe/mSATA
15 Audio jacks
16 four USB (2.0/3.0)
17 two Display Ports
18 two Ethernet Ports
19 Power connector
20 Mic1 connector
21 Headphone connector
22 SPDIF connector
23 USB 3.0 internal header
24 Micro USB 3.0 client connector
25 Right angle SATA connector
26 BIOS recovery Socket
27 System fan connector
28 Front panel header
29 CANBus connector
30 Jumper block

5.2.1. Inferfaces

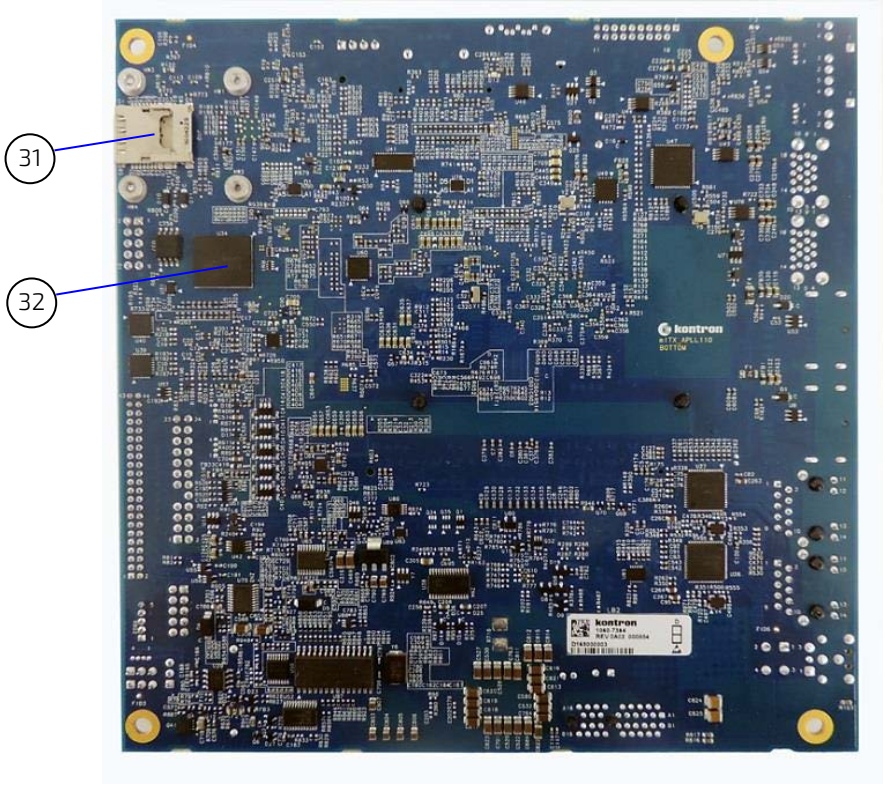
Figure 5: Interfaces



For the numbers look at page 24.

5.2.2. Rear Side

Figure 6: Rear Side



31 MicroSIM/MicroSD Combo adapter
32 eMMC controller

6/ Pin Definitions

The following sections provide pin definitions and detailed description of all on-board connectors.
The connector definitions follow the following notation:

Table 5: Connector Definitions

Column Name	Description
Pin	Shows the pin-numbers in the connector. The graphical layout of the connector definition tables is made similar to the physical connectors.
Signal	The mnemonic name of the signal at the current pin. The notation "XX#" states that the signal "XX" is active low.
Type	AI: Analog Input. AO: Analog Output. I: Input, TTL compatible if nothing else stated. IO: Input / Output. TTL compatible if nothing else stated. IOT: Bi-directional tristate IO pin. IS: Schmitt-trigger input, TTL compatible. IOC: Input / open-collector Output, TTL compatible. IOD: Input / Output, CMOS level Schmitt-triggered. (Open drain output) NC: Pin not connected. O: Output, TTL compatible. OC: Output, open-collector or open-drain, TTL compatible. OT: Output with tri-state capability, TTL compatible. LVDS: Low Voltage Differential Signal. PWR: Power supply or ground reference pins.
	Ioh: Typical current in mA flowing out of an output pin through a grounded load, while the output voltage is > 2.4 V DC (if nothing else stated). Iol: Typical current in mA flowing into an output pin from a VCC connected load, while the output voltage is < 0.4 V DC (if nothing else stated).
Pull U/D	On-board pull-up or pull-down resistors on input pins or open-collector output pins.
Note	Special remarks concerning the signal.
Designation	Type and number of item described
see Section	Number of section in this manual containing detailed description

6.1. Processor Support

The Intel Apollo Lake BGA1296 14 nm is a SoC architecture with integrated Memory and Graphics Controller. The system supports the following embedded Stockkeeping Units (SKUs) for Apollo Lake platform:

- Intel® Atom™ x7 E3950 4C 2.0 GHz, 12 W
- Intel® Atom™ x5 E3940 4C 1.8 GHz, 9.5 W
- Intel® Atom™ x5 E3930 2C 1.8 GHz, 6.5 W
- Intel® Mobile Celeron® N3350 2C 2.3 GHz, 6 W

Kontron has defined the board versions as listed in the following table, so far all based on Embedded CPUs.

Table 6: Processor Support

Name	Product number	Speed	Embed.	Cache	Sspec	TDP / Tj
Atom x7 E3950 4C	46010-0000-20-4	2.0 GHz	Yes	2 MB		12 W/110°C
Atom x5 E3940 4C	46010-0000-18-4	1.8 GHz	Yes	2 MB		9.5 W/85°C
Atom x5 E3930 2C	46010-0000-18-2	1.8 GHz	Yes	2 MB		6.5 W/110°C
Mobile Celeron N3350 2C	46010-0000-23-2	2.3 GHz	Yes	2 MB	SR2YB	6 W/105°C

6.2. System Memory Support

The mITX-APL board supports a single-channel non-ECC DDR3L memory interface with one SODIMM. The integrated memory controller can support memory speeds of 1333/1600/1867 MHz. Maximum memory supported is 8 GB.

- DDR3L, 4 GB 1867MHz, PC3-1867, non-ECC SODIMM, Commercial Temp
- DDR3L, 8 GB 1867MHz, PC3-1867, non-ECC SODIMM, Commercial Temp
- DDR3L, 4 GB 1867MHz, PC3-1867, non-ECC SODIMM, Industrial (E2) Temp
- DDR3L, 8 GB 1867MHz, PC3-1867, non-ECC SODIMM, Industrial (E2) Temp



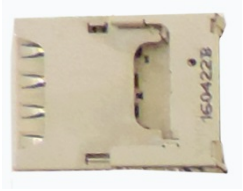
If using 32 Bit OS, less than 4 GB are displayed in the system (Shared Video Memory/PCI resources is subtracted).

6.3. Flash Memory

The mITX-APL supports eMMC interface 5.0 with a maximum bus speed of 400 MB/s. The board will also support a SD card interface UHS-I standard with a maximum bus speed of 104 MB/s.

- The eMMC chip is soldered on board.
- The microSD card interface is sharing a combo connector with the micro SIM card.

Figure 7: Combo Connector for MicroSD and MicroSIM

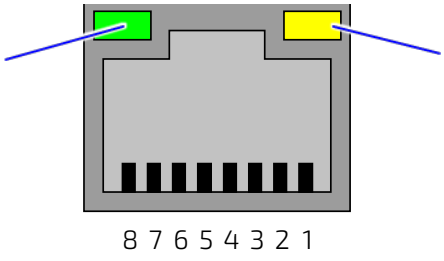


6.4. Ethernet Connectors (I/O area)

The mITX-APL supports three channels of 10/100/1000 Mbit/s Ethernet (LAN1 to LAN3).

In order to achieve the specified performance of the Ethernet port, Category 5 twisted pair cables must be used with 10/100 MByte/s and Category 5E, 6 or 6E with 1 Gbit/s LAN networks.

Figure 8: Ethernet Connector



Pin Assignment

Pin	Signal	Ethernet 10 BaseT/100BaseT	Gigabit-Ethernet
1	MDI0+	TX+	DA+
2	MDI0-	TX-	DA-
3	MDI1+	RX+	DB+
4	MDI1-		DC+
5	MDI2+		DC-
6	MDI2-	RX-	DB-
7	MDI3+		DD+
8	MDI3-		DD-

6.5. USB Connectors (I/O area)

Figure 9: USB 2.0 / 3.0 socket

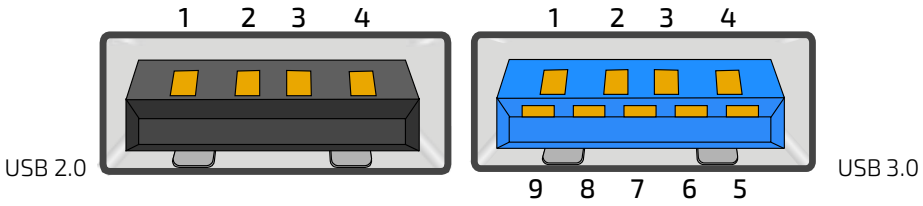


Table 7: Pin Assignment

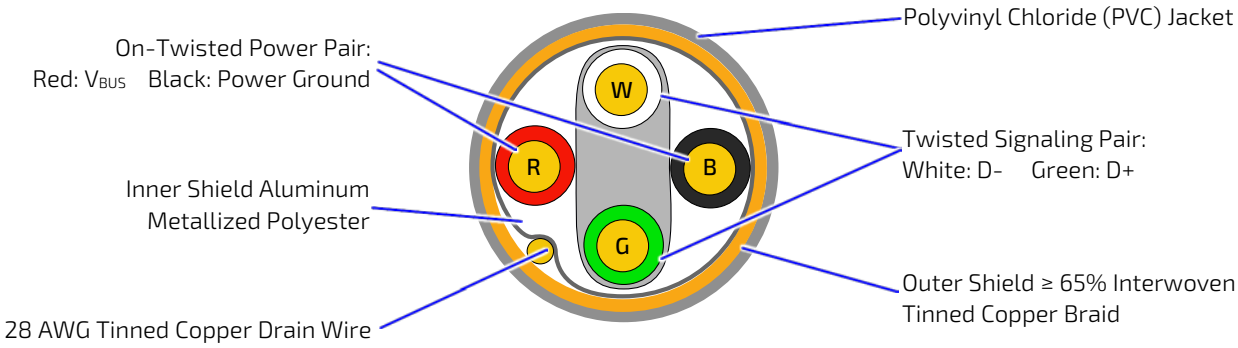
Pin	Type	Signal	Note
1	PWR	5 V / SB 5 V	USB2.0 / 3.0
2	IO	USB 3-	USB2.0 / 3.0
3	IO	USB 3+	USB2.0 / 3.0
4	PWR	GND	USB2.0 / 3.0
5	IO	RX 2-	USB3.0
6	IO	RX 2+	USB3.0
7	PWR	GND	USB3.0
8	IO	TX 2-	USB3.0
9	IO	TX 2+	USB3.0

Table 8: Signal Description

Signal	Description
USBn+ USBn- RXn+ RXn- TXn+ TXn-	Differential pair works as serial differential receive/transmit data lines. (n= 0,1,2,3)
5 V / SB5 V	5 V supply for external devices. SB5 V is supplied during power-down to allow wakeup on USB device activity. Protected by resettable 2 A fuse covering both USB ports.

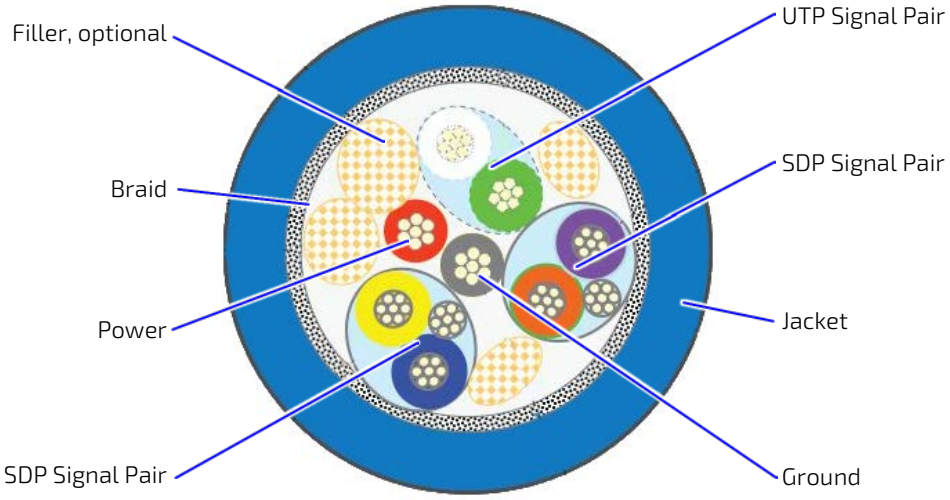
For USB2.0 cabling it is required to use only HiSpeed USB cable, specified in USB2.0 standard:

Figure 10: USB 2.0 High Speed Cable



For USB3.0 cabling it is required to use only HiSpeed USB cable, specified in USB3.0 standard:

Figure 11: USB 3.0 High Speed Cable



6.6. DC Power-Jack Connector J56

Figure 12: DC Power-Jack Connector

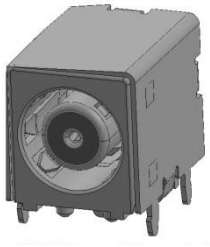


Table 9: DC Power-Jack Connector

Pin	Signal	Description	Type
Center	Vin	Power +12 V to 24 V (2.5 mm Center Pin)	PWR
Ring	GND	Ground (5.5 mm Ring hole)	PWR

⚠CAUTION

The board can be supplied via the AC/DC adapter plugged into the power jack. Such adapters have usually no connection to protective earth. Consequently, the potential of the conductive parts on the board may drift. If a human touches such a part, this may lead to an electric shock. The board must be grounded separately, if the unit is supplied via power jack.

6.7. Audio Jack Connectors (I/O area)

Figure 13: Audio Jacks



Table 10: Pin Assignment (Line Out, green, Figure 13 left)

Pin	Signal
1	GND
2	Lineout_Rear_L/Headphone_L
3	Lineout_Rear_JD
4	GND
5	Lineout_Rear_R/Headphone_R

Table 11: Pin Assignment (Line In, blue, Figure 13 right)

Pin	Signal
1	GND
2	Linein_Rear_L
3	Linein_Rear_JD
4	GND
5	Linein_Rear_R

6.8. Fan Connectors (internal)

The FANSYS (SYS_FAN) can be used to power, control and monitor a fan for chassis ventilation etc.

The FANCPU (CPU_FAN) is used for the connection of the FAN for the CPU.

The 4-pin header is recommended to be used for driving 4-wire type Fan in order to implement FAN speed control.

Figure 14: 4-pin Fan Connector

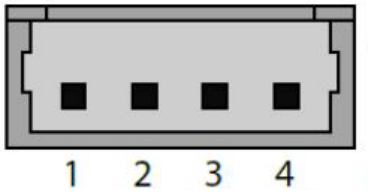


Table 12: 4-pin Mode

Pin	Signal	Description	Type
1	GND	Ground	PWR
2	12 V	+12 V supply	PWR
3	TACHO	Fan speed sense	I

Pin	Signal	Description	Type
4	PWM	Fan speed control.	O

Table 13: Signal Description

Signal	Description	Type
GND	Power Supply GND signal	PWR
12 V	+12 V supply for fan. A maximum of 2000 mA can be supplied from this pin.	PWR
TACHO	Tacho input signal from the fan, for rotation speed supervision RPM (Rotations Per Minute).	I
PWM	Output signal for FAN speed control.	O

6.9. Front Panel 1 (internal)

Figure 15: FP1 Connector

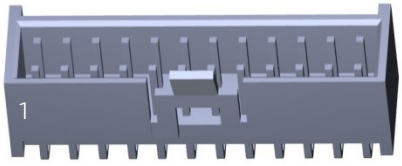


Table 14: FP1 Connection

Pin	Description	Pin	Description
1	USB_PWR_D2	2	USB_PWR_D3
3	USBhub_D2-	4	USBhub_D3-
5	USBhub_D2+	6	USBhub_D3+
7	GND	8	GND
9	NC	10	LINE2-L
11	+5 V	12	+5 V
13	SATA_LED#	14	SUS_LED
15	GND	16	PWRBTN_IN#
17	RSTIN#	18	GND
19	SB3V3	20	LINE2-R
21	AGND	22	AGND
23	MIC2-L	24	MIC2-R

6.10. RS232 Header (internal)

Figure 16: 2-wire RS232

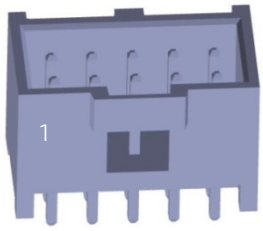


Table 15: RS232 Header

Pin	Description	Pin	Description
1	NC	2	NC
3	NSIN	4	NC
5	NSOUT	6	NC
7	NC	8	NC
9	GND	10	5 V

Table 16: Signal Description

Signal	Description
NSIN	User Input
NSOUT	User Output
GND	Ground

Figure 17: Available Cable Kit (DB9 adapter cables)



6.11. RS-485 Header (internal)

Figure 18: RS-485 Header

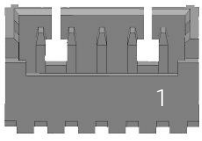


Table 17: RS-485 Header

Pin	Description
1	TX1-
2	RX1+

Pin	Description
3	TX1+
4	RX1-
5	GND

6.12. Feature Connector

Figure 19: Internal Feature Connector (2x22 pins)

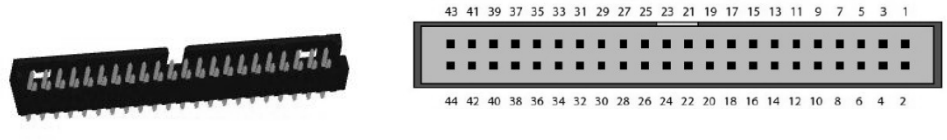


Table 18: Feature Connector

Pin	Description	Pin	Description
1	NC	2	SMBC
3	S4#	4	SMBD
5	PWR_OK	6	EXT_BAT
7	NC	8	NC
9	SB3V3	10	SB5V
11	GPIO0	12	GPIO1
13	GPIO2	14	GPIO3
15	GPIO4	16	GPIO5
17	GPIO6	18	GPIO7
19	GND	20	GND
21	GPIO8	22	GPIO9
23	GPIO10	24	GPIO11
25	GPIO12	26	GPIO13
27	GPIO14	28	GPIO15
29	GPIO16	30	GPIO17
31	GND	32	GND
33	EGCLK	34	EGCS#
35	EGAD	36	TMA0
37	+12 V	38	GND
39	NC	40	NC
41	GND	42	GND
43	GND	44	S3#

6.13. CMOS1 Internal

Figure 20: CMOS1 Internal Connector

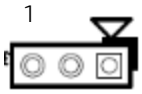


Table 19: CMOS1 Internal Connection

Pin	Description
1	GND
2	RTCRST#
3	NC

6.14. SPK Internal

Figure 21: SPK Internal Connector

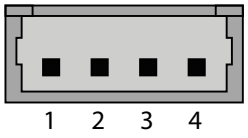


Table 20: SPK Internal Connection

Pin	Description
1	GND
2	HP Left
3	GND
4	HP Right

6.15. MIC1 Connector (J22)

The MIC1 interface is available through the connector J22 (four pins). The input is enabled through the Windows Audio Manager. The Signal-to-Noise Ratio (SNR) is up to 100 dB.

Figure 22: MIC1 Connector

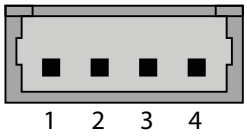


Table 21: Pin Assignment

Pin	Signal	Type
1	GND	PWR
2	MIC1_L_Header	AO
3	GND	PWR
4	MIC1_R_Header	AO

6.16. SPDIF-OUT Connector (J25)

The digital audio interface (electrical SPDIF-Out) is available through the 2-pin connector J25 and can be used to implement 6 (5.1) Channel High Definition Audio. Circuit is based on high fidelity 6-channel HD audio codec which is compatible with Intel HD Audio specification and supports stereo 24-bit resolution and up to 192 kHz sample rate for DACs/ADCs. The Signal-to-Noise Ratio (SNR) is up to 90 dB. 16/20/24-bit SPDIF TX Outputs are supporting 48 K/96 K/44.1 K/88.2 KHz sample rate.

Figure 23: SPDIF-OUT Connector

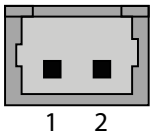


Table 22: Pin Assignment

Pin	Signal	Type
1	F_SPDIF_OUT	O-3.3
2	GND	PWR

6.17. LVDS internal (J3)

Figure 24: LVDS Connector

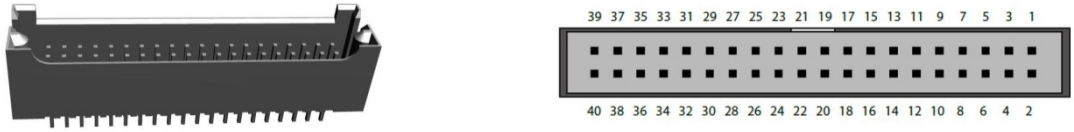


Table 23: LVDS Pin Assignment

Pin	Description	Pin	Description
1	+12 V	2	+12 V
3	+12 V	4	+12 V
5	+12 V	6	GND
7	DTR	8	GND
9	GND	10	5V
11	DDC CLK	12	DDC DATA
13	BKLTCTL	14	VDD ENABLE
15	BKLTEN#	16	GND

Pin	Description	Pin	Description
17	LVDS A0-	18	LVDS A0+
19	LVDS A1-	20	LVDS A1+
21	LVDS A2-	22	LVDS A2+
23	LVDS ACLK-	24	LVDS ACLK+
25	LVDS A3-	26	LVDS A3+
27	GND	28	GND
29	LVDS B0-	30	LVDS B0+
31	LVDS B1-	32	LVDS B1+
33	LVDS B2-	34	LVDS B2+
35	LVDS BCLK-	36	LVDS BCLK+
37	LVDS B3-	38	LVDS B3+
39	GND	40	GND

6.18. SATA (Serial ATA) Disk Interfaces (internal)

Figure 25: SATA Connector

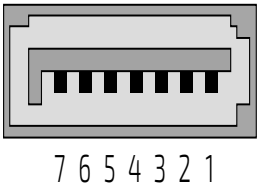


Table 24: Pin Assignment

Pin	Signal	Type
1	GND	PWR
2	SATA* TX+	
3	SATA* TX-	
4	GND	PWR
5	SATA* RX-	
6	SATA* RX+	
7	GND	PWR

Table 25: Signal Description

Signal	Description
SATA* RX+ / RX-	Host transmitter differential signal pair
SATA* TX+ / TX-	Host receiver differential signal pair

"*" specifies 0 or 1 depending on SATA port.

Figure 26: Available Cable Kit



6.19. SATA Power Connector (J14)

Figure 27: SATA Power Connector

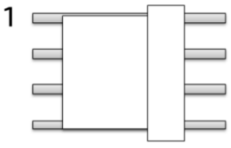


Table 26: Pin Assignment

Pin	Signal	Description	Type
1	+5VS	Power +5V	PWR
2	GND	Ground	PWR
3	GND	Ground	PWR
4	+12VS	Power +12V	PWR

6.20. Display Port

The two external Display Port 1.2 at rear I/O space are supporting Active/Passive HDMI 1.4a and DVI adapters.

Figure 28: Display Port

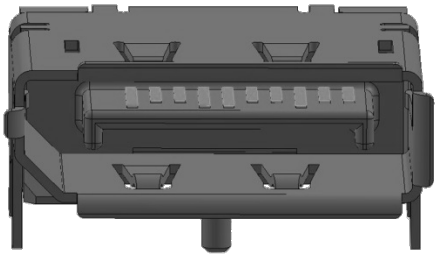


Table 27: Display Port

Pin	Signal	Description
1	ML_Lane 0 (p)	Lane 0 (positive)
2	GND	Ground
3	ML_Lane 0 (n)	Lane 0 (negative)
4	ML_Lane 1 (p)	Lane 1 (positive)
5	GND	Ground
6	ML_Lane 1 (n)	Lane 1 (negative)

Pin	Signal	Description
7	ML_Lane 2 (p)	Lane 2 (positive)
8	GND	Ground
9	ML_Lane 2 (n)	Lane 2 (negative)
10	ML_Lane 3 (p)	Lane 3 (positive)
11	GND	Ground
12	ML_Lane 3 (n)	Lane 3 (negative)
13	CONFIG1	connected to Ground
14	CONFIG2	Connected to Ground
15	AUX CH (p)	Auxiliary Channel (positive)
16	GND	Ground
17	AUX CH (n)	Auxiliary Channel (negative)
18	Hot Plug	Hot Plug Detect
19	Return	Return for Power
20	DP_PWR	Power for connector (3.3 V 500 mA)

6.21. DC Power Connector

Figure 29: Power Connector

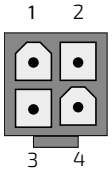


Table 28: Pin Assignment

Pin	Signal	Description	Type
1	GND	Ground	PWR
2	GND	Ground	PWR
3	12 V	Power +12 V to +24 V	PWR
4	12 V	Power +12 V to +24 V	PWR

6.22. SPI Connector (J2)

Figure 30: SPI Connector 10x Pin header



Table 29: Pin Assignment

Pin	Signal	Type
1	CLK	
2	SB3V3	PWR
3	CS0#	I
4	ADDIN	IO
5	3V3_SPI	
6	NC	
7	MOSI	IO
8	ISOLATE#	IO
9	MISO	IO
10	GND	PWR

Table 30: Signal description

Signal	Description
CLK	Serial Clock
SB3V3/3V3_SPI	3.3 V Standby Voltage power line. Normally output power, but when Motherboard is turned off then the on-board SPI Flash can be 3.3 V power sourced via this pin.
CS0#	CS0# Chip Select 0, active low.
ADDIN	ADDIN input signal must be NC
MOSI	Master Output, Slave Input.
ISOLATE#	The ISOLATE# input, active low, is normally NC, but must be connected to GND when programming the SPI flash. Power Supply to the Motherboard must be turned off when loading SPI flash. The pull up resistor is connected via diode to 5VSB.
MISO	Master Input, Slave Output

6.23. Combo Connector for MicroSD and MicroSIM

The mITX-APL supports eMMC interface 5.0 with a maximum bus speed of 400 MB/s. The board will also support a SD card interface UHS-I standard with a maximum bus speed of 104 MB/s.

- The eMMC chip is soldered on board.
- The microSD card interface is sharing a combo connector with the micro SIM card.

Figure 31: Combo Connector for MicroSD and MicroSIM

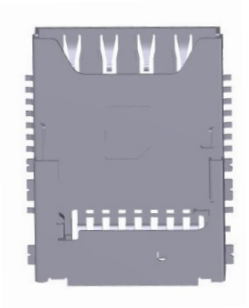


Table 31: Pin Assignment MicroSIM

Pin	Type
1	V_VCC
2	RST
3	CLK_S3
4	RSVD_S4
5	GND_S5
6	V_VPP
7	I/O
8	RSVD_S8

Table 32: Pin Assignment MicroSD

Pin	Type
1	DAT2
2	CD/DAT3
3	CMD
4	V_VDD
5	CLK_T5
6	VSS/GND
7	DAT0
8	DAT8

6.24. Slot Connector (mPCIe/mSATA) (J29)

NOTICE

The Slot connector has two functions: mSATA or miniPCIe. The Slot connector detects the mounted card technology with autosensing. So there is no need for further configuration.

NOTICE

mSATA functionality is multiplexed with right angle SATA connector (J16). You can only use one function (mSATA or standard SATA)

Figure 32: Slot Connector (mPCIe)

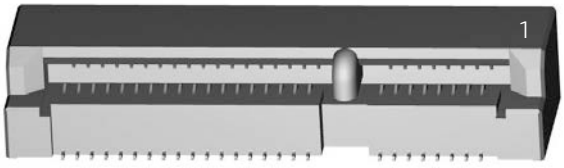


Table 33: Pin Assignment

Pin	Signal	Type
1	WAKE#	
2	+3V3	PWR
3	NC	NC
4	GND	PWR
5	NC	NC
6	+1.5V	PWR
7	CLKREQ#	
8	UIM_PWR	PWR
9	GND	PWR
10	UIM_DATA	NC
11	PCIE_mini CLK#	
12	UIM_CLK	NC
13	PCIE_mini CLK	
14	UIM_RESET	NC
15	GND	PWR
16	UIM_VPP	NC
17	UIM_IC_DM	NC
18	GND	PWR
19	UIM_IC_DP	
20	W_Disable#	
21	GND	PWR
22	RST#	
23	PCIE_RX-/SATA_RX-	

Pin	Signal	Type
24	+3V3	PWR
25	PCIE_RX+/SATA_RX+	
26	GND	PWR
27	GND	PWR
28	+1.5 V	PWR
29	GND	PWR
30	SMB_CLK	
31	PCIE_TX-/SATA_TX-	
32	SMB_DATA	
33	PCIE_TX+/SATA_TX+	
34	GND	PWR
35	GND	PWR
36	USBhub_D1_N	IO
37	GND	PWR
38	USBhub_D1_P	IO
39	+3V3	PWR
40	GND	PWR
41	+3V3	PWR
42	NC	NC
43	SATA_DET5#	
44	NC	NC
45	NC	NC
46	NC	NC
47	NC	NC
48	+1.5 V	PWR
49	NC	NC
50	GND	PWR
51	NC	NC
52	+3V3	PWR

6.25. PCIe x1 Connector (J17)

Figure 33: PCIe x1 Connector

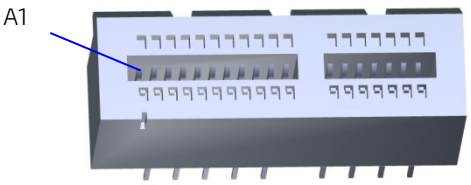


Table 34: PCIe x1

Pin	Side B Connector		Side A Connector	
#	Name	Description	Name	Description
1	+12v	+12 volt power	PRSNT#1	Hot plug presence detect
2	+12v	+12 volt power	+12v	+12 volt power
3	+12v	+12 volt power	+12v	+12 volt power
4	GND	Ground	GND	Ground
5	SMCLK	SMBus clock	JTAG2	TCK
6	SMDAT	SMBus data	JTAG3	TDI
7	GND	Ground	JTAG4	TDO
8	+3.3v	+3.3 volt power	JTAG5	TMS
9	JTAG1	+TRST#	+3.3v	+3.3 volt power
10	3.3Vaux	3.3v volt power	+3.3v	+3.3 volt power
11	WAKE#	Link Reactivation	PWRGD	Power Good
Mechanical Key				
12	RSVD	Reserved	GND	Ground
13	GND	Ground	REFCLK+	Reference Clock
14	HSOp(0)	Transmitter Lane 0,	REFCLK-	Differential pair
15	HSOn(0)	Differential pair	GND	Ground
16	GND	Ground	HSIp(0)	Receiver Lane 0,
17	PRSNT#2	Hotplug detect	HSIn(0)	Differential pair

6.26. RTC/Clear CMOS

Table 35: RTC/Clear CMOS Configurations

RTC_RST# / RTC_TEST#	DIS_SECCMOS	State
PIN 2 - 3 (open)	PIN 2 - 3 (open)	Default state
PIN 1 - 2 (short)	PIN 1 - 2 (short)	clear
RTC_RST# / RTC_TEST#	DIS_SECCMOS	state

7/ uEFI BIOS

7.1. Starting the uEFI BIOS

The pITX-APL is provided with a Kontron-customized, pre-installed and configured version of American Megatrends, Inc. (AMI). It is based on the Unified Extensible Firmware Interface (uEFI) specification and the Intel® Platform Innovation Framework for EFI. This uEFI BIOS provides a variety of new and enhanced functions specifically tailored to the hardware features of the pITX-APL.



The BIOS version covered in this document might not be the latest version. The latest version might have certain differences to the BIOS options and features described in this chapter.

The uEFI BIOS comes with a Setup program which provides quick and easy access to the individual function settings for control or modification of the uEFI BIOS configuration. The Setup program allows the accessing of various menus which provide functions or access to sub-menus with more specific functions of their own.

To start the uEFI BIOS Setup program, follow the steps below:

1. Power on the board.
2. Wait until the first characters appear on the screen (POST messages or splash screen).
3. Press the <DEL> key.
4. If the uEFI BIOS is password-protected, a request for password will appear. Enter either the User Password or the Supervisor Password (see Security menu), press <RETURN>, and proceed with step 5.
5. A Setup menu will appear.

The pITX-APL uEFI BIOS Setup program uses a hot key-based navigation system. A hot key legend bar is located on the bottom of the Setup screens.

The following table provides information concerning the usage of these hot keys.

Table 36: Navigation Hot Keys Available in the Legend Bar

Hotkeys	Description
<F1>	The <F1> key is used to invoke the General Help window.
<->	The<Minus> key is used to select the next lower value within a field.
<+>	The <Plus> key is used to select the next higher value within a field.
<F4>	The <F4> key is used to Exit saving Changes.
<F3>	The <F3> key is used to load Optimized Defaults.
<→> or <←>	The <Left/Right> arrows are used to select major Setup menus on the menu bar. For example: Main screen, Advanced screen, Security screen, etc.
<↑> or <↓>	The <Up/Down> arrows are used to select fields in the current menu. For example a Setup function or a sub-screen.
<ESC>	The <ESC> key is used to exit a Setup menu.
<ENTER>	The <ENTER> key is used to execute a command or select a submenu.

7.2. Setup Menus

The Setup utility features a selection bar at the top of the screen that lists the available menus:

1. Main
2. Advanced
3. Chipset
4. Security
5. Boot
6. Save & Exit

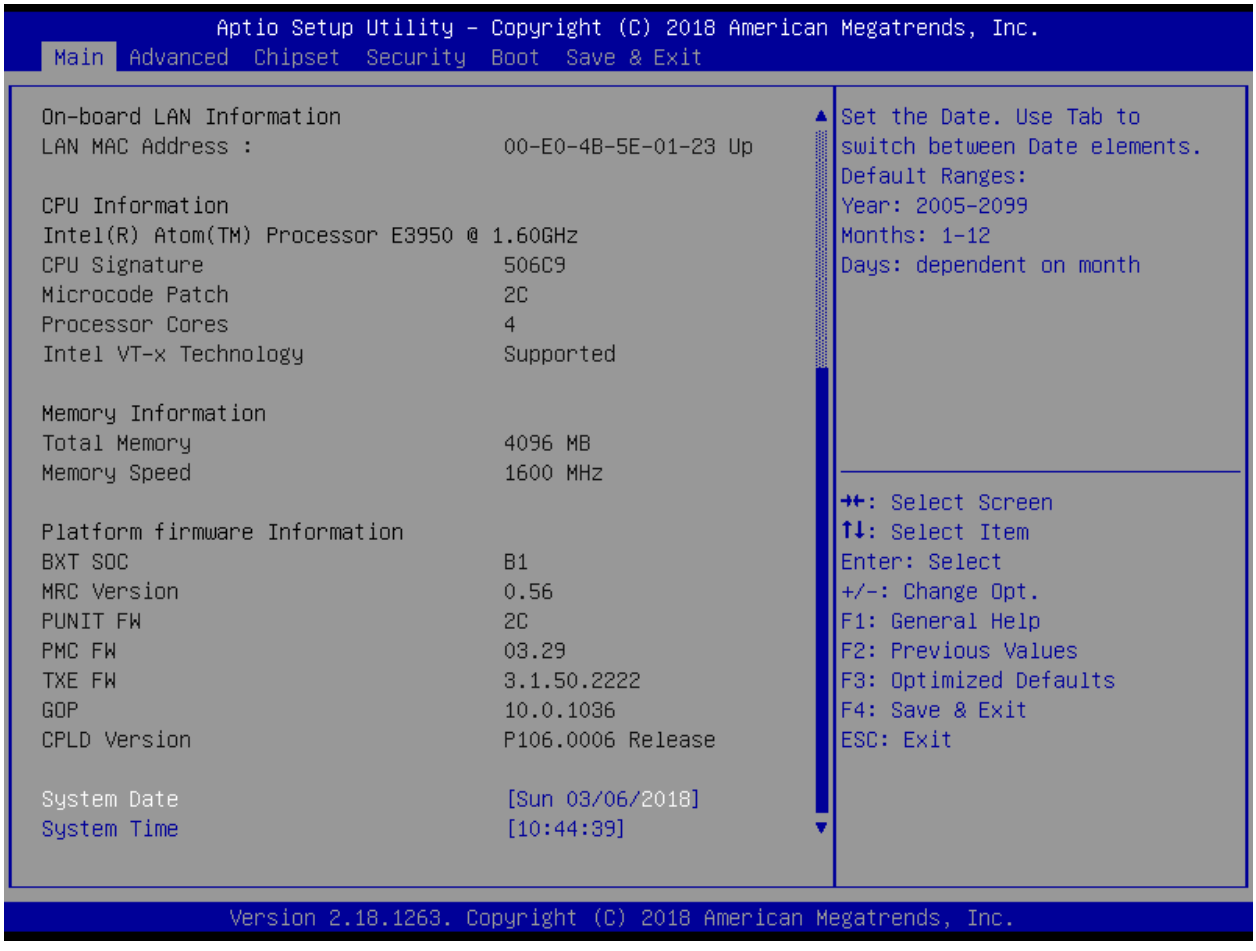
The currently active menu and the currently active uEFI BIOS Setup item are highlighted in white. Use the left and right arrow keys to select the Setup menus.

Each Setup menu provides two main frames. The left frame displays all available functions. Configurable functions are displayed in blue. Functions displayed in black provide information about the status or the operational configuration. The right frame displays a Help window providing an explanation of the respective function.

7.2.1. Main Setup Menu

On entering the uEFI BIOS, the Setup program displays the Main Setup menu. This screen lists basic system and board information.

Figure 34: Main Setup Menu Initial Screen



The following table shows Main sub-screens and functions, and describes the content. Default settings are in **bold**.

Table 37: Main Setup Menu Sub-screens

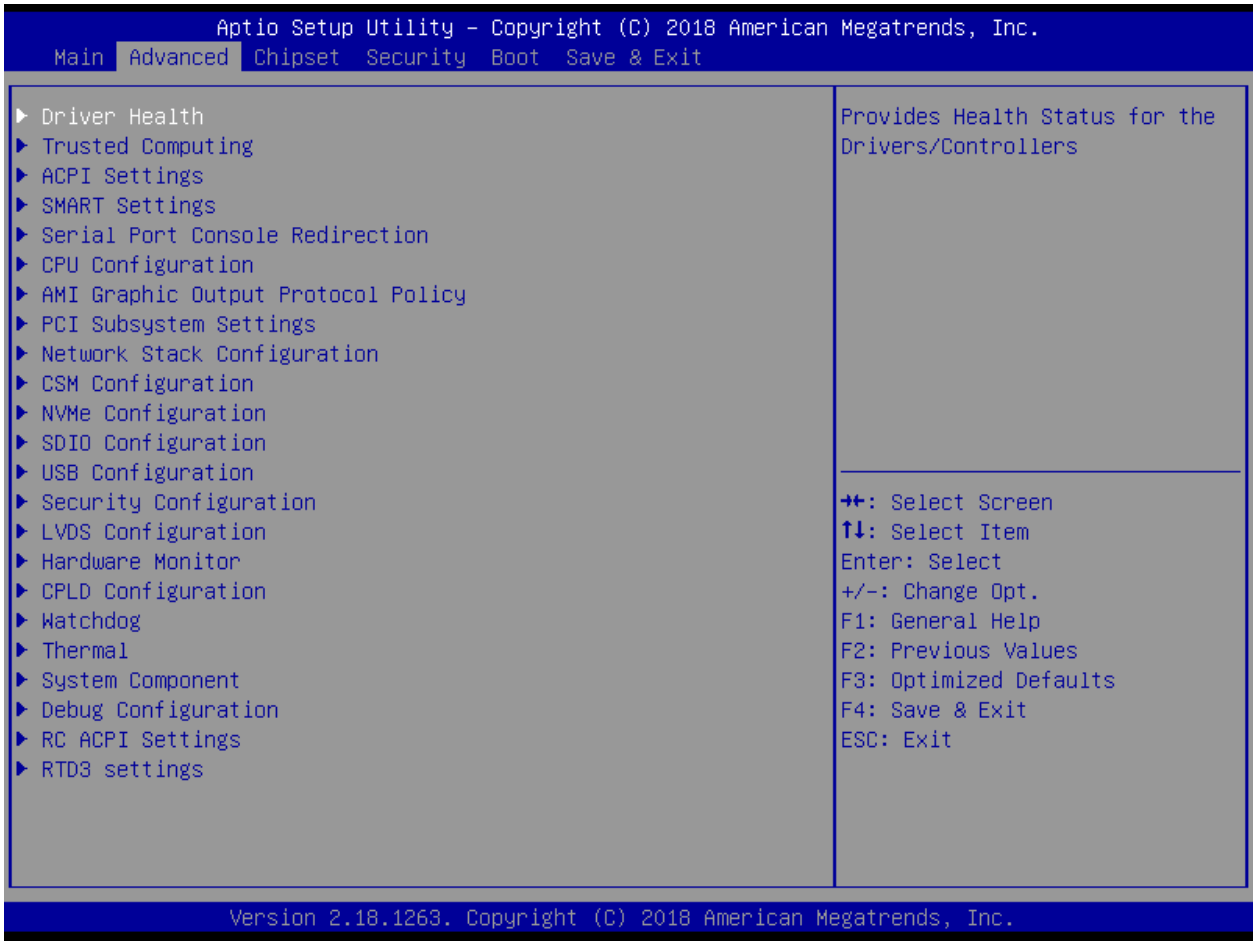
Sub-Screen	Function	Second level Sub-Screen / Description
BIOS Information	Read only field	
	Displays BIOS Information	
	Board Vendor, BIOS Version, Build Date and Time, Access Level	
Board Information	Read only field	
	Displays Board Information	
	Manufacturer, Product Name, PCB Version, Serial Number, Part Number, Boot Count	
On-board LAN Information	Read only field	
	Displays LAN MAC Address	
CPU Information	Read only field	
	Displays CPU Information	
Memory Information	Read only field	
	Displays Memory Information	
Platform firmware Information	Read only field	
	Displays Platform firmware Information	
System Date>	Sets the system date	
	[mm/dd/yyyy]	
System Time>	Sets the system time	
	[hh:mm:ss]	

7.2.2. Advanced Setup Menu

The Advanced Setup menu provides sub-screens and second level sub-screens with functions, for advanced configuration and Kontron specific configurations.

NOTICE Setting items, on this screen, to incorrect values may cause system malfunctions.

Figure 35: Advanced Setup Menu Initial Screen



The following table shows the Advanced sub-screens and functions and describes the content. Default settings are in **bold** and some functions include additional information. The function / submenu in *italic* indicate either status display or submenu string that cannot be selected. The underlined statement indicates the condition for the availability of the second-level submenu in reference to submenu.

Table 38: Advanced Setup menu Sub-screens and Functions

Sub-Screen	Function	Second level Sub-Screen / Description
Driver Health	*Intel® PRO/1000 7.0.06 PCI-E*	
Trusted Computing	*TPM20 Device Status, Vendor and Firmware Version.* Security Device Support **[Enable]**	When set to Enable: *Active PCR banks* *Available PCR banks*
		SHA-1 PCR Bank **[Enabled]**
		SHA256 PCR Bank **[Enabled]**
		Pending operation **[None]**
		Platform Hierarchy **[Enabled]**
		Storage Hierarchy **[Enabled]**
		Endorsement Hierarchy **[Enabled]**
		TPM2.0 UEFI Spec Version **[TCG_2]**
		Physical Presence Spec Version **[1.3]**
		TPM 20 InterfaceType [TIS]
		Device Select **[Auto]**
ACPI Settings	Enable ACPI Auto Configuration **(Disabled)**	When set to Disable: Enable Hibernation **[Enabled]** ACPI Sleep State **[S3 (Suspend to RAM)]** Lock Legacy Resources **[Disabled]**
SMART Settings	SMART Self Test **[Disabled]**	
Serial Port Console Redirection	Console Redirection (COM0) > **[Disabled]**	When set to Enabled: COM# Console Redirection Settings **[ANSI]** Bits per second **[115200]** Data Bits **[None]** Stop Bits **[1]** Flow Control **[None]** VT-UTF8 Combo Key Support **[Enabled]** Recorder Mode **[Disabled]** Resolution 100x31 **[Disabled]** Legacy OS Redirection Resolution **[80x24]** Putty KeyPad **[VT100]** Redirection After BIOS POST **[Always Enable]**
	Legacy Console Redirection Settings >	Legacy Serial Redirection Port [COM0]
	Serial Port for Out-of-Band Management / Windows Emergency Management Services (EMS) Console Redirection > **[Disabled]**	When set to Enabled: Console Redirection Settings > Out-of-Band Mgmt Port [COM0] Terminal Type **[VT-UTF8]** Bits per second **[115200]** Flow Control **[None]** Data Bits **[8]**

Sub-Screen	Function	Second level Sub-Screen / Description
		Parity **[None]** Stop Bits **[1]**
CPU Configuration	Turbo Mode **[Enabled]**	
	Intel Virtualization Technology **[Enabled]**	
	VT-d **[Disabled]**	
	Monitor Mwait **[Disabled]**	
AMI Graphic Output Control Policy	*Intel ® Graphics Controller* *Intel ® GOP Driver* Output select **[DP1]**	
PCI Subsystem Settings	*AMI PCI Driver Version* Above 4G Decoding **[Disabled]**	
	Hot-Plug Support **[Enabled]**	
Network Stack Configuration	Network Stack **[Disabled]**	
CSM Configuration	CSM Support **[Enabled]**	When set to Enabled: *CSM16 Module Version 07.79* GateA20 Active **[Upon Request]** INT19 Trap Response **[Immediate]** Boot option filter **[UEFI and Legacy]** *Option ROM execution* Network **[UEFI]** Storage **[UEFI]** Video **[UEFI]** Other PCI devices **[UEFI]**
NVMe Configuration	*NVME controller and Drive information*	
SDIO Configuration	SDIO Access Mode **[Auto]** *Mass Storage Devices:*	
USB Configuration	Legacy USB Support **[Enabled]**	
	XHCI Hand-off **[Enabled]**	
	USB Mass Storage Driver Support **[Enabled]**	
	USB transfer time-out **[20 sec]**	
	Device reset time-out **[20 sec]**	
	Device power-up delay **[Auto]**	
Security Configuration	TXE HMRFPO **[Disabled]**	
	TXE EOP Message **[Enabled]**	

Sub-Screen	Function	Second level Sub-Screen / Description
LVDS Configuration	LVDS Flat Panel Display Support **[Disabled]**	<u>When set to Enabled:</u> Panel Type **[Standard]** Resolution **[1024 x 768]** Panel Color Depth **[24-Bit VESA]** Panel Voltage **[3.3V]** Channel **[Dual]** Bus Swapping **[Normal]** Clock Frequency Center Spread **[Disabled]** Differential Output Swing Level **[300 mV]** Backlight **[Enable]** Backlight Signal Inversion **[Disable]** Backlight PWM Frequency **[200 Hz]** Brightness Level **[80%]**
Hardware Monitor	*Hardware Monitoring:* *CPU DTS Temperature (CPU MSR)* *PCB Temperature (TD1)* *NCT7802Y Temperature (LTD)* *LM75B Temperature (I2C0)* *NCT7802Y Voltage (VCC)* *RTC Voltage (VCORE)* *DDR Voltage (VSENS2)* *Input Voltage (VSENS3)*	
	CPU Fan: CPU Fan Pulse CPU Fan Control Mode **[SMART FAN IV]** Fan Trip Point Trip Point Speed	
CPLD Configuration	Serial Port 0 **[Enabled]**	<u>When set to Enabled:</u> Base Address **[3E8]** IRQ **[10]**
	GPIO IRQ **[Disabled]** I2C IRQ **[Disabled]**	
Watchdog	Auto-reload **[Disabled]**	
	Global Lock **[Disabled]**	
	Stage 1 mode **[Disabled]**	
Thermal	Automatic Thermal Reporting **[Disabled]**	<u>When set to Disabled:</u> Critical Trip Point **[125 C]** Passive Trip Point **[95 C]** Passive TC1 value 1 Passive TC2 value 5 Passive TSP value 10
System Component	OS Reset Select **[Cold Reset]**	
	Spread Spectrum Clocking Configuration	
	DDR SSC **[Enable]**	<u>When set to Enable:</u> DDR SSC Selection Table **[-0.5%]**

Sub-Screen	Function	Second level Sub-Screen / Description
	DDR SSC Bending Selection Table **[0% (No Clock Bending)]**	
	HighSpeed SerialIO SSC **[Enable]**	When set to Enable: HighSpeed SerialIO SSC Selection Table **[-0.5%]**
Debug Configuration	*Kernel Debugger Configuration* Kernel Debugger Enable **[Disabled]**	
	APEI BERT Configuration APEI BERT **[Enable]**	
	ACPI Memory Debug Switch ACPI Memory Debug **[Disable]**	
	TXE Debug Option End of Post **[Disable]** Lock Directory **[Disable]**	
	PTT Debug Option Suppress PTT Commands **[Disable]**	
	TDO GPIO Pin Switch TDO GPIO Pin **[Enable]** Max Memory 2G **[Disable]** Persistent RAM Size **[Disable]**	
	OS DnX OS DnX focus entry **[Disable]**	
	Processor Trace Configuration Processor Trace memory allocation **[Disable]**	
	CSE Data Clear Option CSE Data Clear (Yes / No)	
	Option to clear Data region during IFWI Update Capsule Data Clear **[Enable]**	
	NPK Debug Configuration >	North Peak Enable **[Auto]** FW Trace Enable **[Enable]** FW Trace Destination **[PTI]** NPK Recovery Dump **[Disable]** Memory Region 0 Buffer Size **[None]** Memory Region 0 Buffer WrapAround **[Wrap]** Memory Region 1 Buffer Size **[None]** Memory Region 1 Buffer WrapAround **[Wrap]** PTI Mode **[X4]** PTI Training **[Off]** PTI Speed **[Quarter Speed]**

Sub-Screen	Function	Second level Sub-Screen / Description
		Punit Message Level **[LEVEL LOW]** PMC Message Level **[LEVEL LOW]**
RC ACPI Settings	Native PCIE Enable **[Enable]**	
	Native ASPM **[Enable]**	
RTD3 Settings	RTD3 Support **[Disable]**	

7.2.3. Chipset Setup Menu

The Chipset Setup menu provides sub-screens, second level and third level sub-screens with functions, for Intel Chipset configurations.

Figure 36: Chipset Setup Menu Initial Screen

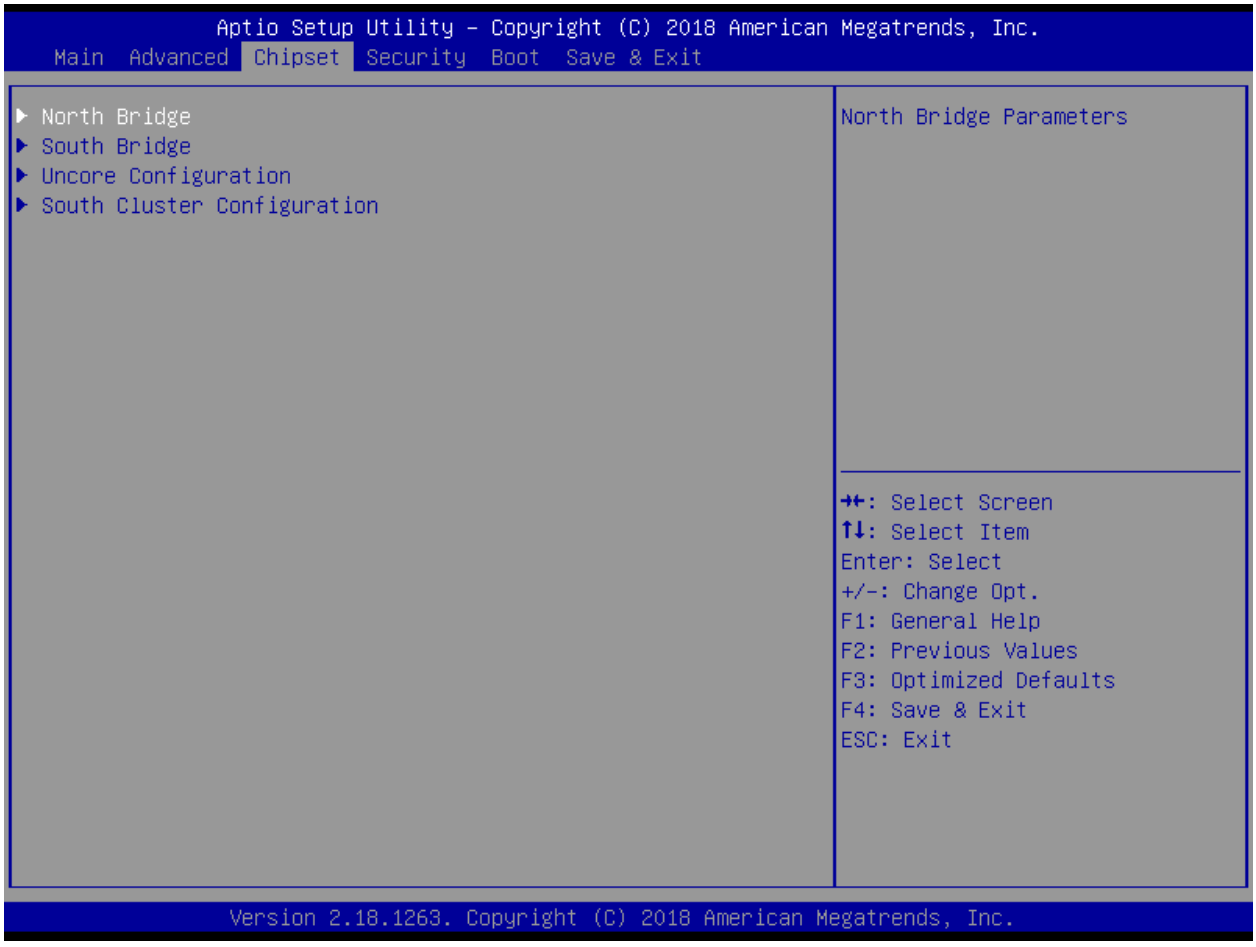


Table 39: Chipset Setup menu Sub-screens and Functions

Sub-Screen	Function	Second level Sub-Screen / Description
North Bridge	Max TOLUD **[2 GB]** PCIE VGA Workaround **[Disable]**	
South Bridge	Serial IRQ Mode **[Continuous]**	
	SMBus Support **[Enabled]**	

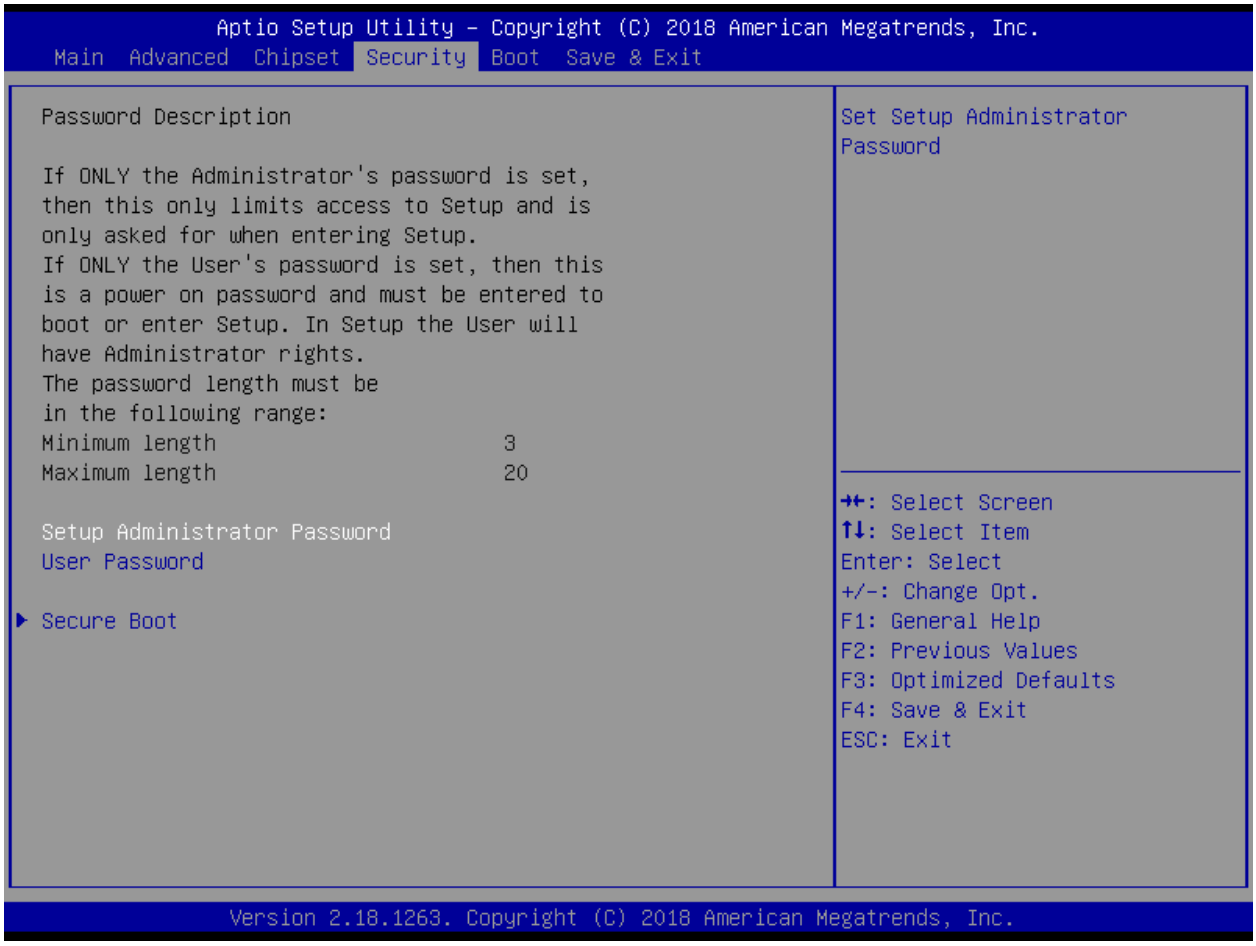
Sub-Screen	Function	Second level Sub-Screen / Description
	OS Selection **[Windows 10 (Ver>=167)]**	
	PCI Clock Run **[Enable]**	
	Real Time Option **[RT Disable]**	
Uncore Configuration	*GOP Configuration* GOP Driver **[Enable]** Intel Graphics Pei Display PEIM **[Disable]** GOP Brightness Level **[140]**	
	IGD Configuration Integrated Graphics Device **[Enable]** Primary Display **[IGD]** RC6 (Render Standby) **[Disable]** GTT Size **[8MB]** Aperture Size **[256MB]** DVMT Pre-Allocated **[64M]** DVMT Total Gfx Mem **[256M]** Cd Clock Frequency **[624 MHz]** GT PM Support **[Enable]** PAVP Enable **[Enable]**	
	IGD – LCD Control BIA **[Auto]** ALS Support **[Enable]** IGD Flat Panel **[Auto]** IGD Boot Type **[Auto]** Panel scaling **[Auto]** GMCH BLC Control **[PWM-Inverted]**	
South Cluster Configuration	*HD-Audio Configuration >*	HD-Audio Support **[Enable]**
	LPSS Configuration >	*Low Power Sub System* LPSS HSUART #3 Support (D24:F2) **[Enable]** LPSS SPI #1 Support (D25:F0) **[Enable]** LPSS IOSF PMCTL SOix Enable **[Enable]**
	PCI Express Configuration >	*PCI Express Configuration* PCI Express Clock Gating **[Enable]** Port8xh Decode **[Disable]** Peer Memory Write Enable **[Disable]** Compliance Mode **[Disable]** > PCIe #0 BDF[00:13:00] LAN 1 > PCIe #1 BDF[00:13:01] mPCIe <u>When PCIE #X is enabled:</u> PCIe #X BDF[XX:XX:XX] **[Auto]** ASPM **[Disable]** L1 Substates **[L1.1 & L1.2]** ACS **[Enable]** URR **[Disable]** FER **[Disable]** NFER **[Disable]** CER **[Disable]** CTO **[Default Setting]** SEFE **[Disable]** SENFE **[Disable]** SECE **[Disable]** PME SCI **[Enable]** Hot Plug **[Disable]** PCIE Speed **[Auto]** Transmitter Half Swing **[Disable]** *Extra Bus Reserved 0* *Reserved Memory 10* *Reserved I/O 4*

Sub-Screen	Function	Second level Sub-Screen / Description
		PCH PCIE LTR **[Enable]** Snoop Latency Override **[Auto]** Non Snoop Latency Override **[Auto]** PCIE LTR Lock **[Disable]** PCIE Selectable De-emphasis **[Enable]**
	SATA Drives >	*SATA Drives* *Chipset-SATA Controller Configuration* *SATA Port 0* Port 0 **[Enable]** SATA Port 0 Hot Plug Capability **[Disable]** *SATA Port 1 (mSATA)* Port 0 **[Enable]** SATA Port 0 Hot Plug Capability **[Disable]**
	SCC Configuration >	SCC SD Card Support (D27:F0) **[Enable]**
	USB Configuration >	USB Port Disable Override **[Disable]** XHCI Disable Compliance Mode **[FALSE]**
	Miscellaneous Configuration >	State After G3 **[S0 State]** Power Button Debounce Mode **[Enable]** Wake on LAN **[Disable]** BIOS Lock **[Disable]** RTC Lock **[Enable]** TCO Lock **[Disable]** DCI Enable (HDCIEN) **[Disable]** DCI Auto Detect Enable **[Enable]** GPIO Lock **[Disable]**

7.2.4. Security Setup Menu

The Security Setup menu provides information about the passwords and functions for specifying the security settings. The passwords are case-sensitive.

Figure 37: Security Setup Menu Initial Screen



The following table shows Security sub-screens and functions.

Table 40: Security Setup Menu Functions

Function	Description
Setup Administrator Password User Password	Create / change password to enter Setup
HDD Security Configuration	Create / change password to allow access to Set, Modify and Clear HardDisk User and Master Passwords for Enabling Security.
Attempt Secure Boot **[Disable]**	Enable or Disable the Secure Boot support. Please also set Secure Boot Mode to "Standard" to install standard Microsoft Platform Key (PK).
Secure Boot Mode	Set Secure Boot Mode to "Standard" to boot standard Windows or Linux boot loader signed with Microsoft's platform key. Select "Customized" mode only if you have a custom OS with OS boot loader signed with your own platform key. Kontron provide services for Customized Secure Boot, visit Kontron SEC-Line home

Function	Description
	page https://www.kontron.com/products/solutions/security/sec-line.html for more information.
Key Management	Enables expert users to modify Secure Boot Policy Variables without full authentication.

If only the administrator's password is set, then only access to the setup is limited and is requested when entering the setup.

If the user's password is set, then the password is a power on password and must be entered to boot or enter setup. In the setup the user has restricted rights.

7.2.5. Remember the Password

It is highly recommended to keep a record of all passwords in a safe place. Forgotten passwords result in the user being locked out of the system.

If the system cannot be booted because the User Password or the Supervisor Password are not known, contact Kontron Support for further assistance.

7.2.6. Boot Setup Menu

The Boot Setup menu lists dynamically generated boot device priority order.

Figure 38: Boot Setup Menu Initial Screen



The following table shows Boot sub-screens and functions, and describes the content. Default settings are in **bold**.

Table 41: Boot Setup Menu Functions

Function	Description
Boot Configuration Setup Prompt Timeout **1** Bootup NumLock State **[On]** Quiet Boot **[Enabled]**	
Boot Option Priorities Boot Option #1 Boot Option #2 Boot Option #3 Boot Option #4 Fast Boot **[Enable]** SATA Support VGA Support USB Support	To set the system boot order. Use +/- keys to change option. When Fast Boot is Enabled, SATA, VGA, USB, PS2 support, devices initialization, Network Stack driver can be customized.

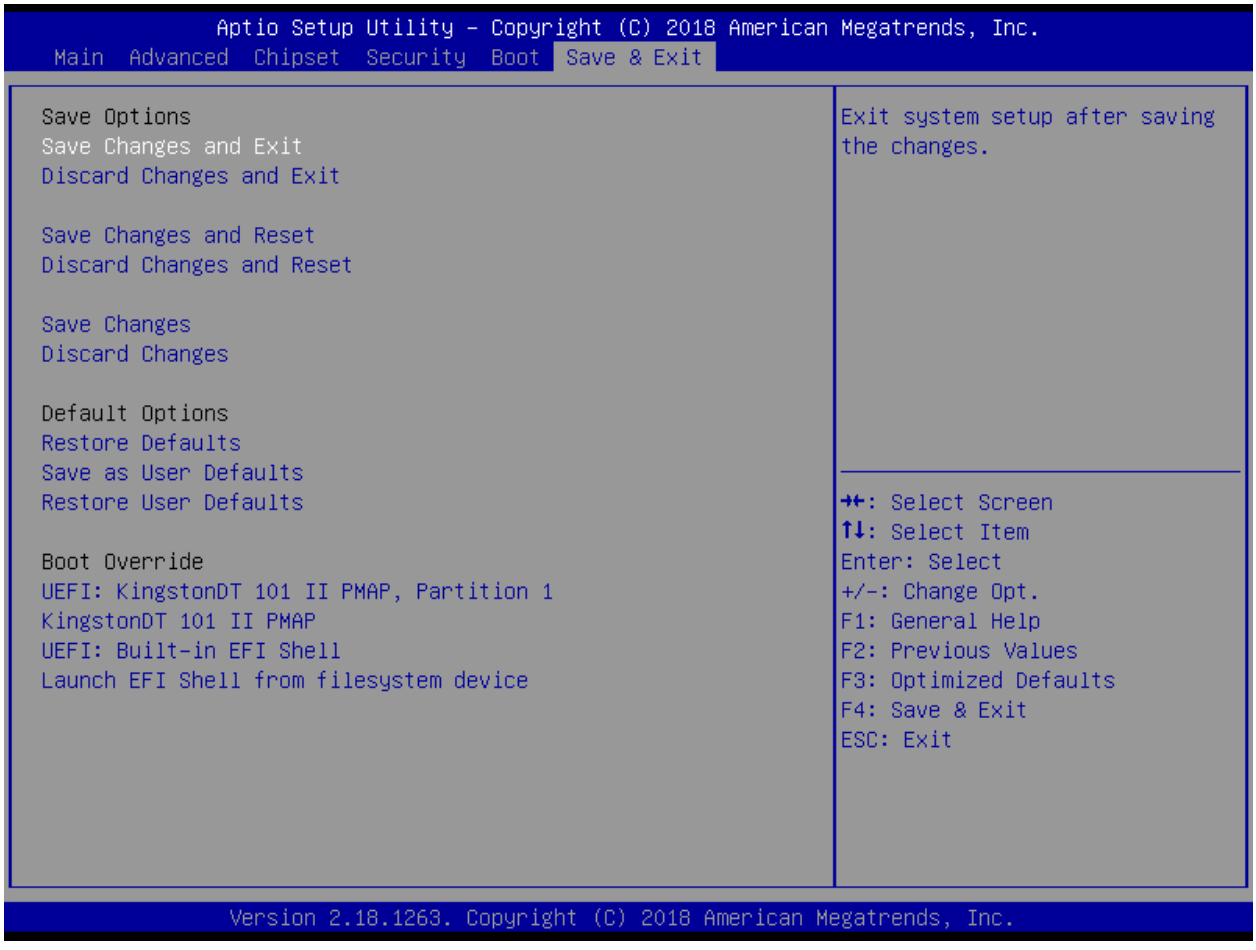
Function	Description
PS2 Support Network Stack Driver Support Redirection Support	
New Boot Option Policy	Controls the placement of newly detected UEFI boot options
Hard Drive BBS Priotities	Sets the placement of legacy boot options

7.2.7. Exit Setup Menu

The Save and Exit Setup menu provides functions for handling changes made to the uEFI BIOS settings and exiting the Setup program.

If system cannot boot or work properly due to incorrect setting, shorting Pin-1 and Pin-2 on J15 jumper will load the default setting of BIOS upon power cycle. Once safely booted with default setting, you may undo the jumper setting to save new changes on BIOS Setup Menu.

Figure 39: Save and Exit Setup Menu Initial Screen



The following table shows the Exit menu sub-screens and functions, and describes the content.

Table 42: Save and Exit Setup Menu Functions

Function	Description
Save Options Save Changes and Exit Discard Changes and Exit Save Changes and Reset Discard Changes and Reset *Default Options* Restore Defaults Save as User Defaults Restore User Defaults	
Boot Override UEFI: Built-in EFI Shell Launce EFI Shell from filesystem device	

7.3. The uEFI Shell

The Kontron uEFI BIOS features a built-in and enhanced version of the uEFI Shell. For a detailed description of the available standard shell scripting, refer to the EFI Shell User Guide. For a detailed description of the available standard shell commands, refer to the EFI Shell Command Manual. Both documents can be downloaded from the EFI and Framework Open Source Community homepage (http://sourceforge.net/projects/efi-shell/files/documents/).

Kontron uEFI BIOS does not provide all shell commands described in the EFI Shell Command Manual. If Secure Boot is enabled, the UEFI shell may not be able to be entered.

7.3.1. Basic Operation of the uEFI Shell

7.3.1.1. Entering the uEFI Shell

To enter the uEFI Shell, follow the steps below:

1. Power on the board.
2. Press the <F7> key (instead of <DEL>) to display a choice of boot devices.
3. Choose 'UEFI: Built-in EFI Shell'.

```
EFI Shell version 2.50 [5.12]
Current running mode 1.1.2
Device mapping table
fs0        :Removable HardDisk - Alias hd18c0b blk0
        PciRoot(0x0)/Pci(0x15,0x0)/USB(0x2,0x0)/HD(1,MBR,0x0002B27D,0x3F,0x785BEC)
blk0    :Removable HardDisk - Alias hd18c0b fs0
        PciRoot(0x0)/Pci(0x15,0x0)/USB(0x2,0x0)/HD(1,MBR,0x0002B27D,0x3F,0x785BEC)
blk1    :Removable BlockDevice - Alias (null)
        PciRoot(0x0)/Pci(0x15,0x0)/USB(0x2,0x0)
```

Press the ESC key within 5 seconds to skip startup.nsh, and any other key to continue.

4. The output produced by the device-mapping table can vary depending on the board's configuration.
5. If the ESC key is pressed before the 5 second timeout elapses, the shell prompt is shown:

```
Shell>
```

7.3.1.2. Exiting the uEFI Shell

To exit the uEFI Shell, follow one of the steps below:

1. Use the **exit** uEFI Shell command to select the boot device, in the Boot menu, that the OS will boot from.
2. Reset the board using the **reset** uEFI Shell command.

7.4. uEFI Shell Scripting

7.4.1. Startup Scripting

If the ESC key is not pressed and the timeout has run out then the uEFI Shell tries to execute some startup scripts automatically. It searches for scripts and executes them in the following order:

1. Initially searches for Kontron flash-stored startup script.
2. If there is no Kontron flash-stored startup script present then the uEFI-specified **startup.nsh** script is used. This script must be located on the root of any of the attached FAT formatted disk drive.
3. If none of the startup scripts are present or the startup script terminates then the default boot order is continued.

7.4.2. Create a Startup Script

Startup scripts can be created using the uEFI Shell built-in editor edit or under any OS with a plain text editor of your choice. To create a startup shell script, simply save the script on the root of any FAT-formatted drive attached to the system.

7.4.3. Examples of Startup Scripts

7.4.3.1. Execute Shell Script on other Harddrive

This example (s**tartup.nsh**) executes the shell script named **bootme.nsh** located in the root of the first detected disc drive (**fs0**).

```
fs0:
bootme.nsh
```

7.5. Firmware Update

Firmware updates are typically delivered as a ZIP archive containing only the firmware images. The content of the archive with the directory structure must be copied onto a data storage device with FAT partition.

7.5.1. Updating Procedure

BIOS can be updated with the Intel tool fpt64.efi using the procedure below:

1. Copy these files to an USB stick.
   - flash.nsh or flash_with_fpt.nsh (if available)
   - fpt.efi
   - fparts.txt
   - pITX_APL_BIOS_Ver_<xxx>……bin (where xxx stands for the version #)

Start the system into the uEFI shell (see chapter 7.3.1.1 "Entering the uEFI Shell").

2. Change to the drive representing the USB stick.

```
fsx:   (x = 0, 1, 2, etc. represents the USB stick)
```

Change to the directory where you copied the flash tool.

```
cd <your_directory>
```

3. Start flash.nsh or flash_with_fpt.nsh (if available)

OR type

```
fpt -y -f pITX_APL_BIOS_Ver_<xxx>……bin
```

4. Wait until flashing is successful and then power cycle the board.



Do not switch off the power during the flash process!

8/ Technical Support

For technical support contact our Support department:

E-mail: support@kontron.com
Phone: +49-821-4086-888

Make sure you have the following information available when you call:

Product ID Number (PN),
Serial Number (SN)



The serial number can be found on the Type Label, located on the product's rear side.

Be ready to explain the nature of your problem to the service technician.

8.1. Warranty

Due to their limited service life, parts that by their nature are subject to a particularly high degree of wear (wearing parts) are excluded from the warranty beyond that provided by law. This applies to the CMOS battery, for example.



If there is a protection label on your product, then the warranty is lost if the product is opened.

8.2. Returning Defective Merchandise

All equipment returned to Kontron must have a Return of Material Authorization (RMA) number assigned exclusively by Kontron. Kontron cannot be held responsible for any loss or damage caused to the equipment received without an RMA number. The buyer accepts responsibility for all freight charges for the return of goods to Kontron's designated facility. Kontron will pay the return freight charges back to the buyer's location in the event that the equipment is repaired or replaced within the stipulated warranty period. Follow these steps before returning any product to Kontron.

1. Visit the RMA Information website:
http://www.kontron.com/support-and-services/support/rma-information

   Download the RMA Request sheet for **Kontron Europe GmbH** and fill out the form. Take care to include a short detailed description of the observed problem or failure and to include the product identification Information (Name of product, Product number and Serial number). If a delivery includes more than one product, fill out the above information in the RMA Request form for each product.

2. Send the completed RMA-Request form to the fax or email address given below at Kontron Europe GmbH. Kontron will provide an RMA-Number.

   Kontron Europe GmbH
   RMA Support
   Phone: +49 (0) 821 4086-0

Fax: +49 (0) 821 4086 111
Email: service@kontron.com

3. The goods for repair must be packed properly for shipping, considering shock and ESD protection.



Goods returned to Kontron Europe GmbH in non-proper packaging will be considered as customer caused faults and cannot be accepted as warranty repairs.

4. Include the RMA-Number with the shipping paperwork and send the product to the delivery address provided in the RMA form or received from Kontron RMA Support.

List of Acronyms

BSP	Board Support Packages
DP	Display Port
ECC	Error Checking and Correction
eDP	Embedded Display Port
GPIO	General Purpose In-Output
mITX	Mini ITX
PCIe	PCI-Express
RTC	Real Time Clock
SKUs	Stockkeeping Units
SPI	Serial Peripheral Interface
TPM	Trusted Platform Module

About Kontron

Kontron is a global leader in Embedded Computing Technology (ECT). As a part of technology group S&T, Kontron offers a combined portfolio of secure hardware, middleware and services for Internet of Things (IoT) and Industry 4.0 applications. With its standard products and tailor-made solutions based on highly reliable state-of-the-art embedded technologies, Kontron provides secure and innovative applications for a variety of industries. As a result, customers benefit from accelerated time-to-market, reduced total cost of ownership, product longevity and the best fully integrated applications overall.

For more information, please visit: **http://www.kontron.com/**

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