JRex-CE



Intel®
Communications
Alliance
Associate Member
SILVER

Product Manual

Document Revision 1.1

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1. USER INFORMATION

1.1 About This Manual

This document provides information about products from Kontron Embedded Computers AG and/or ist subsidiaries. No warranty of suitability, purpose, or fitness is implied.
While every attempt has been made to ensure that the information in this document is accurate, the information contained within is supplied “as-is” and is subject to change without notice.
For the circuits, descriptions and tables indicated, Kontron assumes no responsibility.

1.2 JUMPtec® Brand

JUM*Ptec* Industrielle Computertechnik AG and Kontron Embedded Computers AG merged in July 2002. JUM*Ptec* is now known as Kontron Embedded Modules GmbH.
Products labeled and sold under the Kontron Embedded Modules name (formerly JUM*Pte*c) are now considered Kontron products for all practical purposes, including warranty and support.
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1.3 Copyright Notice

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1.4 Trademarks

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- IBM, XT, AT, PS/2 and Personal System/2 are trademarks of International Business Machines Corp.
- Microsoft is a registered trademark of Microsoft Corp.
- All other products and trademarks mentioned in this manual are trademarks of their respective owners.

1.5 Standards

Kontron Embedded Modules is certified to ISO 9000 standards.

1.6 Warranty

This Kontron Embedded Modules product is warranted against defects in material and workmanship for the warranty period from the date of shipment. During the warranty period, Kontron Embedded Modules will at its discretion decide to repair or replace defective products.

Within the warranty period, the repair of products is free of charge as long as warranty conditions are observed.
You may receive a bill for test costs if Kontron Embedded Modules finds no fault with the product. You also may receive a bill for repairs if a product's warranty has expired.
For warranty service or repair, return the product to a Kontron Embedded Modules service facility listed in the Technical Support section of this document.
The warranty does not apply to defects resulting from improper or inadequate maintenance or handling by the buyer, unauthorized modification or misuse, operation outside of the product's environmental specifications or improper installation or maintenance.
Kontron Embedded Modules will not be responsible for any defects or damages to other products not supplied by Kontron Embedded Modules that are caused by a faulty Kontron Embedded Modules product.

1.7 Technical Support

Technicians and engineers from Kontron Embedded Modules and/or ist subsidiaries are available for technical support. We are committed to making our product easy to use and will help you use our products in your systems. Before contacting Kontron Embedded Modules technical support, please consult our **Web site** for the latest product documentation, utilities, and drivers. If the information does not help solve the problem, contact us by email or telephone. The table below lists technical support contacts and service facilities for Kontron Embedded Modules.

Asia	Europe	North/South America
Kontron Asia	**Kontron Embedded Modules**	**Kontron Americas**
5F-1, 341, Sec 4 Chung Hsiao E. Road Taipei, Taiwan	Brunnwiesenstr. 16 94469 Deggendorf – Germany	3988 Trust Way Hayward, CA 94545
Tel: +886 2 2751 7192	Tel: +49 (0) 991-37024-0	Tel: 510-732-6900
Fax: +886 2 2772 0314	Fax: +49 (0) 991-37024-104	Fax: 510-732-7655
http://www.jumptec.com.tw/ http://www.kontron.com.tw/	http://www.jumptec.de/ http://www.kontron-em.de/	http://www.kontron.com/
		techsupport@jumptec.com

2. INTRODUCTION

JRex-CE is a member of the Kontron Embedded Modules' 3.5" board family. JRex modules feature the same pinout and interface for the following components and peripherals:

- Reset- and powerbutton with Harddisk- and LAN LED (Accessory)
- ATX or 5V-only power
- 2xUSB 2.0
- 10 / 100BaseT Ethernet
- Keyboard/Mouse combiconnector
- CompactFlash
- VGA
- RS232 serial port
- LPT
- FDC
- IDE

These family features allow you to re-use chassis and maximize design re-use.
The JRex-CE hosts a ULV Intel® Celeron® processor.
A SDRAM-DIMM socket for up to 512MB allows you to use standard PC100 or PC133 DIMM memory modules.
The compatible features allow easy upgrades within the JRex product family.
Display connections (24 bit TFT) are simplified by using the JUMPtec Intelligent LVDS Interface (JILI), which automatically recognizes the display that is connected and independently sets all video parameters. All JRex are plug-and-work enabled.

JRex-CE are tested with Windows 9x/ Me, Windows NT4, Windows 2000, Windows XP and Linux. For other OS please contact your OS distributor for supporting this chipset.
It's strictly recommended to use the latest chipset drivers for your OS !

3. SPECIFICATIONS

3.1 Functional Specifications

- **Processor:**
  ULV Intel® Celeron® @ 400MHz or LV Intel® Celeron® @ 733MHz
- **Chipset:**
  Intel® 815E Chipset graphics memory controller hub
- **Super I/O:**
  Winbond W83627HF
- **Memory:**
  One 168-pin DIMM 3.3V SDRAM, up to 512MB
- **Serial Port:**
  COM1 RS232
- **Parallel Port:**
  LPT1 Enhanced Parallel Port (EPP) and Extended Capabilities Port (ECP) with bi-directional capability
- **Floppy port**
- **EIDE port**
  (Enhanced Intelligent Drive Electronics): Two Peripheral Component Interconnect (PCI) Bus Master, IDE port support: Ultra 100 Direct Memory Access (UDMA100) mode
- **Universal Serial Bus (USB):**
  2 USB 2.0 ports
  USB legacy keyboard support
  USB floppy-, CDROM-, USB stick boot support
- **Onboard Ethernet:**
  integrated Intel® 82562 10/100BASE-T LAN
- **Onboard VGA:**
  Intel® 815E Chipset graphics memory controller hub
- **Audio:**
  Integrated Intel® SoundBlaster™ AC97, Windows Sound System™ compatible
- **BIOS:**
  Phoenix™
- **NV-EEPROM** for CMOS-setup retention w/o battery
- **PS/2 keyboard and mouse** controller
- **Watchdog** timer (WDT)
- **Real-time clock** with battery onboard

3.2 Mechanical Specifications

Mechanical: 101,6mm x 147,3mm (4.0" x 5.8")

3.3 Electrical Specifications

3.3.1 Supply Voltage

5V DC +/- 5%

3,3V DC +/- 5%

5V DC Standby +/- 5%

12V, -12V, -5V ... not used

3.3.2 Supply Voltage Ripple

100 mV peak to peak 0-20 MHz

3.3.3 Typical Supply Current

- ATX Version, Celeron 733MHz, 512MB SDRAM, 96MB CF-card

  140 mA @ 5V Standby
  1,33 A @ 5V
  2,55 A @ 3.3V

- ATX Version, Celeron 400MHz, 512MB SDRAM, 96MB CF-card

  140 mA @ 5V Standby
  1,05 A @ 5V
  2,10 A @ 3.3V

- 5V-only Version, Celeron 733MHz, 512MB SDRAM, 96MB CF-card

  3,16 A @ 5V

- 5V-only Version, Celeron 400MHz, 512MB SDRAM, 96MB CF-card

  1,97 A @ 5V

3.3.4 RTC Battery

Real-time clock (RTC) battery voltage: 1.8 - 4.0V (typ. 3.0V)

RTC battery quiescent current: max. 3,5uA @ 3.0 V

CAUTION TEXTS CONCERNING LITHIUM BATTERIES

English:
CAUTION ! **Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.**

Deutsch:
VORSICHT ! **Explosionsgefahr bei unsachgemäßem Austausch der Batterie. Ersatz nur durch den selben oder einen vom Hersteller empfohlenen gleichwertigen Typ. Entsorgung gebrauchter Batterien nach Angaben des Herstellers.**

Danish:
ADVARSEL ! **Lithiumbatteri – Ekspiosionsfare ved fejlagtig håandtering. Udskifting må kun ske med batteri af samme fabrikat og type. Lever det brugte batteri tilbage til leveradøren.**

Norwegian:
ADVARSEL ! **Eksplosjonsfare ved feilaktlg skifte av batteri. Benytt samme batteritype eller en tilsvarende type anbefalt av apparatfabrikanten. Brukte batterier kasseres I hendhold til fabrikantens instruksjoner.**

Swedish:
VARNING ! **Explosionsfara vid felaktigt batteribyte. Anvãnd samma batterityp eller en ekvivalent typ som rekommenderas av apparattillverkaren. Kassera anvãnt batteri enligt fabrikantens instruktion.**

Finnish:
VAROITUS ! **Paristo voi rãjähtãã, jos se on virheellisesti asennettu. Vaihda paristo ainoastaan laltevalmistajan suosittelmaan tyyppiln. Havita kaytetty paristo valmistajan ohjeiden mukaisesti.**

3.4 Environmental Specifications

3.4.1 Temperature

operating 0 to +60 °C ((*)with appropriate airflow))

Intel® Celeron® is specified for proper operation when junction temperature is within the specified range of 0°C to 100°C.

Intel® 815E Chipset temperature max. 100°C

Intel® ICH4 I/O Controller Hub 4 (82801DB) case temperature max. 110°C

Nonoperating: -10 to + 85 ° C

(*) The maximum operating temperature is the maximum measurable temperature on any spot on the modules´s surface. It is the user´s responsibility to maintain this temperature within the above specification.

JRex-CE has an overtemperature protection. The sytem is automatically switching off on 115 °C CPU temperature. For other temperature control features refer the „ACPI Control“ Menu at the „Power“ Menu at the BIOS Setup.

3.4.2 Humidity

Operating:	10% to 90% (noncondensing)
Nonoperating:	5% to 95% (noncondensing)

4. CPU AND CHIPSET

4.1 Intel® Celeron® CPU

- Supports the Intel Architecture with Dynamic Execution
- On-die primary 16-Kbyte instruction cache and 16-Kbyte write-back data cache
- On-die second level cache (256-Kbyte) with Advanced Transfer Cache Architecture
- Data Prefetch Logic
- Integrated math co-processor
- Support for MMX™ technology
- Support for Streaming SIMD Extensions
- Power Management Features Quick Start, Deep Sleep and Deeper Sleep modes provide low power dissipation

4.2 Intel® 815E Chipset GMCH

Processor/Host Bus Support
- Intel® Pentium® III processor and Intel® Celeron®
- Supports processor 370-Pin Socket
- Supports 32-Bit System Bus Addressing
- 4 deep in-order queue; 4 or 1 deep request queue
- In-order and Dynamic Deferred Transaction Support
- 66/100/133MHz System Bus Frequency
- GTL+ I/O Buffer

Integrated SDRAM Controller
- 32 MB to 512 MB using 16Mb/64Mb/128Mb/256Mb technology
- 64-bit data interface
- 100/133 MHz system memory bus frequency
- Support for Asymmetrical SDRAM addressing only
- Support for x8 and x16 SDRAM device width
- Unbuffered, Non-ECC SDRAM only supported
- Refresh Mechanism: CBR ONLY supported
- Enhanced Open page arbitration SDRAM paging scheme

Power Management Functions
- Stop Clock Grant and Halt special cycle translation from the host to the hub interface
- ACPI Compliant power management
- APIC Buffer Management

Integrated Graphics Controller
- 3D Hyper Pipelined Architecture
- Full 2D H/W Acceleration
- Motion Video Acceleration
- Mip Maps with Trilinear and Anisotropic Filtering
- 85 MHz Flat Panel Monitor/Digital CRT Interface Or Digital Video
- Integrated 24-bit 230 MHz RAMDAC
- Gamma Corrected Video
- DDC2B Compliant
- Up to 1600x1200 in 8-bit Color at 85 Hz Refresh
- Hardware Accelerated Functions
- 3 Operand Raster BitBLTs
- 64x64x3 Color Transparent Cursor

5. SYSTEM MEMORY

5.1 Memory Socket

The JRex-CE uses one standard 168 pin SDRAM memory module.

Supported devices on module: 16-Mbit, 64-Mbit, 128-Mbit, and 256-Mbit technologies chips

6. USB INTERFACE

The JRex-CE comes with two USB 2.0 ports, which you can expand by adding external hubs. You can connect up to 127 USB peripherals.

6.1 USB Connectors

Pin	Pin Function
1	USB1_+5V
2	USB1**-**
3	USB1**+**
4	USB1_GND

Note: The current of each power lines is internal limited to 500mA by a resetable fuse.

6.2 Driver, Configuration

For the USB Port at the JRex-CE just enable USB UHCI Host Controller 1 (default value is Enabled). For additional USB Ports at JFLEX Extension cards enable USB UHCI Host Controller 2 (default value is Disabled).

Importand Note: some OS without USB 2.0 support doesnt working well with USB 2.0. If you install your OS at JRex-CE please disable the USB 2.0 support at setup at first (Default Value is Disabled). After the full install process you can enable the USB 2.0 controller like the description below.

For USB 2.0 installation just

- Be sure to enable @ BIOS setup, "Advanced" - "I/O Device Configuration" - "USB EHCI Host Controller" the USB 2.0 functionality.

- install the USB 2.0 driver –
  just type "usb2.0.exe" on http://downloadfinder.intel.com) for Windows98SE , WindowsME, Windows 2000 and Windows XP

- for other OS please contact your OS distributor for a USB 2.0 driver; we are not able by law to ship USB 2.0 driver ...

7. SERIAL-COMMUNICATION INTERFACE

The JRex-CE has two 16550-compatible serial ports.

The line drivers of COM-A conform to the IEEE RS232C standard. This port is accessible through a 9-pin DSUB connector.

COM-B features TTL level signals on an internal micro pin header. To have the signals available on the standard serial interface connectors DSUB9 or DSUB25, an adapter cable is required. A 9-pin DSUB cable is available from Kontron (KAB-DSUB9-3, Part Number 96061-0000-00-0).

7.1 Serial Connectors

COM-A (RS232C)	
Pin	**DSUB-9**
1	DCD
2	RxD
3	TxD
4	DTR
5	GND
6	DSR
7	RTS
8	CTS
9	RI

COM-B (TTL)	
Pin	**Molex 53047-1010**
1	DCD
2	DSR
3	RxD
4	RTS
5	TxD
6	CTS
7	DTR
8	RI
9	GND
10	VCC (+5V)

7.2 Configuration

See BIOS Setup.

8. PARALLEL-COMMUNICATION INTERFACE

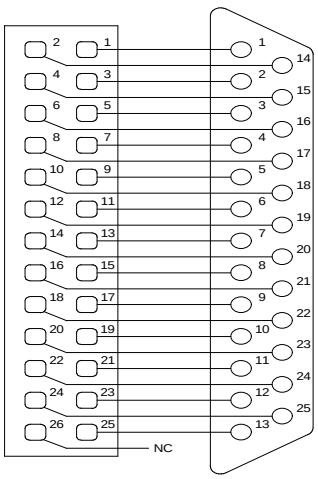
The JRex-CE supports one parallel port in either extended capabilities port (ECP) or enhanced parallel port (EPP) mode.

8.1 Parallel Connector

Parallel Port LPT 1				
Pin	**Signal Name**	**Function**	**In / Out**	**DSUB-25 (need adapter)**
1	Strobe#		Out	1
3	Data 0		I/O	2
5	Data 1		I/O	3
7	Data 2		I/O	4
9	Data 3		I/O	5
11	Data 4		I/O	6
13	Data 5		I/O	7
15	Data 6		I/O	8
17	Data 7		I/O	9
19	ACK#		In	10
21	BUSY		In	11
23	PAPER out		In	12
25	SEL out		In	13
2	AUTOFD#		Out	14
4	ERROR#		In	15
6	INIT#		Out	16
8	SEL in		Out	17
26	VCC (*)	+ 5 V	--	NC
10,12	GND	Signal Ground	--	18 - 25
14,16	GND	Signal Ground	--	18 - 25
18,20	GND	Signal Ground	--	18 - 25
22,24	GND	Signal Ground	--	18 - 25

Note: (*) To protect external power lines of peripheral devices, make sure that
-- the wires have the right diameter to withstand maximum available current
-- the enclosure of the peripheral device fulfils fire-protecting requirements of IEC/EN 60950.

You can use an adapter cable to change from the 26-pin header style of the JRex-CE to the more common 25-pin female D-sub.



26-pin Header to 25-pin D-Subconversion

8.2 Configuration

The JRex-CE parallel ports are bi-directional. The bi-directional functions are compatible with those of a PS/2 style parallel port. The functionality is always available and does not conflict with normal printer use. The parallel-port mode, I/O addresses, and IRQs are defined in the PhoenixBIOS Setup Utility.
Please see BIOS Setup.

9. KEYBOARD AND PS/2 MOUSE INTERFACE

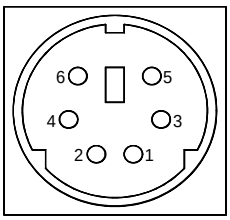
This interface consists of Keyboard and PS/2 Mouse. A PS/2 keyboard works directly; by using a PS/2 mouse please use a Y-cable for mouse and KB. Some of this Y-cable we see (Laptop-PS/2 Y) has to be connected the following way:
M - Keyboard
K - Mouse



To find the location of keyboard/ mouse Connector on the JRex-CE board, please see the **Appendix E: Connector Layout** chapter.

9.1 Keyboard/ Mouse Connector

Pin	Signal Name	Function
1	KBDAT	Keyboard Data
2	MSDAT	Mouse Data
3	GND	Ground
4	VCC	+5V Vcc
5	KBCLK	Keyboard Clock
6	MSCLK	Mouse Clock



9.2 Configuration

Please see BIOS Setup.

10. FLOPPY-DRIVE INTERFACE

The floppy-drive interface can support one 3.5” drive, using the adapter cable ADA-Floppy 2, (part number 96001-0000-00-0).

The board can support the following drive capacities:
720K

1.44M

2.88M

10.1 Floppy Connector

Signal	Function	Pin	Signal	Function
VCC (*)	+ 5V	2	IDX	Index
VCC (*)	+ 5V	4	DS0	Drive select 0
VCC (*)	+ 5V	6	DCHNG#	Disk change
NC	-	8	NC	-
NC	-	10	Mo0	Motor on
NC	-	12	DIR	Direction select
NC	-	14	STEP	Step
GND	Ground	16	WD	Write data
GND	Ground	18	WG	Write gate
GND	Ground	20	TR00	Track 00
GND	Ground	22	WP	Write protect
GND	Ground	24	RD	Read data
GND	Ground	26	SIDE	Side one select

Note: (*)To protect the external power lines of peripheral devices, make sure that:
- wires have the right diameter to withstand the maximum available current
- the enclosure of the peripheral device fulfils the fire protecting requirements of IEC/EN 60950.

10.2 Configuration

Specify the drive type using the PhoenixBIOS Setup Utility.

Choices for the 3.5" drive type include:
360KB, 1.2MB, 720Kb, 1.44MB, 2.88MB, None

You can disable the floppy-disk interface from the PhoenixBIOS Setup Utility.

Please show BIOS Setup for information on configuration.

11. IDE-CONTROLLER INTERFACE

PCI bus devices serve as primary and secondary IDE hosts on the JRex-CE. BIOS automatically configures them, but you can disable them by using the BIOS Setup Utility. Resources used by primary and secondary IDE host adapters are compatible with the PC/AT.

The IDE controller supports the following modes:
Ultra 100 DMA mode with a 80 pin UDMA100 cable

PIO modes up to Mode-4 timing

Multiword DMA Mode 1 and 2 with independent timing

11.1 IDE Connector

The IDE connector is a 40-pin, dual in-line, 2,54mm-pitch, male header.
To find the location of the Connector on the JRex-CE board, please see the

Appendix E: Connector Layout chapter.

If you are using JFLEXÔ extension modules please remove the strain relief.

If you are using a non standard DMA66 or DMA100 cable or adapter to connect a fast harddisk reduce the speed in the setup Menu.

11.2 Configuration

You can connect one or two IDE drives to the header by using an appropriate flat-ribbon cable. For UDMA100 please use a UDMA cable.

1. Configure the first drive as master.
2. Configure the second drive (at the end of the cable) as slave.
3. Consult your disk-drive manual for instructions.

11.3 CompactFlash Connector

A CompactFlash socket for commercial CompactFlash Memory Cards (only Type I) is integrated on the bottom side of the JRex-CE board.

11.4 Configuration

You can use the CompactFlash Memory card as a master device on the secondary IDE port. The BIOS will automatically detect size of this medium.
Please show BIOS Setup for information on configuration.

12. ETHERNET-CONTROLLER INTERFACE

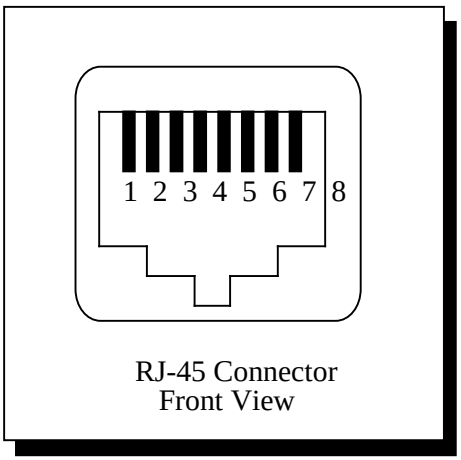
The JRex-CE on-board Ethernet interface use Intel® 82562 Family Platform LAN Connect Fast Ethernet Controller.

The network controllers support a 10/100Base-T interface. The device auto-negotiates the use of a 10Mbit/sec or 100Mbit/sec connection.

All major network-operating systems and several real-time and embedded operating systems support the interface.

12.1 LAN Connector

The 10/100Base-T connector is a standard 8-pin RJ45 jack.



RJ-45 Connector
Front View

Pin#	Signal Name	Function	In/Out
1	TXD+[1]	100/10BASE-T Transmit	Differential Output
2	TXD-[1]	100/10BASE-T Transmit	Differential Output
3	RXD+[2]	100/10BASE-T Receive	Differential Input
4	NC	Unused Pin	
5	NC	Unused Pin	
6	RXD-[2]	100/10BASE-T Receive	Differential Input
7	NC	Unused Pin	
8	NC	Unused Pin	

Notes:

[1]TXD+, TXD- Differential output pair drives 10 and 100Mb/s Manchester-encoded data to the 100/10BASE-T transmit lines.

[2]RXD+, RXD- Differential input pair receives 10 and 100Mb/s Manchester-encoded data from the 100/10BASE-T receive lines.

12.2 Configuration

The configuration of the on-board PCI Ethernet interface via the PhoenixBIOS Setup is automatically.

12.3 Ethernet Technical Support

You can solve some Ethernet problems by using the latest drivers for the intel 82562 controller. We provide you with the latest tested drivers, which can differ from newer ones.

For further technical support, contact either **Kontron** or get support information and download software update from intel (just type “82562” on http://downloadfinder.intel.com)

13. 4-BIT GPIO PORT

The JRex-CE Module provides 4 GPIO Pins. Each pin is individually configurable as an input or Open-Drain output. When configured as output the user must provide a pullup resistor to the desired output voltage level. All output pins have 12mA drive strength. The output LowLevel is max. 0,4V.

13.1 Programming

The W83627HF Super I/O controller consists of several logical devices, which correspond to individual functionality. Logical Device 7 reflect the GPIO Port 1. Each Logical Device has it´s own configuration registers. The designer can access the desired configuration Registers by selecting a logical device through the Extended Functions Data Register (I/O port index address 2Eh and data address 2Fh).

Configuration Register Logical Device 7

Index F0h: GPIO1 selection register. Default 0FFh
When set to a '1' respective GPIO pin is programmed as an input.
When set to a '0' respective GPIO pin is programmed as an output

Index F1h: GPIO1 data register. Default 00h
If GPIO is programmed to be an output port, then the respective bit can be written, else if the GPIO is programmed as input port , then the respective bit can be read.

Index F2h: GPIO1 inversion register. Default 00h
When set to a '1' respective GPIO pin will be inverted
When set to a '0' respective GPIO pin stay same as in data register

Programming example

```
W83697_IOBASE           EQU     02Eh      ;base address for index/data port
W83697_CONFIG_ENABLE    EQU     087h      ;data for unlock sequence
W83697_CONFIG_DISABLE   EQU     0AAh      ;data for lock sequence

;+---------------------------------------------------------------------------
;
; sioGpio1ReadData – read data from GPIO1
;
;       Entry:
;        None
;       Exit:
;        AH: input value
;
sioGpio1ReadData   PROC NEAR PUBLIC
      pushf                             ; no INTs while accessing
            cli                         ; W83697UF devices.

            Mov    al, 07h              ; device selection register 07h
      mov   ah, 07h                     ; select logical device
      call  sioRegWrite8

      Mov   al, 0F0h                    ; GPIO1 selection register
      mov   ah, 0FFh                    ; set to be an input port
      call  sioRegWrite8

      mov   al, 0F1h                    ; GPIO1 data register
      call  sioRegRead8                 ; read data from port
```

```
      popf
      ret
sioGpio1ReadData   ENDP

;+-------------------------------------------------------------------------
;
; sioGpio1WriteData – write data to GPIO1;
;       Entry:
;        AH: output value
;       Exit:
;        None
;
sioGpio1WriteData  PROC NEAR PUBLIC
      push   ax                         ; store output value
      pushf                             ; no INTs while accessing
             cli                        ; W83697UF devices.

             Mov    al, 07h             ; device selection register 07h
      mov    ah, 07h                    ; select logical device 7
      call   sioRegWrite8

      Mov    al, 0F0h                   ; GPIO1 selection register
      mov    ah, 087h                   ; Bit 3...6 set to be output
      call   sioRegWrite8

      pop    ax                         ; restore output value
      mov    al, 0F1h                   ; GPIO1 data register
      call   sioRegWrite8               ; write data to port

      popf
      pop    ax
      ret
sioGpio3ReadData   ENDP


;+-------------------------------------------------------------------------
;
;       sioRegRead8 – reads an 8-bit SIO configuration register
;
;       Entry:
;        AL – register index
;
;       Exit:
;        AH – register value
;
sioRegRead8    PROC NEAR PUBLIC
      pushf                             ; no INTs while SIO configuration
      cli                               ; register access.
      Push   dx

             mov    ah, al                      ; save register index.

             Mov    dx, W83697_IOBASE           ; port 2Eh – perform unlock
      Mov    al, W83697_CONFIG_ENABLE
      out    dx, al
      out    dx, al

             mov    al, ah                      ; write register index.
      Out    dx, al
             xchg   ah, al

      inc    dx                         ; port 2Fh – read register data .
      in     al, dx
      xchg   ah, al

             push    ax                ; Save index and data.

      Dec    dx                         ; port 2Eh – perform lock mechanism.
      Mov    al, W83697_CONFIG_DISABLE
      out    dx, al
```

```
            pop     ax
            pop     dx
            popf
            ret
sioRegRead8    ENDP

;+---------------------------------------------------------------------------
;
;       sioRegWrite8 – writes an 8-bit SIO configuration register
;
;       Entry:
;        AL – register index
;        AH – register value
;
;       Exit:
;        none
;
sioRegWrite8   PROC NEAR PUBLIC
      pushf                             ; no INTs while SIO2 configuration
            cli                                 ; register access.
            Push   dx
            push   ax

            mov    dx, W83697_IOBASE  ; port 2Eh – perform unlock mechanism.
      Mov    al, W83697_CONFIG_ENABLE
      out    dx, al
      out    dx, al

            pop    ax                  ; port 2Eh – write register index.
            Push   ax
      out    dx, al

            mov    al, ah              ; port 2Fh – write register data.
      Inc    dx
      out    dx, al

      dec    dx                         ; port 2Eh – perform lock mechanism.
      Mov    al, W83697_CONFIG_DISABLE
      out    dx, al

            pop    ax
            pop    dx
            popf
            ret
sioRegWrite8   ENDP
```

13.2 Connector

A Molex 53047-0410 connector is used.

13.3 Connector Pinout

Connector Pin Number	GPIO Number	Super-IO Pin Name
1	4	GPIO16
2	3	GPIO15
3	2	GPIO14
4	1	GPIO13

14. GRAPHICS-CONTROLLER INTERFACE

14.1 Flat Panel LVDS (JILI) Connector

The user interface for flat panels is the JUMPtec Intelligent LVDS Interface (JILI). The implementation of this subsystem complies with the JILI Specification.

To find the location of this Connector on the JRex-CE board, please see the Appendix E: Connector Layout chapter.

On VCC pins:
To protect the external powerlines of peripheral devices the customer has to take care about:

- **that the wires have the right diameter to withstand the maximum available current**
- **that the enclosure of the peripheral device fulfils the fire protecting requirements of IEC/EN 60950.**

14.2 VGA Connector

DSUB15 (J2)	Signal Name	Function
1	RED	Analog Video Red
2	GREEN	Analog Video Green
3	BLUE	Analog Video Blue
5	GND	Signal Ground
6	GND	Signal Ground
7	GND	Signal Ground
8	GND	Signal Ground
10	GND	Signal Ground
13	HSYNC	Horizontal Sync
14	VSYNC	Vertical Sync

14.3 Configuration

Refer the „Advanced Chipset Control“ Menu at the BIOS Setup for configuration.

For drivers go to http://downloadfinder.intel.com and type 855.

Install the “INF Update Utility” at first, then the “Intel® Extreme Graphics driver” for your OS.

On Problems:

- check out the latest drivers
- set the values on the „Advanced Chipset Control“ Menu to the highest values
- use a clean installation of your OS

Note: When using Windows XP do not connect a Flat Panel during installation. Connect Flat Panel after installation of the video driver has been done.

15. POWER (CONNECTOR AND BUTTON)

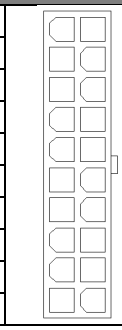
The JRex-CE uses +5V, +3.3V. +5V Standby and a power good signal. For some panels or some JFLEX modules +12V are required. Also by some harddisks and floppy drives. Please make sure that all voltages will connect to the board at the same time.

It is recommend to use a standard ATX power supply.

In difference to the ATX specification the JRex-CE is starting by switching on the primary supply voltage of the ATX power supply (auto start after power fail).

By using a non ATX power supply please connect just 3.3 V on all pins "+3.3V" and 5V on all pins "+5V" and "+5V Standby". Leave "Power Good" and "Power supply on" unconnected.

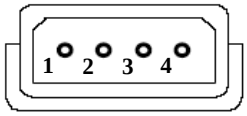
15.1 ATX Power Connector

Power Connector		
+12V (don't need on JRex-CE)		+5V
+5V Standby		+5V
Power Good		-5V (don't need)
Ground		Ground
+5V		Ground
Ground		Ground
+5V		Power Supply On
Ground		Ground
+3.3V		-12V (don't need)
+3.3V		+3.3V

Cable Connector for power available from

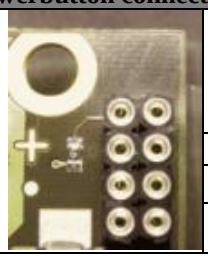
- Molex as 20 pin 5557d use with 5556 or 44476 terminals

15.2 5V-only Power Connector



Pin	Description
1	+5V
2	GND
3	GND
4	+12V

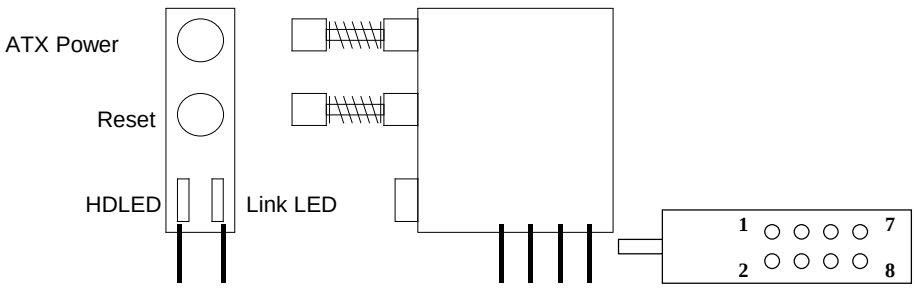
15.3 Socket Powerbutton

Powerbutton connector		
HDLED (Cathode)		LAN LinkLED (Cathode)
+5V (Anode)		+3.3V (Anode)
Reset		Ground
Powerbutton		Ground

15.4 Powerbutton

In the front oft the Board there is a button for switching the ATX power supply on or off. Additional there is a button for reset the board.

Also there are LEDs for Harddisk activity (HDLED) and for displaying a link to a network (Link LED).



16. JFLEXÔ EXTENSION CONNECTOR

Our JFLEX™ Extension Concepts includes 2 Connectors with 120 pins.
This Connectors allows to extend our JRex Boards with extra functions.
On the JRex-CE we provide:

- second COM Port TTL
- LPC Bus for more I/O devices
- PCI Bus for up to 3 PCI devices
- AC97 Bus for sound
- LVDS panel output
- Digital video out port DVO for optional TV-Out Encoders, TMDS and LVDS transmitters

We will bring out some of this function on the market to allow you to add interesting functions.
Some **JFLEX** modules are available at the product website www.j-rex.com.
Our JRex extension specification and design guide is only available from Kontron Embedded Modules GmbH by signing a NDA.
If you have more ideas for more functionability please feel free to inform us via your sales channel or discuss your wishes in our forum on www.j-rex.com.
We will also make an overview of certified partners available to make designs for your own extended functions.
If you are interested and if you have expiriences on digital panel adaptations or on PCI Bus please contact us on our webpage to get an membership in the certified partner program.

17. WATCHDOG TIMER

Programming:

The system BIOS makes it very easy to use the watchdog via software interrupt 15h. Two ways are possible to access the watchdog: The simplest way is to use AH=0E0h to init or trigger the watchdog.

For detailed describtion see Application Notes and our Specification X00391.doc.
Both documents can be downloaded from our webpage or ask our technical support.

APPENDIX A: SYSTEM-RESOURCE ALLOCATIONS

I/O Port Assignments

Devices on the JRex-CE use I/O addresses common to the PC/AT.

Interrupt Request Lines

The following table describes the allocation of the 16 hardware-interrupt lines for the JRex-CE.

IRQ #	Primary Use	Available	Comment
0	Timer0	No	
1	Keyboard	No	
2	Cascade	No	
3	COM2	Yes	
4	COM1	No	Note (1)
5	Soundblaster Compatibility mode	No	Note (1)
6	FDC	No	Note (1)
7	LPT1	No	Note (1)
8	RTC	No	
9	Free	Yes	
10	Free	Yes	
11	Free	Yes	
12	PS/2 Mouse	No	Note (1)
13	FPU	No	
14	IDE0	No	Note (1)
15	IDE1 (Compact Flash)	No	Note (1)

Notes: [1] If the “Used For” device is disabled in setup, the corresponding interrupt is available for other devices.

Direct Memory Access (DMA) Channels

DMA #	Used For	Available
0		Yes
1	Sound	No
2	FDC	No
3	LPT	No
4	Cascade	No
5		Yes
6		Yes
7		Yes

Note: [1] If the “Used For” device is disabled in setup, the corresponding interrupt is available for other devices.

Upper Memory Area Map

Upper Memory	Use	Available
C0000h – CBFFFh	VGA BIOS	No
CC000h – DFFFFh		Yes
E0000h – EFFFFh		Yes
F0000h – EC000h	System BIOS	No

PCI Devices

PCI Device #	IDSEL #	IRQ	Busmaster
AGP Grafic	Separated Bus	-	-
Intel Ethernet	AD24	E	Internal
Davicom Ethernet	AD17	D	
AC97 Sound Controller	Separated Bus	B	Internal
1st USB Controller	Separated Bus	A	Internal
2nd USB Controller	Separated Bus	D	Internal
EHCI USB Controller	Separated Bus	H	Internal

Please refer „*Intel® 82801DB ICH4 Datasheet*“ for additional information.

APPENDIX B: BIOS OPERATION

The JRex-CE comes equipped with Phoenix BIOS 4.0, which is located in an onboard Flash. The device has an 8-bit access. The shadow RAM feature offers faster access (16 bit). You can update the BIOS using a Flash utility. For complete Phoenix BIOS 4.0 information, visit the **Phoenix Technologies Web site**.

BIOS Version

The BIOS version displays onscreen during the POST at boot.

Setup Guide

The PhoenixBIOS setup utility allows you to change system behavior by modifying the BIOS configuration. Setup-utility menus allow you to make changes and turn features on or off.

BIOS-setup menus represent those found in most models of the JRex-CE. The BIOS setup utility for specific models can differ slightly.

Note: Selecting incorrect values can cause system boot failure. Load setup-default values to recover by pressing <**F9**>.

Start Phoenix BIOS Setup Utility

To start the PhoenixBIOS setup utility, press <**F2**> when the following string appears during bootup.

```
Press <F2> to enter Setup
```

The Main Menu then appears.

Several sections comprise the **Setup Screen.**

Setup Screen	Location	Function
Menu Bar	Top	Lists and selects all top level menus
Legend Bar	Bottom	Lists setup navigation keys
Item Specific Help Window	Right	Help for selected item
Menu Window	Left Center	Selection fields for current menu
General Help Window	Overlay (center)	Help for selected menu

Menu Bar

The menu bar at the top of the window lists menus. Use the left/right arrow keys to make a selection.

Legend Bar

Use the keys listed in the legend bar on the bottom to make your selections or exit the current menu. The table below describes the legend keys and their alternates.

Key	Function
<F1> or <Alt-H>	General Help window
<Esc>	Exit menu
← or → Arrow key	Select a menu
↑ or ↓ Arrow key	Select fields in current menu
<Tab> or <Shift-Tab>	Cycle cursor up and down
<Home> or <End>	Move cursor to top or bottom of current window
<PgUp> or <PgDn>	Move cursor to next or previous page
<F5> or <->	Select previous value for the current field
<F6> or <+> or <Space>	Select next value for the current field
<F9>	Load the default configuration values for this menu
<F10>	Save and exit
<Enter>	Execute command or select submenu
<Alt-R>	Refresh screen

Selecting an Item

Use the ↑ or ↓ key to move the cursor to the field you want. Then use the + and - keys to select a value for that field. The **Save Value** commands in the **Exit** menu save the values displayed in all the menus.

Displaying Submenus

Use the ← or → key to move the cursor to the submenu you want. Then press <Enter>. A pointer (4) indicates submenus.

Item Specific Help Window

The Help window on the right side of each menu displays the Help text for the selected item. It updates as you move the cursor to each field.

General Help Window

Pressing <**F1**> or <**ALT-F1**> on a menu brings up the General Help window that describes legend keys and alternates. Press <**Esc**> to exit the General Help window.

Menu Description

For the Menu description please refer the „Item Specific Help“ on the right side of the Setup Menu.

Updating BIOS with Phoenix Phlash

Phoenix Phlash allows you to update BIOS using a floppy disk without having to install a new ROM chip. Phoenix Phlash is a utility for flashing a BIOS to the Flash ROM installed on the JRex-CE

Use Phoenix Phlash to:
Update the current BIOS with a newer version

Restore a corrupt BIOS (see below)

You can download Phoenix Plash as a compressed file, CRISBQT3.ZIP, from the Web site. It contains the following files:

File	Purpose
MAKEBOOT.EXE	Creates the custom boot sector on the Crisis Recovery Diskette.
CRISBOOT.BIN	Serves as the Crisis Recovery boot sector code.
MINIDOS.SYS	Allows the system to boot in Crisis Recovery Mode.
PHLASH.EXE	Programs the flash ROM.
WINCRISIS.EXE	Creates the Crisis Recovery Diskette from Windows.
WINCRISIS.HLP	Serves as the help file of WINCRISES.EXE.
PLATFORM.BIN	Performs platform-dependent functions.
BIOS.ROM	Serves as the actual BIOS image to be programmed into Flash ROM.

To install Phoenix Phlash on a hard disk, unzip the content of CRISBQT3.ZIP into a local directory such as C:\PHLASH.

Creating a Crisis Recovery Diskette

Insert a blank diskette into Drive A: or B: and execute WINCRISIS.EXE. This copies four files onto the Crisis Recovery Diskette.

File	Purpose
MINIDOS.SYS	Allows the system to boot in Crisis Recovery Mode.
PHLASH.EXE	Programs the flash ROM.
PLATFORM.BIN	Performs platform-dependent functions.
BIOS.ROM	Serves as the actual BIOS image to be programmed into Flash ROM.

If the BIOS image (BIOS.ROM) changes due to an update or bug fix, copy the new BIOS.ROM image onto the diskette.

Phoenix Phlash runs in one of two modes:
Command Line Mode

Crisis Recovery Mode

Use the Command Line mode to update or replace a BIOS. To execute Phlash in this mode, move to the Crisis Recovery Disk and type:

```
PHLASH BQT3R110.ROM
```

Phoenix Phlash will update the BIOS. Phlash can fail if the system uses memory managers. If this occurs, the utility displays the following message:

```
Cannot flash when memory manager are present.
```

Update the BIOS image by typing:

```
PHLASH /X BQBAR110.ROM
```

Boot Block Support

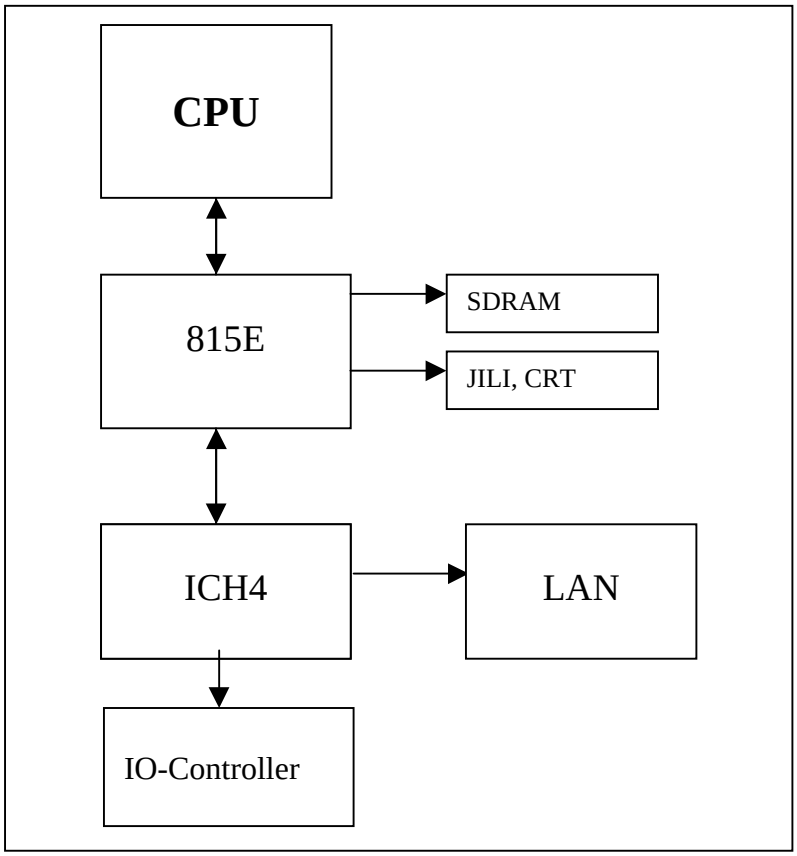
Updating the BIOS represents a potential hazard. Power failures or fluctuations that occur when you update the Flash ROM can damage the BIOS code, making the system unbootable.

To prevent this hazard, many systems come with a boot-block Flash ROM. The boot-block region contains a fail-safe recovery routine. If the boot-block code finds a corrupted BIOS (checksum fails), it boots into the crisis recovery mode and loads a BIOS image from a crisis diskette (see above).

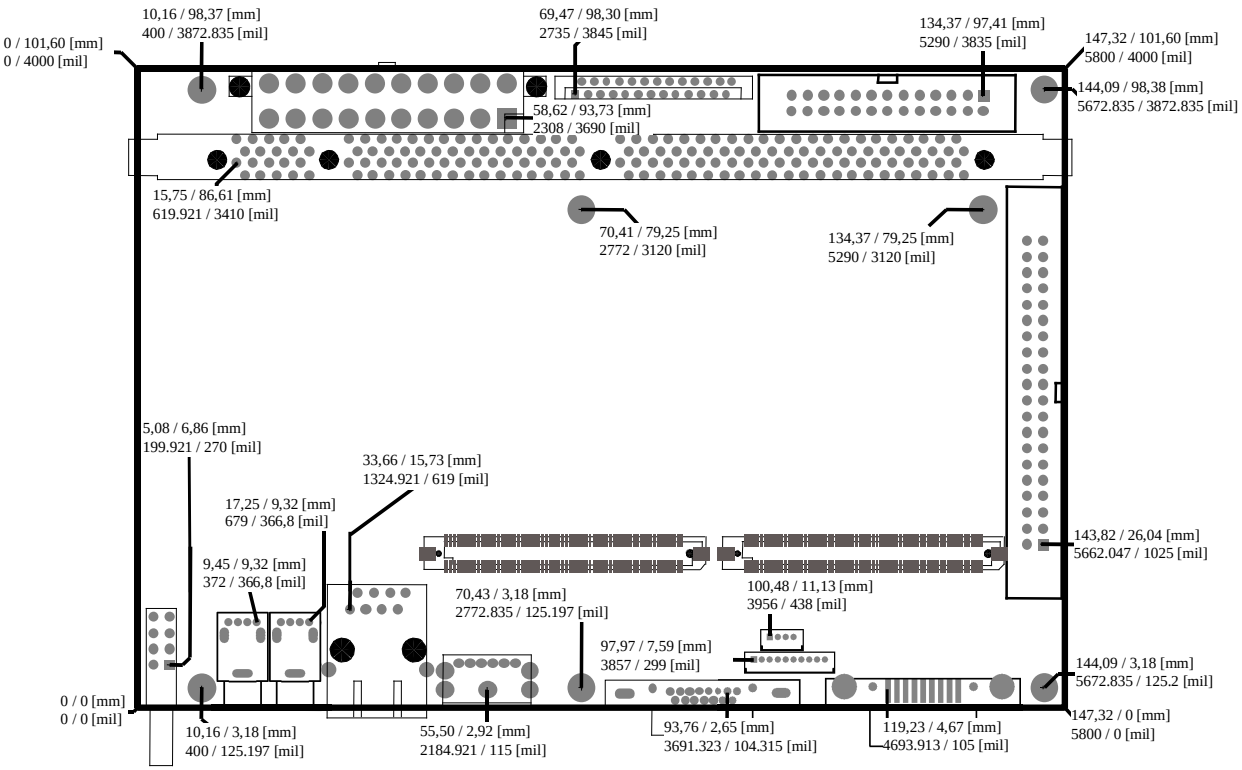
Additionally, the end user can insert an update key into the serial port (COM1 only) to force initiating the boot block recovery routine.

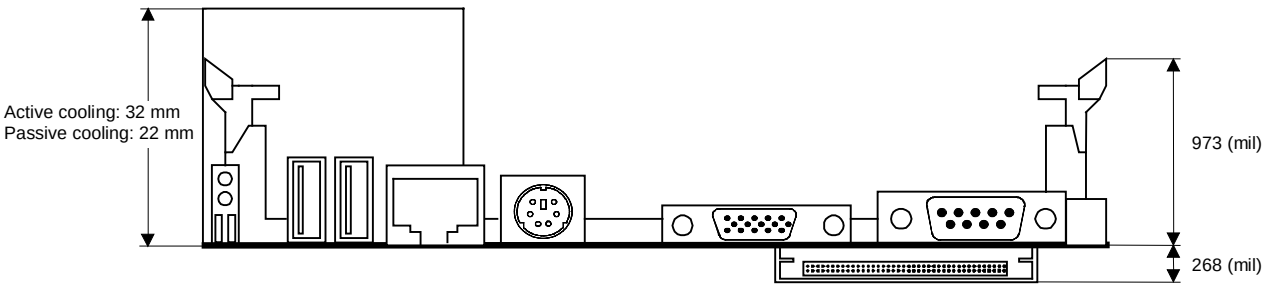
For further information on the update key and the crisis diskette, see application note **JAP0034**.

APPENDIX C: BLOCK DIAGRAM

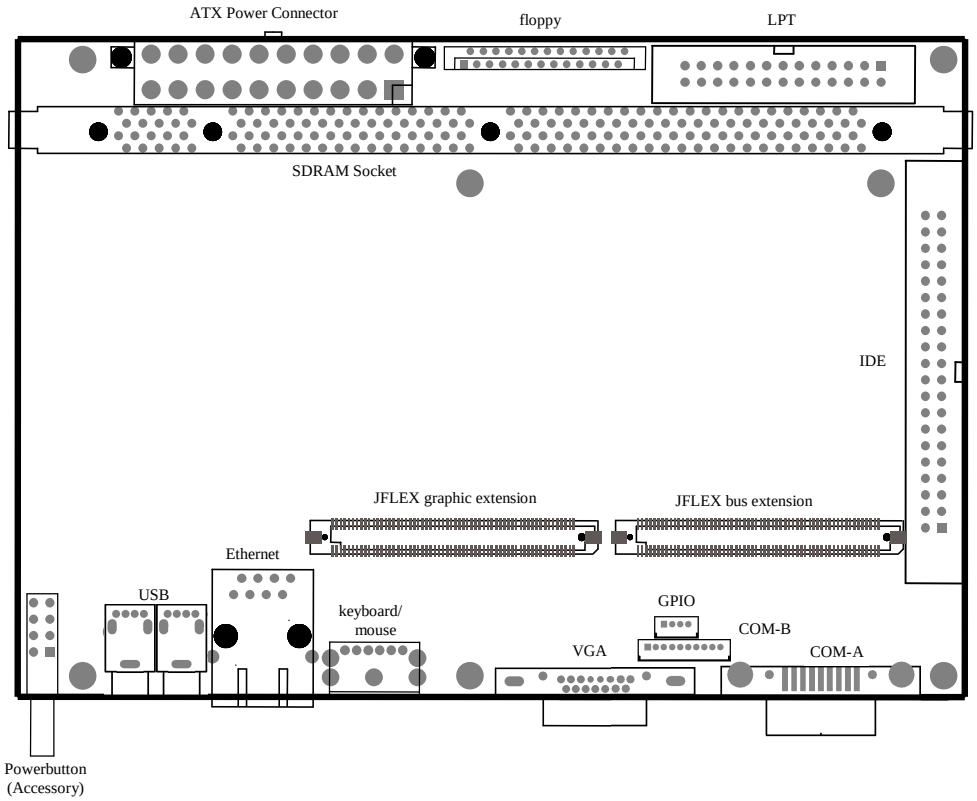


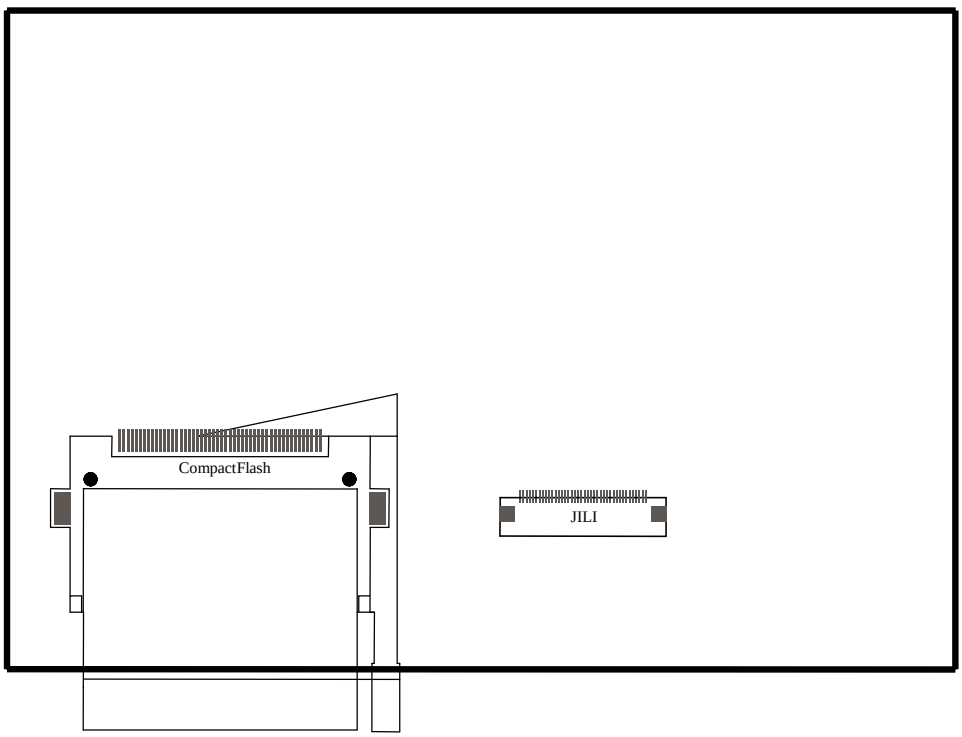
APPENDIX D: MECHANICAL DIMENSIONS





APPENDIX E: CONNECTOR LAYOUT





APPENDIX F: JIDA STANDARD

Every board with an on-board BIOS extension supports the following function calls, which supply information about the board. Jump*tec* Intelligent Device Architecture (JIDA) functions are called via Interrupt 15h. Functions include:

AH=EAh

AL=function number

DX=4648h (security word)

CL=board number (starting with 1)

The interrupt returns a CL≠0 if a board with the number specified in CL does not exist. CL will equal 0 if the board number exists. In this case, the content of DX determines if the operation was successful. DX=6B6Fh indicates success; other values indicate an error.

Obtaining Information about Boards that Use the JIDA Standard

To obtain information about the installed boards that follow the JIDA standard, use the following procedure.

1. Call Get BIOS ID with CL=1.
   The name of the first device installed will be returned.
   If you see the result **Board exists** (CL=0), increment CL, and call **Get BIOS ID** again.
2. Repeat until you see **Board not present** (CL≠0).
   You now know the names of all boards within your system that follow the JIDA standard.
3. You can find out more information about a specific board by calling the appropriate inquiry function with the board's number in CL.

Note: Association between board and board number may change because of configuration changes. Do not rely on any association between board and board number. Always use the procedure described above to determine the association between board and board number.

Refer to the JIDA manual in the jidai110.zip folder for further information on implementing and using JIDA calls with C sample code.

APPENDIX G: LITERATURE AND STANDARDS

Below is a list of information sources to help you to further understand PC architecture.

Buses

ISA, Standard PS/2 - Connectors

- *AT Bus Design: Eight and Sixteen-Bit ISA, E-ISA and EISA Design,* Edward Solari, **Annabooks**, 1990, ISBN 0-929392-08-6
- *AT IBM Technical Reference Vol 1&2*, 1985
- *ISA & EISA Theory and Operation*, Edward Solari, **Annabooks**, **1992,** ISBN 0929392159
- *ISA Bus Specifications and Application Notes,* Jan. 30, 1990, Intel
- *ISA System Architecture, Third Edition,* Tom Shanley and Don Anderson, Addison-Wesley Publishing Company, 1995, ISBN 0-201-40996-8
- *Personal Computer Bus Standard P996*, Draft D2.00, Jan. 18, 1990, IEEE Inc
- *Technical Reference Guide, Extended Industry Standard Architecture Expansion Bus,* Compaq 1989

PCI

- **PCI SIG**
  The PCI-SIG provides a forum for its ~900 member companies, who develop PCI products based on the specifications that are created by the PCI-SIG.
- *PCI & PCI-X Hardware and Software Architecture & Design*, Fifth Edition, Edward Solari and George Willse, Annabooks, 2001, ISBN 0-929392-63-9.
- *PCI System Architecture*, Tom Shanley and Don Anderson, Addison-Wesley, 2000, ISBN 0-201-30974-2.

General PC Architecture

- *Embedded PCs*, Markt&Technik GmbH, ISBN 3-8272-5314-4 (German)
- **ePanorama PC Hardware**
  ePanorama.net is dedicated to offer information on electronics found on the Web.
- *Hardware Bible*, Winn L. Rosch, SAMS, 1997, 0-672-30954-8
- *Interfacing to the IBM Personal Computer*, Second Edition, Lewis C. Eggebrecht, SAMS, 1990, ISBN 0-672-22722-3
- *The Indispensable PC Hardware Book*, Hans-Peter Messmer, Addison-Wesley, 1994, ISBN 0-201-62424-9
- *The PC Handbook: For Engineers, Programmers, and Other Serious PC Users, Sixth Edition*, John P. Choisser and John O. Foster, **Annabooks**, 1997, ISBN 0-929392-36-1

Ports

RS-232 Serial

- *RS-232 Made Easy: Connecting Computers, Printers, Terminals, and Modems*, Martin D. Seyer, Prentice Hall, 1991, ISBN 0-13-749854-3
- **National Semiconductor**
  Interface Data Book includes application notes. Type “232” as a search criteria to obtain a list of application notes.

IDE

Technical Committee T13
is responsible for all interface standards relating to the popular AT Attachment (ATA) storage interface utilized as the disk drive interface on most personal and mobile computers today.

The X3T10 standard defines an integrated bus interface between disk drives and host processors. It provides a common point of attachment for systems manufacturers and the system.
We recommend you also search for information on “4.2 I/O cable” if you use hard disks in a DMA3, DMA4 , DMA5 or PIO4 mode.

USB

USB specification
USB Implementers Forum, Inc. is a non-profit corporation founded by the group of companies that developed the Universal Serial Bus specification. The USB-IF was formed to provide a support organization and forum for the advancement and adoption of Universal Serial Bus technology.

Programming

- *C Programmer’s Guide to Serial Communications*, Second Edition, Joe Campbell, SAMS, 1987, ISBN 0-672-22584-0
- *Programmer's Guide to the EGA, VGA, and Super VGA Cards*, Third Edition, Richard Ferraro, Addison-Wesley, 1990, ISBN 0-201-57025-4
- *The Programmer’s PC Sourcebook*, Second Edition, Thom Hogan, Microsoft Press, 1991, ISBN 1-55615-321-X
- *Undocumented PC, A Programmer’s Guide to I/O, CPUs, and Fixed Memory Areas*, Frank van Gilluwe, Second Edition, Addison-Wesley, 1997, ISBN 0-201-47950-8

APPENDIX H: DOCUMENT REVISION HISTORY

Version	Date	Edited by	Changes
0.1	13.08.2004	BAJ	Created preliminary manual
1.0	01.12.2004	BAJ	First public release
1.1	07.03.2005	BAJ	Added COM-B and GPIO description