

MOPSlcd7

User's Guide

Document Revision 1.7

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1. USER INFORMATION

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Technicians and engineers from KONTRON Embedded Modules and/or its subsidiaries and official distributors are available for technical support. We are committed to making our product easy to use and will help you use our products in your systems.

Before contacting KONTRON Embedded Modules technical support, please consult our Web site for the latest product documentation, utilities, and drivers. If the information does not help solve the problem, contact us by telephone.

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2. INTRODUCTION

2.1 *MOPSlcd7*

The MOPS*lcd*7 single-board computer offers the choice of a high-performance Intel Mobile Pentium III® (500MHz or 700MHz) or low-cost, low-power Celeron® processors (300MHz). When configured with the Celeron processor, the MOPS*lcd*7 only needs fanless, passive cooling. The Intel Mobile Pentium III version is ideal for applications that require high-performance processing power. The MOPSlcd7 is a versatile, low-cost, low-power module that conforms to the industry standard 90mm x 96mm PC/104 form factor. The board's chipset includes a VIA Twister-T VT8606 north bridge, a VT82C686B south bridge, and an integrated S3 ProSavage4 graphics controller.

For visualization tasks, the S3 ProSavage4 graphics controller features up to 32MB of Shared Memory Architecture (SMA) and a JUMPtec Intelligent LVDS Interface (JILI) for trouble-free adaptation to all common LCD panels. Standard VGA output also is available.

The MOPSlcd7 features the following:

- CPU
- System ROM (BIOS)
- Up to 512MB SDRAM support
- Direct memory access (DMA) controllers
- Counters
- Interrupt controllers
- Keyboard/mouse controllers
- Speaker interface
- Floppy-drive interface
- Integrated Drive Electronics (IDE) hard-disk interface
- Serial ports (COM1 and COM2)
- Parallel port (LPT1)
- Real-time clock
- Watchdog timer
- Universal serial bus (USB) ports
- 10/100Base-TX Ethernet

2.2 MOPS Family

MOPS (**M**inimized **O**pen **P**C **S**ystem) PC/104 products represent the “Proven PC Platform for Instant Solutions." Each MOPS module is characterized by the same pinout for the keyboard, COM1 and COM2, 44-pin IDE, LPT, and 1st LAN. These homogeneous features facilitate easy upgrades within the Kontron Embedded Modules GmbH MOPS PC/104 product family.

Whenever a LCD panel is required, MOPS products with onboard graphics controllers serve as the right choice. Display connections are simplified when using these units, which come with a JUMPtec Intelligent LVDS Interface (JILI) or a JUMPtec Intelligent Panel Adapter (JIPA) interface. The two interfaces can recognize which display is connected and then independently set all video parameters. These interfaces are not available on all MOPS products. All MOPS-PC/104 are plug-and-work enabled to further reduce time-to-market.

As part of the standard features package, all MOPS PC/104 modules come with a JUMPtec Intelligent Device Architecture (JIDA) interface, which is integrated into the BIOS of the PC/104 modules. This interface enables hardware-independent access to the MOPS-PC/104 features that cannot be accessed via standard APIs. Functions such as watchdog timer, brightness and contrast of LCD backlight, and user bytes in the EEPROM can be configured with ease by taking advantage of this standard MOPS PC/104 module feature.

All MOPS PC/104 products can be controlled remotely by using JRC software through a serial port. The software allows you to change, update, and maintain the MOPS products from a host computer via a serial connection.

2.3 PC/104 an Embedded PC Standard

Over the past decade, PC architecture has become an accepted platform for far more than desktop applications. Dedicated and embedded applications for PCs are beginning to appear everywhere.

By standardizing hardware and software around the broadly supported PC architecture, embedded system designers can substantially reduce development costs, risks, and time-to-market.

For these reasons, companies that embed microcomputers as controllers within their products seek ways to reap the benefits of using the PC architecture. However, the standard form factor of a PC bus (12.4" x 4.8") and its associated card cages and backplanes are too bulky and expensive for most embedded control applications.

The only practical way to embed the PC architecture in space-and power-sensitive applications has been to design a PC chip by chip directly into the product. But this runs counter to growing trend away from "reinventing the wheel." Whenever possible, management encourages outsourcing of components and technologies to reduce development costs and accelerate product design cycles.

A need has arisen for a more compact implementation of the PC bus, satisfying the reduced space and power constraints of embedded control applications. PC/104 was developed in response to this need. It offers full architecture, hardware and software compatibility with the PC bus but in ultra-compact (3.6" x 3.8") stackable modules. PC/104 is ideally suited to the unique requirements of embedded control applications.

Although configuration and application possibilities with PC/104 modules are practically limitless, there are two ways to use them in embedded system designs:

- **Standalone module stacks**
  PC/104 modules are self-stacking. The modules are used like ultra-compact bus boards but do not need backplanes or card cages. Stacked modules are spaced 0.6 inches apart. (The stack of three modules measures 3.6 by 3.8 by 2 inches.) Companies using PC/104 module stacks within their products frequently create one or more of their own application-specific PC/104 modules.

- **Component-line applications**
  In this configuration, the modules function as highly integrated components, plugged into custom carrier boards that contain application-specific interfaces and logic. The modules' self-stacking bus can be useful to install multiple modules in one location. This facilitates product upgrades or options and allows temporary addition of modules during system debug or test.

3. GETTING STARTED

The easiest way to get the MOPSlcd7 board running is to use a starter kit from Kontron Embedded Modules GmbH. Take the following steps:

1. Turn off the power supply (part of the starter kit).
2. Connect the power supply to the starter kit baseboard (part of the starter kit).
3. Plug the MOPSlcd7 to the PC/104 and PC/104Plus bus connectors on the starter kit baseboard.
4. Make all necessary connections from the MOPSlcd7 to the starter kit board. (Cables come with the starter kit). The starter kit board offers various interfaces on standard connectors.
5. Plug a suitable SDRAM memory module into the SODIMM socket of the MOPSlcd7.
6. Connect the CRT monitor to the CRT interface or a LCD panel to the JILI interface by using the corresponding adapter cable.
7. Plug a keyboard to the starter kit's keyboard connector.
8. Connect the floppy drive (part of the starter kit) with the data cable (part of the starter kit) to the MOPSlcd7 floppy interface.
9. Connect the power supply to the floppy's power connector.
10. Plug a hard-drive data cable to the MOPSlcd7 hard-disk interface. Attach the hard disk to the connector at the opposite end of the cable.
11. If necessary, connect the power supply to the hard disk's power connector.
12. Make sure all your connections have been made correctly.
13. Turn on the power.
14. Enter the BIOS by pressing the F2 key during boot-up. Make all changes in the BIOS setup. See the BIOS chapter of this manual for details.

4. SPECIFICATIONS

4.1 *Functional Specifications*

- Processor
  - Mobile Pentium III® processor – 500MHz or 700MHz
  - Ultra Low Power (ULP) Celeron® processor - 300MHz
- Cache
  - Pentium III - 256KB
  - Celeron - 128KB
- Bus
  - 100MHz CPU bus
  - 100MHz or 133MHz memory bus
- Chipset
  - VIA VT8606/VT82C686B (north bridge/south bridge)
- Power Supply
  - 5V supply
  - Onboard power supply to low-voltage technology
- Super I/O
  - Integrated in VIA VT82C686B (south bridge)
- Memory
  - One 144-pin SODIMM interface
  - 3.3V PC-133 or PC-100 unbuffered SDRAM, up to 512MB
- Two Serial Ports
  - COM1 and COM2 (RS232C compatible)
- One Parallel Port (LPT1)
  - Enhanced Parallel Port (EPP) and Extended Capabilities Port (ECP) with bi-directional capability
- Floppy Drive Interface
- System Monitor Controller for Temperature and Fan

- Enhanced Intelligent Drive Electronics (EIDE)
  - UDMA Peripheral Component Interconnect (PCI) Bus Master IDE ports (up to two devices)
- Universal Serial Bus (USB)
  - Two USB 1.1 ports (UHCI)
  - USB legacy keyboard and mouse support
  - USB floppy-boot and CDROM-boot support
- Ethernet
  - DAVICOM DM9102A 10/100 Mbps PCI Fast Ethernet controller
- Onboard Video Graphics Array (VGA)
  - Integrated in VIA VT8606 (north bridge)
  - 4x AGP, ProSavage4 controller
  - Up to 32MB Video RAM (SMA)
  - Cathode ray tube (CRT) and low voltage differential signaling (LVDS) LCD/flat-panel interfaces
- Phoenix BIOS, 512KB Flash BIOS
- NV-EEPROM for CMOS Setup Retention without Battery
- PS/2 Keyboard Controller
- PS/2 Mouse Interface
- Watchdog timer (WDT) with PIC
- Real-time Clock (requires external battery)

4.2 *Mechanical Specifications*

4.2.1. PC/104 Bus Connector (ISA part)

- One 2 X 32 pin stackthrough and one 2 X 20 pin stackthrough connector

4.2.2. PC/104-Plus Bus Connector (PCI part)

- One 4 x 30 pin 2mm downward connector

The PC/104plus connector does not have a connector shroud. You cannot use a PC/104plus board on the top of a MOPS*lcd*7. This mechanical limitation does not reduce the functionality of a MOPS*lcd*7 board.

4.2.3. Module Dimensions

- 95 x 90 mm (3.7" x 3.5")

4.2.4. **Height** (including PC/104 connector pins and cooler/fan)

- For boards equipped with Mobile Pentium III® processor : 27.2 mm max (1.07")
  These boards are equipped with a fan.
- For boards equipped with ULP Celeron® processor: 26.7 mm max (1.05")
  This board is equipped with a passive cooler.

4.2.5. Weight

- 140 g (full feature version without memory module)

4.3 *Electrical Specifications*

4.3.1. Supply Voltage

- 5V DC +/- 5%

4.3.2. Supply Voltage Ripple

- 100 mV peak to peak 0 - 20 MHz

4.3.3. Supply Current (Typical)

Power-consumption tests were executed during the DOS prompt. The tested boards were equipped with 256MB SDRAM and a 32MB chipDISK.

CPU	ULP Celeron (300MHz)			Mobile PIII (500MHz)			Mobile PIII (700MHz)		
Mode	Normal	Standby	Suspend	Normal	Standby	Suspend	Normal	Standby	Suspend
Power Consumption	2.12 A	1.58 A	1.49 A	3.12 A	2.02 A	1.90 A	3.47 A	1.84 A	1.70 A

4.3.4. Supply Current (maximum)

CPU	ULP Celeron (300MHz)	Mobile PIII (500MHz)	Mobile PIII (700MHz)
Power Consumption	2.96A	4.46A	4.89A

4.3.5. External RTC Battery

- Voltage range: 2.4V-3.6V (typ. 3.0V)
- Maximum current: 10µA

4.4 MTBF

The following MTBF (Mean Time Between Failure) values were calculated using a combination of manufacturer's test data, if the data was available, and a Bellcore calculation for the remaining parts. The Bellcore calculation used is "Method 1 Case 1". In that particular method the components are assumed to be operating at a 50 % stress level in a 40° C ambient environment and the system is assumed to have not been burned in. Manufacturer's data has been used wherever possible. The manufacturer's data, when used, is specified at 50° C, so in that sense the following results are slightly conservative. The MTBF values shown below are for a 40° C office or telecommunications environment. Higher temperatures and other environmental stresses (extreme altitude, vibration, salt water exposure, etc.) will lower the MTBF values.

- System MTBF (hours) : 209,056

  (full featured maximum performance version)

Notes: Fans usually shipped with Kontron Embedded Modules GmbH products have 50,000-hour typical operating life. The above estimates assume no fan, but a passive heat sinking arrangement.
Estimated RTC battery life (as opposed to battery failures) is not accounted for in the above figures and need to be considered for separately. Battery life depends on both temperature and operating conditions. When the Kontron unit has external power; the only battery drain is from leakage paths.

4.5 Environmental Specifications

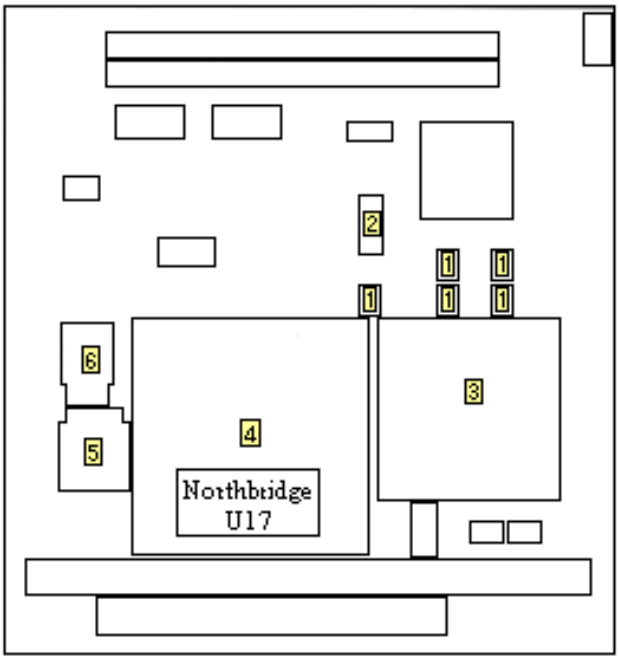
4.5.1. Temperature

The Intel® Mobile Pentium® III and Intel® Mobile Celeron® low voltage CPU is specified for proper operation when the junction temperature is within the specified range of 0°C to 100°C. The system controller can measure the temperature.

- Operating:
  - **MOPSlcd7-C3/300 MHz: 0 to +60°C with appropriate airflow***
  - **MOPSlcd7-PIII/500 MHz: 0 to +50°C with appropriate airflow***
  - **MOPSlcd7-PIII/700 MHz: 0 to +45°C with appropriateairflow***
- Non-operating: -10 to +85 °C (non-condensing)

Note: (*) The maximum operating temperature is the maximum measurable temperature on any spot on the module's surface. You must maintain the temperature according to the above specification.

For devices that are specified for higher temperatures, please see the following table and drawing.



Measure Point	Device	Max. operating temperature of the device
1	MOSFET SI4410	+110°C
2	LTC1702	+ 85°C
3	SB VT82C686B	+ 85°C
4	NB PN133T	+ 85°C
5	LX8580	+ 85°C
6	FAN1084	+85°C

Note: If you intend to use 3D applications, make sure that the temperature of the PN133T does not exceed 85°C. A heat sink on the north bridge (U17) and appropriate airflow are necessary.

4.6 *Humidity*

- Operating : 10% to 90% (noncondensing)
- Nonoperating : 5% to 95% (noncondensing)

5. CPU, CHIPSET, AND SUPER I/O

5.1 CPU

The central processing unit (CPU) consists of one of the following chips, depending upon which MOPS*lcd*7 board you use:

- Mobile Intel® Pentium® III (700MHz) processor with 256KB of integrated L2 cache. This board is equipped with a fan for the processor.
- Mobile Intel® Pentium® III (500MHz) processor with 256KB of integrated L2 cache. This board is equipped with a fan for the processor.
- Intel® Ultra Low Power (ULP) Celeron® processor (300MHz) with 128KB of integrated L2 cache. This board is equipped with a passive cooler.

5.2 Chipset

The VIA Technologies' Twister-T chipset consists of:

- VT8606 controller (north bridge)
  - High performance SMA North Bridge
  - Integrated VIA Pro133A and S3 ProSavage4™ in a single chip
  - 133/100MHz CPU Front Side Bus (FSB)
  - Advanced High-Performance 64bit DRAM controller
  - DRAM interface runs synchronous mode or pseudo-synchronous mode with FSB
  - Concurrent CPU, AGP and PCI access
  - Supports standard PC133 and PC100 SDRAM memory types
  - PCI 2.2 compliant bus controller
  - 32bit 3.3V PCI interface with 5V tolerant inputs
  - Advanced system power management support
- VT82C686B controller (south bridge)
  - PCI 2.2 compliant PCI to ISA bridge with DMA, timer and interrupt controller
  - Integrated keyboard controller with PS/2 mouse support
  - Integrated Real Time Clock (RTC)
  - Integrated USB controller
  - Integrated Enhanced-IDE controller
  - Integrated Super-I/O controller
  - System Management (SM) bus interface

5.3 Super I/O

The super I/O device is integrated in the south bridge of the VIA chipset, the VT82C686B. It offers the following features:

- Two serial ports
- One Multi-Mode Parallel Port
- Floppy Disk Controller

5.4 CPU, Chipset and Super-I/O Configuration

See the Advanced Menu and its submenus section of the Appendix B: BIOS chapter for information on possible settings.

6. SYSTEM MEMORY

The MOPSlcd7 uses only 144-pin Small Outline-Dual Inline Memory Modules (SODIMMs). One socket is available for 3.3 Volt (power level) unbuffered PC-133 or PC-100 Synchronous Dynamic Random Access Memory (SDRAM) of up to 512MB.

The total amount of memory available on the SDRAM module is used for main memory and graphic memory on the MOPSlcd7. Shared Memory Architecture (SMA) manages the sharing of the system memory between graphic controller and processor. Therefore, the full memory size is not available for software applications. Up to 32MB of system memory are used as graphic memory.

To find the location of the SDRAM socket U1 on the MOPSlcd7 board, please see the Appendix E: Connector Layout chapter.

7. ISA AND PCI BUS EXPANSION

The design of the MOPSlcd7 follows the standard PC/104 form factor and offers both ISA- and PCI-bus signals. The PC/104-Plus standard is downward compatible with PC/104 and enables the use of standard PC/104 and PC/104-Plus adapter cards.

7.1 *PC/104 Bus (ISA part)*

The PC/104 bus consists of two connectors that use 104 pins in total.

- XT bus connector (64 pins)
- AT bus connector (40 pins, which is optional for 16 bit-data bus system)

The pinout of the PC/104 bus connectors corresponds to the pinout of the ISA bus connectors with some added ground pins. The two PC systems with different form factors are electrically compatible.

The **XT bus connector**, Row A and B.

The corresponding 64-pin stackthrough header (ISA bus = 62pins) has two added ground pins at the end of the connector (Pin A32 and Pin B32). The pinout between PC/104 bus and XT ISA bus is identical between A1 - A31 and B1 - B31.

The **AT bus extension connector**, Row C and D.

The corresponding 40-pin stackthrough header (ISA bus = 36 pins) has four added ground pins, two on each side of the connector. To avoid confusion, the first two pins are defined as Pin C0 and Pin D0. The additional ground pins at the end of the connector are defined as C19 and D19. The pinout between PC/104 bus and AT ISA bus is identical between C1 - C18 and D1 - D18.

7.1.1. PC/104 Connectors

The MOPSlcd7 features both – XT bus and AT bus extension – on two, dual-row socket connector with 2.54mm x 2.54mm grid (0.1" x 0.1").

The PC-104 XT bus is available through the J16 connector. The PC/104 AT bus is available through the J17 connector.

A detailed description of the signals including electrical characteristics and timings is beyond the scope of this document. Please refer to the official ISA bus and PC/104 specifications for more details.

7.1.2. PC/104 Configuration

When using add-on boards on the PC/104 bus, make sure that there are no resource conflicts in the system. Carefully choose hardware interrupts, DMA channels, memory and I/O address ranges to avoid resource conflicts, which are often the reason for a board or a feature not functioning correctly. See Appendix A: System Resource Allocation for information about the resources already used by the MOPSlcd7.

7.2 *PC/104-Plus (PCI part)*

The MOPS*lcd*7 offers the PC/104-Plus bus on a quad-row downward connector with a 2mm x 2mm (0.79" x 0.79") pitch. This implements the standard 32-bit PCI bus signals.

7.2.1. PC/104-Plus Connector

You cannot use PC/104-Plus adapter boards on the top of a MOPS*lcd*7 as it only offers a downward connector. Additionally the PC/104plus connector does not have a connector shroud.

The PC/104-Plus bus is available through the optional connector J18.

A description of the signals, including electrical characteristics and timings, is beyond the scope of this document. Please refer to the official PCI bus and PC/104-Plus specifications for more details.

7.2.2. PC/104-Plus Configuration

When using add-on boards on the PC/104-Plus bus, these boards have to be associated to a "PCI-slot". Make sure that there are no resource conflicts in the system. Carefully choose PCI interrupts, REQ/GNT pairs and IDSEL for the add-on board. See the technical manual of the add-on board for more details.

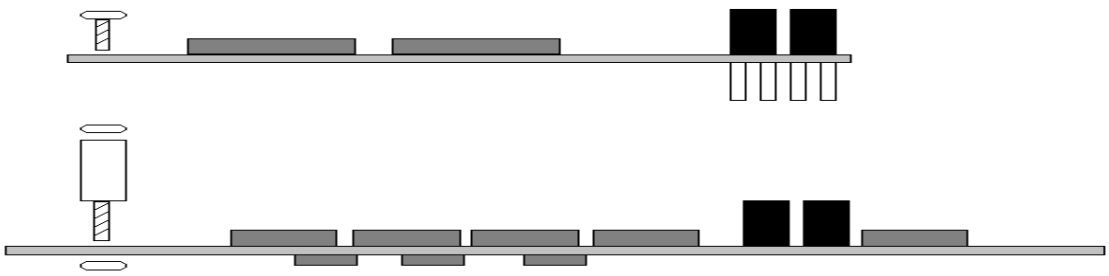
The MOPSlcd7 's PCI bus can be configured to optimize your system. See the PCI Configuration Submenu in Appendix B: BIOS for more information on configuration.

7.3 PC/104 and PC/104-Plus Stack

PC/104 and PC/104-Plus adapter cards are mounted in a stack-through manner. Adapter cards are designed with plugs on their topsides and/or undersides that mate with the PC/104 connectors of the MOPSlcd7.

Whenever possible use the MOPSlcd7 as top module of the PC/104 stack as the CPU board is normally the board with the highest heat dissipation.

Note: A MOPSlcd7 requires CPU cooling and therefore exceeds the standard height of PC/104 adapters. It should only be used as top module on a stack. Additionally the PC/104-Plus bus only uses a downward connector and does not allow to use adapter cards of this type on top.



8. GRAPHICS INTERFACES

8.1 *Graphic Controller*

The MOPSlcd7 uses an integrated S3 ProSavage4 chip, a high-speed video controller, which is contained in the VIA Twister T chipset (north bridge). The S3 ProSavage4 chip features the following benefits:

- Full internal AGP 4x performance
- Optimized Shared Memory Architecture (SMA)
- 8 / 16 / 32 MB frame buffer using system memory
- Floating point triangle set-up engine
- Significant internal architectural upgrades
- Single cycle 128-bit 3D architecture
- 8M triangles/second setup engine
- 140M pixels/second trilinear fill rate
- Microsoft Direct X texture compression
- Next generation, 128-bit 2D graphics engine
- Support for flat-panel monitor
- 2D/3D resolutions up to 1920x1440
- 3D-rendering features
- 2D-hardware-acceleration features
- Motion video architecture
- Extensive LCD support
- Integrated 2-channel, 110MHz LVDS interface
- Support for all resolutions up to 1600x1200

The graphics controller on board the MOPSlcd7 supports CRT monitors and a variety of LCD panels with up to 2x18 Bit and resolutions up to UXGA (1600x1200). 2x24bit panels are only supported if they can work in 2x18bit compatible mode. Display connections are simplified by using the JUMPtec Intelligent LVDS Interface (JILI). This interface can recognize which display is connected and then independently set all video parameters. Setting jumpers or changing software is not required. Because nearly all LCDs use different connectors, pinout, or LCD voltages, this is the easiest and safest way to configure different panels.

8.2 CRT Connector

The CRT monitor interface is available through the J9 connector (6 pins). To have the signals available on a standard DSUB-15 CRT monitor connector, an adapter cable is required. A 15-pin DSUB cable is available from Kontron (KAB-VGA-2, Part Number 96053-0000-00-0).

Header	Pin	Signal Name	Function	DSUB-25
	1	RED	Analog video red	1
	2	GRN	Analog video green	2
	3	BLU	Analog video blue	3
	4	GND	Signal ground	7
	5	VSYNC	Vertical sync	14
	6	HSYNC	Horizontal sync	13

To find the location of the CRT connector on the MOPSlcd7 board, please see the Appendix E: Connector Layout chapter.

8.3 LCD Panel Connector

The interface for the LCD Panel is available through the J13 connector (40 pins) on the top side of the board. This connector represents the JILI interface (**J**UMPtec **I**ntelligent **L**VDS **I**nterface). The implementation of this subsystem complies with the JILI Specification of Kontron Embedded Modules GmbH. The MOPSlcd7 already supports the JILI3 implementation. A variety of cables for different display types are available from Kontron. Please refer to the actual cable list on the Kontron Web site for part numbers and cable names. A detailed description of the JILI interface standard also is available in a separate document JILIM???.PDF. The three question marks represent the documents revision number. You can download this document from the Kontron Web site, or contact your local Kontron technical support to receive it.

To find the location of the LCD Panel interface connector on the MOPSlcd7 board, please see the Appendix E: Connector Layout chapter.

8.4 Display Power Considerations

When using a LCD Panel, additional voltages may be required to drive the displays logic, supply the backlight converter and the display's contrast voltage.

The display logic may require +5V for standard or +3.3V for low-power LCDs. Contrast voltages for passive displays are normally very different and can range from –30V to +30V. Backlight converters usually are +5V or +12V types. When using a Kontron JILI cable, you do not need to determine such configurations. Display logic voltage and contrast voltage come preconfigured on the JILI cable. On occasion, backlight voltage has to be adjusted on the cable.

Even though the MOPSlvdVE is a +5V-only board, you need to supply the +12V for the backlight converter additionally when using such a converter type.

The onboard 3.3V-circuitry of the MOPSlcd7 and the +3.3V logic voltage of low-voltage panels are powered by separate voltage regulators. The one for the LCD is mounted on the JILI adapter cable.

8.5 Connecting a LCD Panel

To determine whether your panel display is supported, check the Kontron Web site for panel lists. We regularly update the list of panels that have been tested with the MOPSlcd7.

Many panel adapters for a wide spread variety of displays are available through Kontron. If you use one of those adapters supplied by Kontron, configuration is easy:

1. Check whether you have the correct adapter and cable for the panel you plan to use. Inspect the cable for damages.
2. Disconnect the power from your system.
3. Connect the panel adapter to the LCD Panel connector (JILI interface) on the MOPSlcd7.
4. Connect the other end of the cable to your display.
5. Connect the backlight converter.
6. Supply power to your system.
7. If no image appears on your display, connect a CRT monitor to the CRT connector.
8. If necessary program the EEPROM on the JILI cable with the matching configuration data.
9. If you still do not see improvement, consider contacting the dealer for technical support.

8.6 Configuration

You can set the general configuration for the graphic controller in the BIOS setup utility. Refer to the Advanced Chipset Control submenu and the Display Control submenu in the Appendix B: BIOS Operation chapter for more configuration information.

You can download available drivers for the graphics controller from the Kontron Web site. For further information read the read-me or help files or contact technical support.

8.7 Graphics Technical Support

If problems occur, you can solve some of them by using the latest drivers for the graphics controller. Kontron provides you with the latest tested drivers, which can differ from newer ones. For further technical support, contact either Kontron, or obtain support information and downloadable software updates from VIA Technologies or S3.

8.8 Available Video Modes

The following list shows the video modes supported by the graphics controller with maximum frame buffer size. When configured for smaller frame buffers and/or using a LCD panel on the JILI interface, not all of the video modes listed below may be available. Capability depends on system configuration and on display capabilities. Different operating systems also may not support all listed modes by the available drivers.

Standard IBM-Compatible VGA Modes

Video Mode	Type	Characters/Pixels	Colors/Gray val.
00h/01h	Text	40x25	16
02h/03h	Text	80x25	16
04h/05h	Graphics	320x200	4
06h	Graphics	640x200	2
0Dh	Graphics	320x200	16
0Eh	Graphics	640x200	16
0Fh	Graphics	640x350	Mono
10h	Graphics	640x350	16
11h	Graphics	640x480	2
12h	Graphics	640x480	16
13h	Graphics	320x200	256

Extended VESA VGA Modes

VESA	Display	Pixels	Colors
100h	Graphics	640x400	256
101h	Graphics	640x480	256
102h	Graphics	800x600	16
103h	Graphics	800x600	256
105h	Graphics	1024x768	256
107h	Graphics	1280x1024	256
10Eh	Graphics	320x200	64K
10Fh	Graphics	320x200	16M
111h	Graphics	640x480	64K
112h	Graphics	640x480	16M
114h	Graphics	800x600	64K
115h	Graphics	800x600	16M
117h	Graphics	1024x768	64K
118h	Graphics	1024x768	16M
11Ah	Graphics	1280x1024	64K
11Bh	Graphics	1280x1024	16M
11Dh	Graphics	640x400	64K
11Eh	Graphics	640x400	16M
120h	Graphics	1600x1200	256
122h	Graphics	1600x1200	64K
124h	Graphics	1600x1200	16M
12Eh	Graphics	320x200	256
131h	Graphics	320x240	256
133h	Graphics	320x240	64K
134h	Graphics	320x240	16M
13Bh	Graphics	1400x1050	256
13Ch	Graphics	1400x1050	64K
13Eh	Graphics	1400x1050	16M
141h	Graphics	400x300	256
143h	Graphics	400x300	64K
144h	Graphics	400x300	16M
151h	Graphics	512x384	256
153h	Graphics	512x384	64K
154h	Graphics	512x384	16M

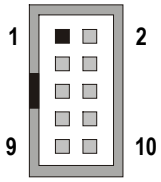
9. SERIAL-COMMUNICATION INTERFACES

Two fully functional serial ports (COMA and COMB) provide asynchronous serial communications. COMA and COMB support RS-232 operation modes. They are 16550 high-speed UART compatible and support 16-byte FIFO buffers for transfer rates from 50baud to 115.2Kbaud.

9.1 *Connectors*

COMA is available through the J11 connector (10 pins) and COMB through the J4 connector (10 pins). To have the signals available on the standard serial interface connectors DSUB9 or DSUB25, an adapter cable is required. A 9-pin DSUB cable is available from Kontron (KAB-DSUB9-2, Part Number 96017-0000-00-0).

The following table shows the pinouts for COMA and COMB, as well as necessary connections for DSUB adapters.

Header	Pin	Signal Name	Function	In / Out	DSUB-25	DSUB-9
	1	/DCD	Data Carrier Detect	In	8	1
	2	/DSR	Data Set Ready	In	6	6
	3	RxD	Receive Data	In	3	2
	4	/RTS	Request to Send	Out	4	7
	5	TxD	Transmit Data	Out	2	3
	6	/CTS	Clear to Send	In	5	8
	7	/DTR	Data Terminal Ready	Out	20	4
	8	/RI	Ring Indicator	In	22	9
	9	GND	Signal Ground	--	7	5
	10	VCC *	+5V	--	--	--

Notes: (*) To protect the external power lines of peripheral devices, make sure that:
-- the wires have the right diameter to withstand the maximum available current
-- the enclosure of the peripheral device fulfils the fire-protecting requirements of
-- IEC/EN 60950.

To find the location of the serial ports on the MOPSlcd7 board, please see the Appendix E: Connector Layout chapter.

9.2 *Configuration*

You can set the two serial input/output interfaces to a variety of I/O addresses and IRQ configurations. Settings are changeable from the MOPSlcd7 BIOS menu. Refer to the I/O Device Configuration submenu in the Appendix B: BIOS Operation chapter for configuration information.

Note: Most operating systems detect the serial port with the I/O address 3F8h as COM1 and 2F8h as COM2.

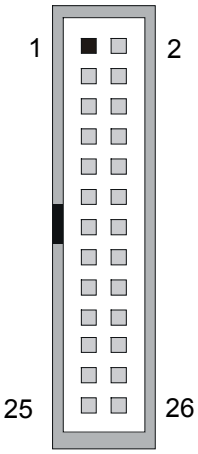
10. PARALLEL-PORT INTERFACE

The MOPSlcd7 incorporates a parallel port that can be set to uni-directional and supports EPP and ECP operating modes.

10.1 *Connector*

The parallel port is available through the J12 connector (26 pins). To have the signals available on a standard, parallel-interface connector DSUB-25, an adapter cable is required, which is offered by Kontron (KAB-DSUB25-1, Part Number 96015-0000-00-0).

The following table shows the pinout as well as necessary connections for a DSUB-25 adapter.

Header	Pin	Signal Name	Function	In / Out	DSUB-25
	1	/STB	Strobe	Out	1
	3	PD0	Data 0	I/O	2
	5	PD1	Data 1	I/O	3
	7	PD2	Data 2	I/O	4
	9	PD3	Data 3	I/O	5
	11	PD4	Data 4	I/O	6
	13	PD5	Data 5	I/O	7
	15	PD6	Data 6	I/O	8
	17	PD7	Data 7	I/O	9
	19	/ACK	Acknowledge	In	10
	21	/BUSY	Busy	In	11
	23	PE	Paper out	In	12
	25	/SLCT	Select out	In	13
	2	/AFD	Autofeed	Out	14
	4	/ERR	Error	In	15
	6	/INIT	Init	Out	16
	8	/SLIN	Select in	Out	17
	26	VCC *	+ 5 V	--	NC
	10,12	GND	Signal Ground	--	18 - 25
	14,16	GND	Signal Ground	--	18 - 25
	18,20	GND	Signal Ground	--	18 - 25
	22,24	GND	Signal Ground	--	18 - 25

Notes: (*) To protect the external power lines of peripheral devices, make sure that:
-- the wires have the right diameter to withstand the maximum available current
-- the enclosure of the peripheral device fulfils the fire-protecting requirements of
-- IEC/EN 60950.

To find the location of the parallel port on the MOPSlcd7 board, please see the Appendix E: Connector Layout chapter.

10.2 *Configuration*

The parallel-port mode, I/O addresses, and IRQs are changeable in the MOPSlcd7 BIOS Setup Utility. You can program the base I/O-address 378h, 3BCh, 278h, disable the interface or set it to AUTO. You can choose IRQ5 or IRQ7 as the parallel-port interrupt. In ECP mode, you can choose DMA 1 or DMA 3.

Refer to the I/O Device Configuration Submenu in the Appendix B: BIOS Operation chapter for additional information on configuration.

11. KEYBOARD INTERFACE

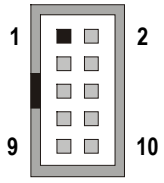
The keyboard and feature connector of the MOPSlcd7 offers four functions. The interface connects the following:

- Keyboard
- Speaker
- Battery
- Reset Button

11.1 *Connector*

The keyboard and feature connector is available through Connector J14 (10 pins). An adapter cable is required to connect a standard keyboard to this interface. There are two adapter cables available from Kontron. One can be used for AT-keyboard (KAB-KB-1, Part Number 96023-0000-00-0), the other for PS/2-keyboard (KAB-KB-PS2, Part Number 96060-0000-00-0). The adapter cables do not know the other functions on this interface.

The following table shows the pinout as well as necessary connections for adapters.

Header	Pin	Signal Name	Function	5-pin Din (Diode)	6-pin MiniDin (PS2)
	1	Speaker	Speaker output		
	2	GND	Ground		
	3	/RESIN	Reset input		
	4	NC **	Not connected		
	5	KBDAT	Keyboard data	2	1
	6	KBCLK	Keyboard clock	1	5
	7	GND	Ground	4	3
	8	VCC *	+5V	5	4
	9	BATT	Battery in (3,0V)		
	10	PWRGOOD	Powergood		

Notes: (*) To protect the external power lines of peripheral devices, make sure that:
-- the wires have the right diameter to withstand the maximum available current
-- the enclosure of the peripheral device fulfils the fire-protecting requirements of
-- IEC/EN 60950.
(**) This pin is /KBLOCK on other MOPS products and not supported on MOPSlcd7.

To find the location of the keyboard and feature connector on the MOPSlcd7 board, please see the Appendix E: Connector Layout chapter.

11.2 Signal Descriptions

/RESIN and PWRGOOD (Reset Inputs)

- Input on CPU modules
- When POWERGOOD goes high, it starts the reset generator on the CPU module to pull the onboard reset line high after a valid reset period. You also can use this pin as a low active hardware reset for modules.

Speaker

- Open collector output on modules that drive a piezo electronic speaker.
- Input on modules that connects a 5V piezo electronic speaker to this pin.
- An 8-Ohm loudspeaker also can be connected between SPEAKER and GND, but because of current limitation the volume will be low.
- Connect only one speaker to this pin. The CPU usually drives this pin. However, other modules also can use this signal to drive the system speaker.

KBDAT (Keyboard Data)

- Bi-directional I/O pin on CPU modules
- Keyboard data signal

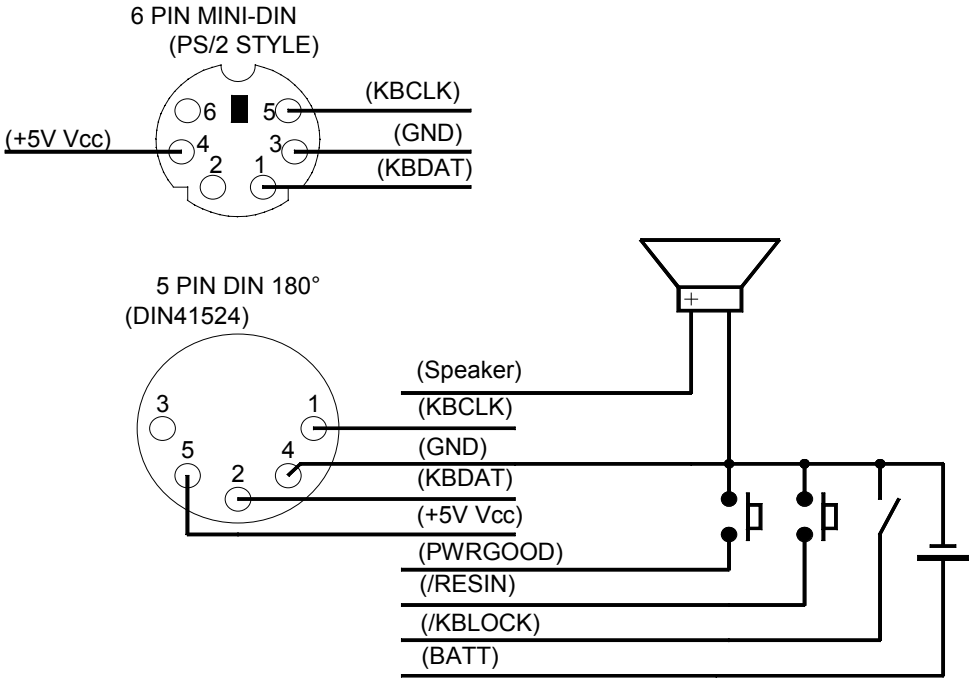
KBCLK (Keyboard Clock)

- Bi-directional I/O pin on CPU modules
- Keyboard clock signal

BATT (System Battery Connection)

- This pin connects a system battery to all modules.
- The battery voltage has to be higher than 2.4V and lower than 3.6V. A 3V battery is recommended.
- A battery is not needed to hold CMOS setup data. Your configurations for hard disks, floppy drives, and other peripherals are saved in an onboard EEPROM. However, you need a battery to save the CMOS date and time when power supply is turned off.

11.2.1. Example Connection AT-keyboard and Other Functions



11.3 *Configuration*

See the Keyboard Features submenu in the Appendix B: BIOS Operation to set the Numlock, Key Click, Keyboard Auto-repeat Rate, and the Keyboard Auto-repeat Delay.

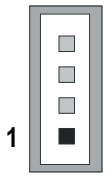
12. PS/2-MOUSE INTERFACE

The super chipset of the MOPSlcd7 supports a PS/2 mouse.

12.1 *Connector*

The PS/2 mouse interface is available on Connector J15 (4 pins). An adapter cable is required to connect a standard PS/2 mouse. The cable is available from Kontron (KAB-MOUSE-PS2, Part Number 96062-0000-00-0).

The following table shows the pinout and connections for a PS/2 mouse adapter.

Header	Pin	Signal Name	Function	6-pin MiniDin (PS2)
	1	MSDAT	Mouse data	1
	2	VCC *	+5V	4
	3	GND	Ground	3
	4	MSCLK	Mouse clock	5

Notes: (*) To protect the external power lines of peripheral devices, make sure that:
-- the wires have the right diameter to withstand the maximum available current
-- the enclosure of the peripheral device fulfils the fire-protecting requirements of
-- IEC/EN 60950.

To find the location of the PS/2 mouse connector on the MOPSlcd7 board, please see the Appendix E: Connector Layout chapter.

12.2 *Configuration*

You can set the PS/2 mouse to enabled, disabled or auto detect from the BIOS Setup. If you enable the mouse, the IRQ12 is used as the interrupt and is no longer available for other devices. Please refer to the Advanced Menu in the Appendix B: BIOS chapter for additional information on configuration.

13. USB INTERFACE

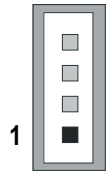
The USB interface of the MOPSlcd7 is integrated in the VT82C686B south bridge. It comes with two USB ports, which follow the UHCI specification and are USB-1.1 compliant.

You can expand the amount of USB connections by adding external hubs. You can connect up to 127 USB peripherals to each hub.

13.1 *Connector*

The USB ports are available through the J7 and J8connectors (each 4 pins). To have the signals available on the standard USB interface connectors, an adapter cable is required. An USB interface cable is available from Kontron (KAB-USB-1, Part Number 96054-0000-00-0).

The following table shows the pinouts for the USB connectors.

Header	Pin	Signal Name	Function
	1	VCC *	+5V
	2	USB0	USB-
	3	USB1	USB+
	4	GND	Ground

Notes: (*) To protect the external power lines of peripheral devices, make sure that:
-- the wires have the right diameter to withstand the maximum available current
-- the enclosure of the peripheral device fulfils the fire-protecting requirements of
-- IEC/EN 60950.

To find the location of the USB ports on the MOPSlcd7 board, please see the Appendix E: Connector Layout chapter.

13.2 *Configuration*

Configuration entries are available for the USB ports in the BIOS Setup Utility. You can enable/disable the USB controller as well as the USB legacy support. Please refer to the I/O Device Configuration submenu in the Appendix B: BIOS chapter for information.

13.3 Limitations

The power contacts for USB devices on Pin 1 and Pin 4 are not protected. They are suitable to supply connected USB devices with a maximum of 500mA power dissipation. Do not supply external USB devices with higher power dissipation through these pins. Always use a fuse for power on external USB connectors, otherwise a defective USB device may damage the M0PSlcd7. Kontron recommends using a resetable fuse, which follows the USB 1.1 specification, for power on external USB connectors.

14. FLOPPY-DRIVE INTERFACE

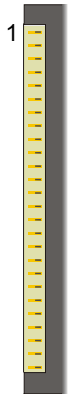
The floppy-drive interface of the MOPSlcd7 uses a 2.88MB super I/O floppy-disk controller and can support one floppy disk drive with densities that range from 360kB to 2.88MB. The controller is 100% IBM compatible.

14.1 *Connector*

The floppy disk interface is available on the flat-foil connector J6 (26 pins). This type of connector is often internally used in notebooks to connect a slim-line floppy drive.

Accessories are available for this interface from Kontron. To connect a standard 3.5" floppy drive, use an adapter cable (ADA-FLOPPY-2, Part Number 96001-0000-00-0). If you have a slim-line 3.5" floppy drive, you may need a flat foil cable (KAB-FLOPPY/MOPS-1, Part Number 96019-0000-00-0). It also is possible to get a slim line 3.5" floppy drive with cable from Kontron (FLOPPY-MOPS-1, Part Number 96010-0000-00-0).

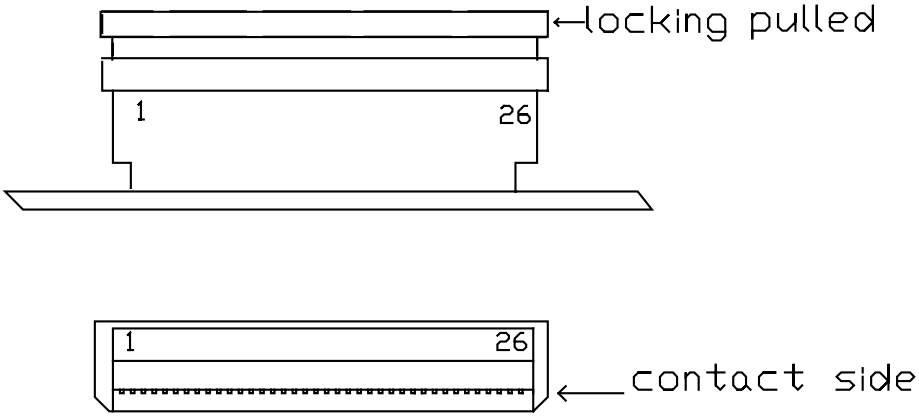
The following table shows the connector pinout.

Header	Pin	Signal Name	Function	Pin	Signal Name	Function
	1	VCC *	+5V	2	/IDX	Index
	3	VCC *	+5V	4	/DR0	Drive Select 0
	5	VCC *	+5V	6	/DSKCHG	Disk Change
	7	NC	Not connected	8	NC	Not connected
	9	NC	Not connected	10	/MTR0	Motor on 0
	11	NC	Not connected	12	/FDIR	Direction Select
	13	NC	Not connected	14	/STEP	Step
	15	GND	Ground	16	/WDATA	Write Data
	17	GND	Ground	18	/WGATE	Write Gate
	19	GND	Ground	20	/TRK0	Track 00
	21	GND	Ground	22	/WRTPRT	Write Protect
	23	GND	Ground	24	/RDATA	Read Data
	25	GND	Ground	26	/HDSEL	Side One Select

Notes: (*) To protect the external power lines of peripheral devices, make sure that:
-- the wires have the right diameter to withstand the maximum available current
-- the enclosure of the peripheral device fulfils the fire-protecting requirements of
-- IEC/EN 60950.

To find the location of floppy-drive interface on the MOPSlcd7 board, please see the Appendix E: Connector Layout chapter.

14.1.1. Connector Diagram



14.2 *Configuration*

You can configure the floppy disk interface in the BIOS Setup Utility. You can choose the 3.5" (common) or 5.25" drive types with densities of 360kB, 720kB, 1.2MB, 1.25MB, 1.44MB or 2.88MB. Refer to the Main Menu section of the Appendix B: BIOS Operation chapter for more information on configuring the floppy drive.

You also can disable the floppy-disk interface in the I/O Device Configuration Submenu.

15. IDE INTERFACE

The MOPSlcd7 features one EIDE interface (Ultra DMA 33 mode) that can drive two hard disks. When two devices share a single adapter, they are connected in a master/slave, daisy-chain configuration. If only one drive is in the system, you must set it as the master.

15.1 *Connector*

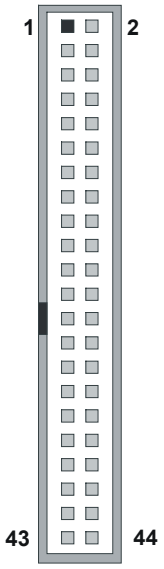
The IDE interface is available through Connector J3 (44 pins). This interface is designed in 2mm grid for optimal connectivity to a 2.5" hard disk.

There are several accessories available for IDE connectivity.

You can use two cables to directly connect a hard disk in a 2.5" form factor (KAB-IDE-2MM, Part Number 96021-0000-00-0) or a 3.5" form factor (KAB-IDE-25, Part Number 96020-0000-00-0).

You can plug a Kontron chipDISK, which is an IDE hard disk that uses Flash technology, into the IDE interface and mechanically mount it by using a mini-spacer on the chipDISK hole. You also can use a chipDISK adapter (chipDISK-ADA1, Part Number 96004-0000-00-0) or compact Flash adapter (CFC-ADA1, Part Number 96004-0000-00-2) for more disk support.

The following table shows the pinout.

Header	Pin	Signal Name	Function	Pin	Signal Name	Function
	1	/RESET	Reset	2	GND	Ground
	3	HDD7	Data 7	4	HDD8	Data 8
	5	HDD6	Data 6	6	HDD9	Data 9
	7	HDD5	Data 5	8	HDD10	Data 10
	9	HDD4	Data 4	10	HDD11	Data 11
	11	HDD3	Data 3	12	HDD12	Data 12
	13	HDD2	Data 2	14	HDD13	Data 13
	15	HDD1	Data 1	16	HDD14	Data 14
	17	HDD0	Data 0	18	HDD15	Data 15
	19	GND	Ground	20	Key (NC)	Key pin
	21	DRQ	IDE DMA Request	22	GND	Ground
	23	/IOW	I/O write	24	GND	Ground
	25	/IOR	I/O read	26	GND	Ground
	27	IOCHRDY	I/O channel ready	28	CSEL**	Cable Select
	29	/ACK	Acknowledge	30	GND	Ground
	31	IRQ	Interrupt	32	NC	Not connected
	33	SA1	Addr 1	34	/PDIAG	Passed Diag
	35	SA0	Addr 0	36	SA2	Addr 2
	37	/CS1	Chip select 1	38	/CS3	Chip select 3
	39	NC	Not connected	40	GND	Ground
	41	VCC *	+5V	42	VCC Motor *	+5V
	43	GND	Ground	44	NC	Not connected

Notes: (*) To protect the external power lines of peripheral devices, make sure that:
-- the wires have the right diameter to withstand the maximum available current
-- the enclosure of the peripheral device fulfils the fire-protecting requirements of
-- IEC/EN 60950.

(**) Pin 28 is connected with 470Ω to Ground for Cable Select IDE devices.

To find the location of IDE interface on the MOPSlcd7 board, please see the Appendix E: Connector Layout chapter.

15.2 *Configuration*

The IDE interface offers several configuration settings. Refer to the Main menu and the I/O Device Configuration submenu section in the Appendix B: BIOS Operation chapter for additional information on configuration.

16. ETHERNET CONTROLLER

The MOPSlcd7 uses a Davicom DM9102A PCI Fast Ethernet Controller. The network controllers support 10/100Base-T interfaces. The devices auto-negotiate the use of a 10Mbit/sec or 100Mbit/sec connection. You can enable an onboard LAN RPL ROM to support the boot up of the system via Ethernet and a PXE-boot server.

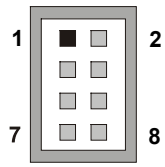
The Davicom DM9102A provides the following features:

- Integrated Fast Ethernet MAC, Physical Layer, and transceiver on one chip
- Compliance with PCI Specification 2.2
- PCI-bus-master architecture
- EEPROM 93C46 interface supports node ID, access-configuration information
- Compliance with IEEE 802.3u 100Base-TX and 802.3 10Base-T
- Compliance with IEEE 802.3u autonegotiation protocol for automatic link- type selection
- Full-duplex/half-duplex capability
- Support IEEE 802.3x Full Duplex Flow Control
- Digital clock recovery circuit using advanced digital algorithm to reduce jitter
- High-performance 100Mbps clock generator and data-recovery circuit
- Loopback mode for easy system diagnostics

16.1 Connector

The Ethernet interface is available through Connector J5 (8 pins). To have the signals of the Ethernet connection available on a standard RJ45 connector, you need an adapter cable, which is offered by Kontron (KAB-MOPS-ETN1, Part Number 96048-0000-00-0).

The following table shows the pinout.

Header	Pin	Signal Name	Function	In/Out
	1	TXD+	10BASE-T Transmit	Differential Output
	2	TXD-	10BASE-T Transmit	Differential Output
	3	RXD+	10BASE-T Receive	Differential Input
	4	SHLDGND	Shield ground	
	5	SHLDGND	Shield ground	
	6	RXD-	10BASE-T Receive	Differential Input
	7	SHLDGND	Shield ground	
	8	SHLDGND	Shield ground	

Notes: TXD+, TXD- differential-output pair drives 10 and 100Mb/s Manchester-encoded data to 100/10BASE-T transmit lines.
RXD+, RXD- differential input pair receives 10 and 100Mb/s Manchester-encoded data from 100/10BASE-T receive lines.

To find the location of the Ethernet interface on the MOPSlcd7 board, please see the Appendix E: Connector Layout chapter.

16.2 Configuration

The onboard Davicom DM9102A Ethernet controller cannot be disabled in BIOS setup utility, it is permanently available.

You can download available drivers from the Kontron Web site. For further information read the read-me file or contact technical support.

16.3 Ethernet Technical Support

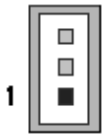
If any problems occur, you can solve some of them by using the latest drivers for the Davicom DM9102A controller. Kontron provides you with the latest Kontron-tested drivers, which can differ from newer ones. For further technical support, contact either Kontron or get support information and downloadable software updates from Davicom.

17. FAN INTERFACE

Use the fan connector to connect a fan to cool the CPU. The connector and the system controller support the speed monitoring of the fan. This connector only supports 5V fans.

17.1 *Connector*

The fan connector is available through Connector J10 (3 pins).

Header	Pin	Signal Description	Function
	1	VCC*	+5V Power supply for fan.
	2	GND	Ground
	3	+12V*	+12V

Notes: (*) To protect the external power lines of peripheral devices, make sure that:
-- the wires have the right diameter to withstand the maximum available current
-- the enclosure of the peripheral device fulfils the fire-protecting requirements of
-- IEC/EN 60950.

To find the location of the fan connector on the MOPSlcd7 board, please see the Appendix E: Connector Layout chapter.

17.2 *Configuration*

You do not need to configure this feature.

18. POWER CONNECTOR

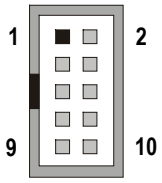
In some applications, the MOPSlcd7 is intended for use as a stand-alone module without a backplane. You need to have a power connector available on the board for direct power supply. The MOPSlcd7 is a +5V-only board. Peripherals can obtain additional voltage from the power connector next to the PC/104 bus. The additional voltages (+12V, -5V and -12V) are not generated onboard the MOPSlcd7.

Note: The MOPS*lcd7* is equipped with an onboard DC/DC converter to supply +3.3V to the PC/104-Plus connector. Adapter cards powered by this supply voltage are only allowed to consume up to maximum 1.5A from this converter.
Other products of the MOPS family do not supply +3.3V to the PC/104-Plus connector.

18.1 *Connector*

The power connector is available as J1 (10 pins).

The following table shows the pinout.

Header	Pin	Signal Name	Function
	1	+12V	+12V
	2	GND	Ground
	3	VCC	+5V
	4	VCC	+5V
	5	GND	Ground
	6	GND	Ground
	7	VCC	+5V
	8	VCC	+5V
	9	GND	Ground
	10	+12V	+12V

To find the location of the power connector on the MOPSlcd7 board, please see the Appendix E: Connector Layout chapter.

18.2 *Configuration*

The MOPSlcd7 is equipped with a power management system (APM). You can configure lots of options for power-saving states such as standby state with partial power reduction and suspend state with full-power reduction. You can specify wake-up events that bring the system back to full-on state. Please refer to the Power menu section in the Appendix B: BIOS Operation chapter for more information about power savings.

18.3 Power Pins

Every power pin on the power connector as well as on the PC/104 bus connector is limited to a maximum current of 1A per pin.

If a system using a MOPSlcd7 is only supplied from the power connector, the following limitations apply:

Power	Number of Pins	Max. Current
VCC (+5V)	4	4A
+12V	2	2A
-12V	-	-
-5V	-	-
GND	4	4A

A system using the MOPSlcd7 also can be supplied from the PC/104 bus connectors. If only those supply voltages pins are used, the following limitations apply:

Power	Number of Pins on ISA Part	Max. Current
VCC (+5V)	4	4A
+12V	2	2A
-12V	2	2A
-5V	2	2A
GND	8	8A

Modules on the PC/104 bus consuming a higher supply current must provide power supply through an additional connector.

Note: The MOPSlcd7 is not a replacement for a backplane. Use all power pins on the power connector and on the PC/104 connectors for power supply to the MOPSlcd7, and also use all additional power connectors on additional I/O cards if your system exceeds the above limitations. It is not acceptable to use only the power pins of the PC/104 connector for power supply to the full PC/104 stack.

18.4 External Battery

You can connect an external battery only on Pin 9 of the Keyboard connector. For more information refer to the Keyboard chapter of this manual.

19. WATCHDOG TIMER

The watchdog timer is integrated in an onboard PIC controller of the MOPSlcd7 and can issue a reset to the system or generate a non-maskable interrupt (NMI). The watchdog timer circuit has to be triggered within a specified time by the application software. If the watchdog is not triggered because proper software execution fails or a hardware malfunction occurs, it will reset the system or generate the NMI.

19.1 *Configuration*

You can set the watchdog timer to disabled, reset or NMI mode. You can specify the delay time from 1 second to 30 minutes and timeout (trigger period) from 0.4 second up to 10 minutes. The delay time is the time after first initialization before the trigger period starts. The timeout is the time the watchdog has to be triggered within. You can make the initialization settings in the BIOS setup. Refer to the Watchdog Settings Submenu in the Appendix B: BIOS Operation chapter for information on configuration.

19.2 *Programming*

19.2.1. Initialization

You can initialize the watchdog timer from the BIOS setup. You also can set up the initialization from the application software with help of the JIDA (Jumptec Intelligent Device Architecture) programmer's interface or by using low-level programming.

19.2.2. Trigger

The watchdog needs to be triggered out of the application software within a specified timeout period. You can only do this in the application software by using low-level programming or with help of the JIDA programmer's interface.

For information about low-level programming for the watchdog timer, refer to Application Note WdogPVC3_E???.DOC, which you can request from Kontron technical support.

For information about the JIDA programmer's interface refer to the JIDA BIOS extension section in the Appendix B: BIOS chapter and separate documents available in the JIDA software packages on the Kontron Web site.

20. SYSTEM CONTROLLER

National Semiconductor's LM84 monitors several critical hardware parameters of the system, including power-supply voltages and temperatures, which are very important for a high-end computer system to remain stable and properly. The LM84 is connected via the system management (SM) bus to the south bridge.

The following parameters are monitored:

- +3.3V from onboard DC/DC
- Gun Transceiver Logic (GTL) voltage
- CPU core voltage
- +2.5 onboard voltage
- +5V
- LM84 local temperature
- CPU temperature with on-die diode

20.1 *Configuration*

You can use the Hardware Monitor submenu in the BIOS Setup Utility to obtain information on power plane voltages and to check the temperatures on the LM84 sensor and the CPU die. For more information on this submenu, see the Appendix B: BIOS Operation chapter in this manual.

To monitor the parameters of this feature from your operating system, Kontron recommends that you use the 32-bit protected mode JUMP*tec*'s Intelligent Device Architecture 32-bit driver (JIDA 32) with the test and demo application for Windows 95/98/ME/NT/2000/XP, which is available on the KONTRON Web site.

There are several monitoring programs on the market that can work with SM-Bus controllers like the LM84 (e.g. MBM Motherboard Monitor or Hardware Monitor), too. Please search the Web for such monitoring programs. KONTRON does not provide support for these tools, because they are not sold by us.

21. APPENDIX A: SYSTEM-RESOURCE ALLOCATION

21.1 *Interrupt Request Lines*

Please note that Kontron PC/104 devices were designed after the draft of P996 Specification for ISA systems. Because of this, shareable interrupts are not supported. Some PC/104 add-on board manufacturers do not follow the P996 Specification and allow shareable interrupts. If you want to use such PC/104 boards with Kontron devices, contact the manufacturer of the add-on board and ask about switching to non-interrupt sharing.

IRQ #	Use	Available	Comment
0	Timer0	No	
1	Keyboard	No	
2	Cascade	No	
3	COM2	No	Note (1), Note (2)
4	COM1	No	Note (1), Note (2)
5		Yes	Note (3)
6	FDC	No	Note (1)
7	LPT1	No	Note (1), Note (3)
8	RTC	No	
9		Yes	
10	COM3	Yes	Note (4)
11	COM4	Yes	Note (4)
12	PS/2 Mouse	No	Note (1)
13	FPU	No	
14	IDE0	No	Note (1)
15	CompactFlash	No	Note (1)

Notes: (1) If the „used for“ device is disabled in setup, the corresponding interrupt is available for other devices.
(2) ATTENTION: BIOS settings determine which physical COM connector is assigned to a logical COM port.
(3) LPT1 also can be configured for IRQ5.
(4) Possible interrupts, if an external SMsC 669 Super-I/O controller is in the system

21.2 Direct Memory Access (DMA) Channels

DMA #	Used for	Available	Comment
0		Yes	
1		Yes	Note (3)
2	FDC	No	Note (1)
3	LPT	No	Note (2), Note (3)
4	Cascade	No	
5		Yes	
6		Yes	
7		Yes	

Notes: (1) If the „used for“-device is disabled in setup, the corresponding DMA channel is available for other devices.
(2) The DMA channel is only used in ECP mode of LPT, in other modes it is available.
(3) Possible alternative setting of LPT in ECP mode for used DMA channel.

21.3 I/O Address Map

The I/O-port addresses of the processor module MOPSlcd7 are functionally identical to a standard PC/AT. All addresses not mentioned in this table should be available. We recommend that you do not use I/O addresses below 0110hex with additional hardware for compatibility reasons, even if available.

I/O Address (h)	Use	Available	Comment
0000 - 001F	DMA Controller 1	No	Fixed
0010	System Control	No	Fixed
0020 - 003F	Interrupt Controller 1	No	Fixed
0040 - 005F	Timer, Counter	No	Fixed
0060 - 006F	Keyboard controller	No	Fixed
0070	NMI Enable Register	No	Fixed
0070 - 0077	Real Time Clock and CMOS Registers	No	Fixed
0080	BIOS POST	No	Fixed
0081 - 008F	DMA Page Register	No	Fixed
0092	System Control	No	Fixed
00A0 00BF	Interrupt Controller 2	No	Fixed
00C0 - 00DF	DMA Controller 2	No	Fixed
00E0 - 00EF	System Control	No	Fixed
00F0 - 00FF	Math Coprocessor	No	Fixed
0100 - 010F	General Purpose I/O	No	Kontron Control Port, Fixed
01F0 - 01F7	Fixed Disk	No	Free, if device is disabled in setup
0278 - 027F		Yes	Free in standard configuration, but possible address of LPT1.
02E8 - 02EF		Yes	Free in standard configuration, but possible address of COM.
02F8 - 02FF	Serial Port 2	No	Default for COM B, free with different configuration.
0378 - 037F	Parallel Port 1	No	Default for LPT 1; free with different configuration.
03BC - 03C4		Yes	Free in standard configuration, but possible address of LPT1.
03C0 - 03DF	Video Control	No	Fixed
03E8 - 03EF		Yes	Free in standard configuration, but possible address of COM.
03F0 - 03F7	Diskette Controller	No	Free, if device is disabled in setup
03F8 - 03FF	Serial Port 1	No	Default for COM A, free with different configuration.
04D0 - 04D1	Interrupt Select	No	Fixed
0678 - 067A	LPT ECP Extension	Yes	Free in standard configuration, but possible adresses for ECP mode
0778 - 077A	LPT ECP Extension	No	Free, if LPT not used in ECP mode
07BC - 07C3	LPT ECP Extension	Yes	Free in standard configuration, but possible adresses for ECP mode
0CF8 - 0CFF	PCI Configuration	No	Fixed
1000 - 10FE	Ethernet Controller	No	Free, if device is disabled in setup
1400 - 14FE	IDE Controller	No	Free, if device is disabled in setup
1800 - 181F	USB Controller Port 0/1	No	Free, if device is disabled in setup
3400 - 347F	Distributed DMA	Yes	Distributed DMA will only be used when PCI extension cards supporting this feature are used.
6800 - 687F	Hardware Monitoring	No	Fixed
8000 - 807F	Power Management Unit	No	Fixed
8100 - 810F	System Management Bus Controller	No	Fixed

21.4 *Memory Map*

The MOPSlcd7 processor module can support up to 512MB memory modules. As the MOPSlcd7 uses Shared Memory Architecture (SMA) the amount of graphic memory reduces the available amount of system memory. The first 640KB of DRAM are used as main memory.

Using DOS, you can address 1MB of memory directly. Memory area above 1MB (high memory, extended memory) is accessed under DOS via special drivers such as HIMEM.SYS and EMM386.EXE, which are part of the operating system. Please refer to the operating system documentation or special textbooks for information about HIMEM.SYS and EMM386.EXE.

Other operating systems (Linux or Windows versions) allow you to address the full memory area directly.

Upper Memory	Use	Available	Comment
A0000h – BFFFFh	VGA Memory	No	Mainly used by graphic adapter cards.
C0000h – CBFFFh	VGA BIOS	No	The VGA-BIOS exceeds the standard area of C0000h - C7FFFh normally used by ISA VGA cards.
CC000h – DFFFFh		Yes	Free for ISA bus or shadow RAM in standard configurations. If onboard LAN RPL ROM is enabled, or JRC is used, a 16K block is shadowed for BIOS extensions, starting with first free area at CC000h or D0000h, D4000h, D8000hor DC000h. (BIOS extensions do not use the whole shadow block). UHCI Data Area in USB Legacy Support is starting at DC000h by default setting.
E0000h – F0000h	System BIOS	No	

21.4.1. Using Expanded Memory Managers

MOPSlcd7 extension BIOSes may be mapped to an upper memory area. (See the previous table.). Some add-on boards also have optional ROMs or use drivers that communicate with their corresponding devices via memory mapped I/O such as dual-ported RAM. These boards have to share the upper memory area with the Expanded Memory Manager's EMS frame. This often causes several problems in the system.

Most EMMs scan the upper memory area for extension BIOSes (optional ROMs) and choose a free memory area for their frame if it is not explicitly set. Normally, they are not always capable of detecting special memory-mapped I/O areas. You need to tell the EMM which memory areas are not available for the EMS frames, which is most of the time done by using special exclusion parameters.

If the Expanded Memory Manager you use cannot detect extension BIOSes (optional ROMs), make sure you excluded all areas in the upper memory, which are used by extension BIOSes, too. Your instruction in the CONFIG.SYS concerning the Expanded Memory Manager should look like this: (question marks for location of extension BIOS).

MS-DOS Example

```
DEVICE=EMM386.EXE X=????-???? X=E000-FFFF
```

Note: When booting up your system using this configuration under MS-DOS, the exclusion of area F000 to FFFF causes a warning. Microsoft reports that this message will always appear when the F000 segment lies in the shadow RAM. This is a bug of EMM386, not of the MOPSlcd7.

Please read the technical manuals of add-on cards used with the MOPSlcd7 for the memory areas they use. If necessary, also exclude their memory locations to avoid a conflict with the EMM.

21.5 PCI Devices

All devices follow the Peripheral Component Interconnect 2.1 (PCI 2.1) specification. The BIOS and OS control memory and I/O resources. Please see the PCI 2.1 specification for details.

PCI Device (IDSEL)	PCI IRQ	REQ / GNT	Comment
AGP Graphic	INTA#	-	Integrated in chipset
Ethernet DM9102 (AD13)	INTD#	Discrete channel for Ethernet	
USB Controller	INTD#	-	Integrated in chipset

Note: PC/104-Plus specification allows 3 external masters (REQ0, REQ1 and REQ2).

21.6 SM-Bus Devices

The MOPSlcd7 uses an onboard System Management (SM) Bus. This bus is not available on an peripheral connector and therefore cannot be used for external SM-Bus devices.

SM Bus Address	SM Device	Comment
9Ch/9Dh	Temp. Sensor (LM84)	Onboard temperature sensor.

Note: There are more devices connected to the SM-Bus than listed in this table, but access to these devices in not permitted. Don't access any other device addresses except those listed above.

22. APPENDIX B: BIOS OPERATION

The MOPSlcd7 uses the Phoenix BIOS 4.0, Release 6.1, which is located in the onboard Flash. The BIOS version displays onscreen during the POST at boot. The device has an 8-bit access. The shadow RAM feature offers faster access (16 bit). The onboard Flash EEPROM also holds some special Kontron BIOS extensions, which are loaded during boot up if the corresponding feature is enabled.

You can update the BIOS using a Flash utility.

22.1 *Determining the BIOS Version*

To determine the BIOS version of the MOPSlcd7, immediately press the **<Pause/Break>** key on your keyboard as soon as you see the following text display in the upper left corner of your screen:

```
PhoenixBIOS 4.0 Release 6.1
Copyright 1985-2003 Phoenix Technology Ltd.
All Rights Reserved
Kontron(R) BIOS Version <PVC3R112>
(C)Copyright 2004 Kontron Embedded Modules GmbH
```

Whenever you contact technical support about BIOS issues, providing a BIOS version <PVC3R???> is especially helpful.

The system BIOS provides additional information about the board's serial number, CPU, and memory information by displaying information similar to the following:

```
S/N: XK4090004

CPU = Intel(R) Mobile Pentium(R) III processor 500 MHz
639K System RAM Passed
55M Extended RAM Passed
256K Cache SRAM Passed
System BIOS shadowed
Video BIOS shadowed
```

The board's serial number has value to technical support. MOPSlcd7 serial numbers always start with XK and are followed by six or seven digits. The first digit represents the year of manufacturing, the next two digits stand for the lot number, and the last three or four digits are the number of the board in that lot.

In the example above, the board with the serial number XK4090004 was manufactured in year 2004, lot 9 of that year, and is board number 4 of that lot.

22.2 *Setup Guide*

The Phoenix BIOS Setup Utility changes system behavior by modifying the BIOS configuration. The setup program uses a number of menus to make changes and turn features on or off.

The BIOS setup menus documented in this section represent those found in most models of the MOPSlcd7. The BIOS setup for specific models can differ slightly.

Note: Selecting incorrect values may cause system boot failure. Load setup-default values to recover by pressing <F9>.

22.2.1. Start Phoenix BIOS Setup Utility

To start the Phoenix BIOS Setup Utility, press the **<F2>** key when the following string appears during boot up.

```
Press <F2> to enter Setup
```

The Main Menu then appears.

22.2.2. General Information

The **Setup Screen** is composed of several sections:

Setup Screen	Location	Function
Menu Bar	Top	Lists and selects all top-level menus.
Legend Bar	Bottom	Lists setup navigation keys.
Item Specific Help Window	Right	Help for selected item.
Menu Window	Left Center	Selection fields for current menu.
General Help Window	Overlay (center)	Help for selected menu.

Menu Bar

The menu bar at the top of the window lists different menus. Use the left/right arrow keys to make a selection.

Legend Bar

Use the keys listed in the legend bar on the bottom to make your selections or exit the current menu. The table below describes the legend keys and their alternates.

Key	Function
<F1> or <Alt-H>	General Help window.
<Esc>	Exit menu.
← or → Arrow key	Select a menu.
↑ or ↓ Arrow key	Select fields in current menu.
<Tab> or <Shift-Tab>	Cycle cursor up and down.
<Home> or <End>	Move cursor to top or bottom of current window.
<PgUp> or <PgDn>	Move cursor to next or previous page.
<F5> or <->	Select previous value for the current field.
<F6> or <+> or <Space>	Select next value for the current field.
<F9>	Load the default configuration values for this menu.
<F10>	Save and exit.
<Enter>	Execute command or select submenu.
<Alt-R>	Refresh screen.

Selecting an Item

Use the ↑ or ↓ key to move the cursor to the field you want. Then use the + and - keys to select a value for that field. **Save Value** commands in the **Exit** menu save the values displayed in all menus.

Displaying Submenus

Use the ← or → key to move the cursor to the submenu you want. Then press <Enter>. A pointer (▸) marks all submenus.Item Specific Help Window

The Help window on the right side of each menu displays the Help text for the selected item. It updates as you move the cursor to each field.

General Help Window

Pressing <**F1**> or <**ALT-F1**> on a menu brings up the General Help window that describes the legend keys and their alternates. Press <**Esc**> to exit the General Help window.

22.3 Main Menu

Feature	Option	Description
System Time	HH:MM:SS	Sets system time. Press <Enter> to move to MM or SS.
System Date	MM/DD/YYYY	Sets system date. Press <Enter> to move to DD or YYYY.
Legacy Diskette A	360 kilobits, 5 ¼ “ 1.2 MB, 5 ¼ “ 720 kilobits, 3 ½ “ **1.44/1.25 MB, 3 ½ “** 2.88 MB, 3 ½ “ Disabled	Sets type of floppy disk drive.
‣ Primary Master	Autodetected drive	Displays result of PM autotyping.
‣ Primary Slave	Autodetected drive	Displays result of PS autotyping.
SMART Device Monitoring	Disabled **Enabled**	Disables or enables IDE failure prediction
‣ Memory Shadow	Submenu	Opens Memory Shadow submenu.
‣ Memory Cache	Submenu	Opens Memory Cache submenu.
System Memory	N/A	Displays amount of conventional memory detected during boot-up.
Extended Memory *	N/A	Displays amount of extended memory detected during boot-up.
BIOS Date	MM/DD/YY	Displays date of BIOS

Notes: In the Option column, bold shows default settings.
(*) Extended Memory = capacity of memory module – selected frame buffer memory size

22.3.1. Master or Slave Submenus

Feature	Option	Description
Type	None User **Auto** CD-ROM ATAPI Removable IDE Removable Other ATAPI	None = Autotyping is not able to supply the drive type or end user has selected None, disabling any drive that may be installed. User = End user supplies the hdd information. Auto = Autotyping, the drive itself supplies the information. CD-ROM = CD-ROM drive. ATAPI Removable = Read- and writeable media e.g. LS120 and USB-ZIP IDE Removable = Removable HDDs Other ATAPI = for ATAPI devices not supported by other HDD features.
Cylinders	1 to 65,536	Number of cylinders.
Heads	1 to 256	Number of read/write heads.
Sectors	1 to 63	Number of sectors per track.
Maximum Capacity	N/A	Displays the calculated size of the drive in CHS.
Total Sectors	N/A	Number of total sectors in LBA mode.
Maximum Capacity	N/A	Displays calculated size of drive in LBA.
Multi-Sector Transfer	**Disabled** 2 sectors 4 sectors 8 sectors 16 sectors	Any selection except Disabled determines the number of sectors transferred per block. The standard is one sector per block.
LBA Mode Control	**Disabled** Enabled	Enabling LBA causes Logical Block Addressing to be used in place of CHS.
32-Bit I/O	**Disabled** Enabled	Enables 32-bit communication between CPU and IDE card. Requires PCI or local bus.
Transfer Mode	**Standard** Fast PIO 1 Fast PIO 2 Fast PIO 3 Fast PIO 4 FPIO 3 / DMA 1 FPIO 4 / DMA 2	Selects the method for transferring the data between the hard disk and system memory.
Ultra DMA Mode	**Disabled** MOD0 MOD1 MOD2	Selects UDMA mode to move data to/from the drive. Autotype the drive to select the optimum transfer mode. This feature is auto-detected.
SMART Monitoring	Disabled Enabled	Shows whether a disk supports SMART.

Note: In the Option column, bold shows default settings.

22.3.2. Memory Shadow Submenu

Feature	Option	Description
CC00 - CFFF	**Disabled** Enabled	Accesses to this upper memory region go to the ISA bus if Disabled or to local memory if Enabled.
D000 - D3FF	**Disabled** Enabled	See above.
D400 - D7FF	**Disabled** Enabled	See above.
D800 - DBFF	**Disabled** Enabled	See above.
DC00 - DFFF	**Disabled** Enabled	See above.

Note: In the Option column, bold shows default settings.

22.3.3. Memory Cache Submenu

Feature	Option	Description
Memory Cache	Disabled, **Enabled**	Enables or Disables L2 cache.
Cache System BIOS Area	Uncached **Write Protect**	Controls caching of system BIOS area.
Cache Video BIOS Area	Uncached **Write Protect**	Controls caching of system BIOS area.
Cache Extended Memory Area	Uncached Write Through Write Protect **Write Back**	Controls caching of system memory above 1MB.
CC00 - CFFF	**Disabled,** Write Through, Write Protect, Write Back	Disabled: block is not cached. Write Through: Write are cached and sent to main memory at once. Write Protect: Writes are ignored. Write Back: Writes are cached but not sent to main memory until necessary.
D000 - D3FF	**Disabled,** Write Through, Write Protect, Write Back	See above.
D400 - D7FF	**Disabled,** Write Through, Write Protect, Write Back	See above.
D800 - DBFF	**Disabled,** Write Through, Write Protect, Write Back	See above.
DC00 - DFFF	**Disabled,** Write Through, Write Protect, Write Back	See above.

Note: In the Option column, bold shows default settings.

22.4 Advanced Menu

Feature	Option	Description
▸ Advanced Chipset Control	Submenu	Opens Advanced Chipset Control submenu.
PNP OS Installed	Yes **No**	If system has a PNP OS, such as Win95, select Yes to let OS configure PNP devices not required for boot. Selecting No makes BIOS configure them.
Reset Configuration Data	Yes **No**	Yes erases all configuration data in Extended System Configuration Data (ESCD), which stores the configuration settings for plug-in devices. Select Yes when required to restore the manufacturer's defaults.
Secured Setup Configuration	**Yes** No	Yes prevents a Plug and Play OS from changing system settings.
▸ PCI Configuration	Submenu	Opens PCI Configuration submenu.
PS/2 Mouse	**Auto Detect** Enabled Disabled	Disabled prevents installed PS/2 mouse from functioning but frees IRQ12. Enabled forces the PS/2 mouse port to be enabled regardless if a mouse is present. Auto Detect enables the PS/2 mouse only if present during boot up.
▸ Keyboard Features	Submenu	Opens Keyboard Features submenu.
▸ I/O Device Configuration	Submenu	Opens I/O Device Configuration submenu.
▸ Hardware Monitor	Submenu	Opens Hardware Monitor submenu.
Large Disk Access Mode	**DOS** Other	Select DOS if you have DOS. Select Other if you have another OS, such as UNIX. A large disk has more than 1024 cylinders, more than 16 heads, or more than 63 sectors per track.
Halt On Errors	Yes **No**	Determines if errors detected during boot up cause system to halt.

Note: In the Option column, bold shows default settings.

22.4.1. Advanced Chipset Control Submenu

Feature	Option	Description
PCI Delay Transaction	**Enabled** Disabled	Latches PCI-to-ISA cycles into buffer to free the PCI bus.
Aperture Size	2M, 4M, 8M, 16M, 32M, **64M**, 128M, 256M	Select size of AGP graphics aperture. Half of installed system memory is normally the best choice.
Frame Buffer Size *	None, **8 MB**, 16 MB, 32 MB	Select size of VGA SMA frame buffer. None uses the minimum size for the onboard graphic to function correctly.
Enable Memory Gap	**Disabled** Conventional Extended	Turns part of system RAM off and frees address space (512kB-640kB or 15MB-16MB) for use with an option card.
Spread Spectrum Modulation	**Disabled** 0.25% 0.5%	Enables spread spectrum modulation of clock synthesizer.

Note: In the Option column, bold shows default settings.
(*) Selection for this entry reduces available system memory.

22.4.2. PCI Configuration Submenu

Feature	Option	Description
PCI IRQ Line 1	Disabled, **Auto Select** IRQ3, 4, 5, 7, 9, 10, 11, 12, 14, 15	Select IRQ for PCI interrupt INT A. Select Auto to let BIOS assign IRQ.
PCI IRQ Line 2	Disabled, **Auto Select** IRQ3, 4, 5, 7, 9, 10, 11, 12, 14, 15	Select IRQ for PCI interrupt INT B. Select Auto to let BIOS assign IRQ.
PCI IRQ Line 3	Disabled, **Auto Select** IRQ3, 4, 5, 7, 9, 10, 11, 12, 14, 15	Select IRQ for PCI interrupt INT C. Select Auto to let BIOS assign IRQ.
PCI IRQ Line 4	Disabled, **Auto Select** IRQ3, 4, 5, 7, 9, 10, 11, 12, 14, 15	Select IRQ for PCI interrupt INT D. Select Auto to let BIOS assign IRQ.
▸ PCI/PNP ISA UMB Region Exclusion	Submenu	Opens UMB Region Exclusion submenu.
▸ PCI/PNP ISA IRQ Resource Exclusion	Submenu	Opens IRQ Exclusion submenu.
Default Primary Video Adapter	**AGP** PCI	Selects the onboard AGP graphic adapter or an external PCI graphic adapter to be the boot display device
Assign IRQ to PCI VGA	**Yes** No	Some PCI graphic adapters need to be assigned to an IRQ

Note: In the Option column, bold shows default settings.

22.4.3. PCI/PNP ISA UMB Region Exclusion Submenu

Feature	Option	Description
CC00 - CFFF	**Available** Reserved	Reserves specified block of upper memory for use by legacy ISA devices.
D000 - D3FF	**Available** Reserved	Reserves specified block of upper memory for use by legacy ISA devices.
D400 - D7FF	**Available** Reserved	Reserves specified block of upper memory for use by legacy ISA devices.
D800 - DBFF	**Available** Reserved	Reserves specified block of upper memory for use by legacy ISA devices.
DC00 - DFFF	**Available** Reserved	Reserves specified block of upper memory for use by legacy ISA devices.

Note: In the Option column, bold shows default settings.

22.4.4. PCI/PNP ISA IRQ Exclusion Submenu

Feature	Option	Description
IRQ3	**Available** Reserved	Reserves specified IRQ for use by legacy ISA devices.
IRQ4	**Available** Reserved	See above.
IRQ5	**Available** Reserved	See above.
IRQ7	**Available** Reserved	See above.
IRQ9	**Available** Reserved	See above.
IRQ10	**Available** Reserved	See above.
IRQ11	**Available** Reserved	See above.
IRQ12	**Available** Reserved	See above.
IRQ14 *	**Available** Reserved	See above.
IRQ15	**Available** Reserved	See above.

Note: In the Option column, bold shows default settings.
(*) Only visible if the Local Bus IDE Adapter is disabled

22.4.5. Keyboard Features Submenu

Feature	Option	Description
Numlock	**Auto** On Off	On or Off turns NumLock on or off at boot-up. Auto turns NumLock on if it finds a numeric keypad.
Key Click	**Disabled** Enabled	Turns audible key click on.
Keyboard auto-repeat rate	**30/sec**, 26.7/sec, 21.8/sec, 13.3/sec, 10/sec, 6/sec, 2/sec	Sets number of times to repeat a keystroke per second if you hold the key down.
Keyboard auto-repeat delay	¼ sec, ½ **sec**, ¾ sec, 1 sec	Sets delay time after key is held down before it begins to repeat the keystroke.

Note: In the Option column, bold shows default settings.

22.4.6. I/O Device Configuration Submenu

Feature	Option	Description
Local Bus IDE adapter	**Enabled** Disabled	Enables onboard PCI IDE device.
Floppy Disk controller	Disabled **Enabled** Auto	Enables onboard FDC controller.
Serial Port A Serial Port B	Disabled Enabled **Auto**	Disabled turns off port. Enabled requires user to enter base I/O address and IRQ. Auto makes BIOS configure port.
Serial Port C * Serial Port D *	**Disabled** Enabled Auto	Disabled turns off port. Enabled requires user to enter base I/O address and IRQ. Auto makes BIOS configure port.
Base I/O address	**3F8h, 2F8h**, 3E8h, 2E8h	Select I/O base of port.
Interrupt (Port A and B)	IRQ 3, IRQ 4	Select IRQ of Port A and B
Interrupt (Port C and D) *	IRQ 10, IRQ 11	Select IRQ of Port C and D
Parallel Port	Disabled Enabled **Auto**	Disabled turns off port. Enabled requires user to enter base I/O address and IRQ. Auto makes BIOS configure port.
Mode	**Uni-directional** EPP ECP	Sets the mode for parallel port.
Base I/O address	**378h**, 278h, 3BCh	Select I/O base of port.
Interrupt	IRQ 5, **IRQ 7**	Select IRQ of parallel port.
DMA Channel	DMA1, **DMA3**	Select DMA channel of port if in ECP mode.
OnChip USB Device	**Enabled** Disabled	Enables onchip USB device.
Legacy USB Support **	**Disabled** Enabled	Enable or disable support for USB keyboard and mice as well as USB boot support. Enable for use with non-USB aware OSes such as UNIX and DOS.
‣ Watchdog Settings	Submenu	Opens Watchdog Settings submenu.

Note: In the Option column, bold shows default settings.

(*) Only visible if an external I/O controller (SMSC669) is on the OEM backplane

(**) A 16kb UMB area (most likely DC000h-DFFFFh or if this area is not available in conventional memory 98000h-9CFFFh) is used for USB BIOS Legacy Support.

22.4.7. Watchdog Settings Submenu

Feature	Option	Description
Mode	**Disabled** Reset NMI	Select watchdog timer operation mode.
Timeout	0.4s, 1s, 5s, 10s, **30s**, 1min, 5min, 10min	Select maximum trigger period.
Delay	1s, 5s, 10s, **30s**, 1min, 5min, 10min, 30min	Select time until the watchdog counter starts counting. Useful to handle longer boot times.

Note: In the Option column, bold shows default settings.

22.4.8. Hardware Monitor Submenu

This submenu shows the current voltages and temperatures of the system.

Voltage/Temperature	Description
V(3.3)	3.3V power plane voltage
Vgtl	Gun Transceiver Logic (GTL) bus voltage (1.25 or 1.50V)
Vcore	Core voltage ~ 1.05V for EDEN 300 MHz ~ 1.20V for EDEN 600 MHz ~ 1.05V for EDEN 1.0 GHz
V(2.5)	2.5V power plane voltage
V(5)	5V power plane voltage
T(lm84)	Temperature of onboard LM84 sensor (local temperature)
T(cpu)	Temperature of CPU die (LM84 remote temperature)

22.5 Security Menu

Feature	Option	Description
Supervisor Password is	Clear / Set	Displays whether a password is set or not
User Password is	Clear / Set	Displays whether a password is set or not
Set Supervisor Password *	Up to seven alphanumeric characters	Pressing <Enter> displays the dialog box for entering the user password. In related systems, this password gives full access to setup.
Set User Password *	Up to seven alphanumeric characters	Pressing <Enter> displays the dialog box for entering the user password. In related systems, this password gives restricted access to setup.
Diskette Access	User **Supervisor**	Enabled requires supervisor password to access floppy disk.
Fixed Disk Boot Sector	**Normal** Write protected	Write protect the boot sector on the hard disk for virus protection. Requires a password to format or Fdisk the hard disk.
Virus Check Reminder	**Disabled** Daily Weekly Monthly	Displays a message during boot-up asking (Y/N) if you backed up the system or scanned for viruses. Message returns on each boot until you respond with Y. Daily displays the message on the first boot of the day, Weekly on the first boot after Sunday, and monthly on the first boot of the month.
System Backup Reminder	**Disabled** Daily Weekly Monthly	Displays a message during boot-up asking (Y/N) if you backed up the system or scanned for viruses. Message returns on each boot until you respond with Y. Daily displays the message on the first boot of the day, Weekly on the first boot after Sunday, and monthly on the first boot of the month.
Password on Boot	**Disabled** Enabled	Enabled requires a password on boot. Requires prior setting of the supervisor password. If supervisor password is set and this option is disabled, BIOS assumes user is booting.

Notes: In the Option column, bold shows default settings.
(*) Enabling “Set Supervisor Password” requires a password for entering Setup. Passwords are not case sensitive.
User and Supervisor passwords are related. You cannot have a User password without first creating a Supervisor password

22.6 *Power Menu*

A power-management system reduces the amount of energy used after specified periods of inactivity. The setup menu supports:

- Full On State
- Standby State with Partial Power Reduction
- Suspend State with Full Power Reduction

Use the **IRQs Activity Monitoring** submenu to specify whether an activity can terminate a Standby or Suspend state and restore Full On.

Feature	Option	Description
Power Savings	**Disabled** Customized Maximum Power Saving Maximum Performance	Maximum options select predefined values. Select Customized to make selections from the following fields. Disabled turns off power management.
‣ IRQs Activity Monitoring	Submenu	Opens IRQ Activity Monitoring submenu.
Idle Mode	**Off** On	Idle mode slows down the CPU during brief periods of inactivity.
Standby Timeout	**Off**, 1min, 2min, 4min, 6min, 8min, 12min, 16min	Inactivity period required to put system in Standby mode (partial power shutdown).
Auto Suspend Timeout	**Off**, 5min, 10min, 15min, 20min, 30min, 40min, 60min	Inactivity period required after Standby to enter Suspend mode (maximum power shutdown).
Hard Disk Timeout	**Disabled**, 10 sec – 15 min	Inactivity period of hard disk required before standby (motor off).
Video Timeout	**Disabled**, 10 sec – 15 min	Inactivity period of user input device before the screen is turned off.
Resume on Modem Ring	**Off** On	On wakes the system on incoming calls detected by mode (RI).
Resume on Time	**Off** On	On wakes the system at a specific time.
Resume Time	00:00:00	Specifies when system wakes.

Note: In the Option column, bold shows default settings.

22.6.1. Wake Up Events Submenu

This menu allows the user to enable or disable IRQs as activities and resume event.

Feature	Option	Description
IRQ1	**Enabled** Disabled	Wakes up system on IRQ1 (Keyboard).
IRQ12	**Enabled** Disabled	Wakes up system on IRQ12 (PS/2 Mouse).
IRQ3, 4, 5, 7, 9, 10,. 11, 15	Enabled **Disabled**	Wakes up system on IRQ if set to Enabled.

Note: In the Option column, bold shows default settings.

22.7 *Boot Menu and Utilities*

Feature	Option	Description
Floppy Check	**Disabled** Enabled	Enabled verifies floppy type on boot. Disabled speeds boot.
Summary Screen	**Disabled** Enabled	If enabled, a summary screen is displayed just before booting the OS to let user see system configuration.
QuickBoot Mode	Disabled **Enabled**	Allows system to skip certain tests while booting. This decreases the time needed to boot the system.
Dark Boot	**Disabled** Enabled	If enabled, system comes up with a blank screen instead of the diagnostic screen during boot-up.
Onboard LAN PXE ROM	**Disabled** Enabled	Enables PXE ROM of the onboard LAN controller. Supports Intel PXE. Check the Intel Web site for more information.
‣ Boot Device Priority	Submenu	Opens boot-device priority submenu.
‣ Display Control	Submenu	Opens display control submenu.

Note: In the Option column, bold shows default settings.

22.7.1. Dark Boot

After turning on or resetting the board, Dark Boot displays a graphical logo (default is a blank screen) instead of a text-based POST screen, which displays diagnostic messages.

The graphical logo is visible until just before the OS load unless:

- <**Esc**> is pressed to display the POST screen.
- <**F2**> is pressed to enter Setup.
- POST issues an error message.
- The BIOS or an option ROM requests keyboard input.

22.7.2. Display Control Submenu

Feature	Option	Description
JDA Revision		Shows the actual revision of used JDA (JILI Data Area).
Display Mode	CRT only LCD only **CRT+LCD**	Selects display boot devices. CRT+LCD is the simultaneous mode.
Flat Panel Type	**Auto Detect** VGA, SVGA, XGA,SXGA UXGA * Enter PAID Enter FPID	Select Auto Detect whenever using a JILI cable on the LCD interface. VGA, SVGA, XGA, SXGA, UXGA provide standard timings for LCD panel resolutions. You can enter the Panel Adapter ID (PAID) or the Flat Panel ID (FPID) manually.
LCD Backlight **	0 – 255	Enter a value to adjust backlight of the LCD.
LCD Contrast ***	0 – 63	Enter a value to adjust contrast of the LCD.

Note: In the Option column, bold shows default settings**.**

(*) Standard timings for VGA to UXGA panels cannot drive all available displays of that type that are on the market. Use a JILI cable whenever possible.

(**) Only visible if the panel adapter is equipped with a MAX5362 DAC for backlight control.

(***) Only visible if the panel adapter is equipped with a Xicore X9429 digital potentiometer for contrast control.

22.8 *MultiBoot*

MultiBoot is a boot utility integrated in the PhoenixBIOS 4.0. The MOPS*lcd*7 provide different versions of this feature depending on the BIOS revision:

- MultiBoot 3 (available up to BIOS version PVC3R111)
- MultiBoot XP (available since BIOS version PVC3R112)

22.8.1. MultiBoot 3

MultiBoot 3 expands your boot options by letting you choose your boot device—a hard disk, floppy disk, CD-ROM or network card. You can select your boot device in Setup, or you can choose a different device each time you boot by selecting your boot device in the Boot First Submenu.

Multiboot 3 allows you to boot from the following devices:

- Hard Drives
- USB devices: floppy, LS-120, ZIP, CD-ROM
- Zip
- LS-120
- CD-ROM

MultiBoot 3 consists of the following submenus:

- Boot Device Priority
- Removable Devices
- Hard Drive Priority
- Network Boot Priority
- Boot First

Boot Device Priority Submenu

This submenu allows you to select the order of devices from which the BIOS will attempt to boot the OS. During POST, if BIOS is unsuccessful at booting from one device, it will try the next one.

The selections on this menu each may represent the first of a class of items. For example, if there is more than one hard disk drive, Hard Drive represents the first of such drives as specified in the Hard Drive menu described below.

To change the order, select the device to change and press <-> to decrease or <+> to increase priority.

Feature	Option	Description
▸ Hard Drives	Boot priority & submenu.	Sets boot priority of Hard Disks as described in the respective submenu.
▸ Removable Devices	Boot priority & submenu.	Sets boot priority of Removable Devices as described in the respective submenu.
CD-ROM Drive	Boot priority.	Sets boot priority of ATAPI CD:ROM drives.
▸ Network Boot	Boot priority & submenu.	Sets boot priority of Network Adapters as described in the respective submenu.

Removable Devices Submenu

If there is more than one Removable Media drive, select Removable Devices and press <Enter> to display the Removable Media menu and choose which drive is represented in the boot-order menu.

Note: The standard 1.44MB floppy drive is referenced as Legacy Floppy Drives.

Hard Drive Priority Submenu

If there is more than one bootable hard drive, select Hard Drive and press <Enter> to display the Fixed Disk Menu and choose a boot priority.

Network Boot Priority Submenu

If there is more than one bootable network adapter in the system, select Network Boot and press <Enter> to display available network adapters and choose the boot priority.

22.8.2. MultiBoot XP

MultiBoot XP comes with a complete new look of the Boot Device Priority submenu. This submenu is now separated into two sections:

- Boot Priority Order
- Excluded from Boot Order

It can display the setup menus by each kind of device type and arrange the boot priority order with any sequence of devices. MultiBoot XP meets the requirements of PC 98 and accommodates more devices that are bootable. It employs a boot scheme that is generic and flexible enough to boot from any current device. You can select your boot device in Setup, or you can choose a different device each time you boot by selecting your boot device in the Boot First Submenu.

An available bootable device can be easily switched between the two sections by just highlighting the device and then pressing <X>. To change the order, select the device to change and press <-> to decrease or <+> to increase priority. You can also choose between four default configurations for the boot order <1>-<4>.

Boot Priority Order

This section shows eight configuration entries for up to eight devices that can be arranged in boot priority order (1: highest priority, 8: lowest priority).

Excluded from Boot Order

This section shows all devices that are excluded from the boot order. Any device listed here will never be used as boot device and not appear in the Boot First Submenu.

The following table shows a list of supported devices:

Device	Description
IDE 0	Primary master IDE hard drive
IDE 1	Primary slave IDE hard drive
IDE 2	Secondary master IDE hard drive
IDE 3	Secondary slave IDE hard drive
Legacy Floppy Drives	Standard Legacy Diskette Drives
USB FDC	USB Diskette Drive
USB HDD	USB Hard Drive and memory sticks that follow MMS specification
USB CDROM	USB CD-ROM Drive
USB ZIP	USB ZIP Drive
USB LS120	USB LS120 Drive
PCI LAN	Ethernet Controller on the PCI Bus with LAN Boot ROM
PCI SCSI	SCSI Controller on the PCI Bus with SCSI BIOS ROM
Legacy Network Card	Ethernet Controller on the ISA Bus with LAN Boot ROM

22.8.3. Boot First Submenu

Display the Boot First Menu by pressing <Esc> during POST. In response, the BIOS displays the message Entering Boot Menu and then displays the Boot Menu at the end of POST. With the MultiBoot XP feature only devices detected during boot up are displayed.

Use the menu to select a following option:

- Override the existing boot sequence (for this boot only) by selecting another boot device. If the specified device does not load the OS, the BIOS reverts to the previous boot sequence.
- Enter Setup.
- Press <Esc> to continue with the existing boot sequence.

22.9 *Exit Menu*

Feature	Option	Description
Exit Saving Changes	Saves selections and exits setup. The next time the system boots, the BIOS configures the system according to the Setup selection stored in CMOS.	Exit saving changes.
Exit Discarding Changes	Exits Setup without storing in CMOS any new selections you may have made. The selections previously in effect remain in effect.	Exit discarding changes.
Load Setup Defaults	Displays default values for all the Setup menus.	Load setup defaults.
Discard Changes	If, during a Setup session, you change your mind about changes you have made and have not yet saved the values to CMOS, you can restore the values you saved to CMOS.	Discard changes.
Save Changes	Saves all the selection without exiting Setup. You can return to the other menus to review and change your selection.	Save changes.

Note: In the Option column, bold shows default settings.

22.10 Kontron BIOS Extensions

Besides the Phoenix System BIOS, the MOPSlcd7 comes with a few BIOS extensions that support special features. All extensions are located in the onboard Flash. Some extensions are permanently available; some are loaded if required during boot-up. Supported features include:

- JIDA standard
- Remote Control feature (JRC)
- Onboard LAN RPL ROM

All enabled BIOS extensions require shadow RAM. They will load into the same 16K shadowed memory block, if possible. However, if the system memory cannot find free memory space because all the memory is already used for add-on peripherals, the BIOS extensions do not load.

22.10.1. JIDA BIOS extension

The JUMPtec Intelligent Device Architecture (JIDA) interface is integrated into the BIOS of the MOPSlcd7 modules. This interface enables hardware-independent access to features that cannot be accessed via standard APIs. Functions such as watchdog timer, brightness and contrast of LCD backlight, and user bytes in the EEPROM can be configured with ease by taking advantage of this standard MOPS PC/104 module feature.

The JIDA BIOS extension is not a true extension BIOS. It is part of the system BIOS and is located in the system BIOS segments after boot-up. It is permanently available and supports the JIDA 16-bit standard and the JIDA 32-bit standard.

The JIDA 16-bit standard is a software interrupt 15hex-driven interface for programmers and offers lots of board information functions. For detailed information about programming, refer to the JIDA specification and a source code example (JIDAI???.ZIP), which you can find on the Kontron Web site. The three question marks represent the revision number of the file. You also can contact technical support for this file.

For other operating systems, special drivers (JIDAIA??.ZIP) are available. You can download the zip file from the Kontron Web site.

22.10.2. Remote Control Client Extension

You can remotely control the MOPSlcd7 using software available from Kontron (JRC-1, Part Number 96047-0000-00-0). This software tool can communicate with the board via one of the serial ports. During boot-up, the system BIOS scans the serial ports for an available JRC connection. If detected, it loads the JRC client BIOS extension into the memory. With the JRC client loaded into the first detected free memory location between D0000hex and DFFFFhex, a 16K block is shadowed.

For more information on the Remote Control usage, refer to the JRC-1 technical manual or Application Note JRCUsage_E???.PDF, which you can find on the Kontron Web site.

22.10.3. LAN PXE ROM

This optional ROM allows you to boot the MOPSlcd7 over an Ethernet connection. If the onboard LAN PXE ROM is enabled in the system BIOS setup, an optional ROM for the Ethernet controller loads into memory during boot up. A server with Intel PXE boot support is required on the other side of the Ethernet connection. The setup and configuration of the server, including PXE support, is not the responsibility of Kontron.

The PXE ROM extension is loaded into the first free memory area between D0000hex and DFFFFhex, and a 16K block of memory is shadowed.

22.11 Updating or Restoring BIOS Using PhoenixPhlash

If your MOPSlcd7 board requires a newer BIOS version or the BIOS is damaged, you may need to update or restore the BIOS.

Phoenix PHLASH allows you to update or restore the BIOS with a newer version or restore a corrupt BIOS by using a floppy disk without having to install a new ROM chip.

1) Download Phoenix Phlash as a compressed file, CRD1PVC3.ZIP, from the Kontron Web site. It contains the following files:

File	Purpose
MAKEBOOT.EXE	Creates the custom boot sector on the Crisis Recovery Diskette.
CRISBOOT.BIN	Serves as the Crisis Recovery boot sector code.
MINIDOS.SYS	Allows the system to boot in Crisis Recovery Mode.
PHLASH.EXE	Programs the Flash ROM.
WINCRISIS.EXE	Creates the Crisis Recovery Diskette from Windows.
WINCRISIS.HLP	Serves as the help file of WINCRISES.EXE.
PLATFORM.BIN	Performs platform-dependent functions.
BIOS.ROM	Serves as the actual BIOS image to be programmed into Flash ROM.

2) To install Phoenix Phlash on a hard disk, unzip the content CRD1PVC3.ZIP into a local directory such as C:\PHLASH.

3) To create a Crisis Recovery Diskette, insert a blank diskette into Drive A: or B: and execute WINCRISIS.EXE. This copies four files onto the Crisis Recovery Diskette.

File	Purpose
MINIDOS.SYS	Allows the system to boot in Crisis Recovery Mode.
PHLASH.EXE	Programs the Flash ROM.
PLATFORM.BIN	Performs platform-dependent functions.
BIOS.ROM	Serves as the BIOS image to be programmed into Flash ROM.

4) If the BIOS image (BIOS.ROM) changes because of an update or bug fix, copy the new BIOS.ROM image onto the diskette.

22.11.1. Running Phoenix Phlash

You can run Phoenix Phalsh in one of two modes:

- Command Line
- Crisis Recovery

Phlash can fail if the system uses memory managers. If this occurs, the utility displays this message:

```
Cannot flash when memory managers are present.
```

If you see this message after you execute Phlash, disable the memory manager.

22.12 *Preventing Problems When Updating or Restoring BIOS*

Updating the BIOS represents a potential hazard. Power failures or fluctuations that can occur during updating the Flash ROM can damage the BIOS code, making the system unbootable.

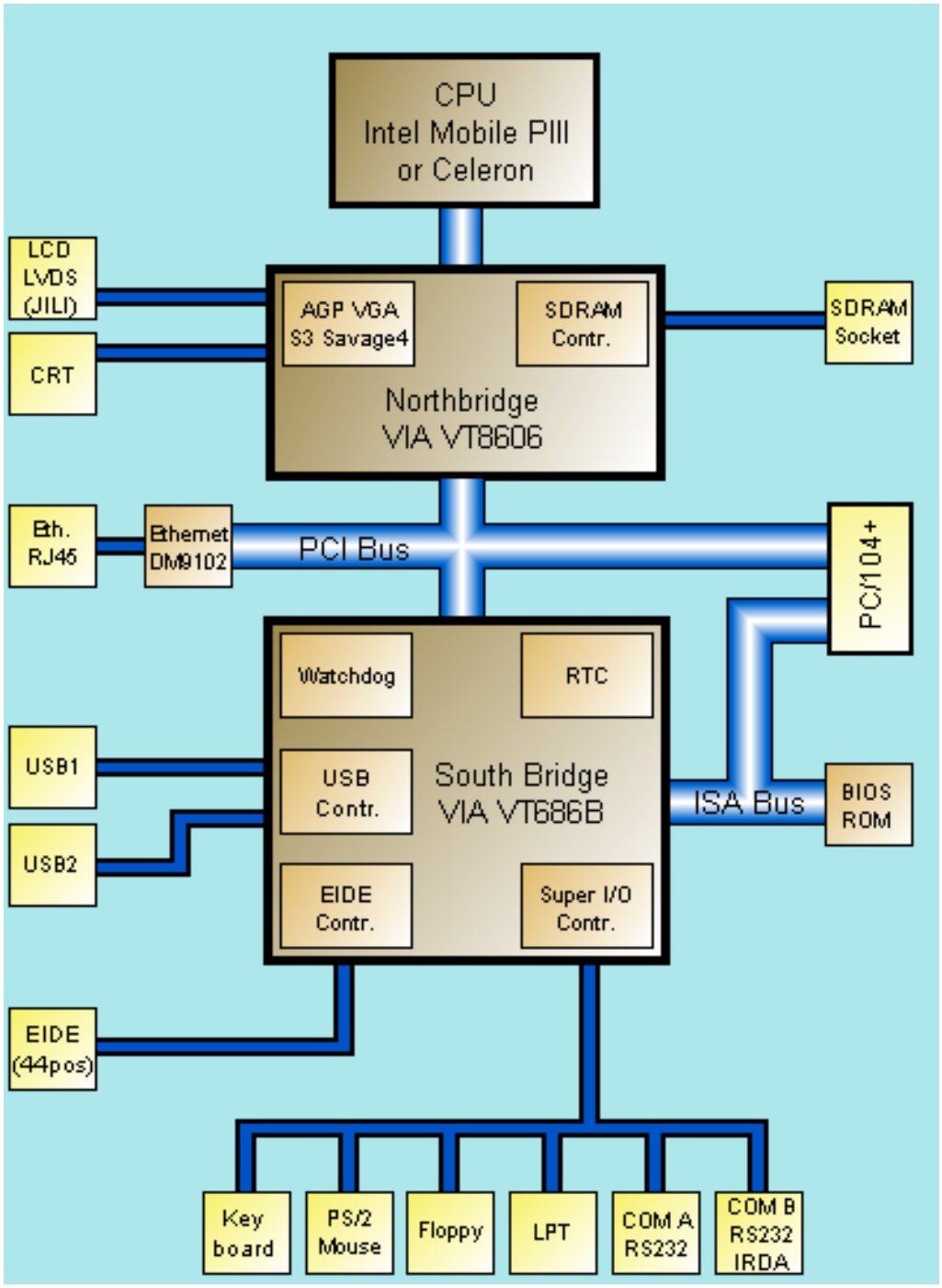
To prevent this potential hazard, many systems come with a boot-block Flash ROM. The boot-block region contains a fail-safe recovery routine. If the boot-block code finds a corrupted BIOS (checksum fails), it boots into the crisis recovery mode and loads a BIOS image from a crisis diskette (see above).

Additionally, the end user can insert an update key into the parallel port to force initiating the recovery routine for the boot block.

For further information on the update key and the crisis diskette, see a special application note (PHLASH_SC_E???.PDF), which is available from the Kontron Web site. (The three question marks indicate the revision number of the document.)

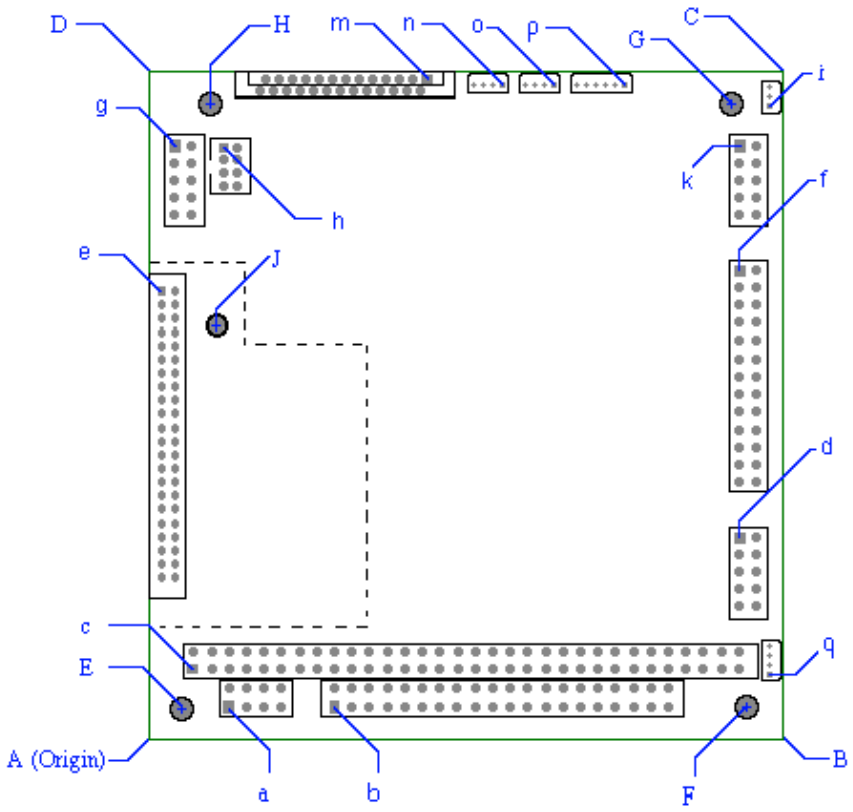
Note: The file BIOS.ROM on the crisis recovery disk may not be the latest version of the ROM file. Contact Kontron technical support for the latest version. Do not flash a BIOS ROM file if you are not sure it matches your hardware because the system might become unbootable. Kontron is not obligated to recover your system free of charge if the board does not boot because flash tools were used incorrectly.

23. APPENDIX C: BLOCK DIAGRAM



24. APPEDNIX D: MECHANICAL DIMENSIONS

24.1 *Top View*

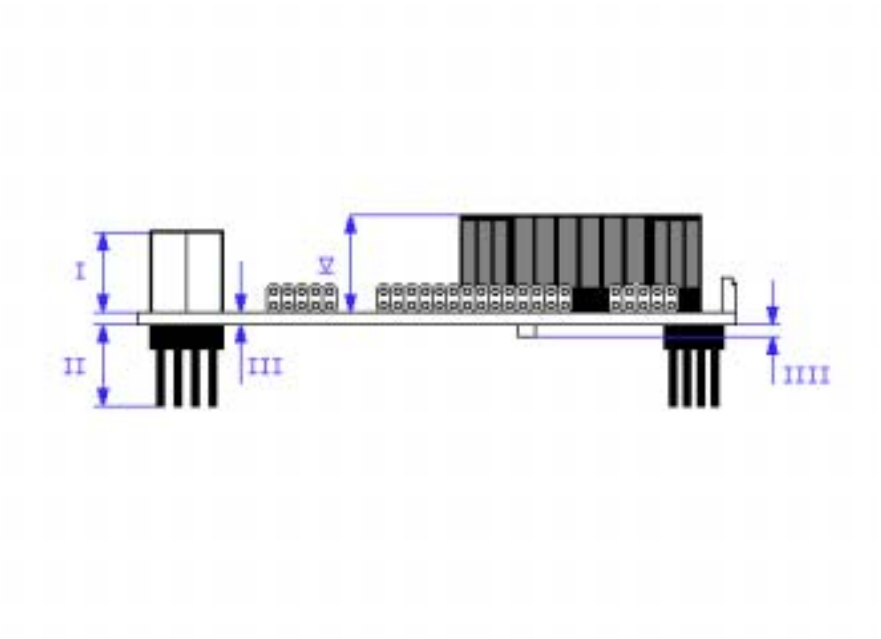


All Dimensions in the tables below are relative to the origin location A.

Location	Horizontal (mm)	Vertical (mm)	Horizontal (mil)	Vertical (mil)
PCB Dimensions				
A (Origin)	0	0	0	0
B	90.17	0	3550	0
C	90.17	95.89	3550	3775
D	0	95.89	0	3775
Mounting Holes				
E	5.08	5.08	200	200
F	85.09	5.08	3350	200
G	82.55	90.81	3250	3575
H	8.89	90.81	350	3575
J	10.13	59.28	399	2333.84

Location	Horizontal (mm)	Vertical (mm)	Horizontal (mil)	Vertical (mil)
Interface Connectors				
a	11.43	5.08	450	200
b	26.67	5.08	1050	200
c	6.35	10.16	250	400
d	83.54	29.24	3289	1151
e	1.75	64.80	69	2551
f	83.54	67.34	3289	2651
g	4.04	85.12	159	3351
h	10.29	86.10	405	3390
i	87.88	90.43	3460	3560
k	83.54	85.12	3289	3351
m	40.54	94.89	1596	3736
n	49.58	93.73	1952	3690
o	56.69	93.73	2232	3690
p	66.27	93.73	2609	3690
q	88.15	10.29	3470	405

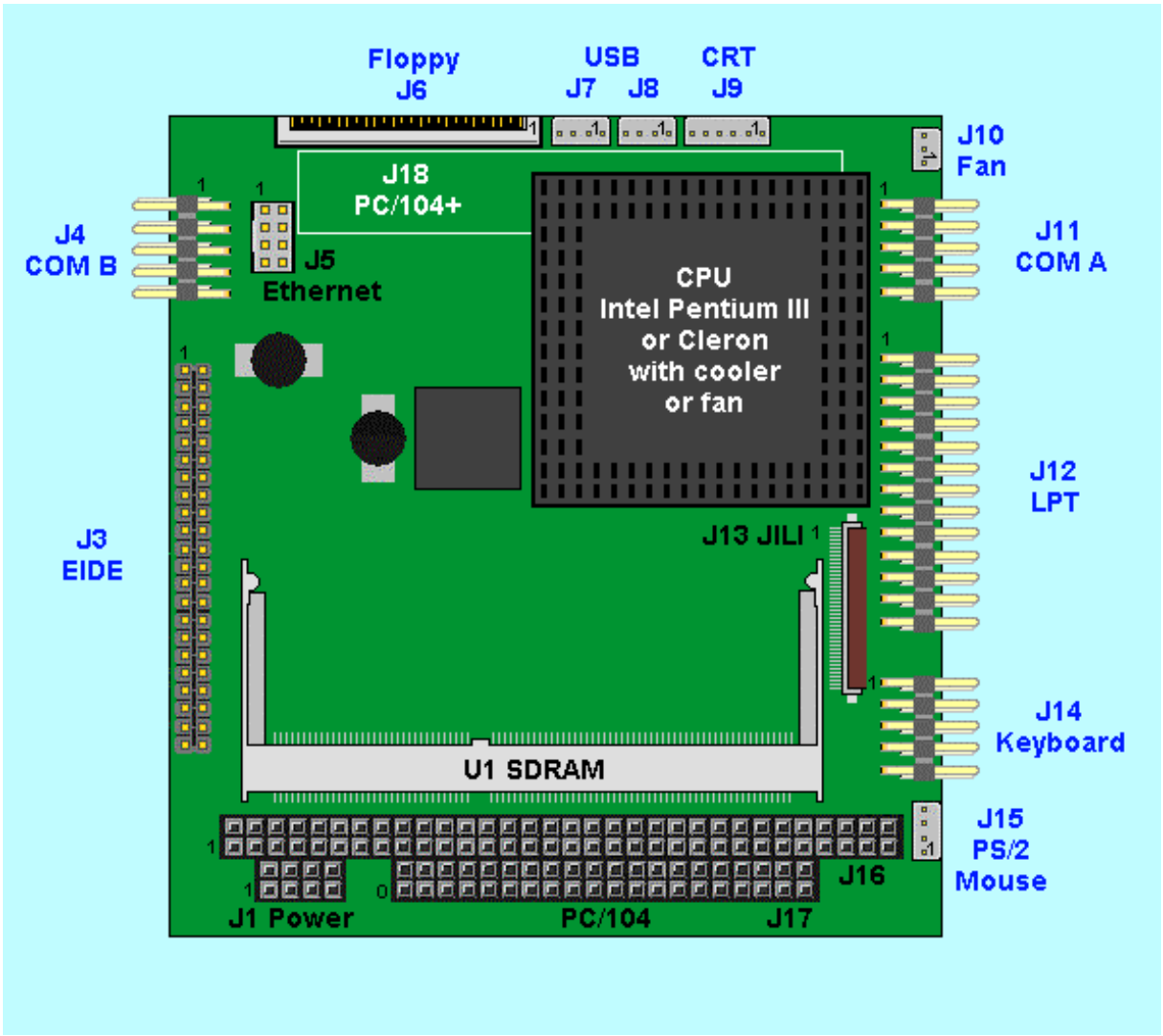
24.2 *Side View*



Height	Dimension (mm)	Dimension (mil)
I	11.05	435
II	10.67	420
III	1.58	62
IIII	3.05	120
V (max)	15.25	600

25. APPENDIX E: CONNECTOR LAYOUT

Pin 1 of any connector is marked with "1" in this drawing and with a rectangular pad at the bottom side of the board's PCB.



25.1 Connector Functions and Interface Cables

The table notes connector functions, as well as mating connectors and available cables.

Connector	Function	Mating Connector	Available Cable	Cable Description
J1	Power Connector	2.54mm 8 pos. (EPT 962-60043-12 or compatible for board to board connection)		
J3	IDE Hard Disk Connector	2mm 44 pos. (Berg 89361-144 or compatible)	KAB-IDE-25 (PN 96020-0000-00-0) or KAB-IDE-2MM (PN 96021-0000-00-0)	For 3.5" HDD Or 2.5" HDD.
J4, J11	Serial Interfaces COM A and COM B Connectors	2.54mm 10 pos. (AMP 1-215882-0 or compatible)	KAB-DSUB9-2 (PN 96017-0000-00-0)	For DSUB 9 adaptation.
J5	Ethernet Interface Connector	2mm 8 pos. (Berg 90311-008 or compatible)	KAB-MOPS-ETN1 (PN 96048-0000-00-0)	For RJ45 adaptation.
J6	Floppy Drive Connector		ADA-FLOPPY-2 (PN 96001-0000-00-0) or KAB-FLOPPY/MOPS-1 (PN 96019-0000-00-0)	For 3.5" floppy or slim-line floppy.
J7, J8	USB interface Connectors	1.25mm 4 pos. (Molex 51021-0400 or compatible)	KAB-USB-1 (PN 96054-0000-00-0)	For standard USB adaptation.
J9	CRT Monitor Connector	1.25mm 6 pos. (Molex 51021-0600 or compatible)	KAB-VGA-2 (PN 96053-0000-00-0)	For DSUB 15 adaptation.
J10	Fan Connector	1.25mm 3 pos. (Molex 51021-0300 or compatible)		
J12	LPT Connector	2.54mm 26 pos. (AMP 2-215882-6 or compatible)	KAB-DSUB25-1 (PN 96015-0000-00-0)	For DSUB 25 adaptation.
J13	Flat-panel display Connector	-	KAB-JILI-?????	Kontron JILI cables.
J14	Keyboard and Feature Connector	2.54mm 10 pos. (AMP 1-215882-0 or compatible)	KAB-KB-1 (PN 96023-0000-00-0) or KAB-KB-PS2 (PN 96060-0000-00-0)	For AT-keyboard or PS/2 keyboard.
J15	PS/2 Mouse Connector	1.25mm 4 pos. (Molex 51021-0400 or compatible)	KAB-MOUSE-PS2 (PN 96062-0000-00-0)	For PS/2 mouse.
J16	PC/104 Bus (XT-bus part)	2.54mm 64 pos. (EPT 962-60323-12 or compatible for board to board connection)		
J17	PC/104 Bus (AT-bus part)	2.54mm 40 pos. (EPT 962-60203-12 or compatible for board to board connection)		
J18	PC/104-Plus Bus (PCI part)	2mm 120pos. (EPT 264-60303-12)		
U1	SDRAM	-	-	-

25.2 Pinout Table

Pin	PC104-XT Bus (A) J16	PC104-XT Bus (B) J16	PC104-AT Bus (C) J17	PC104-AT Bus (D) J17
0			GND	GND
1	/IOCHCK	GND	/SBHE	/MEMCS16
2	SD7	RESETDRV	LA23	/IOCS16
3	SD6	VCC (***)	LA22	IRQ10
4	SD5	IRQ9	LA21	IRQ11
5	SD4	-5V	LA20	IRQ12
6	SD3	DRQ2	LA19	IRQ15
7	SD2	-12V	LA18	IRQ14
8	SD1	/0WS	LA17	/DACK0
9	SD0	+12V	/MEMR	DRQ0
10	IOCHRDY	GND (*)	/MEMW	/DACK5
11	AEN	/SMEMW	SD8	DRQ5
12	SA19	/SMEMR	SD9	/DACK6
13	SA18	/IOW	SD10	DRQ6
14	SA17	/IOR	SD11	/DACK7
15	SA16	/DACK3	SD12	DRQ7
16	SA15	DRQ3	SD13	VCC (***)
17	SA14	/DACK1	SD14	/MASTER
18	SA13	DRQ1	SD15	GND
19	SA12	/REFRESH	GND	GND
20	SA11	SYSCLK		
21	SA10	IRQ7		
22	SA9	IRQ6		
23	SA8	IRQ5		
24	SA7	IRQ4		
25	SA6	IRQ3		
26	SA5	/DACK2		
27	SA4	T/C		
28	SA3	BALE		
29	SA2	VCC (***)		
30	SA1	OSC		
31	SA0	GND		
32	GND	GND		

Notes: (*) Key pin for PC/104; GND for PC/104+ specification
(***) To protect the external power lines of peripheral devices, make sure that:
- the wires have the right diameter to withstand the maximum available current
- the enclosure of the peripheral device fulfils the fire protecting requirements of
- IEC/EN 60950.

Pin	PC104+ Bus (A) J18	PC104+ Bus (B) J18	PC104+ Bus (C) J18	PC104+ Bus (D) J18
1	GND	Reserved	VCC (***)	AD00
2	VCC (***)	AD02	AD01	AD03
3	AD05	GND	AD04	AD03
4	C/BE0	AD07	GND	AD06
5	GND	AD09	AD08	GND
6	AD11	VCC (***)	AD10	GND
7	AD14	AD13	GND	AD12
8	VCC3 (**)	C/BE1	AD15	VCC3 (**)
9	SERR	GND	SB0	PAR
10	GND	PERR	VCC3 (**)	SDONE
11	STOP	VCC3 (**)	LOCK	GND
12	VCC3 (**)	TRDY	GND	DEVSEL
13	FRAME	GND	IRDY	VCC3 (**)
14	GND	AD16	VCC3 (**)	C/BE2
15	AD18	VCC3 (**)	AD17	GND
16	AD21	AD20	GND	AD19
17	VCC3 (**)	AD23	AD22	VCC3 (**)
18	IS0 (AD20)	GND	IS1 (AD21)	IS2 (AD22)
19	AD24	C/BE3	VI/O	IS3 (AD23)
20	GND	AD26	AD25	GND
21	AD29	VCC (***)	AD28	AD27
22	VCC (***)	AD30	GND	AD31
23	REQ0	GND	REQ1	VI/O
24	GND	REQ2	VCC (***)	GNT0
25	GNT1	VI/O	GNT2	GND
26	VCC (***)	CLK0	GND	CLK1
27	CLK2	VCC (***)	CLK3	GND
28	GND	INTD	VCC (***)	RST
29	+12V	INTA	INTB	INTC
30	-12V	Reserved	Reserved	Reserved

Notes: (**) The DC/DC converter for +3.3V PC/104+ bus is capable of supplying maximum 1.5A to adapter cards.

(***) To protect the external power lines of peripheral devices, make sure that:
- the wires have the right diameter to withstand the maximum available current
- the enclosure of the peripheral device fulfils the fire protecting requirements of
- IEC/EN 60950.

Pin	IDE J3	Floppy J6	LPT J12	Power J1	COM A J11	COM B J4
1	/RESET	VCC (***)	/STB	+12V (***)	/DCD1	/DCD2
2	GND	/IDX	/AFD	GND	/DSR1	/DSR2
3	HDD7	VCC (***)	PD0	VCC (***)	RXD1	RXD2
4	HDD8	/DR0	/ERR	VCC (***)	/RTS1	/RTS2
5	HDD6	VCC (***)	PD1	GND	TXD1	TXD2
6	HDD9	/DSKCHG	/INIT	GND	/CTS1	/CTS2
7	HDD5	VCC (***)	PD2	VCC (***)	/DTR1	/DTR2
8	HDD10	NC	/SLIN	VCC (***)	/RI1	/RI2
9	HDD4	NC	PD3	GND	GND	GND
10	HDD11	/MTR0	GND	+12V (***)	VCC (***)	VCC (***)
11	HDD3	NC	PD4			
12	HDD12	/FDIR	GND			
13	HDD2	NC	PD5			
14	HDD13	/STEP	GND			
15	HDD1	GND	PD6			
16	HDD14	/WDATA	GND			
17	HDD0	GND	PD7			
18	HDD15	/WGATE	GND			
19	GND	GND	/ACK			
20	KEY (NC)	/TRK0	GND			
21	DRQ	GND	BUSY			
22	GND	/WRTPRT	GND			
23	/IOW	GND	PE			
24	GND	/RDATA	GND			
25	/IOR	GND	SLCT			
26	GND	/HDSEL	VCC (***)			
27	IOCHRDY					
28	CSEL					
29	/AKJ					
30	GND					
31	SIRQ					
32	NC					
33	SA1					
34	NC					
35	SA0					
36	SA2					
37	/CS1					
38	/CS3					
39	NC					
40	GND					
41	VCC (***)					
42	VCC (***)					
43	GND					
44	NC					

Notes: (***) To protect the external power lines of peripheral devices, make sure that:
- the wires have the right diameter to withstand the maximum available current
- the enclosure of the peripheral device fulfils the fire protecting requirements of
- IEC/EN 60950.

Pin	KBD J14	LAN J5	CRT J9	PS/2 Mouse J15	USB 1 J7	USB 2 J8	Fan J10
1	SPEAKER	TXD+	RED	MSDAT	VCC (***)	VCC (***)	VCC (***)
2	GND	TXD-	GRN	VCC (***)	USB00	USB10	GND
3	/RESIN	RXD+	BLU	GND	USB01	USB11	+12V(***)
4	NC	SHLDGND	GND	MSCLK	GND	GND	
5	KBDAT	SHLDGND	VSYNC				
6	KBCLK	RXD-	HSYNC				
7	GND	SHLDGND					
8	VCC (***)	SHLDGND					
9	BATT						
10	PWRGOOD						

Notes: (***) To protect the external power lines of peripheral devices, make sure that:
- the wires have the right diameter to withstand the maximum available current
- the enclosure of the peripheral device fulfils the fire protecting requirements of
- IEC/EN 60950.

26. APPENDIX F: PC ARCHITECTURE INFORMATION

The following sources of information can help you better understand PC architecture.

26.1 *General PC Architecture*

- *Embedded PCs*, Markt&Technik GmbH, ISBN 3-8272-5314-4 (German)
- *Hardware Bible*, Winn L. Rosch, SAMS, 1997, 0-672-30954-8
- *Interfacing to the IBM Personal Computer*, Second Edition, Lewis C. Eggebrecht, SAMS, 1990, ISBN 0-672-22722-3
- *The Indispensable PC Hardware Book*, Hans-Peter Messmer, Addison-Wesley, 1994, ISBN 0-201-62424-9
- *The PC Handbook: For Engineers, Programmers, and Other Serious PC Users*, John P. Choisser and John O. Foster, Annabooks, 1997, ISBN 0-929392-36-1

26.2 *Buses*

26.2.1. ISA, Standard PS/2 - Connectors

- *AT Bus Design: Eight and Sixteen-Bit ISA, E-ISA and EISA Design*, Edward Solari, Annabooks, 1990, ISBN 0-929392-08-6
- *AT IBM Technical Reference Vol 1&2*, 1985
- *ISA & EISA Theory and Operation*, Edward Solari, Annabooks, 1992, ISBN 0929392159
- *ISA Bus Specifications and Application Notes*, Jan. 30, 1990, Intel
- *ISA System Architecture, Third Edition,* Tom Shanley and Don Anderson, Addison-Wesley Publishing Company, 1995, ISBN 0-201-40996-8
- *Personal Computer Bus Standard P996*, Draft D2.00, Jan. 18, 1990, IEEE Inc
- *Technical Reference Guide, Extended Industry Standard Architecture Expansion Bus*, Compaq 1989

26.2.2. PCI and PC/104

- Embedded PC 104 Consortium

The consortium provides information about PC/104 and PC/104-Plus technology. You can search for information about the consortium on the Web.

- PCI SIG

The PCI-SIG provides a forum for its ~900 member companies, who develop PCI products based on the specifications that are created by the PCI-SIG. You can search for information about the SIG on the Web.

- *PCI & PCI-X Hardware and Software Architecture & Design*, Fifth Edition, Edward Solari and George Willse, Annabooks, 2001, ISBN 0-929392-63-9.

- *PCI System Architecture,* Tom Shanley and Don Anderson, Addison-Wesley, 2000, ISBN 0-201-30974-2.

26.3 *Ports*

26.3.1. RS-232 Serial

- EIA-232-E standard

The EIA-232-E standard specifies the interface between (for example) a modem and a computer so that they can exchange data. The computer can then send data to the modem, which then sends the data over a telephone line. The data that the modem receives from the telephone line can then be sent to the computer. You can search for information about the standard on the Web.

- *RS-232 Made Easy: Connecting Computers, Printers, Terminals, and Modems*, Martin D. Seyer, Prentice Hall, 1991, ISBN 0-13-749854-3

- National Semiconductor

The Interface Data Book includes application notes. Type “232” as a search criteria to obtain a list of application notes. You can search for information about the data book on National Semiconductor’s Web site.

26.3.2. ATA

AT Attachment (ATA) Working Group
This X3T10 standard defines an integrated bus interface between disk drives and host processors. It provides a common point of attachment for systems manufacturers and the system. You can search for information about the working group on the Web.
We recommend you also search the Web for information on *4.2 I/O cable*, if you use hard disks in a DMA3 or PIO4 mode.

26.3.3. USB

- USB Specification

USB Implementers Forum, Inc. is a non-profit corporation founded by the group of companies that developed the Universal Serial Bus specification. The USB-IF was formed to provide a support organization and forum for the advancement and adoption of Universal Serial Bus technology. You can search for information about the standard on the Web.

26.4 *Programming*

- *C Programmer's Guide to Serial Communications*, Second Edition, Joe Campbell, SAMS, 1987, ISBN 0-672-22584-0
- *Programmer's Guide to the EGA, VGA, and Super VGA Cards*, Third Edition, Richard Ferraro, Addison-Wesley, 1990, ISBN 0-201-57025-4
- *The Programmer's PC Sourcebook,* Second Edition, Thom Hogan, Microsoft Press, 1991, ISBN 1-55615-321-X
- *Undocumented PC, A Programmer's Guide to I/O, CPUs, and Fixed Memory Areas*, Frank van Gilluwe, Second Edition, Addison-Wesley, 1997, ISBN 0-201-47950-8

27. APPENDIX G: DOCUMENT REVISION HISTORY

Revision	Date	Edited by	Changes
PVC3M001	05.04.2002	IK	Created manual.
PVC3M002	24.04.2002	JL	Formatted and edited manual.
PVC3M003	20.06.2002	IK	First review.
PVC3M004	24.06.2002	JL	Incorporates changes from 1st review.
PVC3M005	23.07.2002	JL	Incorporates new Kontron name throughout manual.
PVC3M006	11.09.2002	IK and JL	Incorporate updated technical information.
PVC3M007	25.09.2002	CR	Updates BIOS chapter.
PVC3M008	27.09.2002	CR	Additional updates to BIOS chapter.
PVC3M009	09.10.2002	CR	Additional changes to BIOS chapter.
PVC3M110	31.10.2002	JL	Manual reviewed.
PVC3M111	25.02.2003	VGG	Added additional information.
PVC3M112	15.04.2003	KFR	Changed Environmental Specifications.
PVC3M113	07.05.2003	KFR	Released manual for publication.
PVC3M114	12.05.2003	KFR	Updated PS/2-mouse interface chapter.
PVC3M115	19.05.2003	KFR	Updated mechanical dimensions information.
PVC3M116	18.11.2004	BHO	Brought to Kontron style, added lots of drawings, corrected and completed specifications, completed resource lists, added BIOS information.
PVC3M117	08.03.2005	BHO	Corrected Power connector J1 information on page 82, minor changes.