Modular Computers ®

PB-DOUT8

Eight-Channel Digital I/O

ModPack Piggyback

Manual ID 17984, Index 0110
Oct 98

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Preface

Revision History *0-6*
For Your Safety *0-5*
Special Handling and Unpacking Instructions *0-5*
HV Safety Instructions *0-6*
Two Years Warranty *0-7*
Table of Contents *0-8*

Revision History

REVISION HISTORY				
Manual/Product Title:	**PB-DOUT8**			
Manual ID Number:	**17984**			
Rev. Index	**Brief Description of Changes**	**PCB Index**		**Date of Issue**
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Table of Contents

Chapter 1

1. Introduction ..... 1 - 3
1.1 EMC Compliance ..... 1 - 3
1.2 Board Overview ..... 1 - 3
1.3 Main Features ..... 1 - 4
1.4 Board Layout ..... 1 - 5
1.5 Technical Specification ..... 1 - 6

Chapter 2

2. Configuration ..... 2 - 3
2.1 Pinout ..... 2 - 3
2.2 Jumper Configuration ..... 2 - 5

Chapter 3

3. Installation ..... 3 - 3
3.1 Carrier Board Interfacing ..... 3 - 3
3.2 Carrier Board Installation ..... 3 - 6

Chapter 4

4. Software References ..... 4 - 3
4.1 Technical Features ..... 4 - 3
4.2 Memory Map ..... 4 - 3
4.3 PB-DOUT8 Registers ..... 4 - 4
4.4 Error Analysis ..... 4 - 6

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Chapter 1

Introduction

1.1 EMC Compliance ..... 1 - 3
1.2 Board Overview ..... 1 - 3
1.3 Main Features ..... 1 - 4
1.3.1 High-Side Power Switches ..... 1 - 4
1.3.2 Low-Side Power Switches ..... 1 - 5
1.3.3 Board Interfaces ..... 1 - 5
1.4 Board Layout ..... 1 - 5
1.5 Technical Specification ..... 1 - 6

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1. Introduction

The PB-DOUT8 is a single-size ModPack piggyback (100 mm x 48 mm) designed to fit any of the following carrier boards of the *PEP Modular Computers* ModPack range:

- VMOD
- VMOD-2/VMOD-2D,VMOD-4D
- VM642/662
- CXM-IMOD

It will also, where possible and appropriate, be compatible with future Modpack boards

The PB-DOUT8 is an 8-channel digital output module utilising “intelligent” power transistors which prevent damage to the circuitry resulting from exposure to the following factors:

- overload;
- undervoltage and overvoltage;
- short circuit;
- overtemperature;
- electrostatic discharges.

In addition, the PB-DOUT8 module is provided with open-load detection.

1.1 EMC Compliance

The PB-DOUT8 piggyback module complies with the requirements of the following CE-relevant standards:

- Emission: EN50081-1;
- Immission: EN50082-2;
- Electrical Safety: EN60950.

1.2 Board Overview

PB-DOUT8 is a piggyback output module consisting of eight channels with high-side and eight channels with low-side switches. Each channel has its own status bit. The switches are divided into four separate groups, each group having individual power supply (up to 40 V) and grounding. The channel groups are galvanically isolated from one another and towards the VMEbus.

The output channels switch direct current, namely 1.3 A on the low side and 1.8 A on the high side, although the minimum output current may vary with different temperatures (see table 2-1 for exact figures). The maximum (peak) output current is instead typically 4.0 A on the low side and 5.0 A on the high side. The output voltage is typically 24 V DC.

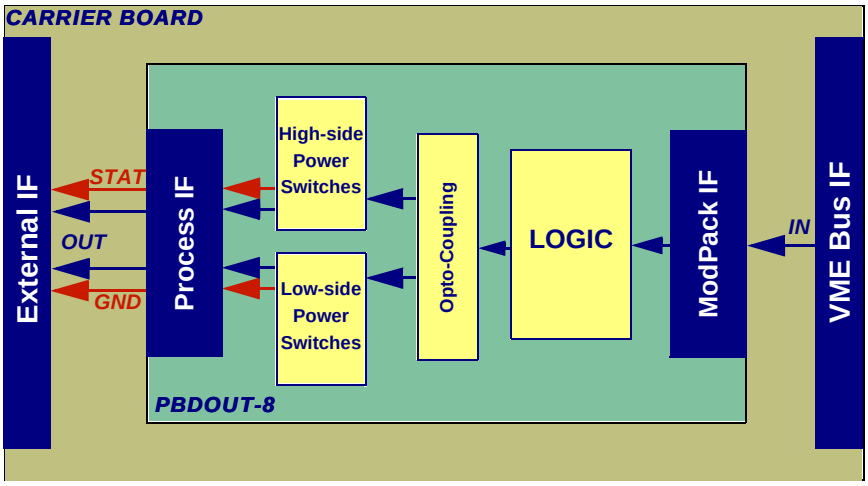
The board interrupts, which are hard-coded, are generated and handled according to various smart transistor conditions.

Attention!

Please check the specification of your carrier board to make sure that it supports the output current of the PB-DOUT8.

PB-DOUT8 does not have a reverse voltage protection for the external 24 V power supply lines.

Figure 1-1: PB-DOUT8 Functional Block Diagram



Legend:

STAT = status
GND = ground

1.3 Main Features

In the following the main features of the principal functional blocks of the PB-DOUT8 digital output module are described.

1.3.1 High-Side Power Switches

The PB-DOUT8 module is provided with eight Siemens BTS412B2 smart power transistors for high-side switching having the following features:

- overload protection
- current limitation
- short-circuit protection
- thermal shutdown
- undervoltage and overvoltage shutdown
- open-load detection
- loss-of-ground protection
- ESD protection

1.3.2 Low-Side Power Switches

The PB-DOUT8 module is provided with four two-channel Siemens TLE 5224 G2 smart power transistors for low-side switching having the following features:

- overload protection
- power limitation
- short-circuit protection
- overtemperature monitoring
- overvoltage protection
- ESD protection

1.3.3 Board Interfaces

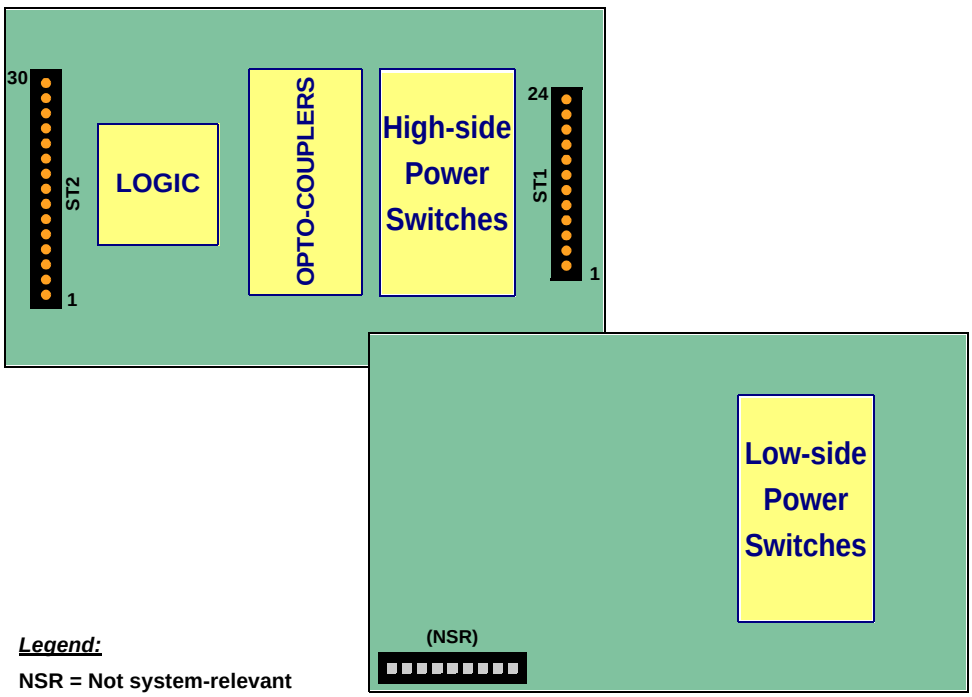
The PB-DOUT8 piggyback module is provided with two digital I/O connectors. The one on the input side is a 15-pin double-row connector, the one on the process side a 12-pin double-row connector. The input connector is wired via the carrier board to a 50-pin DSUB or to a 50-pin FB connector, while the process interface is wired to the carrier board's VMEbus socket.

Attention!

In fitting your PB-DOUT8 piggyback module onto its carrier board, please make sure the PB-DOUT8 pin rows match the corresponding rows of pinholes of the carrier board socket (see chapter 3).

1.4 Board Layout

Figure 1-2: PB-DOUT8 Board Layout — Component Side (Left) and Solder Side (Right)



1.5 Technical Specification

Table 1-1: PB-DOUT8 Technical Specification

PB-DOUT8	Specification
Channels and Channel Grouping	4 groups of channels, each consisting of - 2 channels with high-side switches - 2 channels with low-side switches
Isolation Voltages	Group-to-group: 0.7 mm (0.7 kV) Group-to-VMEbus:4.0 mm (4.0 kV)
Input Voltage	Range: 10...40 V DC Nominal: 24 V DC
Power Consumption	24V side:typ. 2mA per group VMEbus side:typ. 95 mA
Temperature Range: - Standard Operation - Extended Operation - Storage	 0° to + 70°C - 40° to + 85°C - 55° to + 125°C
Driving Current	Typically: 1.3 A DC (low side), 1.8 A DC (high side) Minimum (LS/HS): 1.0 A DC (0...+70°C), 0.6 A DC (-40...0°C) Maximum (typ.) 4.0 A (low side), 5.0 A (high side)
Open Circuit Detection	Typ. 30 µA
Operating Frequency	0...250 Hz, incl. inductive load
Inductive Load	24 V/0.5 A/1,0 Henry
On-State Resistance	Typically: 250 mOhm (low side), 220 mOhm (high side)
Switching Speed	Typ. 1 ms, incl. status feedback

Chapter 2

Configuration

2.1 Pinout ..... 2 - 3
2.2 Jumper Configuration ..... 2 - 5

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2. Configuration

2.1 Pinout

The PBDOUT-8 is connected via its carrier board to a 50-way flat-band cable or DSUB connector. Depending on the carrier board location where the piggyback is installed (“A” of “B”), either the upper half or the lower half of the connector pins are used

The following tables show the output registers and the corresponding output lines for the upper (“A”) and lower (“B”) location, with reference to the relative DSUB/FB connectors of the carrier board:

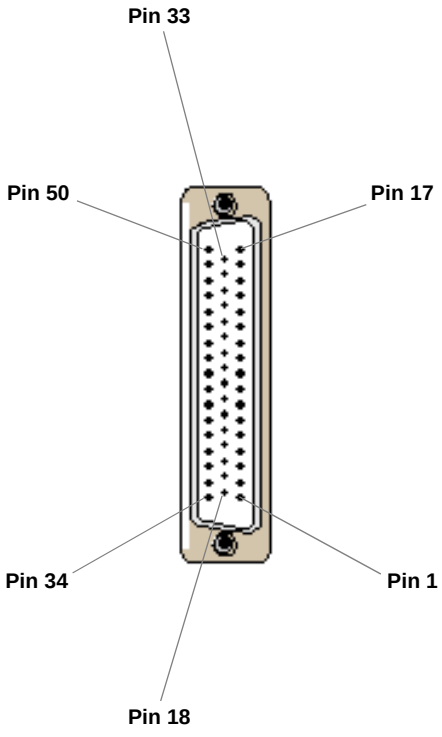
Table 2-1: PB-DOUT8 Pinout (Lower Position)

Pin	DSUB 50	FB 50	Pin	DSUB 50	FB 50
OUT07L	Pin 1	Pin 1	OUT03L	Pin 5	Pin 13
OUT07H	Pin 34	Pin 2	OUT03H	Pin 38	Pin 14
OUT06L	Pin 18	Pin 2	OUT02L	Pin 22	Pin 15
OUT06H	Pin 2	Pin 4	OUT02H	Pin 6	Pin 16
GND0607	Pin 35	Pin 5	GND0203	Pin 39	Pin 17
VSS0607	Pin 19	Pin 6	VSS0203	Pin 23	Pin 18
OUT05L	Pin 3	Pin 7	OUT01L	Pin 7	Pin 19
OUT05H	Pin 36	Pin 8	OUT01H	Pin 40	Pin 20
OUT04L	Pin 20	Pin 9	OUT00L	Pin 24	Pin 21
OUT04H	Pin 4	Pin 10	OUT00H	Pin 8	Pin 22
GND0405	Pin 37	Pin 11	GND0001	Pin 41	Pin 23
VSS0405	Pin 21	Pin 12	VSS0001	Pin 25	Pin 24

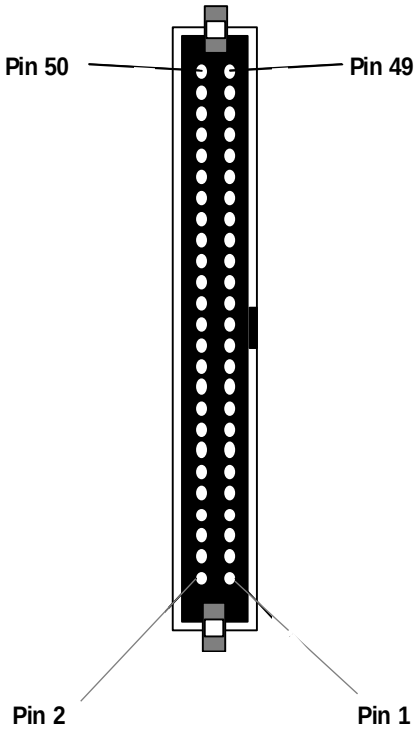
Table 2-2: PB-DOUT8 Pinout (Upper Position)

Pin	DSUB 50	FB 50	Pin	DSUB 50	FB 50
OUT07L	Pin 26	Pin 27	OUT03L	Pin 30	Pin 39
OUT07H	Pin 10	Pin 28	OUT03H	Pin 14	Pin 40
OUT06L	Pin 43	Pin 29	OUT02L	Pin 47	Pin 41
OUT06H	Pin 27	Pin 30	OUT02H	Pin 31	Pin 42
GND0607	Pin 11	Pin 31	GND0203	Pin 15	Pin 43
VSS0607	Pin 44	Pin 32	VSS0203	Pin 48	Pin 44
OUT05L	Pin 28	Pin 33	OUT01L	Pin 32	Pin 45
OUT05H	Pin 12	Pin 34	OUT01H	Pin 16	Pin 46
OUT04L	Pin 45	Pin 35	OUT00L	Pin 49	Pin 47
OUT04H	Pin 29	Pin 36	OUT00H	Pin 33	Pin 48
GND0405	Pin 13	Pin 37	GND0001	Pin 17	Pin 49
VSS0405	Pin 46	Pin 38	VSS0001	Pin 50	Pin 50

Figure 2-1: Pin Numbering of DSUB 50 and Front Panel Connector (FB 50)



DSUB 50



FB 50

2.2 Jumper Configuration

The PB-DOUT8 module does not have any jumpers to be configured.

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Chapter 3

Installation

3.1 Carrier Board Interfacing ..... 3 - 3
3.1.1 Carrier Board VMEbus Connector BU1A/B..... 3 - 4
3.1.2 Carrier Board External Interface Connector BU2A/B .... 3 - 4
3.2 Carrier Board Installation..... 3 - 6

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3. Installation

3.1 Carrier Board Interfacing

This section shows how to proceed with the installation of the PB-DOUT8 piggyback module on a carrier board. Figure 2-2 shows an example configuration where two piggybacks standing in this case for two PB-DOUT8 modules are fit to a VMOD-2. The first PB-DOUT8 on a carrier board would fit in the upper position (“A”), the second in the lower position (“B”).

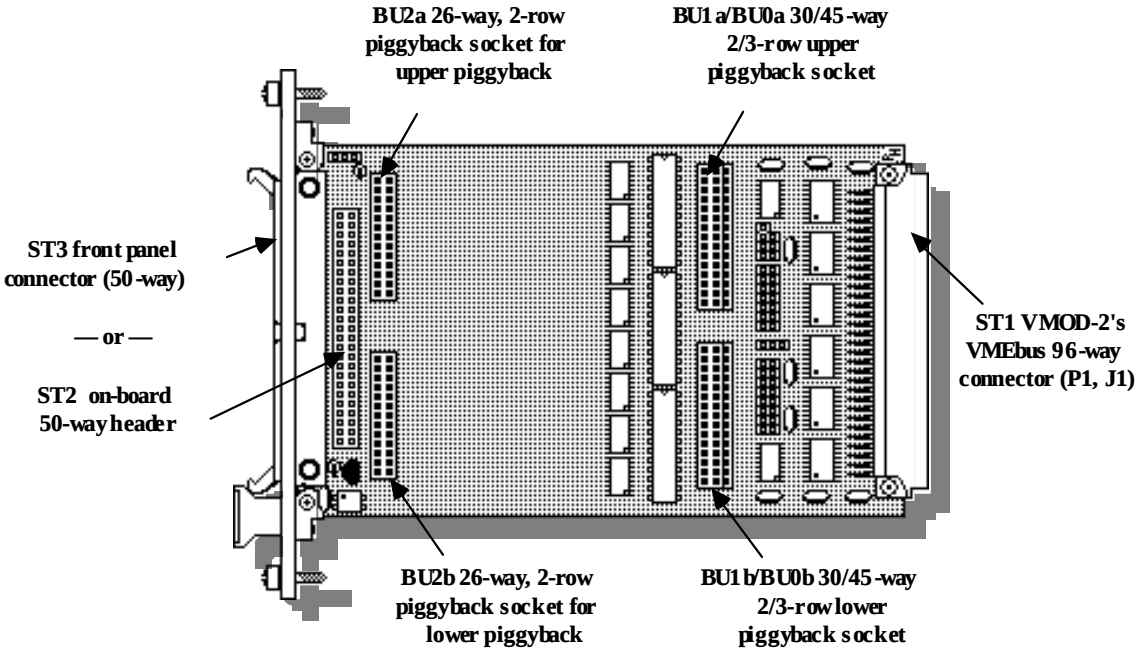
At first the two header-type connectors (BU1a/BU1b and BU0a/BU0b) of the carrier board are illustrated, which directly interface to the PB-DOUT8 ST1 pin rows. The lower case letters in the socket numbers refer to which piggyback location the connector is used for, e.g. BU1a is socket 1 for PB-DOUT8 location “A”. An illustration showing in detail all carrier board connectors concerning piggyback installation is given below.

Important!

Please take care to note that the denominations “ST1” and “ST2” used for the PB-DOUT8 refer only to the piggyback pin row connectors themselves and fit to headers BU1a and BU2a or, respectively, BU1b and BU2b on the carrier board.

Also the carrier boards have plugs called “ST1” (VMEbusVMEbus connector) and “ST2” (50-way header), which have no direct relationship to those of the PB-DOUT8 connectors described in this manual.

Figure 3-1: Carrier Board Connector Denominations



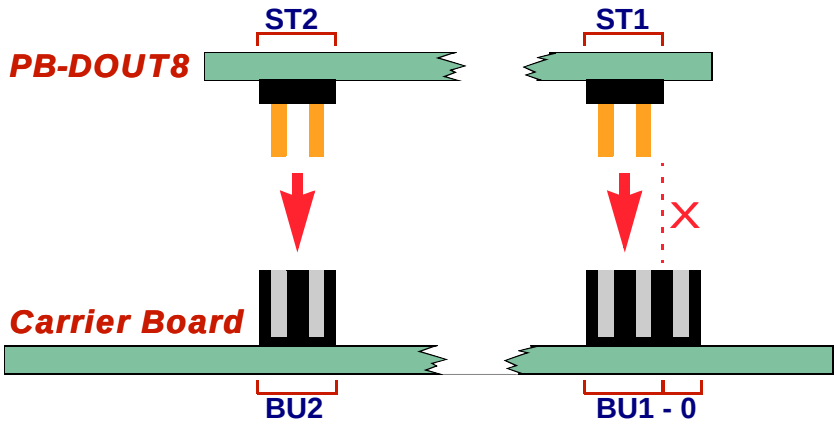
3.1.1 Carrier Board VME Bus Connector BU1A/B

The Modpack carrier boards are provided with a three-row 45-pin socket. Some piggyback modules, like for instance PB-DOUT8, use only the first two rows (30 pins) of the header, while other piggybacks, having three-row headers, use also the third row. For this reason, the first two rows of the connector are named as if they were a separate socket — “BU1”; the remaining third row instead is called “BU0”.

Attention!

When installing your PB-DOUT8 on its carrier board, please make sure the piggyback’s pin rows match with the carrier board’s headers as is shown in the following figure.

Figure 3-2: Correct Installation of PB-DOUT8 on the Carrier Board

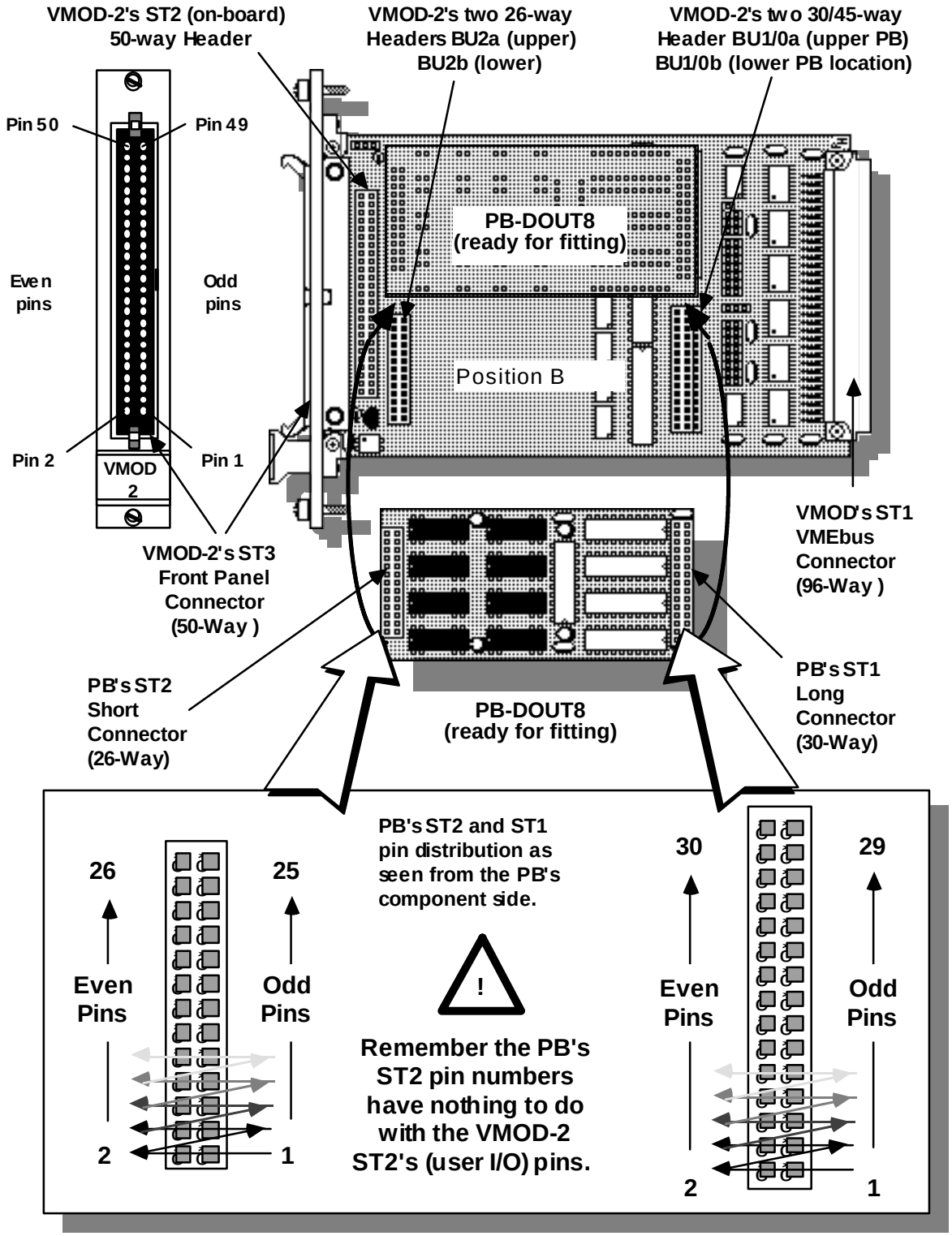


3.1.2 Carrier Board External Interface Connector BU2A/B

The 26-pin double-row sockets are totally isolated from the remaining circuits of the carrier board and only connect the output side of the PB-DOUT8 26-pin output header directly to the upper or lower half of the carrier board’s 50-way front panel connector.

For a better understanding, an overview of piggyback connection in general to VMOD/ VMOD-2 is given in figure 3-3.

Figure 3-3: PB-DOUT8 Carrierboard Connection



3.2 Carrier Board Installation

After the installation of the PB-DOUT8 piggyback on its carrier board, the latter has to be configured and installed. Please refer to your carrier board's user manual for configuration and installation of the latter.



Attention!

Please refer to your carrier board's user manual also for all security advice on high voltage and ESD.



Chapter 4

Software References

4.1 Technical Features ..... 4 - 3
4.2 Memory Map ..... 4 - 3
4.3 PB-DOUT8 Registers ..... 4 - 4
4.3.1 Interrupt Handling ..... 4 - 4
4.3.2 Assembly, Revision and ID Codes ..... 4 - 4
4.3.3 I/O Registers ..... 4 - 5
4.4 Error Analysis ..... 4 - 6

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4. Software References

4.1 Technical Features

PB-DOUT8 is wired via the carrier board it is fit into to a 50-pin DSUB or to a 50-pin FB connector. There are no jumpers on the PB-DOUT8 piggyback.

During VMEbus reset, all low-side and high-side channels are switched off. Channels are kept in sitched-off condition also during power-up/down (undervoltage) of the VMEbus. External reset from VMOD2/CXM-IMOD is supported. Interrupts are supported, including a software-programmable IRQ vector.

The PB-DOUT8 read-back for output registers, including status bits, contribute to simplify software. All output registers are “0” after a hardware reset. Each group of channels has its own register.

Attention!

Depending on the number of channels being switched on/off and the actual load, PB-DOUT8 may require forced cooling if run above standard/extended temperatures.

4.2 Memory Map

The PB-DOUT8 software interface supports eight I/O lines with eight byte-wide read/write registers. If your VMOD-2 is jumpered to the base address $87FE2400, the memory map is the following:

Base +$01 Byte 1 DOUT00read/write
Base +$03 Byte 1 DOUT01read/write
Base +$05 Byte 1 DOUT02read/write
Base +$07 Byte 1 DOUT03read/write
Base +$09 Byte 1 DOUT04read/write
Base +$0B Byte 1 DOUT05read/write
Base +$0D Byte 1 DOUT06read/write
Base +$0F Byte 1 DOUT07read/write

..... reserved do not access

Base +$79 Interrupt control registerread/write
Base +$7B Assembly revision coderead/write*
Base +$7D Software revision coderead/write*
Base +$7F ID Byte ($E3)read/write*

Legend

read/write	read/write operation
*	writing is possible, but data are not used

4.3 PB-DOUT8 Registers

4.3.1 Interrupt Handling

The piggyback interrupt register (IRQ register) is located on offset $79. Each HS/LS channel is controlled by its own “interrupt enable” flag, which can be turned on/off at any time, whether an interrupt is pending or not. After reset, all interrupts are disabled automatically.

The summarised “IRQ enabled” status of all single-channel interrupts is sent to a flag (SI, “sum of interrupts”) in the interrupt status register, which permits a quick overview on whether an interrupt is pending or not through the single channels. If an interrupt request bit (SI bit) should be sent to the VMEbus, the “Master Interrupt Enable” bit (MIE bit) is set. If the factor causing the interrupt request disappears by itself, for instance if a low-side switch having undercurrent at switch on of an inductive load, the SI bit will clear itself immediately. However, the interrupt request that was generated will stay active independently of such error self-clearing. The interrupt to the VMEbus is cleared in the IRQ service routine by clearing the MIE flag. After all errors have been handled in the interrupt service routine, the MIE bit must be switched on again by the irg service routine to re-enable the interrupts.

4.3.2 Assembly, Revision and ID Codes

Hardware Assembly and Revision Code

The hardware assembly code, which is made available after having completed the installation of the piggyback, is stored on offset $7B. There is a difference between TLE5224G and TLE5224G2 due to slightly different error behaviour.

The following hardware revision codes exist:

- $00: PB-DOUT8 Ind. 00 with TLE5224G assembled;
- $01: PB-DOUT8 Ind. 01 with TLE5224G assembled;
- $02: PB-DOUT8 Ind. 01 with TLE5224G2 assembled.

Writing to this register is possible. However, the written data are not used.

Software Revision Code

The software revision code is stored on offset $7D.The following software revision codes exist:

- $00: Initial version;
- $01: Interrupts supported.

Writing to this register is possible. However, the written data are not used.

ID Code

The piggyback ID code §E3 is stored on offset $7F. Writing to this register is possible. However, the written data are not used.

4.3.3 I/O Registers

The input/output registers controlling the lines DOUT00 to DOUT07 are accessed on offsets $01, $03, $05 ... $0F. In order to simplify multitasking applications, these registers can be read back. The read-back values stand for the status lines of the high-side/low-side drivers. The write access will set the output lines.

Both the VMEbus and the VMOD-2 external reset signals reset the control logic, thus, switching off all input lines. During VMEbus reset or VMEbusVMEbus undervoltage all high-side/low-side drivers are switched off, and a local reset for the PBDOUT8 is created. After the reset is terminated, all output registers are set back to “0” and can be read back as $00.

Each output uses a single high-side driver (BTS412B2) and half a double low-side driver (TLE5224G2). The “enable” line of the TLE5224G2 (pin 11) is set permanently to “1”.

The data register offsets $01 to $0F control the data lines of the high-side and low-side drivers as follows:

Table 4-1: Registers DOUT00 to DOUT07

	MSB	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	LSB
Read	IE	0	0	0	STH	STL	DOH	DOL
Write	IE	—	—	—	—	—	DOH	DOL
Reset	0	0	0	0	0	0	0	0

Legend:

“0” Read bit as “0”. This data bit is not used, write “0”:

DOL Data output line controlling low-side driver:
“0” = driver disabled,
“1” = driver enabled.

DOH Data output line controlling high-side driver:
“0” = driver disabled,
“1” = driver enabled.

STL Status input line from the low-side driver. The status line from the low-side switch is shown inverted in this register.

STH Status input line from the high-side driver. The status line from the high-side switch is shown inverted in this register.

IE “IRQ enable” bit:
“0” = interrupt disabled,
“1” = interrupt enabled.

Table 4-2: IRQ Control Register ($77)

	MSB	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	LSB
Read	IV7	IV6	IV5	IV4	IV3	BUSI	SI	MIE
Write	IV7	IV6	IV5	IV4	IV3	BUSI	SI	MIE
Reset	0	0	0	0	0	0	0	0

Legend:

"0" Read bit as "0". This data bit is not used, write "0":

MIE "Master interrrupt enable" bit:
"0" = board is not generating interrupt,
"1" = board is generating interrupt.

SI Sum of interrupts:
"0" = non of the 8 channels is generating an interrupt,
"1" = one or more of the 8 channels is generating an interrupt.

BUSI VMEbus interrupt:
If both SI and MIE are equal to "1" BUSI is set by the Hardware Logic and an interrupt request is sent to the carrier board on which your PB-DOUT8 is installed. Thus, BUSI directly represents the status of the PB-DOUT8 IRQ line.

Inside the interrupt service routine, the MIE bit must be written with "0". The BUSI bit will be cleared by the Hardware and the PB-DOUT8 interrupt request will be cleared.

After handling all error flags of all high side switches, the SI flag will be reset to "0" by the PB-DOUT8 logic.

To enable further interrupt in case of any errors, the application interrupt service routine needs to write a "1" to the MIE bit.

IV7..3Programmable interrupt vector:
IV7...3 can be programmed, IV2...IV0 cannot be programmed and are preset to "1". IV7...IV0 are equal to $0F after reset.

4.4 Error Analysis

The PB-DOUT8 output module supports the following diagnostics modes:

- External power supply ON/OFF
- Overtemperature
- Short circuit to GND
- Short circuit to VCC
- Open load
- Undervoltage detection
- Overvoltage detection