speedMOPSlcdPM

User’s Guide

PRELIMINARY

Document Revision 0.9



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1. USER INFORMATION

1.1 About This Manual

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This KONTRON Embedded Modules product is warranted against defects in material and workmanship for the warranty period from the date of shipment. During the warranty period, KONTRON Embedded Modules will at its discretion decide to repair or replace defective products.

Within the warranty period, the repair of products is free of charge as long as warranty conditions are observed.

The warranty does not apply to defects resulting from improper or inadequate maintenance or handling by the buyer, unauthorized modification or misuse, operation outside of the product's environmental specifications or improper installation or maintenance.

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1.6 *Technical Support*

Technicians and engineers from KONTRON Embedded Modules and/or its subsidiaries and official distributors are available for technical support. We are committed to making our product easy to use and will help you use our products in your systems.

Before contacting KONTRON Embedded Modules technical support, please consult our Web site for the latest product documentation, utilities, and drivers. If the information does not help solve the problem, contact us by telephone.

Asia	Europe	North/South America
Kontron Embedded Technology (Asia Pacific)	Kontron Embedded Modules GmbH	Kontron America
Far East Science Park, 2nd Floor No. 2, Lane 50, Nan Kang Road Section 3, Nan Kang District Taipei, Taiwan	Brunnwiesenstr. 16 94469 Deggendorf – Germany	6260 Sequence Drive San Diego, CA 92121-4371
Tel: +886-2-2782-0201	Tel: +49 (0) 991-37024-0	Tel: 888-294-4558
Fax: +886-2-2782-7486	Fax: +49 (0) 991-37024-104	Fax: (858) 677-0898

2. INTRODUCTION

2.1 *speedMOPSlcdPM*

The speedMOPSlcdPM hosts Intel® Pentium® M processor in combination with an Intel® 855GM/GME chipset with an integrated graphic memory controller hub. Celeron M versions of this board are possible, too. A SDRAM-SODIMM socket can hold either PC100 or PC133 SODIMM memory modules up to 1GB. Two USB 2.0 ports and one 10/100 MBit Ethernet interfaces extend the standard connectivity of two serial ports, one parallel port, a PS/2 mouse and keyboard interface.

The speedMOPSlcdPM is a member of Kontron Embedded Modules GmbH's speedMOPS family.

2.2 *The speedMOPS Family*

Each speedMOPS module features the same pinout and interface for the following components and peripherals:

- **PC/104 and PC/104+ connector**
- **Sound**
- **2xUSB 2.0**
- **10 / 100BaseT Ethernet**
- **Keyboard**
- **PS/2 Mouse**
- **VGA**
- **RS232 serial port**
- **LPT**
- **FDC**
- **IDE1 and IDE2**

These family features allow the use of the same chassis over the whole product line and maximize design reuse.

SpeedMOPS modules allow the use of standard notebook SODIMM memory modules.

Display connections are simplified when using the onboard standard JILI Interface (JUMPtec® Intelligent LVDS Interface). JILI automatically recognizes which display is connected and independently sets all video parameters. All sppedMOPS modules are plug-and-work enabled to further reduce time-to-market.

As part of the standard features package, all sppedMOPS modules come with a JUMPtec Intelligent Device Architecture (JIDA) interface, which is integrated into the BIOS. This interface enables hardware- independent access to features that cannot be accessed via standard APIs. Functions such as watchdog timer, brightness and contrast of LCD backlight, and user bytes in the EEPROM can be configured with ease by taking advantage of this standard speedMOPS module feature.

The speedMOPS line products support the PC/104-Plus (PCI) and the PC/104 (ISA) standard via Kontron’s own, special PCI-to-ISA bridge. Because of the availability of both extension buses, all past and future PC/104 expansion assemblies with state-of-the-art processor performance can be accommodated.

3. GETTING STARTED

The easiest way to get the speedMOPSlcdPM board running is to use a starter kit from Kontron Embedded Modules GmbH. Take the following steps:

1. Turn off the power supply (part of the starter kit).
2. Connect the power supply to the starter kit baseboard (part of the starter kit).
3. Plug a suitable DDRAM memory module into the SODIMM socket of the speedMOPS.
4. Plug the speedMOPS to the PC/104 and PC/104Plus bus connectors on the starter kit baseboard.
5. Make all necessary connections from the speedMOPS to the starter kit board. (cables come with the starter kit). The starter kit board offers various interfaces on standard connectors.
6. Connect the CRT monitor to the CRT interface or a LCD panel to the JILI interface by using the corresponding adapter cable.
7. Plug a keyboard to the starter kit’s keyboard connector.
8. Connect the floppy drive (part of the starter kit) with the data cable (part of the starter kit) to the speedMOPS floppy interface.
9. Connect the power supply to the floppy’s power connector.
10. Plug a hard-drive data cable to the speedMOPS hard-disk interface. Attach the hard disk to the connector at the opposite end of the cable.
11. If necessary, connect the power supply to the hard disk’s power connector.
12. Make sure all your connections have been made correctly.
13. Turn on the power.

14. Enter the BIOS by pressing the F2 key during boot-up. Make all changes in the BIOS setup. See the BIOS chapter of this manual for details.

4. SPECIFICATIONS

4.1 *Functional Specifications*

- **Processor**
  - Intel® Pentium®-M 1.8GHz CPU
  - Intel® Celeron®-M 600 MHz or 1.0GHz ULV
  - Further processor support including Celeron®-M planned
- **Chipset**
  - Intel® 855GM/GME Chipset graphics memory controller hub
- **Power Supply**
  - +5V-only
- **Super I/O**
  - Winbond W83627HF
- **Cache**
  - On-die second level cache between 512KB and 2MB depending on used CPU
- **Memory**
  - One 200-pin 2.5V PC-1600/2100 unbuffered DDR-SDRAM, up to 1GB
- **Two Serial Ports (COM A and COM B)**
  - RS232C serial ports (10-pin headers)
  - 16550-compatible
- **One Parallel Port (LPT1)**
  - Enhanced Parallel Port (EPP) and Extended Capabilities Port (ECP) with bi-directional capability
- **Floppy Interface**
- **Enhanced Intelligent Drive Electronics (EIDE)**
  - Two Peripheral Component Interconnect (PCI) Bus Master IDE ports (up to 4 devices)

- **Universal Serial Bus (USB)**
  - 2 USB 2.0 ports
  - USB legacy keyboard support
  - USB floppy, CDROM, USB stick boot support
- **Ethernet Controller**
  - Integrated Intel® 82562 10/100BASE-T LAN
  - Follows the common criteria of the embedded technology market segment
- **Onboard Video Graphics Array (VGA)**
  - Intel® 855GM/GME Chipset graphics memory controller hub with Intel® Extreme Graphics 2 technology
  - CRT (Cathode Ray Tube) and LCD flat panel LVDS interface (JILI)
- **Audio**
  - Integrated Intel® SoundBlaster™ AC97
  - Windows Sound System™ compatible
- **Phoenix BIOS, 1024KB Flash BIOS**
- **NV-EEPROM for CMOS Setup Retention without Battery**
- **PS/2 Keyboard Controller**
- **PS/2 Mouse Controller**
- **Watchdog Timer (WDT)**
- **Real Time Clock (RTC) with Onboard Battery Supply**

4.2 *Mechanical Specifications*

4.2.1. PC/104 Bus Connector (ISA part)

- One 2 X 32 pin stackthrough and one 2 X 20 pin stackthrough connector

4.2.2. PC/104-Plus Bus Connector (PCI part)

- One 4 x 30 pin 2mm stackthrough connector

The PC/104plus connector does not have a connector shroud. This mechanical limitation does not reduce the functionality of a sppedMOPSlcdCE board.

4.2.3. Dimensions

- Length x Width: 96mm x 147mm (3,8" x 5,8")

4.2.4. Height on Top

- Maximum 31.25mm (1.23”)
- Height is depending upon CPU cooler/fan.

4.2.5. Height on Bottom

- Maximum 10.67mm (0.42”) including PC/104plus connectors

4.3 *Electrical Specifications*

4.3.1. Supply Voltage

- +5V DC +/- 5%

4.3.2. Supply Voltage Ripple

- 100mV peak to peak 0 - 20MHz

4.3.3. Supply Current (typical)

The speedMOPSlcdPM is equipped with power-saving features. Different power-consumption tests were executed to give an overview of the electrical conditions for several operational states. The board used a 512MB SDRAM module for test results shown below. An attached hard disk was not supplied through the measurement path, and there was no extension module in the system.

- speedMOPSlcdPM 0.8GHz (Celeron-M®)

Operation State	@ +5V
DOS Prompt	tbd
DOS Standby	tbd
Windows Idle	tbd
Windows Standby	tbd
Windows 100% CPU Load	tbd

- speedMOPSlcdPM 1.0GHz (Celeron-M®)

Operation State	@ +5V
DOS Prompt	2,6 A
DOS Standby	2,1 A
Windows Idle	2,2 A
Windows Standby	1,9 A
Windows 100% CPU Load	2,9 A

- speedMOPSlcdPM 1.8GHz

Operation State	@ +5V
DOS Prompt	5,7 A
DOS Standby	4,1 A
Windows Idle	4,1 A
Windows Standby	3,7 A
Windows 100% CPU Load	8,2 A

4.3.4. Real-time Clock (RTC) Battery

- Voltage range: 2.0 - 4.0V (typ 3.0V)
- Quiescent current: max. 3,5uA@ 3.0 V

English:
CAUTION ! Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.

Deutsch:
VORSICHT ! Explosionsgefahr bei unsachgemäßem Austausch der Batterie. Ersatz nur durchden selben oder einen vom Hersteller empfohlenen gleichwertigen Typ. Entsorgung gebrauchter Batterien nach Angaben des Herstellers.

French:
ATTENTION ! Risque d'explosion avec l'échange inadéquat de la batterie. Remplacement seulement par le même ou un type équivalent recommandé par le producteur. L'évacuation des batteries usagées conformément à des indications du fabricant.

Danish:
ADVARSEL ! Lithiumbatteri – Eksplosionsfare ved fejlagtig Håndtering. Udskifting må kun skemed batteri af samme fabrikant og type. Lever det brugte batteri tilbage til leverandØren.

Finnish:
VAROITUS ! Paristo voi räjähtää, jos se on virheellisesti asennettu. Vaihda paristo ainoastaan laltevalmistajan suosittelmaan tyyppiln. Havita kaytetty paristo valmistajan ohjeiden mukaisesti.

Spanish:
Precaución ! Peligro de explosión si la batería se sustituye incorrectamente. Sustituya solamente por el mismo o tipo equivalente recomendado por el fabricante. Disponga las baterías usadas según las instrucciones del fabricante.

The battery of this product is not considered to be accessible by the end user. Safety instructions are given only in English, German, French, Danish, Finish and Spanish. If the battery is accessible by the end user, it is in the responsibility of the customer to give the corresponding safety instructions in the required language(s).

4.4 MTBF

The following MTBF (Mean Time Between Failure) values were calculated using a combination of manufacturer's test data (if the data was available) and a Bellcore calculation for the remaining parts. The Bellcore calculation involved the "Method 1 Case 1" method. In that particular method, the components were assumed to be operating at a 50% stress level in a 40° C ambient environment, and the system was assumed to have not been burned in. Manufacturer's data was used wherever possible. The manufacturer's data, when used, was specified at 50° C, which means that the following results were slightly conservative. The MTBF values shown below were for a 40° C office or telecommunications environment. Higher temperatures and other environmental stresses (extreme altitude, vibration, and salt water exposure) will lower the MTBF values.

- System MTBF (hours) : tbd

Notes: Fans shipped with Kontron Embedded Modules GmbH products have an operating life of up to 50,000 hours.
The estimates above assumed that a passive heat-sinking arrangement was used instead of a fan.
Estimated RTC battery life (as opposed to battery failures) was not accounted for in the above figures and needs separate consideration. Battery life depends on temperature and operating conditions. When the Kontron unit has external power, battery drain comes from leakage paths.

4.5 *Environmental Specifications*

4.5.1. Temperature

The Intel® Mobile Pentium®-M is specified for proper operation when junction temperature is within the specified range of 0°C to 100°C.

The Intel® 855GM/GME Chipset temperature and the Intel® ICH4 I/O Controller Hub 4 (82801DB) case temperature are maximum 110°C.

- Operating: 0 to +60 C (*) (with appropriate airflow)
- Non-operating: -10 to +85 °C (non-condensing)

Note: (*) The maximum operating temperature is the maximum measurable temperature on any spot on the module's surface. You must maintain the temperature according to the above specification.

4.5.2. Humidity

- Operating: 10% to 90% (non-condensing)
- Non-operating: 5% to 95% (non-condensing)

5. CPU, CHIPSET AND SUPER I/O

5.1 CPU

The speedMOPSlcdPM is available with an Intel® Mobile Pentium®-M central processing unit (CPU) of 1.8GHz. However, other GHz as well as Celeron®-M versions (half cache size, no SpeedStep® technology) of this board are planned.

Intel® Mobile Pentium®-M CPU features include:

- Supports Intel® Architecture with Dynamic Execution
- High performance, low-power core
- On-die, primary 32-kbyte instruction cache and 32-kbyte write-back data cache
- On-die, 1-MByte (BANIAS), 2-MByte (DOTHAN) or 512-kByte (CELERON) second level cache with Advanced Transfer Cache Architecture
- Advanced Branch Prediction and Data Prefetch Logic
- Streaming SIMD Extensions 2 (SSE2)
- 400-MHz, Source-Synchronous processor system bus
- Advanced Power Management features, including Enhanced Intel SpeedStep® technology (only for Pentium® M processors)

5.2 *Chipset*

The chipset of the speedMOPSlcdPM consists of the Intel® 855GM/GME chipset GMCH (Graphics and Memory Controller Hub) and the Intel ® 82801DB ICH-4 (I/O Controller Hub 4).

5.2.1. GMCH (855GM/GME Chipset)

- **Processor/Host Bus Support**
  - Intel® Pentium® M and Celleron® M processors
  - Supports system bus at 400MHz
  - Supports Enhanced Intel® SpeedStep® technology
- **Memory System**
  - Directly supports one DDR SDRAM channel, 64-bits wide
  - Supports 200/266-MHz DDR SDRAM devices with double-sided SO-DIMMs (four rows populated) with unbuffered PC1600/PC2100 DDR SDRAM.
  - Supports 128-Mbit, 256-Mbit, and 512-Mbit technologies providing maximum capacity of 1 GB with x16 devices
  - All supported devices have four banks
- **Internal Graphics Features**
  - Up to 32MB of dynamic video memory allocation
  - Display image rotation
  - Graphics core frequency
  - Display core frequency at 133MHz or 200MHz
  - Render core frequency at 100MHz,133MHz, 200MHz
  - 2D graphics engine
  - 3D graphics engine
  - Single- or dual-channel LVDS panel support up to UXGA panel resolution with frequency range from 25MHz to 112MHz (single channel/dual channel)
- **Video Stream Decoder**
  - Improved hardware motion compensation for MPEG2
  - Software DVD at 60 Fields/second and 30 frames/second full screen
  - Support for standard definition DVD (i.e. NTSC pixel resolution of 720x480, etc.) quality encoding at low CPU utilization
- **Power Management**
  - APM 1.2 compliant power management
  - ACPI 1.0b, 2.0 support
  - Enhanced Intel® SpeedStep Technology support

5.2.2. ICH4 (82801DB)

- **PCI 2.2 Bus interface at 33MHz**
- **Integrated LAN controller**
  - WfM 2.0 and IEEE802.3 compliant with 10/100 Mbit/s Ethernet support
- **USB**
  - Two UHCI USB 1.1 or one EHCI high speed USB 2.0 host controller(s)
- **AC-Link for AC'97 support**
- **Integrated IDE controller**
  - Ultra ATA33 and PIO mode support
  - Two channels for up to 3 devices with independent timing
  - Support of "Native Mode" register and interrupts
- **Interrupt Controller**
  - Two cascade 83C59 with 15 interrupts
  - Integrated I/O APIC capability with 24 interrupts
- **Enhanced DMA**
  - Two cascaded 8237 controllers
  - Supports PC/PCI DMA and LPC DMA
  - Supports DMA collection buffers
- **Timers based on 82C54**
- **Power Management Logic**
  - ACPI 2.0 compliant
  - Supports PCI PME#
- **Low Pin Count (LPC) Interface**
- **SM Bus 2.0 interface (System Management Bus)**

5.3 Super I/O

A super I/O Winbond W83627HF device is connected to the LPC (Low Pin Count) Bus. This device provides the following additional features:

- Two serial ports (RS232)
- One Multi-Mode Parallel Port
- Floppy Disk Controller
- PS/2-Keyboard and PS/2-Mouse Interface

5.4 CPU, Chipset and Super-I/O Configuration

See the Advanced Menu and its submenus section in the Appendix C: BIOS chapter for information on setting choices.

6. SYSTEM MEMORY

The speedMOPSlcdPM 200-pin DDR Small Outline-Dual Inline Memory Modules (SO-DIMMs). One socket is available for a 2.5-volt, unbuffered PC-1600/2100 DDR-SDRAM with ECC, module of 128, 256, 512MB or 1GB capacity

The total amount of memory available on the DDRAM module is used for main memory and graphics memory on the speedMOPSlcdPM. The Unified Memory Architecture (UMA) manages how the system shares memory between the graphics controller and the processor.

7. ISA AND PCI BUS EXPANSION

The design of the speedMOPSlcdPM offers ISA- and PCI-bus signals on PC/104 and PC/104-Plus connectors. The PC/104-Plus standard is downward compatible with PC/104 and enables the use of standard PC/104 and PC/104-Plus adapter cards.

7.1 *PC/104 Bus (ISA part)*

The PC/104 bus consists of two connectors that use 104 pins in total.

- **XT bus connector (64 pins)**
- **AT bus connector (40 pins, which is optional for 16-bit, data-bus system)**

The pin-out of the PC/104 bus connectors corresponds to the pin-out of the ISA bus connectors with some added ground pins. The two PC systems with different form factors are electrically compatible.

The **XT bus connector**, Row A and B.

The corresponding 64-pin female header (ISA bus = 62pins) has two added ground pins at the end of the connector (Pin A32 and Pin B32). The pin-out between PC/104 bus and XT ISA bus is identical between A1 - A31 and B1 - B31.

The **AT bus extension connector**, Row C and D.

The corresponding 40-pin female header (ISA bus = 36 pins) has four added ground pins, including two on each side of the connector. To avoid confusion, the first two pins are defined as Pin C0 and Pin D0. The additional ground pins at the end of the connector are defined as C19 and D19. The pin-out between PC/104 bus and AT ISA bus is identical between C1 - C18 and D1 - D18.

7.1.1. PC/104 Connectors

The speedMOPSlcdPM features the XT bus and AT bus extension on two, dual-row socket connectors with a 2.54mm x 2.54mm grid (0.1" x 0.1").

The PC-104 bus is available through Connectors J6B and J6C.

A description of the signals, including electrical characteristics and timings is beyond the scope of this document. Please refer to the official ISA bus and PC/104 specifications for more details.

7.1.2. PC/104 Configuration

When using add-on boards on the PC/104 bus, make sure that there are no resource conflicts in the system. Carefully choose hardware interrupts, DMA channels, and memory and I/O address ranges to avoid resource conflicts, which are often the reason for a board or a feature not functioning correctly. See Appendix A: System Resource Allocation for information about the resources already used by the speedMOPSlcdPM.

7.2 *PC/104-Plus (PCI part)*

The speedMOPSlcdPM offers the PC/104-Plus bus on a quad-row female connector with a 2mm x 2mm (0.79” x 0.79”) pitch. This connector implements the standard 32-bit PCI bus signals.

7.2.1. PC/104-Plus Connector

You can use PC/104-Plus adapter boards on the top and on the bottom of a speedMOPSlcdPM’s stackthrough connector. The PC/104plus connector does not have a connector shroud. If you intend to use +3.3V powered PC/104plus adapter cards, the +3.3V has to be supplied separately, because it is not generated onboard of the speedMOPSlcdPM.

The PC/104-Plus bus is available through Connector J8.

A description of signals, including electrical characteristics and timings, is beyond the scope of this document. Please refer to the official PCI bus and PC/104-Plus specifications for more details.

7.2.2. PC/104-Plus Configuration

Add-on boards on the PC/104-Plus bus have to be associated to a “PCI-slot.” Make sure that there are no resource conflicts in the system. Carefully choose PCI interrupts, REQ/GNT pairs, and IDSEL for the add-on board. See the technical manual of the add-on board for more details.

The speedMOPSlcdPM’s PCI bus can be configured to optimize your system. See the PCI Configuration Submenu in Appendix C: BIOS for more information on configuration.

8. GRAPHICS INTERFACES

8.1 *Video Controller*

The uses the graphics accelerator integrated in the Intel® 855GM/GME chipset, which delivers high-performance 2D, 3D and video capabilities. With its interface to UMA (Unified Memory Architecture) up to 32MB of system memory are used as video memory.

The controller can drive two interfaces with its graphics engines on the speedMOPSlcdPM:

- Cathode Ray Tube (CRT) interface
- Low Voltage Differential Signaling (LVDS) interface

8.2 *CRT Connector*

The CRT monitor interface is available through the X21 connector (6 pins). To have the signals available on a standard DSUB-15 CRT monitor connector, an adapter cable is required. A 15-pin DSUB cable is available from Kontron (KAB-VGA-2, Part Number 96053-0000-00-0).

The following table shows the pin-out of the CRT connector.

Header	Pin	Signal Name	Function	DSUB-25
	1	RED	Analog video red	1
	2	GRN	Analog video green	2
	3	BLU	Analog video blue	3
	4	GND	Signal ground	7
	5	VSYNC	Vertical sync	14
	6	HSYNC	Horizontal sync	13

8.3 Flat Panel LVDS Interface (JILI) Connector

The interface for the LCD Panel is available through Connector X2 (40 pins). To find the location of the LCD Panel interface connector, please see the Appendix E: Connector Layout chapter.

This connector represents the JILI interface (**J**UMPtec **I**ntelligent **L**VDS **I**nterface). The implementation of this subsystem complies with the JILI Specification from Kontron Embedded Modules GmbH. This supports the JILI3 implementation. A variety of cables for different display types are available from Kontron. Please refer to the actual cable list on the Kontron Web site for part numbers and cable names. A detailed description of the JILI interface standard also is available in a separate document JILIM???.PDF. The three question marks represent the documents revision number. You can download this document from the Kontron Web site, or contact your local Kontron technical support to receive it.

8.4 Display Power Considerations

When using a LCD Panel, additional voltages may be required to drive the display's logic and to supply the backlight converter and the contrast voltage.

The display logic may require +5V for standard or +3.3V for low-power LCDs. Contrast voltages for passive displays are normally very different and can range from –30V to +30V. Backlight converters usually are +5V or +12V types. When using a Kontron JILI cable, you do not need to determine the configuration. Display logic voltage and contrast voltage come pre-configured on the JILI cable. On occasion, the backlight voltage has to be adjusted on the cable.

Even though the speedMOPSlcdPM also is available as a +5V-only board, you need to supply the +12V for the backlight converter when using such a converter type.

The onboard 3.3V-circuitry of the speedMOPSlcdPM and the +3.3V logic voltage of low-voltage panels are powered by separate voltage regulators. The one for the LCD is mounted on the JILI adapter cable.

8.5 Connecting a LCD Panel

To determine whether your panel display is supported, check the Kontron Web site for panel lists. We regularly update the list of panels that have been tested with our boards.

Many panel adapters for a wide spread variety of displays are available through Kontron. If you use one of those adapters supplied by Kontron, configuration is easy:

1. Check whether you have the correct adapter and cable for the panel you plan to use. Inspect the cable for damages.
2. Disconnect the power from your system.
3. Connect the panel adapter to the LCD Panel connector (JILI) on the speedMOPSlcdPM.
4. Connect the other end of the cable to your display.
5. Connect the backlight converter.
6. Supply power to your system.
7. If no image appears on your display, connect a CRT monitor to the CRT connector.
8. If necessary program the EEPROM on the JILI cable with the matching configuration data.
9. If you still do not see improvement, consider contacting the dealer for technical support.

8.6 Configuration

You can set the general configuration for the graphics controller in the BIOS setup utility. Refer to the Advanced Chipset Control submenu and the Display Control submenu in the Appendix C: BIOS Operation chapter for more configuration information.

You can download available drivers for the graphics controller from the Kontron Web site. For further information read the read-me or help files or contact technical support.

8.7 Graphics Technical Support

If problems occur, you can solve some of them by using the latest drivers for the graphics controller. Kontron provides you with the latest tested drivers, which can differ from newer ones. For further technical support, contact either Kontron, or obtain support information and downloadable software updates from Intel®.

8.8 *Available Video Modes*

The following list shows the video modes supported by the graphics controller with their maximum legacy frame-buffer size. When configured for smaller frame buffers and/or using a LCD panel on the JILI interface, not all of the video modes listed below may be available. Capability depends on the system configuration and on the display. Different operating systems also may not support all listed modes by the available drivers.

8.8.1. Standard IBM-Compatible VGA Modes

Video Mode	Type	Characters/Pixels	Colors/Gray val.
00h/01h	Text	40x25	16
02h/03h	Text	80x25	16
04h/05h	Graphics	320x200	4
06h	Graphics	640x200	2
0Dh	Graphics	320x200	16
0Eh	Graphics	640x200	16
0Fh	Graphics	640x350	Mono
10h	Graphics	640x350	16
11h	Graphics	640x480	2
12h	Graphics	640x480	16
13h	Graphics	320x200	256

8.8.2. Extended VESA VGA Modes

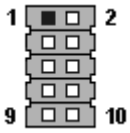
VESA	Display	Pixels	Colors
101h	Graphics	640x480	256
103h	Graphics	800x600	256
105h	Graphics	1024x768	256
107h	Graphics	1280x1024	256
111h	Graphics	640x480	64K
112h	Graphics	640x480	16M
114h	Graphics	800x600	64K
115h	Graphics	800x600	16M
117h	Graphics	1024x768	64K
118h	Graphics	1024x768	16M
11Ah	Graphics	1280x1024	64K
11Bh	Graphics	1280x1024	16M
13Ah	Graphics	1600x1200	256
13Ch	Graphics	1920x1440	256
14Bh	Graphics	1600x1200	64K
14Dh	Graphics	1920x1440	64K
15Ah	Graphics	1600x1200	16M
15Ch	Graphics	1920x1440	16M

9. SERIAL-COMMUNICATION INTERFACES

Two fully functional serial ports (COMA and COMB) provide asynchronous serial communications. COMA and COMB support RS-232 operation modes. They are 16550 high-speed UART compatible and support 16-byte FIFO buffers for transfer rates from 50baud to 115.2Kbaud.

9.1 *Connectors*

COMA is available through the X13 connector (10 pins) and COMB through the X15 connector (10 pins). To have the signals available on the standard serial interface connectors DSUB9 or DSUB25, an adapter cable is required. A 9-pin DSUB cable is available from Kontron (KAB-DSUB9-2, Part Number 96017-0000-00-0). The following table shows the pinouts for COMA and COMB, as well as necessary connections for DSUB adapters.

Header	Pin	Signal Name	Function	In / Out	DSUB-25	DSUB-9
	1	/DCD	Data Carrier Detect	In	8	1
	2	/DSR	Data Set Ready	In	6	6
	3	RxD	Receive Data	In	3	2
	4	/RTS	Request to Send	Out	4	7
	5	TxD	Transmit Data	Out	2	3
	6	/CTS	Clear to Send	In	5	8
	7	/DTR	Data Terminal Ready	Out	20	4
	8	/RI	Ring Indicator	In	22	9
	9	GND	Signal Ground	--	7	5
	10	VCC *	+5V	--	--	--

Notes: (*) To protect the external power lines of peripheral devices, make sure that:
-- the wires have the right diameter to withstand the maximum available current
-- the enclosure of the peripheral device fulfils the fire-protecting requirements of
-- IEC/EN 60950.

To find the location of the serial ports on the board, please see the Appendix E: Connector Layout chapter.

9.2 *Configuration*

You can set the two serial input/output interfaces to a variety of I/O addresses and IRQ configurations. Settings are changeable from the BIOS menu. Refer to the I/O Device Configuration submenu in the Appendix C: BIOS Operation chapter for configuration information.

Note:	Most operating systems detect the serial port with the I/O address 3F8h as COM1 and 2F8h as COM2.

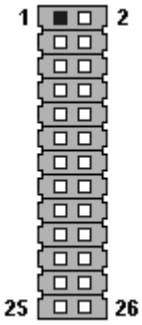
10. PARALLEL-PORT INTERFACE

The speedMOPSlcdPM incorporates a parallel port that can be set to uni-directional and supports EPP and ECP operating modes.

10.1 *Connector*

The parallel port is available through the X10 connector (26 pins). To have the signals available on a standard, parallel-interface connector DSUB-25, an adapter cable is required, which is offered by Kontron (KAB-DSUB25-1, Part Number 96015-0000-00-0).

The following table shows the pinout as well as necessary connections for a DSUB-25 adapter.

Header	Pin	Signal Name	Function	In / Out	DSUB-25
	1	/STB	Strobe	Out	1
	3	PD0	Data 0	I/O	2
	5	PD1	Data 1	I/O	3
	7	PD2	Data 2	I/O	4
	9	PD3	Data 3	I/O	5
	11	PD4	Data 4	I/O	6
	13	PD5	Data 5	I/O	7
	15	PD6	Data 6	I/O	8
	17	PD7	Data 7	I/O	9
	19	/ACK	Acknowledge	In	10
	21	/BUSY	Busy	In	11
	23	PE	Paper out	In	12
	25	/SLCT	Select out	In	13
	2	/AFD	Autofeed	Out	14
	4	/ERR	Error	In	15
	6	/INIT	Init	Out	16
	8	/SLIN	Select in	Out	17
	26	VCC *	+ 5 V	--	NC
	10,12	GND	Signal Ground	--	18 - 25
	14,16	GND	Signal Ground	--	18 - 25
	18,20	GND	Signal Ground	--	18 - 25
	22,24	GND	Signal Ground	--	18 - 25

Notes: (*) To protect the external power lines of peripheral devices, make sure that:
-- the wires have the right diameter to withstand the maximum available current
-- the enclosure of the peripheral device fulfils the fire-protecting requirements of
-- IEC/EN 60950.

To find the location of the parallel port on the board, please see the Appendix E: Connector Layout chapter.

10.2 Configuration

The parallel-port mode, I/O addresses, and IRQs are changeable in the MOPSlcd7 BIOS Setup Utility. You can program the base I/O-address 378h, 3BCh, 278h, disable the interface or set it to AUTO. You can choose IRQ5 or IRQ7 as the parallel-port interrupt. In ECP mode, you can choose DMA 1 or DMA 3.

Refer to the I/O Device Configuration Submenu in the Appendix C: BIOS Operation chapter for additional information on configuration.

11. KEYBOARD AND FEATURE INTERFACE

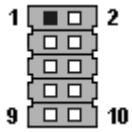
The keyboard and feature connector of the speedMOPSlcdPM offers five functions. The interface connects the following:

- Keyboard
- Keyboard lock switch
- Speaker
- Battery
- Reset button

11.1 *Connector*

The keyboard and feature connector is available through Connector X14 (10 pins). An adapter cable is required to connect a standard keyboard to this interface. There are two adapter cables available from Kontron. One can be used for AT-keyboard (KAB-KB-1, Part Number 96023-0000-00-0), the other for PS/2-keyboard (KAB-KB-PS2, Part Number 96060-0000-00-0). The adapter cables do not know the other functions on this interface.

The following table shows the pinout as well as necessary connections for adapters.

Header	Pin	Signal Name	Function	5-pin Din (Diode)	6-pin MiniDin (PS2)
	1	Speaker	Speaker output		
	2	GND	Ground		
	3	/RESIN	Reset input		
	4	/KBLOCK	Keyboard lock		
	5	KBDAT	Keyboard data	2	1
	6	KBCLK	Keyboard clock	1	5
	7	GND	Ground	4	3
	8	VCC *	+5V	5	4
	9	BATT	Battery in (3,0V)		
	10	PWRGOOD	Powergood		

Notes: (*) To protect the external power lines of peripheral devices, make sure that:
-- the wires have the right diameter to withstand the maximum available current

```
-- the enclosure of the peripheral device fulfils the fire-protecting requirements of
-- IEC/EN 60950.
```

To find the location of the keyboard and feature connector on the board, please see the Appendix E: Connector Layout chapter.

11.2 Signal Descriptions

/KBLOCK (Keyboard Lock)

- Input on CPU modules
- Output on any other module
- Input to the keyboard controller input Port 1, Bit 7

/RESIN and PWRGOOD (Reset Inputs)

- Input on CPU modules
- When POWERGOOD goes high, it starts the reset generator on the CPU module to pull the onboard reset line high after a valid reset period. You also can use this pin as a low active hardware reset for modules.

Speaker

- Open collector output on modules that drive a piezo electronic speaker.
- Input on modules that connects a 5V piezo electronic speaker to this pin.
- An 8-Ohm loudspeaker also can be connected between SPEAKER and GND, but because of current limitation the volume will be low.
- Connect only one speaker to this pin. The CPU usually drives this pin. However, other modules also can use this signal to drive the system speaker.

KBDAT (Keyboard Data)

- Bi-directional I/O pin on CPU modules
- Keyboard data signal

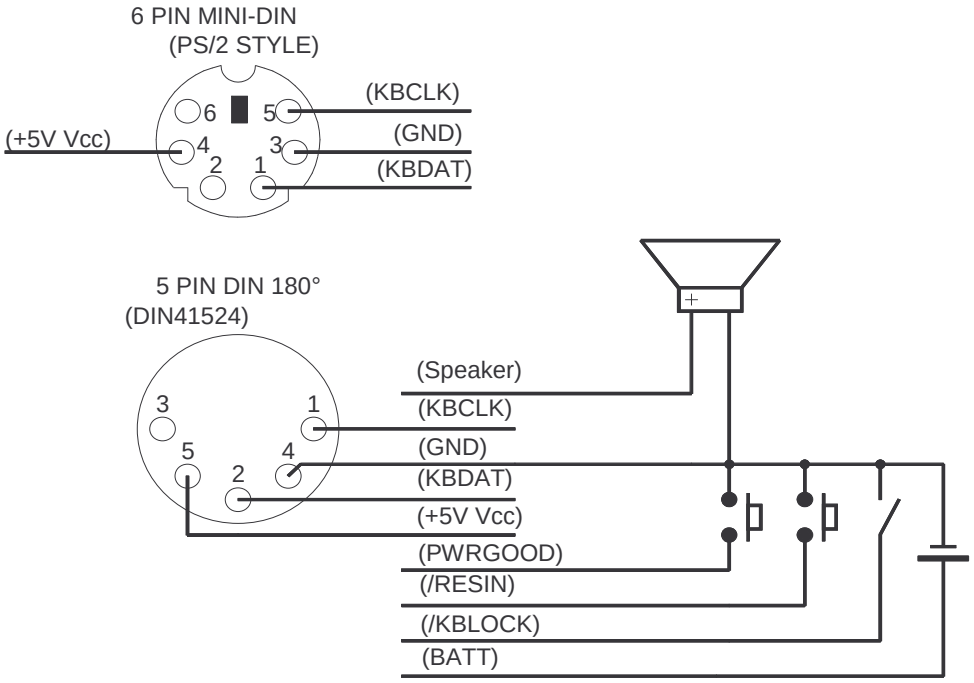
KBCLK (Keyboard Clock)

- Bi-directional I/O pin on CPU modules
- Keyboard clock signal

BATT (System Battery Connection)

- This pin connects a system battery to all modules.
- The battery voltage has to be higher than 2.2V and lower than 4.5V. A 3V battery is recommended.
- A battery is not needed to hold CMOS setup data. Your configurations for hard disks, floppy drives, and other peripherals are saved in an onboard EEPROM. However, you need a battery to save the CMOS date and time when power supply is turned off.

11.2.1. Example Connection AT-keyboard and Other Functions



11.3 *Configuration*

Refer to the Keyboard Features submenu in the Appendix C: BIOS chapter for information on configuration of the keyboard interface.

12. PS/2 MOUSE INTERFACE

The super-I/O controller of the speedMOPSlcdPM supports a PS/2 mouse.

12.1 Connector

The PS/2 mouse interface is available on Connector X18 (4 pins). An adapter cable is required to connect a standard PS/2 mouse. The cable is available from Kontron (KAB-MOUSE-PS2, Part Number 96062-0000-00-0).

The following table shows the pinout and connections for a PS/2 mouse adapter.

Header	Pin	Signal Name	Function	6-pin MiniDin (PS2)
	1	MSDAT	Mouse data	1
	2	VCC *	+5V	4
	3	GND	Ground	3
	4	MSCLK	Mouse clock	5

Notes: (*) To protect the external power lines of peripheral devices, make sure that:
-- the wires have the right diameter to withstand the maximum available current
-- the enclosure of the peripheral device fulfils the fire-protecting requirements of
-- IEC/EN 60950.

To find the location of the PS/2 mouse connector on the board, please see the Appendix E: Connector Layout chapter.

12.2 Configuration

You can set the PS/2 mouse to enabled, disabled or autodetect from the BIOS Setup. If you enable the mouse, the IRQ12 is used as the interrupt and is no longer available for other devices. Please refer to the Advanced Menu in the Appendix C: BIOS chapter for additional information on configuration.

13. USB INTERFACES

The speedMOPSlcdPM comes with two USB 2.0 ports, which you can expand by adding external hubs. You can connect up to 127 USB peripherals.

13.1 *Connector*

The USB ports are available through the X16 and the X17 connectors (4 pins) each. To find the location of the USB ports on the speedMOPSlcdPM board, please see the Appendix E: Connector Layout chapter. To have the signals available on the standard USB interface connectors, an adapter cable is required. A USB interface cable is available from Kontron (KAB-USB-1, Part Number 96054-0000-00-0).

The following table shows the pinouts for the USB connector.

Header	Pin	Signal Name	Function
	1	VCC *	+5V
	2	USB0	USB-
	3	USB1	USB+
	4	GND	Ground

Notes: (*) To protect the external power lines of peripheral devices, make sure that:
-- the wires have the right diameter to withstand the maximum available current
-- the enclosure of the peripheral device fulfils the fire-protecting requirements of
-- IEC/EN 60950.

The current of each power line is internal limited to 500mA by a resetable fuse.

13.2 Configuration

You can enable or disable the USB UHCI Host Controller in the BIOS Setup Utility for support of USB 1.1 devices.

For high-speed USB 2.0 support of the two ports, enable the USB EHCI Host Controller.

You also can enable or disable the legacy USB support. Legacy support is required for a USB keyboard and a USB Mouse when used with non USB aware operating systems such as Unix or DOS. It also is required to boot from USB mass storage devices. For more information, see the I/O Device Configuration Submenu section in Appendix C: BIOS Operation.

You can download available drivers or get driver download support information from the Kontron Web site. Kontron offers the latest Kontron-tested drivers, which can differ from newer ones. For further technical questions, contact your local support or get support information and downloadable software updates from Intel®.

Notes:	1.	Some operating systems without USB 2.0 support do not work well with EHCI controller enabled. If you install such an OS at this board please disable the EHCI controller in the Setup Utility before installation.
	2.	For operating systems not listed on our Web site please contact your OS distributor for an USB 2.0 driver. We are not allowed by law to ship USB 2.0 drivers.

14. FLOPPY INTERFACE

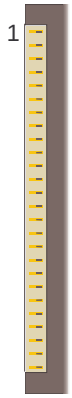
The floppy-drive interface of the speedMOPSlcdPM uses a 2.88MB super I/O floppy-disk controller and can support one floppy disk drive with densities that range from 360kB to 2.88MB.

14.1 *Connector*

The floppy disk interface is available on the flat-foil Connector X9 (26 pins). To find the location of floppy-drive interface on the speedMOPSlcdPM board, please see the Appendix E: Connector Layout chapter. This type of connector is often internally used in notebooks to connect a slim-line floppy drive.

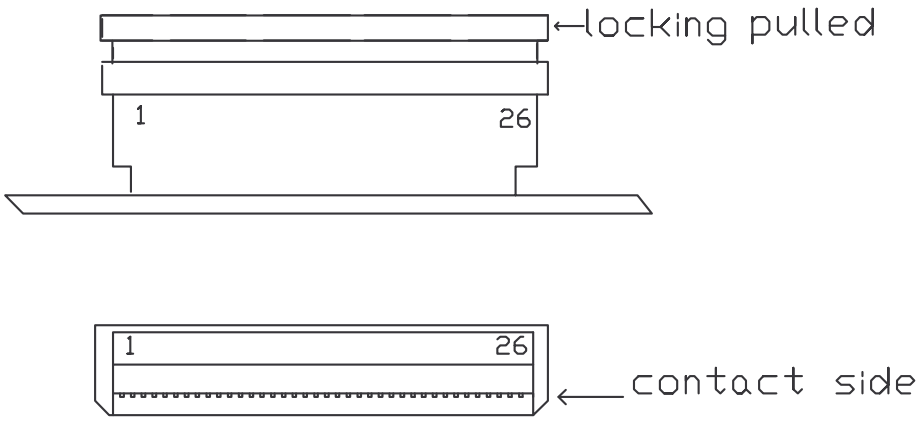
Accessories are available for this interface from Kontron. To connect a standard 3.5" floppy drive, use an adapter cable (ADA-FLOPPY-2, Part Number 96001-0000-00-0). If you have a slim-line 3.5" floppy drive, you may need a flat foil cable (KAB-FLOPPY/MOPS-1, Part Number 96019-0000-00-0). It also is possible to get a slim line 3.5" floppy drive with cable from Kontron (FLOPPY-MOPS-1, Part Number 96010-0000-00-0).

The following table shows the connector pin-out.

Header	Pin	Signal Name	Function	Pin	Signal Name	Function
	1	VCC *	+5V	2	/IDX	Index
	3	VCC *	+5V	4	/DR0	Drive Select 0
	5	VCC *	+5V	6	/DSKCHG	Disk Change
	7	NC	Not connected	8	NC	Not connected
	9	NC	Not connected	10	/MTR0	Motor on 0
	11	NC	Not connected	12	/FDIR	Direction Select
	13	NC	Not connected	14	/STEP	Step
	15	GND	Ground	16	/WDATA	Write Data
	17	GND	Ground	18	/WGATE	Write Gate
	19	GND	Ground	20	/TRK0	Track 00
	21	GND	Ground	22	/WRTPRT	Write Protect
	23	GND	Ground	24	/RDATA	Read Data
	25	GND	Ground	26	/HDSEL	Side One Select

Notes: (*) To protect the external power lines of peripheral devices, make sure that:
-- the wires have the right diameter to withstand the maximum available current
-- the enclosure of the peripheral device fulfils the fire-protecting requirements of
-- IEC/EN 60950.

14.1.1. Connector Diagram



14.2 *Configuration*

You can configure the floppy disk interface in the BIOS Setup Utility. You can choose the 3.5” (common) or 5.25” drive types with densities of 360kB, 720kB, 1.2MB, 1.25MB, 1.44MB or 2.88MB. Refer to the Main Menu and the Miscellaneous Menu section of the Appendix C: BIOS Operation chapter for more information on configuring the floppy drive.

You also can disable the floppy-disk interface in the I/O Device Configuration Submenu.

15. IDE INTERFACES

The speedMOPSlcdPM features two EIDE interfaces (Ultra DMA 33 mode) that can drive up to four hard disks. When two devices share a single adapter, they are connected in a master/slave, daisy-chain configuration.

15.1 *Connector*

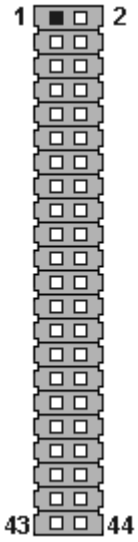
The IDE interfaces are available through Connector X11 (IDE1 - 44 pins) and X12 (IDE2 - 44 pins). These interfaces are designed in 2mm grid for optimal connectivity to a 2.5” hard disk.

There are several accessories available for IDE connectivity.

You can use two cables to directly connect a hard disk in a 2.5” form factor (KAB-IDE-2MM, Part Number 96021-0000-00-0) or a 3.5” form factor (KAB-IDE-25, Part Number 96020-0000-00-0).

You can plug a Kontron chipDISK, which is an IDE hard disk that uses Flash technology, into the IDE interface. You also can use a chipDISK adapter (chipDISK-ADA1, Part Number 96004-0000-00-0) or compact Flash adapter (CFC-ADA1, Part Number 96004-0000-00-2) for more disk support.

The following table shows the pin-out of the two IDE connectors.

Header	Pin	Signal Name	Function	Pin	Signal Name	Function
	1	/RESET	Reset	2	GND	Ground
	3	HDD7	Data 7	4	HDD8	Data 8
	5	HDD6	Data 6	6	HDD9	Data 9
	7	HDD5	Data 5	8	HDD10	Data 10
	9	HDD4	Data 4	10	HDD11	Data 11
	11	HDD3	Data 3	12	HDD12	Data 12
	13	HDD2	Data 2	14	HDD13	Data 13
	15	HDD1	Data 1	16	HDD14	Data 14
	17	HDD0	Data 0	18	HDD15	Data 15
	19	GND	Ground	20	Key (NC)	Key pin
	21	DRQ	IDE DMA Request	22	GND	Ground
	23	/IOW	I/O write	24	GND	Ground
	25	/IOR	I/O read	26	GND	Ground
	27	IOCHRDY	I/O channel ready	28	CSEL	Cable select
	29	/AKJ	Acknowledge	30	GND	Ground
	31	SIRQ	Interrupt	32	NC	Not connected
	33	SA1	Addr 1	34	NC	Not connected
	35	SA0	Addr 0	36	SA2	Addr 2
	37	/CS1	Chip select 1	38	/CS3	Chip select 3
	39	NC	Not connected	40	GND	Ground
	41	VCC (*)	+5V	42	VCC (*)	+5V
	43	GND	Ground	44	NC	Not connected

Notes: (*) To protect the external power lines of peripheral devices, make sure that:
-- the wires have the right diameter to withstand the maximum available current
-- the enclosure of the peripheral device fulfils the fire-protecting requirements of
-- IEC/EN 60950.

To find the location of IDE-controller interfaces on the speedMOPSlcdPM board, please see the Appendix E: Connector Layout chapter.

15.2 *Configuration*

The IDE interface offers several configuration settings. Refer to the “I/O Device Configuration Submenu” section in the “Appendix C: BIOS Operation” chapter for additional information on configuration.

16. ETHERNET INTERFACES

The Ethernet interface of the speedMOPSlcdPM uses the ICH4's integrated 32-bit PCI LAN controller in combination with the Intel® 82562 platform LAN connect device.

The network controller support a 10/100Base-T interface. The devices auto-negotiate the use of a 10Mbit/sec or 100Mbit/sec connection.

All major network-operating systems and several real-time and embedded operating systems support the interface.

16.1 *First Ethernet Controller*

Intel® 82562 features include:

- IEEE 802.3 10Base-T/100Base-TX Compliant Physical Layer Interface
- IEEE 802.3u Auto-Negotiation Support
- IEEE 802.3x Full Duplex Flow Control Standard
- Digital Adaptive Equalization Control
- Link Status Interrupt Capability
- 10Base-T auto-polarity correction
- Platform LAN Connect Interface Support
- Diagnostic Loopback Mode
- 1:1 transmit transformer ratio support
- Low power (less than 300mW in active transmit mode)
- Reduced power in "unplugged mode"

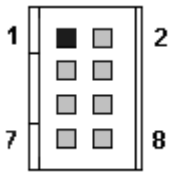
Note: The Ethernet interface works according to the common criteria of the embedded technology market segment.

16.2 Connector

The Ethernet interface is available through connector X19 (8 pins).

To have the signals of the Ethernet connection available on a standard RJ45 connector, you need an adapter cable, which is offered by Kontron (KAB-MOPS-ETN1, Part Number 96048-0000-00-0).

The following table shows the pinout.

Header	Pin	Signal Name	Function	In/Out
	1	TXD+	10BASE-T Transmit	Differential Output
	2	TXD-	10BASE-T Transmit	Differential Output
	3	RXD+	10BASE-T Receive	Differential Input
	4	SHLDGND	Shield ground	
	5	SHLDGND	Shield ground	
	6	RXD-	10BASE-T Receive	Differential Input
	7	SHLDGND	Shield ground	
	8	SHLDGND	Shield ground	

Notes: TXD+, TXD- differential-output pair drives 10 and 100Mb/s Manchester-encoded data to 100/10BASE-T transmit lines.
RXD+, RXD- differential input pair receives 10 and 100Mb/s Manchester-encoded data from 100/10BASE-T receive lines.

To find the location of the Ethernet interfaces on the board, please see the Appendix E: Connector Layout chapter.

16.3 Configuration

The onboard LAN controller can be enabled or disabled from the BIOS Setup Utility. You also can enable the onboard LAN PXE boot ROM to allow the system to boot-up via a network connection from a PXE boot server. Refer to the I/O Device Configuration Submenu in the Appendix C: BIOS Operation chapter for additional information on configuration.

You can download available drivers from the Kontron Web site. For further information read the read-me file or contact technical support.

16.4 Ethernet Technical Support

If any problems occur, you can solve some of them by using the latest drivers for the Intel® LAN controller. Kontron provides you with the latest Kontron-tested drivers, which can differ from newer ones. For further technical support, contact either Kontron

or get support information and downloadable software updates from Intel®.

17. SOUND INTERFACE

The speedMOPSlcdPM uses a Crystal CS4299 sound codec. The CS4299 is an 18-bit, full duplex AC'97 2.1 compatible stereo audio CODEC designed for PC multimedia systems.

All major operating systems support the interface.

The CS4299 features:

- AC '97 2.1 Compatible
- 18-bit stereo Analog-to-Digital Converters
- 20-bit Stereo Digital-to-Analog Converters
- Sample Rate Converters
- MIC input
- Extensive Power Management Support

17.1 Connector

The sound connector is available through Connector X1 (6 pins). The following table shows the pinout.

Header	Pin	Signal Name	Function
	1	Right	Line-level stereo output right.
	2	ASGND	Analog Ground
	3	Left	Line-level stereo output left.
	4	AUXAR_C	Auxiliary A input right. Normally intended for connection to an internal or external CD-ROM analog output.
	5	MIC_C	Mono Microphone input.
	6	AUXAL_C	Auxiliary A input left. Normally intended for connection to an internal or external CD-ROM analog output.

17.2 Configuration

From the BIOS Setup Utility in the I/O Device Configuration Submenu, you can set the onboard legacy audio to Disabled (default) or Enabled. You can enable legacy Sound Blaster compatibility mode or MPU-401 legacy MIDI support. Several configurations for I/O-addresses, interrupts and DMA-channels are possible. Refer to the Appendix C: BIOS operation for more details

You can download available drivers for the sound controller from the Kontron Web site or use the drivers provided by the manufacturer Realtek. Search for ALC650 drivers for the required operating system.

17.3 Technical Support for Sound

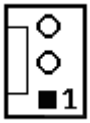
If problems occur, you can solve some of them by using the latest drivers for the Sound controller. Kontron provides you with the latest tested drivers, which can differ from newer ones. For further technical support, contact either Kontron, or obtain support information and downloadable software updates from Realtek.

18. FAN INTERFACE

Some speedMOPSlcdPMs can be equipped with a fan. If a fan has to be changed or added, use this interface to connect a fan to cool the CPU. The connector and onboard system controller monitor the fan's speed. This connector supports 5V fans only.

18.1 *Connector*

The fan interface is available on Connector X20 (3 pins). For the location of the fan connector see Appendix E: Connector Layout.

Header	Pin	Signal Description	Function
	1	Sense	Speed Monitoring
	2	VCC *	+5V
	3	GND	Ground

Notes: (*) To protect the external power lines of peripheral devices, make sure that:
-- the wires have the right diameter to withstand the maximum available current
-- the enclosure of the peripheral device fulfils the fire-protecting requirements of
-- IEC/EN 60950.

18.2 *Configuration*

You do not need to configure this feature.

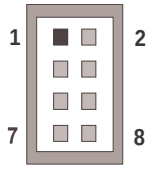
19. POWER INTERFACE

In some applications, the speedMOPSlcdPM is intended for use as a stand-alone module without a backplane. You need to have a power connector available on the board for direct power supply. The speedMOPSlcdPM is a +5V-only board. Peripherals can obtain additional voltage from the power connectors next to the PC/104 bus. The additional voltages (+3.3V, +12V, -5V and -12V) are not generated onboard the speedMOPSlcdPM.

Two connectors provide power to the speedMOPSlcdPM and it is strictly recommended to use both connectors. To find the location of the power connectors on the board, please see the Appendix E: Connector Layout chapter.

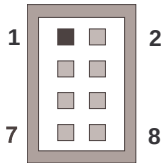
19.1 *Main Power Connector*

The main power connector is available as X4A (8 pins). The following table shows the pinout.

Header	Pin	Signal Name	Function
	1	GND	Ground
	2	VCC	+5V
	3	BATT	Battery
	4	+12V	+12V
	5	-5V	-5V
	6	-12V	-12V
	7	GND	Ground
	8	VCC	+5V

19.2 *Auxiliary Power Connector*

The auxiliary power connector is available as X8 (8 pins). The following table shows the pinout.

Header	Pin	Signal Name	Function
	1	GND	Ground
	2	VCC	+5V
	3	VCC	+5V
	4	GND	Ground
	5	GND	Ground
	6	VCC	+5V
	7	VCC	+5V
	8	GND	Ground

Notes: (*) To protect the external power lines of peripheral devices, make sure that:
-- the wires have the right diameter to withstand the maximum available current
-- the enclosure of the peripheral device fulfils the fire-protecting requirements of
-- IEC/EN 60950.

19.3 Power Pins

Every power pin on the two power connectors as well as on the PC/104 bus connectors is limited to a maximum current of 1A per pin.

If a system using a speedMOPSlcdPM is only supplied from the two power connectors, the following limitations apply:

Power	Number of Pins on both power connectors	Max. Current
VCC (+5V)	6	6A
+12V	1	1A
-12V	1	1A
-5V	1	1A
GND	6	6A

A system using the speedMOPSlcdPM also can be supplied from the PC/104 bus connectors. If only those supply voltages pins are used, the following limitations apply:

Power	Number of pins on ISA part	Max. Current
VCC (+5V)	4	4A
+12V	2	2A
-12V	2	2A
-5V	2	2A
GND	8	8A

Modules on the PC/104 bus consuming a higher supply current must provide power supply through an additional connector.

Note: The speedMOPSlcdPM is not a replacement for a backplane. Use all power pins on the power connectors and on the PC/104 connectors for power supply to the board, and also use all additional power connectors on additional I/O cards, if your system exceeds the above limitations. It is not acceptable to use only the power pins of the PC/104 connector for power supply of the full PC/104 stack.

19.4 Configuration

The speedMOPSlcdPM is equipped with a power management system (APM). You can configure lots of options for power-saving states such as standby state with partial power reduction and suspend state with full-power reduction. You can specify wake-up events that bring the system back to full-on state. Please refer to the “Power Menu” section in the “Appendix C: BIOS Operation” chapter.

Note:	If running in ACPI mode the video is disabled before shutdown. Therefore the message to switch of the computer can not be seen.

19.5 External Battery

You can connect an external battery to Pin 3 (BATT) of the power connector instead of Pin 9 of the keyboard connector. For more information refer to the Keyboard and Feature Interface section.

Note: The two battery inputs are protected against each other by diodes.

20. WATCHDOG TIMER

The watchdog timer (WDT) is integrated in the Winbond W83627HF controller of the speedMOPSlcdPM and can issue a reset to the system or generate a non-maskable interrupt (NMI). The watchdog timer circuit has to be triggered within a specified time by the application software. If the watchdog timer is not triggered because proper software execution fails or a hardware malfunction occurs, it resets the system or generates the NMI.

20.1 *Configuration*

You can set the watchdog timer to disabled, reset or NMI mode. You can specify the delay time and the timeout (trigger period) from 1 second to 30 minutes. The delay time is the time after first initialization before the trigger period starts. The timeout is the time the watchdog timer has to be triggered within. You can make the initialization settings in the BIOS setup. Refer to the Watchdog Settings Submenu in the Appendix C: BIOS Operation chapter for information on configuration.

20.2 *Programming*

20.2.1. Initializing the WDT

You can initialize the watchdog timer from the BIOS setup. You also can set up the initialization from the application software with help of the JIDA (Jumptec Intelligent Device Architecture) programmer’s interface.

20.2.2. Triggering the WDT

The watchdog timer needs to be triggered out of the application software within a specified timeout period. You can only do this in the application software with the help of the JIDA programmer’s interface.

For information about the JIDA programmer’s interface, refer to the JIDA BIOS extension section in the Appendix C: BIOS chapter and separate documents that are available in the JIDA software packages on the Kontron Web site.

21. HARDWARE MONITOR

The Winbond W83627HF controller monitors several critical hardware parameters of the system, including power-supply voltages, fan speed and CPU temperature, which are very important for a high-end computer system to remain stable and function properly. This controller is connected via the SM (System Management) bus to the south bridge.

The following parameters are monitored:

- +3.3V from onboard DC/DC
- CPU core voltage
- +5V standby voltage
- Battery voltage
- CPU temperature with on-die diode
- CPU fan speed (planed)

21.1 *Configuration*

You can use the Hardware Monitor submenu in the BIOS Setup Utility to obtain information on voltages, fan speed and to check the temperature of the CPU die. For more information on this submenu, see the Appendix C: BIOS Operation chapter in this manual.

To monitor the parameters of this feature from your operating system, Kontron recommends that you use the 32-bit protected mode JUMP*tec*'s Intelligent Device Architecture driver (JIDA 32) with the test and demo application for Windows 95/98/ME/NT/2000/XP, which is available on the KONTRON Web site.

22. THERMAL MANAGEMENT

The Thermal Management feature of the speedMOPSlcdPM helps control the processor's temperature by activating the automatic thermal throttling after the processor silicon reaches a certain temperature. This feature can be enabled and configured in the BIOS Setup utility. You can specify the temperature level when throttling starts, define a hysteresis value to get back to 100% CPU performance, and specify the percentage for CPU performance in throttling mode. Automatic thermal throttling mode does not require additional hardware, software drivers, or interrupt-handling routines.

Additionally the processor of the speedMOPSlcdPM protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all execution when the junction temperature exceeds the sensor setting. This is signaled to the system by the THERMTRIP# (Thermal Trip) pin. Once activated, the signal remains latched, and the processor stopped, until RESET# goes active. There is no hysteresis built into the thermal sensor itself; as long as the die temperature drops below the trip level, a RESET# pulse will reset the processor and execution will continue. If the temperature has not dropped below the trip level, the processor will continue to drive THERMTRIP# and remain stopped. The temperature level for catastrophic overheating being activated is 135°C.

23. APPENDIX A: SYSTEM-RESOURCE ALLOCATION

23.1 *Interrupt Request (IRQ) Lines*

IRQ #	Use	Available	Comment
0	Timer0	No	
1	Keyboard	No	
2	Slave 8259	No	
3	COM2	No	Note (1)
4	COM1	No	Note (1)
5	Sound	No	Note (1), Note (2), Note (3)
6	FDC	No	Note (1)
7	LPT1	No	Note (1)
8	RTC	No	
9		Yes	
10		Yes	
11		Yes	
12	PS/2 Mouse	No	Note (1)
13	FPU	No	
14	IDE0	No	Note (1)
15	IDE11	No	Note (1)

Notes: (1) If the „used for“-device is disabled in setup, the corresponding interrupt is available for other devices.
(2) Possible setting for LPT1. IRQ7 is the default setting.
(3) Used in Soundblaster compatibility mode.

23.2 Direct Memory Access (DMA) Channels

DMA #	Use	Available	Comment
0		Yes	
1	Sound	No	Note (1), (2)
2	FDC	No	Note (1)
3	LPT	Yes	Note (2)
4	Cascade	No	
5		Yes	
6		Yes	
7		Yes	

Notes: (1) If the „used for"-device is disabled in setup, the corresponding DMA channel is available for other devices.
(2) Possible setting for LPT1 if configured for ECP mode.

23.3 Memory Map

speedMOPSlcdPM processor modules can support up to 512MB of memory. The first 640KB of SDRAM are used as main memory.

Using DOS, you can address 1MB of memory directly. Memory area above 1MB (high memory, extended memory) is accessed under DOS via special drivers such as HIMEM.SYS and EMM386.EXE, which are part of the operating system. Please refer to the operating system documentation or special textbooks for information about HIMEM.SYS and EMM386.EXE.

Other operating systems (Linux or Windows versions) allow you to address the full memory area directly.

Upper Memory	Use	Available	Comment
A0000h – BFFFFh	VGA Memory	No	Mainly used by graphic adapter cards. If a PCI graphic card is in the system this memory area is mapped to the PCI bus.
C0000h – CFFFFh	VGA BIOS, PXE ROM	No	
D0000h – DFFFFh		Yes	Free for ISA bus or shadow RAM in standard configurations. If JRC software is used, a 16K block is shadowed for BIOS extension, starting with first free area at D0000h, D4000h, D8000hor DC000h. (BIOS extensions do not use the whole shadow block.).
E0000h – F0000h	System BIOS, USB legacy support	No	

23.3.1. Using Expanded Memory Managers

speedMOPSlcdPM extension BIOSes can be mapped to an upper memory area. (See the previous table.) Some add-on boards also have optional ROMs or use drivers that communicate with their corresponding devices via memory mapped I/O such as dual-ported RAM. These boards have to share the upper memory area with the Expanded Memory Manager's EMS frame. This often causes several problems in the system.

Most EMMs scan the upper memory area for extension BIOSes (optional ROMs) and choose a free memory area for their frame if it is not explicitly set. Normally, they are not always capable of detecting special memory-mapped I/O areas. You need to tell the EMM which memory areas are not available for the EMS frames, which is most of the time done by using special exclusion parameters.

If the Expanded Memory Manager you use cannot detect extension BIOSes (optional ROMs), make sure you excluded all areas in the upper memory, which are used by extension BIOSes, too. Your instruction in the CONFIG.SYS concerning the Expanded Memory Manager should look like this: (question marks for location of extension BIOS).

MS-DOS Example

```
DEVICE=EMM386.EXE X=????-???? X=E000-FFFF
```

Note: When booting up your system using this configuration under MS-DOS, the exclusion of area F000 to FFFF causes a warning. Microsoft reports that this message will always appear when the F000 segment lies in the shadow RAM. This is a bug of EMM386, not the speedMOPSlcdPM.

Please read the technical manuals of add-on cards used with the speedMOPSlcdPM for the memory areas they use. If necessary, also exclude their memory locations to avoid a conflict with EMM386.

23.4 I/O Address Map

The I/O-port addresses of the speedMOPSlcdPM are functionally identical with a standard PC/AT. All addresses not mentioned in this table should be available. We recommend that you do not use I/O addresses below 0110hex with additional hardware for compatibility reasons, even if available.

Address (h)	Use	Available	Comment
0000 - 001F	DMA Controller 1	No	Fixed
0020 - 003D	Interrupt Controller 1	No	Fixed
002E - 002F	LPC Super I/O	No	Fixed
0040 - 0053	Timer, Counter	No	Fixed
004E - 004F	LPC Super I/O	No	Fixed
0060 - 0067	Keyboard controller	No	Fixed
0070 - 0077	Real Time Clock and CMOS Registers	No	Fixed
0080 - 008F	DMA Page Register	No	Fixed
0090 - 009F	DMA Control	No	Fixed
0092	Reset Generator	No	Fixed
00A0 00BF	Interrupt Controller 2	No	Fixed
00C0 - 00DF	DMA Controller 2	No	Fixed
00E1 - 00E2	System Control	No	Fixed
00F0	Math. Coprocessor	No	Fixed
0100 - 010F	General Purpose I/O	No	Kontron Control Port, Fixed
0170 - 0177	Hard Disk Drive (Secondary)	No	Available if IDE port 2 is disabled
01F0 - 01F7	Hard Disk Drive (Primary)	No	Available if IDE port 1 is disabled
0200 - 026F	System Resources	No	Fixed
0274 - 0279	ISA PNP Data	No	Fixed
0278 - 027F	LPT	Yes	Possible address for LPT
0290 - 0297	System Resources	No	Fixed
02F8 - 02FF	COM2	No	Available if COM is disabled
0376	IDE Controller 2	No	Available if IDE port 2 is disabled
0378 - 037F	LPT	No	Available if LPT is disabled
03B0 - 03DF	Graphic Subsystem	No	Fixed
03F0 - 03F7	Floppy Controller	No	Available if floppy controller is disabled
03F6	IDE Controller 1	No	Available if IDE port 1 is disabled
03F8 - 03FF	COM1	No	Available if COM is disabled
04D0 - 04D1	Interrupt Select	No	Fixed
0600 - 060F	System Resources	No	Fixed
0678 - 067F	ECP LPT	Yes	Used when LPT mode is set to ECP
0778 - 077F	ECP LPT	Yes	Used when LPT mode is set to ECP
0A79	ISA PNP Data	No	Fixed
0CF8 - 0CFF	PCI Configuration	No	Fixed
1000 - 107F	System Resources	No	Fixed
1180 - 11BF	System Resources	No	Fixed
1800 - 181F	USB Host Controller	No	Dynamic (address if all PCI onboard devices are on)
1C00 - 1C0F	Ultra ATA Storage Controller	No	Dynamic (address if all PCI onboard devices are on)
2000 - 201F	SM-Bus Controller	No	Dynamic (address if all PCI onboard devices are on)
2400 - 243F	Sound	No	Dynamic (address if all PCI onboard devices are on)
2800 - 28FF	Sound	No	Dynamic (address if all PCI onboard devices are on)
3000 - 30FF	Ethernet Contr. DM9102	No	Dynamic (address if all PCI onboard devices are on)
3400 - 343F	Ethernet Contr. Intel	No	Dynamic (address if all PCI onboard devices are on)

23.5 Peripheral Component Interconnect (PCI) Devices

All devices follow the PCI 2.1 specification. The BIOS and OS control memory and I/O resources. Please refer to the PCI 2.1 specification for details.

PCI Device (IDSEL)	PCI IRQ	REQ/ GNT	Comment
AGP Graphic	-	-	Separate bus, integrated in Intel chipset
Intel Ethernet (AD24)	INTE#	Discrete channel	
Davicom Ethernet (AD17)	INTD#	REQ#3/GNT#3	PC/104-Plus allows 3 external masters REQ#0, REQ#1 and REQ#2
AC97 Sound	INTB#		Separate bus, integrated in Intel chipset
1st UHCI USB Controller	INTA#	-	Separate bus, integrated in Intel chipset
EHCI USB Controller	INTH#		Separate bus, integrated in Intel chipset

23.6 SM Bus Devices

The speedMOPSlcdPM uses an onboard SM (System Management) Bus. This bus is not available on an external connector.

The following SM Bus addresses are already used on the speedMOPSlcdPM.

SM Bus Address	SM Device	Comment
10h/11h	SM-Bus Host	Integrated in Intel ICH4
A0h/A1h	SPD EEPROM	Part of the DDR SDRAM module
D2h/D3h	Clock Generator	

Note: Accesses to the onboard SM Bus devices that are not allowed may cause system failures. Problems resulting from this are not under warranty!

24. APPENDIX B: IMPORTANT TECHNOLOGY INFORMATION

The following technological information is designed to give the reader a better understanding of some of features of the speedMOPSlcdPM. This information can be referenced when reading the “SYSTEM RESOURCES” and “BIOS OPERATION” sections that follow. There are also references to additional documentation that will help to develop a better understanding of the technical information described herein.

24.1 *I/O APIC vs 8259 PIC Interrupt mode*

The I/O APIC (Advanced Programmable Interrupt Controller) handles interrupts differently then the 8259 PIC. The following information explains these differences.

24.1.1. Method of interrupts transmission

The I/O APIC transmits interrupts through the system bus and interrupts are handled without the needs for the processor to run an interrupt acknowledge cycle.

24.1.2. Interrupt priority

The priority of interrupts in the I/O APIC is independent of the interrupt number.

24.1.3. More interrupts

The I/O APIC in the chipset of the speedMOPSlcdPM supports a total of 24 interrupts.

The APIC is not supported by all operating systems. Only Windows Xp supports APIC. The APIC mode must be enabled in the BIOS setup before the OS installation. APIC only works in ACPI mode.

For more information see chapter 8 of the IA-32 Intel Architecture Software Developer’s Manual, Volume 3.

Note: Enable the APIC mode if your OS supports it.

24.2 Native vs. compatible IDE mode

Windows XP SP1 and Windows Server 2003 will switch a native-mode-capable ATA controller from compatible to native mode if the BIOS indicates that the controller can be switched, the controller supports native mode and the appropriate registry entry is set. You must add a DWORD VALUE called **EnableNativeModeATA** under; ***HKEY_LOCAL_MACHINE/System/CurrentControlSet/Control/PnP/Pci/*** and set 1 as the value.

24.2.1. Compatible Mode

The ATA controller emulates a legacy IDE controller, which is a non-standard extension of the ISA-based IDE controller. In compatible mode, the controller requires two ISA IRQs (14 and 15) that cannot be shared with other devices.

24.2.2. Native Mode

The ATA controller acts as a true PCI device that does not require dedicated legacy resources and can be configured anywhere in the system. ATA controllers running in native mode use their PCI interrupt for both channels and can share this interrupt pin with other devices in the system, like any other PCI device.

By requiring only one shareable interrupt instead of two non-shareable ones, native-mode controllers significantly decrease the likelihood that a user will install a device that cannot work because no interrupts are available.

Enable Native IDE mode if your OS supports it.

Note: For more information see:
http://www.microsoft.com/whdc/hwdev/tech/storage/Native-modeATA.mspx

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24.3 Thermal Monitor and Catastrophic Thermal Protection

The Thermal Monitor within the Pentium M processor helps to control the processor temperature by activating the TCC (Thermal Control Circuit) when the processor silicon reaches its maximum operating temperature. The temperature at which the Intel Thermal Monitor activates the TCC is **not** user-configurable and is **not** software visible.

The Thermal Monitor controls the processor temperature by modulating (starting and stopping) the CPU core clocks at a 50% duty cycle (TM1) or by initiating an Enhanced Intel SpeedStep technology transition (TM2) when the processor silicon reaches its maximum operating temperature (selectable in setup).

Notes: TM2 is the recommended mode for the Intel Pentium M processor.
Not supported on the speedMOPSlcdPM Celeron M version.

Thermal Monitor supports two modes to activate the TCC: Automatic and On-Demand mode. The Intel Thermal Monitor Automatic Mode must be enabled via BIOS for the processor to be operating within specification.

Automatic mode does not require any additional hardware, software drivers, or interrupt handling routines.

Note: With a properly designed thermal solution, the TCC is only active for very short periods, hence processor performance impact is expected to be so minor that it would not be detectable.
For more details see *chapter 5.1.2 of the Intel Pentium M Processor Datasheet*.

The Intel Pentium M processor supports the THERMTRIP# signal for catastrophic thermal protection.

In the event of a catastrophic cooling failure, the processor will automatically shut down when the silicon has reached a temperature of approximately 125°C. At this point the system BUS signal THERMTRIP# will go active.

THERMTRIP# activation is independent of processor activity and does not generate any bus cycles.

24.3.1. Summary

Thermal Control Circuit reduces performance when the processor reaches its max. operating temperature (100°C). THERMTRIP# shuts down the system in case of catastrophic cooling failure.

24.4 *Processor Performance Control*

The Pentium M processor can run in different performance states (multiple frequency/voltage operating points). The CPU performance can be altered while the computer is functioning. This allows the processor to run at different core frequencies and voltages depending on CPU thermal state and OS policy.

Windows XP includes built-in processor performance control to operate the processor more efficiently when it is not fully utilized. Win2k, WinME and Win9x do not support processor performance control. Special software is required for OSes not capable of processor performance control.

In Windows, the processor performance control policy is linked to the Power Scheme setting in the control panel power option applet.

Notes: Windows always runs at the highest performance state when the “Home/Office” or “Always On” power scheme is selected.
For a more detailed information about processor performance control, see:
Chapter 8 of the ACPI Specification Revision 2.0c available at www.acpi.info
Windows platform design note at
http://www.microsoft.com/whdc/hwdev/tech/onnow/procperfctrl.mspx

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24.5 *Thermal Management*

ACPI allows the OS to play a role in the thermal management of the system. With the OS in control of the operating environment, cooling decisions can be made based on the application load on the CPU and the thermal heuristics of the system.

The ACPI thermal solution on speedMOPSlcdPM supports three cooling policies:

- Active Cooling

  The OS is turning the fan on/off. Active cooling devices typically consume power and produce noise, but are able to cool a thermal zone without limiting system performance. The **active cooling trip point** declares the temperature threshold the OS uses to decide when to start/stop active cooling devices. See section 14.6 for more information about the speedMOPSlcdPM onboard Fan control.

- Passive Cooling

  The OS reduces the power consumption of the processor by throttling the processor clock to reduce the temperature of the thermal zone. Passive cooling devices (processor) produce no noise. **The passive cooling trip point** declares the temperature threshold where the OS will start or stop passive cooling.

- Critical Trip Point

The OS performs an orderly, but critical, shutdown of the system when the temperature reaches the **critical trip point**.

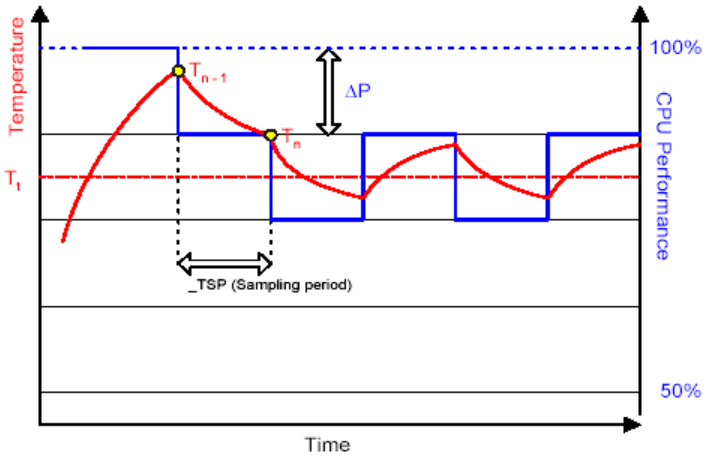
24.6 *speedMOPSlcdPM onboard Fan connector*

This section describes how to connect a fan to the connector located directly on the speedMOPSlcdPM. With certain BIOS-settings it is possible to control the fan depending on the Active Trip Point temperature. The fan switches on/off depending on the adjusted Active Trip Point temperature. In order for this feature to function properly an ACPI compliant OS is necessary.

Note: The speedMOPSlcdPM can not control the revolutions per minute (R.P.M) of the fan.

24.7 Processor Clock Throttling

The ACPI OS assesses the optimum CPU performance change necessary to lower the temperature using the following equation:



$$\Delta P[\%] = TC1(T_n - T_{n-1}) + TC2(T_n - T_t)$$

ΔP is the performance delta, T_t is the target temperature = critical trip point. The two coefficients TC1 and TC2 and the sampling period TSP are hardware dependent constants the end user must supply (setup options section 16.6.1 ACPI Control Submenu).

It's up to the end user to set the cooling preference of the system by setting the appropriate trip points in the BIOS setup.

Note: See chapter 12 of the ACPI specification (www.acpi.info) for more details.

24.8 ACPI Suspend Modes and Resume Events

speedMOPSlcdPM, only supports the S1 (POS=Power On Suspend) state. S3 (=Save to Ram) is not supported.

S4 (=Save to Disk) is not supported by the BIOS (S4_BIOS) but it is supported by the following operating systems:

- **WinME**
- **Win2k**
- **WinXP (S4_OS=Hibernate).**

The following events resume the system from S1:

- **PS/2 Keyboard and Mouse IRQs (1 & 12)**
- **USB Wake Events**
- **PCI Bus signal PME#**

25. APPENDIX C: BIOS OPERATION

The speedMOPSlcdPM comes with Phoenix BIOS 4.0, Release 6.1, which is located in the onboard Flash EEPROM in compressed from. The device has an 8-bit access. The shadow RAM feature offers faster access (16 bit). You can update the BIOS using a Flash utility. For complete Phoenix BIOS 4.0 information, visit the Phoenix Technologies Web site.

25.1 *Determining the BIOS Version*

To determine the BIOS version of the speedMOPSlcdPM, immediately press the <**Pause/Break**> key on your keyboard as soon as you see the following text display in the upper left corner of your screen:

```
PhoenixBIOS 4.0 Release 6.1
Copyright 1985-2003 Phoenix Technology Ltd.
All Rights Reserved
Kontron(R) BIOS Version <PPM1R112>
Copyright 2002-2005 Kontron Embedded Modules GmbH
```

Whenever you contact technical support about BIOS issues, providing a BIOS version <PPM1R???> is especially helpful.

The system BIOS provides additional information about the board's serial number, CPU, and memory information by displaying information similar to the following:

```
S/N: MAA010102

CPU = Intel(R) Pentium(TM) M processor 1.80GHz
247M System RAM Passed
2048K Cache SRAM Passed
System BIOS shadowed
Video BIOS shadowed

UMB upper limit segment address: E554
```

The board's serial number has valuable information for technical support. speedMOPSlcdPM serial numbers always start with MA and are followed by a character and six digits. The first three positions represent the lot number (here A01), and the last four digits are the number of the board in that lot (here board number 102).

25.2 *Configuring the System BIOS*

The Phoenix BIOS setup utility allows you to change system behavior by modifying the BIOS configuration. Setup-utility menus allow you to make changes and turn features on or off.

BIOS setup menus represent those found in most models of the speedMOPSlcdPM. The BIOS setup utility for specific models can differ slightly.

Note: Selecting incorrect values can cause system boot failure. Load setup-default values to recover by pressing <**F9**>.

25.2.1. Start Phoenix BIOS Setup Utility

To start the Phoenix BIOS Setup Utility, press the <**F2**> key when the following string appears during boot-up.

```
Press <F2> to enter Setup
```

The Main Menu then appears.

25.2.2. General Information

The **Setup Screen** is composed of several sections:

Setup Screen	Location	Function
Menu Bar	Top	Lists and selects all top-level menus.
Legend Bar	Bottom	Lists setup navigation keys.
Item Specific Help Window	Right	Help for selected item.
Menu Window	Left Center	Selection fields for current menu.
General Help Window	Overlay (center)	Help for selected menu.

Menu Bar

The menu bar at the top of the window lists different menus. Use the left/right arrow keys to make a selection.

Legend Bar

Use the keys listed in the legend bar on the bottom to make your selections or exit the current menu. The table below describes the legend keys and their alternates.

Key	Function
<F1> or <Alt-H>	General Help window.
<Esc>	Exit menu.
← or → Arrow key	Select a menu.
↑ or ↓ Arrow key	Select fields in current menu.
<Tab> or <Shift-Tab>	Cycle cursor up and down.
<Home> or <End>	Move cursor to top or bottom of current window.
<PgUp> or <PgDn>	Move cursor to next or previous page.
<F5> or <->	Select previous value for the current field.
<F6> or <+> or <Space>	Select next value for the current field.
<F9>	Load the default configuration values for this menu.
<F10>	Save and exit.
<Enter>	Execute command or select submenu.
<Alt-R>	Refresh screen.

Selecting an Item

Use the ↑ or ↓ key to move the cursor to the field you want. Then use the + and - keys to select a value for that field. **Save Value** commands in the **Exit** menu save the values displayed in all menus.

Displaying Submenus

Use the ← or → key to move the cursor to the submenu you want. Then press <**Enter**>. A pointer (▸) marks all submenus.

Item Specific Help Window

The Help window on the right side of each menu displays the Help text for the selected item. It updates as you move the cursor to each field.

General Help Window

Pressing <**F1**> or <**ALT-F1**> on a menu brings up the General Help window that describes the legend keys and their alternates. Press <**Esc**> to exit the General Help window.

25.3 *Main Menu*

Feature	Option	Description
System Time	HH:MM:SS	Sets system time. Press <Enter> to move to MM or SS.
System Date	MM/DD/YYYY	Sets system date. Press <Enter> to move to DD or YYYY.
Legacy Diskette A	360 Kb, 5 ¼ “ 1.2 MB, 5 ¼ “ 720 Kb, 3 ½ “ **1.44/1.25 MB, 3 ½ “** 2.88 MB, 3 ½ “ Disabled	Select the type of floppy disk drive.
Legacy Diskette B	360 Kb, 5 ¼ “ 1.2 MB, 5 ¼ “ 720 Kb, 3 ½ “ 1.44/1.25 MB, 3 ½ “ 2.88 MB, 3 ½ “ **Disabled**	Select the type of floppy disk drive.
‣ Primary Master	Autodetected drive	Displays result of PM autotyping.
‣ Primary Slave	Autodetected drive	Displays result of PS autotyping.
‣ Secondary Master	Autodetected drive	Displays result of SM autotyping.
‣ Secondary Slave	Autodetected drive	Displays result of SS autotyping.
Smart Device Monitoring	Disabled **Enabled**	Turns on Self-Monitoring Analysis-Reporting Technology, which monitors the condition of the hard drive and reports when a catastrophic IDE failure is about to happen.
System Memory	N/A	Displays amount of conventional memory detected during boot-up.
Extended Memory *	N/A	Displays amount of extended memory detected during boot-up.

Notes: In the Option column, bold shows default settings.
(*) Extended Memory = capacity of memory module – selected frame buffer memory size (Video boot type)

25.3.1. Master or Slave Submenus

Feature	Option	Description
Type	None User **Auto** CD-ROM IDE Removable ATAPI Removable Other ATAPI	None = Autotyping is not able to supply the drive type or end user has selected None, disabling any drive that may be installed. User = End user supplies HDD information. Auto = Autotyping. The drive itself supplies the information. CD-ROM = CD-ROM drive. ATAPI Removable = Read- and writeable media e.g. LS120 and USB-ZIP Other ATAPI = for ATAPI devices not supported by other HDD features.
Cylinders	1 to 65,536	Number of cylinders.
Heads	1 to 256	Number of read/write heads.
Sectors	1 to 63	Number of sectors per track.
Maximum Capacity	N/A	Displays the calculated size of the drive in CHS.
Total Sectors	N/A	Number of total sectors in LBA mode.
Maximum Capacity	N/A	Displays the calculated size of the drive in LBA.
Multi-Sector Transfer	**Disabled** 2 sectors 4 sectors 8 sectors 16 sectors	Any selection except Disabled determines the number of sectors transferred per block. The standard is one sector per block.
LBA Mode Control	**Disabled** Enabled	Enabling LBA causes Logical Block Addressing to be used in place of CHS.
32-Bit I/O	**Disabled** Enabled	Enables 32-bit communication between CPU and IDE card. Requires PCI or local bus.
Transfer Mode	**Standard** Fast PIO 1 Fast PIO 2 Fast PIO 3 Fast PIO 4 FPIO 3 / DMA 1 FPIO 4 / DMA 2	Selects the method for transferring the data between the hard disk and system memory.
Ultra DMA Mode *	Disabled MODE 0 MODE 1 MODE 2	Selects the UDMA mode to move data to/from the drive. Autotype the drive to select the optimum transfer mode. This feature is autodetected.
SMART Monitoring	Disabled Enabled	Shows whether a disk supports SMART.

Note: In the Option column, bold shows default settings.
(*) The board only supports up to UDMA33. This is a limitation from the 44pin IDE interfaces.

25.4 *Advanced Menu*

Feature	Option	Description
▸ Advanced Chipset Control	Sub menu	Opens Advanced Chipset Control sub menu.
▸ PCI/PNP Configuration	Sub menu	Opens PCI/PNP Config sub menu.
▸ Memory Cache	Sub menu	Opens Cache Control sub menu.
▸ I/O Device Configuration	Sub menu	Opens Peripheral Config sub menu.
▸ Keyboard Features	Sub menu	Opens Keyboard Features sub menu.
▸ Hardware Monitor	Sub menu	Shows hardware monitor current state.
▸ Watchdog Settings	Sub menu	Opens Watchdog Config sub menu.
▸ Display Control	Sub menu	Opens Display Control sub menu
▸ Miscellaneous	Sub menu	Opens sub menu with miscellaneous options.

25.4.1. Advanced Chipset Control Submenu

Feature	Option	Description
Enable Memory gap	**Disabled** Extended	Allows enabling a 1MB memory gap for add-on cards at 15MB.
Graphics Engine 1	Disabled **Extended**	Enable or Disable the integrated graphics device by setting the desired value.
Graphics Engine 2	Disabled **Extended**	Enable or Disable the integrated graphics device by setting the desired value.
Graphics Memory	UMA = 1MB **UMA = 8MB** UMA = 16MB UMA = 32MB	Select the amount of Main Memory that the integrated graphics device will use.
Assign IRQ to VGA	**Yes** No	Determines whether the integrated graphics device gets an IRQ assigned.

Note: In the Option column, bold shows default settings.

25.4.2. PCI/PNP Configuration Submenu

Feature	Option	Description
PNP OS installed	**No** Yes	If your system has a PnP OS (such as Win9x), select Yes to let the OS configure PnP devices not required for booting. No allows the BIOS to configure them.
Reset Configuration Data *	**No** Yes	Yes erases all configuration data in ESCD, which stores the configuration settings for plug-in devices. Select Yes when required to restore the manufacturer's defaults.
Secured Setup Configuration	**Yes** No	Yes prevents a Plug and Play OS from changing system settings.
‣ PCI Device, Slot #x	Sub menu	Opens sub menu to configure slot x PCI device.
PCI IRQ line 1 PCI IRQ line 2 PCI IRQ line 3 PCI IRQ line 4 Onboard LAN IRQ line ** Onboard USB EHCI IRQ line **	Disabled **Auto Select** IRQ3, 4, 5, 7, 9, 10, 11, 12, 14,15	Select IRQs for external PIC interrupts A/B/C/D and the onboard Davicom LAN and USB2.0 host controller. Select Auto to let the BIOS assign the IRQ.
‣ PCI/PNP UMB Region Exclusion	Sub menu	Opens UMB Region Exclusion sub menu.
‣ PCI/PNP ISA IRQ Resource Exclusion	Sub menu	Opens IRQ Exclusion sub menu.
Default Primary Video Adapter	AGP **PCI**	In a system with an AGP and a PCI video adapter end user can select the adapter, which will be initialized by the BIOS.
Assign IRQ to SMB	No **Yes**	Determines whether the integrated SMBus host controller gets an IRQ assigned.

Notes: In the Option column, bold shows default settings.
(*) Setting this option to "yes", under certain circumstances, may help recovery from a system boot failure or a resource conflict.
(**) Not visible when corresponding device is disabled.

25.4.3. PCI Device, Slot #x Submenu

Feature	Option	Description
Option ROM Scan	Disabled **Enabled**	Initialize device expansion ROM.
Enable Master	**Disabled** Enabled	Enables device in slot as a PCI bus master, not every device can function as a master. Check device documentation.
Latency Timer	**Default**, 20h, 40h, 60h, 80h, A0h, C0h, E0h	Minimum guaranteed time slice allocated for bus master in units of PCI bus clocks. A high-priority, high-throughput device may benefit from a greater value.

Note: In the Option column, bold shows default settings.

25.4.4. PCI/PNP ISA UMB Region Exclusion Submenu

Feature	Option	Description
CC00 – CFFF	**Available** Reserved	Reserves the specified block of upper memory for use by legacy ISA devices.
D000 – D3FF	**Available** Reserved	See above.
D400 – D7FF	**Available** Reserved	See above.
D800 – DBFF	**Available** Reserved	See above.
DC00 - DFFF	**Available** Reserved	See above.

Notes: In the Option column, bold shows default settings.

25.4.5. PCI/PNP ISA IRQ Resource Exclusion Submenu

Feature	Option	Description
IRQ3	**Available** Reserved	Reserves the specified IRQ for use by legacy ISA devices.
IRQ4	**Available** Reserved	See above.
IRQ5	**Available** Reserved	See above.
IRQ7	**Available** Reserved	See above.
IRQ9 *	**Available** Reserved	See above.
IRQ10	**Available** Reserved	See above.
IRQ11	**Available** Reserved	See above.
IRQ12	**Available** Reserved	See above.
IRQ14 **	**Available** Reserved	See above.
IRQ15 **	**Available** Reserved	See above.

Notes: In the Option column, bold shows default settings.
(*) IRQ9 is used for SCI in ACPI mode. Do not use IRQ9 for legacy ISA devices when ACPI enabled.
(**) Entry is only visible when primary IDE or secondary IDE is disabled.

25.4.6. Memory Cache Submenu

Feature	Option	Description
Memory Cache	Disabled **Enabled**	Enables or Disables L2 cache.
Cache System BIOS area	Uncached **Write Protect**	Controls caching of System BIOS area.
Cache Video BIOS area	Uncached **Write Protect**	Controls caching of Video BIOS area.
Cache Base 0-512k	uncached Write Through Write Protect **Write Back**	Controls caching of 512k base memory.
Cache Base 512k-640k	uncached Write Through Write Protect **Write Back**	Controls caching of 512k to 640k base memory.
Cache Extended Memory area	Uncached Write Through Write Protected **Write Back**	Controls caching of system memory above 1MB.
D000 - D3FF D400 - D7FF D800 - DBFF DC00 - DFFF	**Disabled** Write Through Write Protected Write Back	Disabled: block is not cached. Write Through: Write are cached and sent to main memory at once. Write Protect: Writes are ignored. Write Back: Writes are cached but not sent to main memory until necessary.

Note: In the Option column, bold shows default settings.

25.4.7. I/O Device Configuration Submenu

Feature	Option	Description
Local Bus IDE adapter	Disabled Primary Secondary **Both**	Enables onboard PCI IDE device.
USB UHCI Host Controller 1	**Enabled** Disabled	Enable / Disable UHCI 1 Host Controller for USB port 1.
USB UHCI Host Controller 2	**Enabled** Disabled	Enable / Disable UHCI 2 Host Controller for USB port 2.
USB EHCI Host Controller **	**Enabled** Disabled	Controls USB 2.0 functionality.
Legacy USB Support ***	**Enabled** Disabled	Enable support for USB keyboard and mice and boot from USB mass storage devices.
AC97 Audio Controller	**Enabled** Disabled	Enable/Disable the AC97 Audio device.
Onboard LAN Controller	Disabled **Enabled**	Enables the ICH4 internal LAN controller.
Onboard LAN PXE ROM	**Disabled** Enabled	Enables the remote boot BIOS extension for the onboard LAN controller.
Floppy disk controller	Disabled **Enabled**	Enable / Disable the onboard FDC controller.
Serial port A, B	Disabled Enabled **Auto**	Disabled turns off the port. Enabled requires end user to enter the base I/O address and the IRQ. Auto makes the BIOS configure the port.
Base I/O address	3F8h, 2F8h, 3E8h, 2E8h	Select I/O base of port.
IRQ	IRQ 3, IRQ 4	Select IRQ of Port A and B
Parallel Port	Disabled Enabled **Auto**	Disabled turns off the port. Enabled requires end user to enter the base I/O address and the IRQ. Auto makes the BIOS configure the port.
Mode	Output only **Bi-directional** EPP ECP	Set the mode for the parallel port.
Base I/O address	**378h**, 278h	Select I/O base of port.
IRQ	IRQ 5, **IRQ 7**	Select IRQ of parallel port.
DMA	DMA1, **DMA3**	Select DMA channel of port if in ECP mode.

Notes: In the Option column, bold shows default settings.

(*) Only visible if an external I/O controller (SMSC669) is on the OEM backplane.

(**) The USB ports are multiplexed between UHCI and EHCI. Ports are routed to EHCI if an USB 2.0 high-speed device is connected and an EHCI driver is loaded.

(***) If you want to use the USB boot feature, enable USB BIOS Legacy Support. A 16kb UMB area (most likely DC000h-DFFFFh) is used for USB BIOS Legacy Support.

25.4.8. Keyboard Features Submenu

Feature	Option	Description
Numlock	Auto **On** Off	On or Off turns NumLock on or off at boot-up. Auto turns NumLock on if it finds a numeric key pad.
Key Click	**Disabled** Enabled	Turns audible key click on.
Keyboard auto-repeat rate	**30/sec**, 26.7/sec, 21.8/sec, 18,5/sec, 13.3/sec, 10/sec, 6/sec, 2/sec	Sets the number of times to repeat a keystroke per second if you hold the key down.
Keyboard auto-repeat delay	¼ sec, **½ sec**, ¾ sec, 1 sec	Sets the delay time after the key is held down before it begins to repeat the keystroke.

Note: In the Option column, bold shows default settings.

25.4.9. Hardware Monitor Submenu

This submenu shows the current voltages, temperatures and the fan speed of the system.

Voltage/Temperature/Fan	Explanation
VCC 3.3V Voltage	3.3V power plane
CPU Core Voltage	CPU core voltage
5Vsb Voltage	5V-Standby voltage
Battery Voltage	Battery voltage
CPU Temperature	CPU Temperature in ℃ and ℉
CPU Fan Speed	CPU fan speed in rpm, ”no Function” will be displayed on boards with passive cooling

25.4.10. Watchdog Timer Settings Submenu

Feature	Option	Description
Mode	**Disabled** Reset NMI	Select watchdog-timer operation mode.
Delay	1s, 5s, 10s, **30s**, 1min, 5.5min, 10.5min, 30.5min	The time until the watchdog timer counter starts counting. Useful to handle longer boot times.
Timeout	1s, 5s, 10s, **30s**, 1min, 5.5min, 10.5min, 30.5min	Max. trigger period.

Note: In the Option column, bold shows default settings.

25.4.11. Display Control Submenu

Feature	Option	Description
Display Mode	CRT only LFP only **CRT+LFP**	Select display mode.
JDA Revision	x.x	Displays the revision of the JILI data area image.
Flat Panel Type	VGA 1x18 * SVGA 1x18 * XGA 1x18 * XGA 1x24 * XGA 2x18 * SXGA 2x24 * UXGA 2x18 * Enter PAID Enter FPID **Auto**	Select Auto to let the BIOS automatically detect the panel type or use one of the predefined fixed panel types. Choose Enter PAID or Enter FPID to manually set JILI3 ID values.
PAID/FPID **	0 – FFFF, default **0**	Enter the JILI3 ID.
Flat Panel Scaling	Centered **Stretched**	Select scaling mode.
Flat Panel Backlight ***	0 – 255, default **128**	Enter a value to adjust backlight of the LCD.
Flat Panel Contrast ****	0 – 63, default **32**	Enter a value to adjust contrast of the LCD.

Note: In the Option column, bold shows default settings**.**

(*) Standard timings for VGA to SXGA panels cannot drive all available displays of that type that are on the market. Use a JILI cable whenever possible.

(**) Only visible if Enter PAID or Enter FPID are selected.

(***) Only visible if the panel adapter is equipped with a MAX5362 DAC for backlight control.

(****) Only visible if the panel adapter is equipped with a Xicore X9429 digital potentiometer for contrast control.

25.4.12. Miscellaneous Submenu

Feature	Option	Description
Floppy Check	**Disabled** Enabled	Enabled verifies floppy type on boot; disabled speeds boot.
Summary Screen	**Disabled** Enabled	If enabled, a summary screen is displayed just before booting the OS to let the end user see the system configuration.
QuickBoot Mode	Disabled **Enabled**	Allows the system to skip certain tests while booting. This decreases the time needed to boot the system.
Extended Memory Testing	Normal * **Just zero it** None	Determines which type of tests will be performed on memory above 1MB.
Dark Boot	**Disabled** Enabled	If enabled, system comes up with a blank screen instead of the diagnostic screen during boot-up.
Halt On Errors	**Yes** No	Determines if post errors cause the system to halt.
PS/2 Mouse	**Auto Detect** Enabled Disabled	Selecting Disabled prevents any installed PS/2 mouse from functioning but frees up IRQ12. Selecting Autodetect frees IRQ12 if no mouse is detected.
Large Disk Access Mode	**DOS** Other	Select DOS if you have DOS. Select Other if you have another OS such as UNIX. A large disk is one that has more than 1024 cylinders, more than 16 heads or more than 63 sectors per track.
Spread Spectrum	**Disabled** Enabled	Controls the spread spectrum feature of the clock generator.

Note: In the Option column, bold shows default settings**.**
(*) The option normal is not visible when QuickBoot is enabled.

Dark Boot

After you turn on or reset the computer, Dark Boot displays a graphical logo (default is a blank screen) instead of the text based POST screen, which displays a number of PC diagnostic messages.

The graphical logo stays up until just before the OS loads unless:

- You press <Esc> to display the POST screen
- You press <F2> to enter Setup
- POST issues an error message
- The BIOS or an option ROM requests keyboard input

25.5 *Security Menu*

Feature	Option	Description
Supervisor Password is	**Clear** Set	Displays whether password is set.
User Password is	**Clear** Set	Displays whether password is set.
Set Supervisor Password *	Up to seven alphanumeric characters	Pressing <Enter> displays the dialog box for entering the user password. In related systems, this password gives full access to setup.
Set User Password *	Up to seven alphanumeric characters	Pressing <Enter> displays the dialog box for entering the user password. In related systems, this password gives restricted access to setup.
Diskette access	User **Supervisor**	Enabled requires supervisor password to access floppy disk.
Fixed disk boot sector	**Normal** Write protected	Write protect the boot sector on the hard disk for virus protection. Requires a password to format or Fdisk the hard disk.
Virus check reminder	**Disabled** Daily Weekly Monthly	Displays a message during boot-up asking (Y/N) if you backed up the system or scanned for viruses. Message returns on each boot until you respond with Y. Daily displays the message on the first boot of the day, Weekly on the first boot after Sunday, and monthly on the first boot of the month.
System backup reminder	**Disabled** Daily Weekly Monthly	Displays a message during boot-up asking (Y/N) if you backed up the system or scanned for viruses. Message returns on each boot until you respond with Y. Daily displays the message on the first boot of the day, Weekly on the first boot after Sunday, and monthly on the first boot of the month.
Password on boot	**Disabled** Enabled	Enabled requires a password on boot. Requires prior setting of the supervisor password. If supervisor password is set and this option is disabled, BIOS assumes user is booting.

Notes: In the Option column, bold shows default settings.
(*) Enabling Supervisor Password requires a password for entering Setup. Passwords are not case sensitive.
User and Supervisor passwords are related. A User password is possible only if a Supervisor password exists.

25.6 *Power Menu*

A power management system reduces the amount of energy used after specified periods of inactivity. The setup menu supports:

- Full On State
- Standby State with Partial Power Reduction
- Suspend State with Full Power Reduction

Feature	Option	Description
*Enable ACPI	**No** Yes	*Enables/Disables ACPI BIOS (Advanced Configuration and Power Interface). IRQ9 is used for SCI (System Control Interrupt). Do not use for ISA bus devices.
ACPI Control	sub menu	Opens the ACPI sub menu
Max CPU frequency	****1800MHz** 1600MHz 1400MHz 1200MHz 1000MHz 800MHz 600MHz	Warning! Selecting frequencies higher then the default may cause the system to reach “critical trip point” and shutdown if a proper cooling solution is not used. Always ensure that you use proper cooling when selecting higher frequency settings.
***Automatic Thermal Monitor Control Circuit	Disabled TM1 **TM2**	Enables the thermal control circuit (TCC) of the thermal monitor feature of the Pentium-M CPU. TM1 = 50% duty cycle TM2 = Geyserville III **Automatic TTC must be enabled to ensure that the processor operates within specification.**
Power Savings	**Disabled** Customized Maximum Power Saving Maximum Performance	Maximum options select predefined values. Select Customized to make your own selections from the following fields. Disabled turns off all power management.
Standby Timeout	**Off**, 1min, 2min, 4min, 8min	Inactivity period required to put system in Standby mode (partial power shutdown).
Auto Suspend Timeout	**Off**, 5min, 10min, 15min, 20min, 30min, 40min, 60min	Inactivity period required after Standby to Suspend mode (maximum power shutdown).
Hard Disk Timeout	**Disabled**, 10 sec – 15 min	Inactivity period of hard disk required before standby (motor off).
Resume on Modem Ring	**Off** On	Enabled wakes the system on incoming calls detected by mode (RI).
Resume on Time	**Off** On	Enabled wakes the system at a specific time.
Resume Time	00:00:00	Specifies the time when the system is to wake.

Notes: In the Option column, bold indicates default setting.
* See section 13 of this user’s guide for more details about ACPI.
**The CPU frequency values shown in this example are taken from the speedMOPSlcdPM 1.8GHz. Please note that other speedMOPSlcdPM variants capable of CPU frequency switching may have different possible values listed as well as different defaults.
*** The speedMOPSlcdPM Celeron M default setting for this value is TM1 because the Celeron M does not support TM2.

25.6.1. ACPI Control Submenu

Feature	Option	Description
Active Trip Point	**Disabled** 40 C – 100 C	Determines the temperature of the ACPI Active Trip Point, the point at which the OS will turn on/off the CPU fan.
Passive Trip Point	**Disabled** 40 C – 100 C	Determines the temperature of the ACPI Passive Trip Point, the point at which the OS will turn on/off CPU clock throttling.
Passive TC1 Value	**1**, 2, 3, …15**,** 16	Determines the TC1 (temperature coefficient 1) value for the ACPI passive cooling formula. See section 13.6 for more details.
Passive TC2 Value	1, 2, 3, 4, **5**, …15**,** 16	Determines the TC2 (temperature coefficient 2) value for the ACPI passive cooling formula. See section 13.6 for more details.
Passive TSP Value	2, 4, 6, 8, **10**, … 28, 30	Determines the Tsp (sampling period) value for the ACPI passive cooling formula. See chapter 13.6 below for more details.
Critical Trip Point	40 C – **110 C**	This value controls the temperature of the ACPI Critical Trip Point- the point at which the OS will shut the system off.
APIC – IO APIC Mode	**Disabled** Enabled	This item is valid only for Windows XP. Also, a fresh install of the OS must occur when APIC Mode is desired Test the IO APIC by setting an item to Enabled. The APIC Table will then be pointed to by the RSDT, the Local APIC will be initialized, and the proper enable bits will be set in IHC4. See section 14.1
Native IDE Support	**Disabled** Enabled	Enable Native IDE support for WINXP by setting this item. The NATA Package will be created if this item is set to Enabled. Changing this item will have no effect in WIN98, WINME, or WIN2K. See section 13.2 for more details.

Notes: In the Option column, bold indicates default setting.

25.6.2. ACPI Resume Events

speedMOPSlcdPM supports S1 state only, no S3 (S2R) and S4 (S2D). The following events resume the system from S1:

- **PME#**
- **PS/2 keyboard and mouse**
- **USB keyboard and mouse activity**
- **USB resume event**

25.7 *Boot Menu and Utilities*

MultiBoot is a boot utility integrated in the PhoenixBIOS 4.0. The speedMOPSlcdPM provides the MultiBoot XP version with integrated Boot First function.

25.7.1. MultiBoot XP

MultiBoot XP comes with a complete new look of the Boot Device Priority submenu. This submenu is now separated into two sections:

- Boot Priority Order
- Excluded from Boot Order

It can display the setup menus by each kind of device type and arrange the boot priority order with any sequence of devices. MultiBoot XP meets the requirements of PC 98 and accommodates more devices that are bootable. It employs a boot scheme that is generic and flexible enough to boot from any current device. You can select your boot device in Setup, or you can choose a different device each time you boot by selecting your boot device in the Boot First function.

An available bootable device can be easily switched between the two sections by just highlighting the device and then pressing <X>. To change the order, select the device to change and press <-> to decrease or <+> to increase priority. You also can choose between four default configurations for the boot order <1>-<4>.

Boot Priority Order

This section shows eight configuration entries for up to eight devices that can be arranged in boot priority order (1: highest priority, 8: lowest priority).

Excluded from Boot Order

This section shows all devices that are excluded from the boot order. Any device listed here will never be used as boot device and not appear in the Boot First function.

The following table shows a list of supported devices:

Device	Description
IDE 0	Primary master IDE hard drive
IDE 1	Primary slave IDE hard drive
IDE 2	Secondary master IDE hard drive
IDE 3	Secondary slave IDE hard drive
IDE CD	IDE compatible CD-ROM drive
Legacy Floppy Drives	Standard Legacy Diskette Drive
USB KEY	USB stick
USB FDC	USB Diskette Drive
USB HDD	USB Hard Drive and memory sticks that follow MMS specification
USB CDROM	USB CD-ROM Drive
USB ZIP	USB ZIP Drive
USB LS120	USB LS120 Drive
PCI BEV	Ethernet Controller on the PCI Bus with LAN Boot ROM
PCI SCSI	SCSI Controller on the PCI Bus with SCSI BIOS ROM

25.7.2. Boot First Function

Display the Boot First function by pressing <Esc> during POST. In response, the BIOS displays the message Entering Boot Menu and then displays the Boot Menu at the end of POST. With the MultiBoot XP feature only devices detected during boot-up are displayed.

Use the menu to select a following option:

- Override the existing boot sequence (for this boot only) by selecting another boot device. If the specified device does not load the OS, the BIOS reverts to the previous boot sequence.
- Enter Setup.
- Press <Esc> to continue with the existing boot sequence.

25.8 *Exit Menu*

The following sections describe the five options in Exit Menu. Pressing <Esc> does not exit this menu. You must select an item from the menu to exit.

Feature	Option	Description
Exit Saving Changes	Saves selections and exits setup. The next time the system boots, the BIOS configures the system according to the Setup selection stored in CMOS.	Exit saving changes.
Exit Discarding Changes	Exits Setup without storing in CMOS any new selections you may have made. The selections previously in effect remain in effect.	Exit discarding changes.
Load Setup Defaults	Displays default values for all the Setup menus.	Load setup defaults.
Discard Changes	If, during a Setup session, you change your mind about changes you have made and have not yet saved the values to CMOS, you can restore the values you saved to CMOS.	Discard changes.
Save Changes	Saves all the selection without exiting Setup. You can return to the other menus to review and change your selection.	Save changes.

25.9 *Kontron BIOS Extensions*

Besides the Phoenix System BIOS, the speedMOPSlcdPM comes with a few BIOS extensions that support special features. All extensions are located in the onboard Flash EEPROM. Some extensions are permanently available; some are loaded if required during boot-up. Supported features include:

- JIDA standard
- Remote Control feature (JRC)
- Onboard LAN PXE ROM

All enabled BIOS extensions require shadow RAM, which is loaded into the same 32K shadowed memory block, if possible. However, if the system memory cannot find free memory space because all the memory is already used for add-on peripherals, the BIOS extensions do not load.

25.9.1. JIDA BIOS extension

The JUMPtec Intelligent Device Architecture (JIDA) BIOS extension is not a true extension BIOS. It is part of the system BIOS and is located in the system BIOS segments after boot-up. It is permanently available and supports the JIDA 16-bit and JIDA 32-bit standard.

The JIDA 16-bit standard is a software interrupt 15hex driven programmers interface and offers lots of board information functions. For detailed information about programming, refer to the JIDA specification and a source code example (JIDAI???.ZIP), which you can find at the Kontron Web site. The three question marks represent the revision number of the file. You also can contact technical support for this file.

For other operating systems, special 32-bit drivers (JIDAIA??.ZIP) are available. You can download the zip file from the Kontron Web site.

25.9.2. Remote Control Client Extension

You can remotely control the speedMOPSlcdPM using software available from Kontron (JRC-1, Part Number 96047-0000-00-0). This software tool can communicate with the board via one of the serial ports. During boot-up, the system BIOS scans the serial ports for an available JRC connection. If detected, it loads the JRC client BIOS extension into the memory. With the JRC client

loaded into the first detected free memory location between C0000hex and DFFFFhex, a 16K block is shadowed.

For more information on the Remote Control usage, refer to the JRC-1 technical manual or Application Note JRCUsage_E???.PDF, which you can find on the Kontron Web site.

25.9.3. LAN PXE ROM

If the onboard LAN PXE ROM is enabled in the system BIOS setup, a special optional ROM for the Ethernet controller loads into memory during boot-up. This optional ROM allows you to boot the speedMOPSlcdPM over an Ethernet connection. A server with Intel PXE boot support is required on the other side of the Ethernet connection. The setup and configuration of the server, including PXE support, is not the responsibility of Kontron.

The PXE ROM extension is loaded into the first free memory area between C0000hex and DFFFFhex and a 16K block of memory is shadowed.

25.10 Updating or Restoring BIOS Using PhoenixPhlash

PhoenixPhlash allows you to update the BIOS by using a floppy disk without having to install a new ROM chip. PhoenixPhlash is a utility used to flash a BIOS to the Flash ROM installed on the speedMOPSlcdPM.

Use PhoenixPhlash to:

- Update the current BIOS with a newer version
- Restore a corrupt BIOS

25.10.1. Flashing a BIOS

Use the following procedure to update or restore the BIOS.

1. Download the Phoenix Phlash compressed file, CRDxP815.ZIP, from the KONTRON Embedded Modules Web site or contact your local technical support for it. The zip file contains the following:

File	Purpose
MAKEBOOT.EXE	Creates the custom boot sector on the Crisis Recovery Diskette.
CRISBOOT.BIN	Serves as the Crisis Recovery boot sector code.
MINIDOS.SYS	Allows the system to boot in Crisis Recovery Mode.
PHLASH16.EXE	Programs the flash ROM.
WINCRIS.EXE	Creates the Crisis Recovery Diskette from Windows.
WINCRIS.HLP	Serves as the help file of WINCRISES.EXE.
CRISDISK.BAT	Batch file for crisis disk.
BIOS.WPH	Serves as the actual BIOS image to be programmed into Flash ROM.

2. Install Phoenix Phlash on a hard disk by unzipping the contents of the CRDxP815.ZIP into a local directory such as C:\PHLASH.

3. Create a Crisis Recovery Diskette by inserting a blank diskette into Drive A: or B: and execute WINCRISIS.EXE. This copies three files onto the diskette.

File	Purpose
MINIDOS.SYS	Allows the system to boot in Crisis Recovery Mode.
PHLASH16.EXE	Programs the flash ROM.

BIOS.ROM	Serves as the actual BIOS image to be programmed into Flash ROM.

4. If the BIOS image (BIOS.ROM) changes because of an update or bug fix, copy the new BIOS onto the diskette and name it BIOS.ROM.

   Phoenix Phlash runs in either command line mode or crisis recovery mode.

5. Use the command line mode to update or replace the BIOS. To execute Phlash in this mode, move to the Crisis Recovery Disk and type:

   ```
   PHLASH16 <bios name>    (Example: PHLASH16 PPM1R110.WPH)
   ```

   PhoenixPhlash will update the BIOS. PhoenixPhlash can fail if the system uses memory managers. If this occurs, the utility displays the following message:

   ```
   Cannot flash when memory manager are present.
   ```

   If you see this message after you execute Phlash, disable the memory manager or use parameter /x for Phlash16.exe.

   ```
   PHLASH16 /X <bios name>
   ```

25.10.2. Preventing Problems When Updating or Restoring BIOS

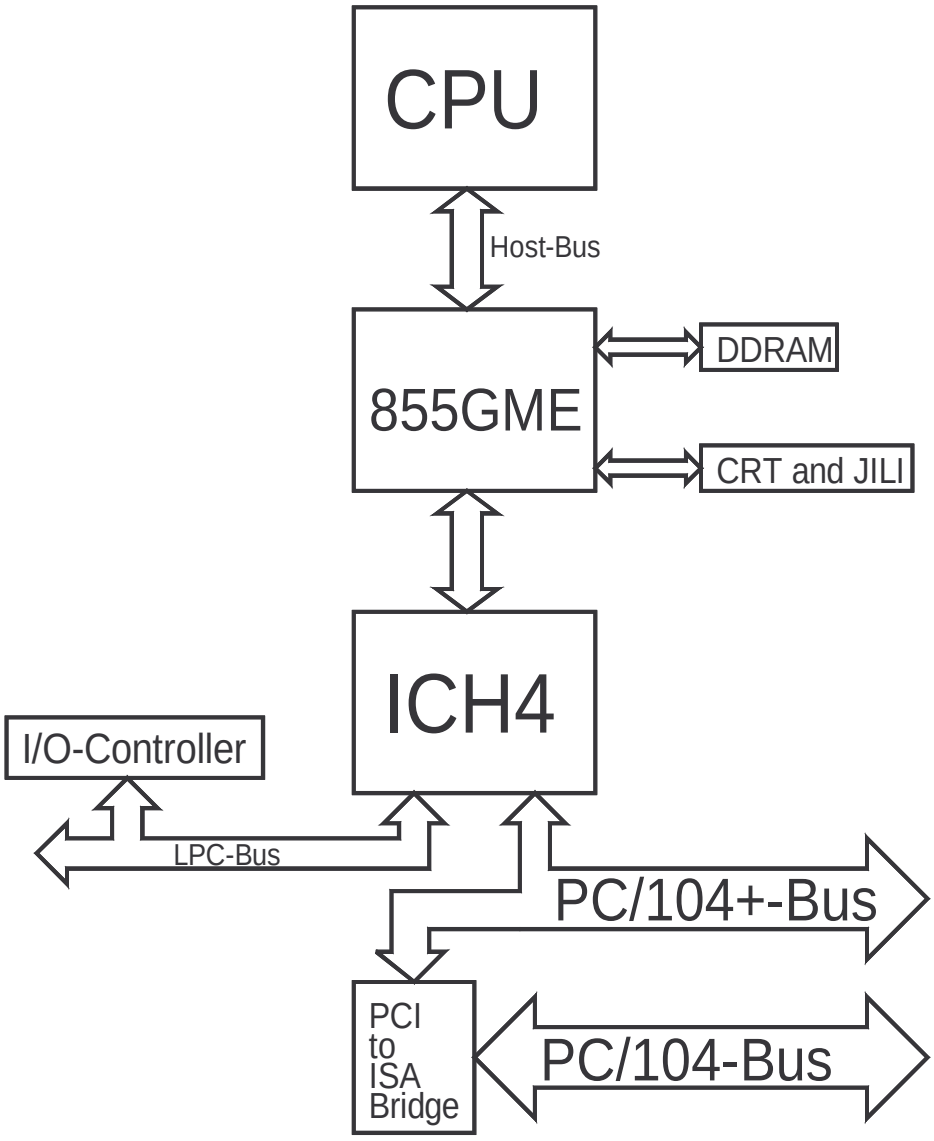
Updating the BIOS represents a potential hazard. Power failures or fluctuations can occur when you update the Flash ROM can damage the BIOS code, making the system unbootable.

To prevent this hazard, many systems come with a boot-block Flash ROM. The boot-block region contains a fail-safe recovery routine. If the boot-block code finds a corrupted BIOS (checksum fails), it boots into the crisis recovery mode and loads a BIOS image from a crisis diskette (see above).

Additionally, the end user can insert an update key into the parallel port (LPT) to force initiating the boot block recovery routine.

For further information on the update key and the crisis diskette, see the Application Note PHLASH_SCE???, which is available from the KONTRON Embedded Modules Web site. The three question marks stand for the revision number of the file.

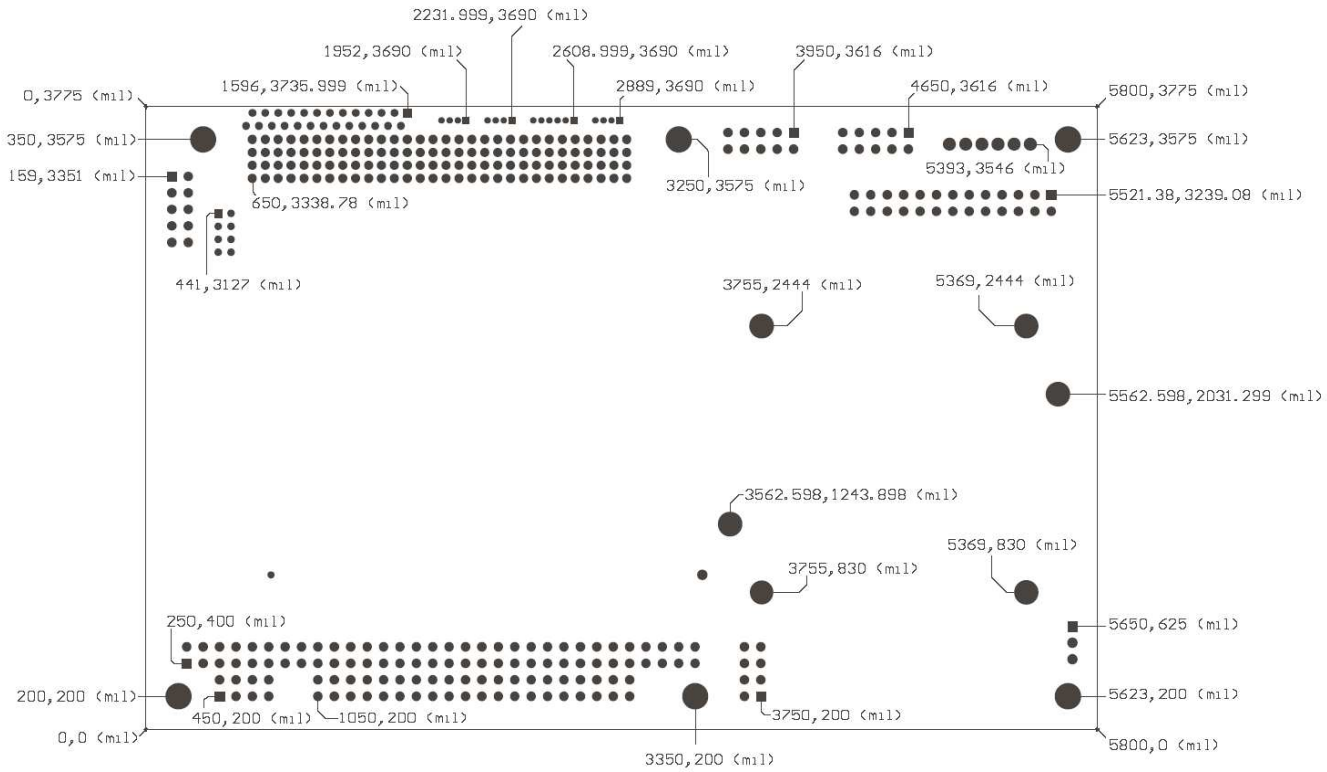
26. APPENDIX D: BLOCK DIAGRAM



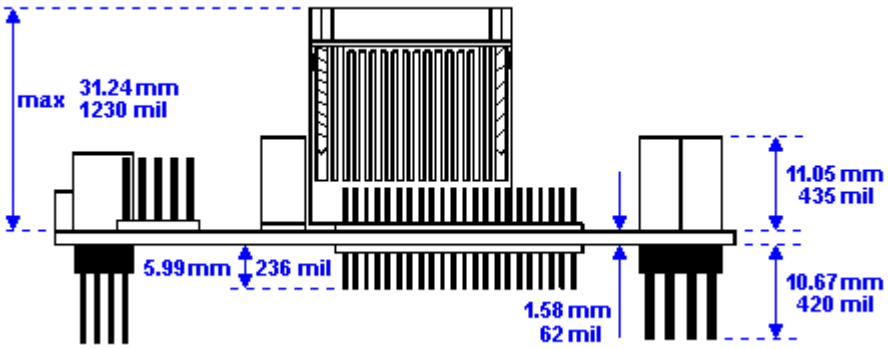
27. APPENDIX E: MECHANICAL DIMENSIONS

27.1 *Board Dimensions and Mounting Holes*

27.1.1. Top View

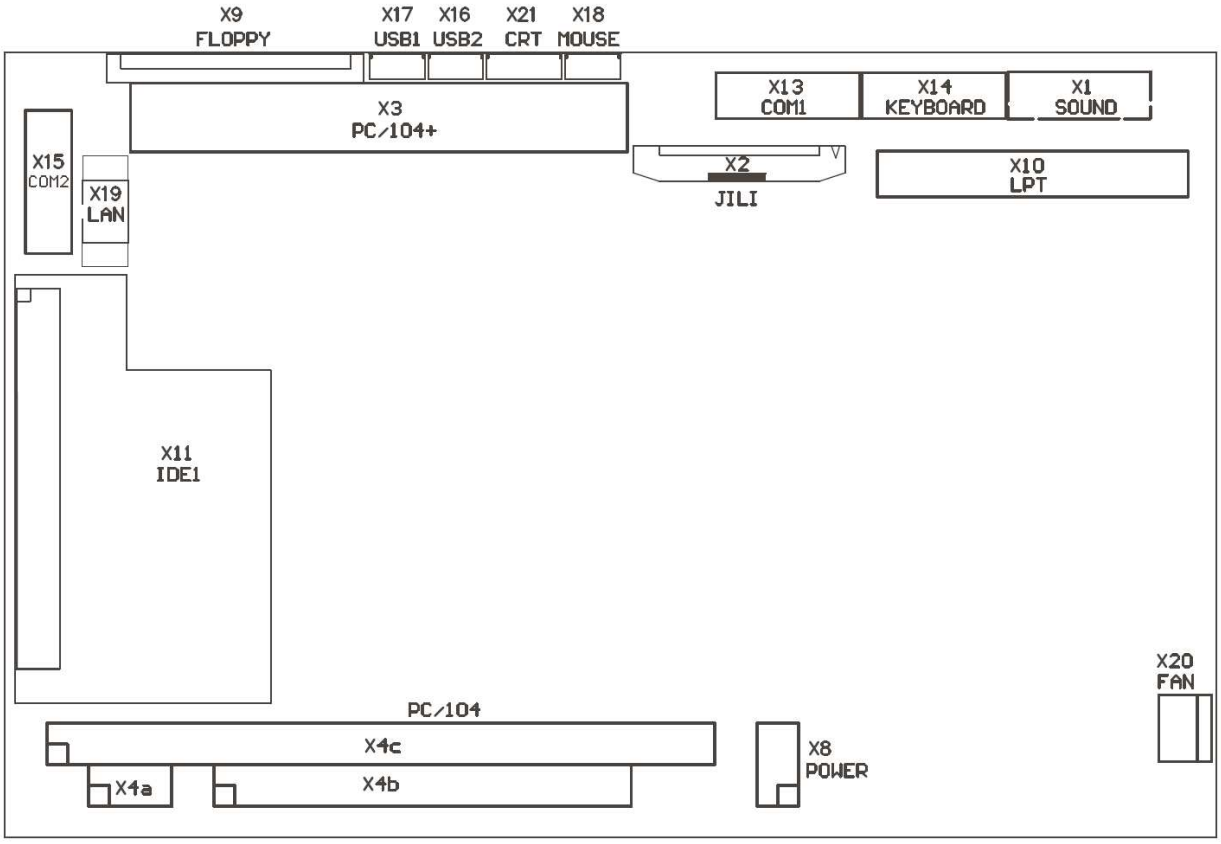


27.1.2. Side View



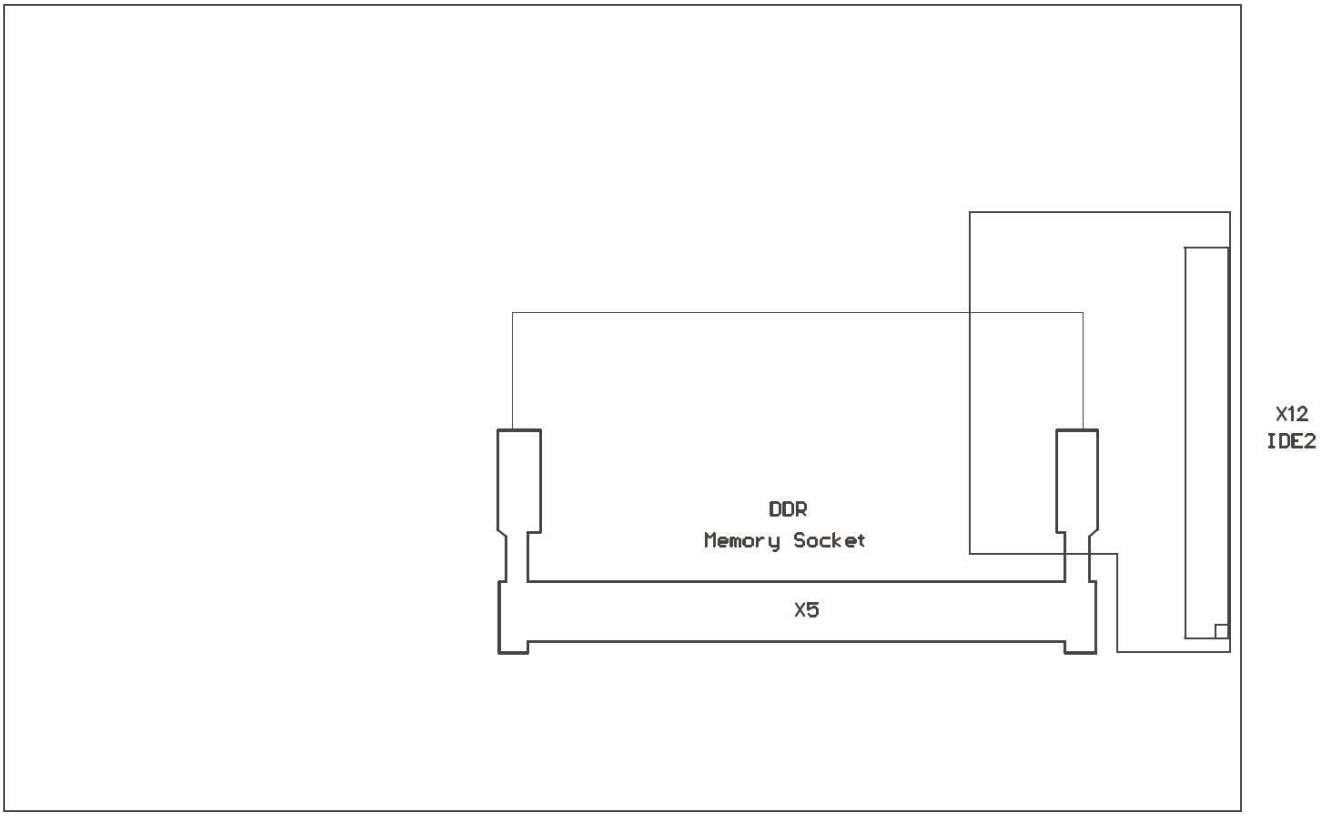
28. APPENDIX F: CONNECTOR LAYOUT

28.1 *Top Side*



Notes: The position of Pin 1 is marked with a quadratic pad on the PCB.

28.2 Bottom Side



28.3 Connector Functions and Interface Cables

The table notes connector functions, as well as mating connectors and available cables.

Connector	Function	Mating Connector	Available Cable	Cable Description
X2	Flat-panel display Connector	-	KAB-JILI-?????	Kontron JILI cables.
X21	CRT Monitor Connector	1.25mm 6 pos. (Molex 51021-0600 or compatible)	KAB-VGA-2 (PN 96053-0000-00-0)	For DSUB 15 adaptation.
X20	Fan Connector	1.25mm 3 pos. (Molex 51021-0300 or compatible)		
X19	Ethernet Interface Connector	2mm 8 pos. (Berg 90311-008 or compatible)	KAB-MOPS-ETN1 (PN 96048-0000-00-0)	For RJ45 adaptation.
X4A, X8	Power Connector	2.54mm 10 pos. (AMP 1-215882-0 or compatible)		
X4B	PC/104 Bus (AT-bus part)	2.54mm 40 pos. (EPT 962-60203-12 or compatible for board to board connection)		
X4C	PC/104 Bus (XT-bus part)	2.54mm 64 pos. (EPT 962-60323-12 or compatible for board to board connection)		
X3	PC/104-Plus Bus (PCI part)	2mm 120pos. (EPT 264-60303-12)		
X18	PS/2 Mouse Connector	1.25mm 4 pos. (Molex 51021-0400 or compatible)	KAB-MOUSE-PS2 (PN 96062-0000-00-0)	For PS/2 mouse.
X14	Keyboard and Feature Connector	2.54mm 10 pos. (AMP 1-215882-0 or compatible)	KAB-KB-1 (PN 96023-0000-00-0) or KAB-KB-PS2 (PN 96060-0000-00-0)	For AT-keyboard or PS/2 keyboard.
X13, X15	Serial Interfaces COM A and COM B Connectors	2.54mm 10 pos. (AMP 1-215882-0 or compatible)	KAB-DSUB9-2 (PN 96017-0000-00-0)	For DSUB 9 adaptation.
X11,X12	IDE Hard Disk Connector	2mm 44 pos. (Berg 89361-144 or compatible)	KAB-IDE-25 (PN 96020-0000-00-0) or KAB-IDE-2MM (PN 96021-0000-00-0)	For 3.5” HDD Or 2.5” HDD.
X16, X17	USB interface Connectors	1.25mm 4 pos. (Molex 51021-0400 or compatible)	KAB-USB-1 (PN 96054-0000-00-0)	For standard USB adaptation.
X9	Floppy Drive Connector		ADA-FLOPPY-2 (PN 96001-0000-00-0) or KAB-FLOPPY/MOPS-1 (PN 96019-0000-00-0)	For 3.5” floppy or slim-line floppy.
X1	Sound Connector	2.54mm 6 pos. (JST XHP-6 with crimp contacts JST SXH-001T-PO.6 Or JST SXH-002T-PO.6)	KAB-SOUND-CMP (PN96063-0000-00-0)	Cable with open ends

Connector	Function	Mating Connector	Available Cable	Cable Description
X10	LPT Connector	2.54mm 26 pos. (AMP 2-215882-6 or compatible)	KAB-DSUB25-1 (PN 96015-0000-00-0)	For DSUB 25 adaptation.

28.4 Pin-out Table

Pin	PC104-XT Bus (A) X4C	PC104-XT Bus (B) X4C	PC104-AT Bus (C) X4B	PC104-AT Bus (D) X4B
0			GND	GND
1	/IOCHCK	GND	/SBHE	/MEMCS16
2	SD7	RESETDRV	LA23	/IOCS16
3	SD6	VCC (***)	LA22	IRQ10
4	SD5	IRQ9	LA21	IRQ11
5	SD4	-5V	LA20	IRQ12
6	SD3	DRQ2	LA19	IRQ15
7	SD2	-12V	LA18	IRQ14
8	SD1	/0WS	LA17	/DACK0
9	SD0	+12V	/MEMR	DRQ0
10	IOCHRDY	GND (*)	/MEMW	/DACK5
11	AEN	/SMEMW	SD8	DRQ5
12	SA19	/SMEMR	SD9	/DACK6
13	SA18	/IOW	SD10	DRQ6
14	SA17	/IOR	SD11	/DACK7
15	SA16	/DACK3	SD12	DRQ7
16	SA15	DRQ3	SD13	VCC (***)
17	SA14	/DACK1	SD14	/MASTER
18	SA13	DRQ1	SD15	GND
19	SA12	/REFRESH	GND	GND
20	SA11	SYSCLK		
21	SA10	IRQ7		
22	SA9	IRQ6		
23	SA8	IRQ5		
24	SA7	IRQ4		
25	SA6	IRQ3		
26	SA5	/DACK2		
27	SA4	T/C		
28	SA3	BALE		
29	SA2	VCC (***)		
30	SA1	OSC		
31	SA0	GND		
32	GND	GND		

Notes: (*) Key pin for PC/104; GND for PC/104+ specification
(***) To protect the external power lines of peripheral devices, make sure that:
- the wires have the right diameter to withstand the maximum available current
- the enclosure of the peripheral device fulfils the fire protecting requirements of
- IEC/EN 60950.

Pin	PC104+ Bus (A) X3	PC104+ Bus (B) X3	PC104+ Bus (C) X3	PC104+ Bus (D) X3
1	GND	Reserved	VCC (***)	AD00
2	VCC (***)	AD02	AD01	AD03
3	AD05	GND	AD04	AD03
4	C/BE0	AD07	GND	AD06
5	GND	AD09	AD08	GND
6	AD11	VCC (***)	AD10	GND
7	AD14	AD13	GND	AD12
8	VCC3 (**)	C/BE1	AD15	VCC3 (**)
9	SERR	GND	SB0	PAR
10	GND	PERR	VCC3 (**)	SDONE
11	STOP	VCC3 (**)	LOCK	GND
12	VCC3 (**)	TRDY	GND	DEVSEL
13	FRAME	GND	IRDY	VCC3 (**)
14	GND	AD16	VCC3 (**)	C/BE2
15	AD18	VCC3 (**)	AD17	GND
16	AD21	AD20	GND	AD19
17	VCC3(**)	AD23	AD22	VCC3 (**)
18	IS0 (AD20)	GND	IS1 (AD21)	IS2 (AD22)
19	AD24	C/BE3	VI/O	IS3 (AD23)
20	GND	AD26	AD25	GND
21	AD29	VCC (***)	AD28	AD27
22	VCC (***)	AD30	GND	AD31
23	REQ0	GND	REQ1	VI/O
24	GND	REQ2	VCC (***)	GNT0
25	GNT1	VI/O	GNT2	GND
26	VCC (***)	CLK0	GND	CLK1
27	CLK2	VCC (***)	CLK3	GND
28	GND	INTD	VCC (***)	RST
29	+12V	INTA	INTB	INTC
30	-12V	Reserved	Reserved	Reserved

Notes: (**) Not generated onboard of the speedMOPSlcdPM

(***) To protect the external power lines of peripheral devices, make sure that:
- the wires have the right diameter to withstand the maximum available current
- the enclosure of the peripheral device fulfils the fire protecting requirements of
- IEC/EN 60950.

Pin	IDE X11 X12	Floppy X9	LPT X10	Power X4A	Sound X1	COM A X15	COM B X13
1	/RESET	VCC (***)	/STB	GND	Right	/DCD1	/DCD2
2	GND	/IDX	/AFD	VCC (***)	ASGND	/DSR1	/DSR2
3	HDD7	VCC (***)	PD0	BATT	Left	RXD1	RXD2
4	HDD8	/DR0	/ERR	+12V (***)	AUXAR_C	/RTS1	/RTS2
5	HDD6	VCC (***)	PD1	-5V (***)	MIC_C	TXD1	TXD2
6	HDD9	/DSKCHG	/INIT	-12V (***)	AUXAL_C	/CTS1	/CTS2
7	HDD5	NC	PD2	GND		/DTR1	/DTR2
8	HDD10	NC	/SLIN	VCC (***)		/RI1	/RI2
9	HDD4	NC	PD3			GND	GND
10	HDD11	/MTR0	GND			VCC (***)	VCC (***)
11	HDD3	NC	PD4				
12	HDD12	/FDIR	GND				
13	HDD2	NC	PD5				
14	HDD13	/STEP	GND				
15	HDD1	GND	PD6				
16	HDD14	/WDATA	GND				
17	HDD0	GND	PD7				
18	HDD15	/WGATE	GND				
19	GND	GND	/ACK				
20	KEY (NC)	/TRK0	GND				
21	DRQ	GND	BUSY				
22	GND	/WRTPRT	GND				
23	/IOW	GND	PE				
24	GND	/RDATA	GND				
25	/IOR	GND	SLCT				
26	GND	/HDSEL	VCC (***)				
27	IOCHRDY						
28	CSEL						
29	/AKJ						
30	GND						
31	SIRQ						
32	NC						
33	SA1						
34	NC						
35	SA0						
36	SA2						
37	/CS1						
38	/CS3						
39	NC						
40	GND						
41	VCC (***)						
42	VCC (***)						
43	GND						
44	NC						

Notes: (***) To protect the external power lines of peripheral devices, make sure that:
- the wires have the right diameter to withstand the maximum available current
- the enclosure of the peripheral device fulfils the fire protecting requirements of
- IEC/EN 60950.

Pin	KBD X14	Eth 1 X19	CRT X21	PS/2 Mouse X18	USB X16 X17	Aux. Power X8	Fan X20
1	SPEAKER	TXD+	RED	MSDAT	VCC (***)	GND	Sense
2	GND	TXD-	GRN	VCC (***)	USB0	VCC (***)	VCC (***)
3	/RESIN	RXD+	BLU	GND	USB1	VCC (***)	GND
4	/KBLOCK	SHLDGND	GND	MSCLK	GND	GND	
5	KBDAT	SHLDGND	VSYNC			GND	
6	KBCLK	RXD-	HSYNC			VCC (***)	
7	GND	SHLDGND				VCC (***)	
8	VCC (***)	SHLDGND				GND	
9	BATT						
10	PWRGOOD						

Notes: (***) To protect the external power lines of peripheral devices, make sure that:
- the wires have the right diameter to withstand the maximum available current
- the enclosure of the peripheral device fulfils the fire protecting requirements of
- IEC/EN 60950.

29. APPENDIX G: PC ARCHITECTURE INFORMATION

The following sources of information can help you better understand PC architecture.

29.1 *Buses*

29.1.1. ISA, Standard PS/2 - Connectors

- AT Bus Design: Eight and Sixteen-Bit ISA, E-ISA and EISA Design, Edward Solari, Annabooks, 1990, ISBN 0-929392-08-6
- AT IBM Technical Reference Vol 1&2, 1985
- ISA & EISA Theory and Operation, Edward Solari, Annabooks, 1992, ISBN 0929392159
- ISA Bus Specifications and Application Notes, Jan. 30, 1990, Intel
- ISA System Architecture, Third Edition, Tom Shanley and Don Anderson, Addison-Wesley Publishing Company, 1995, ISBN 0-201-40996-8
- Personal Computer Bus Standard P996, Draft D2.00, Jan. 18, 1990, IEEE Inc
- Technical Reference Guide, Extended Industry Standard Architecture Expansion Bus, Compaq 1989

29.1.2. PC/104, PCI

- Embedded PC 104 Consortium
  The consortium provides information about PC/104 and PC/104-Plus technology. You can search for information about the consortium on the Web.
- PCI SIG
  The PCI-SIG provides a forum for its ~900 member companies, who develop PCI products based on the specifications that are created by the PCI-SIG. You can search for information about the SIG on the Web.

- PCI & PCI-X Hardware and Software Architecture & Design, Fifth Edition, Edward Solari and George Willse, Annabooks, 2001, ISBN 0-929392-63-9.
- PCI System Architecture, Tom Shanley and Don Anderson, Addison-Wesley, 2000, ISBN 0-201-30974-2.

29.2 General PC Architecture

- Embedded PCs, Markt&Technik GmbH, ISBN 3-8272-5314-4 (German)
- Hardware Bible, Winn L. Rosch, SAMS, 1997, 0-672-30954-8
- Interfacing to the IBM Personal Computer, Second Edition, Lewis C. Eggebrecht, SAMS, 1990, ISBN 0-672-22722-3
- The Indispensable PC Hardware Book, Hans-Peter Messmer, Addison-Wesley, 1994, ISBN 0-201-62424-9
- The PC Handbook: For Engineers, Programmers, and Other Serious PC Users, John P. Choisser and John O. Foster, Annabooks, 1997, ISBN 0-929392-36-1

29.3 Ports

29.3.1. RS-232 Serial

- EIA-232-E standard
  The EIA-232-E standard specifies the interface between (for example) a modem and a computer so that they can exchange data. The computer can then send data to the modem, which then sends the data over a telephone line. The data that the modem receives from the telephone line can then be sent to the computer. You can search for information about the standard on the Web.
- RS-232 Made Easy: Connecting Computers, Printers, Terminals, and Modems, Martin D. Seyer, Prentice Hall, 1991, ISBN 0-13-749854-3
- National Semiconductor
  The Interface Data Book includes application notes. Type “232” as a search criteria to obtain a list of application notes. You can search for information about the data book on National Semiconductor’s Web site.

29.3.2. ATA

AT Attachment (ATA) Working Group
This X3T10 standard defines an integrated bus interface between disk drives and host processors. It provides a common point of attachment for systems manufacturers and the system. You can search for information about the working group on the Web.
We recommend you also search the Web for information on *4.2 I/O cable*, if you use hard disks in a DMA3 or PIO4 mode.

29.3.3. USB

USB Specification
USB Implementers Forum, Inc. is a non-profit corporation founded by the group of companies that developed the Universal Serial Bus specification. The USB-IF was formed to provide a support organization and forum for the advancement and adoption of Universal Serial Bus technology. You can search for information about the standard on the Web.

29.4 *Programming*

- C Programmer's Guide to Serial Communications, Second Edition, Joe Campbell, SAMS, 1987, ISBN 0-672-22584-0
- Programmer's Guide to the EGA, VGA, and Super VGA Cards, Third Edition, Richard Ferraro, Addison-Wesley, 1990, ISBN 0-201-57025-4
- The Programmer's PC Sourcebook, Second Edition, Thom Hogan, Microsoft Press, 1991, ISBN 1-55615-321-X
- Undocumented PC, A Programmer's Guide to I/O, CPUs, and Fixed Memory Areas, Frank van Gilluwe, Second Edition, Addison-Wesley, 1997, ISBN 0-201-47950-8

30. APPENDIX H: DOCUMENT REVISION HISTORY

Version	Date	Edited by	Changes
PPM1M090	05.12.2005	KFR	Created preliminary manual