

TEKNOR
INDUSTRIAL COMPUTERS INC.

TEK-CPCI 1003

CompactPCI Mobile PENTIUM II SBC

TECHNICAL REFERENCE MANUAL **VERSION 1.1b**
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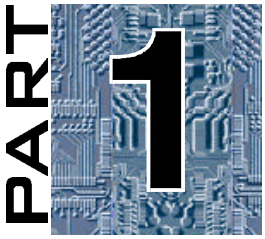
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PRODUCT DESCRIPTION

1. PRODUCT OVERVIEW

2. COMPATIBILITY WITH TEKNOR PRODUCTS

3. UNPACKING

4. SAFETY PRECAUTIONS

5. ONBOARD CONNECTIVITY

6. MEZZANINE CONCEPTS

1. PRODUCT OVERVIEW

The TEK-CPCI-1003 is the first CompactPCI™ industrial SBC based on the Intel's Pentium® II processor in a 'mini-cartridge' package (Mobile Pentium® II).

The board supports 233MHz, 266MHz, 300MHz, and future processors, 512KB L2 pipelined burst cache and Intel's 82443BX and 82371AB PIIX4E chipset. It features J3/J4/J5 de-facto industry standard connectors to handle I/O signals such as serial, parallel, and USB ports, Ethernet, video and V-Port, SCSI, and IDE interfaces, keyboard, speaker, mouse, and reset signals, SMBus and power.

The TEK-CPCI-1003 can be purchased either for front plate I/O interfacing (video, serial ports, Ethernet ports) or rear panel I/O interfacing (no interconnection capability available on the front plate) through CPCI I/O connectors.

The front plate may be adapted (optional) to support standard mouse, keyboard and floppy connections when adding a mezzanine board to the SBC or a PMC card.

The board is intended to provide the highest level of performance and throughput for the 32/64-bit CompactPCI™ operating environments. The rugged design of the TEK-CPCI-1003, as well as its very rich feature-set, makes it an outstanding choice for numerous high-availability applications ranging from telecommunication to computer intensive industrial and mission-critical medical applications.

The TEK-CPCI-1003 board is fully compatible with existing application software and operating systems available for desktop PCs: PC and MS-DOS®, Windows® 3.1, Windows® 95, Windows® NT, OS/2® Warp, QNX™, NOVELL™, UnixWare™.

- **Supported Processors**

  Single 233MHz, 266MHz, or 300MHz Mobile Pentium II processor with Intel's 82443BX and 82371AB PIIX4 chipset.

- **Memory**

  System memory: The TEK-CPCI-1003 supports from 8MB to 384MB vertical SDRAM on three 168-pin DIMMs sockets with ECC capabilities. Registered SDRAM (RSDRAM) is also supported for up to 768MB of system memory.

  Internal cache: 32KB (L1), 512KB (L2) pipelined burst cache is implemented to enhance the processor operations by eliminating wait states on cache accesses.

- **CompactPCI Connectors**

  Rear panel CPCI connectors are PICMG 2.0 R2.1 CompactPCI™ specification compliant. CompactPCI connectors are located at the rear edge of the board. The complete CPCI connector configuration is composed of five connectors referred to as J1, J2, J3, J4, and J5. They are defined as 2mm pitch, shielded connectors with a 5x47 array of pin for signals and 2 rows of 47 pins for shielding.

  Their function is described below:

  J1/J2: carry out arbitration and PCI bus signals, and power.

  J3/J4/J5: handle I/O signals.

▪ Interfacing with the Environment

CPCI The TEK-CPCI-1003 SBC is provided for rack-mounted systems. Through the J1/J2 segment, the board can drive up to seven external CompactPCI slots, supporting individual REQ/GNT arbitration signals and individual clocks.

All I/O signals are duplicated and available through the J3/J4/J5 I/O segment to be distributed to their respective I/O connectors located on the backplane.

When connecting the board to a backplane, ensure the backplane is capable of supporting these signals. It must also make them available on individual local headers.

A backplane dedicated to the TEK-CPCI-1003 is provided by TEKNOR, and is referred to as TEK-CPCI 1103 CPCI Passive Backplane.

Mezzanine The mezzanine is a new hardware concept introduced by TEKNOR to increase the I/O connectivity of the TEK-CPCI-1003, but respecting the dual slot 8U form factor restrictions.

PCI bus, IDE floppy, keyboard and mouse signals are provided on two connectors to support mezzanine applications: optional storage devices (HD and FD), CD-ROM device or PCI-to-PCI bridge can easily be added to the system without any loss of I/O slot on the backplane.

Some mezzanine from TEKNOR feature PS/2 standard mouse and keyboard plugs for direct connection on the face plate (TEK-CPCI-1050 and 1051 storage mezzanines).

2. COMPATIBILITY WITH TEKNOR PRODUCTS

The TEK-CPCI-1003 CPU Single Board Computer is a member of the TEKNOR CompactPCI product family. The board is fully compliant with the PICMG 2.0 R2.1 CompactPCI specification for the PCI bus segment.

When building a basic environment around the TEK-CPCI-1003, the system may be composed with any of the following devices:

- **TEK-CPCI-1003**: 6U system board
- **TEK-CPCI-1103**: 8 slots - CompactPCI backplane
- **TEK-CPCI-1106**: 16 slots - CompactPCI backplane
- **TEK-CPCI 1050**: HD, FD, keyboard, and mouse mezzanine
- **TEK-CPCI 1051**: HD, FD, keyboard, mouse, and PCI-to-PCI bridge mezzanine
- **TEK-CPCI 1070**: 6Ux8HPx100mm - Rear I/O interface module
- **TEK-CPCI 1071**: 6Ux8HPx80mm - Rear I/O interface module
- **TEK-CPCI 1080**: 6Ux8HP – HD and CD-ROM CompactPCI unit
- 3U and 6U CompactPCI devices
- 6U form factor enclosure
- ATX Power Supply
- Hot-swap, load-sharing power supply unit

A CompactPCI Development Platform is available from TEKNOR and is referred to as TEK-CPCI-1203.

3. UNPACKING

Follow these recommendations while unpacking:

1. After opening the box, save it and the packing material for possible future shipment.
2. Remove the board from its antistatic wrapping and place it on a grounded surface.
3. Inspect the board for damage. If there is any damage, or items are missing, notify TEKNOR immediately.

Contents

When unpacking you will find:

1. One TEK-CPCI-1003, Mobile Pentium II Single Board Computer
2. One Quick Reference sheet
3. Diskettes

4. SAFETY PRECAUTIONS

4.1 STATIC ELECTRICITY

Since static electricity can damage the board, the following precautions should be taken:

1. Keep the board in its antistatic package, until you are ready to install it.
2. Touch a grounded surface or wear a grounding wrist strap before removing the board from its package; this will discharge any static electricity that may have built up in your body.
3. Handle the board by the edges.

4.2 STORAGE ENVIRONMENT

Electronic boards are sensitive devices. Do not handle or store devices near strong electrostatic, electromagnetic, magnetic or radioactive fields.

4.3 POWER SUPPLY

Before any installation or setup, ensure that the board is unplugged from power sources or subsystems.

5. ONBOARD INTERCONNECTIVITY

The TEK-CPCI-1003 is not only a matter of computation power. The board also provides a high capability to interface with peripherals through three integrated chipsets:

. Host-to-PCI bridge - 443BX from Intel: interface with the processor (host), system memory, video controller, and Primary PCI bus (3.3V / 33MHz).

. PCI-to-PCI bridge - 21150 from DEC: manage the PCI bus signals on J1 and J2 CPCI connectors. When used with a CompactPCI backplane, the board can drive directly up to seven CPCI slots in PCI bus Master configuration.

. PCI-to-ISA bridge - 82371AB PIIX4 from Intel: interface the ISA bus to the Primary PCI bus.

■ Mobile Pentium® II processor

The TEK-CPCI-1003 system board supports 233MHz, 266MHz, and 300MHz Mobile Pentium® II processors from Intel, which is the first implementation of the Pentium II processor family optimized for the mobile platform.

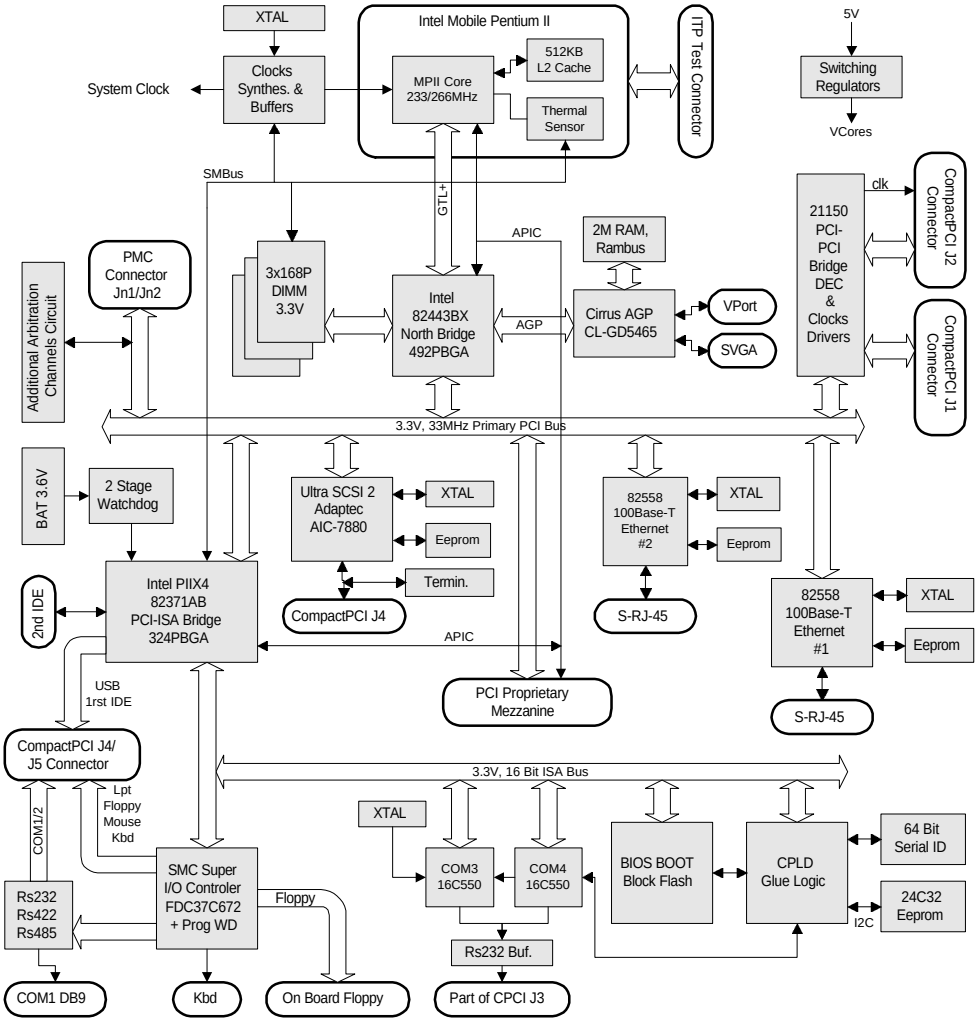
It consists of a mobile Pentium® II processor core with an integrated second level cache and a 64-bit high performance host bus (66MHz bus speed).

The processor interfaces to the 82443BX PCIset through the 64-bit low power GTL+ data bus interface.

■ 443BX PCIset

The 443BX integrates a 32-bit PCI bus arbiter, and is optimized for 66MHz, 64/72-bit SDRAM memory control and data path. It also features the Accelerated Graphics Port (AGP) interface with up to 133MHz data transfer capability for data transfers with the video chip.

TEK-CPCI-1003 Block Diagram



■ 21150 PCI-to-PCI Bridge

The 21150 is a 32/32-bit 33MHz PCI-to-PCI bridge that allows the board to support up to seven loads on its secondary PCI bus through a passive backplane. The bridge is fully compliant the PCI Local Bus Specification, Rev. 2.1. It provides full support for delayed transactions, which enables the buffering of memory read, I/O and configuration transactions. The 21150 have separate posted write, read data and delayed transaction queues with a high buffering capability.

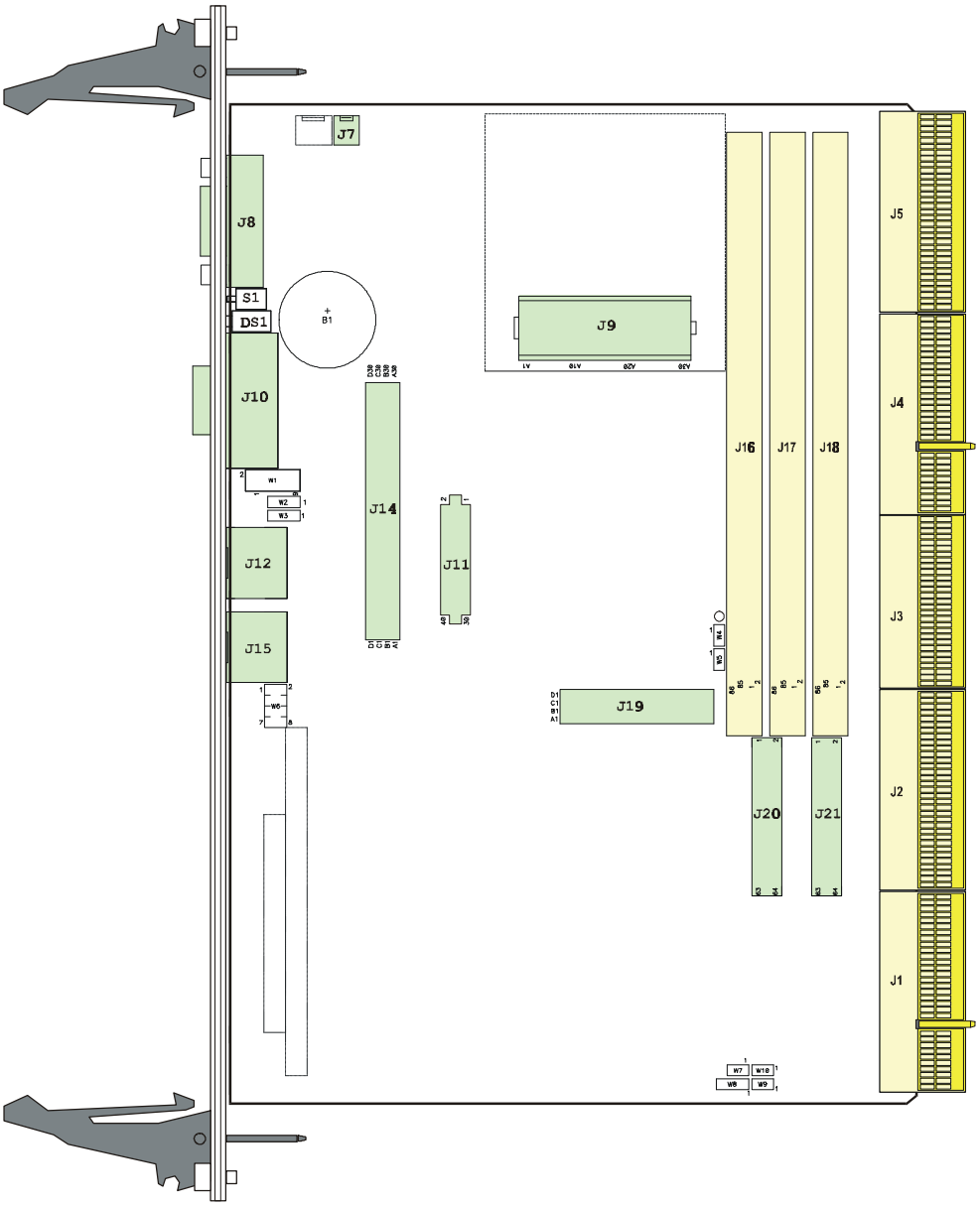
In addition, it supports buffering of simultaneous multiple posted writes and delayed transactions in both directions.

The PCI-to-PCI bridge allows the Primary and Secondary PCI buses to operate concurrently. This means that a master and a target on the same PCI bus can communicate while the other PCI bus is busy. This traffic isolation may increase system performance in applications such as multimedia.

■ 82371AB PCI-to-ISA Bridge / IDE Xcelerator (PIIX4)

The PCI-to-ISA bridge is configured to support signals to directly drive IDE interfaces, USB ports, extra communication ports (Serial Ports 3 and 4), and standard Serial Ports (1 and 2), floppy disk drives, mouse and keyboard through a super I/O controller (FDC37C672).

5.1 CONNECTOR LOCATION



5.2 ONBOARD CONNECTORS AND HEADERS

- **Fan Header (J7)**

  The +12V DC CPU fan power supply is provided through this header.

- **Processor Socket (J9)**

  Mobile Pentium II processor dedicated connector.

- **CompactFlash Connector (J11)**

  This connector is dedicated to the TEKNOR's CompactFlash module to support CompactFlash disks.

- **PCI Mezzanine Connector (J14)**

  This connector handles PCI bus signals to the mezzanine.

- **DIMM Sockets (J16/J17/J18)**

  Three 168-pin DIMM sockets

- **Storage Mezzanine connector (J19)**

  This connector is implemented to support floppy/hard disk, keyboard, and mouse signals.

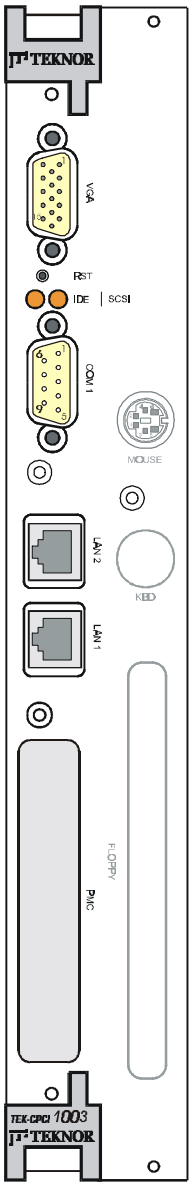
- **PMC Connectors (J20/J21)**

  The PCI Mezzanine Card (PMC) connectors support one standard PMC device.

- **Battery Connector (B1)**

  CMOS backup battery connector.

5.3 FRONT PLATE CONNECTORS



- **Video Connector (J8)**

  Standard 15-pin DSUB female connectors.

- **Reset Button**

  Use a small tool to press the button and proceed to a hardware reset of the board.

- **IDE/SCSI LEDs**

  When lit indicate there is an activity on IDE/SCSI devices.

- **Com Port 1 (J10)**

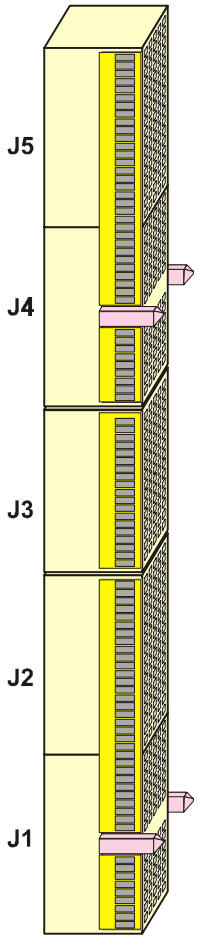
  Standard 9-pin DSUB male connectors.

- **Ethernet Connectors (J12/J15)**

  RJ-45 connectors with built-in activity and link indicators.

The front plate supports a PMC cutout and a cap that also acts as an EMI shield when there is no PMC device installed. An optional front plate with mouse, keyboard, and floppy disk cutouts is available from TEKNOR to support a mezzanine board featuring these functions.

5.4 COMPACTPCI CONNECTORS



- **CPCI J5 Connector**

  Supports PS/2 mouse, serial ports 1 and 3, first IDE channel, parallel port, keyboard, speaker, floppy disk, reset, USB, SMBus and power signals.

- **CPCI J4 Connector**

  Supports Ethernet 0, second IDE channel, SCSI, VGA, and power signals.

- **CPCI J3 Connector**

  Supports serial ports 2, 3 (Infrared), and 4, V-Port, Ethernet 1, and power signals.

- **CPCI J2 Connector**

  Supports additional system slot signals, and power.

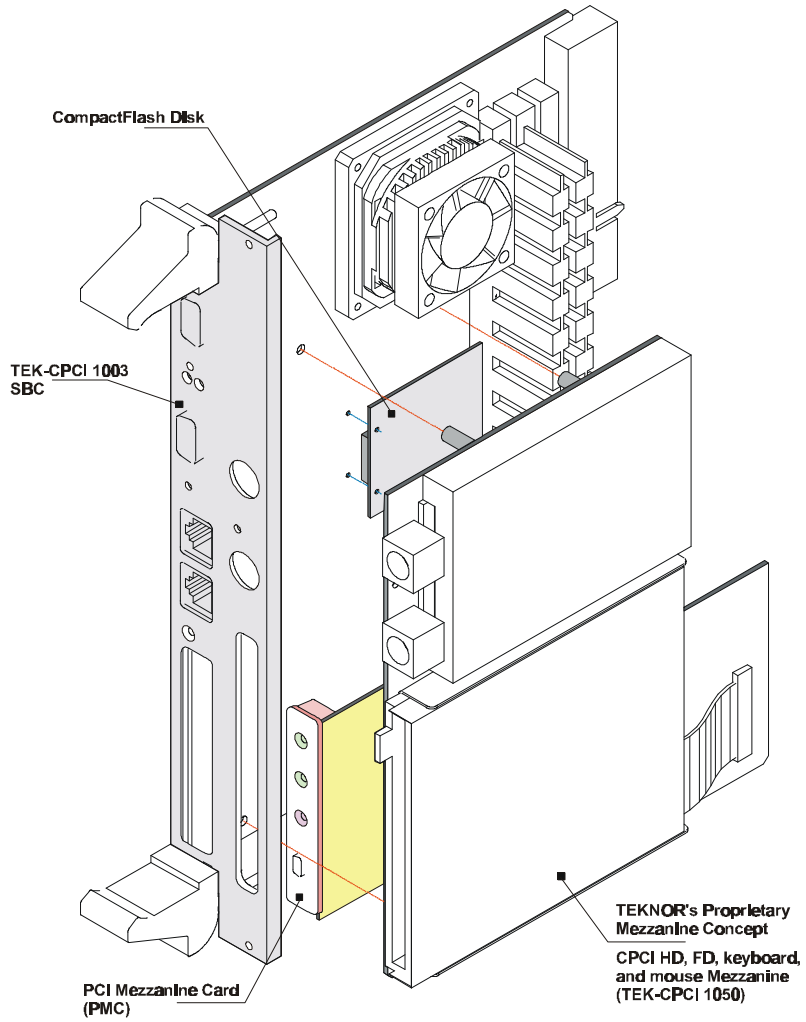
- **CPCI J1 Connector**

  Supports CPCI bus signals, and power.

6. MEZZANINE CONCEPTS

The capability of the TEK-CPCI-1003 to connect with other devices is enforced by three mezzanine board concepts TEKNOR has implemented on the board.

A fully equipped TEK-CPCI-1003 board may appear as follows:



6.1 PROPRIETARY MEZZANINE CONCEPT

This is TEKNOR's proprietary concept to expand the I/O capability of the board. It is built around two connectors:

- **J14**: which handles a complete PCI signal set (Primary bus) including the REQ/GNT arbitration signal pair (REQ4/GNT4).
- **J19**: which handles IDE0, floppy disk drive, keyboard and mouse signals.

These two connectors represent an open door for future development of expansion and I/O mezzanine boards.

The mechanical location of the connectors allows features such as connectors and indicators to be available directly on the front plate.

A Storage Mezzanine Board referred to as TEK-CPCI 1050 is provided by TEKNOR. Many other functions will be available soon. For more information, please contact TEKNOR's offices.

6.2 PMC CONCEPT

PCI Mezzanine Card (PMC) is a standard specification that allows PCI I/O devices to be connected to the PCI bus. It conforms to the ANSI/IEEE P1386.1 specification that defines Standard Physical and Environmental Layers for PMC devices.

The TEK-CPCI-1003 features the PMC concept onboard to provide an extra method to support the 32-bit I/O devices available on the market.

Various devices such as Ultra-SCSI, Fire-Wire, PCMCIA, Bus Analyzers, Digital I/O, ... are available from Silicon Control, Cyclone, Technobox, Vmetro, and many more.

PMC devices connect directly to J20 and J21standard PMC connectors. A mechanical cutout (with its EMI proof cap) is provided to allow integrated connectors and indicators to be available directly on the front plate.

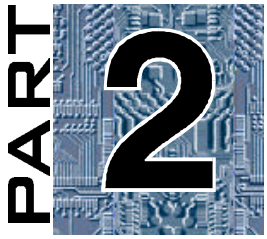
6.3 COMPACTFLASH FEATURE

The TEK-CPCI-1003 board also supports standard CompactFlash disks through a CompactFlash module.

CompactFlash disk is becoming a new standard method of storing and transferring data. It is supported on the board as a standard IDE drive and connects to the EIDE 0 interface.

The CompactFlash drive can be set as a Master or Slave device and combined with any standard hard disk drive.

CompactFlash is installed on J11 connector. For more information on CompactFlash installation and setups, please refer to Section 7.1 – *CompactFlash Interface*.



FEATURE DESCRIPTION

7. ONBOARD FEATURES

7. ONBOARD FEATURES

7.1 COMPACTFLASH INTERFACE

The board supports an IDE compatible flash disk by using a CompactFlash module. CompactFlash (C-Flash) disks are the world's smallest resident industry-standard ATA/IDE subsystem for application, data, image, and audio storage. They have the same functionality and capabilities as intelligent disk drives, but with the advantages of being very compact, rugged (typical M.T.B.F. is 1,000,000 hours) and low power.

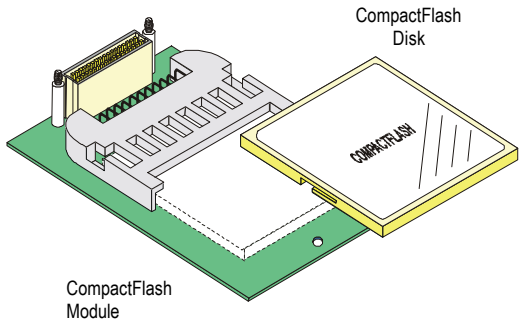
Available capacities are up to 24MB. 40 and 80MB modules will be supported when available.

The C-Flash disk connects on the TEK-CPCI-1003 via the onboard Flash Disk connector referred to as J11.

7.1.1 Working with CompactFlash Module

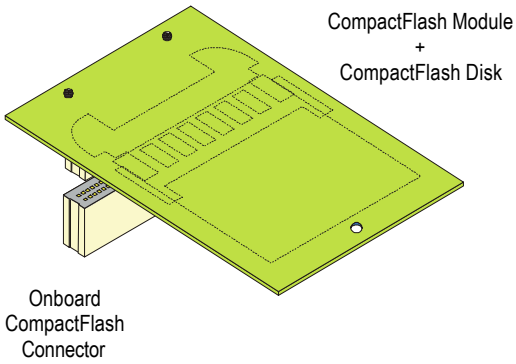
Follow this procedure to install a CompactFlash disk on the TEK-CPCI-1003 board:

1. Slide the CompactFlash disk into its receptacle and press gently to ensure a good insertion and connection.



2. Clip the spacers into the mounting holes: they are located close to the connector.

3. To connect the module to the SBC, line up the J11 connector and the module's connector, and then press the module firmly into the connector to engage the connector and the spacers.



7.1.2 Setups

The CompactFlash disk connects directly on the Primary EIDE interface. It must be declared the same way as a standard hard disk using the BIOS setup program (Autodetect Function).

To setup the CompactFlash disk for Master or Slave configuration, use the W5 jumper located on the SBC.

To locate and install a jumper cap on W5, please refer to Section 10 – *Setting Jumpers*.

NOTE

Since data is accessed like it would on an IDE drive, no specific flash disk driver is required for various operating systems.

7.2 ENHANCED IDE INTERFACES

The board features two Enhanced IDE interfaces dedicated to Primary and Secondary EIDE logical interfaces. Each support up to two IDE devices (including CD-ROMs, hard disks, plus CompactFlash on the secondary IDE interface) with independent timings, in Master/Slave combination.

SIGNAL PATHS

The primary EIDE interface is available through both the J5 CPCI I/O connector and the J19 Mezzanine connector.

Secondary EIDE interface is only available through the J4 CPCI I/O connector.

The IDE interfaces supports PIO IDE transfers up to 14MB/sec and Bus Master IDE transfer up to 33MB/sec (Ultra-DMA 33). It does not consume any ISA DMA resources and integrates 16x32-bit buffers for optimal transfers.



CAUTION

When connecting IDE devices to the Primary IDE interface (IDE0), Master and Slave devices must be shared in respect of the device allocation on both the CPCI I/O connector and the mezzanine

Two Master devices (or two Slave devices) must not be installed on the same interface at the same time.

7.3 ETHERNET INTERFACES

Both Ethernet controllers reside on the Primary PCI bus and are therefore Plug and Play by default. No manual configuration is required.

Each interface supports 10Base-T and 100Base-TX specifications: 10Mbps and 100Mbps network speeds are automatically detected and switched.

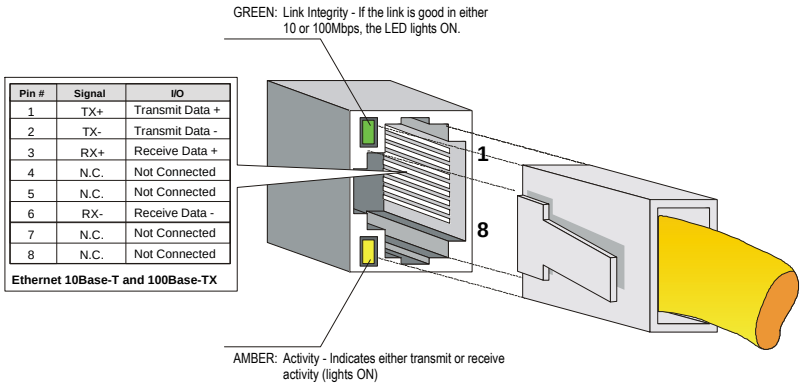
SIGNAL PATH

Ethernet signal path depends on the output configuration you have ordered for the board.

- **Front Plate Configuration**

  Ethernet 0 and 1 signals are respectively available on J15 and J12 RJ-45 connectors only when the board is ordered for front plate operations.

  Activity and link indicators are built in and are described as follows:



Pin #	Signal	I/O
1	TX+	Transmit Data +
2	TX-	Transmit Data -
3	RX+	Receive Data +
4	N.C.	Not Connected
5	N.C.	Not Connected
6	RX-	Receive Data -
7	N.C.	Not Connected
8	N.C.	Not Connected

Ethernet 10Base-T and 100Base-TX

- **CPCI I/O Configuration**

  Ethernet 0 and 1 signals are respectively available on J4 and J3 CPCI I/O connectors only when the board is ordered for rear panel output operations.

  Setting the board to operate in rear panel output configuration requires the installation of zero ohm resistors on the board to connect signals to the connectors.

  Resistor references are listed in the following table:

Ethernet 0 Signals	0 ohm Location:
ERX-0	R257
ERX+0	R264
ETX-0	R263
ETX+0	R265

Ethernet 1 Signals	0 ohm Location:
ERX-1	R262
ERX+1	R256
ETX-1	R261
ETX+1	R260



CAUTION

Ethernet interfaces are provided (factory connected) on CPCI I/O connectors only when the board is ordered for Rear Panel I/O configuration.

The combination of both front and rear panel configurations is not supported.

The Boot from LAN capability is supported. To enable the option, use the BIOS Setup program. Please refer to Section 12.3.2 – *BIOS Feature Setup*.

A diskette entitled “Network Drivers for IN82558 is included with the TEK-CPCI-1003. It contains network drivers for usual operating systems.

To install the drivers, run the “setup.exe” program.

For other operating system drivers and installation instructions, contact TEKNOR’s Technical Support department.

7.4 FLOPPY DISK INTERFACE

The onboard floppy disk controller is IBM PC XT/AT compatible (single and double density), and supports Enhanced Floppy mode (2.88MB). It handles 3.5" and 5.25", low and high density drives. Up to two drives can be supported in any combination.

SIGNAL PATHS

The Floppy Disk Controller interface is available through the J5 CPCI I/O connector and through the J19 Mezzanine connector.



CAUTION

When connecting floppy disk drives to the board, FD0 and FD1 device combination must be shared in respect of the device allocation capability of the floppy disk interface.

Two FD0 devices (or FD1 devices) must not be installed on the same interface at the same time.

7.5 KEYBOARD/MOUSE INTERFACE

The onboard keyboard controller is 8042 software compatible. Keyboard and mouse signals are available through four outputs that support direct connection to the interface. Standard AT keyboard and PS/2 mouse are supported.

SIGNAL PATHS

Standard AT keyboard and PS/2 mouse signals are available through the J5 CPCI I/O connector and the J19 Mezzanine connector.

7.6 PARALLEL PORT

The TEK-CPCI-1003 features one multi-mode parallel port. It is compatible with standard Mode IBM PC/XT, PC/AT, and PS/2 compatible bi-directional parallel port, Enhanced Parallel Port (EPP), and Enhanced Capabilities Port (ECP).

SIGNAL PATHS

The Parallel Port interface is available through the J5 CPCI I/O connector only.

The differences between Standard, EPP, and ECP modes appear in the signal assignation of the pins on the connector. Differences are described as follows:

Pin Number (J5)	Standard Mode	EPP Mode	ECP Mode
A15	SLCT	-	SLCT
B15	PE	-	PERROR[1], ACKREVERS[2]
C15	BUSY	WAIT	BUSY[1], PERIPHACK[2]
D15	/ACK	/INTR	/ACK
E16	/SLCTIN	/ADDRSTRB	/SLCTIN
B17	/INIT	-	/INIT[1], /REVERSERQST[2]
D17	/ERR	-	/FAULT[1], /PERIPHRQST[2]
A18	ALF	DATASTB	ALF[1], HOSTACK[2]
E17	PD0	PD0	PD0
C17	PD1	PD1	PD1
A17	PD2	PD2	PD2
D16	PD3	PD3	PD3
C16	PD4	PD4	PD4
B16	PD5	PD5	PD5
A16	PD6	PD6	PD6
E15	PD7	PD7	PD7

[1] Compatible mode

[2] High Speed Mode

NOTE

To operate in EPP or ECP mode, ensure the peripheral is designed to work in this mode and the BIOS setup is configured to support it.

7.6.1 Standard Mode

The Standard mode is unidirectional. It is supported to maintain the compatibility with the IBM PC standard.

7.6.2 EPP Mode

The EPP (Enhanced Parallel Port) mode consists of a hardware independent method of accessing a parallel port configured as EPP. It provides support for single I/O cycle as well as the high performance block I/O transfers. The EPP mode always uses the most optimum method for I/O transfers. For example, if the hardware supports it, EPP mode will perform 32-bit I/O block transfers.

EPP mode assumes that the parallel port can be used to connect more than one peripheral device using Multiplexor or Daisy Chain configurations.

Multiplexor is an external device that permits up to eight parallel port devices to share a single parallel port.

A Daisy Chain device has two ports: input and output. The input port is connected either to the host parallel port or the daisy chain device in front of it. The output is used to connect the next peripheral device to the daisy chain. The last device, however, can be one without daisy chain support.

7.6.3 ECP Mode

ECP (Extended Capabilities Port) works the same as EPP mode, but it will take precedence over the EPP mode when addressing multiple logical devices in a single physical product. While the EPP mode may intermix read and write operations without any overhead or protocol handshaking, the ECP mode negotiates data transfers using a request from the host and an acknowledgment from the peripheral.

NOTE

For more information on the ECP protocol, please refer to the Extended Capabilities Port Protocol and ISA Interface Standard (available from Microsoft Corporation) or contact our Technical Support department.

7.7 POWER MANAGEMENT

Power Management features are supported at the BIOS level. All Power Management options are described in Section 12.3.4 – *Power Management Setup*.

7.8 SCSI INTERFACE

The board features wide UltraSCSI interface with 32-bit PCI bus master control and zero wait state transfer capabilities.

The Wide UltraSCSI interface supports operation up to 40Mbytes/sec. Signals are available through J4 CPCI I/O connector.

SIGNAL PATH

SCSI interface signals are only available through the J4 CPCI I/O connector.

To operate with SCSI devices the onboard SCSI controller must be set by running the AWARD BIOS setup program (Section 12.3.7 – *Integrated Peripherals*).

To configure or view the default configuration setting for the SCSI host adapter, use the Adaptec SCSISelect utility available on the LAN Boot & SCSI Utility diskette 2.

To install the appropriate SCSI driver for a specific operating system, use the EZ-SCSI software available on the SCSI Utility diskette 1.

7.9 SERIAL PORTS

Four full function serial ports are provided on the board for asynchronous serial communications. They are 16C550 high-speed UART compatible and support 16-byte FIFO buffers for transfer rates at up to 230 and 460Kbaud.

Each serial port is specified as follows:

Designation	Communication Mode	Output Path
Serial Port 1	RS-232	Front Plate DB-9 J10, CPCI J5
Serial Port 2	RS-232	CPCI J3
Serial Port 3	RS-232, RS-422, RS-485, Infrared	CPCI J3, CPCI J5
Serial Port 4	RS-232	CPCI J3

UART registers are individually addressable and fully programmable

7.9.1 Serial Port 1

Serial Port 1 is buffered directly for RS-232 operation. Signals include the complete signal set for handshaking, modem control, interrupt generation, and data transfer. When assigned as COM1, the port is 100% compatible with the IBM-AT serial port in RS-232 mode.

SIGNAL PATH

Serial Port 1 signal path depends on the output configuration you have ordered for the board.

- **Front Plate Configuration**

  Serial Port1 signals are available through the J10 DB-9 connector located on the front plate. In this configuration the port is 100% compatible with the IBM-AT serial port specification.

- **CPCI I/O Configuration**

  The complete signal set is tied to the J5 CPCI I/O connector to be used through a backplane

7.9.2 Serial Port 2

Serial Port 2 is buffered directly for RS-232 operations and is 16C550 PC-Compatible. The interface includes the complete signal set for handshaking, modem control, interrupt generation, and data transfer.

When assigned as COM2 logical port, the port is 100% compatible with the IBM-AT serial port.

SIGNAL PATH

Serial Port 2 signals are only available through the J3 CPCI I/O connector.

7.9.3 Serial Port 3

The Serial Port 3 supports Infrared, RS-232, RS-422, and RS-485 operation modes. When assigned as COM3, the port is 100% compatible with the IBM-AT serial port in RS-232 mode.

RS-422 and RS-485 modes allow communication using differential signals through one pair of wires (RS-485) or two (RS-422) to increase the noise immunity during data transfers.

RS-422 and RS-485 protocols offer advantages such as increased speed over longer distances or improved reliability over similar RS-232 setups.

SIGNAL PATHS

In RS-232, RS-422, and RS-485 operation modes Serial Port 3 signals are only available through the J5 CPCI I/O connector.

In Infrared mode, signals are available through the J2 CPCI I/O connector.

Upon a power-up or reset, the Serial Port 3 interface circuits are automatically configured for the operation mode setup in the BIOS. The Serial Port 3 signal assignation on the J5 CPCI I/O connector depends on the operation mode (RS-232, RS-422, or RS-485) it has been set:

Pin Number (J5)	RS-232	RS-422	RS-485
A11	/JDCD2	/DCD	/DCD
C11	JRXD2	RX(-)	RX/TX(-)
D11	/JDSR2	DSR	DSR
E11	JTXD2	TX(-)	-
A12	/JRTS2	RX(+)	RX/TX(+)
B12	/JCTS2	TX(+)	-
C12	/JRI2	/RI	/RI
E12	/JDTR2	/DTR	/DTR

To configure the Serial Port 3 operation mode, use the BIOS setup program. See Section 12.3.7 - *Integrated Peripherals*.

- **Infrared Mode:**

  Infrared (IR) interface signals are provided to drive IR module for remote operations through Serial Port 3. When set in IR mode, the IR interface supports multi-protocol infrared operations. The IR interface is IrDA 1.1 compliant, and supports TEMIC/HP modules, SHARP ASK IR, and consumer IR.

- **RS-232 Protocol:**

  When configured for RS-232 operation mode, the Serial Port 3 is 100% compatible with the IBM-AT serial port signals.

- **RS-422 Protocol:**

  The RS-422 protocol (Full Duplex) uses both RX and TX lines during a communication session.

  There are no user software restrictions except that software must not attempt to use the handshake line because they are not connected. However, handshaking by software only (XON-XOFF) may be used.

CAUTION

In RS-422 mode, W9 and W10 jumper caps must be installed to connect the 120 ohms termination resistors (See Section 10 – *Jumper Settings*).

- **RS-485 Protocol:**

The RS-485 protocol (Half Duplex) also uses differential signals during a communication session. It differs from the RS-422 mode as it offers the ability to transmit and receive over the same pair of wires, and allows the sharing of the communication line by multiple stations. This configuration (also known as Party Line) allows only one system to take control of the communication line at the time.

In RS-485 mode, the RX lines are used as the transceiver lines, and the RTS signal is used to control the direction of the RS-485 buffer.

When set for RS-485 mode in the BIOS, upon power-up or reset, the transceiver is by default in receiver mode to prevent unwanted perturbation on the line. Party line operation mode requires termination resistors to be installed at both ends of the network.



CAUTION

When installing the TEK-CPCI-1003 at one end of the network, W9 and W10 jumper caps must be installed to connect the 120 ohms termination resistors (See Section 10 – *Jumper Settings*).

7.9.4 Serial Port 4

The Serial Port 4 is buffered directly for RS-232 operations and is 16C550 PC-Compatible. The interface includes the complete signal set for handshaking, modem control, interrupt generation, and data transfer.

When assigned as COM4 logical port, the port is 100% compatible with the IBM-AT serial port.

SIGNAL PATH

Serial Port 4 signals are only available through the J3 CPCI I/O connector.

7.10 THERMAL MANAGEMENT

Two temperature sensors are provided to supervise the thermal environment. One is used to monitor the CPU die temperature, while the second one, located on the casing, allows the monitoring of the ambient temperature around the CPU.

The temperature is controlled according to two temperature levels, the Low temperature limit, which indicates normal operating conditions, and the High temperature limit, which indicates an overheating condition.

The temperature management consists in reducing the CPU clock speed throttling when the temperature goes over the high limit (overheating condition) and suspending the throttling operation as soon as the temperature returns under the low temperature limit (normal condition).

Thermal management operations are controlled by the BX chipset, and settings are provided through the BIOS setup program interface, *Thermal Management Setup* option (See Section 12-12 *Thermal Management Setup*).

Temperature levels of both the die and the casing operate the same way to reduce the CPU clock speed. When the high temperature limit is reached, the clock speed is automatically reduced (if enabled in the BIOS) to 75% of its nominal capacity.

- The clock speed may be throttled by a CPU overheating due to the fan failure. In such a case, the temperature control is triggered as soon as the temperature reaches the high temperature limit of the die.
- The ambient temperature of the CPU raises up due to an augmentation of the temperature in the casing. In that case, the clock speed will be slowed down as soon as the ambient temperature reaches the high ambient temperature value.

7.11 USB INTERFACES

Signals for two USB ports are available through the J5 CPCI I/O connector.

USB is becoming the new essential peripheral interface. The USB strengths are as follows: capability to daisy chain as many as 127 devices per interface, fast bi-directional, isochronous/asynchronous interface, 12Mbps transfer rate, and standardization of peripheral interfaces into a single format.

SIGNAL PATHS

Both USB 0 and USB 1 interface signals are available through the J5 CPCI I/O connector.

USB supports Plug and Play and hot swapping operations (OS level). These user-friendly features allow USB devices to be automatically attached, configured and detached, without reboot or setup run.

The TEK-CPCI-1003 board fully supports the standard universal host controller interface (UHCI) and uses standard software drivers that are UHCI-compatible.

7.12 VIDEO INTERFACE

The high-performance video capability of the board is based on the latest Accelerated Graphics Port (AGP) technology. The video controller, CL-GD5465 from Cirrus Logic, connects directly to the Primary PCI bus, and interfaces with 2MB onboard video memory through the Rambus channel (600MB/sec bandwidth).

64-bit 2D/3D graphics engine, 64-bit GUI accelerator engine with multiple window video acceleration, and Enhanced V-Port interface are some of the major video features.

SIGNAL PATH

The VGA video signal path depends on the output configuration you have ordered for the board.

- **Front Plate Configuration**

  VGA interface signals are available on J8 standard SVGA video connector, located on the front plate of the board, only when the board is ordered for front plate operations. This configuration allows direct connection of CRT display onto the board.

- **CPCI I/O Configuration**

  VGA interface signals are available on J4 CPCI I/O connector only when the board is ordered for rear panel output operations.

  Setting the board to operate in rear panel output configuration requires the installation of zero ohm resistors to connect signals to the CPCI connector. Resistor references are listed in the following table:

Video Signals	0 ohm Location:
VSDA1	R116
VSCL1	R115
BLUE	R118
GREEN	R113
RED	R114
VSYNC	R100
HSYNC	R101

7.12.1 Supported Resolutions

The maximum video resolution and performance depend directly on the drivers running with your software application. Resolution and number of colors specification are listed below:

Resolution	Number of Colors
640x480, 800x600, 1024x768, 1280x1024, 1600x1200	256 (8 bits)
640x480, 800x600, 1024x768	65,536 (16 bits)
640x480, 800x600	16.8 million (24 bits)
640x480, 800x600	16.8 million (32 bits)

7.12.2 Major Features Description

- **VGA Compatibility**

  The video controller includes all registers and data paths required for VGA controllers, and supports extensions to VGA, including resolutions up to 800x600x16.8 million colors non-interlaced. 16-bit images are displayed at up to 1024x768 resolution, and 256-color modes can reach a maximum of 1600x1200 resolution.

- **Rambus**

  The Rambus interface offers up to 600MB/sec bandwidth. Memory bandwidth is allocated during CPU access, DRAM refresh, screen refresh, 2D/3D engine operations, and Enhanced V-Port access.

- **2D Graphics Engine**

  The 2D graphics engine is an advanced 64-bit three-operand engine that accelerates BitBLTs as line draws, polygon draw, and polygon fill. The 2D graphics engine also performs video and bitmap scaling, and data overlay.

- **3D Graphics Engine**

  The 3D graphics engine can draw randomly oriented triangles with Gouraud shading, texture mapping, alpha blending, and Z-buffering. It uses AGP/PCI bus mastering to fetch instructions and parameters from system memory to render scenes with a minimum of host intervention.

7.13 V-PORT

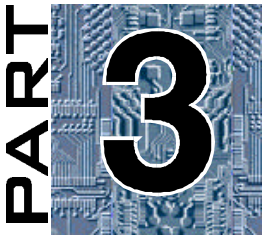
V-Port signals are provided as a dedicated video path to the display memory. It is intended to support a source of live video incoming from an external video source.

The enhanced V-Port captures video off-screen buffers from which it is displayed with resizing and color space conversion. Once initiated, capture and display occurs with a minimum of processor intervention. The I^2C serial interface provides a method of controlling a video controller from the host, as well as DDC2B monitor interfacing.

SIGNAL PATH

V-Port signals are only available through the J3 CPCI I/O.

Video capture and scaling are also supported.



INSTALLATION AND SETTINGS

8. CUSTOMIZING THE BOARD

9. SETTING JUMPERS

10. BUILDING A CPCI SYSTEM

11. CPCI I/O SIGNALS

8. CUSTOMIZING THE BOARD

8.1 PROCESSOR AND FAN

Your board will be installed with one of the available Mobile Pentium II processor: 233MHz, 266MHz or 300MHz, and its adequate cooling system.

8.1.1 Installing Microprocessor

Since CPUs are very sensitive components, particular attention should be given while installing a processor on the board. The CPU core voltage must be set at the adequate value using the W1 jumper and according to the following table:

		W1 Jumper Setting					
Processor	**Core Voltage**	**1-2**	**1-2**	**3-4**	**5-6**	**7-8**	**Vcore**
MP II 233MHz	1.7V	on	on	on	off	on	1.69V
MP II 266MHz	1.7V	on	on	on	off	on	1.69V
MP II 300MHz	1.6V	on	off	on	off	on	1.59V

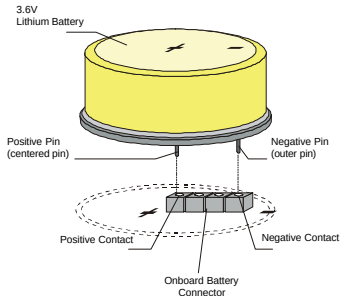
WARNING

Careful attention should be taken when installing a processor: Faulty jumper settings can damage both the board and the processor.

Please refer to Section 9 – *Setting Jumpers* for a complete information on the available core voltage values and associated jumper settings.

8.2 BACKUP MEMORY

An onboard 3.6V lithium battery is provided to backup BIOS setup values and the real time clock (RTC).



When replacing, the battery must be connected as follows:

WARNING

- Danger of explosion if battery is incorrectly replaced -

Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.

8.3 INSTALLING MEMORY

8.3.1 SDRAM System Memory

The TEK-CPCI-1003 supports three 168-pin DIMM (Dual In-Line Memory Module) sockets for memory configuration from 8MB to 384MB of Synchronous DRAM (SDRAM) or 768MB using RSDRAM (Registered SDRAM).

The memory characteristics must conform to the following:

- 1.15 inch height,
- Standard 3.3V only,
- 64-bit and 72-bit modules, single-sided or double-sided,
- Unbuffered 66MHz (SDRAM),
- Serial Presence Detect (SPD) EEPROM,
- Errors Checking and Correction (ECC) capabilities or parity bit with 72-bit modules,
- Compliant with Intel's PC SDRAM Unbuffered DIMM Specification (66MHz) Rev. 1.0.

At least 8MB of memory must be installed on the board for proper operation. Modules can be installed in any socket and order. The total system memory is equal to the sum of the memory module size installed in the three DIMM sockets.

NOTE

When populating with more than one memory module, each socket must be installed with the same memory type (64/72-bit), however the capacity of each module may be different from the other.

The recommended DIMM devices are listed in the table below. Many other models are available and function equally well. Users are encouraged to check with their local distributors for comparable substitutes.

SDRAM DIMM Module	VENDOR	PART NUMBER	MRP Code
32MB - 4M*72	ROCKY MOUNTAIN RAM	4x72CQ2x8S4E	635-049
	CENTON	CFEKG1TTNVU367G	
128MB - 16M*72	ROCKY MOUNTAIN RAM	16x72CQ8x8S4E	635-050

8.3.2 DIMM Installation

To install the DIMMs in the sockets, proceed as follows:

1. With the board flat on the table, turn it so that the front plate is facing you.
2. Hold the module vertically so that the bottom connector key is on the right. Insert the fingers into the socket. The socket's keys will ensure a correct mating.
3. Press firmly on the top edge of the memory module to engage it into the socket. The module is fully inserted when the retaining clips snap into notches located at each end of the module.

If necessary, work your way by inserting the other modules, one by one.

To remove the DIMMs from the sockets, pull simultaneously on the retaining clips located on each side of the socket. Once the module has snapped out, pull gently on it.

8.4 SUPERVISION FEATURES

The TEK-CPCI-1003 provides a set of programmable I/O registers to setup the Intel PIIX4 (I/O addresses 4030h to 4037h) and the XILINX CPLD (I/O addresses programmable at 190h-193h, 290h-293h or 390h-393h using the AWARD Chipset Features Setup).

Only register bits needed to program the power fail detection and watchdog functions are described below.

8.4.1 Power Fail Monitoring

The power failure detector status can be readout from one bit of the system register located at the address 4031h (See table below). The detection conforms to the following conditions (* = active low signal):

1. It always monitors the +5V power supply. When it drops below 4.65V (typical), the system is reset.
2. It can monitor the onboard battery. When the battery is in a low condition (below 2.9V typical), the PFO* (power fail output) signal goes low. The status of the PFO* signal can be read at I/O address 4031h, bit 1 (0 = failed, 1 = good). The PFO* signal can also be connected to the IOCHK* signal to generate an NMI (non-maskable interrupt) by setting W3 jumper. To setup W3, please refer to Section 9 – *Setting Jumpers*.

An interrupt handler can then service the interrupt. If you choose not to generate an NMI, you can use an algorithm to detect a low battery condition and respond accordingly.

Register	Bit #	Function	Software Programming
4030h	0-7	Reserved	Reserved
4031h	0, 2-7	Reserved	Reserved
	1	Power Fail Output (Internal/External Battery or External Power Source)	Read: 0 = Failed, 1 = Good
4032h	0, 2-7	Reserved	Reserved
	1	Watchdog Stage 1 Status	Read: 0 = Timed out, 1 = Normal
4034h	0-7	Reserved	Reserved
4035h	0-1, 4-7	Reserved	Reserved
	2	Watchdog enable	Write: 1 = Disable, 0 = Enable
	3	Watchdog reset	Write: 1-0-1 (toggle) to activate the watchdog (when enabled)
4036h	0-7	Reserved	Reserved
4037h	0-7	Reserved	Reserved

For more information, contact the Technical Support department

8.4.2 Watchdog

The TEK-CPCI-1003 provides a two-stage watchdog to monitor the CPU inactivity. Its function is to issue a failure signal if the processor fails to refresh the watchdog within the watchdog timeout period. The feature is useful in embedded systems where human supervision is not required or impossible.

The watchdog configuration may be selected between Dual-Stage, Single-Stage, or disabled, using the W2 jumper (see Section 9 – *Setting Jumpers*).

The default timeout period is 1.6s for the first stage and 400ms for the second stage; however, the timeout period can be changed:

- Shorting R234 and leaving C248 opened, sets the first stage timeout value to 400ms
- Removing R237 and C248, sets the second stage timeout value to 1.6s

CAUTION

Modifying the Watchdog timeout period will also modify the value of the Reset period according to the following formula:

(200ms/47pF) x C

- **Single-Stage Watchdog**

  In a single-stage configuration, the first watchdog detector monitors the output of the first stage watchdog time-out.

  To operate the watchdog, the processor drives the watchdog input (see register description) with an I/O line. It toggles WDI once every 400ms (typical) to verify the software is running properly. If a hardware or software failure occurs such that WDI is not toggled, the watchdog output (WDO) will go low after 400ms, and reset the CPU. If the processor can continue to run a 0-1-0 toggle routine, WDO will be set high by the next transition of WDI.

  In dual stage configuration, the WDO signal indicates the second stage watchdog when a failure occurs.

  Following a reset, the watchdog is always disabled.

Dual-Stage Watchdog

The dual-stage watchdog consists of a second watchdog in cascade with the first one: in the event the first watchdog failed to toggle, the second stage is set to grant the system an additional 1.6s delay prior to the system reset.

Before the second stage watchdog resets the system, the first watchdog output can be tied to the ISA's IOCHK line to generate an NMI to the CPU, while the two watchdog values are stored. These values may be used to determine the cause of the system's reset.

CAUTION

The user program must provide the first access to address 190h (or 290h or 390h depending on the I/O address selected in BIOS setup), and must also include the refresh routine.

Watchdog Flags

The watchdog status can be read from two bits (5 and 6) of the system register located at the address 191h, 291h or 391h (depending on the I/O address selected in CMOS setup).

The register bits are specified as follows:

Register	Bit #	Function	Software Programming
190h	0-7	Reserved	Reserved
191h	0-4, 6	Reserved	Reserved
	5	Watchdog reset history status	Read: 1 = Last system reset caused by the watchdog timeout
	7	Push button reset history status	Read: 1 = Last system reset caused by the push button reset switch
192h	0	Clear history status (watchdog and push button)	Read/Write: 0 = Clear, 1 = Normal
	1-7	Reserved	Reserved
193h	0-7	Reserved	Reserved

1 May be reprogrammed in the AWARD Chipset Features Setup to addresses 290h-293h or 390h-393h

8.4.3 Thermal Management

The thermal management is built around two digital temperature sensors and a thermal watchdog. Both devices can be programmed to set their outputs when the temperature of the processor or the ambient temperature exceeds a programmable high limit, and reset its output when the temperature is under a programmable low limit. A special routine is implemented to throttle the CPU clock until the temperature falls below the programmed low limit.

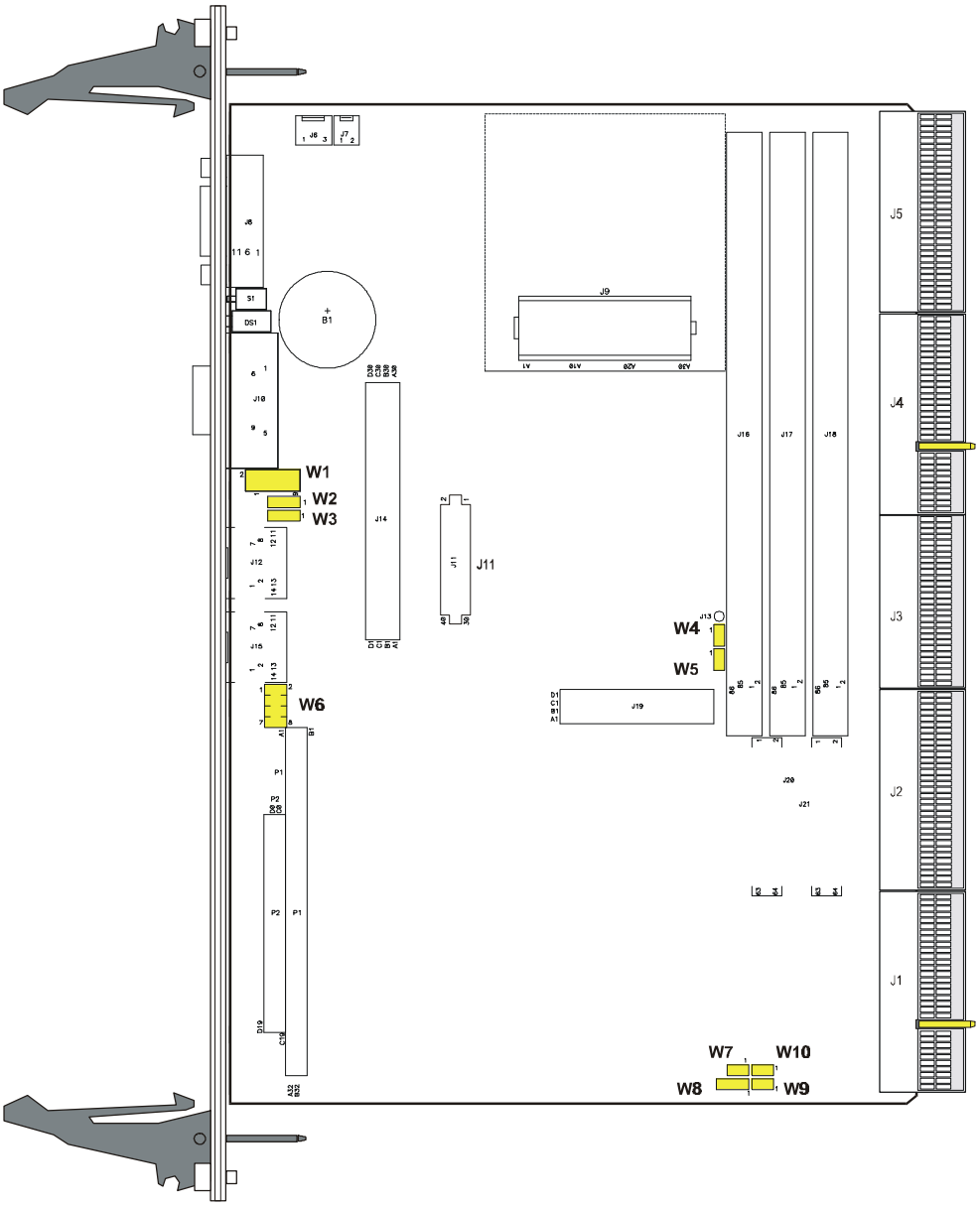
Please refer to Section 12.3.5 – *Thermal Management Setup* for a complete information thermal management setups.

9. Setting Jumpers

Ten jumpers are available to configure the TEK-CPCI-1003:

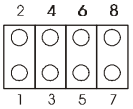
Jumper	Description
W1	**CPU Core Voltage** - Use this jumper to setup the core voltage according to your CPU specification.
W2	**Watchdog** – enables Single or Dual Stage watchdog or disables the watchdog.
W3	**IOCHK Line Assignation** – Use this jumper to select the source signal to be connected to the IOCHK line. Available options are PFO or WDO1 signals.
W4	**Battery** – Connects or Disconnects the battery to/from the board circuitry.
W5	**CompactFlash Setting** – Use this connector to setup the CompactFlash device in Master or Slave configuration.
W6	**VT100 Mode (5-6)** – When enabled, allows VT100 or ANSI terminal connection. **Download Mode (7-8)** – When enabled, allows data serial download from a remote computer.
W7	**Video Enable** – Use this jumper to enable or disable the onboard video feature.
W8	**SCSI Termination** – Use this jumper to disable SCSI termination or select the termination control method from *Software Controlled* and *Hardware Controlled* options.
W9-W10	**Serial Port 3 Termination** – Use these jumpers to connect or disconnect termination resistors on/from Serial Port 3 when set for RS-422/RS-485 operation mode 0.

JUMPER LOCATION



JUMPER SETTINGS (Table 1)

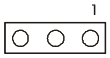
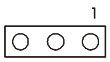
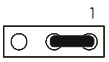
TEK-CPCI 1003 CPU Core Voltage Selection



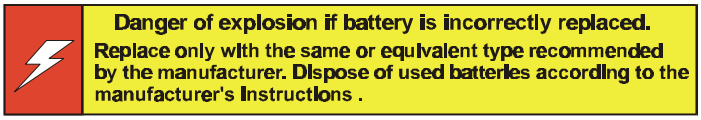
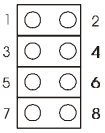
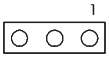
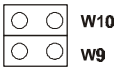
		W1				
	Vcore	1-2	3-4	5-6	7-8	9-10
	1.24	off	off	off	off	off
	1.34	off	off	off	off	on
	1.39	on	off	off	off	on
	1.44	off	on	off	off	on
	1.49	on	on	off	off	on
	1.54	off	off	on	off	on
MPII-300 →	1.59	on	off	on	off	on
	1.64	off	on	on	off	on
MPII-233 / MPII-266 →	1.69	on	on	on	off	on
	1.74	off	off	off	on	on
	1.79	on	off	off	on	on
	1.84	off	on	off	on	on
	1.89	on	on	off	on	on
	1.94	off	off	on	on	on
	1.99	on	off	on	on	on
	2.04	off	on	on	on	on

		W1				
Vcore	1-2	3-4	5-6	7-8	9-10
2.09	on	on	on	on	on
2.14	on	off	off	off	off
2.24	off	on	off	off	off
2.34	on	on	off	off	off
2.44	off	off	on	off	off
2.54	on	off	on	off	off
2.64	off	on	on	off	off
2.74	on	on	on	off	off
2.84	off	off	off	on	off
2.94	on	off	off	on	off
3.04	off	on	off	on	off
3.14	on	on	off	on	off
3.24	off	off	on	on	off
3.34	on	off	on	on	off
3.44	off	on	on	on	off
3.54	on	on	on	on	off

Careful attention should be taken when Installing a processor: Faulty jumper settings may definitely damage both your board and your processor.

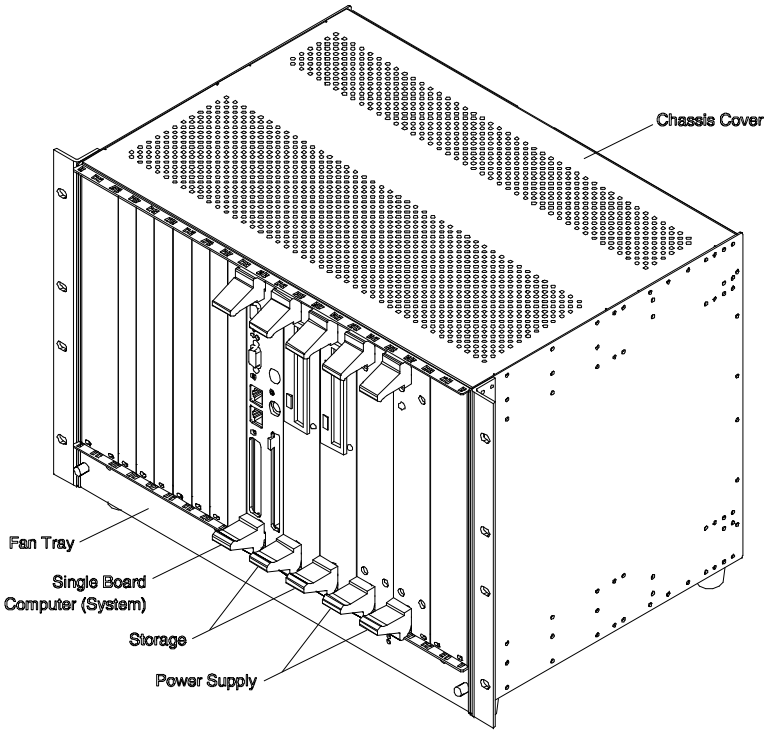
W2	Watchdog	 Disabled *	 Single-Stage	 Dual-Stage
W3	IOCHK Line Assignation	 Not Connected *	 Connected to PFO (Power Fail Out)	 Connected to WDO1 (Watchdog Out 1)

JUMPER SETTINGS (TABLE 2)

<table>
<tr><th>NAME</th><th>FUNCTION</th><th>CONFIGURATION (INITIAL SETTING: *)</th></tr>
<tr><td>W4</td><td>Battery</td><td> Connected *
 Disconnected
</td></tr>
<tr><td>W5</td><td>CompactFlash Setting</td><td> Master
 Slave *</td></tr>
<tr><td>W6</td><td>VT100 / Download Mode Setting</td><td>
<table>
<tr><th>W6</th><th>Function</th><th>Off</th><th>On</th></tr>
<tr><td>1-2</td><td>Reserved</td><td>-</td><td>-</td></tr>
<tr><td>3-4</td><td>Reserved</td><td>-</td><td>-</td></tr>
<tr><td>5-6</td><td>VT100 Mode</td><td>Disabled *</td><td>Enabled</td></tr>
<tr><td>7-8</td><td>Download Mode</td><td>Disabled *</td><td>Enabled</td></tr>
</table></td></tr>
<tr><td>W7</td><td>Video Enable</td><td> Disabled
 Enabled *</td></tr>
<tr><td>W8</td><td>SCSI Termination</td><td> Always Disabled
 Hardware Controlled *
 Software Controlled</td></tr>
<tr><td>W9
W10</td><td>Serial Port 2 Termination in RS-422/RS-485 Mode</td><td> Terminated with Resistors
 No Termination Resistors Installed *</td></tr>
</table>

10. BUILDING A CPCI SYSTEM

When building a CompactPCI system, a minimum requirement consists in: a chassis with 6U slots, CompactPCI backplane, storage module, power supply unit, and ventilation system.



The main AC power is drawn to the chassis components through an IEC power plug with a 2-stage filter, fuse holder and power switch. All power features are provided at the rear of the chassis.

The chassis may be used either as a desktop system or a rack-mount bay.

10.1.1 Backplane

The TEK-CPCI-1003 is compatible with all standard CompactPCI passive backplanes available on the market.

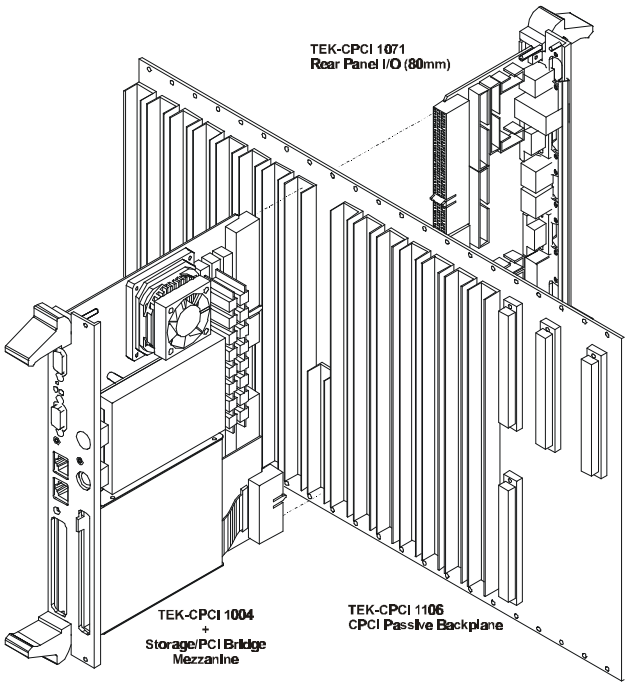
An entry-level backplane is provided by TEKNOR. It is referred to as TEK-CPCI-1103. It features 8 CPCI slots (one PCI I/O segment), and includes P3-P5 I/O connectors on all slots.

A 16-CPCI-slot backplane (TEK-CPCI-1106) is also available from TEKNOR. It supports two PCI I/O segment: one is driven directly by the SBC while the other is managed through a PCI-to-PCI bridge implemented on the TEK-CPCI 1051mezzanine board (Storage/PCI-to-PCI mezzanine).

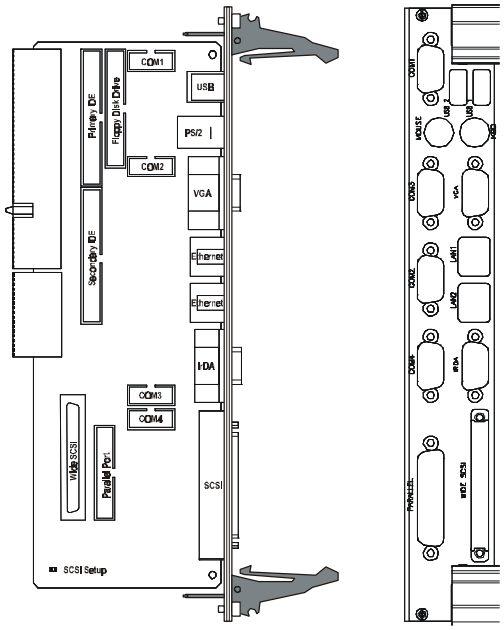
All TEKNOR's CompactPCI backplanes feature pass-through connectors (P3-P5) to support Rear Panel I/O connections.

10.1.2 Rear-Panel I/O

This feature is intended to issue the I/O capabilities of the SBC to the rear of the enclosure using a Rear I/O Transition module (TEK-CPCI 1071).



The Rear I/O Transition module gathers all the I/O signals of the CPU board and makes them easily accessible through standard headers and connectors located at the rear of enclosure. The Rear I/O Transition module (TEK-CPCI-1071) is illustrated below:



10.1.3 Storage Devices

A storage mezzanine (TEK-CPCI-1050/1051) attaches directly to the TEK-CPCI-1003. 6U form factor storage modules are supported when using the TEK-CPCI-1103 backplane.

10.1.4 Power Supply

6U power supply modules featuring load sharing redundant mode and hot-swap capabilities allow on-site replacements of defective a module while the system remains powered.

Standard ATX power supply units are also supported.

10.1.5 Fan Tray

The ventilation unit of the enclosure must conform to the global requirement of the system in fully loaded configuration.

10.2 INSTALLING THE BOARD INTO A BAY

The TEK-CPCI-1003 is a mechanical Eurocard form factor board. It takes advantages of the IEEE1101.10 specifications that ensure a mechanical interchange capability between different plug-in elements in sub-racks.

Due to the high-density pinout of the Hard Metric connector, some precautions must be taken when connecting or disconnecting a board to/from a backplane:

1. Rail guides must be installed on the enclosure to slide the board to the backplane.
2. Do not use force if there is any mechanical resistance while inserting the board.
3. Screw the front plate to the enclosure to firmly attach the board to its enclosure.
4. Use the extractor handles to disconnect and extract the board from its enclosure.

10.2.1 Connector Keying

CompactPCI connector support guide lugs to ensure a correct polarized mating. A proper mating is enhanced by the use of coding keys for 3.3V and 5V operation.

Coding keys prevent inadvertent installation of a 5V peripheral board in a 3.3V slot. The TEK-CPCI-1003 is universal. It does not support coding key. The PCI bus does not require to be keyed. Backplane connectors must always be keyed according to the signaling (VIO) level.

Coding Key Colors are defined as follows:

Signaling Voltage	Key Color
3.3V	Cadmium Yellow
5V	Brilliant Blue
Universal board (5V and 3.3V)	none

10.2.2 Bus Mastering

The TEK-CPCI-1003 provides seven pairs of REQ/GNT (0-7) arbitration signals through the Secondary PCI bus. This means the board is capable of driving up to seven CPCI slots with PCI Bus Master capabilities.

10.2.3 Connection

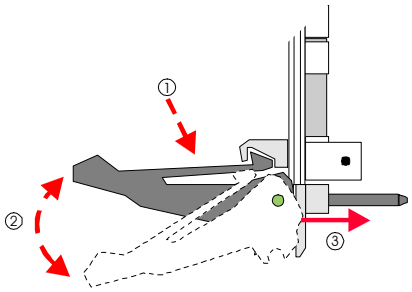
To install the TEK-CPCI-1003 board into a bay, proceed as follows:

1. Power off your CompactPCI system
2. Locate the 6U system slot
3. Remove the front plate of the slot where you intend to insert the TEK-CPCI-1003
4. Ensure the module is properly aligned with the guide-rails and slide it gently until it touches the backplane connector

> **WARNING**
>
> **1. Some mechanical parts of the guide-rail are fragile (shield contacts and clips). Do not use force to insert and connect a CompactPCI module.**
>
> **2. If there is any mechanical resistance while you insert a module, first ensure there is no mechanical obstacle and check for the alignment of all parts.**

5. To engage the board's connectors into the backplane connector, press simultaneously on the front plate and lift up the handle until the retaining clip hooks to the chassis.
6. Fasten the module using the fellow-plate fixing screw to secure the module to the system chassis.

To remove the module from the chassis, proceed as follows:



Remove the front plate fixing screws.

Press the handle (see ①) to disengage the retaining clip.

Press the handle to act as a lever (see ②) to disengage the CompactPCI connector from the backplane.

Pull on the handle and gently remove the board (see ③).

11. CPCI I/O SIGNALS

This section describes integrated feature signals available on rear panel CPCI I/O connectors (J3, J4, and J5).

11.1 J3 SIGNAL SPECIFICATION

11.1.1 V-PORT

Signal	Pin Assignation (J3)	Description
VP-OUT	A1	Reserved
ZVPCLK	B1	V-Port clock from the video source pixel clock
VP-IN	C1	Reserved
VACTI	D1	Video (data) Active Input
VSCL2	B2	I2C clock
VP 0-7	A5, C5, E5, B4, D4, A3, C3, E3	V-Port pixel data
VSDA2	A4	I2C data
/VP-HSYNC	C4	Horizontal Synch.
/VP-VSYNC	D2	Vertical Synch.
/EN-CAM	E4	Enable camera

11.1.2 Ethernet LEDS

Signal	Pin Assignation (J3)	Description
SPEEDLED 0-1	A6, E6	Speed LED signal
LINKLED 0-1	B6, D6	Link integrity LED signal
ACTLED 0-1	C6, A7	Transmit / receive activity LED signal

11.1.3 Ethernet 1

Signal	Pin Assignation (J3)	Description
ETX+1	A9	Ethernet 1 High Transmit Data line
ETX-1	B9	Ethernet 1 Low Transmit Data line
ERX+1	C9	Ethernet 1 High Receive Data line
ERX-1	D9	Ethernet 1 Low Receive Data line

11.1.4 Serial Port 3

Signal	Pin Assignation (J3)	Description
/JDCD3	A13	Data Carrier Detect
JRXD3	C13	Receive Data
/JDSR3	D13	Data Set Ready
JTXD3	E13	Transmit Data
/JRTS3	A14	Ready To Send
/JCTS3	B14	Clear To Send
/JRI3	C14	Ring Indicator
/JDTR3	E14	Data Terminal Ready

11.1.5 Serial Port 4

Signal	Pin Assignation (J3)	Description
/JDCD4	A11	Data Carrier Detect
JRXD4	C11	Receive Data
/JDSR4	D11	Data Set Ready
JTXD4	E11	Transmit Data
/JRTS4	A12	Ready To Send
/JCTS4	B12	Clear To Send
/JRI4	C12	Ring Indicator
/JDTR4	E12	Data Terminal Ready

11.1.6 IDE LED Signals.

Signal	Pin Assignation (J3)	Description
/EXT-SIDEACT	B18	Secondary IDE activity
/EXT-PIDEACT	C18	Primary IDE activity

11.1.7 IR Serial Port 2

Signal	Pin Assignation (J3)	Description
COM2-IRRX	D18	IR receive data line (Serial Port 2)
COM2-IRTX	E18	IR transmit data line (Serial Port 2)

11.1.8 Miscellaneous Signals

Signal	Pin Assignation (J3)	Description
/PWRBT	A19	ACPI Reserved
EXT-SMI	B19	System Management Interrupt Input
PX4-NMI	C19	Non Maskable Interrupt Input
PWROK-33	E19	High when 3.3V supply is valid on the board

11.2 J4 SIGNAL SPECIFICATION

11.2.1 Power Management

Signal	Pin Assignation (J4)	Description
I2C-CLK	A1	I2C clock signal
I2C-DATA	B1	I2C data signal
LID	C1	Reserved
/EXT-FAN0-FAIL	D1	Enclosure fan 0 fail
/EXT-FAN1-FAIL	E1	Enclosure fan 1 fail
/SM-BYPASS	A2	Reserved

11.2.2 SCSI Interface

Signal	Pin Assignation (J4)	Description
SCD 0-15	E7, D7, C7, B7, A7, E6, D6, C6, E2, D2, C2, B2, E8, D8, C8, B8	SCSI Data – The SCSI data lines drive the ID during arbitration and selection, and command and data information as well as status and messages.
/IO	A3	In/Out – Indicates the In direction when asserted and the Out direction when not asserted.
/SREQ	B3	Request – A target will assert REQ to indicate a byte is ready or is needed by the Target.
/CD	C3	Command/Data – Indicates Command or message phase when asserted, and Data phase when not asserted.
/SSEL	D3	SCSI Select – The line is driven after a successful arbitration to select as an initiator or reselect as a target and otherwise it is received.
/SMSG	E3	SCSI Message - Indicates a Message phase when asserted, and Command or Data phase when not asserted.
/RST	A4	Reset – Signal is interpreted as a hard reset and will clear all commands pending on the SCSI bus.
/ACK	B4	Acknowledge – Indicate a byte is ready for or was received from the Target.
/BSY	C4	Busy – Handshake signal used during arbitration.
/SATN	E4	Attention – This line is activated when a special condition occurs.
/WIDEPS	B5	Wide Present – When Low, indicates that a wide (16-bit) cable is present.
TERMPWR	C5, D5	Termination Power.
/SDPH, /SDPL	A8, B6	SCSI High/Low Parity – Provide odd parity for data lines.

11.2.3 Video Interface

Signal	Pin Assignation (J4)	Description
VSDA	D9	Video serial data line (video I2C)
VSCL	A10	Video serial clock line (video I2C)
HSYNC	B10	Horizontal sync line
VSYNC	C10	Vertical sync line
RED	D10	Analog Red video signal
GREEN	E10	Analog Green video signal
BLUE	A11	Analog Blue video signal

11.2.4 Ethernet 0 Interface

Signal	Pin Assignation (J4)	Description
ETX+0	A16	Ethernet 0 High Transmit Data line
ETX-0	B16	Ethernet 0 Low Transmit Data line
ERX+0	C16	Ethernet 0 High Receive Data line
ERX-0	D16	Ethernet 0 Low Receive Data line

11.2.5 EIDE 1 Interface

Signal	Pin Assignation (J4)	Description
/BRSTDRV	A17	
SDD 0-15	B20, E19, C19, A19, D18, B18, E17, C17, D17, A18, C18, E18, B19, D19, A20, C20	Sec. Disk Data – These signals are used to transfer data to or from the IDE device.
SDREQ	A21	Sec. Disk DMA Request - This signal is directly driven from the IDE device DMARQ signal. It is asserted by the IDE device to request a data transfer.
/SDIOW	C21	Sec. Disk I/O Write – In normal IDE mode, this is the command to the IDE device that it may latch data from SDD lines.
/SDIOR	E21	Sec. Disk I/O Read – In normal IDE mode, this is the command to the IDE device that it may drive data on SDD lines.
SIORDY	B22	Sec. I/O Channel Ready – In normal mode, this input signal is driven directly by the corresponding IDE device IORDY signal.
/SDDACK	D22	Sec. DMA Acknowledge – This signal directly drives the IDE device /DMACK signal. It is asserted to indicate to IDE DMA slave devices that a given data transfer cycle is a DMA data transfer cycle.
IRQ15	E22	
/IOCS16	A23	
SDA 0-2	D23, B23, E23	Sec. Disk Address – These signals indicates which byte in either the ATA command block or control block is being addressed.
/SCS1, /SCS3	A24, B24	Secondary Chip Select - For ATA control register.
SEC-PD1	C24	
/FAL1	E24	

Enhanced IDE 1 (EIDE 1) is assigned to the Secondary EIDE logical interface. It supports directly two IDE devices configured as Master and Slave devices.

11.3 J5 SIGNAL SPECIFICATION

11.3.1 EIDE 0 Interface

Signal	Pin Assignation (J5)	Description
/BRSTDRV	A1	
/BRSTDRV	B1	
PDD 0-15	B4, E3, C3, A3, D2, B2, E1, C1, D1, A2, C2, E2, B3, D3, A4, D4	Prim. Disk Data – These signals are used to transfer data to or from the IDE device.
PDREQ	A5	Prim. Disk DMA Request - This signal is directly driven from the IDE device DMARQ signal. It is asserted by the IDE device to request a data transfer.
/PDIOW	C5	Prim. Disk I/O Write – In normal IDE mode, this is the command to the IDE device that it may latch data from SDD lines.
/PDIOR	E5	Prim. Disk I/O Read – In normal IDE mode, this is the command to the IDE device that it may drive data on SDD lines.
PIORDY	B5	Prim. I/O Channel Ready – In normal mode, this input signal is driven directly by the corresponding IDE device IORDY signal.
/PDDACK	D5	Prim. DMA Acknowledge – This signal directly drives the IDE device /DMACK signal. It is asserted to indicate to IDE DMA slave devices that a given data transfer cycle is a DMA data transfer cycle.
IRQ14	E4	IRQ14 line
/IOCS16	A6	IOCS16 line
PDA 0-2	D6, C7, E6	Prim. Disk Address – These signals indicates which byte in either the ATA command block or control block is being addressed.
/PCS1, /PCS3	A7, B7	
PRI-PD1	D7	
/PDIAG	C6	

11.3.2 USB 0 and 1 Interfaces

Signal	Pin Assignation (J5)	Description
USBD1-0 (+/-)	B18, C18, D19, E19	USB Data – Differential data path for USB 0 and 1 ports
USBG 1-0	B19, D18	USB Ground – Differential ground reference for USB 0 and 1 ports
USBV 1-0	C19, E18	USB Voltage – Differential power level for USB 0 and 1 ports

11.3.3 Floppy Disk Interface

Signal	Pin Assignation (J5)	Description
/FD-DRVEN 0-1	E7, A8	Drive 0-1 density select
/FD-INDEX	B8	Index
/FD-MTR 0-1	C8, A9	Motor 0-1 enable
/FD-DS 0-1	E8, D8	Drive 0-1 select
/FD-DIR	B9	Direction
/FD-STEP	C9	Step pulse
/FD-WDATA	D9	Write disk data
/FD-WGATE	E9	Write gate
/FD-TRK0	A10	Track 0
/FD-WRTPRT	B10	Write protected
/FD-RDATA	C10	Read disk data
/FD-HDSEL	D10	Head select
/FD-DSKCHG	E10	Disk change

11.3.4 Serial Port 2

Signal	Pin Assignation (J5)	Description
/JDCD2	A11	Data Carrier Detect
JRXD2	C11	Receive Data
/JDSR2	D11	Data Set Ready
JTXD2	E11	Transmit Data
/JRTS2	A12	Ready To Send
/JCTS2	B12	Clear To Send
/JRI2	C12	Ring Indicator
/JDTR2	E12	Data Terminal Ready

11.3.5 Serial Port 1

Signal	Pin Assignation (J5)	Description
/JDCD1	A13	Data Carrier Detect
JRXD1	C13	Receive Data
/JDSR1	D13	Data Set Ready
JTXD1	E13	Transmit Data
/JRTS1	A14	Ready To Send
/JCTS1	B14	Clear To Send
/JRI1	C14	Ring Indicator
/JDTR1	E14	Data Terminal Ready

11.3.6 Parallel Port

Signal	Pin Assignation (J5)	Description
SLCT	A15	Printer select
PE	B15	Paper end
BUSY	C15	Busy signal
/ACK	D15	Acknowledge handshake
PD 0-7	E17, C17, A17, D16, C16, B16, A16, E15	Parallel port data bus
/SLCTIN	E16	Printer select
ALF	A18	Auto line feed
/INIT	B17	Initiate output
/ERR	D17	Error at printer
/STB	A19	Strobe signal

11.3.7 Miscellaneous Signals

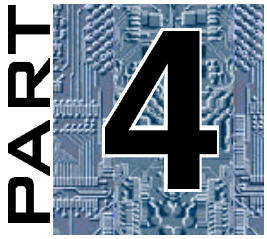
Signal	Pin Assignation (J5)	Description
/SMBDATA	B20	Onboard SMbus data
/SMBALERT	C20	Onboard SMbus Alert (CPU overheating)
SMBCLK	E20	Onboard SMbus Clock
/PBRST	A22	Reset
/DIAG-OC	C22	Reserved
SPK-OUT	E22	Speaker signal

11.3.8 Keyboard Interface

Signal	Pin Assignation (J5)	Description
KDATA	A21	Keyboard data
KCLK	B21	Keyboard clock
VCC-KBD	C21	Keyboard power

11.3.9 Mouse Interface

Signal	Pin Assignation (J5)	Description
MDATA	D21	Mouse data
MCLK	E21	Mouse clock



SOFTWARE SETUPS

12. AWARD SETUP PROGRAM

13. UPDATING THE BIOS WITH UPGBIOS

14. VT100 MODE

12. AWARD SETUP PROGRAM

Normally the software setup will follow all system hardware connections in order to configure controllers and installed devices.

Also, software setup should come before any operating systems and drivers are installed.

NOTES

Make sure you setup the AWARD software prior to installing your operating system and your drivers.

For systems that need the BIOS to first attempt to boot from LAN, follow these steps:

1. Set the Boot From LAN First option to Enabled in the AWARD Setup's BIOS Features Setup

2. Follow the complete procedure in the Boot From LAN utility diskette.

12.1 ACCESSING THE AWARD SETUP PROGRAM

The system BIOS (Basic Input Output System) provides an interface between the operating system and the hardware of the TEK-CPCI-1003 single board computer. The interface provided by AWARD is 100% IBM AT compatible. All functions accept similar inputs as IBM and provide the same results, although the program code itself is different.

The TEK-CPCI-1003 uses the AWARD Setup program, a setup utility in flash memory that is accessed by pressing the DELETE key at the appropriate time during system boot. This utility is used to set configuration data in CMOS RAM.



CAUTION

Before modifying CMOS setup parameters, ensure that the W4 battery selection jumper is installed to enable the CMOS battery back up (please refer to Section 6.2).

To run the AWARD Setup program incorporated in the ROM BIOS:

1. Turn on or reboot the system.
2. Hit the DELETE key before or when the message - "Press **DEL** To Enter SETUP" appears near the bottom of the screen.
3. The main menu of the AWARD BIOS CMOS Setup Utility appears on the screen.

```
                    ROM PCI/ISA BIOS (2A69LB39)
                    CMOS SETUP UTILITY
                    AWARD SOFTWARE, INC.

STANDARD CMOS SETUP                 LOAD BIOS DEFAULTS
BIOS FEATURES SETUP                 LOAD SETUP DEFAULTS
CHIPSET FEATURES SETUP              SUPERVISOR PASSWORD
POWER MANAGEMENT SETUP              USER PASSWORD
THERMAL MANAGEMENT SETUP            IDE HDD AUTO DETECTION
PNP/PCI CONFIGURATION               SAVE & EXIT SETUP
INTEGRATED PERIPHERALS              EXIT WITHOUT SAVING

Esc     :   Quit                    ↑ ↓ → ←     :   Select Item
F10     :   Save & Exit Setup       (Shift)F2   :   Change Color

                    Time, Date, Hard Disk Type . . .
```

12.2 USING AWARD SETUP PROGRAM

The arrow keys (↑ ↓ → ←) are used to highlight items on the menu and the PAGEUP and PAGEDOWN keys are used to change the entry values for the highlighted item. To select an entry, press the ENTER key. Also, you can press the F1 key to obtain help information or the ESC key to leave an option, close a menu or to quit the program.

12.2.1 Using AWARD Setup Program

To navigate in the Setup program, proceed as follows:

Key	Function
↑	Moves to previous item.
↓	Moves to next item.
←	Moves to the item in the left hand.
→	Moves to the item in the right hand.
ESC	In the Main Menu: Quits program (Answer 'Y' to save changes into CMOS). When in other screens: Exits and returns to the Main Menu.
PAGEUP or +	Increases the numeric value or changes value.
PAGEDOWN or -	Decreases the numeric value or changes value.
F5	In the Main Menu: Restores the previous setup values for all the BIOS parameters (except Standard CMOS) which were displayed when you entered the program. In BIOS Features Setup, Chipset Features Setup, Power Management Setup, Thermal Management Setup, PNP/PCI Setup or Integrated Peripherals Setup: Restores the previous setup values for that setup screen only.
F6	In the Main Menu: Loads the BIOS Defaults of all the BIOS parameters (except Standard CMOS). The BIOS Defaults are fail safe settings that consist of the safest set of parameters. In BIOS Features Setup, Chipset Features Setup, Power Management Setup, Thermal Management Setup, PNP/PCI Setup or Integrated Peripherals Setup: Loads the BIOS Defaults for all the BIOS parameters for that setup screen only.
F7	In the Main Menu: Loads the Setup Defaults for all the BIOS parameters (except Standard CMOS). In BIOS Features Setup, Chipset Features Setup, Power Management Setup, Thermal Management Setup, PNP/PCI Setup or Integrated Peripherals Setup: Loads the Setup Defaults for all the BIOS parameters for that setup screen only.
F10	In the Main Menu: Saves all the CMOS changes.

12.2.2 Available Features

The Main Menu includes the following categories:

Standard CMOS Setup	This Setup page includes all the items in a standard, AT-compatible BIOS (date, time, hard disk type, floppy disk type, video adapter type, and memory…).
BIOS Features Setup	This Setup page includes all the items of AWARD's special enhanced features.
Chipset Features Setup	This Setup page includes all the items of the chipset's special features.
Power Management Setup	This Setup page sets power conservation options.
Thermal Management Setup	This Setup page sets thermal management options.
PnP/PCI Configuration	This Setup page sets plug and play and PCI configuration options.
Integrated Peripherals	I/O susbsystems that depend on the integrated peripherals controller in your system.
Load Bios Defaults	The BIOS defaults are fail safe settings which consist of the safest set of parameters. Use them if the system is behaving erratically. They should always work but do not provide optimal system performance.
Load Setup Defaults	The Setup defaults are optimal settings that provide optimum performance for all devices and system features. If CMOS RAM is corrupted, the Setup defaults are loaded automatically.
Supervisor/User Password Setting	Change, set, or disable password. It allows you to limit access to the system and the Setup, or just to the Setup.
IDE HDD Auto Detection	Automatically detect and configure IDE hard disk parameters.

12.2.3 Save & Exit Operations

Use one of the following options available from the Main Menu:

Save & Exit	After having modified the AWARD Setup, you can save the configuration in CMOS RAM and the Flash BIOS, by selecting this option.
Exit Without Saving	This option is used to exit AWARD Setup without saving the configuration to CMOS RAM.

12.3 SETUPS

Whenever you are not sure about a certain setting, you may refer to the list of default values. The list of defaults is provided in the event that a value has been changed and one wishes to set this option to its original value. Loading the BIOS or SETUP defaults will affect all the options in this screen (or all parameters if defaults are loaded from the Main Menu) and will reset options previously altered.

- The BIOS Default settings consist of the safest set of parameters. Use them if the system is behaving erratically. They should always work but do not provide optimal system performance.

- The SETUP Default values provide optimum performance settings for all devices and system features.

CAUTION

These parameters have been provided to give control over the system. However, the values for these options should be changed only if the user has a full understanding of the timing relationships involved.

12.3.1 Standard CMOS Setup

This part of the setup allows you to set the time, date, hard disk type, types of floppy drives and video type.

Date/Time	The current values for each category are displayed. Enter new values through the keyboard.
Hard Disks	Two IDE controllers are defined on the board. The Primary and Secondary controller can have two disks: Master Disk or Slave Disk. The disks are bootable in this order: 1) Primary Master, 2) Primary Slave, 3) Secondary Master, and 4) Secondary Slave. The W5 jumper configures the CompactFlash disk as Secondary Master or Secondary Slave device. Only three settings are available for the hard disk type: Auto, 47 (user defined) and None. Type 1 to 46 are not predefined in the system: Use auto-detect or enter the parameters for the type in the user-defined type 47.
Drive A / Drive B	Select the type of floppy disk installed for drive A and drive B.
Video	This option specifies the basic type of display adapter card installed in the system.
Halt on	This option specifies the type of errors that will stop the system during the BIOS booting procedure. A message asks that you press F1 to continue or press the DELETE key to enter Setup. The settings are: All errors, No errors, All but keyboard, All but diskette, and All but disk/key (default setting).
Memory	This display-only option indicates the amount of Base, Extended and other types of memory installed in the system.

12.3.2 BIOS Features Setup

This part of the setup handles options and features such as boot sequence, NUM LOCK, security options, shadowing, …

Option	BIOS Default	Setup Default	Possible Settings	Description
Virus Warning	Dis.	Dis.	En., Dis.	When Enabled, you receive a warning message if a program (specifically, a virus) attempts to write to the boot sector or the partition table of the hard disk drive. You should then run an anti-virus program. Keep in mind that this feature protects only the boot sector, not the entire hard drive. **Note: Many disk diagnostic programs and OS setups (e.g., Win95 setup), that access the boot sector table, can trigger the virus warning message. If you plan to run such a program, we recommend that you first disable the virus warning.**
CPU Internal Cache	Dis.	En.	En., Dis.	Enables or Disables the CPU Internal Cache (L1 cache).
External Cache	Dis.	En.	En., Dis.	Enables or Disables the External Cache (L2 cache).
CPU L2 Cache ECC Checking	Dis.	En.	En., Dis.	Enables or Disables ECC Checking for L2 cache.
Quick Power On Self Test	Dis.	En.	En., Dis.	Select Enabled to reduce the amount of time required running the power-on self-test (POST). A quick POST skips certain steps. We recommend that you enable quick POST to save time, since most major OS do their own tests
Boot From LAN First	Dis.	Dis.	En., Dis.	If Enabled, the BIOS will first attempt to boot from the LAN. The complete procedure for this function is available on the Boot From LAN utility diskette.
Boot Sequence	A,C, SCSI	C,A, SCSI	See description	This option defines the searching order in the BIOS for the boot device(s). Options are listed as follows: A, C, SCSI ; C, A, SCSI ; C, CDROM, A ; CDROM, C, A ; D, A, SCSI ; E, A, SCSI ; F, A, SCSI ; SCSI, A, C ; SCSI, C, A; C only; LS/ZIP,C.
Floppy Disk Access Control	R/W	R/W.	R/W, Read only	Select R/W to enable Read and Writes operations for the floppy disk drive.
Drive A Boot Permit	En	En.	En., Dis.	Select En. to enable Drive A boot in the bootup sequence. If disabled, the drive is passed over.
Swap Floppy Drive	Dis.	Dis.	En., Dis.	Selecting Enabled assigns physical drive B to logical drive A, and physical drive A to logical drive B. If there is only one floppy on the system, it could be assigned to B with this option.
Boot Up Floppy Seek	En.	Dis.	En., Dis.	When Enabled, the BIOS tests (seeks) floppy drives to determine whether they have 40 or 80 tracks. Only 360KB floppy drives have 40 tracks; drives with 720KB, 1.2MB, and 1.44MB capacity all have 80 tracks. Because very few modern PCs have 40 track floppy drives, we recommend that you set this field to “Disabled” to save time.
Floppy FIFO Control	Dis.	Dis.	En., Dis.	
Drive A Boot Permit	Dis.	Dis.	En., Dis.	
FD Write Protect	Dis.	Dis.	En., Dis.	When Enabled, write access on floppy disk is not allowed
HD Write Protect	Dis.	Dis.	En., Dis.	When Enabled, write access on hard disk is not allowed
HDD S.M.A.R.T. Capability	Dis.	En.	En., Dis.	Allows the BIOS to use the S.M.A.R.T. (System Management and Reporting Technologies) protocol for reporting server system information over a network.
Boot Up NumLock Status	On	On	On, Off	Toggle between On or Off to control the state of the NumLock key when the system boots. When toggled On, the numeric keypad generates numbers instead of controlling cursor operations.
Gate A20 Option	Norm.	Fast	Normal, Fast	When Fast, enables fast switching of Gate A20 via the 440BX chipset, instead of the keyboard controller.

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BIOS Features Setup (Continued)

Option	BIOS Default	Setup Default	Possible Settings	Description
Typematic Rate Setting	Dis.	En.	En., Dis.	When Disabled, the following Typematic Rate and Typematic Delay are irrelevant. Keystrokes repeat at a rate determined by the keyboard controller in your system. When Enabled, you can select a typematic rate and a typematic delay.
Typematic Rate (Chars/Sec)	30	30	6 ..30 char. Per sec.	When Enabled, you can select a typematic rate (the rate at which characters repeat when you hold down a key).
Typematic Delay (Msec)	250	250	250, 500, 750, 1000 ms	When Enabled, you can select a typematic delay (the delay before keystrokes begin to repeat).
Security Option	Setup	Setup	Setup, System	If you have set a password, select whether the password is required every time the system boots ("System" option), or only when you enter Setup ("Setup" option).
PCI/VGA Palette Snoop	Dis.	Dis.	En., Dis.	Palette snooping allows multiple VGA devices operating on different buses to handle data from the CPU on each set of palette registers. When set to Enabled, data read and written by the CPU is directed to both the PCI VGA device's palette registers and the ISA VGA device's palette registers, permitting the palette registers of both to be identical. When Disabled, data read and written by the CPU is only directed to the PCI VGA device's palette registers.
OS Select For DRAM > 64MB	Non-OS2	Non-OS2	Non-OS/2, OS/2	Select OS2 only if you are running OS/2 with greater than 64MB of RAM.
Video BIOS Shadow	Dis.	En.	En., Dis.	Software that resides in a read-only memory (ROM) chip on a device is called *firmware*. Award permits shadowing of firmware such as the system BIOS, video BIOS, and similar operating instructions that come with some expansion peripherals. Shadowing copies from ROM into system RAM, where the CPU can read it through the 16-bit or 32-bit DRAM bus. Firmware not shadowed must be read by the system through the 8-bit X-bus. Shadowing improves the performance of the system BIOS and similar firmware for expansion peripherals. Enable shadowing into each section of memory separately. Many system designers hardwire shadowing of the system BIOS and eliminate a System BIOS Shadow option. Note that on a PCI VGA card (onboard or offboard), the VGA BIOS is always shadowed. Video BIOS shadows into memory area C0000 plus the VGA BIOS size. The remaining areas between C0000 and DFFFF shown on the BIOS Features Setup screen may be occupied by other expansion card firmware. If an expansion peripheral in your system contains ROM-based firmware, you need to know the address range the ROM occupies to shadow it into the correct area of RAM.
C8000-CBFFF Shadow	Dis.	Dis.	En., Dis.	
CC000-CFFFF Shadow	Dis.	Dis.	En., Dis.	
D0000-D3FFF Shadow	Dis.	Dis.	En., Dis.	
D4000-D7FFF Shadow	Dis.	Dis.	En., Dis.	
D8000-DBFFF Shadow	Dis.	Dis.	En., Dis.	
DC000-DFFFF Shadow	Dis.	Dis.	En., Dis.	
Watchdog Timer	Dis.	Dis.	En., Dis.	Enable this option to toggle the watchdog with the watchdog timer during the BIOS bootup.
Watchdog After POST	Dis.	Dis.	En., Dis.	When the watchdog is set, use this option to continue toggling the watchdog with the watchdog timer after the bootup.
Save CMOS in Flash	Dis.	Dis.	En., Dis.	When Enabled, the CMOS RAM Setup will be restored from the Flash BIOS at each power up. If the battery fails, only the date and time could be lost.

12.3.3 Chipset Features Setup

This part of the setup allows you to define chipset-specific options and features.

Option	BIOS Default	Setup Default	Possible Settings	Description
SDRAM CAS Latency Time	3	3	2, 3	For 100MHz SDRAM, set this option to 2 (clocks). For 66MHz SDRAM, set this option to 3 (clocks).
DRAM Data Integrity Mode	Non-ECC	Non-ECC	ECC, Non-ECC	When set to ECC, allows auto-correction of the data read from memory. It does not scrub the memory. The ECC error flags' status register and the error pointer are updated if error correction occurs in this mode. When set to Non-ECC, no error checking or error reporting is done.
System BIOS Cacheable	Dis.	En.	En., Dis.	Selecting Enabled allows caching of the system BIOS ROM at F0000h-FFFFFh, resulting in better system performance. However, if any program writes to this memory area, a system error may occur.
Video BIOS Cacheable	Dis.	En.	En., Dis.	Selecting Enabled allows caching of the video BIOS ROM at C0000h plus the VGA BIOS size, resulting in better video performance. However, in any program writes to this memory area, a system error may occur.
Video RAM Cacheable	Dis.	En.	En., Dis.	When Enabled, video memory region is cacheable. Some offboard video card drivers may behave strangely; in such a case, disable this option.
8 Bit I/O Recovery Time	3	1	1, 2, 3, 4, 5, 6, 7, 8, NA	The I/O recovery mechanism adds bus clock cycles between PCI-originated I/O cycles to the ISA bus. This delay takes place because the PCI bus is so much faster than the ISA bus. These two fields let you add recovery time (in bus clock cycles) for 16-bit and 8-bit I/O.
16 Bit I/O Recovery Time	2	1	1, 2, 3, 4, NA	
Memory Hole At 15M-16M	Dis.	Dis.	En., Dis.	You can reserve this area of system memory for ISA adapter ROM. When this area is reserved, it cannot be cached. The user information of peripherals that need to use this area of system memory usually discusses their memory requirements.
Passive Release	En.	En.	En., Dis.	When Enabled, CPU to PCI bus accesses are allowed during passive release otherwise the arbiter only accepts another PCI master access to local DRAM.
Delayed Transaction	En.	En.	En., Dis.	The chipset has an embedded 32-bit posted write buffer to support delay transactions cycles. Select Enabled to support compliance with PCI specifications version 2.1.
AGP Aperture Size (MB)	64	64	1, 8, ...256	This option determines the aperture size reserved to the Accelerated Graphics Port (AGP).
Supervisor I/O Base Addr.	190h	190h	190h, 290h, 390h	This option determines the base address for the Supervisor I/O Register, which is used for such functions as power fail detection and the watchdog timer.

12.3.4 Power Management Setup

This part of the setup configures power conservation options.

Option	BIOS Default	Setup Default	Possible Settings	Description
ACPI Function	Dis.	En.	En., Dis.	When Enabled and the OS supports ACPI or OSPM (e.g., Win98, Window NT 5), power management functionality moves to the OS. **Note: When Enabled, all other options in the Power Management Setup will not be used.**
Power Management	Dis.	User Def.	Min Saving, Max Saving, User Define, Disable	This option allows you to select the type (or degree) of power saving for Doze, Standby, and Suspend modes. Max Saving: Maximum power savings. Inactivity period is 1 minute in each mode. Min Saving: Minimum power savings. Inactivity period is the maximum setting in each mode (1 hour for Doze, Standby and Suspend). User Define: Set each mode individually. Select time-out periods in the PM Timers section (see below).
PM Control by APM	Yes	Yes	Yes, No	If Yes, the OS will control the PM by APM calls. If No, the BIOS will control the PM and APM calls from the OS will be ignored.
Video Off Method	V/H SYNC +Blk	V/H SYNC +Blk	V/H SYNC+Blank, DPMS, Blank Screen	Determines the manner in which the monitor is blanked. V/H SYNC + Blank: System turns off vertical and horizontal synchronization ports and writes blanks to the video buffer. DPMS Support: Select this option if your monitor supports the Display Power Management Signaling (DPMS) standard of the Video Electronics Standards Association (VESA). Use the software supplied for your video subsystem to select video power management values. Blank Screen: System only writes blanks to the video buffer.
Video Off After	Stand by	Stand by	Doze, Standby, Suspend, NA	As the system moves from lesser to greater power-saving modes, select the mode in which you want the monitor to blank.
Modem Use IRQ	3	3	N/A, 3, 4, 5, 7, 9, 10, 11	Name the IRQ line assigned to the modem (if any) on your system. Activity of the selected IRQ always awakens the system.
PM Timers:				The following modes are Green PC power saving functions. They are user-configurable only during User Defined Power Management mode.
Doze Mode	Dis.	20 Min	1 .. 40 Min, 1 Hour, Disab	After the selected period of system inactivity (1 minute to 1 hour), the CPU clock runs at lower speed while all other devices still operate at full speed.
Standby Mode	Dis.	40 Min	1 .. 40 Min, 1 Hour, Disab.	After entering Doze mode and the selected period of system inactivity (1 minute to 1 hour) has elapsed, the fixed disk drive and the video shut off while all other devices still operate at full speed.
Suspend Mode	Dis.	1 hour	1 .. 40 Min, 1 Hour, Disab.	After entering Standby mode and the selected period of system inactivity (1 minute to 1 hour) has elapsed, all devices except the CPU shut off.
HDD Power Down	Dis	15 min	1, 2, 3, (…), 15 Min, Disab.	After the selected period of drive inactivity (1 to 15 minutes), the hard disk drive powers down while all other devices remain active. The HDD power down mode is only available if the hard drive has this capability.
HDD Down When Suspend	Dis	En.	En. , Dis.	When set, after entering Suspend mode, the hard disk drive powers down.

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Power Management Setup (Continued)

Option	BIOS Default	Setup Default	Possible Settings	Description
Throttle Duty Cycle	75.0%	75.0%	12.5%, 25.0%, 37.5%, 50.0%, 62.5%, 75.0%	When the system enters Doze mode, the CPU clock runs only part of the time. You may select the percentage of time that the clock does not run.
VGA Active Monitor	En.	En.	En., Dis.	When Enabled, any video activity restarts the global timer for Standby mode.
Resume by Ring	Dis.	En.	En., Dis.	When Enabled and a modem is connected to a COM port, allows a modem ring to re-activate the CPU when in Suspend mode.
Resume by Alarm	Dis.	Dis.	En., Dis.	When Enabled, allows setup of a time to re-activate the CPU when in Suspend mode with the options Date (of Month) Alarm and Time (hh:mm:ss) Alarm. **Note: The IRQ 8 Break Suspend option in this setup screen must be Enabled to use the RTC alarm.**
Date (of Month) Alarm	-	-	From 0 to 31	This option appears only if Resume by Alarm is enabled. It specifies the date in the month for the RTC alarm.
Time (hh:mm:ss) Alarm	-	-	from 0:0:0 to 23:59:59	This option appears only if Resume by Alarm is enabled. It specifies time of day for the RTC alarm.
IRQ 8 Break Suspend	Dis.	En.	En., Dis.	When Enabled, the RTC alarm interrupt is monitored to allow an interrupt to awaken the system when in Doze, Standby or Suspend Mode.
Reload Global Timer Events:				When any of the options below is Enabled, monitoring of the interrupt will occur to allow an interrupt to awaken the system when in Doze, Standby or Suspend Mode.
IRQ[3-7,9-15], NMI	Dis.	En.	En., Dis.	
Primary IDE 0	Dis.	Dis.	En., Dis.	
Primary IDE 1	Dis.	Dis.	En., Dis.	
Secondary IDE 0	Dis.	Dis.	En., Dis.	
Secondary IDE 1	Dis.	Dis.	En., Dis.	
Floppy Disk	Dis.	Dis.	En., Dis.	
Serial Port	En.	En.	En., Dis.	
Parallel Port	Dis.	Dis.	En., Dis.	

12.3.5 Thermal Management Setup

This part of the setup configures thermal management options.

Option	BIOS Default	Setup Default	Possible Settings	Description
Thermal Management	Dis.	Dis.	En., Dis.	When this option is enabled, the CPU temperature is monitored. Whenever the CPU overheats, the CPU slows down to lower the temperature.
CPU Temperature (°C)	-	-	Varies	Displays the current CPU temperature, when Thermal Management is enabled.
CPU Low Temp. (°C)	T.B.D.	T.B.D.	T.B.D.	The CPU will be slowed down when it reaches the selected "CPU Overheat (°C)" temperature or higher. Full speed will be resumed when the temperature comes down to the selected "CPU Low Temp. (°C)".
CPU Overheat (°C)	T.B.D.	T.B.D.	T.B.D.	
CPU Case Temp. (°C)	-	-	Varies	Displays the current CPU case temperature, when Thermal Management is enabled.
CPU Case Low Temp. (°C)	T.B.D.	T.B.D.	T.B.D.	The CPU will be slowed down when it reaches the selected "CPU Case Overheat (°C)" temperature or higher. Full speed will be resumed when the temperature comes down to the selected "CPU Case Low Temp. (°C)".
CPU Case Overheat (°C)	T.B.D.	T.B.D.	T.B.D.	

12.3.6 PnP/PCI Configuration

This part of the setup configures PnP/PCI options.

Option	BIOS Default	Setup Default	Possible Settings	Description
PNP OS Installed	No	Yes	Yes, No	If the operating system (OS) is Plug and Play (for example Windows 95), select "Yes" if you want the OS to allocate resources according to Plug and Play standards, or "No" if you want the same resource allocations at every system boot-up. Select "No" when the OS is not Plug and Play (for example, DOS).
Resources Controlled By	Auto	Man.	Auto, Man.	The Award Plug and Play BIOS can automatically configure all the boot and Plug and Play-compatible devices. If you select Auto, all the interrupt requests (IRQs) and DMA assignment fields disappear, as the BIOS automatically assigns them.
Reset Configuration Data	Dis.	Dis.	En., Dis.	Normally, you leave this field Disabled. Select Enabled to reset Extended System Configuration Data (ESCD) when you exit Setup if you have installed a new add-on and the system reconfiguration has caused such a serious conflict that the operating system cannot boot.
IRQ *n* Assigned To	PCI/ ISA PnP	PCI/ ISA PnP	PCI/ISA PnP, Legacy ISA	When resources are controlled manually, assign each system interrupt as one of the following types, depending on the type of device using the interrupt: Legacy ISA: Devices compliant with the original PC AT bus specification, requiring a specific interrupt, such as IRQ4 for serial port 1. PCI/ISA PnP: Devices compliant with the Plug and Play standard, whether designed for PCI or ISA bus architecture. When Legacy ISA is selected for an IRQ line, this resource will not be available for PCI/ISA PnP.
DMA *n* Assigned To	PCI/ ISA PnP	PCI/ ISA PnP	PCI/ISA PnP, Legacy ISA	When resources are controlled manually, assign each system DMA channel as one of the following types, depending on the type of device using the interrupt: Legacy ISA: Devices compliant with the original PC AT bus specification, requiring a specific DMA channel. PCI/ISA PnP: Devices compliant with the Plug and Play standard, whether designed for PCI or ISA bus architecture. When Legacy ISA is selected for a DMA channel, this resource will not be available for PCI/ISA PnP.
Used MEM Base Address	N/A	N/A	N/A, C800, CC00, D000, D400, D800, DC00	Select a base address for the memory area used by any peripheral that requires high memory.
Assign IRQ for USB	En.	En.	En. , Dis.	Select Enable to assign an IRQ (IRQ11) to USB features.
PCI Latency Timer	En.	En.	En. , Dis.	Enable this option to set a mechanism for ensuring that a PCI device does not extend the access latency beyond a specific value.
Used MEM Length	8K	8K	8K, 16K, 32K, 64K	Select a length for the memory area specified in the previous field. This field does not appear if no base address is specified.

12.3.7 Integrated Peripherals

This part of the setup configures Integrated Peripherals options.

Option	BIOS Default	Setup Default	Possible Settings	Description
IDE HDD Block Mode	Dis.	En.	En., Dis.	Block mode is also called block transfer, multiple commands, or multiple sector read/write. If your IDE hard drive supports block mode (most new drives do), select Enabled for automatic detection of the optimal number of block read/writes per sector the drive can support.
IDE Primary/Secondary Master/Slave PIO	Auto	Auto	Mode 0, Mode 1, Mode 2, Mode 3, Mode 4, Auto	These options only appear if the On-Chip Primary/Secondary PCI IDE options are enabled. The four IDE PIO (Programmed Input/Output) fields let you set a PIO mode (0-4) for each of the four IDE devices that the onboard IDE interface supports. Modes 0 through 4 provide successively increased performance and speed. In Auto mode, the system automatically determines the best mode for each device. If you select a mode that the drive does not support, it may not work, so choose a lesser value or Auto to see the best mode for the drive.
IDE Primary/Secondary Master/Slave UDMA	Dis.	Auto	Auto, Dis.	Ultra DMA/33 implementation is possible only if your IDE hard drive supports it and the operating environment includes a DMA driver (Windows 95 OSR2 or a third-party IDE bus master driver). If your hard drive and your system software both support Ultra DMA/33, select Auto to enable BIOS support.
On-Chip Primary/Secondary PCI IDE	En.	En.	En., Dis.	The integrated peripheral controller contains an IDE interface with support for two IDE channels. Select Enabled to activate each channel separately.
Onboard PCI SCSI Chip	En.	En.	En., Dis.`	Enables/disables the onboard SCSI controller
Ethernet 1 and 2	En.	En.	En., Dis.	Enables/disables onboard Ethernet 1 or 2 controller.
USB Keyboard Support	Dis.	Dis.	En., Dis.	Select Enabled, if your system contains an Universal Serial Bus (USB) controller and you have an USB keyboard. **Note: This option is for DOS and BIOS support only (Win95 has its own drivers).**
Onboard FDC Controller	En.	En.	En., Dis.	Select Enabled if your system has a floppy disk controller (FDC) installed on the system board and you wish to use it. If you install an add-in FDC or the system has no floppy drive, select Disabled in this field.
Onboard Serial Ports 1 and 3	Auto	Auto	Dis., Auto 3F8/IRQ4, 2F8/IRQ3, 3E8/IRQ4, 2E8/IRQ3,	Select a COM port address and IRQ# for the first and second serial ports.
Onboard Serial Port 2	2F8	2F8	Dis., 3E8, 2E8, 3F8, 2F8	Select a COM port address for the serial port #2.
IRQ Line	IRQ4	IRQ4	IRQ 3, 4, 5, 7	Select an IRQ line for the serial port #2.
Onboard Serial Port 4	3E8	3E8	Dis., 3E8, 2E8, 3F8, 2F8	Select a COM port address for the serial port #4.
IRQ Line	IRQ3	IRQ3	IRQ 3, 4, 5, 7	Select an IRQ line for the serial port #4.
Serial Port 3 Mode	RS-232	RS-232	IrDA, RS-232, RS-422, RS-485	Select the operation mode for Serial Port 3.

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Integrated Peripherals (Continued)

Option	BIOS Default	Setup Default	Possible Settings	Description
UART 3	Std	Std	Standard, IrDA 1.0, ISK-IR, IrDA 1.1	Selects the operating mode for UART 3.
Duplex Select	Half	Half	Half, Full	IrDA 1.0, ISK-IR, IrDA 1.1 modes only: Select Half for one communication at a time, Full for simultaneous communication.
TxD, RxD Active	Hi/Lo	Hi/Lo	Hi/Hi, Hi/Lo, Lo/Hi, Lo/Lo	IrDA 1.0, ISK-IR, IrDA 1.1 modes only: Determines whether the transmit signal (TxD) and the receive signals are active low (Lo) or active high (Hi)
IRRX Mode Select	IRMod	IRMod	IRMode, IRRX3	IrDA 1.1 mode only: Select operating protocol when in IrDA 1.1 mode.
VT100 Mode on Serial Port 1 or 2	1	1	1, 2, 3, 4	Selects the serial port for VT100 mode.
Onboard Parallel Port	378 /IRQ7	378/ IRQ7	Dis., 3BC/IRQ7, 378/IRQ7, 278/IRQ5,	Select a LPT address and IRQ# for the physical parallel (printer) port.
Parallel Port Mode	ECP+ EPP1.9	ECP+ EPP1.9	Normal, SPP, EPP1.9+SPP, ECP, ECP+EPP1.9, EPP1.7+SPP, ECP+EPP1.7	Select an operating mode for the onboard parallel port. Select ECP or EPP unless you are certain both your hardware and software does not support ECP or EPP mode. Parallel port modes are defined in section 14.2.2.
ECP Mode Use DMA	3	3	1, 3	Select a DMA channel for the port.

13. UPDATING THE BIOS WITH UPGBIOS

UPGBIOS is an utility that allows you to take BIOS files from a disk and update the Boot Block Flash BIOS with them.

The command line format is as follows:

UPGBIOS [/ALL filename] [/VGA VGA_filename] [/?]
[/h]

where:

filename	is the name of the 256KB BIOS file containing all BIOS files. The .BIN extension is used for all BIOS files in a single file.
VGA_filename	is the name of the 64KB file (or less) containing the video BIOS. It will accept various extensions: .VGA, .BFP (flat panel), ...
? or **h**	displays instructions on using the UPGBIOS program.

Please note that the UPGBIOS utility program is presently in development. A complete version of UPGBIOS is upcoming.

13.1 CPLD UPGRADE AFTER A BIOS UPDATE

During the first system bootup after you update the Boot Block Flash BIOS with the UPGBIOS utility, the BIOS may need to upgrade the CPLD devices.

> **WARNING**
>
> **Whenever the BIOS performs a CPLD hardware upgrade, do not interrupt the system in any way (power down, reset, mouse or keyboard functions). The devices will be damaged and your board rendered inoperative if you disturb the update process!**

The following message appears on the screen when the BIOS writes to the devices:

```
A hardware upgrade will be performed on some CPLDs. Follow the
instructions below with special care. Do not disturb the process.


DO NOT RESET OR POWER DOWN THE BOARD!!!



    □□□ Device 1 □□□   0% □□□□□□□□□□□□□□□□□□□□ 100%
    □□□ Device 2 □□□   0% □□□□□□□□□□□□□□□□□□□□ 100%




Status :
         Please wait...
```

The color of the boxes displayed in the message indicates these functions:

Device OK	Green
Device busy	Blue
Device will be updated	Red

- If your device upgrade was successful, the following message is displayed under the "Status:" line prior to rebooting:

```
Update complete successfully, wait for the automatic reboot.
Rebooting in 5 second(s).
```

- **If the update is not successful, the following message appears under the "Status:" line:**

```
ERROR: general failure programming CPLDs!
Please contact Teknor Industrial Computers technical support.
```

You must contact TEKNOR's technical support for further instructions.

14. VT100 MODE

The VT100 operating mode allows remote setups of the board. This configuration requires a remote terminal that must be connected to the board through a serial communication link.

14.1 REQUIREMENTS

The terminal should emulate a VT100 or ANSI terminal. Terminal emulation programs such as Telix or Procomm can also be used.

NOTE
Some strange characters may appear on the screen. This occurs because the VT100 recognizes some control characters, and causes them to perform a specific function, for example, screen erase, cursor position, and so on.

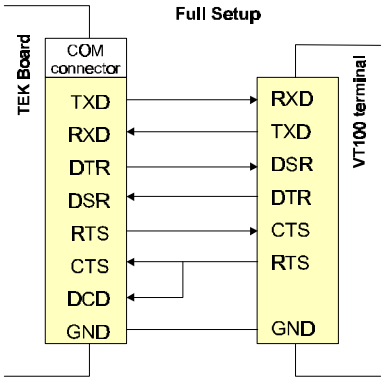
14.2 SETUP & CONFIGURATION

Follow these steps to set up the VT100 mode:

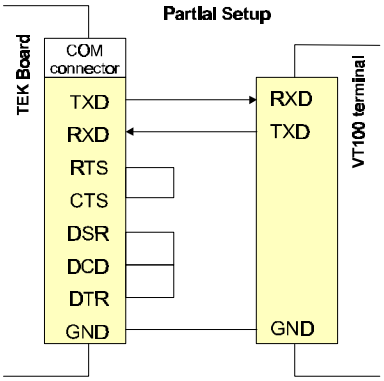
1. Connect a monitor and a keyboard to your board and turn on the power.
2. Enter into the CMOS Setup program.
3. Select the VT100 mode and the appropriate COM port and save your setup.
4. Connect the communications cable as shown in the next page.

   Note: If you do not require a full cable for your terminal, you can set up a partial cable by using only the TXD and RXD lines. To ignore control lines simply loop them back as shown in VT100 Partial Setup cable diagram.
5. Configure your terminal to communicate using 8 bits, no parity. The following speeds are available: 2400, 9600, 19200, 38400, 57600, 115200BPS.
6. Use the remote keyboard and display to setup the BIOS.
7. Save the setup, exit, and disconnect the remote computer from the board to operate in stand-alone configuration.

VT100 Full Setup



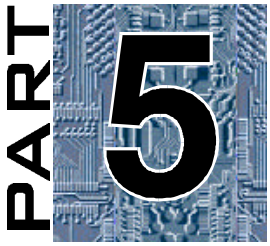
VT100 Partial Setup



14.3 RUNNING WITHOUT A TERMINAL

The board can boot up without a screen or terminal attached. However, if VT100 Mode is desired, but the terminal is to be disconnected, you must ensure the control lines are in an active state. Failing this, the system may "hang" while waiting for the control lines to become active. Wiring the system according to the Partial Setup allows the lines to remain active. This does not apply if the VT100 mode is disabled.

Furthermore, you can run without any console at all by simply not enabling VT100 Mode and by disabling the onboard video function.



APPENDIX

A. BOARD SPECIFICATIONS

B. MEMORY AND I/O MAPS

C. BOARD DIAGRAMS

D. CONNECTOR PINOUTS

E. BIOS SETUP ERROR CODES

A. BOARD SPECIFICATIONS

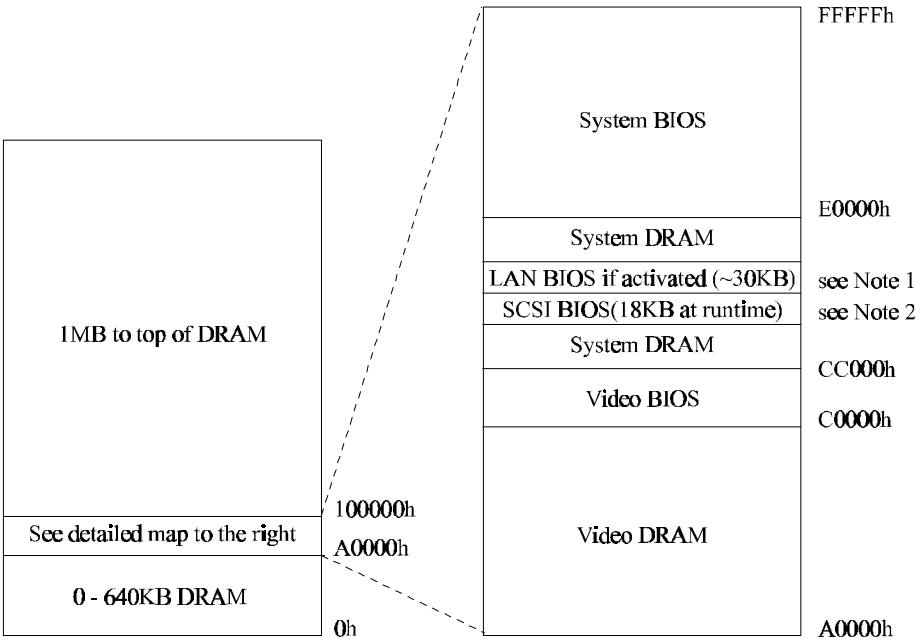
TEK-CPCI-1003	DESCRIPTION
Overview	*Intel Mobile Pentium® II* based CompactPCI System Board
Supported Microprocessors	*Intel Mobile Pentium® II* 233MHz, 266MHz and 300MHz
Bus Interface	CompactPCI bus, 32-bit (33MHz) through J1 and J2 PCI Mezzanine (PMC) Proprietary Mezzanine with PCI bus, FD and EIDE interfaces SMBus (for power management, DRAM control) Data Path: 64-bit on CPU and video memory; 32-bit on local PCI and CPCI
PCI-to-PCI Bridge	Supports up to 7 REQ/GNT arbitration signal pair for fully loaded CompactPCI system
System Memory	From 8MB to 384MB (SDRAM) or 768MB using Registered SDRAM (RSDRAM), supported by three 168-pin DIMM sockets
Cache Memory	Level 1: 16/16KB instruction Level 2: 512KB internal, 64-bit wide, pipelined burst
Boot Block Flash	256KB
I/Os	*USB* Two Universal Serial Bus (USB) ports *Serial* Four UART serial port configurable as COM1-4. COM3 is configurable as RS-232, RS-422, RS-485, Infrared *Parallel* One bi-directional multimode port with all IEEE1284 protocols supported (compatibility, nibble, byte, EPP and ECP) *Hard Disk* Two channel Bus Master PCI Enhanced IDE interfaces for up to four Type 4 devices in Master/Slave configuration; LBA, PIO Mode 0-4 and Ultra DMA/33 *CompactFlash disk*: optional bootable Compact-Flash module interfaces to primary EIDE channel, user upgradable, Master/Slave *Ethernet* Two PCI 10/100 MB interfaces (10Base-T, 100Base-TX) *SCSI* 16-bit Ultra Wide SCSI (40MB/s), 8-bit Ultra SCSI (20MB/s), 8-bit Fast SCSI 2 (10MB/s) *Floppy* Supports for two disk drives from 360KB to 2.88MB *Keyboard* Standard AT keyboard via mezzanine board *Mouse* PS/2 mouse via mezzanine board

TEK-CPCI-1003	DESCRIPTION
Video	64-bit AGP video controller (Cirrus Logic GD5465) 2MB Rambus video memory. CRT only. V-Port (Asynchronous Digital Video) interface supporting video on graphics, and graphics on video overlays; V-Port signals are accessible rear I/O connector
Connectors	*Front Plate* CRT — 15-pin D-Sub Serial Port 1 — 9-pin D-Sub Ethernets — RJ-45 with built-in LEDs PS/2 mouse — 6-pin mini-DIN on mezzanine Keyboard — 6-pin mini-DIN on mezzanine *Rear CPCI I/O Connectors* CRT, V-Port, Serial Ports (4) USB (2), SMBus, Parallel Port Speaker, Infrared, Ethernet (2) PS/2 mouse, Keyboard, SCSI Reset Switch, EIDE (2), Floppy disk *Onboard Expansions* PCI Mezzanine Card PMC. Proprietary mezzanine. CompactFlash.
BIOS Features	Award BIOS in Boot Block Flash. Auto configuration, extended setup, Plug and Play tables. Diskless, keyboardless, and videoless operation extensions. BIOS POST and Setup console redirection to serial port. Support for memory hole at 15-46MB / ISA bus aliasing and CC000-E0000 address blocking. Programmable CPU and memory wait states. System, video, and SCSI BIOS shadowing Advanced power management support. Ability to support MS-DOS and other applications from Flash disk.
Supervisory	Software programmable; 2-level watchdog timer drives NMI on first level and system reset on second level; programmable CPU temperature monitor; /alarm Power failure / low battery detector; front panel LEDs: IDE activity, SCSI activity, Ethernet activity / link.

Operating System Compatibility	MS-DOS®, Windows® 95, Windows® NT, VxWorks®, Psos
Dimensions	9.2 x 6.3 x 1.6 inches / 233 x 160 x 41 mm 6U x 8HP board mechanically compliant to IEEE 1101.10 ; compliant to PICMG 2.0 Rev 2.1.
Power Requirements	*Supply Voltages* +3.3V, ±5% +5V, ±5% +12V, ±5% *Supply Current** 3.3V: 7.5A max. 5V 2.0A max. 12V 0.25A max. ** with 233MHz Mobile Pentium II and 32MB DRAM* *Power Dissipation* 32W max.
Reliability	*MTBF - MIL-HDBK-217F* Over 100,000 hours @ 55°C Designed to meet or exceed: UL, cUL; FCC CFR 47 Part 15, Level A, CE Mark to CISPR 22 EN55022 Class B. USB and keyboard voltage protected by self-resetting fuses. Board serial number in EEPROM
Environnemental Conditions	Operating Temp. 0 to 60°C (w/ airflow) - 5% to 95% RH @ 40°C Storage Temp. -40°C to 70°C - 5% to 95% RH @ 40°C Shock / Vibration IEC 68-2-27 compliant Altitude 15,000feet / 4,572m

B. MEMORY & I/O MAPS

B.1 MEMORY MAPPING



Note 1: LAN BIOS address may vary.

Note 2: SCSI BIOS address may vary.
Size only 2KB if no device.

Address	Function
00000-9FFFF	0-640 KB DRAM
A0000-BFFFF	Video DRAM
C0000-CBFFF	Video BIOS
D8000-FFFFF	System DRAM
	LAN BIOS around 30KB if activated, address may vary
	SCSI BIOS 18KB at runtime, 2KB if no device, address may vary
100000-Top of DRAM	1 MB - Top of DRAM

B.2 I/O MAPPING

Address	Optional Address	Optional Address	Optional Address	Function
000-01F				DMA Controller 1
020-03F				Interrupt Controller 1
040-05F				Timer
060-06F				Keyboard
070-07F				Real-time clock
080-09F				DMA Page Register
0A0-0BF				Interrupt Controller 2
0C0-0DF				DMA Controller 2
0F0-0F1, 0F8-0FF				Math Coprocessor
190-197	290-297	390-397		TEKNOR Control Port
1F0-1F7, 3F6				Primary IDE
170-177, 376				Secondary IDE
3F0-3F7	370-377			Floppy Disk
378-37A	3BC-3BE	278-27A		Parallel Port (LPT1 by default)
3F8-3FF (COM1)	2F8-2FF (COM2)	3E8-3EF (COM3)	2E8-2EF (COM4)	Serial Port 1 (COM1 by default)
2F8-2FF (COM2)	3F8-3FF (COM1)	3E8-3EF (COM3)	2E8-2EF (COM4)	Serial Port 2 (COM2 by default)
3C0-3CF, 3D0-3DF, 3B0-3BB				Graphics Controller (I2C Port)

B.3 IRQ LINES

The board is fully PC compatible with interrupt steering for PCI plug and play compatibility.

Controller # 1		Controller # 2	
IRQ 0	Timer Output 0	IRQ 8	Real-Time Clock
IRQ 1	Keyboard (Output Buffer Full)	IRQ 9	Available [1]
IRQ 2	Cascade Controller # 2	IRQ 10	Available [1]
IRQ 3	Serial Port 2 *	IRQ 11	Available [1]
IRQ 4	Serial Port 1 *	IRQ 12	PS/2 Mouse
IRQ 5	Parallel Port 2 * or Available [1]	IRQ 13	Coprocessor Error
IRQ 6	Floppy Controller *	IRQ 14	Primary IDE * or available [1]
IRQ 7	Parallel Port 1 * or Available [1]	IRQ 15	Secondary IDE * or available [1]

* All functions marked with an asterisk (*) can be disabled or reconfigured.
[1] Available lines service on board and external PCI/ISA PnP devices or a Legacy ISA device.

B.4 DMA CHANNELS

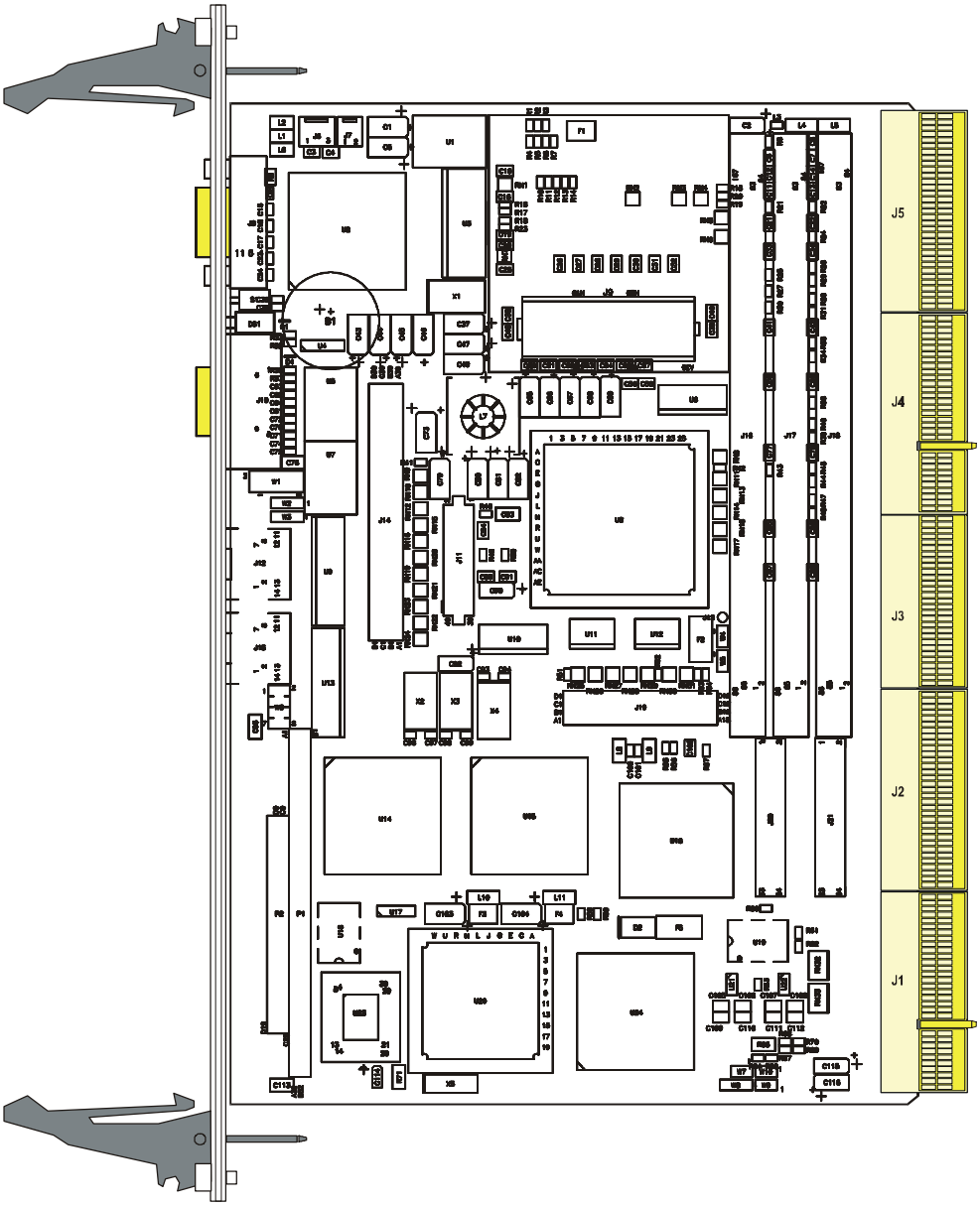
The TEK-CPCI-1003 integrates the functionality of two 8237 DMA controllers. Eight DMA channels are available.

According to Plug and Play standards, the system BIOS automatically allocates DMA Channel 1 or 3 for the parallel port's ECP mode. Channel 2 is reserved for the floppy controller and Channel 4 is used to cascade Channels 0 through 7 to the microprocessor.

DMA Channel	Function
DMA 0	Available
DMA 1	PnP available (ECP)
DMA 2	Floppy controller
DMA 3	PnP available (ECP)
DMA 4	Cascade controller # 1
DMA 5	PnP available
DMA 6	PnP available
DMA 7	PnP available

C. BOARD DIAGRAMS

C.1 ASSEMBLY - TOP DIAGRAM



D. CONNECTOR PINOUTS

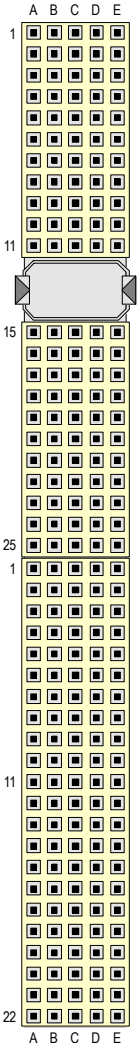
TEK-CPCI-1003 connectors and headers are listed below:

J1	CPCI Bus Connector
J2	CPCI Bus Connector
J3	CPCI I/O Connector
J4	CPCI I/O Connector
J5	CPCI I/O Connector
J7	Fan Connector
J8	CRT VGA Connector (Front panel configuration only)
J10	Serial Port 1 – RS-232 (Front panel configuration only)
J11	CompactFLASH Disk Connector
J12	Ethernet 1 Connector (Front panel configuration only)
J14	Mezzanine PCI Connector
J15	Ethernet 0 Connector (Front panel configuration only)
J19	Mezzanine Storage Connector
J20	PMC Connector
J21	PMC Connector

D.1 J1, J2 – CPCI BUS CONNECTORS

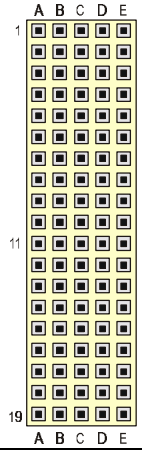
	ROW "A"			ROW "B"			ROW "C"		
	#	Ref.	SIGNAL	#	Ref.	SIGNAL	#	Ref.	SIGNAL
	1	A1	+5V	1	B1	-12V	1	C1	/TRST
	2	A2	TCK	2	B2	+5V	2	C2	TMS
	3	A3	/INTA	3	B3	/INTB	3	C3	/INTC
	4	A4	N.C.	4	B4	GND	4	C4	VI/O
	5	A5	N.C.	5	B5	N.C.	5	C5	/RST
	6	A6	/REQ0	6	B6	GND	6	C6	+3.3V
	7	A7	AD30	7	B7	AD29	7	C7	AD28
	8	A8	AD26	8	B8	GND	8	C8	VI/O
	9	A9	/CBE3	9	B9	N.C.	9	C9	AD23
	10	A10	AD21	10	B10	GND	10	C10	+3.3V
	11	A11	AD18	11	B11	AD17	11	C11	AD16
J1 (P1)	15	A15	+3.3V	15	B15	/FRAME	15	C15	/IRDY
	16	A16	/DEVSEL	16	B16	GND	16	C16	VI/O
	17	A17	+3.3V	17	B17	SDONE	17	C17	/SBO
	18	A18	/SERR	18	B18	GND	18	C18	+3.3V
	19	A19	+3.3V	19	B19	AD15	19	C19	AD14
	20	A20	AD12	20	B20	GND	20	C20	VI/O
	21	A21	+3.3V	21	B21	AD9	21	C21	AD8
	22	A22	AD7	22	B22	GND	22	C22	+3.3V
	23	A23	+3.3V	23	B23	AD4	23	C23	AD3
	24	A24	AD1	24	B24	+5V	24	C24	VI/O
	25	A25	+5V	25	B25	/REQ64	25	C25	/PME
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	26	A1	CLK1	26	B1	GND	26	C1	/REQ1
	27	A2	CLK2	27	B2	CLK3	27	C2	/SYSEN
	28	A3	CLK4	28	B3	GND	28	C3	/GNT3
	29	A4	VI/O	29	B4	N.C.	29	C4	N.C.
	30	A5	N.C.	30	B5	GND	30	C5	VI/O
	31	A6	N.C.	31	B6	N.C.	31	C6	N.C.
	32	A7	N.C.	32	B7	GND	32	C7	VI/O
	33	A8	N.C.	33	B8	N.C.	33	C8	N.C.
	34	A9	N.C.	34	B9	GND	34	C9	VI/O
	35	A10	N.C.	35	B10	N.C.	35	C10	N.C.
J2 (P2)	36	A11	N.C.	36	B11	GND	36	C11	VI/O
	37	A12	N.C.	37	B12	N.C.	37	C12	N.C.
	38	A13	N.C.	38	B13	GND	38	C13	VI/O
	39	A14	N.C.	39	B14	N.C.	39	C14	N.C.
	40	A15	N.C.	40	B15	GND	40	C15	/FAL
	41	A16	N.C.	41	B16	N.C.	41	C16	/DEG
	42	A17	N.C.	42	B17	GND	42	C17	/PRST
	43	A18	N.C.	43	B18	N.C.	43	C18	N.C.
	44	A19	N.C.	44	B19	GND	44	C19	N.C.
	45	A20	CLK5	45	B20	GND	45	C20	N.C.
	46	A21	CLK6	46	B21	GND	46	C21	N.C.
	47	A22	N.C.	47	B22	N.C.	47	C22	N.C.

	ROW "D"			ROW "E"			PINOUT
	#	Ref.	SIGNAL	#	Ref.	SIGNAL	(Top View)
	1	D1	+12V	1	E1	+5V	
	2	D2	TDO	2	E2	TDI	
	3	D3	+5V	3	E3	/INTD	
	4	D4	IRQ14	4	E4	IRQ15	
	5	D5	GND	5	E5	/GNT0	
	6	D6	CLK0	6	E6	AD31	
	7	D7	GND	7	E7	AD27	
	8	D8	AD25	8	E8	AD24	
	9	D9	GND	9	E9	AD22	
	10	D10	AD20	10	E10	AD19	
	11	D11	GND	11	E11	/C/BE2	
J1 (P1)	15	D15	GND	15	E15	/TRDY	**J1 (P1)**
	16	D16	/STOP	16	E16	/LOCK	
	17	D17	GND	17	E17	/PERR	
	18	D18	PAR	18	E18	/CBE1	
	19	D19	GND	19	E19	AD13	
	20	D20	AD11	20	E20	AD10	
	21	D21	N.C.	21	E21	/CBE0	
	22	D22	AD6	22	E22	AD5	
	23	D23	+5V	23	E23	AD2	
	24	D24	AD0	24	E24	AD0	
	25	D25	+3.3V	25	E25	+5V	
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	26	D1	/GNT1	26	E1	/REQ2	
	27	D2	/GNT2	27	E2	/REQ3	
	28	D3	/REQ4	28	E3	/GNT4	
	29	D4	GND	29	E4	N.C.	
	30	D5	N.C.	30	E5	N.C.	
	31	D6	GND	31	E6	N.C.	
	32	D7	N.C.	32	E7	N.C.	
	33	D8	GND	33	E8	N.C.	
	34	D9	N.C.	34	E9	N.C.	
	35	D10	GND	35	E10	N.C.	
J2 (P2)	36	D11	N.C.	36	E11	N.C.	**J2 (P2)**
	37	D12	GND	37	E12	N.C.	
	38	D13	N.C.	38	E13	N.C.	
	39	D14	GND	39	E14	N.C.	
	40	D15	/REQ5	40	E15	/GNT5	
	41	D16	GND	41	E16	N.C.	
	42	D17	/REQ6	42	E17	/GNT6	
	43	D18	GND	43	E18	N.C.	
	44	D19	N.C.	44	E19	N.C.	
	45	D20	GND	45	E20	N.C.	
	46	D21	N.C.	46	E21	N.C.	
	47	D22	N.C.	47	E22	N.C.	



D.2 J3 – CPCI I/O CONNECTORS

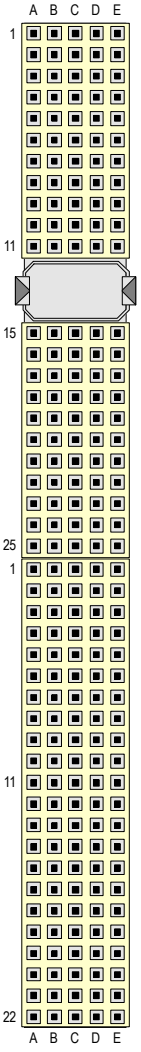
	ROW "A"			ROW "B"			ROW "C"		
	#	Ref.	SIGNAL	#	Ref.	SIGNAL	#	Ref.	SIGNAL
J3 (P3)	1	A1	VP-OUT	1	B1	ZVPCLK	1	C1	VP-IN
	2	A2	GND	2	B2	VSCL2	2	C2	GND
	3	A3	VP5	3	B3	+5V	3	C3	VP6
	4	A4	VSDA2	4	B4	VP3	4	C4	/VP-HSYNC
	5	A5	VP0	5	B5	GND	5	C5	VP1
	6	A6	SPEEPLED0	6	B6	LINKLED-0	6	C6	ACTLED0
	7	A7	ACTLED1	7	B7	Reserved	7	C7	Reserved
	8	A8	GND	8	B8	+5V	8	C8	+5V
	9	A9	ETX+1	9	B9	ETX-1	9	C9	ERX+1
	10	A10	GND	10	B10	Reserved	10	C10	N.C.
	11	A11	/JDCD4	11	B11	GND	11	C11	JRXD4
	12	A12	/JRTS4	12	B12	/JCTS4	12	C12	/JRI4
	13	A13	/JDCD3	13	B13	+5V	13	C13	JRXD3
	14	A14	/JRTS3	14	B14	/JCTS3	14	C14	/JRI3
	15	A15	N.C.	15	B15	N.C.	15	C15	N.C.
	16	A16	N.C.	16	B16	N.C.	16	C16	N.C.
	17	A17	N.C.	17	B17	N.C.	17	C17	N.C.
	18	A18	N.C.	18	B18	/EXT-SIDEACT	18	C18	/EXT-PIDEACT
	19	A19	/PWRBT	19	B19	EXT-SMI	19	C19	PX4-NMI

	ROW "D"			ROW "E"			PINOUT	
	#	Ref.	SIGNAL	#	Ref.	SIGNAL	(Top View)	
J3 (P3)	1	D1	VACTI	1	E1	GND		**J3 (P3)**
	2	D2	VP-VSYNC	2	E2	GND		
	3	D3	GND	3	E3	VP7		
	4	D4	VP4	4	E4	/EN-CAM		
	5	D5	GND	5	E5	VP2		
	6	D6	LINKLED-1	6	E6	SPEEDLED-1		
	7	D7	Reserved	7	E7	Reserved		
	8	D8	Reserved	8	E8	Reserved		
	9	D9	ERX-1	9	E9	GND		
	10	D10	Reserved	10	E10	Reserved		
	11	D11	/JDSR4	11	E11	JTXD4		
	12	D12	+5V	12	E12	/JDTR4		
	13	D13	/JDSR3	13	E13	JTXD3		
	14	D14	GND	14	E14	/JDTR3		
	15	D15	N.C.	15	E15	N.C.		
	16	D16	N.C.	16	E16	N.C.		
	17	D17	N.C.	17	E17	N.C.		
	18	D18	COM2-IRRX	18	E18	COM2-IRTX		
	19	D19	N.C.	19	E19	PWROK-33		

D.3 J4, J5 – CPCI I/O CONNECTORS

	ROW "A"			ROW "B"			ROW "C"		
	#	Ref.	SIGNAL	#	Ref.	SIGNAL	#	Ref.	SIGNAL
	1	A1	I2C-CLK	1	B1	I2C-DATA	1	C1	LID
	2	A2	SM-BYPASS	2	B2	/CD11	2	C2	/CD10
	3	A3	/SIO	3	B3	/SREQ	3	C3	/CD
	4	A4	/RST	4	B4	/ACK	4	C4	/BSY
	5	A5	GND	5	B5	/WIDEPS	5	C5	TERMPWR
	6	A6	GND	6	B6	/DPL	6	C6	/CD7
	7	A7	/CD4	7	B7	/CD3	7	C7	/CD2
	8	A8	DPH	8	B8	/CD15	8	C8	/CD14
	9	A9	GND	9	B9	GND	9	C9	N.C.
	10	A10	VSCL	10	B10	HSYNC	10	C10	VSYNC
	11	A11	BLUE	11	B11	GND	11	C11	N.C
J4 (P4)	15	A15	GND	15	B15	+5V	15	C15	+5V
	16	A16	TX+0	16	B16	TX-0	16	C16	ERX+0
	17	A17	/BRSTDRV	17	B17	GND	17	C17	SDD7
	18	A18	DD9	18	B18	DD5	18	C18	SDD10
	19	A19	DD3	19	B19	DD12	19	C19	SDD2
	20	A20	DD14	20	B20	DD0	20	C20	SDD15
	21	A21	DREQ	21	B21	GND	21	C21	/SDIOW
	22	A22	GND	22	B22	IORDY	22	C22	N.C.
	23	A23	/IOCS16	23	B23	DA1	23	C23	GND
	24	A24	/CS1	24	B24	/CS3	24	C24	SEC-PD1
	25	A25	N.C.	25	B25	N.C.	25	C25	N.C.
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	26	A1	/BRSTDRV	26	B1	/BRSTDRV	26	C1	PDD7
	27	A2	PDD9	27	B2	PDD5	27	C2	PDD10
	28	A3	PDD3	28	B3	PDD12	28	C3	PDD2
	29	A4	PDD14	29	B4	PDD0	29	C4	GND
	30	A5	PDREQ	30	B5	PIORDY	30	C5	/PDIOW
	31	A6	/IOCS16	31	B6	GND	31	C6	/PDIAG
	32	A7	PCS1	32	B7	/PCS3	32	C7	PDA1
	33	A8	/FD-DRVEN1	33	B8	/FD-INDEX	33	C8	/FD-MTR0
	34	A9	/FD-MTR1	34	B9	/FD-DIR	34	C9	/FD-STEP
	35	A10	/FD-TRK0	35	B10	/FD-WRTPRT	35	C10	/FD-RDATA
J5 (P5)	36	A11	/DCD2	36	B11	GND	36	C11	JRXD2
	37	A12	/RTS2	37	B12	/CTS2	37	C12	/JRI2
	38	A13	/DCD1	38	B13	+5V	38	C13	JRXD1
	39	A14	/RTS1	39	B14	/CTS1	39	C14	/JRI1
	40	A15	SLCT	40	B15	PE	40	C15	BUSY
	41	A16	PD6	41	B16	PD5	41	C16	PD4
	42	A17	PD2	42	B17	/INIT	42	C17	PD1
	43	A18	ALF	43	B18	USBD1+	43	C18	USBD1-
	44	A19	/STB	44	B19	USBG1	44	C19	USBV1
	45	A20	+5V	45	B20	/SMBDATA	45	C20	/SMBALERT
	46	A21	KDATA	46	B21	KCLK	46	C21	VCC-KBD
	47	A22	/PRST	47	B22	GND	47	C22	/DIAG-OC

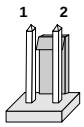
	ROW "D"			ROW "E"			PINOUT
	#	Ref.	SIGNAL	#	Ref.	SIGNAL	(Top View)
	1	D1	/EXT-FAN0-FAIL	1	E1	/DEG1	
	2	D2	SD9	2	E2	/SCD8	
	3	D3	/SSEL	3	E3	/SMSG	
	4	D4	GND	4	E4	/SATN	
	5	D5	TERMPWR	5	E5	GND	
	6	D6	/SDC6	6	E6	/SCD5	
	7	D7	/SCD1	7	E7	/SCD0	
	8	D8	/SCD1	8	E8	/SCD12	
	9	D9	VSDA	9	E9	N.C.	
	10	D10	RED	10	E10	GREEN	
	11	D11	GND	11	E11	IGND	
J4 (P4)	15	D15	N.C.	15	E15	N.C.	**J4 (P4)**
	16	D16	ERX-0	16	E16	GND	
	17	D17	SDD8	17	E17	SDD6	
	18	D18	SDD4	18	E18	SDD11	
	19	D19	SDD13	19	E19	SDD1	
	20	D20	GND	20	E20	N.C.	
	21	D21	GND	21	E21	/SDIOR	
	22	D22	/SDDACK	22	E22	IRQ15	
	23	D23	SDA0	23	E23	SDA2	
	24	D24	GND	24	E24	/FAL1	
	25	D25	N.C.	25	E25	+5V	
--------	-----	-----	----------	-----	-----	----------	--------
	26	D1	PDD8	26	E1	PDD6	
	27	D2	PDD4	27	E2	PDD11	
	28	D3	PDD13	28	E3	PDD1	
	29	D4	PDD15	29	E4	IRQ14	
	30	D5	/PDDACK	30	E5	/PDIOR	
	31	D6	PDA0	31	E6	PDA2	
	32	D7	PRI-PD1	32	E7	/FD-DRVEN0	
	33	D8	/FD-DS1	33	E8	/FD-DS1	
	34	D9	/FD-WDATA	34	E9	/FD-WGATE	
	35	D10	/FD-HDSEL	35	E10	/FD-DSKCHG	
J5 (P5)	36	D11	/JDSR2	36	E11	JTXD2	**J5 (P5)**
	37	D12	+5V	37	E12	/JDTR2	
	38	D13	/JDSR1	38	E13	JTXD1	
	39	D14	GND	39	E14	/JDTR1	
	40	D15	/ACK	40	E15	PD7	
	41	D16	PD3	41	E16	/SLCTIN	
	42	D17	/ERR	42	E17	PD0	
	43	D18	USBG0	43	E18	USBV0	
	44	D19	USBD0+	44	E19	USBD0-	
	45	D20	GND	45	E20	SMBCLK	
	46	D21	MDATA	46	E21	MCLK	
	47	D22	+5V	47	E22	SPK-OUT	



D.4 FAN CONNECTOR (J7)

Pin #	Signal
1	+12V DC
2	GND

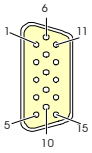
Front View



D.5 CRT VGA CONNECTOR (J8)

Signal		Signal		Signal	
RED	1	Analog GND	6	Not Connected	11
GREEN	2	Analog GND	7	Not Connected	12
BLUE	3	Analog GND	8	HSYNC	13
Not Connected	4	Not Connected	9	VSYNC	14
GND	5	GND	10	Not Connected	15

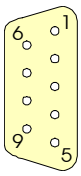
Top View



D.6 SERIAL PORT 1 - RS-232 (J10)

Pin Number	Signal Flow	Signal
DSR 1	I	6
RTS1	O	7
CTS 1	I	8
RI 1	-	9

Top View

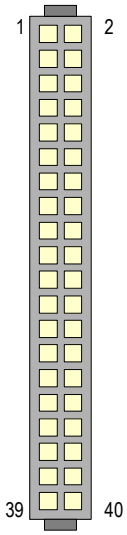


Pin Number	Signal Flow	Signal
1	I	DCD 1
2	I	RXD 1
3	I	TXD 1
4	O	DTR 1
5	O	GND 1

D.7 COMPACTFLASH DISK CONNECTOR (J11)

Signal	Pin Number
D11	1
D12	3
D13	5
D14	7
D15	9
CS3#	11
Not Connected	13
Not Connected	15
PDIAG#	17
RIRQ14	19
VCC	21
GND	23
BRSTDRV#	25
To W5 jumper	27
A1	29
A0	31
D0	33
D1	35
D2	37
IOCS16#	39

Top View

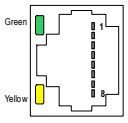


Pin Number	Signal
2	GND
4	D3
6	D4
8	D5
10	D6
12	D7
14	RPCS1#
16	IOR#
18	IOW#
20	VCC
22	VCC
24	GND
26	GND
28	A2
30	CFLASH-ACT#
32	Not Connected
34	D8
36	D9
38	D10
40	GND

D.8 ETHERNET 1 CONNECTOR (J12)

Signal	
TX+	1
TX-	2
RX+	3
Not Connected	4
Not Connected	5
RX-	6
Not Connected	7
Not Connected	8

Top View



D.9 MEZZANINE PCI CONNECTOR (J14)

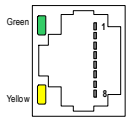
	A	B	Top View A B C D	C	D	
1	5V_KEY	Reserved	1	+5V	AD00	1
2	VI/O (5V)	AD02		AD01	+5V	2
3	AD05	GND		AD04	AD03	3
4	C/BE0#	AD07		GND	AD06	4
5	GND	AD09		AD08	GND	5
6	AD11	VI/O (5V)		AD10	MM66EN	6
7	AD14	AD13		GND	AD12	7
8	+3.3V	C/BE1#		AD15	+3.3V	8
9	SERR#	GND		SB0#	PAR	9
10	GND	PERR#		+3.3V	SDONE	10
11	STOP#	+3.3V		LOCK#	GND	11
12	+3.3V	TRDY#		GND	DEVSEL#	12
13	FRAME#	GND		IRDY#	+3.3V	13
14	GND	AD16		+3.3V	C/BE2#	14
15	AD18	+3.3V		AD17	GND	15
16	AD21	AD20		GND	AD19	16
17	+3.3V	AD23		AD22	+3.3V	17
18	IDSEL0	GND		IDSEL1	IDSEL2	18
19	AD24	C/BE3#		VI/O (5V)	IDSEL3	19
20	GND	AD26		AD25	GND	20
21	AD29	+5V		AD28	AD27	21
22	+5V	AD30		GND	AD31	22
23	REQ0#	GND		REQ1#	VI/O (5V)	23
24	GND	REQ2#		+5V	GNT0#	24
25	GNT1#	VI/O (5V)		GNT2#	GND	25
26	+5V	CLK0		GND	CLK1	26
27	CLK	+5V		CLK3	GND	27
28	GND	INTD#		+5V	RST#	28
29	+12V	INTA#		INTB#	INTC#	29
30	-12V	Reserved	30	Reserved	3.3V_KEY	30

Active Low Signal

D.10 ETHERNET 0 CONNECTOR (J15)

Signal	
TX+	1
TX-	2
RX+	3
Not Connected	4
Not Connected	5
RX-	6
Not Connected	7
Not Connected	8

Top View



D.11 MEZZANINE STORAGE CONNECTOR (J19)

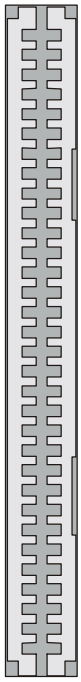
	A	B	Top View A B C D	C	D	
1	VCC	VCC	1	VCC	VCC	1
2	VCC	VCC		VCC	PDD0	2
3	MCLK	MDATA		PDD1	PDD2	3
4	KBDAT	KBCLK		PDD3	PDD4	4
5	VCC-KBDF	GND		PDD5	PDD6	5
6	GND	GND		PDD7	PDD8	6
7	GND	GND		PDD9	PDD10	7
8	GND	GND		PDD11	PDD12	8
9	GND	GND		PDD13	PDD14	9
10	FD-DS1#	FD-DRVEN0#		PDD15	BRSTDRV#	10
11	FD-DRVEN1#	FD-MTR1#		PDIOW#	PDREQ	11
12	FD-INDEX#	FD-DS0#		PIORDY0	PDIOR#	12
13	FD-DSKCHG#	FDET		IRQ14	PDDACK#	13
14	FD-MTR0#	FD-DIR#		PDA0	PDA1	14
15	FD-STEP#	FD-WDATA#		PDA2	GND	15
16	FD-GATE#	FD-TRK0#		HD-ACT#	PCS1#	16
17	FD-WRTPTR#	FD-RDATA#		PCS3#	PDIAG#	17
18	FD-HSEL#	+12V	18	IOCS16#	+12V	18

Active Low Signal

D.12 PMC CONNECTOR (J20)

Pin Number	Signal
1	Not Connected
3	GND
5	INTB#
7	BUSMODE1#
9	INTD#
11	GND
13	PCLK-PMC
15	GND
17	REQ-PMC#
19	VCC
21	AD28
23	AD25
25	GND
27	AD22
29	AD19
31	VCC
33	FRAME#
35	GND
37	DEVSEL#
39	GND
41	PMC-SDONE#
43	PAR
45	VCC
47	AD12
49	AD9
51	GND
53	AD6
55	AD4
57	VCC
59	AD2
61	AD0
63	GND

Top View

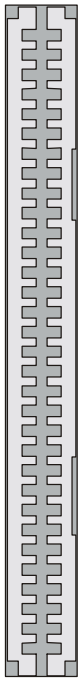


Pin Number	Signal
2	-12V
4	INTA#
6	INTC#
8	VCC
10	Not Connected
12	Not Connected
14	GND
16	GNT-PMC#
18	VCC
20	AD31
22	AD27
24	GND
26	C/BE3#
28	AD21
30	VCC
32	AD17
34	GND
36	IRDY#
38	VCC
40	LOCK#
42	PMC-SB0#
44	GND
46	AD15
48	AD11
50	VCC
52	C/BE0#
54	AD5
56	GND
58	AD3
60	AD1
62	VCC
64	Not Connected

D.13 PMC CONNECTOR (J21)

Pin Number	Signal	Pin Number	Signal
1	+12V	2	Not Connected
3	Not Connected	4	Not Connected
5	Not Connected	6	GND
7	GND	8	Not Connected
9	Not Connected	10	Not Connected
11	BUSMODE2#	12	3.3V
13	PCIRST#	14	BUSMODE3#
15	3.3V	16	BUSMODE4#
17	Not Connected	18	GND
19	AD30	20	AD29
21	GND	22	AD26
23	AD24	24	3.3V
25	IDSEL-PMC#	26	AD23
27	3.3V	28	AD30
29	AD18	30	GND
31	AD16	32	C/BE2#
33	GND	34	Not Connected
35	IRDY#	36	3.3V
37	GND	38	STOP#
39	PERR#	40	GND
41	3.3V	42	SERR#
43	C/BE1#	44	GND
45	AD14	46	AD13
47	GND	48	AD10
49	AD8	50	3.3V
51	AD7	52	Not Connected
53	3.3V	54	Not Connected
55	Not Connected	56	GND
57	Not Connected	58	Not Connected
59	GND	60	Not Connected
61	Not Connected	62	3.3V
63	GND	64	Not Connected

Top View



E. BIOS SETUP ERROR CODES

E.1 POST BEEP

POST beep codes are defined in the BIOS to provide low level tone indication when an error occurs during the BIOS initialization.

Beep codes consist of a combination of long and short beeps. They are described as follows:

Beep Codes

Post code	Beep Code	Description
41	**-*	Enterring the boot block recovery code (i.e. Main BIOS checksum error)
22	*-*-*	Error when getting the boot block flash ID code
33	*-*-*-*	Error when erasing the boot block flash
44	*-*-*-*-*	Error when programming the boot block flash
55	*-*	Success of the boot block recovery code. The board is ready to be manually reset.

LEGEND

Symbol	Description
*	1 Beep code
-	Silence

E.2 POST MESSAGES

During the Power On Self Test (POST), if the BIOS detects an error requiring you to do something to fix, it will either sound a beep code or display a message.

If a message is displayed, it will be accompanied by:

"PRESS F1 TO CONTINUE, DEL TO ENTER SETUP".

E.3 ERROR MESSAGES

One or more of the following messages may be displayed if the BIOS detects an error during the POST. This list includes messages for both the ISA and EISA BIOS.

CMOS BATTERY HAS FAILED

CMOS battery is no longer functional. It should be replaced.

CMOS CHECKSUM ERROR

Checksum of CMOS is incorrect. This can indicates that CMOS has become corrupt. This error may have been caused by a weak battery. Check the battery and replace if necessary.

DISK BOOT FAILURE, INSERT SYSTEM DISK AND PRESS ENTER

No boot device was found. This could mean either a boot drive was not detected or the drive does not contain proper system boot files. Insert a system disk into Drive A and press Enter. If you assumed the system would boot from the hard drive, make sure the controller is inserted correctly and all cables are properly attached. Also be sure the disk is formatted as a boot device. Then reboot the system.

DISKETTE DRIVES OR TYPES MISMATCH ERROR - RUN SETUP

Type of diskette drive installed in the system is different from CMOS definition. Run Setup to reconfigure the drive type correctly.

DISPLAY SWITCH IS SET INCORRECTLY

Display switch on the motherboard can be set to either monochrome or color. This indicates the switch is set to a different setting than indicated in Setup. Determine which setting is correct, and then either turn off the system and change the jumper, or enter Setup and change the VIDEO selection.

DISPLAY TYPE HAS CHANGED SINCE LAST BOOT

Since last powering off the system, the display adapter has been changed. You must configure the system for the new display type.

ERROR ENCOUNTERED INITIALIZING HARD DRIVE

Hard drive cannot be initialized. Be sure the adapter is installed correctly and all cables are correctly and firmly attached. Also be sure the correct hard drive type is selected in Setup.

ERROR INITIALIZING HARD DRIVE DISK CONTROLLER

Cannot initialize controller. Make sure the cord is correctly and firmly installed in the bus. Be sure the correct hard drive type is selected in Setup. Also check to see if any jumper needs to be set correctly on the hard drive.

FLOPPY DISK CNTRLR ERROR OR NO CNTRLR PRESENT

Cannot find or initialize the floppy drive controller. Make sure the controller is installed correctly and firmly. If there are no floppy drives installed, be sure the Diskette Drive selection in Setup is set to NONE.

KEYBOARD ERROR OR NO KEYBOARD PRESENT

Cannot initialize the keyboard. Make sure the keyboard is attached correctly and no keys are being pressed during the boot.

If you are purposely configuring the system without a keyboard, set the error halt condition in Setup to HALT ON ALL, BUT KEYBOARD. This will cause BIOS to ignore the missing keyboard and continue the boot.

MEMORY ADDRESS ERROR AT ...

Indicates a memory address error at a specific location. You can use this location along with the memory map for your system to find and replace the bad memory chips.

MEMORY PARITY ERROR AT ...

Indicates a memory parity error at a specific location. You can use this location along with the memory map for your system to find and replace the bad memory chips.

MEMORY SIZE HAS CHANGED SINCE LAST BOOT

Memory has been added or removed since the last boot. In EISA mode use the Configuration utility to reconfigure the memory configuration. In ISA mode enter Setup and enter the new memory size in the memory fields.

MEMORY VERIFY ERROR AT ...

Indicates an error verifying a value already written to memory. Use the location along with your system's memory size in the memory map to locate the bad chip.

OFFENDING SEGMENT

This message is used in conjunction with the I/O CHANNEL CHECK and RAM PARITY ERROR messages when the segment that has caused the problem cannot be isolated.

PRESS A KEY TO REBOOT

This will be displayed at the bottom screen when an error occurs that requires you to reboot. Press any key and the system will reboot.

PRESS F1 TO DISABLE NMI, F2 TO REBOOT

When BIOS detects a Non-maskable Interrupt condition during boot, this will allow you to disable the NMI and continue to boot, or you can reboot the system with the NMI enabled.

RAM PARITY ERROR - CHECKING FOR SEGMENT ...

Indicates a parity error in Random Access Memory.

E.4 POST CODES

POST #	Designation	Description
01	BOOT BLOCK	Boot Block in EMERGENCY : Clear Base Memory Area.
03	Initialize Chips	1. Clear CMOS shutdown byte. 2. Initialize EISA extended registers. (Not for us since we don't have EISA bus.)
04	Test Memory Refresh Toggle	RAM must be periodically refreshed in order to keep the memory from decaying.
05	Blank Video, Initialize Keyboard	1. Clear CMOS reset status byte. 2. Early Keyboard initialization. Boot Block in EMERGENCY: Initialize Keyboard Controller.
06	EPROM Checksum	1. Test F000h segment shadow readable and writeable for POST access correct. If not, show POST FE and beep continuously… 2. Autodetect Flash EPROM.
07	Test CMOS Interface and Battery Status	1. Install the TEKNOR segment. 2. Verifies CMOS is working correctly (walking bit test). 3. Restore CMOS from Flash if option is enabled. 4. Check for OVERRIDE KEY (INSERT key).
08	Program Chipset default	Program Chipset default (show POST BEh).
09	Early Cache Initialization	1. Check for Intel's and/or Cyrix CPU. 2. Early Cache Initialization when cache is separate from chipset. 3. Turn off Gate A20.
0A	Setup Interrupt Vector Table	1. Initialize first 120 interrupt vectors with SPURIOUS_INT_HDLR and initialize int. 00h-1Fh according to INT_TBL. 2. Early Power Management Initialization.
0B	Test CMOS RAM Checksum	1. Verify time and date for valid values. 2. If Override enabled, check for Override key. If Override key pressed, Kill CMOS checksum. 3. Check CMOS Battery (useless if save CMOS in FLASH enabled since it's already done). 4. Verify Checksum, if bad, load defaults. 5. Copy CMOS in the stack. 6. Clear CMOS Alarm date. 7. Clear HD if Hidden. 8. Clear Floppy "B" if only one drive. 9. Detect for a Math Co-processor. 10. Set Fast Gate A20 Flag in CMOS. 11. If "B" drive only is set the 2 Drive are set… 12. Program Chipset for early Power Management. 13. P6 Bios Update (if applicable). *14. Kill Onboard PnP IO.* 15. PnP Early Initialization. 16. PnP System Resource: 1. Get ESCD. 2. Create default SYSTEM_MAP. 3. Decode/Record ISA ESCD resources. 4. Record I/O port for PnP operation. 17. Chipset Early Shadow.

POST #	Designation	Description	
0C	Initialize Keyboard	1. Open Xilinx I/O Port location to x90h (X=1,2 or 3) inside the chipset (if necessary). 2. Disable (if necessary). Thermal Management. 3. Disable (if necessary) Ethernet Chip.Set IDE Detect counter to 0. 4. Set CD-ROM found variable to 0. 5. Initialize zone 40:0h for the keyboard buffer.	Boot Block 1st : Verify BIOS checksum. Boot Block in EMERGENCY 2nd : Init. vector 00h through 77h.
0D	Initialize Video Interface & Chipset	*1. On M1 set the cache for the memory installed.* *2. On PCI, do a PCI ROM init.* 3. On P6, Init. Apic. 4. Init. Chipset. 5. Turn ON CPU Cache. 6. Set Maximum Speed. 7. Measure CPU Clock Speed. 8. Restore Speed. 9. Turn Off CPU Cache. 10. Early Video Shadow. 11. Read CMOS location 14h to find out type of video to use. Detect and initialize Video Adapter. 12. Init. T380 if necessary.	Boot Block in EMERGENCY: Try to init. Video Card…
0E	Test Video Memory	1. If CGA or MONO, test video memory. 2. Beep the speaker. 3. Show the LOGO. 4. Install VT100 driver if necessary. 5. Write sign-on message to screen. 6. Write Copyright message to screen. 7. Write Evaluation message to screen. 8. Show CPU type and speed.	
0F	Test DMA Controller 0	Test DMA Controller 0.	
10	Test DMA Controller 1	Test DMA Controller 1.	
11	Test DMA Page Registers	Test DMA Page Registers.	
12	Reserved	Reserved for 8254 Counter 0 - Not implemented.	
13	Reserved	Reserved for 8254 Counter 1 - Not implemented.	
14	Test Timer Counter 2	Test 8254 Timer 0 Counter 2.	
15	PIC Test 8259-1 mask bits	Verify 8259 Channel 1 masked interrupts by alternately turning off and on the interrupt lines.	
16	PIC Test 8259-2 mask bits	Verify 8259 Channel 1 masked interrupts by alternately turning off and on the interrupt lines.	

POST #	Designation	Description
17	Test Struck 8259's Interrupt Bits	Nothing
18	Test 8259 Interrupt functionality	Force an interrupt and verify that the interrupt occurred (IRQ 0 - clock int. 8h).
19	Test Struck NMI Bits (Parity/ IO check)	Nothing.
1A-1E	Reserved	Reserved
1F	Set EISA Mode	If EISA non-volatile memory checksum is good, execute EISA initialization. If no, execute ISA test and clear EISA mode flag. Test EISA Configuration Memory integrity (checksum & communication interface).
20-2F	Enable Slots 0-15	Initialize slot 0 (System Board) to slot 15.
30	Size Base & Extended Memory	Size base memory from 256K to 640K and extended memory above 1MB.
31	Test Base & Extended Memory	1. Test base memory from 256K to 640K and extended memory above 1MB using various patterns. 2. The last test is filling memory with 0's. 3. On a quick memory test or if user press the ESC key while testing memory, only the last test is performed.
32	Test EISA Extended Memory	If EISA Mode flag is set, then test EISA memory found in slots Initialization. NOTE 1: This will be skipped in ISA mode. NOTE 2: This POST also Detect & Report I/O PORTS and also Init. Super IO.
33-3C	Reserved	Reserved
3C	Setup Enable	
3D	Initialize & Install PS/2 Mouse	Detect if mouse is present. Initialize mouse. Install interrupt vector.
3E	Setup Cache Controller	Initialize cache controller.
3F-40	Reserved	Reserved
41	Initialize Floppy Drive & Controller	1. Verify if we should enter setup. If so, enter setup. 2. Initialize floppy disk drive controller and any drive. Boot Block in EMERGENCY: Scan for Floppy for emergency disk…
42	Initialize Hard Drive & Controller	Initialize hard drive controller and any drive. (Call HD_INSTALL).
43	Detect & Initialize Serial/Parallel/Joystick ports	Initialize any serial, parallel and game ports.
44	Reserved	Reserved
45	Detect & Initialize Math Coprocessor	Initialize Math Coprocessor.
46	Reserved	Reserved
47	Set Speed for Boot	Set Speed for Boot.
48-4C	Reserved	Reserved
4D	Init. PC-Speaker to LINE OUT	Enable access to PC-Speaker to LINE OUT and Enable/Disable it. (T934).
4E	Manufacturing POST Loop or display Messages	1. Reboot if Manufacturing POST Loop pin is set. 2. Otherwise display any messages (i.e., any non-fatal errors that were detected during POST). 3. Enter SETUP if needed.
4F	Security Check	*Ask password security if needed.*
50	Write CMOS	Write all CMOS values back to CMOS-RAM and clear screen.

POST #	Designation	Description	
51	Pre-Boot Enable	1. Enable Parity checker. 2. Enable NMI. 3. Enable cache before boot.	
52	Initialize Option (ROM scan)	1. Call POST 81 2. Initialize any ROMs present from C8000h to DBFFFh. Disable POST code from segment E0000h. 3. Initialize any ROMs present from DC000h to E0800h. NOTE: When FSCAN option is enabled, will initialize from C8000h to F7FFFh.	
53	Initialize Time Value	Initialize Time value in 40h: BIOS area.	
54-5F	Reserved	Reserved	
60		Store boot partition of head & cylinder.	
61	Final Init	*For last µs detail before boot.*	
62	Num Lock ON	Put Num Lock ON and Daylight Saving.	
63	Boot Attempt	1. Call POST 82. 2. Set Low stack. 3. Boot via int 19h.	
64-7F	Reserved	Reserved	
80	Teknor Segment Move 1	Install the Teknor segment from Flash to DC00:0h.	
81	Teknor Segment Move 2	Install the Teknor segment from DC00:0h to 7000:0h.	
82	Teknor Segment Move 3	Install the Teknor segment from 7000:0h to EC00:0h.	
83	Check & Program CPLD	Check & Program CPLD for valid UserCode & IDCode.	
84	Teknor CRC Check	Check if Teknor block have a valid CRC. If not, the Emergency procedure is launched.	
85-AF	Reserved	Reserved	
B0	Spurious	If interrupt occurs in protected mode.	
B1	Unclaimed NMI	If unmasked NMI occurs, display: Press F1 to disable NMI, F2 reboot.	
B2-BD	Reserved	Reserved	
BE	Early Prog Chipset Def.	Going to early program chipset to default values (called from POST_8s).	
BF	Program Chip Set	Called early at POST 0Dh to program chipset from CT-TABLE.	
C0	Turn ON/OFF Cache	OEM Specific - Cache control.	Boot Block: First POST.
C1	Memory presence	OEM Specific - Test to size on-board memory test.	Boot Block: Search for Boot Block Signature "*BBSS*".
C2	Early Memory Initialization	OEM Specific - Board Initialization.	
C3	Extended Memory Initialization	OEM Specific - Turn ON extended memory DRAM select.	Boot Block: Expand compressed BIOS
C4	Special Display Switch Handling	OEM Specific - Display/Video switch handling so that display switch errors never occur.	
C5	Early Shadow	OEM Specific - Early Shadow enable for fast boot.	Boot Block: Early Shadow System BIOS.
C6	Cache Programming	OEM Specific - Routine for programming which region are cacheable.	Boot Block: Cache Sizing
C7	Reserved	Reserved	
C8	Special Speed Switching	OEM Specific - Routine to handle speed switching.	
C9	Special Shadow Handling	OEM Specific - Normal Shadow routine.	

POST #	Designation	Description
CA	Very Early Initialization	OEM Specific – Initialize hardware before any other hardware initialization.
CB-CF	Reserved	Reserved
D0	Power Management Full speed	Trying to go back or into full speed mode.
D1	Power Management -- Doze mode	Trying to go or in Doze mode.
D2	Power Management --Sleep mode	Trying to go or in Sleep mode.
D3	Power Management – Suspend mode	Trying to go or in Suspend mode.
D4-DF	Debug	Available POST codes for use by source code customers during development.
E0	Reserved	Reserved
E1-EE	Setup Page	Page 1 to Page 14
EF	Shadow Error	In POST 6 to signal a Shadow Error.
F0-FE	Reserved	Reserved
FF	Boot	The system is now booted or waiting for an OS.

F. EMERGENCY PROCEDURE

Follow this procedure only in case of emergency such as a critical error occurred during the Boot Block Flash BIOS update (when using UBIOS utility program or saving VIP-UP parameters flash) or if you meet one of the following symptoms at anytime:

1. No POST code on a power up (when using a POST card).
2. TEKNOR BIOS extension is not present.
3. System stops at POST 41(when using a POST card) and associated beep code is generated (Refer to Section E.1).
4. Board does not boot, even after usual hardware and connection verifications.

F.1 EMERGENCY PROCEDURE

To run an EMERGENCY PROCEDURE, proceed as follows:

1. Remove battery jumper.
2. Disable the Power Fail Detection function.
3. Connected a 1.44MB floppy drive (drive A) to the board, and insert the EMERGENCY diskette in it.
4. Power on the board. (Note that no VGA is present during this procedure.)
5. Boot block flash update will be completed when the POST code 55 is displayed (when using a POST card) or the associated beep code sounds (indicated in Section E-5).
6. After the procedure is successfully completed, power down the board, install your battery and Power Fail Detection jumpers.

   The boot block flash BIOS should be correctly programmed and the system should run properly.

NOTE

If the emergency disk has been lost, see section F.2 Generate a Emergency Floppy Diskette.

F.2 GENERATE AN EMERGENCY FLOPPY DISKETTE:

Use a system that has a 1.44 Mbytes floppy drive A.

1. Insert the TEKNOR EMERGENCY diskette in drive A:
2. Copy the two files WDISK.COM and EMERDISK.TEK from drive A: to your hard drive (those files are available in your TEKNOR diskette package).
3. Remove the TEKNOR EMERGENCY diskette and insert a DOS formatted floppy diskette in drive A:.
4. At the DOS prompt of your hard drive (same path of the two files WDISK.COM and EMERDISK.TEK), type WDISK then press Enter.
5. The program may display one of the following messages:

   "Emergency Code transferred"
   The emergency diskette has been successfully created. Take the appropriate actions and restart from the step 4) when you see the following messages.

   "Write to disk failure!"
   Verify if your floppy diskette is write-protected.

   "The file to program in flash was not found"
   Be sure that EMERDISK.TEK file is in your current path.

   "Unable to read the binary file" or "Unable to close the opened file"
   Possible floppy diskette corruption or bad data transfer between floppy disk and host system.

   "Unable to allocate a memory block of 256 Kbytes"
   Not enough memory to run the WDISK program.

GETTING HELP

At TEKNOR we take great pride in our customer's successes. We strongly believe in providing full support at all stages of your product development.

If at any time you encounter difficulties with your application or with any of our products, or if you simply need guidance on system setups and capabilities, you may contact our Technical Support department at:

CANADIAN HEADQUARTERS

Tel.: (450) 437-5682

Fax: (450) 437-8053

If you have any questions about TEKNOR, our products or services, you may reach us at the above numbers or by writing to:

TEKNOR INDUSTRIAL COMPUTERS INC.

616 Cure Boivin

Boisbriand, Quebec

J7G 2A7 CANADA

LIMITED WARRANTY

TEKNOR INDUSTRIAL COMPUTERS INC. ("the seller") warrants its boards to be free from defects in material and workmanship for a period of two (2) years commencing on the date of shipment. The liability of the seller shall be limited to replacing or repairing, at the seller's option, any defective units. Equipment or parts which have been subject to abuse, misuse, accident, alteration, neglect, or unauthorized repair are not covered by this warranty. This warranty is in lieu of all other warranties expressed or implied.

Returning Defective Merchandise

If your TEKNOR product malfunctions, please do the following before returning any merchandise:

1) Call our Technical Support department in Canada at (450) 437-5682. Make certain you have the following at hand: the TEKNOR Invoice #, your Purchase Order #, and the Serial Number of the defective board.

2) Give the serial number found on the back of the board and explain the nature of your problem to a service technician.

3) If the problem cannot be solved over the telephone, the technician will further instruct you on the return procedure.

4) Prior to returning any merchandise, make certain you receive an RMA # from TEKNOR's Technical Support and clearly mark this number on the outside of the package you are returning. To request a number, follow these steps: make a copy of the request form on the following page, fill it out and fax it to us.

5) When returning goods, please include the name and telephone number of a person whom we can contact for further explanations if necessary. **Where applicable, always include all duty papers and invoice(s) associated with the item(s) in question.**

6) When returning a TEKNOR board:

   i) Make certain that the board is properly packed: Place it in an antistatic plastic bag and pack it in a rigid cardboard box.

   ii) Ship prepaid to (but not insured, since incoming units are insured by TEKNOR):

TEKNOR INDUSTRIAL COMPUTERS INC.

616 Cure Boivin

Boisbriand, Quebec

J7G 2A7 CANADA

TEKNOR
INDUSTRIAL COMPUTERS INC.

RETURN TO MANUFACTURER AUTORIZATION REQUEST

Contact Name: _____

Company Name: _____

Street Address: _____

City: _____ **Province / State:** _____

Country: _____ **Postal / Zip Code:** _____

Phone Number: _____ **Fax Number:** _____

Extension: _____

Serial Number	Failure or Problem Description	P.O. # (if not under warranty)

ref.: RMA-03

Fax this form to TEKNOR's Technical Support department in Canada at (450) 437-8053