RAP-C810

3U CompactPCI® System Processor

Technical Reference Manual
Version 1.3, February 2003

Note: The latest releases of the Technical Reference Manuals are available at:
ftp://ftp.kontron.ca/Support

www.kontron.com

Ref. : M3001_TECH

FOREWORD.

The information in this document is provided for reference purposes only. Kontron does not assume any liability for the application of information or the use of products described herein.

This document may contain information or refer to products protected by the copyrights or patents of others and does not convey any license under the patent rights of Kontron, nor the rights of others.

Printed in Canada.
Copyright 2003 Kontron, Inc., Boisbriand, Qc J7G 2A7.

DOCUMENTATION SURVEY

RAP-C810 – Technical Reference Manual

Your comments are valuable for us and will contribute to improve the quality of this product by complementing and returning this form.

1. Overall rating of the Technical Reference Manual: ❑ Excellent ❑ Satisfactory ❑ Fair ❑ Poor

Did you find easily the information you were seeking for? ❑ Yes ❑ No

If no, can you comment? _____

2. What section of this manual do you refer to the most? _____

3. How can you rate this manual?

In terms of clarity of information: ❑ Excellent ❑ Satisfactory ❑ Fair ❑ Poor

Comments: _____

_____

In terms of complexity: ❑ Too technical ❑ Just OK ❑ Not technical enough

Comments: _____

_____

In terms of classification of information: ❑ Excellent ❑ Satisfactory ❑ Fair ❑ Poor

Comments: _____

_____

5. Is some information missing in this book? ❑ Yes ❑ No

If yes, what information is missing?_____

_____

6. Is some information not properly or clearly explained? ❑ Yes ❑ No

If yes, can you comment?_____

_____

7. Additional comments (suggestions, errors found, etc.):_____

_____

_____

Please send your comments to:

Kontron inc.
Technical Writing dept.
616 Curé Boivin, Boisbriand
(Québec) CANADA J7G 2A7

Optional

Name _____

Company _____

Address _____

_____

_____

ADDITIONAL COMMENTS

READ ME FIRST

Your computer board has a standard non-rechargeable lithium battery. To preserve the battery lifetime, **the battery enable jumper is removed when you receive the board**. If you do not have any jumper cap, we suggest you to use the Watchdog Timer jumper cap.

EXERCISE CAUTION WHILE REPLACING LITHIUM BATTERY

WARNING

Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.

ATTENTION

Il y a danger d'explosion s'il y a remplacement incorrect de la batterie.

Remplacer uniquement avec une batterie du même type ou d'un type équivalent recommandé par le constructeur. Mettre au rebut les batteries usagées conformément aux instructions du fabriquant.

ACHTUNG

Explosionsgefahr bei falschem Batteriewechsel. Verwenden Sie nur die empfohlenen Batterietypen des Herstellers. Entsorgen Sie die verbrauchten Batterien laut Gebrauchsanweisung des Herstellers.

ATENCION

Puede explotar si la pila no este bien reemplazada.

Solo reemplazca la pila con tipas equivalentes segun las instrucciones del manifacturo. Vote las pilas usadas segun las instrucciones del manifacturo.

POWERING-UP THE BOARD

If you should encounter a problem, verify the following items:

Make sure that all connectors are properly connected.

Check your boot diskette.

If the board still does not start up properly, you should try booting your system with only the RAP-C810 installed in the system, a monitor and a mouse connected to the board. This is the minimum required to verify the board's operation.

If you still are not able to verify your board, please refer to the Emergency Procedure in the Appendix Section.

If you still are not able to get your board up and running, contact our Technical Support Department for assistance.

PREVENTING VIRUSES

Kontron Inc. takes every precaution against computer viruses.
To safeguard against computer viruses, regularly perform virus scans on all your computer systems. Contact our Technical Support department for further instructions at (450) 437-5682 (Canada).

ADAPTER CABLES

While adapter cables are provided from various sources, the pinout is often different. The direct crimp design offered by Kontron allows the simplest cable assembly. All cables are available from Kontron Sales Department.

UNPACKING AND SAFETY PRECAUTIONS

STATIC ELECTRICITY

Since static electricity can cause damage to electronic devices, the following precautions should be taken:

1. Keep the board in its anti-static package, until you are ready to install it.
2. Touch a grounded surface or wear a grounding wrist strap before removing the board from its package; this will discharge any static electricity that may have built up in your body.
3. Handle the board by the edges.

Storage Environment

Electronic boards are sensitive devices. Do not handle or store devices near strong electrostatic, electromagnetic, magnetic or radioactive fields.

Power Supply

Before any installation or setup, ensure that the board is unplugged from power sources or subsystems.

Unpacking

Follow these recommendations while unpacking:

1. After opening the box, save it and the packing material for possible future shipment.
2. Remove the board from its anti-static wrapping and place it on a grounded surface.
3. Inspect the board for damage. If there is any damage or missing items, notify Kontron immediately.

When unpacking you will find:

1. One RAP-C810, 3U CompactPCI® SSystem Processor Processor.
2. One Quick Reference sheet
3. One CDROM containing drivers.

TABLE OF CONTENTS

1 PRODUCT DESCRIPTION 1

1.1 PRODUCT SPECIFICATIONS 1-1

1.1.1 CompactPCI Connectors 1-1

1.1.2 Intel's 810 Chipset 1-1

1.2 RAP-C810 TECHNICAL SPECIFICATIONS SHEET 1-6

1.2.1 Power requirements 1-11

1.3 INTERFACING WITH THE ENVIRONMENT 1-12

1.3.1 CPCI 1-12

1.3.2 Compatibility with OTHER Kontron Products 1-12

1.4 KONTRON'S CMC MEZZANINE CONCEPT 1-12

1.4.1 PMC Concept 1-13

1.4.2 CompactFlash Feature 1-13

2 ONBOARD FEATURES 2-1

2.1 COMPACTFLASH INTERFACE 2-1

2.2 ENHANCED IDE INTERFACES 2-2

2.3 ETHERNET INTERFACE 2-3

2.3.1 Boot from LAN 2-3

2.3.2 Drivers 2-3

2.4 FLOPPY DISK INTERFACE 2-4

2.5 PS/2 KEYBOARD / PS/2 MOUSE INTERFACE 2-4

2.6 PARALLEL PORT 2-5

2.6.1 Standard Mode 2-6

2.6.2 EPP Mode 2-6

2.6.3 ECP Mode 2-6

2.7 SERIAL PORTS 2-7

2.7.1 Serial Port 1 2-7
2.7.2 Serial Port 2 2-7
2.8 POWER MANAGEMENT 2-9
2.9 THERMAL MANAGEMENT 2-9
2.10 USB INTERFACES 2-10
2.11 VIDEO INTERFACE 2-10
2.11.1 Supported Resolutions 2-11
2.11.2 Major Features Description 2-11
3 INSTALLING THE BOARD 3-1
3.1 SETTING JUMPERS 3-1
3.2 REGISTER'S DESCRIPTION 3-2
3.2.1 Serial Port 2 Configuration 3-2
3.2.2 History and monitor status 3-3
3.2.3 History status 3-3
3.2.4 Monitoring status and I/O access 3-3
3.2.5 Digital watchdog 3-4
3.2.6 NMI Control 3-4
3.2.7 Register BITs description (summary) 3-5
3.3 RAP-C810 BLOCK DIAGRAM 3-6
3.3.1 Onboard Connectors and Headers 3-7
3.3.2 Front Plate Connectors and Indicators 3-8
3.3.3 CompactPCI Connectors 3-9
3.4 CUSTOMIZING THE BOARD 3-9
3.4.1 Processor 3-9
3.4.2 Backup Battery 3-10
3.4.3 SDRAM System Memory 3-10
3.4.4 Supervision Features 3-12
3.4.5 Storage Devices 3-16

3.4.6 Installing the Board into a Bay 3-16
3.4.7 Connector Keying 3-16
3.4.8 Connection 3-17

4 SOFTWARE SETUPS 1

4.1 BIOS SETUP PROGRAM 4-1
4.1.1 Accessing the BIOS setup program 4-1
4.1.2 The Menu Bar 4-3
4.2 BOOT UTILITIES 4-14
4.2.1 Phoenix QuiteBoot 4-14
4.3 UPDATING OR RESTORING THE BIOS IN FLASH 4-16
4.4 VT100 MODE 4-16
4.4.1 Requirements 4-16
4.4.2 Setup & Configuration 4-16

APPENDICES

A. MEMORY & I/O MAPS A-1

A.1 Memory Mapping A-1

A.2 I/O Mapping A-1

B. INTERRUPT LINES B-1

B.1 IRQ Lines B-1

B.2 DMA Channels B-1

C. BOARD DIAGRAMS C-1

C.1 Assembly Top Diagram C-1

C.2 Assembly Bottom Diagram C-3

C.3 Mounting Holes C-5

D. CONNECTOR PINOUTS D-1

D.1 RAP-C810 Connectors and Headers D-1

D.1.1J1 CPCI Bus Connectors D-2

D.1.2J2 CPCI Bus Connectors D-3

D.1.3J3 - VGA Connector D-4

D.1.4J4 Parallel Port Connector D-4

D.1.5J5 – CPU Fan AND tachometer D-4

D.1.6J6 – Ethernet D-4

D.1.7J7 - USB (FacePlate) D-5

D.1.8J8 & J10 – Serial Port 2 & 1 - RS-232 ..... D-5

D.1.9J8 & J10 – Serial Port 2 & 1 - RS-232 (Onboard header) D-5

D.1.10 J9 – Keyboard and Mouse PS/2 Connector D-6

D.1.11 J11 – Floppy Disk D-6

D.2 J13 – Primary IDE Connector D-7

D.2.1J13 - Mezzanine Connector D-8

D.2.2J14 - Mezzanine Connector D-9

E. BIOS SETUP ERROR CODES.....E-1

E.1 POST Beep.....E-1

E.2 POST Messages.....E-1

E.3 Error Messages.....E-1

F. EMERGENCY PROCEDURE F-1

G. GETTING HELP..... G-1

G.1 Returning Defective Merchandise.....G-1

PART 1

1 PRODUCT DESCRIPTION

1. **PRODUCT SPECIFICATIONS**
2. **RAPC-810TECHNICAL SPECIFICATION SHEET**
3. **INTERFACING WITH THE ENVIRONMENT**
4. **KONTRON'S cMC MEZZANINE CONCEPT**

1.1 PRODUCT SPECIFICATIONS

Kontron's 500MHz Celeron-powered RAP-C810 offers the best value for rock-solid performance in a 3U footprint. Delivering on form, fit and function migration, the RAP-C810 is indispensable to the upscale demands of the test and measurement, in-vehicle (transportable), and automation markets.

Using Intel's Celeron processor, with 66MHz Front side bus and 128KB 64-bit wide L2 cache, the RAP-C810 also combines the latest Intel chipset solution with integrated 2D/3D graphics, and up to 128MB of Synchronous SDRAM on one 144-pin SODIMM socket, to ensure a superior processing capacity.

Part of Kontrons new RAPtor (Ruggedized Applied Platform) line of CompactPCI system processors, the RAP-C810 is built on the same successful technology derived from its family of VIPer half-size single board computers (SBCs).

With its high-density onboard integration, the RAP-C810 also supports up to seven full hot swap peripheral cards, and an assortment of key software interfaces, including Windows® 2000, MS-DOS™, Windows®95/98, Windows®NT, and other OSs.

1.1.1 CompactPCI Connectors

CPCI connectors are PICMG 2.0 Rev 2.1 as well as PICMG 2.0 Rev 3.0 compliant. CompactPCI connectors are located at the rear edge of the processor board. The complete CPCI connector configuration of the RAP-C810 is composed of two connectors referred to as J1 and J2.

Their function is described below:

J1/ 32 bit PCI signaling, power

J2 64 bit extension, arbitration, clocks, reset and. power

CompactPCI™ connectors are also known as 2mm Hard Metric connectors.

1.1.2 Intel's 810 Chipset

The RAP-C810 uses the Intel's 810 Chipset. Here are the main highlights:

- **Highly integrated chipset**
  - Integrated 2D/3D video engine
  - integrated RAMDAC
- **Support Celeron®**
  - 66MHz ot 100MHz host bus
- **Memory**

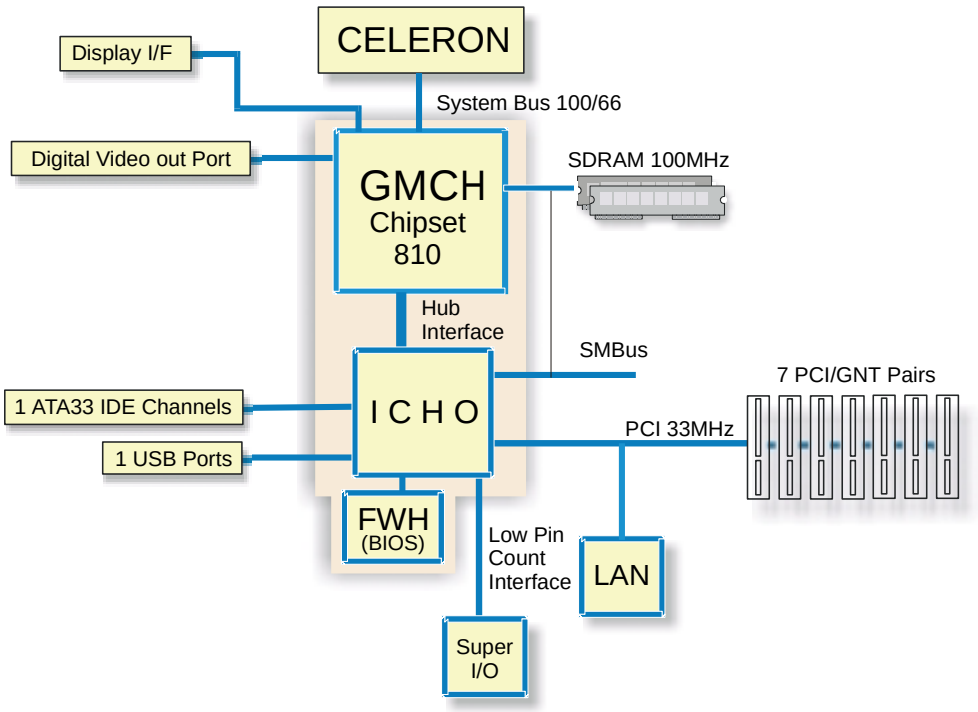
- PC100 SDRAM interface
- Up to 128MB on one SO-DIMM
- Support 32MB/64MB/128MB technology

- **AC97 Support**
  - Sound capability with external CODEC
  - MODEM capability with external CODEC and DAA
- **USB**
  - Support 1 USB ports
- **Firmware Hub**
  - Flash BIOS on LPC bus
  - 2/4/8 Mbits capacity
- **Super IO**
  - Super IO on LPC bus
- **Flat Panel**
  - Support Panel Link (DVI) Flat Panel via DVO port

The Intel® 810 Chipset architecture also enables a new security and manageability infrastructure through the Firmware Hub component. It also removes the requirements for the ISA expansion bus that was traditionally integrated into the I/O subsystem of PCIsets/AGPsets.

The Intel 810 Chipset contains three core components (see diagram)

- The Graphics and Memory Controller Hub (GMCH)
- The I/O Controller Hub (ICH)
- The Firmware Hub (FWH) also referred as BIOS



The GMCH integrates a 66/100MHz bus controller, integrated 2D/3D graphics accelerator, 100MHz SDRAM controller and a high-speed hub interface for communication with the ICH0/ICH. The ICH integrates an Ultra ATA/33 or Ultra ATA/66 (ICH) controller, USB host controller, LPC interface controller, FWH interface controller, PCI interface controller, AC'97 digital controller and a hub interface for communication with the GMCH.

1.1.2.1 The GMCH

The GMCH provides the interconnect between the SDRAM and the rest of the system logic:

- 421 MINI BGA
- Integrated Graphics controller
- 230MHz RAMDAC
- Support for Intel® Celeron™ processors with a 66MHz or 100MHz system bus
- 100MHz SDRAM interface supporting 32MB/64MB/128MB SDRAM
- Downstream hub interface for access to the ICH
- Tvout/Flat Panel Display support

1.1.2.2 The Controller Hub (ICH)

The I/0 Controller Hub provides the I/O subsystem with access to the rest of the system:

- 241 Mini BGA
- Upstream hub interface for access to the GMCH
- PCI2.2 interface
- Bus Master IDE controller – supports either Ultra ATA/33 or Ultra ATA/66 (ICH)
- USB controller
- I/O APIC
- SMBus controller
- FWH interface
- LPC interface
- AC'97 2.1 interface
- Integrated System Management Controller
- IRQ controller

1.1.2.3 The Firmware Hub (FWH)

The FWH component is a key element to enabling a new security and manageability infrastructure for the PC platform. The device operates under the FWH interface and protocol. The hardware features of this device include:

- An integrated hardware Random Number Generator (RNG)
- Register-based locking
- Hardware-based locking
- 5 GPI's

1.2 RAP-C810 TECHNICAL SPECIFICATIONS SHEET

Features	Description
CPU	• Celeron processor – 300/66 MHz to 566/66 MHz and future processor speeds
Chipset	• Intel 810
Bus Interfaces	• Front side bus 66 MHz up to 100MHz • CompactPCI® Bus, 32-bit (33MHz) J1 and J2 • Internal chipset bridging and supports up to 7 REQ/GNT for fully loaded CompactPCI® system • Proprietary mezzanine with FD, EIDE, and Compact Flash support • SMBus (for system management of CPU temperature monitoring, DRAM control, Clock buffers and power control)
Cache	• 16K/16K Instruction / Data CPU-internal Level 1 • 256KB 64-bit wide on-die Level 2 pipelined burst
Memory	• Up to 128MB of Synchronous SDRAM on one 144-pin SODIMM socket • Memory bus speed always at 100MHz (PC-100)
Data Path	• 64-bit on CPU and video memory; 32-bit on local PCI and CompactPCI bus
Interrupts	• 4 PCI level sensitive, configurable to any interrupt vector for PnP compatibility
Flash Memory	• 512KB for BIOS field upgrade • Silicon Serial ID TAG for unique board identification accessible via software • 4Kbytes Serial EEPROM for user configuration

RAP-C810 Technical Specifications Sheet (cont'd)

Features	Description
I/O	• LPC 47B277 Super I/O Controller • USB Ports : One • Serial Ports: COM1, RS-232, , front-accessible COM2 configurable as RS-232/422/485, backplane accessible via mezzanine) • Parallel Port : One bi-directional with all IEEE 1284 protocols supported with BIOS selectable IRQs and addressing • Floppy Disk: Support for two drives (1.44MB) • EIDE: One channel Bus Master PCI EIDE; Support for two IDE drives (type 1 to 4, master/slave configuration); LBA, PIO Mode 0-4 and Ultra DMA/33, DMA/66 • CompactFlash™ Module: Optional bootable CompactFlash™ disk (type 1 or 2) interfaces to primary EIDE channel, user upgradeable, master/slave • Ethernet: One Ethernet, PCI 10/100Base-TX ports (Intel 82559 controller) • HD/FD Mezzanine Card: Optionally onboard using Kontron's cMC series mezzanine cards
Video	• 64-bit AGP video controller (Intel 69000) with 2MB on die video memory • CRT resolutions up to 1600 x 1200 at 256 colors; 1024 x 768 at 65536 colors
Clock/Calendar	• Real-time clock with (replaceable) battery backup • CMOS RAM

RAP-C810 Technical Specifications Sheet (cont'd)

Features	Description
Connectors in "Front" configuration	• CRT (15-pin D-sub) • Parallel (25-pin D-sub) • Serial COM1 (9-pin D-sub) • Ethernet port (RJ-45 with link/activity indicators) • PS/2 mouse/keyboard (6-pin midi-Din)
Onboard headers	• EIDE (40-pin, shrouded • Floppy Disk (34-pin, shrouded) • Serial COM 1 and COM2 (10-pin) • Parallel Port (26-pin) • Mezzanine and DVO (two 50-pin) • CPU fan (3-pin locking)
BIOS Features	• Phoenix BIOS in Boot Block Flash with emergency recovery code; save CMOS in Flash option, and boot from LAN capability • Auto configuration, extended setup; • Setup console redirection to serial port (VT100 mode) with CMOS setup access • Software enable/disable of onboard Ethernet; hardware enable/disable of onboard video • Diskless, keyboardless, and videoless operation extensions • System, video, and LAN BIOS shadowing • Programmable bus and I/0 speeds and memory wait states • Advance security feature for floppy and HDD; DMI and HDD S.M.A.R.T. support • Advanced Power Management (APM 1.2), advanced thermal management (resume, overheat alarm and auto slow down), and Green support

RAP-C810 Technical Specifications Sheet (cont'd)

Features	Description
Supervisory	• Two-stage software programmable Watchdog timer drives NMI on first stage and system reset on second stage • Programmable CPU temperature monitor/alarm • Power failure/low battery detector • Front Panel LEDs: IDE activity, Ethernet activity and link • Voltage monitoring of 1.5V, 2.5V, 3,3V, 5V, 12V, VBAT and Vcore voltage rails
OS Compatibility	• MS-DOS™, Windows® 95/98, Windows® NT, Windows2000, QNX™, Linux, (VxWorks™, pSOS™, and Solaris for future compatibility)
PICMG compliance	• Mechanical compliant to IEEE 1101.10; compliant to PICMG 2.0 Rev 2.1 and PICMG 2.1
Form Factor	• 100 x 160 x 41 mm / 3.9 x 6.3 , 1.6 in; 3U x 8HP (dual slot) • 233 x 160 x 20.5 mm / 9.2 x 6.3 , 0.8 in; 6U x 4HP (dual slot) Mechanically
Power Requirements	• Supply Voltages: +3.3V: ±5% +5V±5% +12V±5% • Supply Current * : 3.3V: 1.3A (1.60A max) 5V 2.7A (4.59A max) 12V: 0.1A (0.12A max) • Power Dissipation: 35W max. *Tested with Celeron processor, 433MHz with 128MB SDRAM*.

RAP-C810 Technical Specifications Sheet (cont'd)

Features	Description		
Environmental		**Operating**	**Storage and Transit**
	Temp.:	0-55°/32-140°F (w/ 150LFM airflow)	-40° to +70° / -40° to 158°F
	Humidity	5% to 95% @ 40°C/104°F non-condensing	5% to 95% @ 40°C/104°F non-condensing
	Altitude	4,572m / 15,000ft	
	Shock	Designed to meet IEC 68-2-27	
	Vibration	Designed to meet IEC 68-2-6	
Reliability	• MTBF:> 100,000 hours @ 55°C/131°F (MIL-HDBK-217F) • Board serial number in EEPROM • USB, keyboard, mouse voltage protected by self-resetting fuses • 2 year limited warranty		
Safety	• Designed to meet or exceed UL 1950; CSA C22.2 No 950; EN 60950; IEC950		
EMI/EMC	• FCC 47 CFR Part 15/CISPR22, Class B; CE Mark to EN55022/EN50082		

1.2.1 Power requirements

The power requirements for the RAP-C810 are specified as follows:

CPU	VCORE	Frequency (MHz) Int/Ext	Power MAX (Watts) 3.3V/5V/12V	Power TYP (Watts) 3.3V/5V/12V	Ambient temp MAX
Celeron	2.0V	300/66	4.0 **/** 16.3 **/** 1.3	4.0 **/** 9.8 **/** 1.2	55 C
Celeron	2.0V	366/66	4.1 **/** 19.7 **/** 1.3	4.1 **/** 11.6 **/** 1.2	55 C
Celeron	2.0V	433/66	4.1 **/** 23.0 **/** 1.3	4.1 **/** 13.5 **/** 1.2	55 C
Celeron	2.0V	500/66	4.1 **/** 26.6 **/** 1.3	4.1 **/** 15.6 **/** 1.2	55 C
Where :					
Power MAX		Running HiPower 3.0 in Windows98SE®			
Power TYP		Doing nothing in DOS 6.22			
Test condition		128MB SDRAM, running Windows98SE®,			

1.3 INTERFACING WITH THE ENVIRONMENT

1.3.1 CPCI

The RAP-C810 peripheral processor allows rack-mounted systems to offer a high level of modularity.



NOTE

The following I/Os are supported on the faceplate SVGA, COM1, LPT1, Ethernet 1, USB, keyboard and mouse.

The following I/Os are available through onboard headers: COM1, COM2, LPT1, Ethernet 1, USB, keyboard and mouse, floppy disk and IDE drives.

All I/O signals are available though the mezzanine connectors.

1.3.2 Compatibility with OTHER Kontron Products

The RAP-C810 Peripheral Processor is a member of the Kontron's CompactPCI product family.

The board is fully compliant with the PICMG 2.0 Rev.2.1 and PICMG 2.1 CompactPCI specifications.

When building a basic environment around the RAP-C810, the platform may be composed of any of the following devices:

1.4 KONTRON'S CMC MEZZANINE CONCEPT

This is Kontron's concept to expand the I/O capability of the board. It is built around two connectors:

- Mezzanine connector handling IDE and floppy disk drive signals.
- Mezzanine connector handling a complete PCI signal set (primary bus) including the REQ/GNT arbitration signal pair.

These two connectors represent an open door for future development of expansion and I/O mezzanine cards.

Kontron developed two series of mezzanine cards: the cMC and the cMCB series. The RAP-C810 supports the cMC series.

1.4.1 PMC Concept

Kontron's PCI Mezzanine Card (PMC) allows PCI based I/O devices to be added to the RAP-C810.

The RAP-C810 features the PMC support onboard to provide an extra method to expand the 32-bit I/O capabilities.

1.4.2 CompactFlash Feature

The RAP-C810 boards also support standard CompactFlash disk through a CompactFlash carrier module.

CompactFlash is a widely available non-volatile memory device electrically configured in a way as to interface directly through IDE. It is supported on the board as a standard IDE drive and connects to the primary EIDE interface.

The CompactFlash disk can be set as a Master or Slave device and combined with any EIDE standard hard disk drive via W1 jumper (located on Raptor's Mezzanine).

The CompactFlash module is installed using the RAP-C810 on-board J13 and J14 connectors. For more information on CompactFlash installation and setups, please refer to Section 2.1 – *CompactFlash Interface*.

PART 2

2 ONBOARD FEATURES

1. COMPACTFLASH INTERFACE
2. ENHANCED IDE INTERFACES
3. ETHERNET INTERFACES
4. FLOPPY DISK INTERFACE
5. PS/2 KEYBOARD AND MOUSE INTERFACE
6. PARALLEL PORT
7. SERIAL PORTS
8. POWER MANAGEMENT
9. THERMAL MANAGEMENT
10. USB INTERFACES
11. VIDEO INTERFACES

2.1 COMPACTFLASH INTERFACE

The RAP-C810 board supports an IDE compatible flash disk by using a CompactFlash carrier module connected to the Kontron's mezzanine. CompactFlash (C-Flash) disks are the resident industry-standard ATA/IDE subsystem for application, data, image, and audio storage. They have the same functionality and capabilities as intelligent disk drives, but with the advantages of being very compact, rugged (typical M.T.B.F. is 1,000,000 hours) and low power. The RAP-C810 supports all CompactFlash sizes presently available and future sizes when available.
The C-Flash disk connects on the RAP-C810 via the onboard Flash Disk connector located on the T3501 Mezzanine.

Related Jumpers
W1 to set the CompactFlash disk as master or slave (Located on the CompactFlash disk).

BIOS Settings
Section 4.1.2.4 Main Menu Selection, Primary Master or Primary Slave, Auto.

The CompactFlash disk connects directly on the primary EIDE interface. It must be configured the same way as a standard hard disk using the BIOS setup program (Autodetect function).

To setup the CompactFlash disk for Master or Slave configuration, use the CompactFlash jumper (W1) located on the mezzanine board.

To locate and install this jumper, please refer to Section 3.1, *Setting Jumpers*.



NOTE

Since CompactFlash devices use the ATA/IDE interface, no specific flash disk driver is required for various operating systems.

2.2 ENHANCED IDE INTERFACES

The RAP-C810 board features one channel Bus Master PCI EIDE dedicated to Primary IDE logical interface. The channel supports up to two IDE devices (including CD-ROMs, hard disks, CompactFlash) with independent timings, in Master/Slave combination.

Signal Paths

The primary IDE interface is available on the CPCI I/O connectors, the mezzanine connector and the Compact Flash connector.

Related Jumpers
None

BIOS Settings
Section 4.1.2.4 Main Menu Selection, Primary Master or Primary Slave.

Section 4.1.2.5 Advanced Menu Selection, I/O Device Configuration, Local Bus IDE Adapter, Enabled or Disabled.

See also section 4.1.2.5 Advanced Menu Selection, I/O Device Configuration, Large Disk Access Mode and LBA Translation Type.

The IDE interface supports PIO mode 4 transfers up to 14MB/sec and Bus Master IDE transfer up to 66MB/sec (Ultra-DMA 66). It does not consume any ISA DMA resources and integrates 16x32-bit buffers for optimal transfers.



CAUTION

When connecting IDE devices to the Primary IDE interface, Master and Slave devices must be shared in respect of the device allocation on both the CPCI I/O connector and the mezzanine

Two Master devices (or two Slave devices) must not be installed on the same interface at the same time.

2.3 ETHERNET INTERFACE

The Ethernet controller is electrically connected to the Primary PCI bus. It supports 10Base-T and 100Base-TX operations: 10Mbps and 100Mbps network speeds are automatically detected and switched.

Signal Path

The Ethernet interface is available through the Front Panel connector J6.

Related Jumpers

None.

BIOS Settings

Section 4.1.2.5, Advanced Menu Selection, Advanced Chipset Control, Onboard Ethernet Controller, Enable or Disable.

See also Boot Menu Selection, Network Boot.

2.3.1 Boot from LAN

The Boot from LAN capability is supported. To enable the option, use the BIOS Setup program. Please refer to Section 4.1.2.7, Boot Menu Selection for Bios Setting.

2.3.2 Drivers

A CDROM is included with the RAP-C810. It contains network drivers for most common operating systems.

2.4 FLOPPY DISK INTERFACE

The onboard floppy disk controller is IBM PC XT/AT compatible. It handles 3.5" and 5.25", low and high density disks. Up to two drives are supported in any combination.

Signal Paths

The Floppy Disk Controller interface is available through the through the Mezzanine connector (see section 1.4.1)

Related Jumpers

None.

BIOS Settings

Section 4.1.2.4 Main Menu Selection, Legacy Diskette A:or Legacy Diskette B. Select the type of floppy installed.

Section 4.1.2.5 Advanced Menu selection, I/O Device Configuration, Floppy disk controller (Enabled, Disabled, Auto or OS Controlled).

2.5 PS/2 KEYBOARD / PS/2 MOUSE INTERFACE

The onboard keyboard controller is 8042 software compatible. PS/2 Keyboard and mouse signals are available through an output that supports direct connection to the interface. Since signals of both devices are combined on the same connector, a Y-cable is required to split the signals and feed a standard AT keyboard and a PS/2 mouse. The part number for this cable is : 150-381-00.

Signal Path

PS/2 keyboard and PS/2 mouse signals are available through the mini-Din connector on the face plate.

Related Jumpers

None.

BIOS Settings

None

2.6 PARALLEL PORT

The RAP-C810 features one IEEE-1854 multi-mode parallel port. It is compatible with Standard Mode IBM PC/XT, PC/AT, and PS/2 compatible bi-directional parallel port, Enhanced Parallel Port (EPP), and Enhanced Capabilities Port (ECP).

Signal Path

The Parallel Port interface is available through the front panel connector J4.

Related Jumpers

None

BIOS Settings

Section 4.1.2.5, Advanced Menu Selection, I/O Device Configuration, Parallel Port (Enabled, Disabled, Auto or OS Controlled).

Section 4.1.2.5, Advanced Menu Selection, I/O Device Configuration, Parallel Port Mode, (Output only, Bi-directional EPP and ECP.

The differences between Standard, EPP, and ECP modes appear in the signal assignation of the pins on the connector. Differences are described as follows:

Pin Number (J5)	Standard Mode	EPP Mode	ECP Mode
A15	SLCT	-	SLCT
B15	PE	-	PERROR[1], ACKREVERS[2]
C15	BUSY	WAIT	BUSY[1], PERIPHACK[2]
D15	/ACK	/INTR	/ACK
E16	/SLCTIN	/ADDRSTRB	/SLCTIN
B17	/INIT	-	/INIT[1], /REVERSERQST[2]
D17	/ERR	-	/FAULT[1], /PERIPHRQST[2]
A18	ALF	DATASTB	ALF[1], HOSTACK[2]
E17	PD0	PD0	PD0
C17	PD1	PD1	PD1
A17	PD2	PD2	PD2
D16	PD3	PD3	PD3
C16	PD4	PD4	PD4
B16	PD5	PD5	PD5
A16	PD6	PD6	PD6
E15	PD7	PD7	PD7

[1] Compatible mode [2] High Speed Mode

NOTE
To operate in EPP or ECP mode, ensure the peripheral is designed to work in this mode and the BIOS setup is configured to support it.

2.6.1 Standard Mode

The Standard mode is unidirectional. It is supported to maintain the compatibility with the IBM PC standard.

2.6.2 EPP Mode

The EPP (Enhanced Parallel Port) mode consists of a hardware independent method of accessing a parallel port configured as EPP. It provides support for single I/O cycle as well as the high performance block I/O transfers. The EPP mode always uses the most optimum method for I/O transfers. For example, if the hardware supports it, EPP mode will perform 32-bit I/O block transfers.

EPP mode assumes that the parallel port can be used to connect more than one peripheral device using multiplexor or daisy chain configurations.

A multiplexor is an external device that permits up to eight parallel port devices to share a single parallel port.

A daisy chain device has two ports: input and output. The input port is connected either to the host parallel port or the daisy chain device in front of it. The output is used to connect the next peripheral device to the daisy chain. The last device, however, can be one without daisy chain support.

2.6.3 ECP Mode

ECP (Extended Capabilities Port) works the same as EPP mode, but it will take precedence over the EPP mode when addressing multiple logical devices in a single physical product. While the EPP mode may intermix read and write operations without any overhead or protocol handshaking, the ECP mode negotiates data transfers using a request from the host and an acknowledgment from the peripheral.



NOTE

For more information on the ECP protocol, please refer to the Extended Capabilities Port Protocol and ISA Interface Standard (available from Microsoft Corporation) or contact our Technical Support department (See appendix G).

2.7 SERIAL PORTS

Two full function serial ports are provided on the board for asynchronous serial communications. They are 16C550 high-speed UART compatible and support 16-byte FIFO buffers for transfer rates from 50bps to 115Kbaud.

UART registers are individually addressable and fully programmable.

2.7.1 Serial Port 1

Serial Port 1 is buffered directly for RS-232 operation. Signals include the complete signal set for handshaking, modem control, interrupt generation, and data transfer. When assigned as COM1, the port is 100% compatible with the IBM-AT serial port in RS-232 mode.

Signal Path

Serial Port 1 signal is available through J10 located on the Raptor's board or through the faceplate DB9 connector labeled as COM1.

Related Jumpers

None

2.7.2 Serial Port 2

The serial port 2 is buffered directly for RS-232, RS-422 or RS-485 operations and is 16C550 PC-Compatible. The interface includes the complete signal set for handshaking, modem control, interrupt generation, and data transfer.

The serial port 2 is 100% compatible with the IBM-AT serial port.

Signal Path

Serial Port 2 signals are only available through J8 10-pin header.

Related Jumpers

None

2.7.2.1 RS-232 Protocol

When configured for RS-232 operation mode, the Serial Port 2 is 100% compatible with the IBM-AT serial port signals.

2.7.2.2 RS-422 Protocol

The RS-422 protocol (Full Duplex) uses both RX and TX lines during a communication session.

> **CAUTION**
>
> In RS-422 mode, W1 and W2 jumper caps must be installed to connect the 120 ohms termination resistors (See Section 3.1 *Jumper Settings*)

2.7.2.3 RS-485 Protocol

The RS-485 protocol (Full Duplex) also uses differential signals during a communication session. It differs from the RS-422 mode as it offers the ability to transmit and receive over the same pair of wires, and allows the sharing of the communication line by multiple stations. This configuration (also known as Party Line) allows only one system to take control of the communication line at the time.

In RS-485 mode, the RX lines are used as the transceiver lines, and the RTS signal is used to control the direction of the RS-485 buffer.

When set for RS-485 mode in the BIOS, upon power-up or reset, the transceiver is by default in receiver mode to prevent unwanted perturbation on the line. Party line operation mode requires termination resistors to be installed at both ends of the network.

> CAUTION
>
> When installing the RAP-C810 at one end of the network, W1 and W2 jumper caps must be installed to connect the 120 ohms termination resistors (See Section 3.1 – *Setting Jumpers*).

2.8 POWER MANAGEMENT

Power Management features are supported at the BIOS level. All Power Management options are described this section.

2.9 THERMAL MANAGEMENT

One temperature sensors are provided to supervise the thermal environment. One is used to monitor the CPU die temperature.

The temperature is controlled according to two temperature levels, the Low temperature limit, which indicates normal operating conditions, and the High temperature limit, which indicates an overheating condition.

The temperature management consists in reducing the CPU clock speed (throttling) when the temperature goes over the high limit (overheating condition) and suspending the throttling operation as soon as the temperature returns under the low temperature limit (normal condition).

The clock speed may be throttled due to CPU overheating caused by the system cooling failure. In such a case, the temperature control is triggered as soon as the temperature reaches the high temperature limit of the die.

The ambient temperature of the CPU generally raises up due to an augmentation of the temperature in the casing. In that case, the clock speed will be slowed down as soon as the ambient temperature reaches the high ambient temperature value.

Thermal management operations are controlled by the ICH, and settings are provided through the BIOS setup program interface, *Thermal Management Setup* option (See Section 4.1.10 *CPU Board Feature Setup, Thermal management Options).*

2.10 USB INTERFACES

Signals for one USB port are available through the J7 located on the faceplate.

USB is becoming the new essential peripheral interface. The USB strengths are as follows: capability to daisy chain as many as 127 devices per interface, fast bi-directional, isochronous/asynchronous interface, 12Mbps transfer rate, and standardization of peripheral interfaces into a single format.

Signal Paths
None

Related Jumpers
None

USB supports Plug and Play and hot swapping operations (OS level). These user-friendly features allow USB devices to be automatically attached, configured and detached, without reboot or running setup.

The RAP-C810 board fully supports the standard universal host controller interface (UHCI) and uses standard software drivers that are UHCI-compatible.

2.11 VIDEO INTERFACE

The high-performance video capability of the board is based on Accelerated Graphics Port (AGP) technology. The video controller with its high performance 2D/3D 64-bit video engine integrated into the chipset supports CRT displays with resolution of up to 1600 x 1200, 256 colors at 85Hz or 1024 x 768, 65536 colors at 85Hz.

Signal Path

VGA interface signals are available on J8, standard VGA connector, located on the faceplate of the board.

Related Jumpers
None

The RAP-C810 supports DSTN and TFT panels through a mezzanine card (optional)

2.11.1 Supported Resolutions

The maximum video resolution and performance depend directly on the drivers running with your software application. Resolution and number of color specification are listed below:

Resolution	Number of Colors
640x480, 800x600, 1024x768, 1280x1024, 1600x1200	256 (8 bits)
640x480, 800x600, 1024x768, 1024x768, 1280x1024	65,536 (16 bits)
640x480, 800x600, 1024x768, 1280x1024	16.8 million (24 bits)

2.11.2 Major Features Description

2.11.2.1 2D/3D Graphics Engine

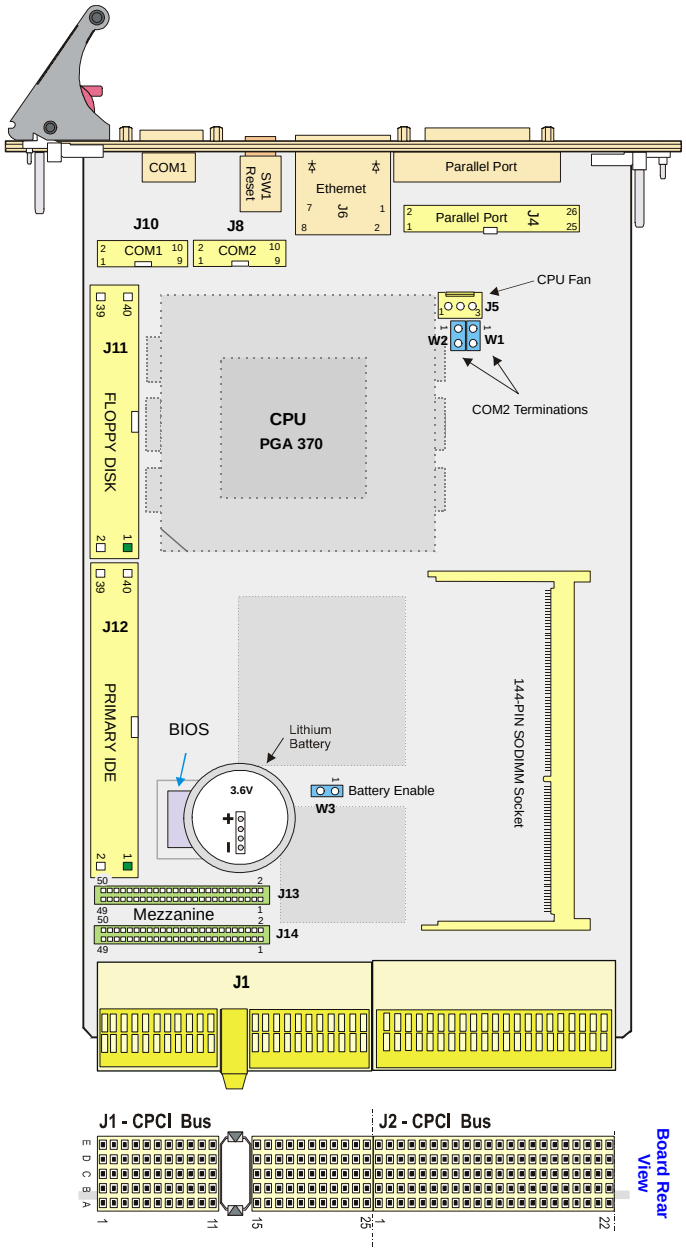
The 2D/3D graphics engine is an advanced 64-bit three-operand engine that accelerates BitBLTs as line draws, polygon draw, and polygon fill. The 2D/3D graphics engine also performs video and bitmap scaling, and data overlay.

PART 3

3 INSTALLING THE BOARD

1. SETTING JUMPERS
2. REGISTER'S DESCRIPTION
3. RAP-C810 BLOCK DIAGRAM
4. CUSTOMIZING THE BOARD

3.1 SETTING JUMPERS



Jumper settings for the RAP-C810		
Description	**Jumpers**	
RS-422/485 modes only	W1	W2
With termination resistors	on	on
Without termination resistors (default setting)	off	off
Onboard Battery	W3	
Battery connected to board	on	
Battery not connected to board (default setting)	off	

3.2 REGISTER'S DESCRIPTION

3.2.1 Serial Port 2 Configuration

FPGA	Address	D7	D6	D5	D4	D3	D2	D1	D0
READ	0x190* 0x290* 0x390*	NU	NU	NU	RS485	RS232	ST1	NU	NU
WRITE	0x190* 0x290* 0x390*	NU	NU	NU	RS485	RS232	ST1	NU	NU
Power-up Default					0	1	0		

ST1 : Enable RTS2 to be used as 485TX ENABLE when in 485 mode
RS232 : Enable UART2 RS232 operation when 1
RS485 : Enable UART2 RS422 and 485 operation when 1

The serial port 2 mode can be controlled by setting three bits. Here are the possibilities.

Mode	Bit RS232	Bit RS485	Bit ST1
RS232	1	0	X*
RS422	0	1	0
RS485	0	1	1

X = Don't care

3.2.2 History and monitor status

FPGA	Address	D7	D6	D5	D4	D3	D2	D1	D0
READ	0x191*	PBRST	NU	WDO	NU	NU	NU	NU	PFO
WRITE	0x191*	NU	NU	NU	NU	NU	NU	NU	NU
Power-up Default									

PFO : Read the external power fail flag
PBRST : When high, indicate that the last system reset was caused by push button reset switch
WDO : When high, indicate that the last system reset was caused by watchdog time out
Note : Since the history is stored in RAM memory, a loss of power will delete it.

3.2.3 History status

FPGA	Address	D7	D6	D5	D4	D3	D2	D1	D0
READ	0x192*	NU	NU	NU	NU	HWD_LCK	WD_LOCK	NU	CLRHIS
WRITE	0x192*	NU	NU	NU	NU	HWD_LCK	WD_LOCK	NU	CLRHIS
Power-up Default						1	1		1

CLRHIS : When low, clear all history bits. Set this bit to 1 to enable history logging.
WD_LOCK : When high, lock the state of the enable bit for the digital watchdog

3.2.4 Monitoring status and I/O access

FPGA	Address	D7	D6	D5	D4	D3	D2	D1	D0
READ	0x193*	NU	NU	NU	NU	IDCHIP	NU	I2C_CLK	I2C_DATA
WRITE	0x193*	NU	NU	NU	NU	IDCHIP	NU	I2C_CLK	I2C_DATA
Power-up Default						0		0	0

I2C_DATA : I2C data
I2C_CLK : I2C Clock
IDCHIP : One-wire clock/data for silicon ID chip

3.2.5 Digital watchdog

FPGA	Address	D7	D6	D5	D4	D3	D2	D1	D0
READ	0x196*	WDEN	WDD2	WDD1	WDD0	NU	NU	NU	NU
WRITE	0x196*	WDEN	WDD2	WDD1	WDD0	NU	NU	NU	NU
Power-up Default		0	0	0	1				

WDEN : Enable/disable digital watchdog.
WDD[2..0] : Duration of digital watch dog.

The digital watchdog duration can be controlled in the following way.

WDD[2..0]	NMI(T)	RESET(T)
000	16T	NMI(T)+8T
001	64T	NMI(T)+8T
010	256T	NMI(T)+8T
011	1024T	NMI(T)+8T
100	4096T	NMI(T)+8T
101	16384T	NMI(T)+8T
110	65536T	NMI(T)+8T
111	262144T	NMI(T)+8T

Time-out selection with T = 1.08ms (TBC)

3.2.6 NMI Control

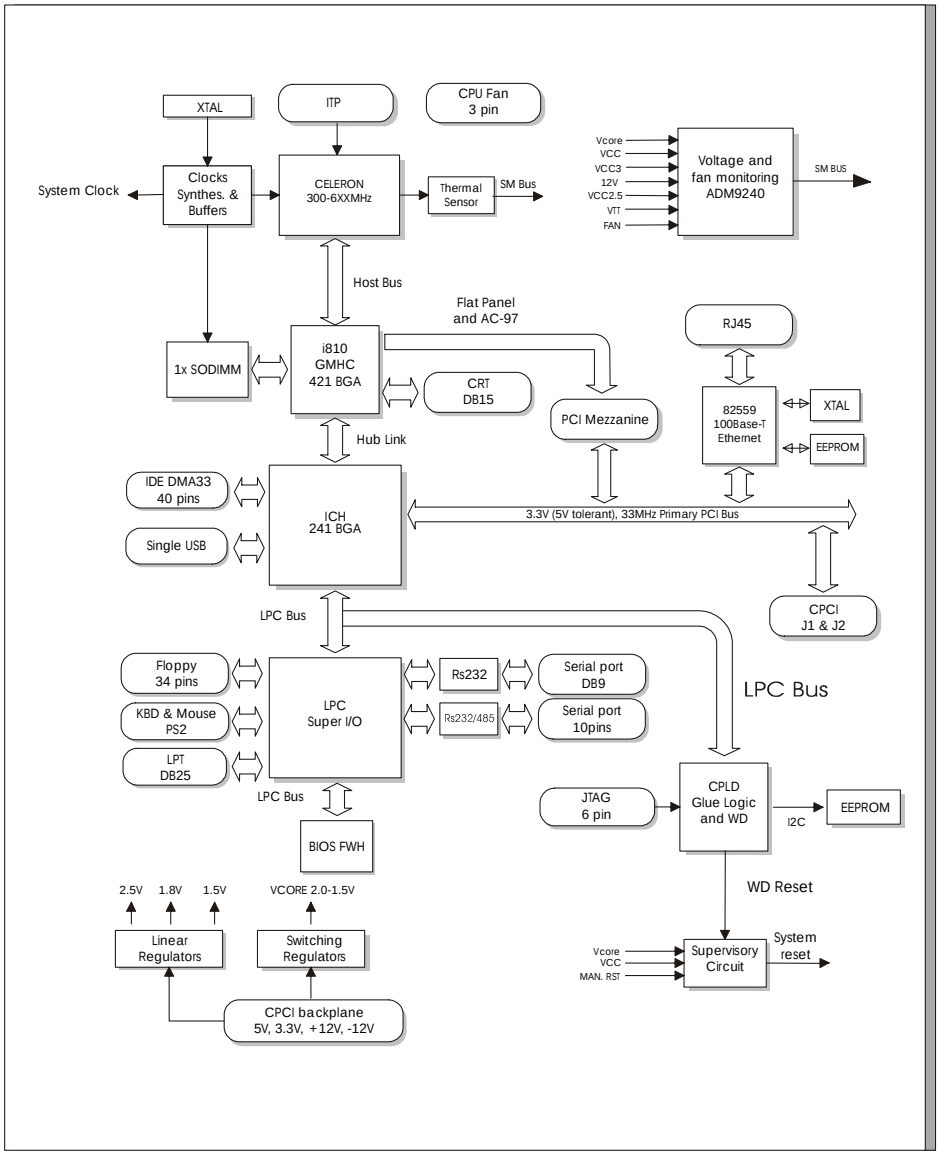
FPGA	Address	D7	D6	D5	D4	D3	D2	D1	D0
READ	0x197*	BATFEN	BATFLT	NU	NU	NU	NU	WDNMIEN	WDNMI
WRITE	0x197*	BATFEN	NU	NU	NU	NU	NU	WDNMIEN	NU
Power-up Default		0						0	

WDNMI : When high, signal NMI from watchdog time-out.
WDNMIEN : Enable NMI generation from digital watchdog
BATFLT : When high, signal NMI from local RTC battery monitor
BATFEN : Enable NMI generation for bat fault.

3.2.7 Register BITs description (summary)

FPGA	Address	D7	D6	D5	D4	D3	D2	D1	D0
READ	0x190	NU	NU	NU	RS485	RS232	ST1	NU	NU
WRITE	0x190	NU	NU	NU	RS485	RS232	ST1	NU	NU
READ	0x191	PBRST	NU	WDO	NU	NU	NU	NU	PFO
WRITE	0x191	NU	NU	NU	NU	NU	NU	NU	NU
READ	0x192	NU	NU	NU	NU	NU	WD_LOCK	NU	_CLRHIS
WRITE	0x192	NU	NU	NU	NU	NU	WD_LOCK	NU	_CLRHIS
READ	0x193	NU	NU	NU	NU	IDCHIP	NU	I2C_CLK	I2C_DATA
WRITE	0x193	NU	NU	NU	NU	IDCHIP	NU	I2C_CLK	I2C_DATA
READ	0x196	WDEN	WDD2	WDD1	WDD0	NU	NU	NU	NU
WRITE	0x196	WDEN	WDD2	WDD1	WDD0	NU	NU	NU	NU
READ	0x197	BATFEN	BATFLT	NU	NU	NU	NU	WDNMIEN	WDNMI
WRITE	0x197	BATFEN	NU	NU	NU	NU	NU	WDNMIEN	NU
0x198 - 0x19F		R E S E R V E D							

3.3 RAP-C810 BLOCK DIAGRAM

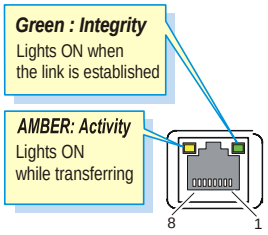


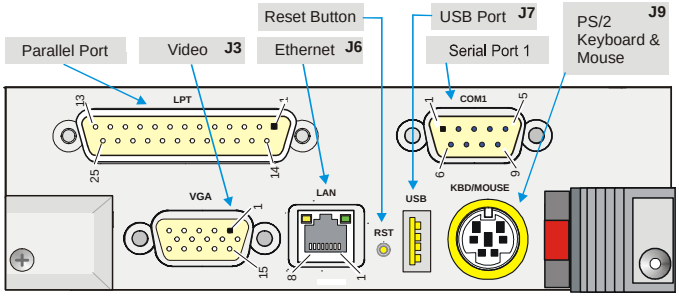
3.3.1 Onboard Connectors and Headers

Description	Comments	
CompactPCI Bus	J1/J2	J1- CPCI bus signals and power. J2 – Additional system slot signals (PCI 64 bits extension)
Fan Header	J5	The +12V DC CPU fan power supply is provided through this header as well as a speed sense input for the fan (J6 only)
VGA	J3	Supports standard 15-pin DSUB female connector.
Serial Port 1/2	J10/J8	Supports 2 x 10-pin DSUB male connector.
Ethernet	J6	RJ-45 connectors with built-in activity and link indicators.
SODIMM Socket	U2	Supports 144-pin 64/72-bit SODIMMs, up to 128MB of SDRAM.
Keyboard/Mouse	J9	Mouse and keyboard signals are combined on a standard 6-pin DSUB female connector.
Kontron's PMC	J20-J21	The PCI Mezzanine Card (PMC) connectors support the Kontron's PMC device.
Battery	B1	CMOS backup battery connector.

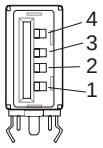
3.3.2 Front Plate Connectors and Indicators

Ethernet Connector

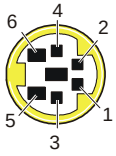




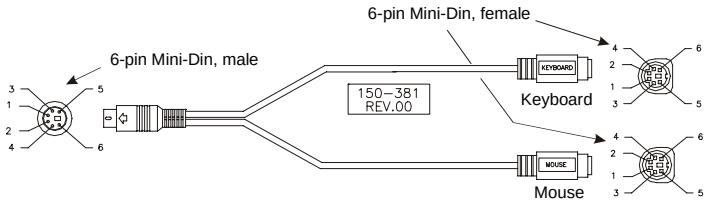
USB connector



PS/2 Keyboard & Mouse connector



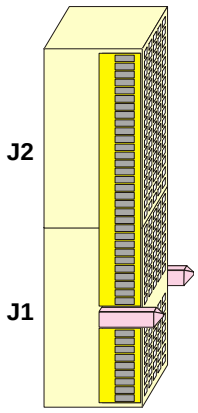
Connector	Description	Comments
J3	VGA Video	Standard 15-pin DSUB female connector
W1	Reset Button	Use a small tool to press the button and proceed to a hardware reset of the board
J10/J8	Serial Port 1/2	Standard 9-pin DSUB male connector
J6	Ethernet	RJ-45 connectors with built-in activity and link indicators
J9	Keyboard and Mouse	To connect a keyboard and/or a mouse through this connector, you need a Y shaped splitter cable (Kontron part number 150-381)



Note This cable is optional. The part number is 150-381-00.

The faceplate supports a PMC cutout with filler cap installed that acts as an EMI shield when there are no PMC device installed.

3.3.3 CompactPCI Connectors



- **CPCI J2 Connector**

  Supports additional system slot signals, PCI 64-Bit extension, and power.

- **CPCI J1 Connector**

  Supports CPCI bus signals, and power.

3.4 CUSTOMIZING THE BOARD

3.4.1 Processor

The RAP-C810 is shipped with a Celeron Processor (supported speeds range from 300/66MHz to 566/66MHz, and future speeds when available).

CAUTION

Since CPUs are very sensitive components, particular attention should be given while installing a processor on the board. Improper installation may damage the board and/or the CPU

Before installing a processor on your board, **you must contact our technical support** for the installation procedure

3.4.2 Backup Battery

An onboard 3.6V lithium battery is provided to backup BIOS setup values and the real time clock (RTC). The board is shipped with W3 (on board enable/disable battery jumper) not installed. Please install this jumper prior to run the RAP-C810.

When replacing, the battery must be connected as follows:

> **Note**
>
> The board is shipped with W3 (on board enable/disable battery jumper) not installed. Please install this jumper prior to run the RAP-C810.
>
> Running the board without installing W3 will cause a CMOS memory error.

> **WARNING**
>
> ***Danger of explosion if battery is incorrectly replaced***
>
> Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.

3.4.3 SDRAM System Memory

The RAP-C810 supports on industry standard 144-pin SODIMMs (Small Outline Dual Inline Memory Module) sockets for memory configuration from 32MB to 128MB of Synchronous DRAM.

The memory characteristics must conform to the following:

- 1.25 inch height (long) or 1 inch height (short), 144-pin SODIMM
- Standard 3V.
- 64-bit modules, single-sided or double-sided.
- Unbuffered 100MHz SDRAM.
- Serial Presence Detect (SPD) EEPROM.

The recommended SODIMM devices are listed in the table below.

Vendor's part number	DIMM's description	Vendor's Name
CTK32M/P100SO	SO-DIMM SDRAM 32MB 4M*64 PC100 SPD 144 P	CENTON
DIM-400464V5S08G	SO-DIMM SDRAM 32MB 4M*64 PC100 SPD 144 P	SHIKATRONICS
CTK64M/P100S0	SO-DIMM SDRAM 64MB 8M*64 PC100 SPD 144 P	CENTON
DIM-400864V5S08G	SO-DIMM SDRAM 64MB 8M*64 PC100 SPD 144 P	SHIKATRONICS
CTK128M/P100SO	SODIMM SDRAM 128MB 16M*64 PC100 SPD 144P	CENTON
DIM-401664VDS08G	SODIMM SDRAM 128MB 16M*64 PC100 SPD 144P	SHIKATRONICS

3.4.3.1 SODIMM Installation and Removal

> NOTE
>
> If a Mezzanine card is installed, it must be removed before installation of SODIMMs.

To install the SODIMMs in the sockets, proceed as follows:

1. With the board flat on the table, turn it so that the faceplate is facing you.
2. Hold the module vertically so that the bottom connector key is at right. Install the SODIMM into the socket. The socket's keys will ensure a correct mating.
3. Press firmly on the top edge of the memory module to engage it into the socket. The module is fully inserted when the retaining clips snap into notches located at each end of the module.

To remove the SODIMMs from the sockets, press simultaneously on the retaining clips located on each side of the socket. Once the module has snapped out, pull gently on it.

3.4.4 Supervision Features

The RAP-C810 provide a set of programmable I/O registers to setup the ICH (I/O addresses 4030h to 4037h) and the XILINX FPGA (I/O addresses programmable at 190h-197h, 290h-297h, and 390-397h using the Phoenix Chipset Features Setup).

Only register bits needed to program the power fail detection and watchdog functions are described below.

3.4.4.1 Power Fail Monitoring

The power failure detector status can be readout from one bit of the system register located at the address 0 x 191h Bit 0. The detection conforms to the following conditions (* = active low signal):

It always monitors the +5V power supply. When it drops below 4.65V (typical), the system is reset.
It can monitor the onboard battery. When the battery is in a low condition (below 2.9V typical), the PFO* (power fail output) signal goes low. An interrupt handler can then service the interrupt. If you choose not to generate an NMI, you can use an algorithm to detect a low battery condition and respond accordingly.

For more information, contact the Technical Support department

3.4.4.2 Watchdog

The function of a watchdog is to reset the CPU board if the processor is not able to generate a trigger for longer than the watchdog time-out period. This feature is useful in embedded systems where human supervision is not required or impossible.

The RAP-C810 provides a two-stage digital watchdog with software programmable time-out period.

Following a reset of any source, the watchdog is disabled. The watchdog can be enabled by software.

Dual Stage Watchdog

Enabling the Programmable Watchdog

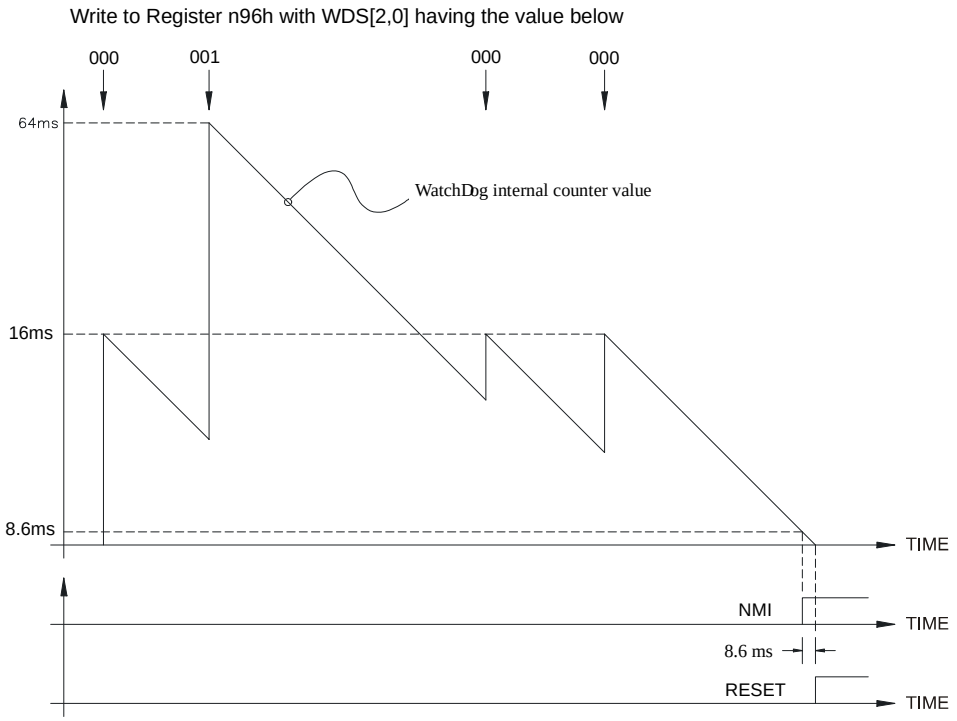
To enable the programmable watchdog, first unlock the enable bit by clearing the lock bit in register n92h (bit 2), then set the bit WDEN (bit 7) in register n96h and relock it by setting the lock bit in register n92 (bit 2). The following is an example in C language:

```
#define TekReg 0x190                    // define base address (0x190)
void ArmWatchdog(void)
{
    outp(TekReg+2,  inp(TekReg+2) & 0xFB);      // unlock watchdog enable bit
    outp(TekReg+6,  inp(TekReg+6) | 0xF0);      // enable and trigger at max time-out
    outp(TekReg+2,  inp(TekReg+2) | 0x04);      // lock watchdog enable bit
}
```

Triggering the Programmable Watchdog

To trigger the programmable watchdog, the processor writes to register n96h (n=1, 2 or 3). The action of writing to the register is the trigger and the value written to the register tells the watchdog the current time-out to use (see register n96h description). For a fixed time-out, the software simply writes a constant in register n96h.

A variable refresh is possible as shown below:



The programmable watchdog can be viewed as a decrementing counter that is initialized by a write to register n96h (n = 1, 2 or 3). The processor must initialize the counter to prevent it from reaching count 0 (timeout).

The following C language procedure can be used to trigger the programmable watchdog.

```
#define TekReg 0x190                    // define base address (0x190, 0x290 or 0x390)
void TrigWatchdog(timeout)     // select timeout at runtime: 0x80 = 0.016s,
                               // 0x90 = 0.065s, 0xA0 = 0.261s, ...
{
   outp(TekReg+6,(inp(TekReg+6) & 0x0F) | (timeout & 0xF0));
}
```

Time-out

The programmable watchdog has two stages: the first stage has a variable time-out while the second stage has a fixed one.

The first stage time-out is chosen at runtime from eight preset values (see table below). The first stage time-out generates an NMI interrupt (if enabled in register n96h, bit 7). An appropriate NMI handler must be written, otherwise this will be treated as a parity error by the default BIOS NMI handler; see register n96h description for a suggestion on how to do this.
The second stage times-out 8.6ms ±10% (depending on the temperature) after the first one and generates a master reset.

WDD[2..0]	NMI(T)	RESET(T)
000	16T	NMI(T)+8T
001	64T	NMI(T)+8T
010	256T	NMI(T)+8T
011	1024T	NMI(T)+8T
100	4096T	NMI(T)+8T
101	16384T	NMI(T)+8T
110	65536T	NMI(T)+8T
111	262144T	NMI(T)+8T

Time-out selection with T = 1ms

A reset from the programmable watchdog is latched for reset source identification; see reset history description in Section 4.3.

The RAP-C810 is equipped with a circuit that can inform the user of the cause for the last system reset. The reset can be caused by the user pushing the push-button reset or the system reset can be caused by the watch dog timer elapsing. Bit D7 in register n91h is high if the last system reset was caused by the push-button reset. Bit D5 of register n91h is high if the watchdog timer elapsing caused the last system reset. These bits can be cleared by writing a “0” to bit D0 at n92h.

3.4.4.3 Thermal Management

The thermal management is built around one digital temperature sensors and a thermal watchdog. The device can be programmed to set their outputs when the temperature of the processor exceeds a programmable high limit, and reset its output when the temperature is under a programmable low limit. A special routine is implemented to throttle the CPU clock until the temperature falls below the programmed low limit.

Thermal management will be done with two resume/overheat temperature stored in the CMOS and controlled by the BIOS setup menu. Current processors and board temperatures will also be reported in the CMOS setup menu. Local and remote sensors are available. The local sensors correspond to the board temperature and the remote sensors to the CPU die temperatures. The user can set an audible alarm on PC speaker when the board or CPU is in an alarm state.

3.4.5 Storage Devices

cMC : Mezzanine Card that is installed directly onto the processor board (see section 1.5 – Mezzanine Card Concept).

3.4.6 Installing the Board into a Bay

Due to the high-density pinout of the RAP-C810's Hard Metric connectors, some precautions must be taken when inserting or removing a board in/out of a system:

1. Properly insert the board in the rail guides and slide the board until the board connectors mate to the backplane.
2. Do not use excessive force if there is any mechanical resistance while inserting the board or serious damage can be incurred to the backplane.
3. Using the extractor handle, push the board to final insertion.
4. Using the face plate bolts, firmly secure the board to the enclosure.
5. Use the extractor handles to disconnect and extract the board from its enclosure.

3.4.7 Connector Keying

CompactPCI connector supports guide lugs to ensure a correct polarized mating. A proper mating is enhanced by the use of color-coded keys for 3.3V and 5V operation.

Color-coded keys prevent inadvertent installation of a 5V peripheral board in a 3.3V slot. The RAP-C810 is universal. It does not require keying. . Backplane connectors are always keyed according to the signaling (VIO) level. Coding Key Colors are defined as follows:

Signaling Voltage	Key Color
3.3V	Cadmium Yellow
5V	Brilliant Blue
Universal board (5V and 3.3V)	none
-48V	Red

3.4.8 Connection

To install the RAP-C810 boards into a bay, proceed as follows:

1. Locate a 3U system slot
2. Remove the blank faceplate of the slot where you intend to insert the RAP-C810.
3. Proceed as per description in 1.2.6

WARNING

1. Some mechanical parts of the guide-rail are fragile (shield contacts and clips). Do not use excessive force to insert and connect a CompactPCI board.
2. If there is any mechanical resistance while you insert a module, first ensure there is no mechanical obstacle and check for the alignment of all parts. A key might be installed preventing the installation of a CPCI board in an incompatible slot.

To remove the module from the chassis, proceed as follows:

1. Unsecure the front plate fixing bolts.
2. Unlock the bottom extractor handle.
3. Use the extractor handles to act as a lever to disengage the CompactPCI connector from the backplane.
4. Pull on the extractor handles and gently remove the board.

PART 4

4 SOFTWARE SETUPS

1. BIOS SETUP PROGRAM
2. BOOT UTILITIES
3. UPDATING OR RESTORING THE BIOS IN FLASH
4. VT100 MODE

4.1 BIOS SETUP PROGRAM

All relevant information for operating the board and connected peripherals is stored in the CMOS memory. A battery-backed up memory holds this information when the board is powered off, the BIOS Setup program is required to make changes to the setup.

NOTES

Make sure you setup the BIOS Setup software prior to installing your operating system and your drivers.

For systems that need the BIOS to first attempt to boot from LAN, follow these steps:

1. Set the "Network Boot" or "Landesk Service Agent II" as the first boot service in the BIOS setup (Boot Menu Selection, Boot First Menu".
2. Follow the complete procedure in the Boot from LAN utility CDROM.

4.1.1 Accessing the BIOS setup program

The system BIOS (Basic Input Output System) provides an interface between the operating system and the hardware of the RAP-C810 peripheral processor. The RAP-C810 uses the Phoenix Setup program, a setup utility in flash memory that is accessed by pressing the DELETE key at the appropriate time during system boot. This utility is used to set configuration data in CMOS RAM.

CAUTION

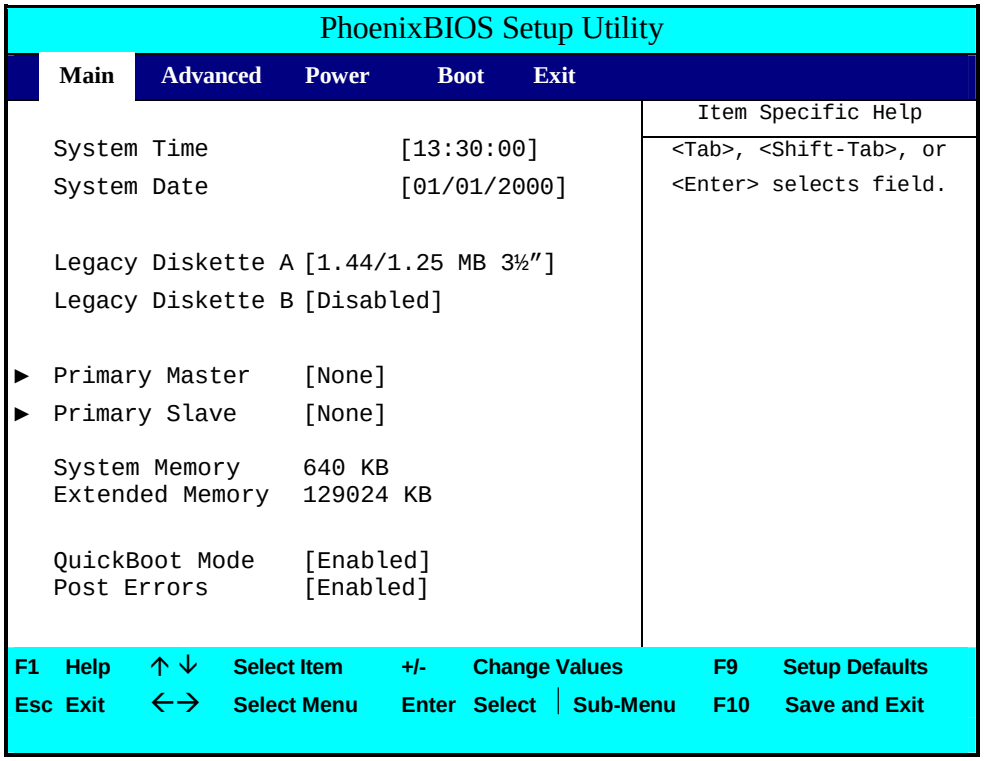
Before modifying CMOS setup parameters, ensure that the W3 battery selection jumper is installed to enable the CMOS battery back up (please refer to Section 3.1).

To run the Phoenix Setup program incorporated in the ROM BIOS:

- Turn on or reboot the system.
- When you get the following message, hit <F2> key to enter SETUP

  PhoenixBIOS 4.0 Release 6.0
  Copyright 1985-1999 Phoenix Technologies Ltd.
  All Rights Reserved
  KONTRON T3001 BIOS Version 1.0

The main menu of the Phoenix BIOS CMOS Setup Utility appears on the screen.



Whenever you are not sure about a certain setting, you may refer to the list of default values. The list of defaults is provided in the event that a value has been changed and one wishes to set this option to its original value. Loading the SETUP defaults will affect all the options in this screen (or all parameters if defaults are loaded from the Main Menu) and will reset options previously altered.

The BIOS Default values provide **optimum performance** settings for all devices and system features.

> ⚠ CAUTION
>
> These parameters have been provided to give control over the system. However, the values for these options should be changed only if the user has a full understanding of the timing relationships involved.

4.1.2 The Menu Bar

The Menu Bar at the top of the window lists these selections:

Menu selection	Description
Main	Use this menu for basic system configuration
Advanced	Use this menu to set the Advanced Features available on your system's chipset.
Power	Use this menu to configure Power Management features
Boot	Use this menu to determine the booting device.
Exit	Exits the current menu.

Use the left and right ← and → arrows keys to make a selection.

4.1.2.1 The Legend Bar

Use the keys listed in the legend bar on the bottom to make your selections or exit the current menu. The chart on the following page describes the legend keys and their alternates:

Key	Function
<F1> or <Alt-H>	General Help windows (see below)
<Esc>	Exit this menu.
← → arrow keys	Select a different menu
<Tab> or <Shift-Tab>	Cycle cursor up and down
<Home> or <End>	Move cursor to top or bottom of window.
<PgUp> or <PgDn>	Move cursor to top or bottom of window.
<F5> ir <->	Select the Previous Value for the field.
<F6> or <+> or <Space>	Select the Next Value for the field.
<F9>	Load the Default Configuration values for this menu
<F10>	Save and exit.
<Enter>	Execute Command or Select the Sub menu

To select an item, use the arrow keys to move the cursor to the field your want. Then use the plus-and-minus value keys to select a value for that field. To save values commands in the Exit Menu save the values currently displayed in all the menus.

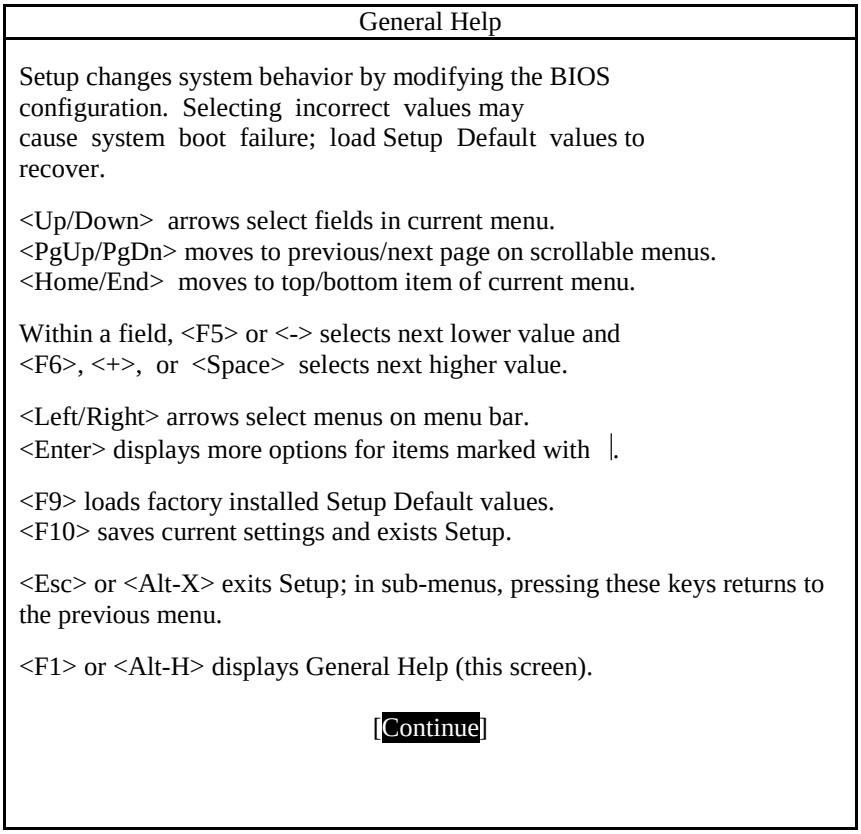
To display a sub-menu, use the arrow keys to move the cursor to the sub menu your want. Then press <Enter>. A pointer (▏) marks all sub menus.

4.1.2.2 The Field Help Window

The help window on the right side of each menu displays the help text for the currently selected field. It updates as you move the cursor to each field.

4.1.2.3 The General Help Windows

Pressing <F1> or <Alt-H> on any menu brings up the General Help window that describes the legend keys and their alternates:



The scroll bar on the right of any windows indicates that there is more than one page of information in the windows. Use <PgUp> and <PgDn> to display all the pages. Pressing <Home> and <End> displays the first and last page. Pressing <Enter> displays each page and then exits the window.

4.1.2.4 Main Menu Selection

You can make the following selections on the Main Menu itself. Use the sub menus for other selections.

Feature	Options		Description
System Time	HH:MM:SS		Set the system time.
System Date	MM/DD/YYYY		Set the system date.
Legacy Diskette A: Legacy Diskette B:	Disabled 360Kb 5.1/4” 1.2MB, 5.1/4” 720 Kb 3 1/2” 1.44/.125 MB 3 1/2” 2.88 MB 3 1/2		Select the type of floppy disk drive installed in your system. **Note :** 1.25MB 3 1/2” references a 1024 byte/sector Japanese media format. The 1.25MB, 3 1/2 diskette requires a 3-Mode floppy-disk drive.
Primary Master	Type	None	None No booting device installed.
		CD-ROM	CD-ROM CD-ROM drive installed.
		CD-ROM	**Multi-Sector Transfers** Any selection except Disabled determines the number of sectors transferred per block. Standard is 1 sector per block. **LBA Mode Control** Enabling LBA causes Logical Block Adressing to be used in place of Cylinders, heads, and Sectors. **32 Bit I/O** Enables 32-bit communication between CPU and IDE card. Requires PCI or local bus. **Transfer Mode** Selects the method for transferring the data between the hard disk and system memory. The Setup menu only lists those options supported by the drive and platform. **Ultra DMA Mode** Select the Ultra DMA mode used for moving data to/from the drive. Autotype the drive to select the optimum transfer mode.
		ATAPI Removable	Choices are same as CD-ROM

Feature	Options		Description
Primary Master (Continued)	Type (continued	IDE Removable	Choices are same as CD-ROM
		USER)	**Cylinders** Set the number of cylinders **Heads** Set the number of heads. Choices are 1 to 16 **Sectors** Set the number of sectors per track **Maximum Capacity** Maximum capacity is displayed according to the cylinders, heads and sectors selected. **Multi-Sector Transfers** Specify the number of sectors per block for multiple sector transfers. "MAX" refers to the size the disk returns when queried. **LBA Mode Control** Enabling LBA cause Logical Block Adressing to be used in place of Cylinders Heads and Sectors **32 Bit I/O** This setting enables or disables 32 bit IDE data transfers. **Transfer Mode** Select the method for moving data to/from the drive. Autotype the deive to select the optimum transfer mode. **Ultra DMA Mode** Select the Ultra DMA mode used for moving data to/from the drive Autotype the drive to select the optimum transfer mode.
		Auto	BIOS autodetects the hard disk installed
Primary Slave	Type	None CD-ROM ATAPI Removable IDE Removable User Auto	Same description as Primary Master
System Memory	n/a		Displays the amount of conventional memory detected during boot up
Extended Memory	n/a		Displays the amount of extended memory detected during boot up
QuickBoot Mode	Enabled Disabled		Allows the system to skip certain tests while booting. This will decrease the time needed to boot the system.
POST Errors	Enabled Disabled		Pauses and displays SETUP entry or resume boot prompt if error occurs on boot. If disabled, system always attempts to boot.

4.1.2.5 Advanced Menu Selection

You can make the following selections on the Advanced Menu. Use the sub menus for other selections.

Feature	Options	Description
Installed O/S	Other Win95 Win98/Win2000	Other : Non PnP or ACPI OS. Win95 : PnP OS. Win98/Win2000 : ACPI OS. Select the operating system installed on your system which you will use most commonly. **Note :** An incorrect setting can cause some operating systems to display unexpected behavior.
Reset Configuration Data	No Yes	Select "Yes" if you want to clear the Extended System Configuration Data (ESCD) area.
Cache Memory	Memory Cache [Enabled / Disabled]	Sets the state of the memory cache..
	Cache System BIOS area	Controls caching of system B0S area.. Choices are: uncached, Write Protect
	Cache Video BIOS area	Controls caching of video BIOS area. Choices are: uncached, Write Protect
	Cache Base 0-512K	Controls caching of 512k base memory Choices are : uncached, Write Through, Write Protect, and Write Back
	Cache Base 512K-640K	Controls caching of 512k-640k base memory Choices are : uncached, Write Through, Write Protect, and Write Back..
	Cache Extended Memory Area	Controls caching of system memory Choices are: uncached, Write Through, Write Protect, and Write Back.
	Cache A000-AFFF	Set the type of caching. Following choices are available : **Disabled** : This block is not cached. **USWC Caching** :Uncached Speculative Write Combined. **Write Through:** Writes are cached and sent to main memory at once. **Write Protect:** Writes are ignored. **Write Back:** Writes are cached, but not sent to main memory until necessary. Set the type of caching. Following choices are available :Disabled, Write Through, Write Protect, and Write Back
	Cache B000-BFFF	Same as above
	Cache C800-CBFF	Set the type of caching. Following choices are available :Disabled, Write Through, Write Protect, and Write Back

Advanced Menu Selection (continued)

Feature	Options	Description
Cache Memory	Cache CC00-CFFF	Same as above
	Cache D000-D3FF	Same as above
	Cache D400-D7FF	Same as above
	Cache D800-DBFF	Same as above
	Cache DC00-DFFF	Same as above
	Cache E000-E3FF	Same as above
	Cache E400- E7FF	Same as above
	Cache E800-EBFF	Same as above
	Cache EC00- EFFF	Same as above
I/O Device Configuration	Serial Port A	Configure serial port A using options: **Disabled :** No configuration **Enabled :** User configuration When Enabled, set the base I/O address for serial port A. Choices are : **3F8, 2F8, 3E8, 2E8** Choices for IRQs are: **IRQ 3** and **IRQ 4** **Auto :** BIOS or OS chooses configuration **OS Controlled :** Displayed when controlled by OS.
	Serial Port B	Same as above
	Mode	Set the mode of rserial port B. Choices are : RS-232, RS-422, and RS-485.
	Parallel port	Configure parallel port using options : **Disabled :** No configuration **Enabled :** User configuration When enabled, set the Base I/O address. Choices are: **378, 278** and **3BC.** Choices for IRQs are: **IRQ5** and **IRQ7.** **Auto:** BIOS or OS chooses configuration **OS Controlled:** Displayed when controlled by OS
	Mode	**Mode** Set the mode for the parallel port using options: **Output only, Bi-directional EPP** and **ECP**

Advanced Menu Selection (continued)

Feature	Options	Description
I/O Device Configuration (continued)	Floppy disk controller	Configure the floppy disk controller by using these options : **Disabled :** No configuration **Enabled:** User configuration **Auto:** BIOS or OS chooses configuration **OS Controlled :** Displayed when controlled by OS**.**
	Base I/O address	Set the base I/O address for the floppy disk controller using options : **Primary** or **Secondary**
Large Disk Access Mode	Other DOS	If you are using UNIX, Novell Netware or other operating systems, select "**Other**". If you are installing new software and the drive fails, change this selection and try again. Different operating systems require different representations of drive geometries.
LBA Translation Type	LBA PTL	LBA assisted translation (Award backward compatible) PTL, Phoenix bit-shifting translation.
Local Bus IDE Adapter	Enabled Disabled	Enable the integrated local bus IDE adapter

Advanced Menu Selection (continued)

Feature	Options	Description
Advanced Chipset Control	Video boot type	Select "Onboard Video" to enable the onboard video controller as the boot display device. Select either 512K or 1MB of System Memory to be allocated to the onboard video controller. Select "Disable Onboard Video" to disable the onboard video controller. No System Memory will be allocated for video.
	Enable memory gap	If enabled, turn system RAM off to free address space for use with an option card. Either a 128KB conventional memory gap, starting at 512KB, or a 1MB extended memory gap, starting at 15MB, will be created in system RAM.
	Enable CD hole	If enabled, turn system RAM off to free address space for use with an option card. A 16KB CD hole, starting at 880KB (DC000h) will be created in system memory space.
	Enable D8 hole	If enabled, turn system RAM off to free address space for use with an option card. A 16KB Memory hole, starting at 864KB (D8000h) will be created in system memory space.
	Frequency Ratio	Select the internal frequency multiplier of the CPU. Choices are 2x, 4x, 3x, 5x, 2.5x, 4.5x, 3.5x, 5.5x, 6x, 8x, 7x, 6.5x, 1.5x, 7.5x, and 2x.
	Legacy USB Support	Enables/Disables support for Legacy Universal Serial Bus.
	Onboard Ethernet Controller	Enables/Disables onboard Ethernet Controller.
	Save CMOS in FLASH	Enable/Disable Save CMOS in FLASH.
	CPU Clock Spread Spectrum	Enables/Disables Spread Spectrum.

4.1.2.6 Power Menu Selection

Feature	Options	Description
Power Savings	Disabled	To turn off power management, choose Disabled.
	Customized	To alter these settings, choose Customized
	Maximum Power Savings	Maximum Power Savings conserves the greatest amount of system power .
	Maximum Performance	Maximum Performance conserves power but allows greatest system performance
Standby Timeout	Off 2 Minutes 4 Minutes 6 Minutes 8 Minutes7 12 Minutes 16 Minutes	Amount of time the system needs to be in Idle Mode before entering the Standby Mode. Standby Mode turns off various devices in the system, including the screen, until you start using the computer again .
Auto Suspend Timeout	Off 5 Minutes 10 Minutes 15 Minutes 20 Minutes 30 Minutes 40 Minutes 60 Minutes	Amount of time the system needs to be in Standby before entering the SUSPEND Mode.
Resume On Time	Off On	Enabled wakes the system up at a specifit time
Resume Time	[00:00:00]	Specify the time when the system is to wake up. <Tab>, <Shift-Tab>, or <Enter> selects field
Resume on Modem Ring	Off On	Enabled wakes the system up when an incoming call is detected on your modem.

4.1.2.7 Boot Menu Selection

Feature	Options	Description
	Removable Devices Legacy Floppy Drives Hard Drive Bootable Add-in Cards * ATAPI CD-ROM Drive Network Boot LANDesk ® Service Agent II	Keys used to view or configure devices: **<Enter>** expands or collapses devices with a **+** or **–** **<Ctrl+Enter>** expands all **<Shift + 1>** enables or disables a device **<+>** or **<->** moves the device up or down **<n>** May move removable device between Hard Disk or Removable Disk **<d>** Remove a device that is not installed. * Note : The hard drives and SCSI drives detected will be listed in this section and the first drive in the list will be the boot drive.

4.1.2.8 Exit Menu Selection

Feature	Options	Description
	Exit Saving Changes	Exit System Setup and save your changes to CMOS.
	Exit Discarding Changes	Exit utility without saving Setup data to CMOS.
	Load Setup Defaults	Load default values for all SETUP items.
	Discard Changes	Load previous values from CMOS for all SETUP items.
	Saves Changes	Save Setup Data to CMOS.

4.2 BOOT UTILITIES

Phoenix Boot Utilities are : Phoenix QuietBoot™
Phoenix MultiBoot™

Phoenix QuietBoot displays a graphic illustration rather than the traditional POST messages while keeping you informed of diagnostic problems.

Phoenix MultiBoot is a boot screen that displays a selection of boot devices from which you can boot your operating system.

4.2.1 Phoenix QuiteBoot

Right after you turn on or reset the computer, Phoenix QuietBoot displays the QuietBoot Screen, a graphic illustration created by the computer manufacturer instead of the text-based POST screen, which displays a number of PC diagnostic messages.

To exit the QuietBoot screen and run Setup, display the Multiboot menu, or simply display the PC diagnostic messages, you can simply press one of the hot keys described below.

The QuietBoot Screen stays up until just before the operating system loads unless:

1. You press <ESC> to display the POST screen.
2. You press <F2> to enter Setup.
3. POST issues an error message.
4. The BIOS or an option ROM requests keyboard input.

»The following explains each of these situations.

4.2.1.1 Press <ESC>

Pressing <ESC> switches the POST screen and takes one of two actions:

1. If Multiboot is installed, the boot process continues with the text-based POST screen until the end of POST, and then displays the BootFirst Menu, with these options:
   a. Load the operating system from a boot device of your choice.
   b. Enter Setup.
   c. Exit the Boot First Menu (with <ESC>) and load the operating system from the boot devices in the order specified in Setup.
2. If Multiboot is not installed, the boot process continues as usual.

4.2.1.2 Press <F2>

Pressing <F2> at any time during POST switches to the POST screen (if not already displayed) and enter Setup.

4.2.1.3 POST Error

Whenever POST detects a non-fatal error, QuietBoot switches to the POST screen and displays the errors. It then displays this message:

Press <F1> to resume, <F2> to Setup

Press <F1> to continue with the boot. Press <F2> if you want to correct the error in Setup.

Keyboard Input Request

If the BIOS or an Option ROM (add-on card) requests keyboard input, QuietBoot switches over to the POST screen and the Option ROM displays prompts for entering the information. POST continues from there with the regular POST screen.

4.2.1.4 Phoenix Multiboot

Phoenix Multiboot expands your boot options by letting you choose your boot device, which could be a hard disk, floppy disk, or CDROM. You can select your boot device in Setup, or you can choose a different device each time you boot during POST by selecting your boot device in **The Boot First Menu**.
Multiboot consist of :

The Setup Boot Menu
The Boot First Menu

4.3 UPDATING OR RESTORING THE BIOS IN FLASH

Symptoms:

- No POST code on a power up (when using a POST card).
- Board does not boot, even after usual hardware and connection verifications.
- At power up, there is floppy disk led activity, which is one sign that the BIOS as detected a corrupted BIOS CRC prior POST and falled back automatically to Emergency Recovery Mode looking for the floppy Emergency disk.

Please go on our FTP site in order to get the latest Emergency Recovery BIOS for that specific product.

BIOS maybe found at: Ftp://Ftp.Kontron.ca/Support/BIOS_Emergency/

Emergency Recovery Procedure is included within the Zip file of the Emergency BIOS to download. Latest Emergency Recovery procedure can be found on the FAQ section of the FTP site under FAQ # KC_0028 at location:

ftp://ftp.kontron.ca/Support/Support_FAQ - Questions & Answers/

4.4 VT100 MODE

The VT100 operating mode allows remote setups of the board. This configuration requires a remote terminal that must be connected to the board through a serial communication link.

4.4.1 Requirements

The terminal should emulate a VT100 or ANSI terminal. Terminal emulation programs such as Telix© or Procom© can also be used.

4.4.2 Setup & Configuration

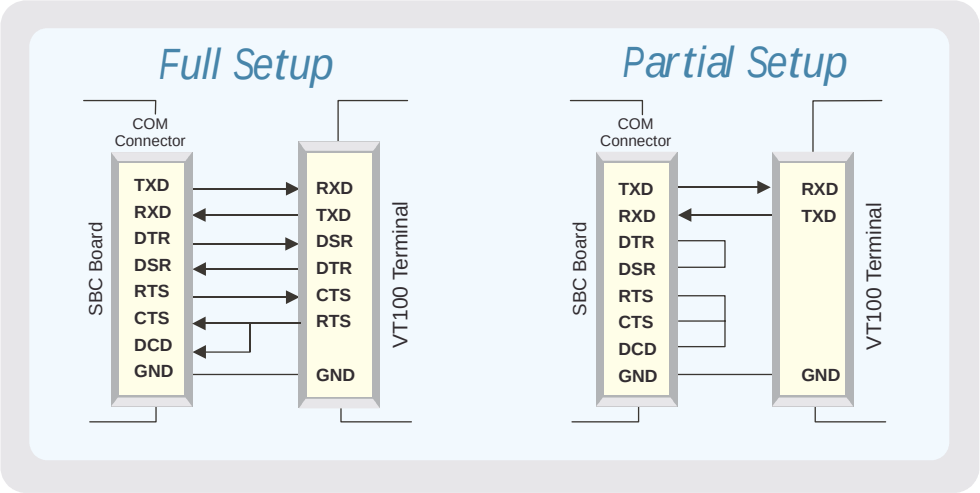
Follow these steps to set up the VT100 mode:

1. Connect a monitor and a keyboard to your board and turn on the power.
2. Enter into the CMOS Setup program in the “BIOS Feature Setup”

3. Select the VT100 mode and the appropriate COM port and save your setup.
4. Connect the communications cable as shown in the next page.

> **NOTE**
>
> If you do not require a full cable for your terminal, you can set up a partial cable by using only the TXD and RXD lines. To ignore control lines simply loop them back as shown in VT100 Partial Setup cable diagram.

5. Configure your terminal to communicate using the same parameters as in CMOS Setup.
6. Reboot the board.
7. Use the remote keyboard and display to setup the BIOS.
8. Save the setup, exit, and disconnect the remote computer from the board to operate in stand-alone configuration.



Running Without a Terminal

The board can boot up without a screen or terminal attached. If the speed is set to Auto and no terminal is connected, the speed is set to 115,200 bauds.

Furthermore, you can run without any console at all by simply not enabling VT100 Mode and by disabling the onboard video.

PART 5

APPENDICES

A. MEMORY & I/O MAPS

B. INTERRUPT LINES

C. BOARD DIAGRAMS

D. CONNECTOR PINOUTS

E. BIOS SETUP ERROR CODES

F. EMERGENCY PROCEDURE

G. GETTING HELP & RMA

A. MEMORY & I/O MAPS

A.1 MEMORY MAPPING

Address	Function
00000-9FFFF	0-640 KB DRAM
A0000-BFFFF	Video DRAM
C0000-CBFFF	Video BIOS
CC000-DFFFF	Optional ROM (Free)
	LAN BIOS around 30KB if activated, address may vary
	SCSI BIOS 18KB at runtime, 2KB if no device, address may vary
E0000-FFFFF	System BIOS
100000-Top of DRAM	1 MB - Top of DRAM

A.2 I/O MAPPING

Address	Optional Address	Optional Address	Optional Address	Function
000-01F				DMA Controller 1
020-03F				Interrupt Controller 1
040-05F				Timer
060-06F				Keyboard
070-07F				Real-time clock
080-09F				DMA Page Register
0A0-0BF				Interrupt Controller 2
0C0-0DF				DMA Controller 2
0F0-0F1, 0F8-0FF				Math Coprocessor
x90-x9F				Kontron Control Port
1F0-1F7, 3F6				Primary IDE
3F0-3F7	370-377			Floppy Disk
378-37A	3BC-3BE	2787-27A		Parallel Port (LPT1 by default)
3F8-3FF (COM1)	2F8-2FF (COM2)	3E8-3EF (COM3)	2E8-2EF (COM4)	Serial Port 1 (COM1 by default)
2F8-2FF (COM2)	3F8-3FF (COM1)	3E8-3EF (COM3)	2E8-2EF (COM4)	Serial Port 2 (COM2 by default)
3C0-3CF, 3D0-3DF, 3B0-3BB				Graphics Controller (I2C Port)

B. INTERRUPT LINES

B.1 IRQ LINES

The board is fully PC compatible with interrupt steering for PCI plug and play compatibility.

Controller # 1		Controller # 2	
IRQ 0	Timer Output 0	IRQ 8	Real-Time Clock
IRQ 1	Keyboard	IRQ 9	Available [1]
IRQ 2	Cascade Controller # 2	IRQ 10	Available [1]
IRQ 3*	Serial Port 2	IRQ 11	Available [1]
IRQ 4*	Serial Port 1	IRQ 12	PS/2 Mouse
IRQ 5*	Available [1]	IRQ 13	Coprocessor Error
IRQ 6*	Floppy Controller	IRQ 14	Primary IDE or available [1]
IRQ 7*	Parallel Port 1 or Available [1]	IRQ 15	N/C

* :All functions marked with an asterisk (*) can be disabled or reconfigured.

1 Available lines service on board and external PCI/ISA PnP devices or a Legacy ISA device.

B.2 DMA CHANNELS

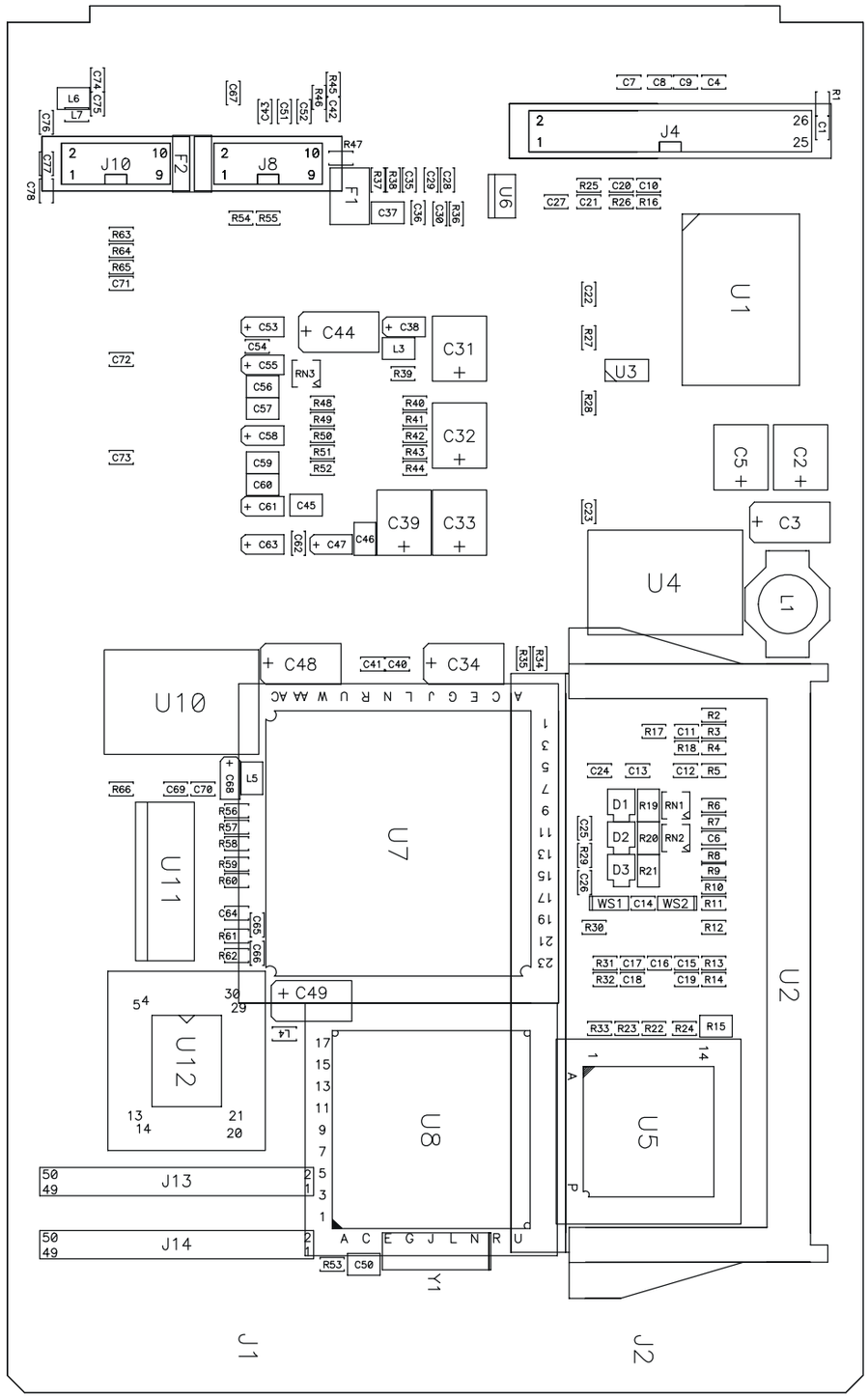
The RAP-C810 integrates the functionality of two 8237 DMA controllers. Eight DMA channels are available.

According to Plug and Play standards, the system BIOS automatically allocates DMA Channel 1 or 3 for the parallel port's ECP mode. Channel 2 is reserved for the floppy controller and Channel 4 is used to cascade Channels 0 through 7 to the microprocessor.

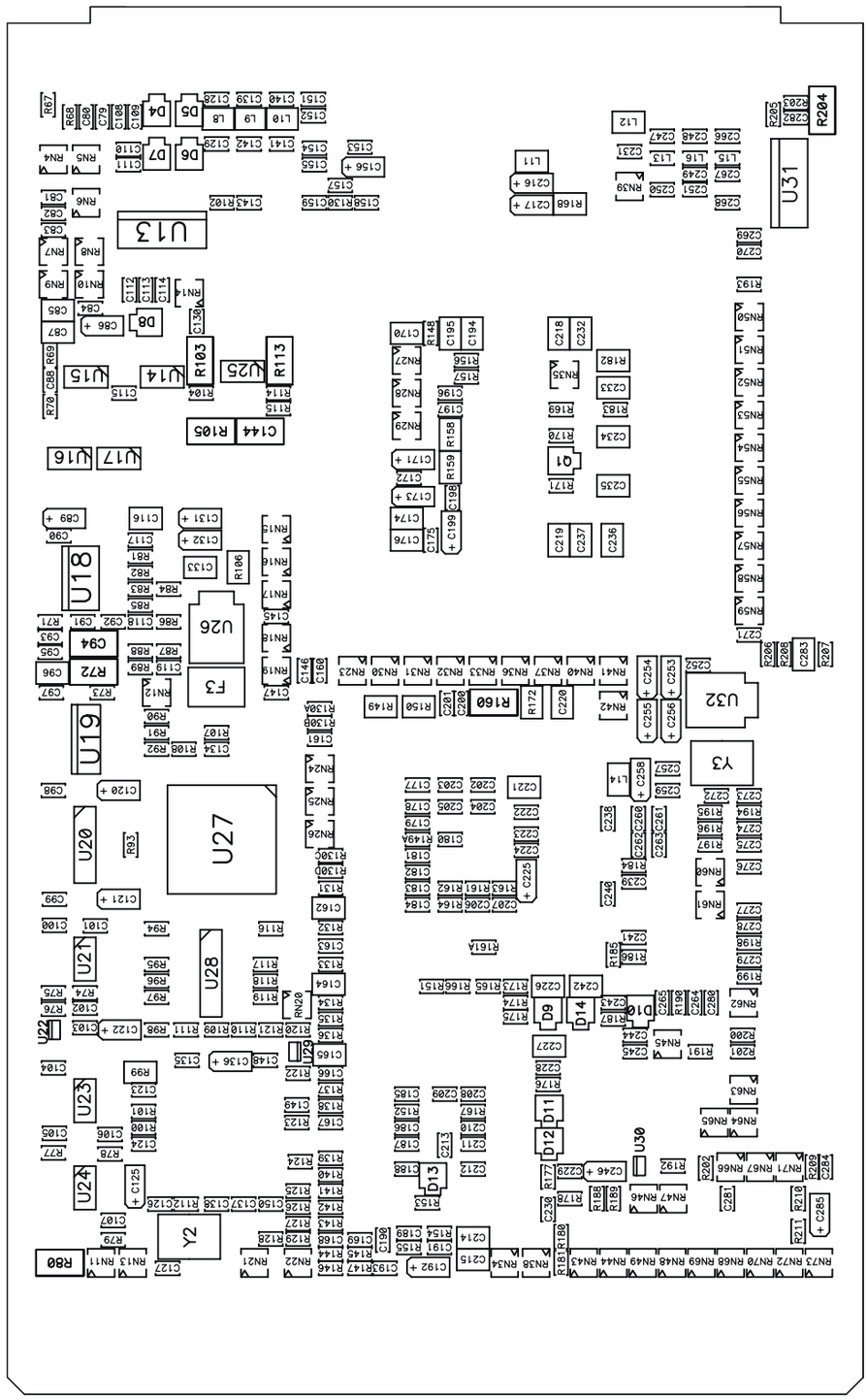
DMA Channel	Function
DMA 0	Available
DMA 1	PnP available (ECP)
DMA 2	Floppy controller
DMA 3	PnP available (ECP)
DMA 4	Cascade controller # 1
DMA 5	PnP available
DMA 6	PnP available
DMA 7	PnP available

C. BOARD DIAGRAMS

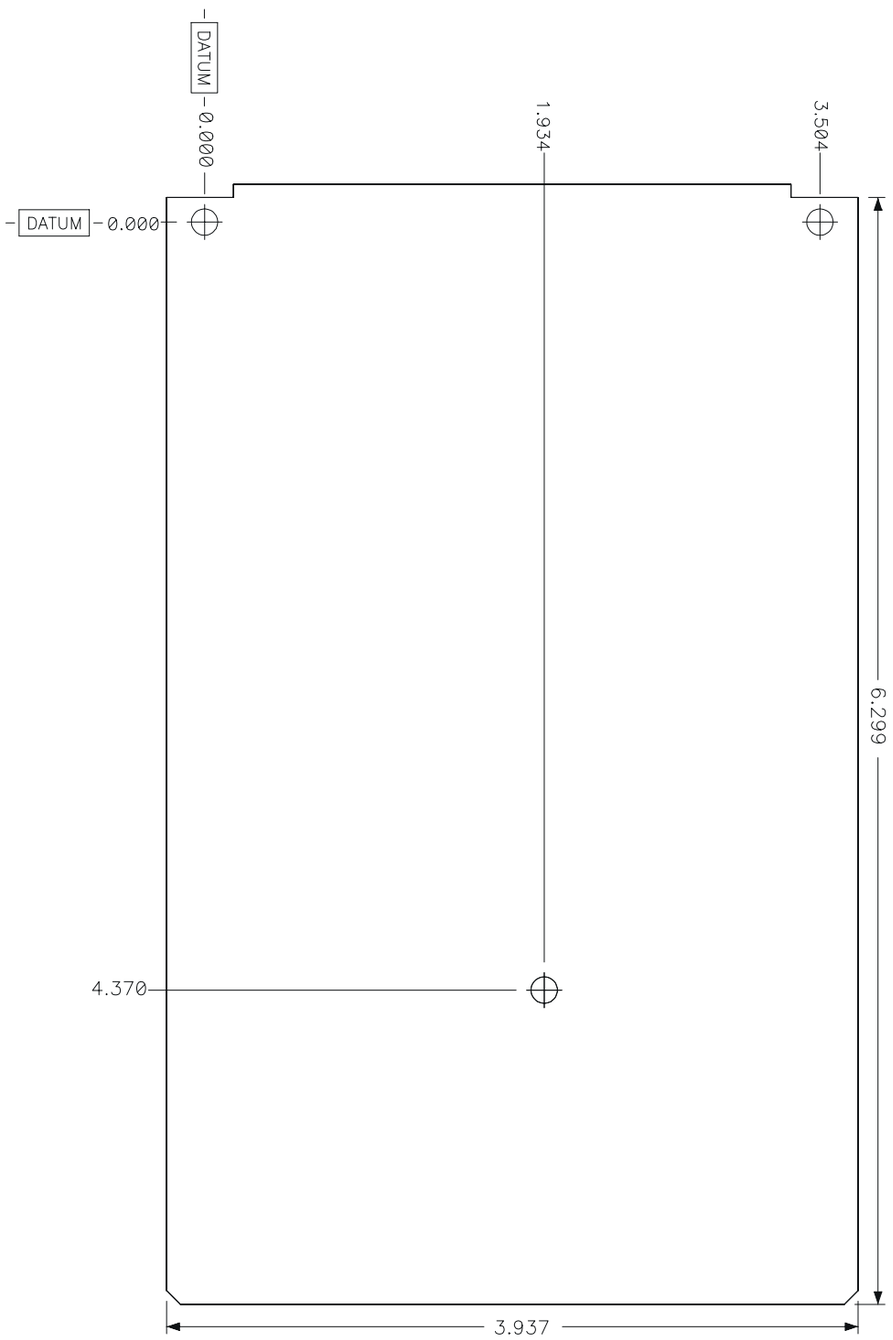
C.1 ASSEMBLY TOP DIAGRAM



C.2 ASSEMBLY BOTTOM DIAGRAM



C.3 MOUNTING HOLES



D. CONNECTOR PINOUTS

D.1 RAP-C810 CONNECTORS AND HEADERS

Connector	Description
J1	CPCI Bus
J2	CPCI Bus r
J3	VGA (Front panel only)
J4	Parallel Port
J5	CPU fan
J6	Ethernet (Front panel configuration only)
J7	USB Port (faceplate)
J8	Serial Port 2 – RS-232
J9	Keyboard/Mouse
J10	Serial Port 1 – RS-232 (Front panel configuration only)
J11	Floppy Disk
J12	Primary IDE
J13/J14	PCI Mezzanine

D.1.1 J1 cPCI Bus Connectors

Pin	ROW A	ROW B	ROW C	ROW D	ROW E
25	VCC	REQ64	ENUM#	VCC3	VCC
24	AD1	VCC	V I/O (1)	ADO	ACK64#
23	VCC3	AD4	AD3	VCC (1)	AD2
22	AD7	GND	VCC3 (1)	AD6	AD5
21	VCC3	AD9	AD8	M66EN	C/BE0#
20	AD12	GND	V I/O	AD11	AD10
19	VCC3	AD15	AD14	GND (1)	AD13
18	SERR#	GND	VCC3	PAR	C/BE1#
17	VCC3	SDONE	SBO#	GND (1))	PERR#
16	DEVSEL#	GND	V I/O	STOP#	LOCK#
15	VCC3	FRAME#	IRDY#	BDSEL# (2)	TRDY#
14	K E Y A R E A				
13					
12					
11	AD18	AD17	AD16	GND (1)	C/BE2#
10	AD21	GND	VCC3	AD20	AD19
9	C/BE3#	IDSEL (2)	AD23	GND (1)	AD22
8	AD26	GND	V I/O	AD25	AD24
7	AD30	AD29	AD28	GND (1)	AD27
6	REQ#	GND	VCC3 (1)	CLK	AD31
5	BRSVP1A5	BRSVP2B5	RST#	GND (1)	GNT#
4	BRSVP1A4	HEALTHY#	V I/O (2)	INTP	INTS
3	INTA	INTB#	INTC#	VCC (1)	INTD#
2	TCK	VCC	TMS	TD0	TD1
1	VCC	-12	TRST#	+12V	VCC

Active low
(1) Short pins (front only)
(2) Long Pins (front only)

D.1.2 J2 cPCI Bus Connectors

Pin	ROW A	ROW B	ROW C	ROW D	ROW E
22	GA4	GA3	GA2	GA1	GA0
21	RSV	RSV	RSV	RSV	RSV
20	RSV	RSV	RSV	GND	RSV
19	RSV	RSV	RSV	RSV	RSV
18	BRSVP2A18	BRSVP2B18	BRSVP2C18	GND	BRSVP2E18
17	BRSVP2A17	GND	RSV	RSV	RSV
16	BRSVP2A16	BRSVP2B16	RSV	GND	BRSVP2E16
15	BRSVP2A15	GND	RSV	RSV	RSV
14	AD35	AD34	AD33	GND	AD32
13	AD38	GND	V I/O	AD37	AD36
12	AD42	AD41	AD40	GND	AD39
11	AD45	GND	V I/O	AD44	AD43
10	AD49	AD48	AD47	GND	AD46
9	AD52	GND	V I/O	AD51	AD50
8	AD56	AD55	AD54	GND	AD53
7	AD59	GND	V I/O	AD58	AD57
6	AD63	AD62	AD61	GND	AD60
5	C/BE5#	GND	V I/O	C/BE4#	PAR64
4	V I/O	BRSVP2B4	CBE7#	GND	C/BE6
3	RSV	GND	RSV	RSV	RSV
2	RSV	RSV	N/C	RSV	RSV
1	RSV	GND	RSV	RSV	RSV

Active low

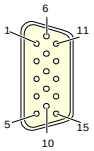
D.1.3 J3 - VGA Connector

Signal	Pin
RED	1
GREEN	2
BLUE	3
Not Connected	4
GND	5

Signal	Pin
Analog GND	6
Analog GND	7
Analog GND	8
Not Connected	9
GND	10

Signal	Pin
Not Connected	11
SDATA	12
HSYNC	13
VSYNC	14
SCLK	15

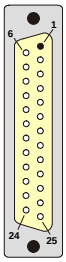
Top View



D.1.4 J4 Parallel Port Connector

Signal	Pin
STROBE#	1
(PD0-PD7)	3-17
ACK#	19
BUSY	21
PE	23
SELECT	25

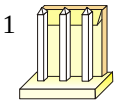
Signal	Pin
AUTOFD#	2
ERROR#	4
INIT#	6
SELECTIN#	8
GND	10-18
GND	20-26



D.1.5 J5 – CPU Fan AND tachometer

Pin #	Signal
1	Sense
2	+12V DC
3	GND

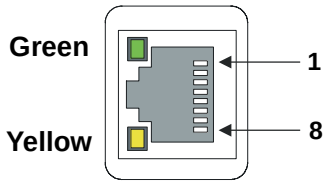
Front View



D.1.6 J6 – Ethernet

Signal	
TX+	1
TX-	2
RX+	3
*RJ1	4
*RJ1	5
RX-	6
*RJ2	7
*RJ2	8

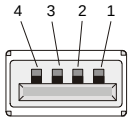
Top View



* Line terminated with 75 ohm resistors.

D.1.7 J7 - USB (FacePlate)

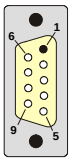
Signal	Pin
VCC USB	1
USB-	2
USB+	3
GND-USB	4



D.1.8 J8 & J10 – Serial Port 2 & 1 - RS-232

Pin Number	Signal Flow	Signal
DSR	In	6
RTS	Out	7
CTS	In	8
RI	In	9

Top View

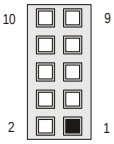


Pin Number	Signal Flow	Signal
1	In	DCD
2	In	RXD#
3	Out	TXD#
4	Out	DTR
5	-	GND

D.1.9 J8 & J10 – Serial Port 2 & 1 - RS-232 (Onboard header)

Pin Number	Signal Flow	Signal
N/C	-	10
RI	In	8
CTS	In	6
RTS	Out	4
DSR	In	2

Top View

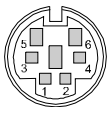


Pin Number	Signal Flow	Signal
9	-	GND
7	Out	DTR
5	Out	TXD#
3	In	RXD#
1	In	DCD

D.1.10 J9 – Keyboard and Mouse PS/2 Connector

Signal	
KDATA	1
MDATA	2
GND	3
5V Fused	4
KBCLK	5
MCLK	6

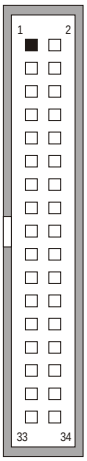
Front View



D.1.11 J11 – Floppy Disk

Pin Number	
Signal	
GND	1
GND	3
GND	5
GND	7
GND	9
GND	11
GND	13
GND	15
N.C.	17
GND	19
GND	21
GND	23
GND	25
N.C.	27
Floppy Detect	29
GND	31
N.C.	33

Top View



Pin Number	
	Signal
2	Drive Density Select 0 #
4	N.C.
6	N.C.
8	Index #
10	Motor On 0#
12	Drive Select 1#
14	Drive Select 0#
16	Motor On 1#
18	Direction Control #
20	Step #
22	Write Data #
24	Write Enable #
26	Track 0#
28	Write Protect #
30	Read Data #
32	Head Select #
34	DSKCHG#

Active Low

D.2 J13 – PRIMARY IDE CONNECTOR

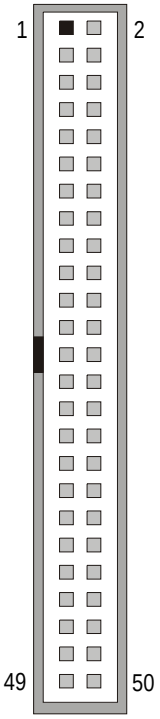
Pin Number		Top View		Pin Number	
Signal					**Signal**
Reset#	1			2	GND
D7	3	1	2	4	D8
D6	5			6	D9
D5	7			8	D10
D4	9			10	D11
D3	11			12	D12
D2	13			14	D13
D1	15			16	D14
D0	17			18	D15
GND	19			20	N.C.
DMARQ	21			22	GND
DIOW#	23			24	GND
DIOR#	25			26	GND
IORDY	27			28	CSEL
DMACK#	29			30	GND
IRQ	31			32	IOCS#16
DA1	33			34	PDIAG#
DA0	35			36	DA2
CS#0	37			38	CS#1
N.C.	39	39	40	40	GND

Active Low Signal

D.2.1 J13 - Mezzanine Connector

Pin Number	Signal
1	PCIRST#
3	FTD10
5	3VFTSDA
7	FTD6
9	FTD8
11	FTHSYNC
13	GND
15	FTD5
17	SERR#
19	FTVSYNC
21	FTBLINK#
23	FTD3
25	FTD0
27	PIRQ#A
29	PIRQ#C
31	GND
33	DEVSEL#
35	PLOCK#
37	AD30
39	AD27
41	GND
43	PLCK_MEZ
45	GND
47	REQ_MEZ
49	GND_MEZ

Top View

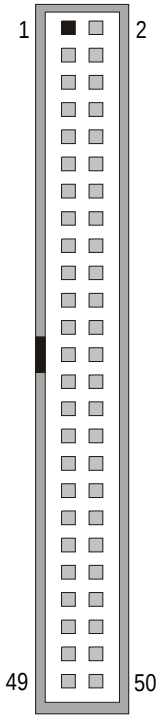


Pin Number	Signal
2	FTD9
4	+12v
6	FTD11
8	3VFTSCL
10	FTD7
12	SL_STALL
14	GND
16	FTCLK1
18	GND
20	FTCLK0
22	GND
24	FTD2
26	FTD4
28	FTD1
30	PIRQ#D
32	VCC 1.8V
34	PIRQ#B
36	AD29
38	PAR
40	AD25
42	AD21
44	GND
46	GPIOMEZ1
48	GND
50	GPIOMEZ2

D.2.2 J14 - Mezzanine Connector

Pin Number	Signal
1	AC_RST#
3	AC_SYNC
5	AC_SDIN1
7	AD0
9	AD1
11	AD3
13	AD5
15	AD13
17	AD8
19	IRDY#
21	AD11
23	AD7
25	VCC3
27	FRAME#
29	AD9
31	AD17
33	AD14
35	GND
37	AD20
39	STOP#
41	AD23
43	C_BE3#
45	VCC3
47	AD28
49	AD24

Top View



Pin Number	Signal
2	AC_SDIN0
4	AC_SDOUT
6	GND
8	AC_BITCLK
10	GND
12	AD2
14	AD4
16	GND
18	AD12
20	AD6
22	C_BE1#
24	C_BE0#
26	GND
28	C_BE#2
30	AD15
32	AD16
34	TRDY#
36	GND
38	AD10
40	AD18
42	AD22
44	AD19
46	VCC
48	AD26
50	AD31

Active low

E. BIOS SETUP ERROR CODES

E.1 POST BEEP

POST beep codes are defined in the BIOS to provide low level tone indication when an error occurs during the BIOS initialization.

Beep codes consist of a combination of long and short beeps. They are described as follows:

Beep Codes

Post code	Beep Code	Description
41	**-*	Enterring the boot block recovery code (i.e. Main BIOS checksum error)
22	*-*-*	Error when getting the boot block flash ID code
33	*-*-*-*	Error when erasing the boot block flash
44	*-*-*-*-*	Error when programming the boot block flash
55	*-*	Success of the boot block recovery code. The board is ready to be manually reset.

Legend * = 1 Short beep code, ** = 1 Long beep code, - = Silence

E.2 POST MESSAGES

During the Power On Self Test (POST), if the BIOS detects an error requiring you to do something to fix, it will either sound a beep code or display a message.

If a message is displayed, it will be accompanied by:

"PRESS F1 TO CONTINUE, DEL TO ENTER SETUP".

E.3 ERROR MESSAGES

One or more of the following messages may be displayed if the BIOS detects an error during the POST.

CMOS BATTERY HAS FAILED

1. If it's the first boot, check for the onboard battery jumper W3. The board is shipped with W3 jumper set to OFF (onboard battery disconnected). This jumper must be shorted (ON) for proper battery operation.
2. CMOS battery is no longer functional. It should be replaced.

CMOS CHECKSUM ERROR

Checksum of CMOS is incorrect. This indicates that CMOS has become corrupt. This error may have been caused by a weak battery. Check the battery and replace if necessary.

DISK BOOT FAILURE, INSERT SYSTEM DISK AND PRESS ENTER

No boot device was found. This could mean either a boot drive was not detected or the drive does not contain proper system boot files. Insert a system disk into Floppy Drive A and press Enter. If you assumed the system would boot from the hard drive, make sure the controller is inserted correctly and all cables are properly attached. Also be sure the disk is formatted as a boot device. Then reboot the system.

KEYBOARD ERROR OR NO KEYBOARD PRESENT

Cannot initialize the keyboard. Make sure the keyboard is attached correctly and no keys are being pressed during the boot.

If you are purposely configuring the system without a keyboard, set the error halt condition in Setup to HALT ON ALL, BUT KEYBOARD. This will cause BIOS to ignore the missing keyboard and continue the boot.

OFFENDING SEGMENT

This message is used in conjunction with the I/O CHANNEL CHECK and RAM PARITY ERROR messages when the segment that has caused the problem cannot be isolated.

PRESS F1 TO DISABLE NMI, F2 TO REBOOT

When BIOS detects a Non Maskable Interrupt condition, this will allow you to disable the NMI and continue to boot, or you can reboot the system with the NMI enabled.

F. EMERGENCY PROCEDURE

Symptoms:

- No POST code on a power up (when using a POST card).
- Board does not boot, even after usual hardware and connection verifications.
- At power up, there is floppy disk led activity, which is one sign that the BIOS as detected a corrupted BIOS CRC prior POST and falled back automatically to Emergency Recovery Mode looking for the floppy Emergency disk.

Please go on our FTP site in order to get the latest Emergency Recovery BIOS for that specific product.

BIOS maybe found at: Ftp://Ftp.Kontron.ca/Support/BIOS_Emergency/

Emergency Recovery Procedure is included within the Zip file of the Emergency BIOS to download. Latest Emergency Recovery procedure can be found on the FAQ section of the FTP site under FAQ # KC_0028 at location:

ftp://ftp.kontron.ca/Support/Support_FAQ - Questions & Answers/

G. GETTING HELP

At Kontron, we take great pride in our customer's successes. We strongly believe in providing full support at all stages of your product development.

If at any time you encounter difficulties with your application or with any of our cts, or if you simply need guidance on system setups and capabilities, you may contact our Technical Support department at:

CANADIAN HEADQUARTERS
Tel. (450) 437-5682
Fax: (450) 437-8053

If you have any questions about Kontron, our products or services, you may reach us at the above numbers or by writing to :

Kontron inc.
616 Curé Boivin
Boisbriand, Québec
J7G 2A7 Canada

LIMITED WARRANTY

KONTRON INC, ("The seller") warrants its boards to be free from defects in material and workmanship for a period of two (2) years commencing on the date of shipment. The liability of the seller shall be limited to replacing or repairing, at the seller's option, any defective units. Equipment or parts, which have been subject to abuse, misuse, accident, alteration, neglect, or unauthorized repair are not covered by this warranty. This warranty is in lieu of all other warranties expressed or implied.

G.1 RETURNING DEFECTIVE MERCHANDISE

If your Kontron product malfunctions, please do the following before returning any merchandise:

1) Call our Technical Support department in Canada at (450) 437-5682. Make certain you have the following at hand:

   - The Kontron Invoice number
   - Your purchase order number
   - The serial number of the defective board.

2) Give the serial number found on the back of the board and explain the nature of your problem to a service technician.

3) If the problem cannot be solved over the telephone, the technician will further instruct you on the return procedure.

4) Prior to returning any merchandise, make certain you receive an RMA number from Kontron's Technical Support and clearly mark this number on the outside of the package you are returning. To request a number, follow these steps:

   - Make a copy of the request form on the following page.
   - Fill out the form and be as specific as you can about the board's problem.
   - Fax it to us.

5) When returning goods, please include the name and telephone number of a person whom we can contact for further explanations if necessary. Where applicable, always include all duty papers and invoice(s) associated with the item(s) in question.

6) When returning a Kontron board:

   i) Make certain that the board is properly packed: Place it in an antistatic plastic bag and pack it in a rigid cardboard box.

   ii) Ship prepaid to (but not insured, since incoming units are insured by Kontron):

Kontron inc.
616 Curé Boivin
Boisbriand, Québec
J7G 2A7 Canada

RETURN TO MANUFACTURER AUTHORIZATION REQUEST

Contact Name : _____

Company Name :_____

Street Address : _____

City : _____ Province/State: _____

Country : _____ Postal/Zip Code: _____

Phone Number : _____ Extension : _____

Fax Number : _____

Serial Number	Failure or Problem Description	P.O. # (if not under warranty)

Fax this form to Kontron's Technical Support department in Canada at (450) 437-8053