

cPCI-DXS64

6U CompactPCI® 64-bit System Dual Processor

Technical Reference Manual
Version 1.3, February 2003

Note: The latest releases of the Technical Reference Manuals are available at:
ftp://ftp.kontron.ca/Support/Product_Manuals/



www.kontron.com

Ref. : M6001_TECH (board revision 0)

FCC COMPLIANCE STATEMENT

Warning

Changes or modifications to this unit not expressly approved by the party responsible for the compliance could void the user's authority to operate this equipment.

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference, in which case the user will be required to correct the interference at his or her own expense.

European Statement

Warning

This is a class A product. In a domestic environment, this product may cause radio interference in which case the user may be required to take adequate measures.

Safety Standard

UL Recognized Component, File # E186339 vol. 1 section 2

Care and handling precautions for Lithium batteries

- Do not short circuit
- Do not heat or incinerate
- Do not charge
- Do not deform or disassemble
- Do not apply solder directly
- Do not mix different types or partially used batteries together
- Always observe proper polarities

FOREWORD

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READ ME FIRST

Your computer board has a standard non-rechargeable lithium battery. To preserve the battery lifetime, **the battery enable jumper is removed when you receive the board**. If you do not have any jumper cap, we suggest you to use the Watchdog Timer jumper cap.

EXERCISE CAUTION WHILE REPLACING LITHIUM BATTERY

WARNING

Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.

ATTENTION

Il y a danger d'explosion s'il y a remplacement incorrect de la batterie. Remplacer uniquement avec une batterie du même type ou d'un type équivalent recommandé par le constructeur. Mettre au rebut les batteries usagées conformément aux instructions du fabriquant.

ACHTUNG

Explosionsgefahr bei falschem Batteriewechsel.
Verwenden Sie nur die empfohlenen Batterietypen des Herstellers. Entsorgen Sie die verbrauchten Batterien laut Gebrauchsanweisung des Herstellers.

ATENCION

Puede explotar si la pila no este bien reemplazada.
Solo reemplazca la pila con tipas equivalentes segun las instrucciones del manifacturo. Vote las pilas usadas segun las instrucciones del manifacturo.

IMPORTANT

J1 and J2 are de-facto industry standard as defined by PICMG

J3, J4 and J5 are user-defined connectors and will vary from various manufacturers. Contact our Technical Support to verify pinout compatibility with other chassis backplane vendors.

POWERING-UP THE SYSTEM

If you should encounter a problem, verify the following items:
Make sure that all connectors are properly connected.
Verify your boot device.
If the system still does not start up properly, you should try booting your system with only the power cord and video monitor connected to the board this is the minimum required to see if the board is working).
If you still are not able to start up your system, please refer to the emergency Procedure in the Appendix Section.
If you still are not able to get your board up and running, contact our technical Support department for further assistance.

ADAPTER CABLES

While adapter cables are provided from various sources, the pinout is often different. The direct crimp design offered by Kontron allows the simplest cable assembly. All cables are available from Kontron Sales Department.

UNPACKING AND SAFETY PRECAUTIONS

Static Electricity

Since static electricity can damage the board, the following precautions should be taken:

1. Keep the board in its antistatic package, until you are ready to install it.
2. Touch a grounded surface or wear a grounding wrist strap before removing the board from its package; this will discharge any static electricity that may have built up in your body.
3. Handle the board by the edges.

Storage Environment

Electronic boards are sensitive devices. Do not handle or store devices near strong electrostatic, electromagnetic, magnetic or radioactive fields.

Power Supply

Before any installation or setup, ensure that the board is unplugged from power sources or subsystems.

Unpacking

Follow these recommendations while unpacking:

1. After opening the box, save it and the packing material for possible future shipment.
2. Remove the board from its antistatic wrapping and place it on a grounded surface.
3. Inspect the board for damage. If there is any damage, or items are missing, inform immediately Kontron.

When unpacking you will find:

1. 6U CompactPCI® 64-bit System Processor board
2. One Quick Reference sheet
3. One CDROM containing drivers.
4. Keyboard/Mouse Y cable

TABLE OF CONTENTS

1. PRODUCT DESCRIPTION 7

1.1. Product Overview 1-1

1.2. Board Specifications 1-2

1.3. Product Options 1-6

1.4. Hot Swap capability 1-7

1.5. Interfacing with the Environment 1-9

1.5.1. CPCI 1-9

1.5.2. Mezzanine 1-9

1.6. Compatibility with other KONTRON Products 1-10

1.7. Mezzanine Card Concept 1-11

1.7.1. Kontron's Mezzanine Concept 1-11

1.7.2. CompactFlash Feature 1-12

1.8. Overview of the Intel's 840 Chipset System Architecture 1-13

1.8.1. The 82840 Memory Controller Hub (MCH) 1-13

1.8.1.1. The 82840 Memory Controller Hub provides: 1-14

1.8.1.2. The 82840 MCH contains the following functionality: 1-14

1.8.2. The 82801 I/O Controller Hub (ICH) 1-15

1.8.3. The 82802 Firmware Hub (FWH) 1-15

1.8.4. The 82806 PCI 64 Hub (P64H) 1-16

1.8.5. The RDRAM Memory Interface 1-16

1.8.5.1. RDRAM Functional Description 1-17

2. ONBOARD FEATURES 19

2.1. CompactFlash Interface 2-1

2.1.1. Setups....2-1
2.2. Enhanced IDE Interfaces....2-2
2.3. Ethernet Interfaces....2-3
2.3.1. Front Plate Configuration....2-3
2.3.2. CPCI I/O Configuration....2-3
2.4. Floppy Disk Interface....2-4
2.5. PS/2 Keyboard / PS/2 Mouse Interface....2-4
2.6. Parallel Port....2-5
2.6.1. Standard Mode....2-6
2.6.2. EPP Mode....2-6
2.6.3. ECP Mode....2-6
2.7. Serial Ports....2-7
2.7.1. SERIAL PORT A....2-7
2.7.1.1. Front Plate Configuration....2-7
2.7.1.2. CPCI I/O Configuration....2-7
2.7.2. Serial Port B....2-8
2.7.2.1. RS-232 Protocol:....2-9
2.7.2.2. RS-422 Protocol:....2-9
2.7.2.3. RS-485 Protocol:....2-9
2.8. Thermal Management....2-10
2.9. USB Interfaces....2-11
2.10. Video Interface....2-11
2.10.1. Supported Resolutions....2-12
2.10.2. Major Features Description....2-12
3. INSTALLING THE BOARD....13
3.1. Setting Jumpers....3-1
3.1.1. Jumper Description for the CPCI-DXS64....3-1

3.1.2. CPCI-DXS64 – Jumper Settings 3-2

3.2. Register's Description 3-3

3.2.1. Supervisor Registers 3-3

3.2.2. Register 190h: Serial port B configuration....3-3

3.2.3. Register 191h: Reset History & CPU Fault 3-4

3.2.4. Register 192h: Clearing Reset History & Lock for Watchdog 3-4

3.2.5. Register 193h: Silicon ID Chip Interface, Local I^2C, System Monitor Connector Interface 3-5

3.2.6. Register 194h & 195h....3-5

3.2.7. Register 196h: Programmable Watchdog 3-5

3.2.8. Register 197h: NMI sources & mask....3-6

3.2.9. Supervision Features....3-7

3.2.9.1. Watchdog 3-7

3.2.9.2. Dual-stage Watchdog 3-7

3.2.9.3. Power Failure Detection 3-9

3.2.10. Reset History....3-10

3.2.11. Register BITs description (summary)....3-11

3.3. Onboard Interconnectivity 3-12

3.3.1. cPCI-DXS64 Block Diagram 3-12

3.3.2. Pentium® III processor....3-13

3.3.3. Onboard Connectors and Headers 3-13

3.3.4. Front Plate Connectors and Indicators....3-14

3.3.5. CompactPCI Connectors....3-15

3.4. Customizing the Board....3-16

3.4.1. Processor and Fan 3-16

3.4.2. Backup Battery....3-17

3.4.3. Memory....3-18

3.5. Building a CPCI System....3-20

3.5.1. Backplane 3-21

3.5.2. Rear-Panel I/O 3-22

3.5.3. Storage Devices 3-24
3.5.4. Power Supply 3-24
3.5.5. Fan Tray 3-24
3.5.6. Installing the Board into a Bay 3-24
3.5.7. Connector Keying 3-25
3.5.8. Bus Mastering 3-25
3.5.9. Connection 3-25
3.6. CPCI I/O Signals 3-26
3.6.1. J3 Signal Specification 3-26
3.6.1.1. Ethernet LEDS 3-26
3.6.1.2. Ethernet 1 3-26
3.6.1.3. Serial Port C 3-27
3.6.1.4. Serial Port D 3-27
3.6.1.5. IDE LED Signals 3-27
3.6.1.6. IR Serial Port B 3-28
3.6.1.7. Hot Swap HA (High Availability) signals 3-28
3.6.2. J4 Signal Specification 3-28
3.6.2.1. Power Management 3-28
3.6.2.2. SCSI Interface 3-29
3.6.2.3. Video Interface 3-30
3.6.2.4. Ethernet 0 Interface 3-30
3.6.2.5. Hot Swap HA (High Availability) signals 3-30
3.6.2.6. IDE 1 Interface 3-31
3.6.3. J5 Signal Specification 3-32
3.6.3.1. IDE 0 Interface 3-32
3.6.3.2. USB 0 and 1 Interfaces 3-33
3.6.3.3. Floppy Disk Interface 3-33
3.6.3.4. Serial Port A 3-34
3.6.3.5. Serial Port B 3-34
3.6.3.6. Parallel Port 3-35
3.6.3.7. Miscellaneous Signals 3-35

3.6.3.8. Keyboard Interface 3-36
3.6.3.9. Mouse Interface 3-36

4. SOFTWARE SETUP 4-1

4.1. PHOENIX BIOS Setup Program 4-1
4.1.1. Accessing the BIOS setup program 4-1
4.1.2. The Menu Bar 4-3
4.1.2.1. The Legend Bar 4-4
4.1.2.2. The Field Help Window 4-4
4.1.2.3. The General Help Windows 4-5
4.1.2.4. Main Menu Selection 4-6
4.1.2.5. Advanced Menu Selection 4-10
4.1.2.6. Power Menu Selection 4-19
4.1.2.7. Boot Menu Selection 4-21
4.1.2.8. Exit Menu Selection 4-21
4.2. Boot Utilities 4-22
4.2.1. Phoenix Quiet Boot 4-22
4.2.1.1. Press <ESC> 4-22
4.2.1.2. Press <Del> 4-23
4.2.1.3. POST Error 4-23
4.2.1.4. Keyboard Input Request 4-23
4.2.1.5. Phoenix Multiboot 4-23
4.3. INSTALLING DRIVERS 4-24
4.3.1. Video Drivers 4-24
4.3.2. Ethernet Drivers 4-24
4.3.3. Other Drivers 4-24
4.4. VT100 Mode 4-25
4.4.1. Requirements 4-25
4.4.2. Setup & Configuration 4-25

PART FIVE – Installation and Settings

A. **MEMORY & I/O MAPS**

Memory Mapping A-1

A.2 I/O Mapping A-2

B. **INTERRUPT LINES**

B.1 IRQ Lines B-1

B.2 DMA Channels B-1

C. **BOARD DIAGRAMS**

Top Devices Surface Mount C-1

BOTTOM DEVICE SURFACE MOUNT C-2

C.3 Mounting Holes C-3

C.4 Connector Holes C-4

D. **CONNECTOR PINOUTS**

D.1 cPCI- DXS64 Connectors and Headers D-1

D.2 J1 CPCI Bus D-2

D.3 J2 CPCI Bus D-3

D.4 J3 CPCI Bus D-4

D.5 J4 CPCI Bus D-5

D.6 J5 CPCI Bus D-6

D.7 J10, Video (VGA) D-7

D.8 J13, Mezzanine (SCSI) D-7

D.9 J14, Serial Port 1 - RS-232 ..... D-8

D.10 J17, CompactFlash Disk D-8

D.11 J18, USB Connectors (Face Plate) D-9

D.12 J19, Mezzanine (PCI) D-9

D.13 J20, Mezzanine (64-BIT/66MHZ) D-10

D.14 J23, Mezzanine (64-BIT/66MHZ) D-11
D.15 J21, PS/2 Mouse & Keyboard D-11
D.16 J22, mezzanine HA connector D-12
D.17 J24, Ethernet 1 and 2 ..... D-12
D.18 J25, Hot Swap Switch D-13
D.19 SW1 – Reset Switch D-13
D.20 SW2 – NMI Switch D-13
D.21 BT1, CMOS Battery Backup Connector D-13

E. **BIOS SETUP ERROR CODES**

E.1 POST Beep E-1
E.2 POST Messages E-2
E.3 Error Messages E-2

F. **BIOS UPDATE & EMERGENCY PROCEDURE**

G. **GETTING HELP** G-1

G.1 Returning Defective Merchandise H-1

PART 1

1. PRODUCT DESCRIPTION

1. PRODUCT OVERVIEW
2. BOARD SPECIFICATIONS
3. PRODUCT OPTIONS
4. HOT SWAP CAPABILITY
4. INTERFACING WITH THE ENVIRONMENT
5. COMPATIBILITY WITH KONTRON PRODUCTS
6. MEZZANINE CONCEPTS
7. OVERVIEW OF THE INTEL'S 840 CHIPSET

1.1. PRODUCT OVERVIEW

The Kontron's cPCI-DXS64 is designed to accommodate the endless demands for increased bandwidth among mission-critical voice messaging, CTI and Internet/Intranet server applications.

The cPCI-DXS64 packs new power onto a single SBC by incorporating two Intel PIII-based processors at a speed of 600MHz, 700MHz and 850MHz, a front side bus of 100MHz, and up to 2GB of new PC800 Direct Rambus memory (RDRAM). Its performance is further enhanced by a 64-bit/66MHz PCI bus design, which effectively quadruples previous PCI bandwidths.

The cPCI-DXS64 6U CompactPCI system processor brings scalable multiprocessing capability to the telecom and industrial automation markets. It is designed to operate as a "system" processor and must be installed in CompactPCI system slot.

Fully hot swappable, the cPCI-DXS64 communicates with other processor boards using the CompactPCI backplane as the physical layer of a 1 Gb/s Ethernet.

To provide the necessary interconnect, support local versions of the following OSs: Microsoft Windows NT, Microsoft Windows 2000, Linux, VxWorks and pSOS.

Multi-level PCI-to-PCI bridging is fully supported. Based on Intel's 21154 PCI-to–PCI - transparent bridge, the feature set of the cPCI-DXS64 includes a rich selection of standard peripherals.

The cPCI-DXS64 offers a natural growth path to high performance, high availability as well as hot swap and scalable multiprocessing technology. It can be ordered in either front I/O interfacing (video, serial port, 2xEthernet, all available on the face plate) or rear I/O interfacing through CPCI I/O connectors J3, J4 and J5 (no interconnection capability on the face plate).

CompactPCI Connectors

Rear I/O CPCI connectors are PICMG 2.0 Rev 3.0 compliant. CompactPCI connectors are located at the rear edge of the processor board. The complete CPCI connector configuration of the cPCI-DXS64 is composed of four connectors referred to as J1, J2, J3, J4, and J5.

Their function is described below:

J1	32 bit PCI signaling, power
J2	64 bit extension, arbitration, clocks, reset and power
J3, J4, J5	Handle I/O signals.

CompactPCI™ connectors are also known as 2mm Hard Metric connectors.

1.2. BOARD SPECIFICATIONS

FEATURES	DESCRIPTION
Overview	6U CompactPCI 64-bit System Processor board
Supported Microprocessors	Single / Dual Pentium III Processor (FC-PGA) at 600, 700 and 850MHz
CHIPSET	• Intel 840 AGPset. • 21-signal High-Availability controller: Select, Healthy, Reset for 7 CPCI I/O slots
Bus Interface	• Front side bus at 100 MHz • Local PCI Bus at 64-bit/66MHz (for PCI-PCI bridges and SCSI controller) • CompactPCI bus up to 64-bit/66MHz • Dual PCI-to-PCI bridge: Intel 21154; supports up to 14 REQ/GNT for fully loaded CompactPCI system • Video AGP 2X • SMBus (for system management of CPU temperature monitoring, DRAM control, and power monitoring) • Kontron embedded mezzanine for second PCI bus, SCSI, and EIDE
Cache Memory	• 16K/16K Instruction / Data CPU-internal Level 1 • 256KB 64-bit wide on-die Level 2 Advanced Transfer Cache
System Memory	• Four 184-pin latching RIMM sockets • Up to 2GB of RDRAM with parity or ECC (for single bit error correction and double bit error detection)
Data Path	• 64-bit on CPU, 32-bit on video memory; 32-bit on first local PCI (Ethernet) ,64-bit on second local PCI (Bridge and Mezzanine) and 64-bit on CompactPCI
Interrupts	8 CompactPCI interrupts, configurable to any interrupt vector for PnP compatibility
Flash Memory	• 1MB Firmware Hub for BIOS field upgrade • Silicon Serial ID TAG for unique board identification accessible via software • 4KB user serial EEPROM
Video	• 64-bit AGP video controller (Intel 69000) with 2MB video memory • CRT resolutions up to 1024 x 768 x 64K colors or 1280 x 1024 x 256 colors

Board Specifications (continued)

Clock/Calendar	Real-time clock with (replaceable) battery backup, CMOS RAM
Connectors in "Front" configuration	**Front Plate** CRT — 15-pin D-Sub COM1 — 9-pin D-Sub Ethernet 1 and 2 — 2 x RJ-45 with built-in LEDs PS/2 mouse + Keyboard — 6-pin mini-DIN USB — 4-pin USB
Interfaces on J3/J4/J5	**Rear CPCI I/O Connectors (J3/J4/J5)** *(Rear-panel transition module, cTM80-STD2S available separately)* CRT, Serial Ports (4), USB (2) Parallel Port, SMBus, I^2C Speaker I/F, Reset Switch, Ethernet (2) PS/2 mouse, Keyboard, SCSI EIDE (2), Floppy disk I/F Fan fail monitoring **Onboard Expansions** PCI Mezzanine Card PMC. Proprietary mezzanine. CompactFlash.
I/O	**I/O** — SMSC LPC47B277 super I/O **USB Ports** — Two (USB 1.1 compliant) **Serial Ports** — Serial Ports: Two (one RS-232 COM1, COM2 configurable as RS-232/422/485 **Parallel Port** — One bi-directional with all IEEE 1284 protocols supported with BIOS selectable IRQs and addressing **Floppy Disk** — Support for two drives (360KB to 1.44MB) **EIDE** — PCI EIDE Ultra DMA/66, support for four IDE drives in a master/slave configuration, PIO Mode4, Bus Master IDE or synchronous DMA mode transfers up to 66MB/s **CompactFlash™** — Optional bootable CompactFlash™ disk interfaces to primary EIDE channel, user upgradable, master/slave. **Ethernet** — Two 10/100Mb/s Ethernet, PCI 10/100Base-TX ports (Intel 82559 controller) HD Mezzanine Card: Optionally onboard using Kontron's cMC series mezzanine cards. **HD Mezzanine Card** — Always Onboard **SCSI** — PCI-ULTRA160 (Ultra3) LVDS SCSI supports up to 320 MB/s dual channel or 160 MB/s single channel (Symbios 53C1010)

Board Specifications (continued)

Supervisory	▸ Two-stage software programmable Watchdog timer drives NMI on first stage and system reset on second stage. Time out from 16msec to 4.5min ▸ **Hardware system monitor** • Power failure detector • Low battery voltage detector • CPU temperature sensor / thermal management • Board temperature sensor • 12V, 5V, 3.3V, 2.5V and Vcore voltage supervisor • Front Panel LEDs: IDE / SCSI activity, Ethernet activity & link
OS Compatibility	▸ **Dual CPU configuration** • Microsoft Windows NT 4.0 • Microsoft Windows 2000 Professional (with and without ACPI) • Linux Red Hat 6.2 • BDSi 4.1 • Sun Solaris 8 • BeOS 5 • OS/2 WARP 4.5 E-Business Server • Novell Netware 5.1 ▸ **Single CPU configuration** • All above mentioned OSs, and the following**:** • MS-DOS 6.22 • PC DOS 2000 • Microsoft Windows 95 OSR2 • Microsoft Windows 98 SE • QNX 4.25 + Photon
BIOS Features	• Phoenix BIOS in Boot Block Flash with recovery code. • Save CMOS in Flash option and Boot from LAN capability. • CC000-E0000 address blocking; PnP tables • Setup console redirection to serial port (VT100 mode) with CMOS setup access • Software enable/disable of onboard Ethernet; hardware enable/disable of onboard video • Diskless, keyboardless, and videoless operation extensions • Programmable I/O wait states • Advanced security feature for floppy and HDD; DMI & HDD S.M.A.R.T. support • Intelligent System Monitoring (chassis intrusion and advanced thermal management such as resume, overheat alarm and auto slow down) • such as resume, overheat alarm and auto slow down) • Green support

Board Specifications (continued)

Mechanical	Compliant to IEEE 1101.10, compliant to PICMG2.0 Rev 2.1) 233x160x41 mm / 9.2 x 6.3 x 1.6 in, 6U x 8HP (dual slot) Mechanically 233x160x20.5 mm / 9.2 x 6.3 x 0.8 in;6U x 4HP (single slot) Mechanically		
Power Requirements	Supply Voltages : +3.3, ±-5%, +5V ±5%, +12V ±5% Supply Current:***** +3.3V, 4.5 Amps maximum +5V, 9 Amps maximum +12V, 0.1 Amps maximum Power Dissipation cPCI-DXS64 : 60W maximum *Tested with Pentium III processor 600Mhz and 1GB RAMBUS		
Environmental		Operating	Storage and Transit
	Temperature	0-50°C / 32-122°F	-40 to +70°C / -40 to 158°F
	Humidity	5% to 95% @ 40°C/104°F non-condensing	5% to95% @ 40°C/104°F non-condensing
	Altitude	4,572m / 15,000 ft	15,240m / 50,000ft
	Shock	Designed to meet IEC 68-2-27	
	Vibration	Designed to meet IEC 68-2-6	
	Reliability	MTBF: 100,000 hours @ 55°C/131°F (MIL-HDBK-217F) Board serial number in EEPROM USB, keyboard and mouse protected by self-resetting fuse 2 year limited warranty Designed to meet or exceed : Safety: UL1950, CSA C22.2 No 950, EN 60950, IEC950 EMI/EMC: FCC 47 CFR Part 15/CISPR22, Class B, CE Mark to EN55022/EN50082	

1.3. PRODUCT OPTIONS

The cPCI-DXS64 can be purchased either for front plate I/O interfacing (video serial port, Ethernet) or RTM (Rear Transition Module) I/O interfacing (no interconnection capability available on the front plate) through CPCI I/O connectors and backplane.

▪ CompactPCI Connectors

Rear panel CPCI connectors are PICMG 2.0 Rev3.0 CompactPCI™ specification compliant. CompactPCI connectors are located at the rear edge of the board. The complete CPCI connector configuration is composed of five connectors referred to as J1, J2, J3, J4, and J5.

Their function is described below:

J1/J2	carry out arbitration and PCI bus signals, and power.
J3/J4/J5	handle I/O signals.

CompactPCI™ connector is also known as 2mm Hard Metric connector.

1.4. HOT SWAP CAPABILITY

The cPCI-DXS64 supports Hot Swap capability which means that hot swappable boards can be removed from or installed in the system while online (without powering-down the system).

Hot Swap consists of board hardware with the Hot Swap additions to the Hardware Connection Layer, and the Hot-Plug Service. Upon insertion of the board (any hot swappable board but the system host, cPCI-DXS64, the hardware connection layer will initialize the board and the Hot-Plug Service provides the means for reconfiguring the system.

High Availability is an attribute of a system designed to keep running (maintain availability) in case of a system component failure. To provide a high degree of availability, a system requires a higher degree of control.

High Availability (HA) uses a higher degree of control than just indicating insertion and extraction. HA systems are able to control the Hardware Connection Process. To do this, the capabilities of the system are extended to allow software control of a board's hardware connection state. A hardware connection sequence is made possible using different pin lengths and the process ends with the mating of the shortest pin (BD_SEL#).

The platform adds hardware to provide more control of each board's Hardware Connection Layer. The signals: BD_SEL#, HEALTHY#, and PCI_RST# are used to individually control each slot of the system.

BD_SEL# is one of the shortest pins. This pin is the last to mate and the first to break contact. This ensures that the sensing of its connection takes place at a time when all other pins are reliably connected. It is driven low to enable power on. For systems not implementing hardware connection control, it is grounded on the backplane.

HEALTHY# is used to acknowledge the health of the board. It signals that a board is suitable to be released from reset and allowed onto the PCI bus. In an HA system, the software can detect a faulty board when it fails to assert HEALTHY# after BD_SEL# has been asserted. A running board can also become not healthy at any time.

PCI_RST# as defined by the CompactPCI® Specification, is a signal on the backplane, driven by the system host. Platforms may implement this signal as a radial signal from the Hot Swap Controller to further control the electrical connection process. Platforms that do this must OR the system host's reset signal with the slot specific signal to maintain the bussed signal's function.

The Software Connection Control resources on the board provide a signal (ENUM#) for system host notification and a switch and LED to interface with the operator.

Full Hot Swap boards drive the ENUM# signal to the system host to indicate a service request. This signal is provided to notify the system host that a board either has been freshly inserted or is about to be extracted. This signal informs the system host that the configuration of the system has changed. The system host then performs any necessary maintenance such as installing a device driver upon board insertion, or unloading drivers for hot swap boards that are about to be extracted. The application that is using the board is also notified that the resource will no longer be available.

The Hot Swap Switch allows the operator to indicate desire to extract the board. A blue LED, located on the front of the board, is illuminated when it is safe to extract the board. This LED indicates that system software has been placed in a state for orderly extraction of the board. The hardware connection layer provides protection only for the hardware during insertions and extractions. This method allows the operator to insert or extract boards without the extra step of reconfiguring the system at the console.

WARNING

All actions are initiated by the operator, and must be performed in the correct sequence for proper system operation.

Full Hot Swap boards present the following resources to software executing on the system host (nominally implementing the Hot-Plug Service and Hot-Plug System Driver)

- An ENUM# signal, which is an open collector (open drain) bussed signal, to signal a change in status for the board.
- A switch actuated with the lower ejector handle, indicating the beginning of the extraction process or end of the insertion process.
- A LED to indicate the status of the software connection process.
- A set of four control and status bits on each board allows the system host's software to determine the source of the ENUM# signal and control the LED.

Full Hot Swap boards allow the full range of system capabilities.

1.5. INTERFACING WITH THE ENVIRONMENT

1.5.1. CPCI

The cPCI-DXS64 system processor is provided for rack-mounted systems to offer the highest modularity. Through the J1/J2 segment, the board can drive up to seven external CompactPCI slots, supporting individual REQ/GNT arbitration pair signals and clock.



NOTE

All I/O signals are available in front I/O and rear I/O configuration.

A. In front I/O configuration, the following I/Os signals are available on the faceplate: SVGA, Serial Port A, Ethernet 1 and 2, keyboard and mouse, USB. All other I/Os are connected to J3-J5.

B. In Rear I/O configuration, all I/O signals are connected to J3-J5

A backplane dedicated to the cPCI-DXS64 is provided by Kontron and is referred to as cBP08R, CPCI Passive Backplane.

1.5.2. Mezzanine

The mezzanine is a hardware interface concept introduced by Kontron to increase the I/O connectivity of the cPCI-DXS64, but respecting the dual slot 6U form factor restrictions.

The onboard mezzanine connector features PCI bus, and IDE signals, for mezzanine applications: Kontron provides a storage/bridging mezzanine with an optional hard drive.

A complete *CompactPCI* development system CxP-0816 is also available from Kontron.

1.6. COMPATIBILITY WITH OTHER KONTRON PRODUCTS

The cPCI-DXS64 System Processor is a member of the Kontron's CompactPCI product family.

The boards are fully compliant with the PICMG 2.0 Rev.2.1 and PICMG 2.1 CompactPCI specifications.

When building a basic environment around the cPCI-DXS64, the platform may be composed of any of the following devices:

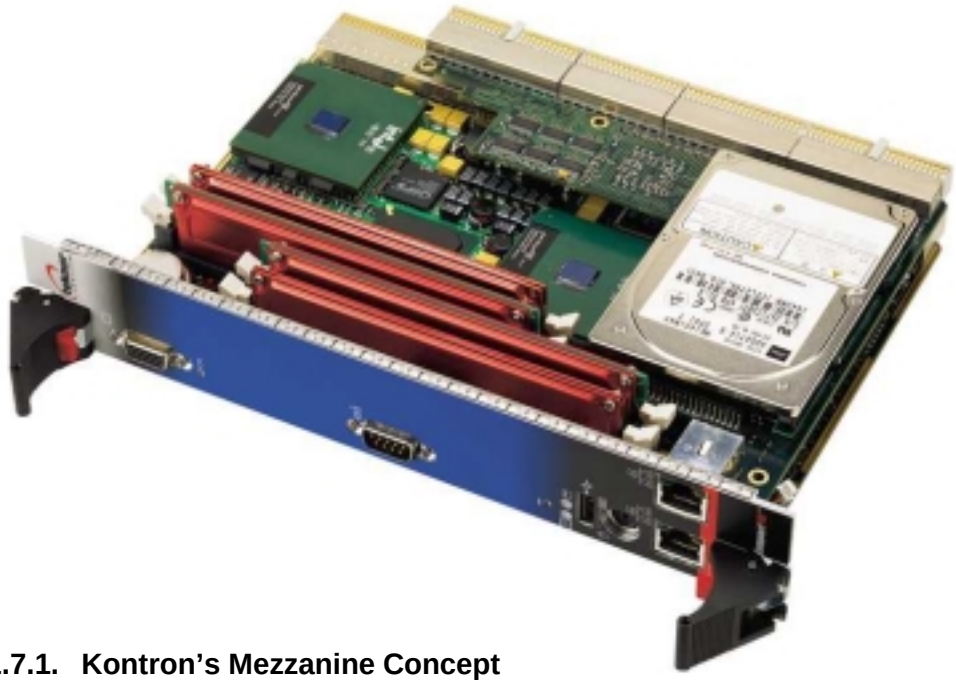
- cPCI-DXS64 6U System Processor
- cSM-DVDHD Storage module with DVD and Hard Disk
- cSM-DVD Storage module with DVD only
- CxP0816 including
    - 8U 19-inch enclosure
    - Front loaded hot swappable 2U fan tray
    - Power supply (300W ATX or 350W AC or DC in single or redundant configuration)
    - One of the following backplanes:

        cBP-08R : 8 slots CompactPCI (PICMG 2.1)

        cBP-16R, 16 slots CompactPCI (PICMG 2.1)
- cTM80-STD2S 6Ux8HPx80mm Rear Transition Module, standard pinout.

1.7. MEZZANINE CARD CONCEPT

The capability of the cPCI-DXS64 to connect with other devices is enforced by PCI Mezzanine Cards (PMC). A fully equipped cPCI-DXS64 board may appear as follows:



1.7.1. Kontron's Mezzanine Concept

This is Kontron's concept to expand the I/O capability of the board. It is built around two connectors:

- Mezzanine connector handling IDE signals.
- Mezzanine connector handling a complete PCI signal set (primary bus) including the REQ/GNT arbitration signal pair.

These two connectors represent an open door for future development of expansion and I/O mezzanine cards.

1.7.2. CompactFlash Feature

The cPCI-DXS64 board also supports standard CompactFlash disk through a CompactFlash module.

CompactFlash disk is a method of storing and transferring data. It is supported on the board as a standard IDE drive and connects to the primary EIDE interface.

The CompactFlash drive can be set as a Master or Slave device and combined with any standard hard disk drive by setting the jumper W6 (5-6) (see Section 3.1, setting jumpers).

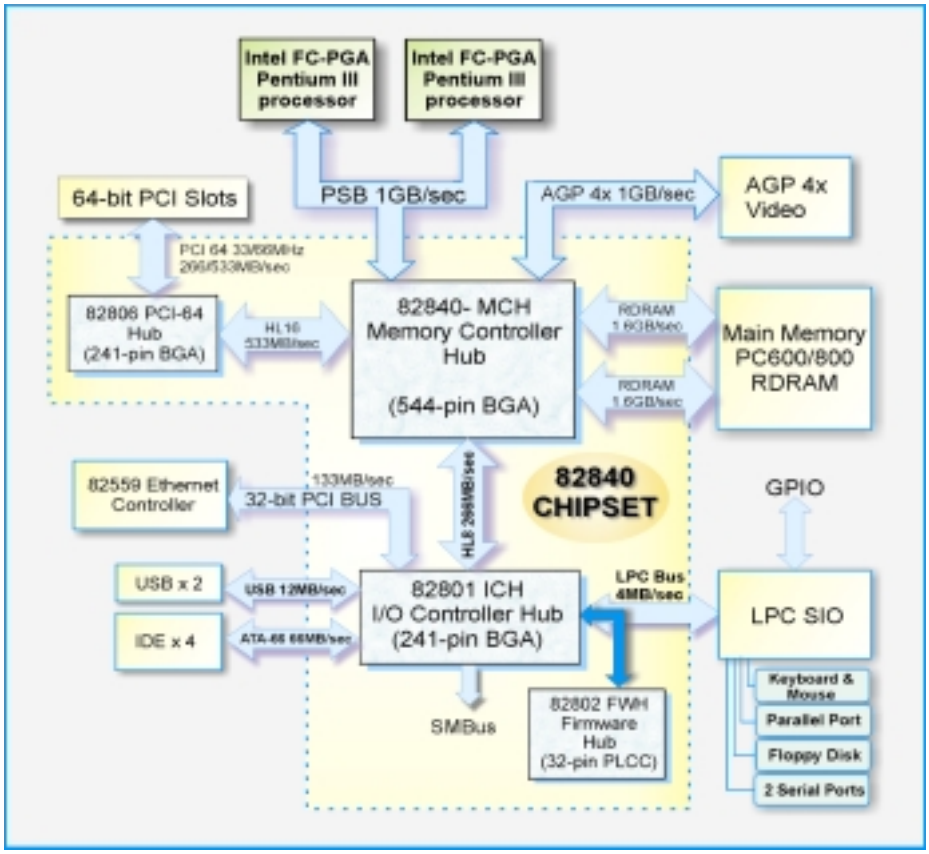
CompactFlash is installed on J17 connector. For more information on CompactFlash installation and setups, please refer to Section 2.1 – *CompactFlash Interface*.

1.8. OVERVIEW OF THE INTEL'S 840 CHIPSET SYSTEM ARCHITECTURE

The chipset contains three main components:

- The 82840 Main Controller Hub (MCH)
- The 82801 I/O Controller (ICH)
- The 82802 Firmware Hub (FWH)

1.8.1. The 82840 Memory Controller Hub (MCH)



1.8.1.1. The 82840 Memory Controller Hub provides:

- The processor interface
- The system bus interface
- The memory controller (DRAM interface)
- An AGP interface
- A hub interface for I/O
- A hub interface for PCI expansion.

It supports dual channels of Direct Rambus DRAM operating in lock-step. It also supports 4x AGP data transfers and 2x/4x AGP Fast Writes.

The MCH contains advances power management logic. The Intel 840 chipset platform uses the dedicated I/O Controller Hub (ICH) designed for use with the MCH to provide the features required by a workstation or a server platform. In addition, the 82840 MCH implements a second 16-bit/66MHz port that is used to connect an advanced 64-bit PCI interface (P64H). Communication with ICH and P64H is accomplished via a high-speed interface called “hub interface”.

1.8.1.2. The 82840 MCH contains the following functionality:

- Support for Single/Dual Processor configuration
- AGTL+host bus supporting 32 or 36-bit host addressing, 100/133MHz
- Dual Direct Rambus channels supported for 300MHz or 400MHz operation
- 2GB support for RDRAM devices
- AGP interface with 4x SBA/Data Transfer and 2x/4x Fast Write capability
- 8-bit, 66MHz hub interface A to ICH
- 16-bit, 66MHz hub interface B to P64H
- Fully optimized data paths and buffering
- Distributed arbitration for highly concurrent operation

1.8.2. The 82801 I/O Controller Hub (ICH)

The ICH is a highly integrated multifunctional I/O Controller Hub that provides the interface to the PCI Bus and integrates many of the functions needed in today's PC platforms. The MCH and ICH communicate over a dedicated hub interface. Functions and capabilities include:

- PCI Rev 2.2 compliant with support for 33MHz PCI operations
- Upstream hub link to the MCH
- Supports up to 6 Req/Gnt pairs (PCI slots)
- Power Management Logic Support
- Enhanced DMA Controller, Interrupt Controller and Timer Functions
- Integrated IDE controller; 2 channel Ultra ATA/66 Bus Master IDE controller
- USB host interface with support for 2 USB ports
- System Management Bus (SMBus)
- Firmware Hub (FWH) interface support
- Alert on LAN

1.8.3. The 82802 Firmware Hub (FWH)

This device operates under the FWH interface/protocol. It provides the boot flash memory for the system (BIOS)

Functions and capabilities include:

- 8M-bits of flash memory
- Interfaces to ICH using FWH protocol (sharing of LPC bus)
- Operates with 33MHz PCI clock
- 64K-byte symmetric blocks
- Hardware Random Number Generator
- 5 GPI ports
- Address/Address Multiplexed (A/A Mux) interface for programming
- Hardware protection for the top boot block
- Available in 32-pin PLCC or 40-pin TSOP

1.8.4. The 82806 PCI 64 Hub (P64H)

The PCI-64 Hub (P64H) is a peripheral chip that performs PCI bridging functions between the hub interface and the PCI Bus and is used as an integral part of the Intel® 840 chipset. The P64H has a 16-bit primary hub interface to the Memory Controller Hub (MCH) and secondary 64-bit or 32-bit devices. The P64H is fully compliant with the PCI Local Bus Specification, Revision 2.2. The P64H functions include:

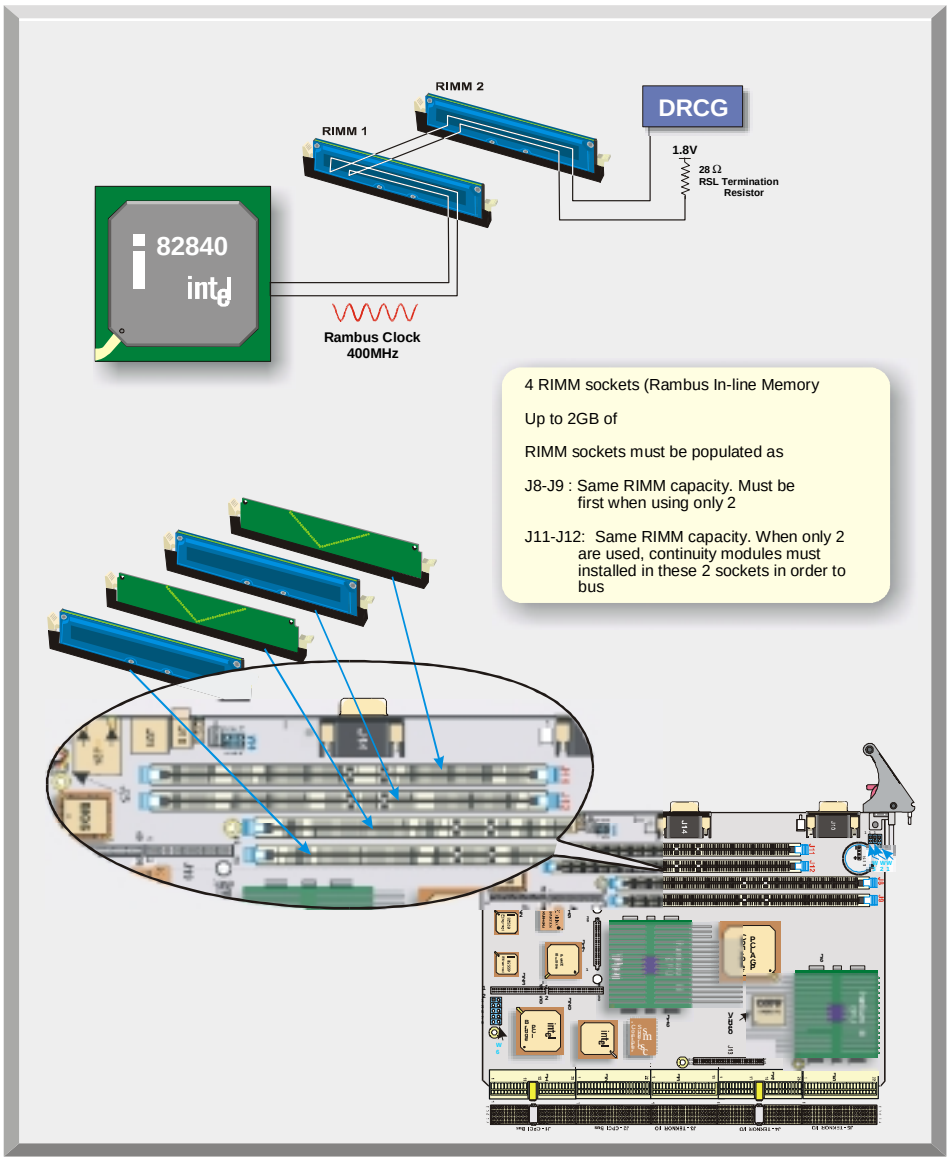
- Upstream 16-bit hub link to the MCH
- Supports both 64-bit/32-bit, 33MHz or 66MHz devices
- Arbitration support for 6 PCI devices
- Supports either 2 x 66MHz or 4 x 33MHz PCI slots
- I/O APIC to provide 24 interrupts
- 6 copies of PCI clocks
- Supports PERR# and SERR#
- Integrated PCI low skew clock driver

1.8.5. The RDRAM Memory Interface

The RDRAM memory interface features:

- Dual RDRAM channel, PC800 or PC600 support
- 400MHZ or 300MHz differential clocks provided by 2 Direct Rambus Clock Generators (DRCG)
- 4 RIMM sockets (Rambus In-Line Memory Module), up to 2GB of memory
- All 4 sockets must be equally populated. A continuity Module is required in empty sockets to censure a bus continuity
- Up to 8 simultaneous open pages
- 3 operating modes: Active, Standby and NAP.

1.8.5.1. RDRAM Functional Description



PART 2

2. ONBOARD FEATURES

1. COMPACTFLASH INTERFACE
2. ENHANCED IDE INTERFACES
3. ETHERNET INTERFACES
4. FLOPPY DISK INTERFACE
5. PS/2 KEYBOARD AND MOUSE INTERFACE
6. PARALLEL PORT
7. SERIAL PORTS
8. THERMAL MANAGEMENT
9. USB INTERFACES
10. VIDEO INTERFACES

2.1. COMPACTFLASH INTERFACE

The board supports an IDE compatible flash disk by using a CompactFlash module. CompactFlash (C-Flash) disks are the resident industry-standard ATA/IDE subsystem for application, data, image, and audio storage. They have the same functionality and capabilities as intelligent disk drives, but with the advantages of being very compact, rugged (typical M.T.B.F. is 1,000,000 hours) and low power. The cPCI-DXS64 supports all CompactFlash sizes presently available and future sizes when available.

The C-Flash disk connects on the cPCI-DXS64 via the onboard Flash Disk connector.

Related Jumpers

cPCI-DXS64: W6 (5-6) to set the CompactFlash disk as master or slave.

BIOS Settings

Section 4.1.2.4 Main Menu Selection: Hard Disk auto-detection to set the type of hard disk.

2.1.1. Setups

The CompactFlash disk connects directly on the primary EIDE interface. It must be declared the same way as a standard hard disk using the BIOS setup program (Auto-detect function).

To setup the CompactFlash disk for Master or Slave configuration, use the CompactFlash jumper located on the system processor.

To locate and install this jumper, please refer to Section 3.1, *Setting Jumpers*.



NOTE

Since device use ATA/IDE interface, no specific flash disk driver is required for various operating systems.

2.2. ENHANCED IDE INTERFACES

The board features two channel Bus Master PCI EIDE dedicated to Primary and Secondary IDE logical interfaces. Each channel supports up to two IDE devices (including CD-ROMs, hard disks, plus CompactFlash on the secondary IDE interface) with independent timings, in Master/Slave combination.

Signal Paths

The primary IDE interface is available through both the CPCI I/O connector and the Mezzanine connector.

The secondary IDE interface is only available through the CPCI I/O connector.

Related Jumpers

None

BIOS Settings

Section 4.1.2.5 , Advanced Menu Selection

The IDE interfaces supports PIO mode 4 transfers up to 16.6MB/sec and Bus Master IDE transfer up to 66MB/sec (Ultra-DMA 66).

CAUTION

When connecting IDE devices to the Primary IDE interface, Master and Slave devices must be shared in respect of the device allocation on both the CPCI I/O connector and the mezzanine

Two Master devices (or two Slave devices) must not be installed on the same interface at the same time.

2.3. ETHERNET INTERFACES

Both Ethernet controllers reside on the Primary PCI bus.

Each interface supports 10Base-T and 100Base-TX specifications: 10Mbps and 100Mbps network speeds are automatically detected and switched.

Related Jumpers
None.

BIOS Settings
Section 4 Advanced Menu, Onboard Ethernet Controller.

2.3.1. Front Plate Configuration

Ethernet 1 and 2 signals are available on front plate connectors only when the board is ordered for front access.

Activity and link indicators are built in the connector.

2.3.2. CPCI I/O Configuration

> **CAUTION**
>
> The combination of both front and rear panel configurations is not supported.

The Boot from LAN capability is supported. To enable the option, use the BIOS Setup program. Please refer to Section 4.1 PHOENIX BIOS Setup Program.

A diskette entitled **"Network Drivers** for Intel 82559 is included with the cPCI-DXS64. It contains network drivers for most common operating systems.

2.4. FLOPPY DISK INTERFACE

The onboard floppy disk controller is IBM PC XT/AT compatible. It handles 3.5" and 5.25", low and high density disks. Up to two drives can be supported in any combination.

Signal Paths

The Floppy Disk Controller interface is available through the CPCI I/O connector.

Related Jumpers

None.

BIOS Settings

Section 4.1.1, Main Menu, Legacy Diskette A and Legacy Diskette B.

Section 4.1.2.5, Advanced Menu Selection, I/O Device Configuration, Floppy Disk Controller and Base I/O address.

2.5. PS/2 KEYBOARD / PS/2 MOUSE INTERFACE

The onboard keyboard controller is 8042 software compatible. PS/2 Keyboard and mouse signals are available through an output that supports direct connection to the interface. Since signals of both devices are combined on the same connector, a Y-cable is required to split the signals and feed a standard AT keyboard and a PS/2 mouse.

Signal Path

PS/2 keyboard and PS/2 mouse signals are available through J5 CPCI I/O connector and J21 faceplate connector.

Related Jumpers

None.

2.6. PARALLEL PORT

The cPCI-DXS64 features one multi-mode parallel port. It is compatible with Standard Mode IBM PC/XT, PC/AT, and PS/2 compatible bi-directional parallel port, Enhanced Parallel Port (EPP), and Enhanced Capabilities Port (ECP).

Signal Path

The Parallel Port interface is only available through J5 CPCI I/O connector.

Related Jumpers

None

BIOS Settings

Advanced/ Onboard devices: Onboard Parallel Port; Parallel Port Mode

The differences between Standard, EPP, and ECP modes appear in the signal assignation of the pins on the connector. Differences are described as follows:

Pin Number (J5)	Standard Mode	EPP Mode	ECP Mode
A15	SLCT	-	SLCT
B15	PE	-	PERROR[1], ACKREVERS[2]
C15	BUSY	WAIT	BUSY[1], PERIPHACK[2]
D15	/ACK	/INTR	/ACK
E16	/SLCTIN	/ADDRSTRB	/SLCTIN
B17	/INIT	-	/INIT[1], /REVERSERQST[2]
D17	/ERR	-	/FAULT[1], /PERIPHRQST[2]
A18	ALF	DATASTB	ALF[1], HOSTACK[2]
E17	PD0	PD0	PD0
C17	PD1	PD1	PD1
A17	PD2	PD2	PD2
D16	PD3	PD3	PD3
C16	PD4	PD4	PD4
B16	PD5	PD5	PD5
A16	PD6	PD6	PD6
E15	PD7	PD7	PD7

[1] Compatible mode

[2] High Speed Mode

NOTE

To operate in EPP or ECP mode, ensure the peripheral is designed to work in this mode and the BIOS setup is configured to support it.

2.6.1. Standard Mode

The Standard mode is unidirectional. It is supported to maintain the compatibility with the IBM PC standard.

2.6.2. EPP Mode

The EPP (Enhanced Parallel Port) mode consists of a hardware independent method of accessing a parallel port configured as EPP. It provides support for single I/O cycle as well as the high performance block I/O transfers. The EPP mode always uses the optimum method for I/O transfers. For example, if the hardware supports it, EPP mode will perform 32-bit I/O block transfers.

EPP mode assumes that the parallel port can be used to connect more than one peripheral device using multiplexor or daisy chain configurations.

A multiplexor is an external device that permits up to eight parallel port devices to share a single parallel port.

A daisy chain device has two ports: input and output. The input port is connected to either the host parallel port or the daisy chain device in front of it. The output is used to connect the next peripheral device to the daisy chain. The last device, however, can be one without daisy chain support.

2.6.3. ECP Mode

ECP (Extended Capabilities Port) works the same as EPP mode, but it will take precedence over the EPP mode when addressing multiple logical devices in a single physical product. While the EPP mode may intermix read and write operations without any overhead or protocol handshaking, the ECP mode negotiates data transfers using a request from the host and an acknowledgment from the peripheral.



NOTE

For more information on the ECP protocol, please refer to the Extended Capabilities Port Protocol and ISA Interface Standard (available from Microsoft Corporation) or contact our Technical Support department.

2.7. SERIAL PORTS

Two full function serial ports are provided on the board for asynchronous serial communications. They are 16C550 high-speed UART compatible and support 16-byte FIFO buffers for transfer rates from 50bps to 115Kbps.

Each serial port is specified as follows:

Designation	Communication Mode	Output Path
Serial Port A	RS-232	Front Plate DB-9, CPCI J5
Serial Port B	RS-232/RS422/RS485	CPCI J3

UART registers are individually addressable and fully programmable.

2.7.1. SERIAL PORT A

Serial Port A is buffered directly for RS-232 operation. Signals include the complete signal set for handshaking, modem control, interrupt generation, and data transfer. When assigned as Serial Port A, the port is 100% compatible with the IBM-AT serial port in RS-232 mode.

Signal Path

Serial Port A signal path depends on the output configuration you have ordered for the board

Related Jumpers

None

BIOS Settings

Section 4.1.2.5, Advanced Menu Selection, Onboard Device Configuration, Serial Port A.

2.7.1.1. Front Plate Configuration

The Serial Port A signals are available through a DB-9 connector located on the front plate (J14).

2.7.1.2. CPCI I/O Configuration

The complete signal set is tied to the J5 CPCI I/O connector to be used through the Rear Transition Module (RTM).

2.7.2. Serial Port B

Serial Port B is buffered directly for RS-232 operations and is 16C550 PC-Compatible. The interface includes the complete signal set for handshaking, modem control, interrupt generation, and data transfer.

The Serial Port B port is 100% compatible with the IBM-AT serial port.

Signal Path
Serial Port B signals are only available through the J3 CPCI I/O connector

Related Jumpers
None

BIOS Settings

Section 4.1.2.5, Advanced Menu Selection, Onboard Device Configuration, Serial Port B.

Upon a power-up or reset, the Serial Port B interface circuits are automatically configured for the operation mode setup in the BIOS. The Serial Port B signal assignation on the J5 CPCI I/O connector depends on the operation mode (RS-232, RS-422, or RS-485) it has been set.

2.7.2.1. RS-232 Protocol:

When configured for RS-232 operation mode, the Serial Port B is 100% compatible with the IBM-AT serial port signals.

2.7.2.2. RS-422 Protocol:

The RS-422 protocol (Full Duplex) uses both RX and TX lines during a communication session.

> **CAUTION**
>
> In RS-422 mode, W6 (1-2 and 3-4) jumper caps must be installed to connect the 120 ohms termination resistors (See Section 3.1 *Jumper Settings*)

2.7.2.3. RS-485 Protocol:

The RS-485 protocol (Half Duplex) also uses differential signals during a communication session. It differs from the RS-422 mode as it offers the ability to transmit and receive over the same pair of wires, and allows the sharing of the communication line by multiple stations. This configuration (also known as Party Line) allows only one system to take control of the communication line at the time.

In RS-485 mode, the RX lines are used as the transceiver lines, and the RTS signal is used to control the direction of the RS-485 buffer.

When set for RS-485 mode in the BIOS, upon power-up or reset, the transceiver is by default in receiver mode to prevent unwanted perturbation on the line. Party line operation mode requires termination resistors to be installed at both ends of the network.

> **CAUTION**
>
> When installing the cPCI-DXS64 at one end of the network, W6 (1-2 and 3-4) jumper caps must be installed to connect the 120 ohms termination resistors (See Section 3.1 – *Setting Jumpers*).

2.8. THERMAL MANAGEMENT

The processor module includes a user-defined temperature sensor / alarm function, which provides thermal monitoring of the processor.

Two temperature sensors are provided to supervise the thermal environment. One is used to monitor the CPU die temperature, while the second one, located on the CPU casing, allows the monitoring of the ambient temperature around the CPU.

The temperature is controlled according to two temperature levels, the Low Temperature Limit, which indicates normal operating conditions, and the High Temperature Limit, which indicates an overheating condition.

The temperature management consists in reducing the CPU clock speed throttling when the temperature goes over the high limit (overheating condition) and suspending the throttling operation as soon as the temperature returns under the low temperature limit (normal condition).

The clock speed may be throttled by a CPU overheating due to the fan failure. In such a case, the temperature control is triggered as soon as the temperature reaches the high temperature limit of the die.

The ambient temperature of the CPU generally raises up due to an augmentation of the temperature in the casing. In that case, the clock speed will be slowed down as soon as the ambient temperature reaches the high ambient temperature value.

Thermal management operations are controlled by the chipset, and settings are provided through the BIOS setup program interface (see section 4.1.2.6 PHOENIX BIOS *Setup Program, Power Menu Selection, and Hardware Monitor Controls).*

2.9. USB INTERFACES

The USB strengths are as follows: capability to daisy chain as many as 127 devices per interface, fast bi-directional, isochronous/asynchronous interface, 12Mbps transfer rate, and standardization of peripheral interfaces into a single format.

Signal Paths
Both USB 0 and USB 1 interface signals are available through the CPCI I/O connector (J5) and through J18 (on faceplate).

Related Jumpers
None

BIOS Settings
Advanced : Legacy USB Support (keyboard and mouse)

USB supports Plug and Play and hot swapping operations (OS level). These user-friendly features allow USB devices to be automatically attached, configured and detached, without reboot or running setup.

The cPCI-DXS64 board fully supports the standard universal host controller interface (UHCI) and uses standard software drivers that are UHCI-compatible.

2.10. VIDEO INTERFACE

The high-performance video capability of the board is based on Accelerated Graphics Port (AGP) technology. The video controller, Intel 69000, with its integrated 2Meg of high performance SDRAM is capable of CRT resolutions up to 1024 x 768 x 64K colors or 1280 x 1024 x 256 colors.

The video interface features 64-bit 2D graphics engine, 64-bit GUI accelerator engine with multiple window video acceleration.

Signal Path
The VGA video signal path depends on the output configuration you have ordered for the board.

Related Jumpers
W3 to enable or disable onboard VGA feature.
See section 3.1 – *Jumper Settings*

BIOS Settings
Advanced PCI, Default Primary Video Adapter, Advanced Chipset Control: Graphic Aperture.

- **Front Plate Configuration**
  VGA interface signals are available on J4, standard VGA connector, located on the front plate of the board, only when the board is ordered for front access operations. This configuration allows direct connection of CRT display onto the board.

- **CPCI I/O Configuration**
  VGA interface signals are available on J10 CPCI I/O connector only when the board is ordered for rear panel output operations.

2.10.1. Supported Resolutions

The maximum video resolution and performance depend directly on the drivers running with your software application. Resolution and number of colors specification are listed below:

Resolution	Number of Colors
640x480, 800x600, 1024x768, 1280x1024	256 (8 bits)
640x480, 800x600, 1024x768	65,536 (16 bits)
640x480, 800x600	16.8 million (24 bits)
640x480, 800x600	16.8 million (32 bits)

2.10.2. Major Features Description

- **VGA Compatibility**

  The video controller includes all registers and data paths required for VGA controller and supports extensions to VGA, including resolutions up to 800x600x16.8 million colors non-interlaced. The 16-bit images are displayed at up to 1024x768 resolution.

- **2D Graphics Engine**

  The 2D graphics engine is an advanced 32-bit three-operand engine that accelerates BitBLTs as line draws, polygon draw, and polygon fill. The 2D graphics engine also performs video and bitmap scaling, and data overlay.

PART 3

3. INSTALLING THE BOARD

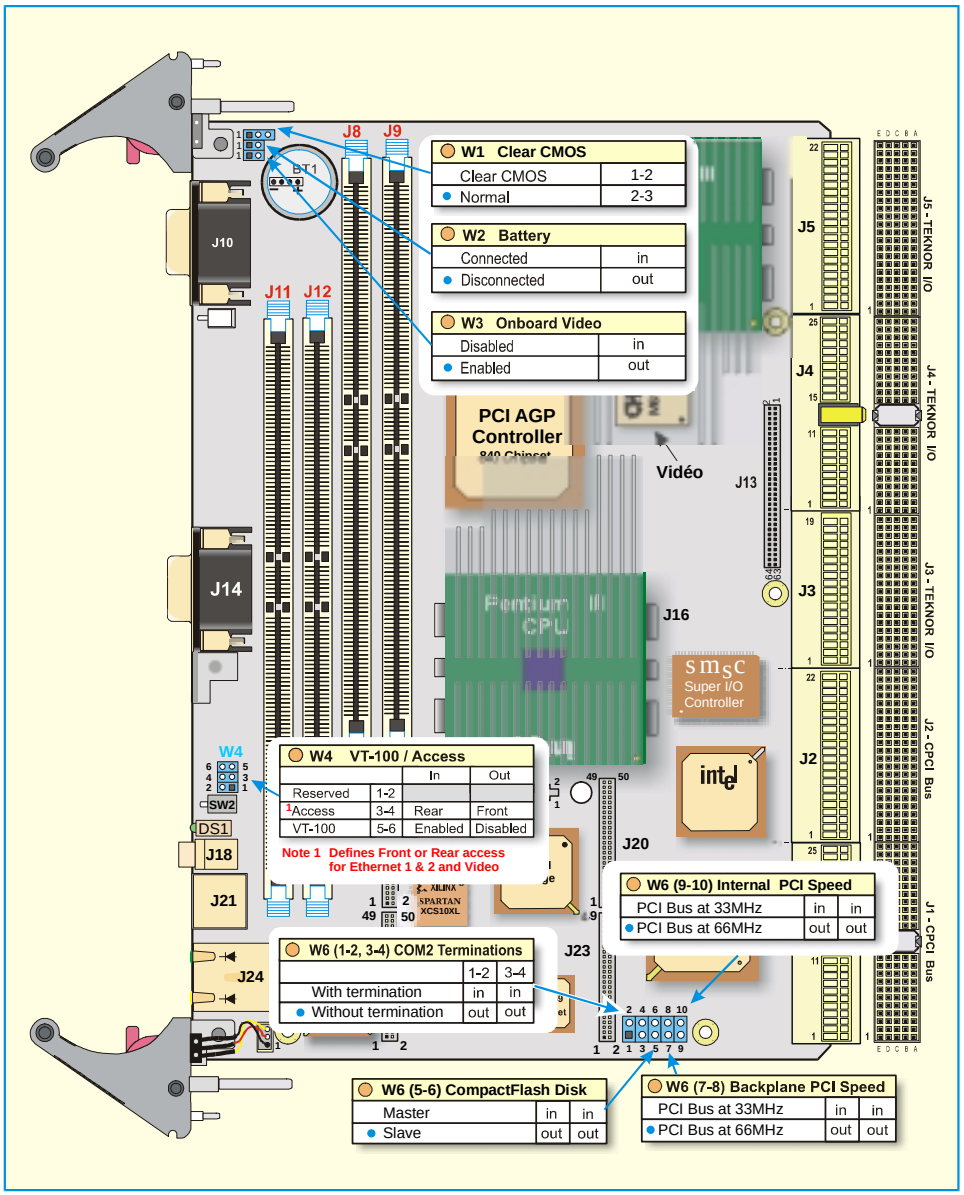
1. SETTING JUMPERS
2. REGISTER'S DESCRIPTION
3. ONBOARD INTERCONNECTIVITY
4. CUSTOMIZING THE BOARD
5. BUILDING A CPCI SYSTEM
6. CPCI I/O SIGNALS

3.1. SETTING JUMPERS

3.1.1. Jumper Description for the cPCI-DXS64

Description			
Clear CMOS	On position 1-2, all CMOS information is cleared. This jumper is set by default at position 2-3.		**W1**
Onboard Battery	Connects or Disconnects the battery to/from the board circuitry.		**W2**
Onboard Video	Use this jumper to disable the onboard video feature.		**W3**
Reserved	Jumper W4 (1-2) is reserved	**1-2**	**W4**
Access mode	Sets access, Front or Rear.	**3-4**	
Download Mode	When enabled, allows VT100 or ANSI terminal connection (data serial download from a remote computer).	**5-6**	
Serial Port B Termination	Use these jumpers to connect or disconnect the termination resistors on/from Serial Port C when set for RS-422/RS-485 operation mode 0.	**1-2** **3-4**	**W6**
CompactFlash Setting	Use this connector to setup the CompactFlash device in Master or Slave configuration.	**5-6**	
Backplane PCI Speed	This jumper sets the backplane PCI bus speed at 33 or 66MHz.	**7-8**	
Internal PCI Speed	This jumper sets the internal PCI bus speed at 33 or 66MHz.	**9-10**	

3.1.2. cPCI-DXS64 – Jumper Settings



3.2. REGISTER'S DESCRIPTION

3.2.1. Supervisor Registers

The Supervisor Registers consist of eight I/O registers that are used to configure and control the special features of the board, the Programmable Watchdog and the Power Fail Detection.

These registers are 8-bit wide and can be located at three different I/O base addresses: 190h.

This section includes a description of each I/O register and bit available for programming and configuring the CPCI-DXS64.

3.2.2. Register 190h: Serial port B configuration.

Bit	7	6	5	4	3	2	1	0
Reset				0	0	0		
Read				RS485	RS232	ST1		
Write				RS485	RS232	ST1		

Used by the BIOS, only during the POST.

Serial port B configuration/use

ST1 Enable RTS2 to be used as 485TX enable when in 485 mode (1: enable, 0: disable).

RS232 Enable RS-232 mode for serial port B (1: enable, 0: disable).

RS485 Enable RS-422/RS-485 mode for serial port B (1: enable, 0: disable).

> **NOTE**
>
> The RS232 and RS485 bits are initialized by the BIOS during POST (Power-On Self Test). If a modification of these bits is required, be aware that there is a hardware protection so that RS232 and RS485 buffers cannot be activated at the same time. This protection is provided at the register level. If you write to 90h register with bits 3 and 4 set, you will actually write 0 in both of these bits. This condition can be read back.

3.2.3. Register 191h: Reset History & CPU Fault

Bit	7	6	5	4	3	2	1	0
Reset								
Read	PBRES		WDO					
Write								

Used by the BIOS at runtime; do not write to this register.

Reset history

PBRES This bit is set when the reset button is pressed. It is cleared at power-up and when the bit CLRHIS* is "0" (see register 192h description).

WDO This bit is set when the watchdog produces a reset. It is cleared at power-up and when the bit CLRHIS* is "0" (see register 192h description).

* = Active low signal

3.2.4. Register 192h: Clearing Reset History & Lock for Watchdog

Bit	7	6	5	4	3	2	1	0
Reset						1		1
Read						LOCK		CLRHIS*
Write						LOCK		CLRHIS*

Not used by the BIOS.

Reset history

CLRHIS* A 0-1 pulse will clear all reset history bits (refer to the 191h register described previously). In normal operation, always keep the CLRHIS* bit to "1" otherwise the reset source will not be captured (the history latch are disabled when CLRHIS* is "0").

Programmable watchdog

LOCK When set, the state of the enable bit for the programmable watchdog (WDEN) cannot be changed.

* = Active low signal

3.2.5. Register 193h: Silicon ID Chip Interface, Local I²C, System Monitor Connector Interface

Bit	7	6	5	4	3	2	1	0
Reset	1	1	1		1		1	1
Read	APPFLT* (pin)	GPIO2 (pin)	GPIO1 (pin)		DCHIP (pin		SCL (pin)	SDA (pin)
Write	APPFLT* (reg)	GPIO2 (reg)	GPIO2 (reg)		DCHIP (reg.		SCL (reg.)	SDA (reg.)

* Not used by the BIOS.

Silicon ID chip

IDCHIP Used to read the onboard silicon serial number using the Dallas Semiconductor one-wire protocol.

User EEPROM

SCL/SDA Clock and data I²C link to user EEPROM.

General purpose I/O

GPIO1 & 2 General purpose I/O. +5V pull-up of 8.2K ohms is connected to each I/O.

Application Fault

APPFLT* Used to indicate an application fault. See the System monitor pinout in the Appendix D.

* = Active low signal

3.2.6. Register 194h & 195h

These registers are reserved.

3.2.7. Register 196h: Programmable Watchdog

Bit	7	6	5	4	3	2	1	0
Reset	0	1	1	1				
Read	WDEN	WDS2	WDS1	WDS0				
Write	WDEN	WDS2	WDS1	WDS0				

Not used by the BIOS, except when the Watchdog Option is enabled in BIOS SETUP and After POST is set.

WDEN When this bit is set, the programmable watchdog is enabled with the current timeout specified by WDS[2..0] (Refers to the dual-stage programmable watchdog description in section 3.6).
To avoid accidental deactivation of the watchdog, the bit WDEN is normally locked by the bit LOCK of register 192h (see register 192h description).

WDS[2..0] Timeout selection.

3.2.8. Register 197h: NMI sources & mask

Bit	7	6	5	4	3	2	1	0
Reset	0		0		0		0	
Read	BatFltEn	BatFlt	FanFltEn	FanFlt	ExtFltEn	ExtFlt	WdNmiEn	WdNmi
Write	BatFltEn		FanFltEn		ExtFltEn		WdNmiEn	

Not used by the BIOS.

WdNmi	Watchdog NMI: NMI from the Watchdog timeout.
WdNmiEn	Enable NMI from the Watchdog.
ExtFlt	External fault NMI: see System Monitor Connector in Appendix D. This 5V CMOS input is pulled-up to +5V by a 8.2K resistor.
ExtFltEn	Enable NMI from ExtFltEn.
FanFlt	External fan fault NMI: see System Monitor Connector in Appendix D. This 5V CMOS input is pulled-up to +5V by a 8.2K resistor.
FanFltEn	Enable NMI from FanFlt.
BatFlt	Battery Fault: NMI from power failure detection.
BatFltEn	Enable NMI from BatFlt.

All bits are active "1" regardless of the electrical state of the signal. Inversion is provided by the hardware when required. When an NMI source is enabled, the corresponding event is latched until the enable bit is cleared. When the enable bit is cleared, the status bit reflects the signal (not latched).

The NMI itself is generated through the IOCHK* signal. As a result, it can be monitored on the ISA backplane, and the NMI handler must reset the IOCHK* latch.

* = Active low signal



NOTE

When a watchdog NMI occurs, the CPU must trigger or disable the watchdog within 1ms or the watchdog will generate a master reset. Knowing that an NMI is the highest priority interrupt on the CPU, if the CPU cannot answer the NMI within 1ms then there is a major problem and the system must be reset. Normally, the CPU will answer the NMI and reinitialize the watchdog for the time it needs to shut down properly.

3.2.9. Supervision Features

3.2.9.1. Watchdog

The function of a watchdog is to reset the CPU board when the processor is unable to generate a trigger for longer than the watchdog timeout period. This feature is useful in embedded systems where human supervision is not required or impossible.

The CPCI-DXS64 provides a two-stage digital watchdog with a software programmable timeout period.

The watchdog can be enabled by software.

3.2.9.2. Dual-stage Watchdog

3.2.9.2.1. Enabling the Programmable Watchdog

To enable the programmable watchdog, first unlock the enable bit by clearing the lock bit in register 192h, then set the bit WDEN in register 196h and re-lock it by setting the lock bit in register 192h. The following is an example in C language.

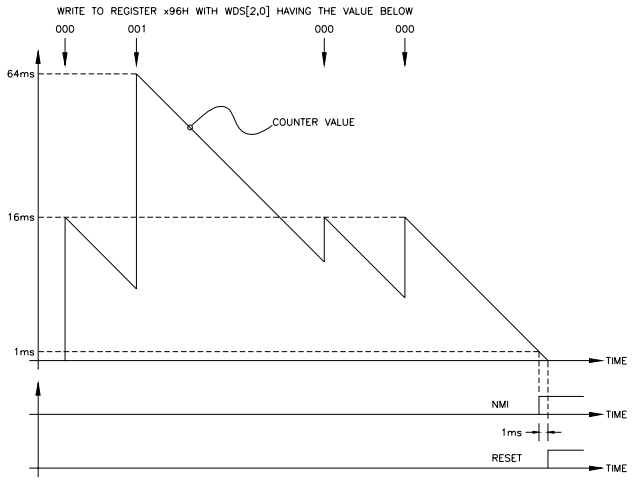
```
#define TekReg 0x190            // define base address (0x190, 0x290 or 0x390)

void ArmWatchdog(void)
{
   outp(TekReg+2,inp(TekReg+2) & 0xFB);  // unlock watchdog enable bit
   outp(TekReg+6,inp(TekReg+6) | 0xF0);  // enable & trigger at max timeout
   outp(TekReg+2,inp(TekReg+2) | 0x04);  // lock watchdog enable bit
}
```

3.2.9.2.2. Triggering the Programmable Watchdog

To trigger the programmable watchdog, the processor writes to register 196h. The result of writing to the register is the trigger and the value written to the register telling the watchdog the current timeout to use (see register 196h description). For a fixed timeout, the processor simply writes a constant in register 196h.

A variable refresh is possible as shown below:



The programmable watchdog can be viewed as a decrementing counter that is initialized by a write to register 196h. The processor must initialize the counter to prevent it from reaching count 0 (timeout).

The following C language function can be used to trigger the programmable watchdog.

```
#define TekReg 0x190              // define base address (0x190, 0x290 or 0x390)
void TrigWatchdog(timeout)        // select timeout at runtime: 0x80, 0x90, 0xA0, ... 0xF0
{
   outp(TekReg+6,(inp(TekReg+6) & 0x0F) | (timeout & 0xF0));
}
```

3.2.9.2.3. Timeout

The programmable watchdog has two stages: the first stage has a variable timeout while the second stage has a fixed one.

The first stage timeout is chosen at runtime from eight preset values (see table below). The first stage timeout generates an NMI interrupt (if enabled in register 197h). An appropriate NMI handler must be written, otherwise this will be treated as a parity error by the default BIOS NMI handler (see register 197h description for a suggestion on how to do this).

The second stage times-out 1ms after the first one and generates a master reset.

WDS[2,0]	NMI Timeout	RESET Timeout
000	15ms	0.015s + 8.06ms
001	62.5ms	0.0625s + 8.06ms
010	250ms	0.250s + 8.06ms
011	1s	1s+ 8.06ms
100	4s	4s + 8.06ms
101	16s	16s + 8.06ms
110	64s	64s + 8.06ms
111	256s	256 + 8.06ms

When the NMI is enabled, if the processor is still running and memory content is not corrupted, the processor can answer the NMI and trigger the watchdog again to gain time for a graceful shutdown.

A reset from the programmable watchdog is latched for reset source identification; refer to the 192h register description in Section 3.2.4.

3.2.9.3. Power Failure Detection

The board has many power failure detection features (* = active low signal):

It always monitors the +12V, +5V, +3.3V, +2.5V and V_{CORE} power supply voltages. When one of these voltages drops below a typical threshold value, the system is reset.

It can monitor the onboard battery. Jumper W3 must be shorted to connect the onboard battery. When the battery is in a low condition (below 2.9V typical), the BatFlt bit at I/O address 197h, will read 1 (197h, bit 6: 1 = failed, 0 = good). To generate an NMI (non-maskable interrupt) when the battery fails, the BatFltEn bit must contain a 1 (197h, bit 7: 1 = enable NMI, 0 = disable NMI). The interrupt can then be serviced by an interrupt handler. If you choose not to generate an NMI, you can still use an algorithm to detect a low battery condition at 197h, bit 6, and respond accordingly.

It can monitor an offboard 3.6V battery. Jumper W3 must be shorted to connect the offboard battery.

3.2.10. Reset History

Following a reset, the application software can read the register 191h and examine the bits PBRES and WDO. Based on the values of those bits, the following conclusions can be drawn about the reset source.

PBRES	WDO	RESET Source
0	0	Power-up, Ctrl-Alt-Del or software runaway
1	0	Reset switch or remote reset
0	1	Programmable watchdog
1	1	Watchdog and a reset switch.

For proper operation, the bit CLRHIS* of register 192h should be pulsed (0-1) immediately after reading the history bits.

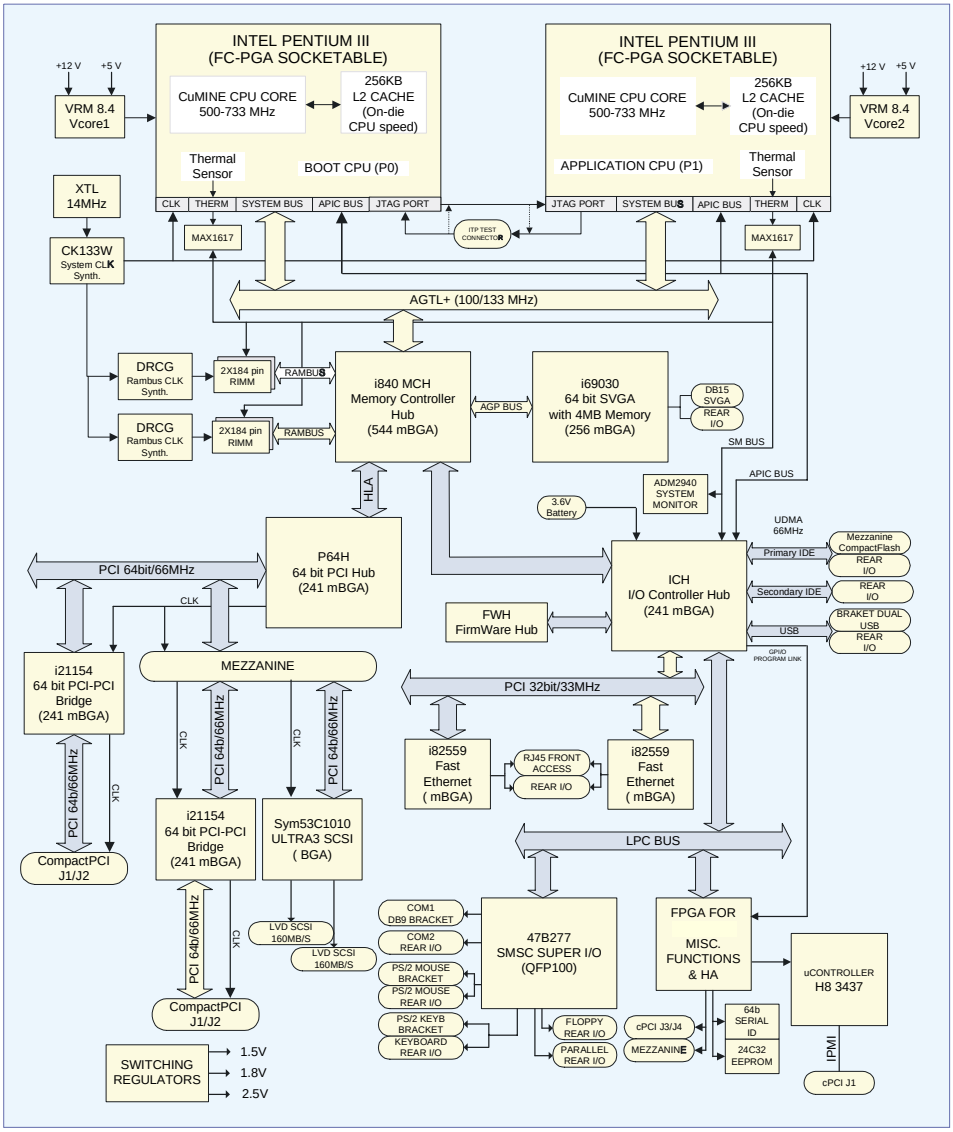
3.2.11. Register BITs description (summary)

Address	CPLD	D7	D6	D5	D4	D3	D2	D1	D0
190*	READ	NU			RS485	RS232	ST1	NU	
	WRITE								
191*	READ	PBRST	NU	WDO	NU				PFO
	WRITE	NU		NU					NU
192*	READ	NU					WD_LOCK	NU	_CLRHIS
	WRITE								
193*	READ	NU				IDCHIP	NU	I2C_CLK	I2C_DATA
	WRITE								
194*	READ	_CND3	CIS3_1	CIS3_0	CBAS3_1	CBAS3_0	RESERVED		
	WRITE								
195*	READ	_CND4	CIS4_1	CIS4_0	CBAS4_1	CBAS4_0	NU		RESERV.
	WRITE								NU
196*	READ	WDEN	WDD2	WDD1	WDD0	NU			
	WRITE								
197*	READ	BATFEN	BATFLT	NU				WDNMIEN	WDNMI
	WRITE		NU						NU
198*	READ	RESERVED							
	WRITE								
199*	READ	RESERVED							
	WRITE								
19A*	READ	NU	RESERVED						
	WRITE		NU						
19B*	READ	NU			RESERVED				
	WRITE				NU				

The base address for the Supervisor I/O Register, which is used for such functions as power fail detection and the watchdog timer can be set to 190h, 290h, and 390h (see *Chipset Features Setup*).

3.3. ONBOARD INTERCONNECTIVITY

3.3.1. cPCI-DXS64 Block Diagram



3.3.2. Pentium® III processor

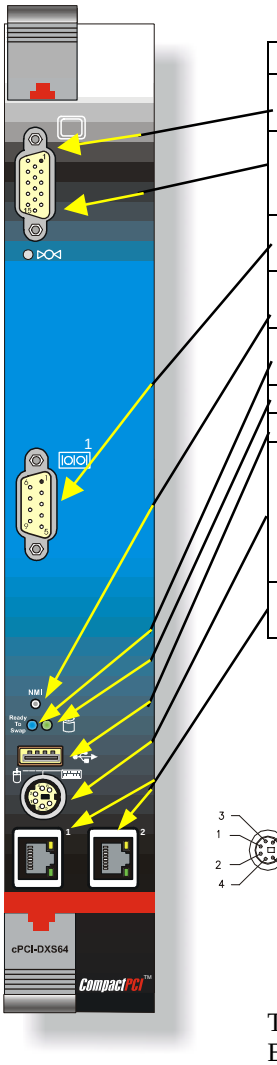
The cPCI-DXS64 system board supports the Intel's 600, 700 and 850MHz Pentium III processor (Higher clock speeds will be available when Intel will release the corresponding parts).

It consists of a Pentium® III processor core with an integrated second level cache of 256KB (on-die, full CPU speed, ECC capable) and a 64-bit high performance 100MHz front side bus The processor interfaces to the 840BX AGPset through the 64-bit low power GTL + data bus interface.

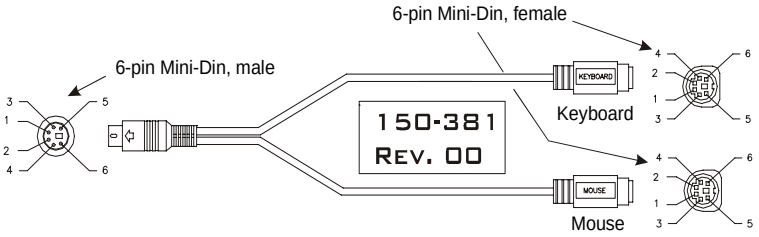
3.3.3. Onboard Connectors and Headers

Description	Connector	Comments
CompactPCI Bus	J1/J2	J1- CPCI bus signals and power. J2 – Additional system slot signals.
CompactPCI I/O	J3	Serial Ports B/C/D, Ethernet 1, power.
CompactPCI I/O	J4/J5	Supports PS/2 mouse, serial ports A and B, first IDE channel, parallel port, keyboard, speaker, floppy disk, reset, USB, SMBus, and power signals.
Processor Socket	J6, J16	PGA370 Sockets supporting Pentium III processors.
N/u	J7, J15	Not used.
RIMM Sockets	J8, J9, J11, J12	Four 184-pin latching RIMM sockets. Up to 2 GB of DRAM with parity or ECC (for single bit error correction and multiple bit error detection).
VGA	J10	Supports standard 15-pin DSUB female connector.
Storage Mezzanine	J13, J19	This mezzanine supports 1 hard drive EIDE HA and 1 Ethernet (RJ45).
Serial Port A	J14	Supports standard 9-pin DSUB male connector.
CompactFlash	J17	Supports the Kontron's module dedicated to CompactFlash disks.
USB	J18	USB connector located on the faceplate.
PMC	J19, J22	The PCI Mezzanine Card (PMC) connectors support one standard PMC device.
Mezzanine	J20, J23	64-bit/66MHz Mezzanine.
Keyboard/Mouse	J21	Keyboard signals (6-pin DSUB female connector).
Ethernet 1	J24	RJ-45 connector with built-in activity and link indicators.
Hot Swap	J25	Hot Swap Switch.
Battery	BT1	CMOS backup battery connector.

3.3.4. Front Plate Connectors and Indicators

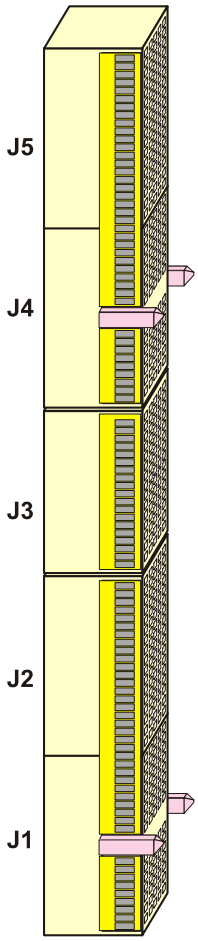


Name	Description	Comments
J10	Video Connector	Standard 15-pin DSUB female connector
S1	Reset Button	Use a small tool to press the button and proceed to a hardware reset of the board
J14	Com Port 1	Standard 9-pin DSUB male connector
SW2	NMI	This switch generates an NMI interrupt when pressed
Blue LED	Ready to Swap	Lights when the board is ready to be swapped.
Green LED	HDD Activity	Indicates an activity on IDE
J18	USB	Standard 4-pin USB connector
J21	PS/2 Mouse and Keyboard	To connect a keyboard and/or a mouse through this connector, you need a Y shaped splitter cable (Kontron part number 150-381)
J24	Ethernet 1 and 2	RJ-45 connectors with built-in activity and link indicators



The front plate supports a PMC cutout and a cap that also act as an EMI shield when there are no PMC device installed.

3.3.5. CompactPCI Connectors



- **CPCI J5 Connector**

  Supports PS/2 mouse, serial ports A and C, primary IDE channel, parallel port, keyboard, speaker, floppy disk, reset, USB, SMBus and power signals.

- **CPCI J4 Connector**

  Supports Ethernet1, secondary IDE channel, SCSI, VGA, and power signals.

- **CPCI J3 Connector**

  Supports serial ports B, C, and D, V-Port, Ethernet1, and power signals.

- **CPCI J2 Connector**

  Supports additional system slot signals, PCI 64-Bit extension, and power.

- **CPCI J1 Connector**

  Supports CPCI bus signals, and power.

3.4. CUSTOMIZING THE BOARD

3.4.1. Processor and Fan

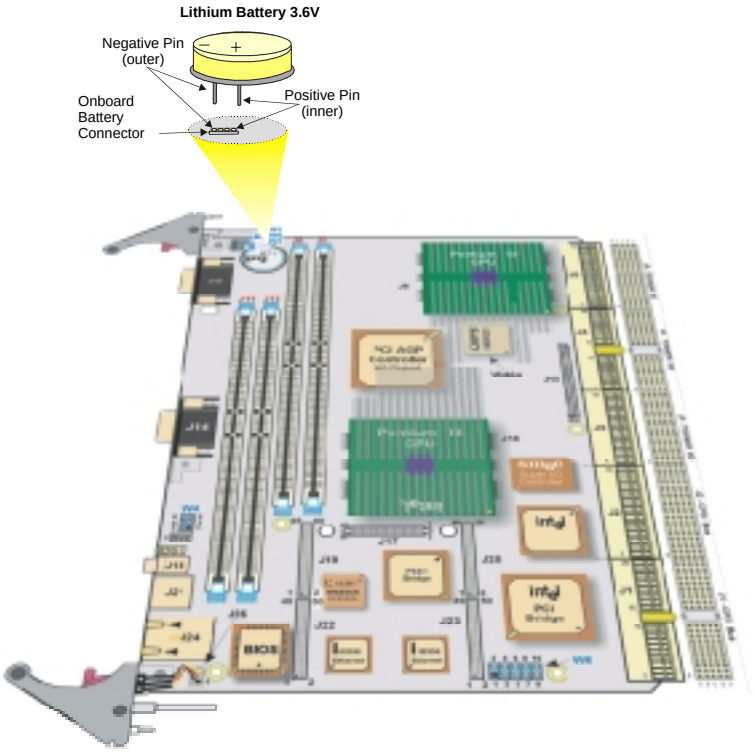
Your board will be installed with Pentium III processors and their adequate cooling system.

> **CAUTION**
>
> Since CPUs are very sensitive components, particular attention should be given while installing a processor on the board. Improper installation may damage the board and/or the CPU
>
> Before installing a processor on your board, **you must contact our technical support** for the installation procedure

3.4.2. Backup Battery

An onboard 3.6V lithium battery is provided to backup BIOS setup values and the real time lock (RTC).

When replacing, the battery must be connected as follows:



WARNING

Danger of explosion if battery is incorrectly replaced

Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions. When you receive a board, remove the **onboard battery jumper** to enable the battery (See section 3 for jumper settings)

3.4.3. Memory

The board supports 256MB or 1GB of 64/72-bit Rambus DRAM (RDRAM) divided into four RIMM sockets (J8, J9, J11 and J12). The minimum configuration is 128MB (2 X 64MB)

> **NOTE**
>
> All memory sockets must be populated for proper operation. If a memory bank is not used, it should be populated with a memory continuity module.

Related Jumpers
None

BIOS Setups
See 4.1.2.4 – *Phoenix Setup Program, Advanced, Advanced Chipset Control*

For the latest list of tested RIMMs devices please consult our FTP site at :

ftp://ftp.kontron.ca/Support/Product_Memory_AVL_Approved%20Vendor%20List/

> **NOTE**
>
> The total size of the system memory available on the board is equal to the sum of the memory module sizes installed in the RIMM sockets.

The RDRAM RIMMs must conform to the following:

- 2.5V only, single-sided or double-sided
- (PC-600) RDRAM
- Serial Presence Detect (SPD) EEPROM
- 64-bit and 72-bit RIMMs
- Error Checking and Correction (ECC) or parity bit, with 72-bit RIMMs.

Installation

- On an anti-static plane, place the board so that you are facing the RIMM sockets (the edge bracket must be located on the right).
- Insert the RIMM into the socket, aligning the notches on the module with the socket's key inserts.
- Push vertically the RIMM into the socket until the retaining clips on each side snap on. Repeat these steps to populate the other sockets.

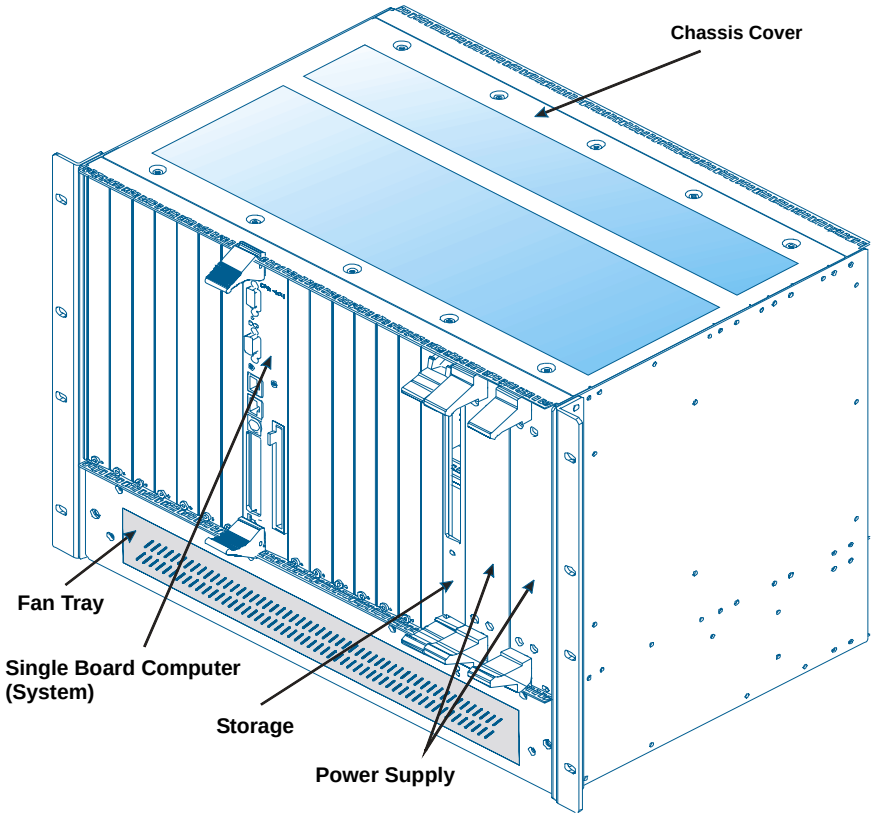
To remove a RIMM from a socket, push down the retaining clips on each side of the socket, to release the module. Pull the module upward to remove.

3.5. BUILDING A CPCI SYSTEM

When building a CompactPCI system, a minimum requirement consists in a chassis, a CompactPCI backplane, a storage module, a power supply unit, and a ventilation system.

The main AC power is drawn to the chassis components through an IEC power plug with a 2-stage filter, fuse holder and power switch. All power features are provided at the rear of the chassis.

The chassis may be used either as a desktop system or a rack-mount bay.



CxP0816

3.5.1. Backplane

An entry-level backplane is provided by Kontron. It is referred to as cBP-08R. It features 8 CPCI slots (one PCI I/O segment), and includes J3-J5 I/O connectors on all slots.

A 16-CPCI-slot backplane (cBP-16R) is also available from Kontron. It supports two PCI I/O segment: one is driven directly by the system processor while the other is managed through a PCI-to-PCI bridge implemented on the cMCB-2RC mezzanine card (Storage/PCI-to-PCI mezzanine).

All Kontron's CompactPCI backplanes feature pass-through connectors (J3-J5) to support Rear Panel I/O connections.

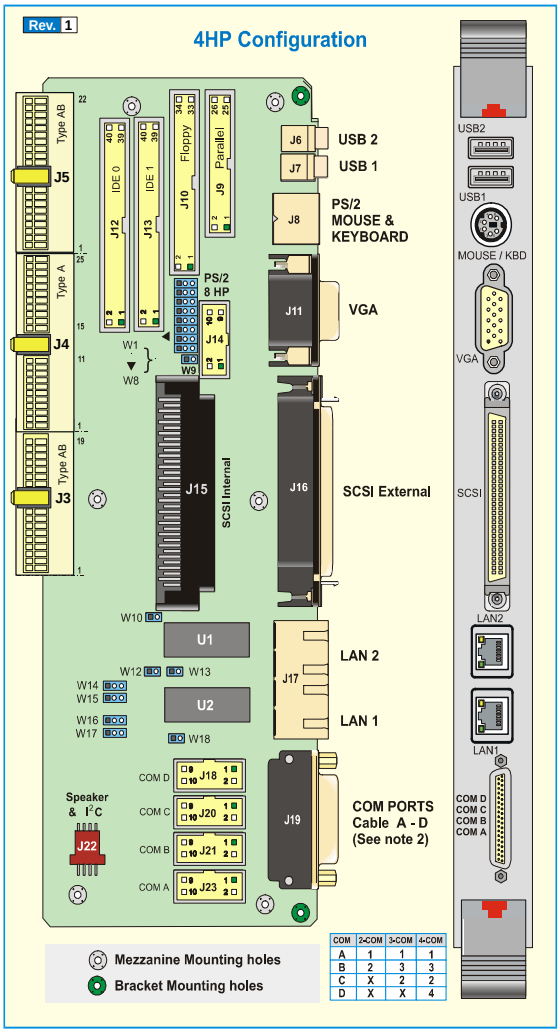
IMPORTANT

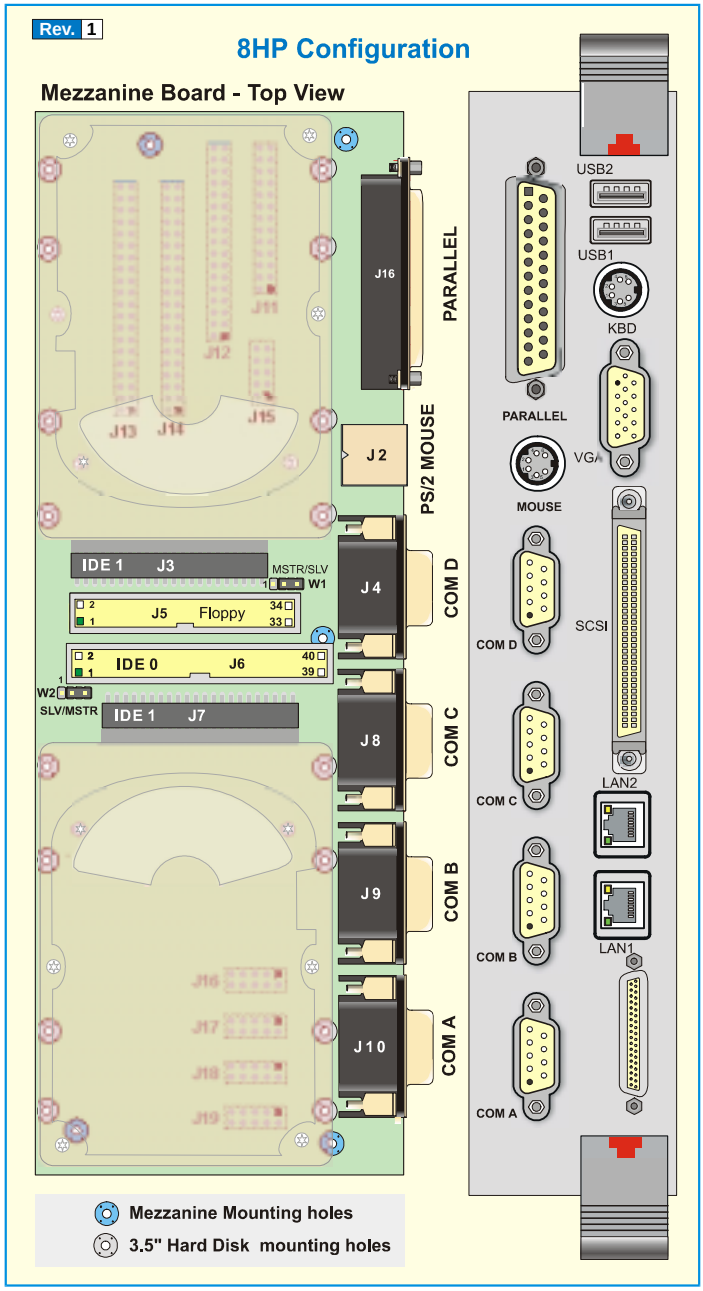
J1 and J2 are de-facto industry standard as defined by PICMG. J3, J4 and J5 are user-defined connectors and will vary from various manufacturers. Contact our Technical Support to verify pinout compatibility with other chassis backplane vendors.

3.5.2. Rear-Panel I/O

This feature is intended to issue the I/O capabilities of the system processor to the rear of the enclosure using a Rear I/O Transition module (cTM80-STD2S).

The Rear I/O Transition module gathers all the I/O signals of the CPU board and makes them easily accessible through standard headers and connectors located at the rear of enclosure. The cTM80-STD Transition Module is illustrated below.




Rev. 1
8HP Configuration
Mezzanine Board - Top View
J16
PARALLEL
J2
PS/2 MOUSE
J4
COM D
J8
COM C
J9
COM B
J10
COM A
IDE 1 J3
MSTR/SLV
W1
J5 Floppy
IDE 0 J6
W2
SLV/MSTR
IDE 1 J7
USB2
USB1
KBD
PARALLEL
VGA
MOUSE
COM D
SCSI
COM C
LAN2
COM B
LAN1
COM A
Mezzanine Mounting holes
3.5" Hard Disk mounting holes

3.5.3. Storage Devices

A mezzanine card attaches directly to the system processor. 6U form factor storage modules are supported when using the cBP-08R backplane.

There are two ways of supplying data storage with Kontron's product line.

1. On board Mezzanine Card that is installed directly onto the processor board.
2. cSM-DVD : 6U form factor storage module that is front loaded into the CxP0816 chassis.

3.5.4. Power Supply

6U power supply modules featuring load sharing redundant mode and hot-swap capabilities allow on-site replacements of defective module while the system remains powered.

A standard ATX power supply unit is also supported.

3.5.5. Fan Tray

The ventilation unit of the enclosure conforms to the global requirement of the system in fully loaded configuration.

3.5.6. Installing the Board into a Bay

The cPCI-DXS64 is mechanical Eurocard form factor boards. It takes advantages of the IEEE1101.10 specifications that ensure a mechanical interchange capability between different plug-in elements in sub-racks.

Due to the high-density pinout of the Hard Metric connector, some precautions must be taken when connecting or disconnecting a board to/from a backplane:

1. Rail guides must be installed on the enclosure to slide the board to the backplane.
2. Do not use force if there is any mechanical resistance while inserting the board.
3. Screw the front plate to the enclosure to firmly attach the board to its enclosure.
4. Use the extractor handles to disconnect and extract the board from its enclosure.

3.5.7. Connector Keying

CompactPCI connector support guide lugs to ensure a correct polarized mating. A proper mating is enhanced by the use of color coded keys for 3.3V and 5V operation.

Color coded keys prevent inadvertent installation of a 5V peripheral/system board in a 3.3V slot. The cPCI-DXS64 is 3.3v only to support 66Mhz pci bus. It does support Yellow coding key. The PCI bus require to be keyed. Backplane connectors must always be keyed according to the signaling (VIO) level.
Coding Key Colors are defined as follows:

Signaling Voltage	Key Color
3.3V	Cadmium Yellow
5V	Brilliant Blue
Universal board (5V and 3.3V)	none
-48V	Red

3.5.8. Bus Mastering

The cPCI-DXS64 provides seven pairs of REQ/GNT (0-6) arbitration signals through the Secondary PCI bus. This means the board is capable of driving up to seven CPCI slots with PCI Bus Master capabilities.

3.5.9. Connection

To install the cPCI-DXS64 board into a bay, proceed as follows:

1. Locate the 6U system slot
2. Remove the front plate of the slot where you intend to insert the cPCI-DXS64.
3. Ensure the module is properly aligned with the guide-rails and slide it gently until it touches the backplane connector

WARNING

1. Some mechanical parts of the guide-rail are fragile (shield contacts and clips). Do not use force to insert and connect a CompactPCI module.

2. If there is any mechanical resistance while you insert a module, first ensure there is no mechanical obstacle and check for the alignment of all parts.

4. To engage the board's connectors into the backplane connector, press simultaneously on the front plate.
5. Fasten the module using the fellow-plate fixing screw to secure the module to the system chassis.

To remove the module from the chassis, proceed as follows:

1. Remove the front plate fixing screws.
2. Press the handle to act as a lever to disengage the CompactPCI connector from the backplane.
3. Pull on the handle and gently remove the board.

3.6. CPCI I/O SIGNALS

This section describes integrated feature signals available on rear panel CPCI I/O connectors (J3, J4, and J5)

3.6.1. J3 Signal Specification

3.6.1.1. Ethernet LEDS

Signal	Pin Assignation	Description
SPEEDLED 0-1	A6, E6	Speed LED signal
LINKLED 0-1	B6, D6	Link integrity LED signal
ACTLED 0-1	C6, A7	Transmit / receive activity LED signal

3.6.1.2. Ethernet 1

Signal	Pin Assignation	Description
ETX+1	A9	Ethernet 1 High Transmit Data line
ETX-1	B9	Ethernet 1 Low Transmit Data line
ERX+1	C9	Ethernet 1 High Receive Data line
ERX-1	D9	Ethernet 1 Low Receive Data line

3.6.1.3. Serial Port C

Signal	Pin Assignation	Description
DCD3#	A13	Data Carrier Detect
RXD3	C13	Receive Data
DSR3#	D13	Data Set Ready
TXD3	E13	Transmit Data
RTS3#	A14	Ready To Send
CTS3#	B14	Clear To Send
RI3#	C14	Ring Indicator
DTR3#	E14	Data Terminal Ready

3.6.1.4. Serial Port D

Signal	Pin Assignation	Description
DCD4#	A11	Data Carrier Detect
RXD4	C11	Receive Data
DSR4#	D11	Data Set Ready
TXD4	E11	Transmit Data
RTS4#	A12	Ready To Send
CTS4#	B12	Clear To Send
RI4#	C12	Ring Indicator
DTR4#	E12	Data Terminal Ready

3.6.1.5. IDE LED Signals.

Signal	Pin Assignation	Description
EXT_SIDEACT#	B18	Secondary IDE activity
HD_ACT#	C18	Primary IDE activity

3.6.1.6. IR Serial Port B

Signal	Pin Assignation	Description
COM2_IRRX	D18	IR receive data line (Serial Port B)
COM2_IRTX	E18	IR transmit data line (Serial Port B)

3.6.1.7. Hot Swap HA (High Availability) signals

Signal	Pin Assignation	Description
BDSEL# S2-S5	A15, B15, E15, D19	Board Select, one of the shortest pins (the last to mate and the first to break contact).
HEALTHY# S2-S4	A16, B16, D17	Used to acknowledge the health of the board
PCIRST S2-S4	A17, C15, E17	Used to indicate the CompactPCI Bus reset signal

3.6.2. J4 Signal Specification

3.6.2.1. Power Management

Signal	Pin Assignation	Description
I2C-CLK	A1	I2C clock signal
I2C-DATA	B1	I2C data signal
LID	C1	Reserved
EXT-FAN0-FAIL#	D1	Enclosure fan 0 fail
EXT-FAN1-FAIL#	E1	Enclosure fan 1 fail
SM-BYPASS#	A2	Reserved

3.6.2.2. SCSI Interface

Signal	Pin Assignation	Description
SD - 0-15	E7, D7, C7, B7, A7, E6, D6, C6, E2, D2, C2, B2, E8, D8, C8, B8	SCSI Data – The SCSI data lines drive the ID during arbitration and selection, and command and data information as well as status and messages.
SIO -	A3	In/Out – Indicates the In direction when asserted and the Out direction when not asserted.
SREQ -	B3	Request – A target will assert REQ to indicate a byte is ready or is needed by the Target.
SCD -	C3	Command/Data – Indicates Command or message phase when asserted, and Data phase when not asserted.
SSEL -	D3	SCSI Select – The line is driven after a successful arbitration to select as an initiator or reselect as a target and otherwise it is received.
SMSG -	E3	SCSI Message - Indicates a Message phase when asserted, and Command or Data phase when not asserted.
RST -	A4	Reset – Signal is interpreted as a hard reset and will clear all commands pending on the SCSI bus.

SCSI Interface

SACK -	B4	Acknowledge – Indicate a byte is ready for or was received from the Target.
SBSY -	C4	Busy – Handshake signal used during arbitration.
SATN -	E4	Attention – This line is activated when a special condition occurs.
WIDEPS –	B5 (not connected)	Wide Present – When Low, indicates that a wide (16-bit) cable is present.
TERMPWR	C5, D5	Termination Power.
SDP1 - , SDP0 -	A8, B6	SCSI High/Low Parity – Provide odd parity for data lines.

3.6.2.3. Video Interface

Signal	Pin Assignation	Description
VSDA	D9	Video serial data line (video I2C)
VSCL	A10	Video serial clock line (video I2C)
HSYNC	B10	Horizontal sync line
VSYNC	C10	Vertical sync line
RED	D10	Analog Red video signal
GREEN	E10	Analog Green video signal
BLUE	A11	Analog Blue video signal

3.6.2.4. Ethernet 0 Interface

Signal	Pin Assignation	Description
ETX+0	A16	Ethernet 0 High Transmit Data line
ETX-0	B16	Ethernet 0 Low Transmit Data line
ERX+0	C16	Ethernet 0 High Receive Data line
ERX-0	D16	Ethernet 0 Low Receive Data line

3.6.2.5. Hot Swap HA (High Availability) signals

Signal	Pin Assignation	Description
BDSEL# S6-S8	C11, E20, B25	Board Select, one of the shortest pins (the last to mate and the first to break contact).
HEALTHY# S5-S8	C9, D15, C22, C25	Used to acknowledge the health of the board
PCIRST# S5-S8	E9, E15, A25, D25	Used to indicate the CompactPCI Bus reset signal

3.6.2.6. IDE 1 Interface

Signal	Pin Assignation	Description
IDE1_RST#	A17	Reset signal
SDD 0-15	B20, E19, C19, A19, D18, B18, E17, C17, D17, A18, C18, E18, B19, D19, A20, C20	Sec. Disk Data – These signals are used to transfer data to or from the IDE device.
SDREQ	A21	Sec. Disk DMA Request - This signal is directly driven from the IDE device DMARQ signal. It is asserted by the IDE device to request a data transfer.
SDIOW#	C21	Sec. Disk I/O Write – In normal IDE mode, this is the command to the IDE device that it may latch data from SDD lines.
SDIOR#	E21	Sec. Disk I/O Read – In normal IDE mode, this is the command to the IDE device that it may drive data on SDD lines.
SIORDY	B22	Sec. I/O Channel Ready – In normal mode, this input signal is driven directly by the corresponding IDE device IORDY signal.
SDDACK#	D22	Sec. DMA Acknowledge – This signal directly drives the IDE device /DMACK signal. It is asserted to indicate to IDE DMA slave devices that a given data transfer cycle is a DMA data transfer cycle.
IRQ15	E22	IRQ15 line
IOCS16#	A23	Not connected
SDA 0-2	D23, B23, E23	Sec. Disk Address – These signals indicates which byte in either the ATA command block or control block is being addressed.
SCS1#, SCS3#	A24, B24	Secondary Chip Select - For ATA control register.
SD14+	C24	SCSI Data – The SCSI data lines drive the ID during arbitration and selection, and command and data information as well as status and messages.
IDE1_SDIAG#	D7 **(on J5)**	Secondary Diagnostic
Reserved	E24	Reserved

IDE 1 (IDE 1) is assigned to the Secondary IDE logical interface. It supports directly two IDE devices configured as master and slave devices.

3.6.3. J5 Signal Specification

3.6.3.1. IDE 0 Interface

Signal	Pin Assignation	Description
IDE0_RST#	A1	IDE0 Reset line
IDE0_RST#	B1	IDE0 Reset line
PDD 0-15	B4, E3, C3, A3, D2, B2, E1, C1, D1, A2, C2, E2, B3, D3, A4, D4	Prim. Disk Data – These signals are used to transfer data to or from the IDE device.
PDREQ	A5	Prim. Disk DMA Request - This signal is directly driven from the IDE device DMARQ signal. It is asserted by the IDE device to request a data transfer.
PDIOW#	C5	Prim. Disk I/O Write – In normal IDE mode, this is the command to the IDE device that it may latch data from SDD lines.
PDIOR#	E5	Prim. Disk I/O Read – In normal IDE mode, this is the command to the IDE device that it may drive data on SDD lines.
PIORDY	B5	Prim. I/O Channel Ready – In normal mode, this input signal is driven directly by the corresponding IDE device IORDY signal.
PDDACK#	D5	Prim. DMA Acknowledge – This signal directly drives the IDE device /DMACK signal. It is asserted to indicate to IDE DMA slave devices that a given data transfer cycle is a DMA data transfer cycle.
IRQ14	E4	IRQ14 line
Reserved	A6	Reserved
PDA 0-2	D6, C7, E6	Prim. Disk Address – These signals indicates which byte in either the ATA command block or control block is being addressed.
PCS1#, PCS3#	A7, B7	Primary Chip Select
PDIAG#	C6	Pass Diagnostic

3.6.3.2. USB 0 and 1 Interfaces

Signal	Pin Assignation	Description
USBD1-0 (+/-)	B18, C18, D19, E19	USB Data – Differential data path for USB 0 and 1 ports
USBG 1-0	B19, D18	USB Ground – Differential ground reference for USB 0 and 1 ports
USBV 1-0	C19, E18	USB Voltage – Differential power level for USB 0 and 1 ports

3.6.3.3. Floppy Disk Interface

Signal	Pin Assignation	Description
FD-DRVEN 0-1#	E7, A8	Drive 0-1 density select
FD-INDEX#	B8	Index
FD-MTR 0-1#	C8, A9	Motor 0-1 enable
FD-DS 0-1#	E8, D8	Drive 0-1 select
FD-DIR#	B9	Direction
FD-STEP#	C9	Step pulse
FD-WDATA#	D9	Write disk data
FD-WGATE#	E9	Write gate
FD-TRK0#	A10	Track 0
FD-WRTPRT#	B10	Write protected
FD-RDATA#	C10	Read disk data
FD-HDSEL#	D10	Head select
FD-DSKCHG#	E10	Disk change

3.6.3.4. Serial Port A

Signal	Pin Assignation	Description
DCD1#	A13	Data Carrier Detect
RXD1	C13	Receive Data
DSR1#	D13	Data Set Ready
TXD1	E13	Transmit Data
RTS1#	A14	Ready To Send
CTS1#	B14	Clear To Send
RI1#	C14	Ring Indicator
DTR1#	E14	Data Terminal Ready

3.6.3.5. Serial Port B

Signal	Pin Assignation	Description
DCD2#	A11	Data Carrier Detect
RXD2	C11	Receive Data
DSR2#	D11	Data Set Ready
TXD2	E11	Transmit Data
RTS2#	A12	Ready To Send
CTS2#	B12	Clear To Send
RI2#	C12	Ring Indicator
DTR2#	E12	Data Terminal Ready

3.6.3.6. Parallel Port

Signal	Pin Assignation	Description
SLCT	A15	Printer select
PE	B15	Paper end
BUSY	C15	Busy signal
ACK#	D15	Acknowledge handshake
PD 0-7	E17, C17, A17, D16, C16, B16, A16, E15	Parallel port data bus
SLCTIN#	E16	Printer select
ALF	A18	Auto line feed
INIT#	B17	Initiate output
ERR#	D17	Error at printer
STB#	A19	Strobe signal

3.6.3.7. Miscellaneous Signals

Signal	Pin Assignation	Description
SMBDATA#	B20	Onboard SMbus data
SMBALERT#	C20	Onboard SMbus Alert (CPU overheating)
SMBCLK	E20	Onboard SMbus Clock
PBRST#	A22	Reset
DIAG-OC#	C22	Reserved
SPK-OUT	E22	Speaker signal

3.6.3.8. Keyboard Interface

Signal	Pin Assignation	Description
KDATA	A21	Keyboard data
KCLK	B21	Keyboard clock
VCC-KBD	C21	Keyboard power

3.6.3.9. Mouse Interface

Signal	Pin Assignation	Description
MDATA	D21	Mouse data
MCLK	E21	Mouse clock

PART 4

4. SOFTWARE SETUP

1. PHOENIX BIOS SETUP PROGRAM
2. BOOT UTILITIES
3. INSTALLING DRIVERS

4.1. PHOENIX BIOS SETUP PROGRAM

All relevant information for operating the board and connected peripherals is stored in the CMOS memory. A battery-backed up memory holds this information when the board is powered off, the BIOS Setup program is required to make changes to the setup.

NOTES

Make sure you setup the BIOS Setup software prior to installing your operating system and your drivers.

For systems that need the BIOS to first attempt to boot from LAN, follow these steps:

1. Set the "Network Boot" or "Landesk Service Agent II" as the first boot service in the BIOS setup (Boot Menu Selection).

2. Follow the complete procedure in the Boot from LAN utility CDROM.

4.1.1. Accessing the BIOS setup program

The system BIOS (Basic Input Output System) provides an interface between the operating system and the hardware of the cPCI-DXS64 System processor. This board uses the Phoenix Setup program, a setup utility in flash memory that is accessed by pressing the <DELETE> key at the appropriate time during system boot. This utility is used to set configuration data in CMOS RAM.

CAUTION

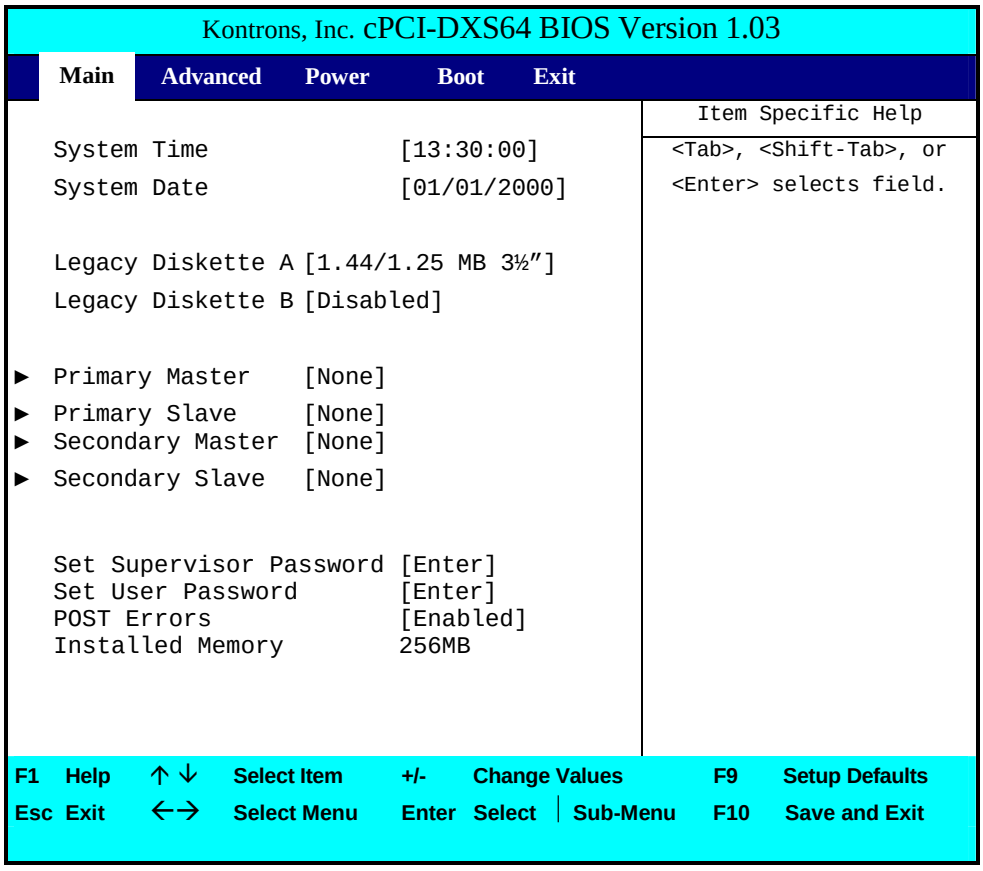
Before modifying CMOS setup parameters, ensure that the W2 battery selection jumper is installed to enable the CMOS battery back up (please refer to Section 3.1).

To run the Phoenix Setup program incorporated in the ROM BIOS:

- Turn on or reboot the system.
- When you get the following message, hit <DELETE> key to enter SETUP

```
PhoenixBIOS 4.0 Release 6.0
Copyright 1985-2000 Phoenix Technologies Ltd.
All Rights Reserved
KONTRONS INC cPCI-DXS64 BIOS Version 1.4
```

The main menu of the Phoenix BIOS CMOS Setup Utility appears on the screen.



Whenever you are not sure about a certain setting, you may refer to the list of default values. The list of defaults is provided in the event that a value has been changed and one wishes to set this option to its original value. Loading the SETUP defaults will affect all the options in this screen (or all parameters if defaults are loaded from the Main Menu) and will reset options previously altered.

The BIOS Default values provide **optimum performance** settings for all devices and system features.

> **CAUTION**
>
> These parameters have been provided to give control over the system. However, the values for these options should be changed only if the user has a full understanding of the timing relationships involved.

4.1.2. The Menu Bar

The Menu Bar at the top of the window lists these selections:

Menu selection	Description
Main	Use this menu for basic system configuration
Advanced	Use this menu to set the Advanced Features available on your system's chipset.
Power	Use this menu to configure Power Management features
Boot	Use this menu to determine the booting device.
Exit	Exits the current menu.

Use the left and right ← and → arrows keys to make a selection.

4.1.2.1. The Legend Bar

Use the keys listed in the legend bar on the bottom to make your selections or exit the current menu. The chart on the following page describes the legend keys and their alternates:

Key	Function
<F1> or <Alt-H>	General Help windows (see 4.1.2.2)
<Esc>	Exit this menu.
← → arrow keys	Select a different menu
<Tab> or <Shift-Tab>	Cycle cursor up and down
<Home> or <End>	Move cursor to top or bottom of window.
<PgUp> or <PgDn>	Move cursor to top or bottom of window.
<F5> or <->	Select the Previous Value for the field.
<F6> or <+> or <Space>	Select the Next Value for the field.
<F9>	Load the Default Configuration values for this menu
<F10>	Save and exit.
<Enter>	Execute Command or Select the Sub menu

To select an item, use the arrow keys to move the cursor to the field your want. Then use the plus-and-minus value keys to select a value for that field. To save values commands in the Exit Menu save the values currently displayed in all the menus.

To display a sub-menu, use the arrow keys to move the cursor to the sub menu your want. Then press <Enter>. A pointer (►) marks all sub menus.

4.1.2.2. The Field Help Window

The help window on the right side of each menu displays the help text for the currently selected field. It updates as you move the cursor to each field.

4.1.2.3. The General Help Windows

Pressing <F1> or <Alt-H> on any menu brings up the General Help window that describes the legend keys and their alternates:

```
                    General Help

Setup changes system behavior by modifying the BIOS
configuration. Selecting incorrect values may
cause system boot failure; load Setup Default values to
recover.

<Up/Down>  arrows select fields in current menu.
<PgUp/PgDn> moves to previous/next page on scrollable menus.
<Home/End>  moves to top/bottom item of current menu.

Within a field, <F5> or <-> selects next lower value and
<F6>, <+>,  or  <Space>  selects next higher value.

<Left/Right> arrows select menus on menu bar.
<Enter> displays more options for items marked with |.

<F9> loads factory installed Setup Default values.
<F10> saves current settings and exists Setup.

<Esc> or <Alt-X> exits Setup; in sub-menus, pressing these keys returns to
the previous menu.

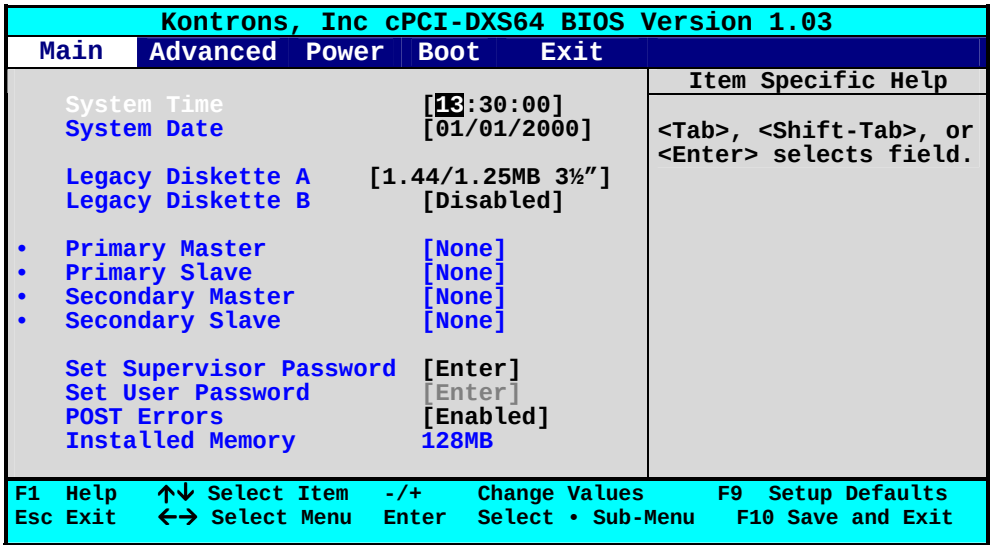
<F1> or <Alt-H> displays General Help (this screen).

                        [Continue]
```

The scroll bar on the right of any windows indicates that there is more than one page of information in the windows. Use <PgUp> and <PgDn> to display all the pages. Pressing <Home> and <End> displays the first and last page. Pressing <Enter> displays each page and then exits the window.

4.1.2.4. Main Menu Selection

You can make the following selections on the Main Menu itself. Use the sub menus for other selections.



Main Menu Selection

Feature	Options	Description
System Time	HH:MM:SS	Set the system time.
System Date	MM/DD/YYYY	Set the system date.
Legacy Diskette A: Legacy Diskette B:	Disabled 360Kb 5.1/4" 1.2MB, 5.1/4"< 720 Kb 3 1/2" 1.44/1. 2 MB 3 1/2" 2.88 MB 3 ½ Disabled	Select the type of floppy disk drive installed in your system. **Note :** 1.25MB 3 1/2" references a 1024 byte/sector Japanese media format. The 1.25MB, 3 1/2 diskette requires a 3-Mode floppy-disk drive.

Main Menu Selection (continued)

Feature	Options			Description
Primary Master	Type	CD-ROM	Multi-Sector Transfers LBA Mode Control 32 BIT I/O Transfer Mode Ultra DMA Mode SMART Monitoring	**Multi-Sector Transfers** Choices : Disabled, 2,4,8, and 16 sectors Any selection except Disabled determines the number of sectors transferred per block. Standard is 1 sector per block. **LBA Mode Control** Choices : Disabled, Enabled Enabling LBA causes Logical Block Addressing to be used in place of Cylinders, heads, and Sectors. **32 Bit I/O** Choices : Disabled, Enabled Enables 32-bit communication between CPU and IDE card. Requires PCI or local bus. **Transfer Mode** Choices : Standard, Fast PIO 1, Fast PIO 2, Fast PIO 3, Fast PIO 4, FPI0 3 / DMA 1, FPIO 4 / DMA2. Selects the method for transferring the data between the hard disk and system memory. The Setup menu only lists those options supported by the drive and platform. **Ultra DMA Mode** Choices : Disabled, Mode 0, 1, 2, 3, 4. Select the Ultra DMA mode used for moving data to/from the drive. Autotype the drive to select the optimum transfer mode. **SMART Monitoring** Display type of Monitoring. This field is a “Display Only”. This option can be changed in the Advanced Menu.
		ATAPI Removable		Same choices as CD-ROM

Main Selection Menu (continued)

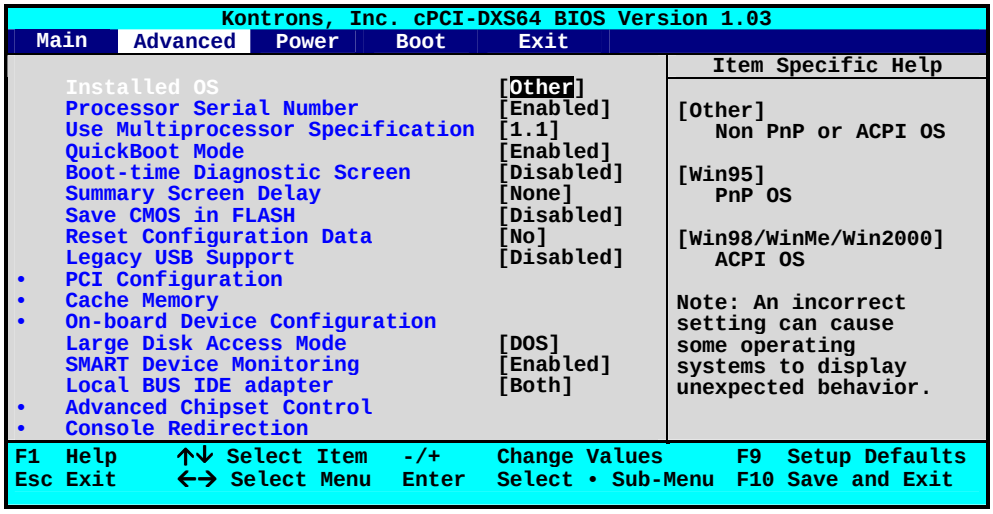
Feature	Options			Description
Primary Master (Continued)	Type (continued	IDE Removable		Same choices as CD-ROM
		Other ATAPI		Same choices as CD-ROM
		(USER)	Cylinders	**Cylinders** Set the number of cylinders
			Heads	**Heads** Set the number of heads. Choices are 1 to 16
			Sectors	**Sectors** Set the number of sectors per track
			Maximum Capacity	**Maximum Capacity** Maximum capacity is displayed according to the cylinders, heads and sectors selected.
			Multi-Sector Transfers	**Multi-Sector Transfers** Choices are : Disabled, 2, 4, 8 and 16 sectors. Specify the number of sectors per block for multiple sector transfers. “MAX” refers to the size the disk returns when queried.
			LBA mode Control	**LBA Mode Control** Choices are : Enabled, Disabled Enabling LBA cause Logical Block Addressing to be used in place of Cylinders Heads and Sectors
			32 Bit I/O	**32 Bit I/O** Choices are : Enabled, Disabled. This setting enables or disables 32 bit IDE data transfers.
			Transfer Mode	**Transfer Mode** Choices are : Standard, Fast PIO 1, Fast PIO 2, Fast PIO 3, Fast PIO 4, FPI0 3 / DMA 1, FPIO 4 / DMA2. Select the method for moving data to/from the drive. Autotype the drive to select the optimum transfer mode.
			Ultra DMA Mode	**Ultra DMA Mode** Choices are: Disabled, Mode 0 to 4. Select the Ultra DMA mode used for moving data to/from the drive Autotype the drive to select the optimum transfer mode.
			SMART Monitoring	**SMART Monitoring** IDE Failure Prediction

Main Menu Selection (continued)

Feature	Options		Description
		Auto	BIOS autodetects the hard disk installed
Primary Slave	Type (continued)	None CD-ROM ATAPI Removable IDE Removable User Auto	Same description as Primary Master
Secondary Master	Same as Primary Master		
Secondary Slave	Same as Primary Master		
Set Supervisor Password	[ENTER]		Enter the new Supervisor Password and Confirm it If a Supervisor Password already exists, you can change it.
Set User Password	[ENTER]		Can be accessed only if a Supervisor Password already exists. Enter the new User Password and Confirm it If a User Password already exists, you can change it.
POST Errors	Enabled Disabled		Pauses and displays SETUP entry or resume boot prompt if error occurs on boot. If disabled, system always attempts to boot.
Installed Memory	Depends on the memory installed on your computer		Displays the amount of RAM memory detected during boot up.

4.1.2.5. Advanced Menu Selection

You can make the following selections on the Advanced Menu. Use the sub menus for other selections.



Feature	Options	Description
Installed O/S	Other Win95 Win98 WinMe Win2000	Other : Non PnP or ACPI OS. Win95 : PnP OS. Win98/Win2000 : ACPI OS. Select the operating system installed on your system, which you will use most commonly. **Note :** An incorrect setting can cause some operating systems to display unexpected behavior.
Processor Serial Number	Enabled Disabled	Controls detection of Processor Serial Number. The System must be reset or restarted from power-on to activate or deactivate this option.
Use Multiprocessor Specification	1.1 1.4	Configures the multiprocessor specification revision level. Some operating systems will require revision 1.1 for compatibility reasons.
QuickBoot Mode	Enabled Disabled	Allows the system to skip certain tests while booting. This will decrease the time needed to boot the system.
Boot-time Diagnostic Screen	Enabled Disabled	Displays the Diagnostic Screen during Boot. Always Enabled when Console Redirection is activated.
Summary Screen Delay	None 30 seconds	Delay to display the system configuration at boot time.
Save CMOS in FLASH	Disabled Enabled	Saving CMOS memory content into Flash Memory will prevent loosing CMOS options when battery fails.
Reset Configuration Data	No Yes	Select “Yes” if you want to clear the Extended System Configuration Data (ESCD) area.

Advanced Menu Selection (continued)

Feature	Options		Description
PCI Configuration	Onboard Ethernet 1 Controller	Disabled Enabled	Enables / Disables the onboard Ethernet controller.1
	Onboard Ethernet 2 Controller	Disabled Enabled	Enables / Disables the onboard Ethernet controller 2
	Onboard SCSI Controller	Disabled Enabled	Enables / Disables the onboard SCSI controller.
	Onboard PCI-PCI Bridge	Enabled Disabled	Enables / Disables onboard PCI-PCI bridge controller.
	Mezzanine PCI-PCI Bridge	Enabled Disabled	Enables / Disables the Mezzanine PCI-PCI bridge controller.
	Default Primary Video Adapter	PCI AGP	Select "PCI" to have the PCI video card (must be installed) to be set as the Boot Display Device. Select "AGP" to have the onboard AGP video card (must be installed) to be set as the Boot Display Device.
	PCI Bridge Cache Line Size	0, 2, 8 or 16	Set the Cache Line Size of PCI-PCI bridges in DWORDS.
	Default Primary Latency timer	Default, 20h, 40h, 60h, 80h, A0h, C0h or E0h	Minimum guaranteed time slice allotted for bus master in units of PCI bus clocks. Primary Latency value to be used for all devices not directly controlled by specific Setup options. Default value is the actual calculated value based on each devices request (MIN_GNT).
	Default Secondary Latency Timer	Default, 20h, 40h, 60h, 80h, A0h, C0h or E0h	Minimum guaranteed time slice allotted for bus master in units of PCI bus clocks. Secondary Latency value of PCI bridges to be used for all bridges not directly controlled by specific Setup options. Default value equals 44h.

Advanced Menu Selection (continued)

	ICH Secondary Latency timer	Default, 20h, 40h, 60h, 80h, A0h, C0h or E0h	Minimum guaranteed time slice allotted for bus master in units of PCI bus clocks. Default value equals 0h (No Latency).
	ICH MTT Latency Timer	Default, 20h, 40h, 60h, 80h, A0h, C0h or E0h	Multi Transaction Timer defines the minimum guaranteed time slice allotted for PCI initiator to perform Multiple back-to-back transactions on the PCI bus in units of PCI bus clocks. Default value equal 0h (No Latency).
	HLB Secondary Latency Timer	Default, 20h, 40h, 60h, 80h, A0h, C0h or E0h	Minimum guaranteed time slice allotted for bus master in units of PCI bus clocks. Default value equal 0h (No Latency).
	P64H Secondary Latency Timer	Default, 20h, 40h, 60h, 80h, A0h, C0h or E0h	Minimum guaranteed time slice allotted for bus master in units of PCI bus clocks. Default value equal 0h (No Latency).
	P64 MTT Latency Timer	Default, 20h, 40h, 60h, 80h, A0h, C0h or E0h	Multi Transaction Timer defines the minimum guaranteed time slice allotted for PCI initiator to perform Multiple back-to-back transactions on the PCI bus in units of PCI bus clocks. Default value equal 0h (No Latency).

Advanced Menu Selection (continued)

Feature	Options		Description
Cache Memory	L1 Cache Memory	Enabled Disabled	Sets the state of L1 memory cache.
	L2 Cache Memory	Enabled Disabled	Sets the state of L2 memory cache.
	Cache System BIOS area	Uncached Write Protect	Controls caching of system B0S area.
	Cache Video BIOS area	Uncached Write Protect	Controls caching of video BIOS area.
	Cache Base 0-512K	Uncached Write Through Write Protect Write Back	Controls caching of 512k base memory
	Cache Base 512K-640K	Same as above	Controls caching of 512k-640k base memory
	Cache Extended Memory Area	Same as above	Controls caching of system memory
	Cache A000-AFFF	Disabled USWC Caching Write Through Write Protect Write Back	Set the type of caching. Following choices are available : **Disabled** : This block is not cached. **USWC Caching** :Uncached Speculative Write Combined. **Write Through:** Writes are cached and sent to main memory at once. **Write Protect:** Writes are ignored. **Write Back:** Writes are cached, but not sent to main memory until necessary. Set the type of caching. Following choices are available :Disabled, Write Through, Write Protect, and Write Back
	Cache B000-BFFF	Same as above	
	Cache C800-CBFF		

Advanced Menu Selection (continued)

Feature	Options		Description	
Cache Memory	Cache CC00-CFFF		Same as above	
	Cache D000-D3FF			
	Cache D400-D7FF			
	Cache D800-DBFF			
	Cache DC00-DFFF			
	Cache E000-E3FF			
	Cache E400- E7FF			
	Cache E800-EBFF			
	Cache EC00- EFFF			
Onboard Device Configuration	Serial Port A	Disabled Enabled Auto OS Controlled	Configure serial port A using options: **Disabled :** No configuration **Enabled :** User configuration When Enabled, set the base I/O address for serial port A. **Auto :** BIOS or OS chooses configuration **OS Controlled :** Displayed when controlled by OS.	
		Base I/O address	3F8 2F8 3E8 2E8	Set the base I/O address for serial port A.
		Interrupt	IRQ 3 IRQ 4	Set the interrupt for serial port A.
	Serial Port B	Disabled Enabled Auto OS Controlled	Same description as Serial Port A.	
		Base I/O address		
		Interrupt		
		Mode	RS-422 RS-485 RS-232	Set the mode for serial port B.

Advanced Menu Selection (continued)

Feature	Options		Description	
I/O Device Configuration (continued)	Parallel port	Disabled Enabled Auto OS Controlled	Configure parallel port using options : **Disabled :** No configuration **Enabled :** User configuration When enabled, set the Base I/O address. **Auto:** BIOS or OS chooses configuration **OS Controlled:** Displayed when controlled by OS	
		Mode	Output only Bi-directional EPP ECP	Set the mode for the parallel port.
		Base I/O address	378 278 3BC	Set the base I/O address for the parallel port.
		Interrupt	IRQ 5 IRQ 7	Set the interrupt for the parallel port.
	Floppy Disk Controller	Disabled Enabled Auto OS Controlled	Configure the floppy disk controller by using these options : **Disabled :** No configuration **Enabled:** User configuration **Auto:** BIOS or OS chooses configuration **OS Controlled :** Displayed when controlled by OS**.**	
	Base I/O address	Primary Secondary	Set the base I/O address for the floppy disk controller.	
Large Disk Access Mode	Other DOS	If you are using UNIX, Novell Netware or other operating systems, select "**Other**". If you are installing new software and the drive fails, change this selection and try again. Different operating systems require different representations of drive geometry.		
SMART Device Monitoring	Disabled Enabled	IDE Failure Prediction		
Local Bus IDE adapter	Disabled Primary Secondary Both	Enable the integrated local bus IDE adapter.		

Advanced Menu Selection (continued)

Feature	Options		Description
	Graphics Aperture	4, 8, 16, 32, 64, 128 or 256Mb	Select the size of the Graphics Aperture for the AGP video device.
	Enable memory gap	Disabled Enabled	If enabled, turns system RAM off to allocate this address space to an optional card. A 1MB extended memory gap, starting at 15MB, will be created in system RAM.
	ECC Config	Disabled EC ECC ECC Scrub	If all memory in the system supports ECC (x72), this selection selects from no ECC, checking only, checking and correction, or checking correction with scrubbing.
	ECC Error Type	None NMI SMI SCI	When an ECC error occurs, it generates an interrupt. Selects the type of interrupt to report: NMI : Non Maskable Interrupt SMI System Management Interrupt SCI System Control Interrupt
	SERR signal condition	None Single bit Multiple bit Both	Selects ECC error conditions that SERR# be asserted.
	Pool A Capacity	1, 2, 4 or 8	Defines the maximum number of RDRAM device pairs that can be in active mode at same time.
	Pool B Capacity	1, 4, 8 or 16	Defines the maximum number of RDRAM device pairs that can be in standby mode at same time.

Advanced Menu Selection (continued)

	Watchdog Timer	Disabled, Enabled		Enables the Watchdog circuit when the POST is running.
	Watchdog After POST	Disabled, Enabled		Enables the Watchdog circuit after the POST sequence. The BIOS will hook the Timer Tick interrupt to automatically refresh the Watchdog, unless the OS replaces the interrupt service.
	Watchdog Duration (ms)	16, 64, 256, 1024 4096, 16384 65536, 262144		Selects the duration time (in ms) of the Watchdog timing circuitry.
	Console Redirection			Useful sequences: F1 = Esc O P F9 = Esc [2 0 F10 = Esc O p Ward Reset = Esc Del
		Com Port Address	On-board COMA On-Board COMB	If enabled, it will use a port on the motherboard. Install the VT100 jumper to use the Console Redirection.
		Baud Rate	300, 1200, 2400, 9600, 19.2K, 38.4K, 57.6K, 115.2K	Enables the specified baud rate.
		Console Type	PC ANSI VT-100	Enables the specified console type.
		Flow Control	None XON/XOFF CTS/RTS	Enables Flow Control
		Continue C.R. after POST	Off, On	Enables Console Redirection after OS has loaded.

4.1.2.6. Power Menu Selection

Feature	Options	Description	
Intelligent System Monitor	Intelligent System Monitoring	Disabled Enabled	Enables/Disables the Intelligent System Monitor device. When enabled, the system will monitor some system states such as temperature and power supplies.
	Interrupt Generation	Disabled Enabled	Enables/Disables the generation of interrupts when an event occurs. This must be set to DISABLED when programs such as LANDesk® are loaded onto the system.
	Chassis Intrusion	Disabled Enabled	Enables/Disables the detection of chassis intrusion.
	Secured Chassis	Disabled Enabled	Controls the SECURE CHASSIS feature. If set to ENABLED and a chassis intrusion is detected, the user is required to enter SETUP and set the option "Reset chassis intrusion" to "Yes", before the system is allowed to complete the boot.
	Reset Chassis Intrusion	No Yes	Selecting "Yes" will reset the chassis intrusion circuitry on the next boot.
	Beep codes for non-thermal events	Disabled Enabled	Produces beep codes when the Intelligent System Monitoring events occur for either the chassis, the fan or the voltages. Codes are as follows: One long beep plus: 2 short beeps for chassis intrusion 3 short beeps for fan events 4 short beeps for voltage events This alarm may not be supported by the operating system.
	Thermal Audio Alarm	Disabled Enabled	When the Thermal Management option and this option are enabled, a continuous audible alarm is sounded when the temperature specified in the Overheat Alarm options is reached. This alarm may not be supported by the operating system.

Power Menu Selection (continued)

Feature	Options		Description
Hardware Monitor Inputs	Present LoLimit HiLimit Vcore CPU 1 1.65V ----- ----- Vcore CPU 2 1.66V ----- ----- Vin 2.5 2.48 ----- ----- Vin 3.3 3.29 ----- ----- Vin 5 5.09V ----- ----- Vin 12 12.09 ----- ----- CPU Fan 1 Speed (RPM) 5625 CPU Fan 2 Speed (RPM) 6081 CPU 1 Die Temperature 30°C/86°F CPU 2 Die Temperature 31°C/86°F		All items on this menu cannot be modified in user mode. If one or more items require changes,please consult your System Supervisor.
Hardware Monitor Controls	Vcore CPU 1 Voltage Interrupt Vcore CPU 2 Voltage Interrupt Vin 2.5 Voltage Interrupt Vin 3.3 Voltage Interrupt Vin 5 Voltage Interrupt Vin 12 Voltage Interrupt FAN 1 Interrupt FAN 2 Interrupt CPU 1 Temperature Interrupt CPU 2 Temperature Interrupt Resume Alarm (°C) Overheat Alarm (°C) Shutdown Alarm (°C)	Disabled / Enabled Disabled / Enabled Disabled / Enabled Disabled / Enabled Disabled / Enabled Disabled / Enabled Disabled / Enabled Disabled / Enabled Disabled / Enabled Disabled / Enabled [42] [50] [60]	This option enables (Voltage, Fan or Temperature) events handling.

4.1.2.7. Boot Menu Selection

Feature	Options	Description
	Hard Drive Bootable Add-in Cards Primary Master Removable Devices Legacy Floppy Drives Hard Drive Bootable Add-in Cards * ATAPI CD-ROM Drive Network Boot	Keys used to view or configure devices: **<Enter>** expands or collapses devices with a **+** or **–** **<Ctrl+Enter>** expands all **<Shift + 1>** enables or disables a device **<+>** or **<->** moves the device up or down **<n>** May move removable device between Hard Disk or Removable Disk **<d>** Remove a device that is not installed. * Note : The hard drives and SCSI drives detected will be listed in this section and the first drive in the list will be the boot drive.

4.1.2.8. Exit Menu Selection

Feature	Options		Description
	Exit Saving Changes Exit Discarding Changes Load Setup Defaults Discard Changes Saves Changes	Yes / No Yes / No Yes / No Yes / No	**Exit Saving Changes** Setup and save your changes to CMOS. **Exit Discarding Changes** Exit utility without saving Setup data to CMOS. **Load Setup Defaults** Exit utility without saving Setup data to CMOS. **Load Setup Defaults** Load default values for all SETUP items. **Discard Changes** Load previous values from CMOS for all SETUP items. **Save Changes** Save Setup Data to CMOS.

4.2. BOOT UTILITIES

Phoenix Boot Utilities are : Phoenix QuietBoot™
Phoenix MultiBoot™

Phoenix QuietBoot displays a graphic illustration rather than the traditional POST messages while keeping you informed of diagnostic problems.

Phoenix MultiBoot is a boot screen that displays a selection of boot devices from which you can boot your operating system.

4.2.1. Phoenix Quiet Boot

Right after you turn on or reset the computer, Phoenix QuietBoot displays the QuietBoot Screen, a graphic illustration created by the computer manufacturer instead of the text-based POST screen, which displays a number of PC diagnostic messages.

To exit the QuietBoot screen and run Setup, display the Multiboot menu, or simply display the PC diagnostic messages, you can simply press one of the hot keys described below.

The QuietBoot Screen stays up until just before the operating system loads unless:

1. You press <ESC> to display the POST screen.
2. You press <Del> to enter Setup.
3. POST issues an error message.
4. The BIOS or an option ROM requests keyboard input.

The following explains each of these situations.

4.2.1.1. Press <ESC>

1. Pressing <ESC> switches the POST screen and The boot process continues with the text-based POST screen until the end of POST, and then displays the BootFirst Menu, with these options:
   a. Load the operating system from a boot device of your choice.
   b. Enter Setup.
   c. Exit the Boot First Menu (with <ESC>) and load the operating system from the boot devices in the order specified in Setup.

4.2.1.2. Press <Del>

Pressing < Del > at any time during POST switches to the POST screen (if not already displayed) and enter Setup.

4.2.1.3. POST Error

Whenever POST detects a non-fatal error, QuietBoot switches to the POST screen and displays the errors. It then displays this message:

Press <F1> to resume, <Del> to Setup

Press <F1> to continue with the boot. Press <Del> if you want to correct the error in Setup.

4.2.1.4. Keyboard Input Request

If the BIOS or an Option ROM (add-on card) requests keyboard input, QuietBoot switches over to the POST screen and the Option ROM displays prompts for entering the information. POST continues from there with the regular POST screen.

4.2.1.5. Phoenix Multiboot

Phoenix Multiboot expands your boot options by letting you choose your boot device, which could be a hard disk, floppy disk, or CDROM. You can select your boot device in Setup, or you can choose a different device each time you boot during POST by selecting your boot device in **The Boot First Menu**.
Multiboot consist of:

The Setup Boot Menu
The Boot First Menu

4.3. INSTALLING DRIVERS

4.3.1. Video Drivers

Various drivers are provided for different operating systems and software. To install a driver, refer to the Setup program located on the CD-ROM (provided with your board).

4.3.2. Ethernet Drivers

Various drivers are provided for different operating systems and software. To install a driver, use the Setup program and the ReadMe.bat file located on the CD-ROM (provided with your board).

4.3.3. Other Drivers

For other operating system drivers and installation instructions or for more information, contact Kontron's Technical Support department.

4.4. VT100 MODE

The VT100 operating mode allows remote setups of the board. This configuration requires a remote terminal that must be connected to the board through a serial communication link.

4.4.1. Requirements

The terminal should emulate a VT100 or ANSI terminal. Terminal emulation programs such as Telix© or Procom© can also be used.

4.4.2. Setup & Configuration

Follow these steps to set up the VT100 mode:

1. Connect a monitor and a keyboard to your board and turn on the power.
2. Enter into the CMOS Setup program in the "Advanced" page, "Console Redirection" menu.
3. Select the VT100 mode and the appropriate COM port and save your setup.
4. Connect the communications cable as shown in the next page.

> **NOTE**
>
> If you do not require a full cable for your terminal, you can set up a partial cable by using only the TXD and RXD lines. To ignore control lines simply loop them back as shown in VT100 Partial Setup cable diagram.

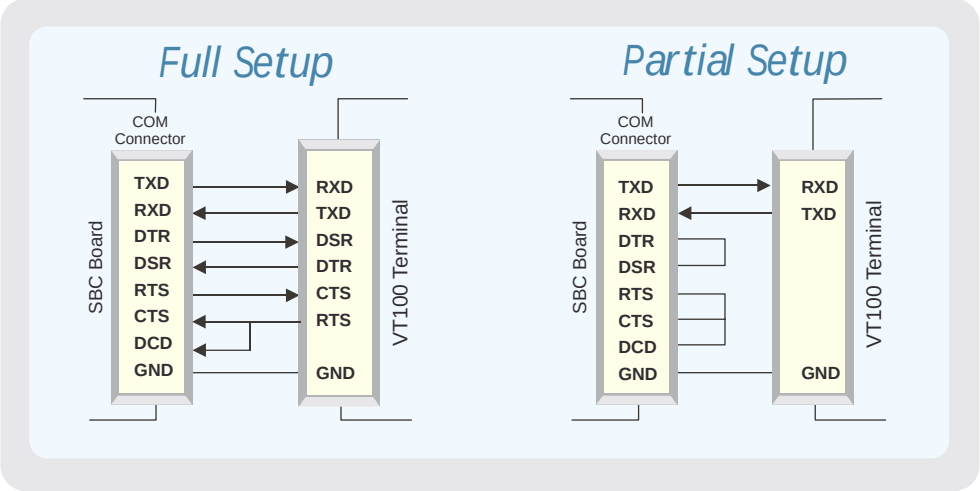
5. Configure your terminal to communicate using the same parameters as in CMOS Setup.
6. Install the VT100 jumper. Reboot the board.
7. Use the remote keyboard and display to setup the BIOS.

Save the setup, exit, and disconnect the remote computer from the board to operate in stand-alone configuration.

Console Redirection is done by refreshing the Video address @ B8000h at the selected BAUD rate. This means that a low baud rate refreshes the screen slowly, but the CPU time is maximized for the applications. A high BAUD rate refreshes the screen rapidly but the CPU is frequently interrupted by the Serial Port.

Console Redirection provided by Phoenix based BIOS offers various escape sequences to emulate keyboard function keys. The following table lists the escape sequences available.

Escape sequence	Function		Escape sequence	Function
Esc Del	Warm Reset		Esc [6 4 ~	cF1 (Ctrl-F1)
Esc O P	F1		Esc [6 5 ~	cF2
Esc O Q	F2		Esc [6 6 ~	cF3
Esc O R	F3		Esc [6 7 ~	cF4
Esc O S	F4		Esc [6 8 ~	cF5
Esc O w	F3		Esc [6 9 ~	cF6
Esc O x	F4		Esc [7 0 ~	cF7
Esc O t	F5		Esc [7 1 ~	cF8
Esc O u	F6		Esc [7 2 ~	cF9
Esc O q	F7		Esc [7 3 ~	cF10
Esc O r	F8		Esc [7 4 ~	cF11
Esc O p	F10		Esc [7 5 ~	cF12



PART 5

APPENDICES

A. MEMORY & I/O MAPS

B. INTERRUPT LINES

C. BOARD DIAGRAMS

D. CONNECTOR PINOUTS

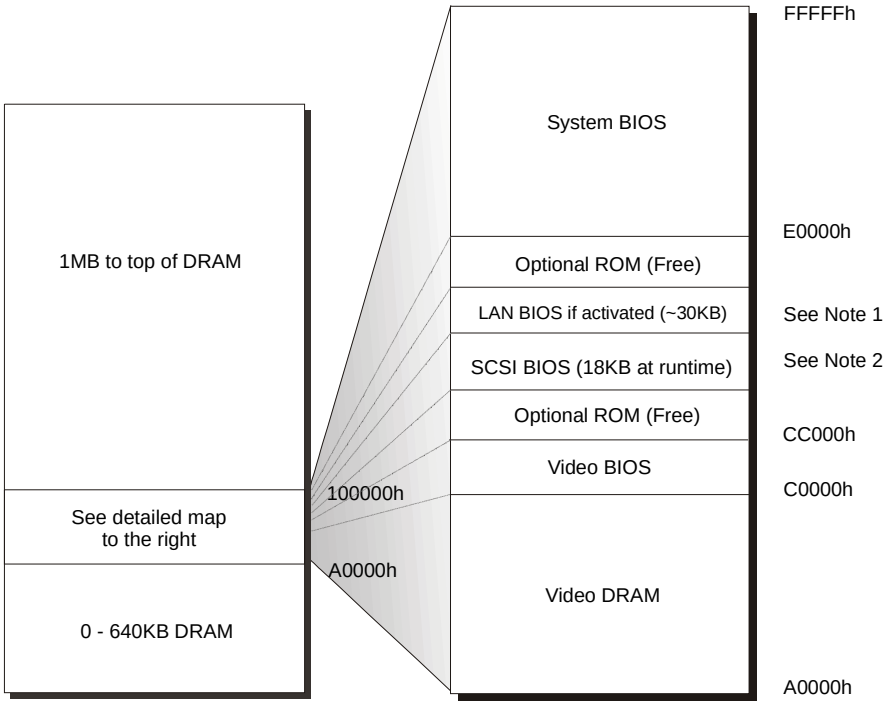
E. BIOS SETUP ERROR CODES

F. BIOS UPDATE & EMERGENCY PROCEDURE

G. GETTING HELP & RMA

A. MEMORY & I/O MAPS

A.1 MEMORY MAPPING



Note 1 : LAN BIOS address may vary

Note 2 : SCSI BIOS address may vary.
Size is only 2KB if no device.

Address	Function
00000-9FFFF	0-640 KB DRAM
A0000-BFFFF	Video DRAM
C0000-CBFFF	Video BIOS
CC000-FFFFF	Optional ROM (Free)
	LAN BIOS around 30KB if activated, address may vary
E0000-FFFFF	System BIOS
100000-Top of DRAM	1 MB - Top of DRAM

A.2 I/O MAPPING

Address	Optional Address	Optional Address	Optional Address	Function
000-01F				DMA Controller 1
020-03F				Interrupt Controller 1
040-05F				Timer
060-06F				Keyboard
070-07F				Real-time clock
080-09F				DMA Page Register
0A0-0BF				Interrupt Controller 2
0C0-0DF				DMA Controller 2
0F0-0F1, 0F8-0FF				Math Coprocessor
190-197	290-297	390-397		Kontron Control Port
1F0-1F7, 3F6				Primary IDE
170-177, 376				Secondary IDE
3F0-3F7	370-377			Floppy Disk
378-37A	3BC-3BE	278-27A		Parallel Port (LPT1 by default)
3F8-3FF (COM1)	2F8-2FF (COM2)	3E8-3EF (COM3)	2E8-2EF (COM4)	Serial Port 1 (COM1 by default)
2F8-2FF (COM2)	3F8-3FF (COM1)	3E8-3EF (COM3)	2E8-2EF (COM4)	Serial Port 2 (COM2 by default)
3C0-3CF, 3D0-3DF, 3B0-3BB				Graphics Controller (I2C Port)

B. INTERRUPT LINES

B.1 IRQ LINES

The board is fully PC compatible with interrupt steering for PCI plug and play compatibility.

Controller # 1		Controller # 2	
IRQ 0	Timer Output 0	IRQ 8	Real-Time Clock
IRQ 1	Keyboard (Output Buffer Full)	IRQ 9	Available [1]
IRQ 2	Cascade Controller # 2	IRQ 10	Available [1]
IRQ 3*	Serial Port 2	IRQ 11	Available [1]
IRQ 4*	Serial Port 1	IRQ 12	PS/2 Mouse
IRQ 5*	Parallel Port 2 or Available [1]	IRQ 13	Coprocessor Error
IRQ *6	Floppy Controller	IRQ 14	Primary IDE * or available [1]
IRQ 7*	Parallel Port 1 or Available [1]	IRQ 15	Secondary IDE * or available [1]

* :All functions marked with an asterisk (*) can be disabled or reconfigured.
1 Available lines service on board and external PCI/ISA PnP devices or a Legacy ISA device.

B.2 DMA CHANNELS

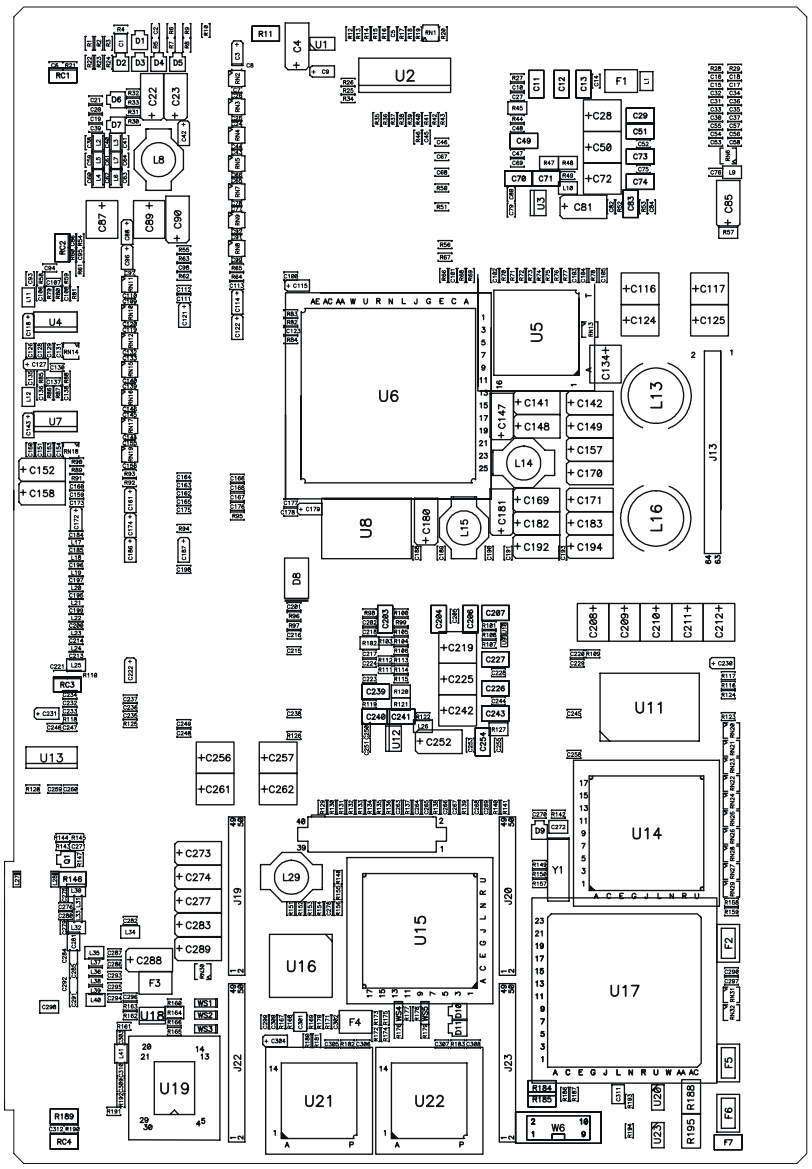
The cPCI-DXS64 integrates the functionality of two 8237 DMA controllers. Eight DMA channels are available.

According to Plug and Play standards, the system BIOS automatically allocates DMA Channel 1 or 3 for the parallel port's ECP mode. Channel 2 is reserved for the floppy controller and Channel 4 is used to cascade Channels 0 through 7 to the microprocessor.

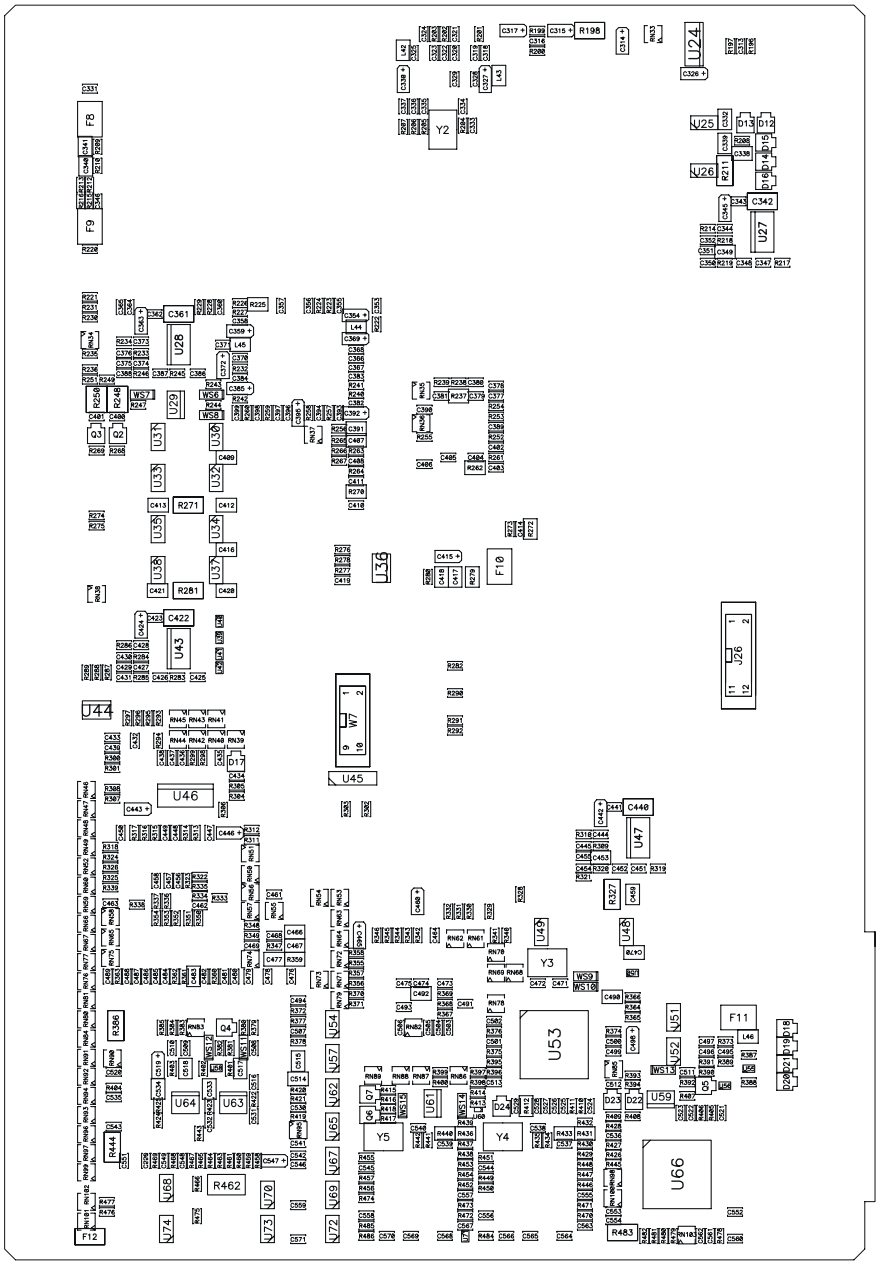
DMA Channel	Function
DMA 0	Available
DMA 1	PnP available (ECP)
DMA 2	Floppy controller
DMA 3	PnP available (ECP)
DMA 4	Cascade controller # 1
DMA 5	PnP available
DMA 6	PnP available
DMA 7	PnP available

C. BOARD DIAGRAMS

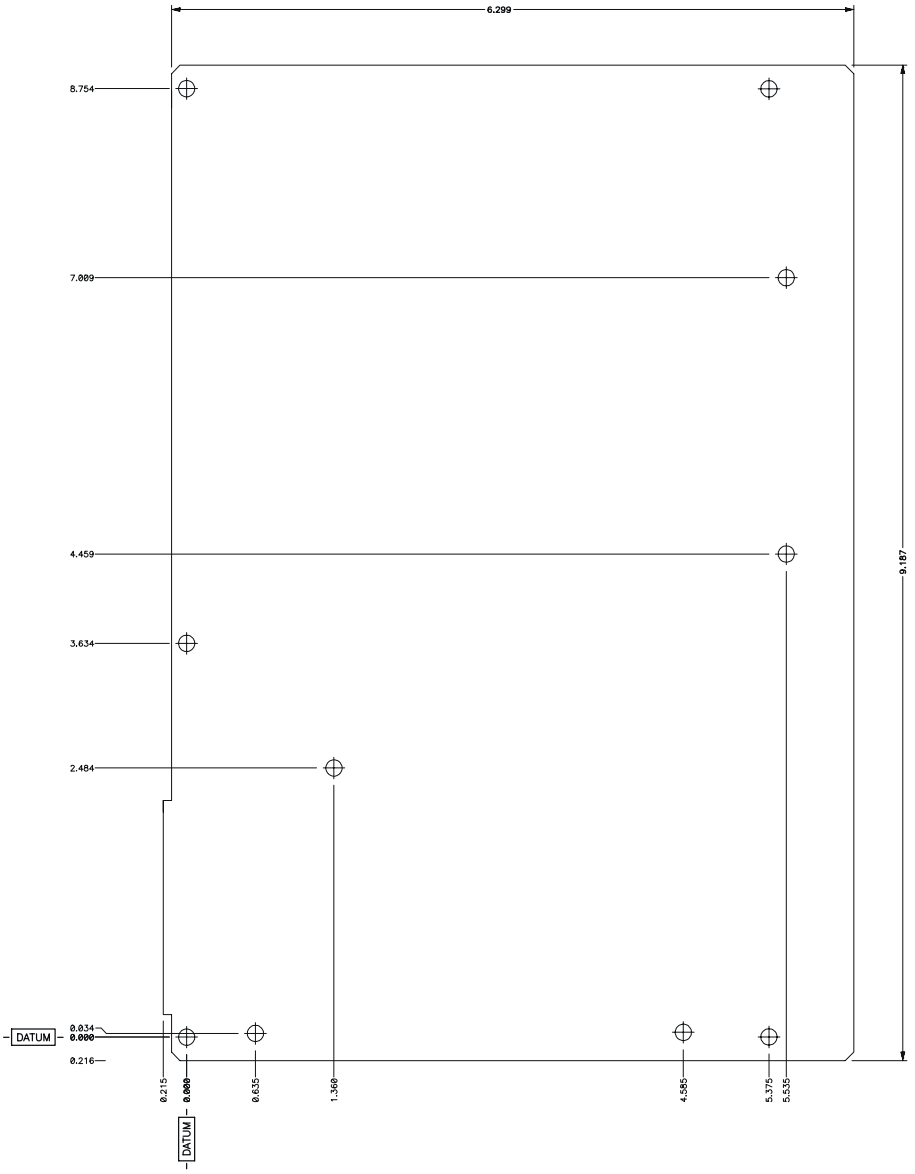
C.1 TOP DEVICES SURFACE MOUNT



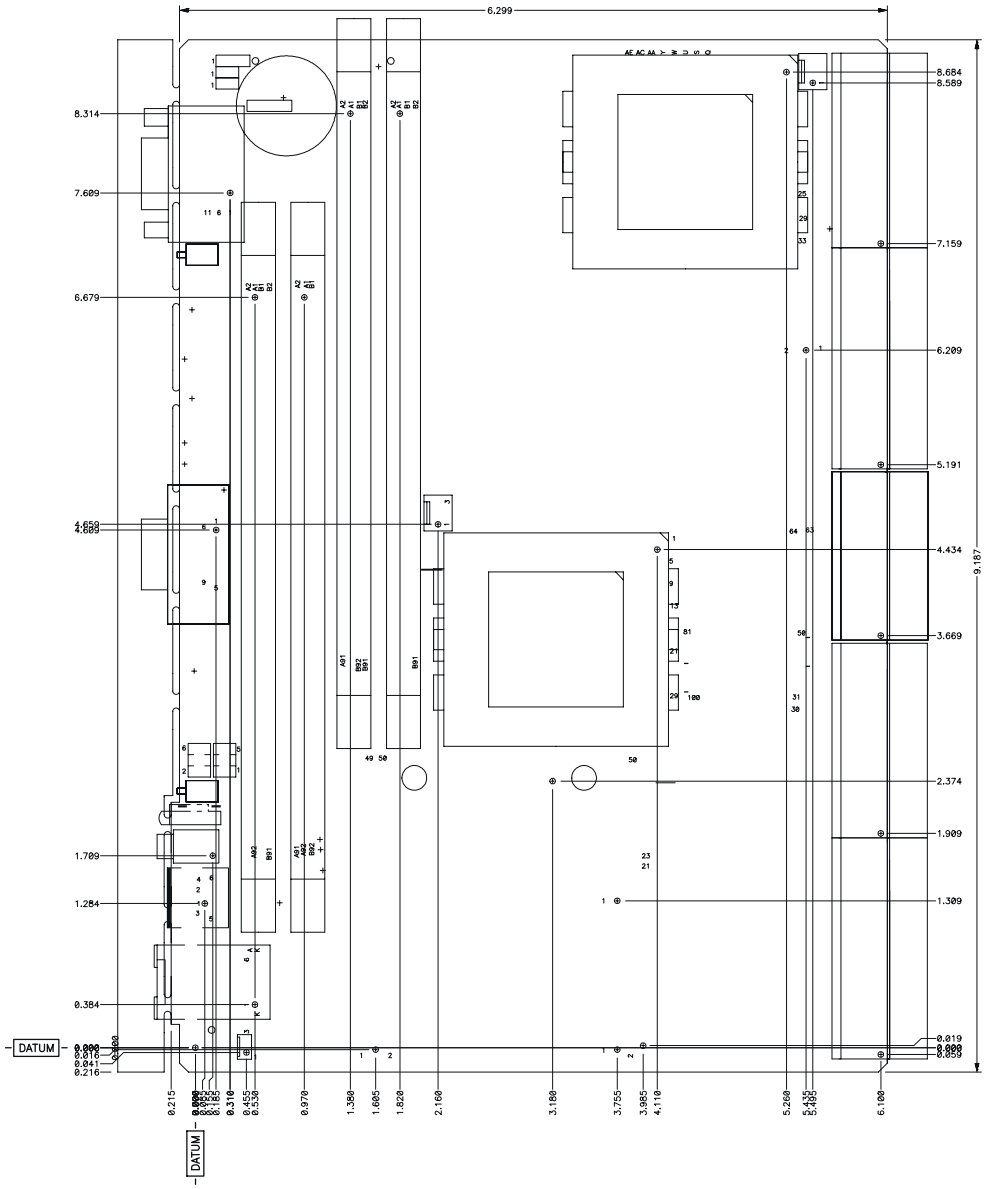
C.2 BOTTOM DEVICE SURFACE MOUNT



C.3 MOUNTING HOLES



C.4 CONNECTOR HOLES



D. CONNECTOR PINOUTS

D.1 cPCI- DXS64 CONNECTORS AND HEADERS

DXS64	Connector J14
J1	CPCI Bus connector
J2	CPCI Bus connector
J3	CPCI I/O connector
J4	CPCI I/O connector
J5	CPCI I/O connector
J6, J16	CPU socket, PGA370
J7, J15	Not used
J8, J9, J11, J12	RIMM sockets
J10	CRT VGA Connector (Front panel configuration only)
J13	Mezzanine
J14	Serial Port 1 – RS-232 (Front panel configuration only)
J17	CompactFLASH disk connector
J18	USB Port (Front panel configuration only)
J19	PCI Mezzanine card (PMC)
J20, J23	64Bit/66MHz mezzanine
J21	PS/2 Keyboard connector
J22	PCI Mezzanine connector
J24	Dual Ethernet connector (Front panel configuration only)
J25	Hot Swap switch
J20, J23	Ethernet 2 connector (Front panel configuration only)
SW1	Reset switch
SW2	NMI switch
BT1	CMOS Battery Backup connector

D.2 J1 cPCI Bus

	ROW A	ROW B	ROW C	ROW D	ROW E
1	VCC5E	-12VE	RSV	+12VE	VCCE
2	RSV	VCCE	RSV	RSV	RSV
3	INTA#	INTB#	INTC#	VCCE	INTD#
4	IPMB0_PWR	HEALTHY#	VI/O	INTP	INTS
5	BRSVP1A5	BRSVP1B5	RST#	GND	GNT0#
6	REQ0#	GND	VCC3E	CLK0	AD31
7	AD30	AD29	AD28	GND	AD27
8	AD26	GND	V I/O	AD25	AD24
9	CBE3#	RSV	AD23	GND	AD22
10	AD21	GND	VCC3E	AD20	AD19
11	AD18	AD17	AD16	GND	CBE2#
12 13 14	**KEY AREA**				
15	VCC3E	FRAME#	IRDY#	BD_SEL#	TRDY#
16	DEVSEL#	GND	V I/O	STOP#	LOCK#
17	VCC3E	IPMB0_SCL	IPMB0_SDA	GND	PERR#
18	SERR#	GND	VCC3E	PAR	CBE1#
19	VCC3E	AD15	AD14	GND	AD13
20	AD12	GND	V I/O	AD11	AD10
21	VCC3E	AD9	AD8	M66EN	CBE0#
22	AD7	GND	VCC3E	AD6	AD5
23	VCC3E	AD4	AD3	VCCE	AD2
24	AD1	VCCE	V I/O	AD0	ACK64#
25	VCCE	REQ64#	ENUM#	VCC3E	VCCE

Active Low

Long pins : 3D, 4C,5D, 6C, 7D, 9D, 10D, 17D, 19D, 22C, 23D, 24C

Short pins : 9B, 15D

D.3 J2 cPCI Bus

		ROW A	ROW B	ROW C	ROW D	ROW E
1		S_CLK1	GND	REQ1#	GNT1#	REQ2#
2		S_CLK2	S_CLK3	SYSEN#	GNT2#	REQ3#
3		S_CLK4	GND	GNT3#	REQ4#	GNT4#
4		V I/O	BRSV	CBE7#	GND	CBE6#
5		CBE5#	RSV	V I/O	CBE4#	PAR64
6		AD63	AD62	AD61	GND	AD60
7		AD59	GND	V I/O	AD58	AD57
8		AD56	AD55	AD54	GND	AD53
9		AD52	GND	V I/O	AD51	AD50
10		AD49	AD48	AD47	GND	AD46
11		AD45	GND	V I/O	AD44	AD43
12		AD42	AD41	AD40	GND	AD39
13		AD38	GND	V I/O	AD37	AD36
14		AD35	AD34	AD33	GND	AD32
15		BRSV	GND	FAL#	REQ5#	GNT5#
16		BRSV	BRSV	DEG#	GND	BRSV
17		BRSV	GND	PRST#	REQ6#	GNT6
18		BRSV	BRSV	BRSV	GND	BRSV
19		GND	GND	IMPB_SCL	IMPB1_SDA	IPMB_ALERT
20		CLK5	GND	RSV	GND	RSV
21		CLK6	GND	RSV	RSV	RSV
22		GA4	GA3	GA2	GA1	GA0

Active Low

D.4 J3 cPCI Bus

	ROW A	ROW B	ROW C	ROW D	ROW E
1	RSV	SCSI:D11+	SCSI:I/O+	RSV	GND
2	GND	RSV	GND	RSV	GND
3	RSV	VCC	SCSI:D9+	SCSI:DIFFSENS	RSV
4	RSV	SCSI:D10+	RSV	SCSI:C/D+	RSV
5	RSV	GND	RSV	GND	SCSI:SEL+
6	SPEEDLED0	LINKLED_0	ACTLED0	LINKLED_1	SPEEDLED1
7	ACTLED_1	SD7	SD6	SD5	SD4
8	GND	VCC	VCC	SD3	SD2
9	LAN1 :ETX+	LAN1 :ETX-	LAN1 :ERX+	LAN1 :ERX-	GND
10	GND	WR_80#	SD1	+12V	+12V
11	COM4:DCD#	GND	COM4:RXD	COM4:DSR	COM4:TXD
12	COM4:RTS#	COM4:CTS#	COM4:RI#	VCC	COM4:DTR#
13	COM3:DCD#	VCC	COM3:RXD	COM3:DSR	COM3:TXD
14	COM3:RTS#	COM3:CTS#	COM3:RI#	SD8	COM3:DTR
15	S2_BD_SEL#	S3_BD_SEL#	S3_PCI_RST#	SD0	S4_BD_SEL#
16	S2_HEALTHY#	S3_HEALTHY#	TD-GLAN2_MEZ	RD-GLAN2_MEZ	SCSI:REQ+
17	S2-PCI_RST#	TD+GLAN2_MEZ	RD+GLAN2_MEZ	S4_HEALTHY#	S4_PCI_RST#
18	N/C	IDE1:DASP#	IDE0:DASP#	N/C	N/C
19	RSV	RSV	RSV	S5_BD_SEL#	RSV

Active Low

D.5 J4 cPCI Bus

	ROW A	ROW B	ROW C	ROW D	ROW E
1	I2C-CLK	I2C-DATA	LID	EXTFAN0FAIL#	EXTFAN1FAIL#
2	SM-BYPASS#	SCSI:D11-	SCSI:D10-	SCSI:D9-	SCSI:D8-
3	SCSI:I/O-	SCSI:REQ-	SCSI:C/D-	SCSI:SEL-	SCSI:MSG-
4	SCSI:RST-	SCSI:ACK-	SCSI:BSY-	SCSI:BSY+	SCSI:ATN-
5	SCSI:ACK+	RSV	SCSI:TERMPWR	SCSI:TERMPWR	SCSI:DPO+
6	SCSI:ATN+	SCSI:DP0-	SCSI:D7-	SCSI:D6-	SCSI:D5-
7	SCSI:D4-	SCSI:D3-	SCSI:D2-	SCSI:D1-	SCSI:D0-
8	SCSI:DP1-	SCSI:D15-	SCSI:D14-	SCSI:D13-	SCSI:D12-
9	SCSI:RST+	SCSI:MSG+	R_S5HEALTHY#	VGA:SDA	S5PCIRST#
10	VGA :SCL	VGA :HSYNC	VGA:VSYNC	VGA:RED	VGA:GREEN
11	VGA:BLUE	SCSI:D3+	S6BDSEL#	SCSI:D5+	SCSI:D6+
12 13 14	**KEY AREA**				
15	SCSI:D0+	+5V	+5V	S6HEALTHY#	S6PCIRST#
16	LAN0:ETX+	LAN0 :ETX-	LAN0 :ERX+	LAN0 :ERX-	SSCI:D7+
17	SRST#	SCSI:D15+	IDE1:D7	IDE1:D8	IDE1:D6
18	IDE1:D9	IDE1:D5	IDE1:D10	IDE1:D4	IDE1:D11
19	IDE1:D3	IDE1:D12	IDE1:D2	IDE1:D13	IDE1:D1
20	IDE1:D14	IDE1:D0	IDE1:D15	SCSI:D4+	S7BDSEL#
21	SREQ	SCSI:D13+	IDE1:IOW#	SCSI:DP1+	IDE1:IOR#
22	SCSI:D12+	IDE1:IORDY	S7HEALTHY#	IDE1:DACK#	IRQ15
23	IDE1:I/O16	IDE1:A1	SCSI:D2+	IDE1:A0	IDE1:A2
24	IDE1:CS1#	IDE1:CS3#	SCSI:D14+	SCSI:D1+	SM_BTI#
25	S7PCIRST#	S8BDSEL#	S8HEALTHY#	S8PCIRST#	+5V

Active Low

D.6 J5 cPCI Bus

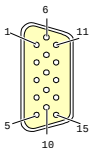
		ROW A	ROW B	ROW C	ROW D	ROW E
1		IDE0:RST#	IDE0:RST#	IDE0:D7	IDE0:D8	IDE0:D6
2		IDE0:D9	IDE0:D5	IDE0:D10	IDE0:D4	IDE0:D11
3		IDE0:D3	IDE0:D12	IDE0:D2	IDE0:D13	IDE0:D1
4		IDE0:D14	IDE0:D0	USB1:GND	IDE0 :D15	IDE0 :IRQ14
5		IDE0:REQ	IDE0:I0RDY	IDE0:IOW#	IDE0:DACK#	IDE0:IOR#
6		RSV	GND	IDE0:DIAG#	IDE0:A0	IDE0:A2
7		IDE0:CS1#	IDE0:CS3#	IDE0:A1	S66DETECT	FD:DRVEN0#
8		FD:DRVEN1#	FD:INDEX#	FD:MTR0#	FD:DS1#	FD:DS0#
9		FD:MTR1#	FD:DIR#	FD:STEP#	FD:WDATA#	FD:WGATE#
10		FD:TRK0#	FD:WRTPRT#	FD:RDATA#	FD:HDSEL#	FD:DSKCHG#
11		COM2:DCD#	GND	COM2:RXD	COM2:DSR#	COM2:TXD
12		COM2:RTS#	COM2:CTS#	COM2:RI#	VCC	COM2:DTR#
13		COM1:DCD#	VCC	COM1:RXD	COM1:DSR#	COM1:TXD
14		COM1:RTS#	COM1:CTS#	COM1:RI#	GND	COM1:DTR#
15		LPT:SLCT	LPT:PE	LPT:BUSY	LPT:ACK#	LPT:D7
16		LPT:D6	LPT:D5	LPT:D4	LPT:D3	LPT:SLCTIN#
17		LPT:D2	LPT:INIT#	LPT:D1	LPT:ERR#	LPT:D0
18		LPT:ALF#	USB1:DATA+	USB1:DATA-	USB0:GND	USB0:VCC
19		LPT:STB#	USB1:GND	USB1:VCC	USB0:DATA+	USB0:DATA-
20		VCC	SMBDATA	SMBALERT#	GND	SMBCLK
21		KB:DATA	KB:CLK	KB:VCC	MOUSE:DATA	MOUSE:CLK
22		PBRST#	GND	DIAG_OC#	VCC	SPK-OUT

Active Low

D.7 J10, VIDEO (VGA)

Signal		Signal		Signal	
RED	1	Analog GND	6	Not Connected	11
GREEN	2	Analog GND	7	SDATA	12
BLUE	3	Analog GND	8	HSYNC	13
Not Connected	4	Not Connected	9	VSYNC	14
GND	5	GND	10	SCLK	15

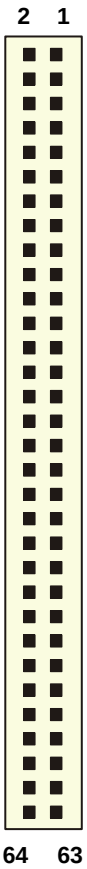
Top View



D.8 J13, MEZZANINE (SCSI)

Pin Number	Signal
SD-12	2
SD-13	4
SD-14	6
SD-15	8
SDP-1	10
SD-0	12
SD-1	14
SD-2	16
SD-3	18
SD-4	20
SD-5	22
SD-6	24
SD-7	26
SDP-0	28
GND	30
EN_SCSI	32
TERMPWR	34
SCSIACT#	36
GND	38
SATN-	40
SBSY-	42
SACK-	44
SRST-	46
SMSG-	48
SSEL-	50
SCD-	52
SREQ-	54
SIO-	56
SD-8	58
SD-9	60
SD-10	62
SD-11	64

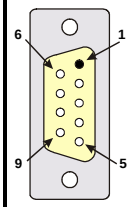
Top View



Pin Number	Signal
1	SD+12
3	SD+13
5	SD+14
7	SD+15
9	SDP+1
11	SD+0
13	SD+1
15	SD+2
17	SD+3
19	SD+4
21	SD+5
23	SD+6
25	SD+7
27	SDP+0
29	GND
31	DIFFSENS
33	TERMPWR
35	TERMPWR
37	GND
39	SATN+
41	SBSY+
43	SACK+
45	SRST+
47	SMSG+
49	SSEL+
51	SCD+
53	SREQ+
55	SIO+
57	SD+8
59	SD+9
61	SD+10
63	SD+11

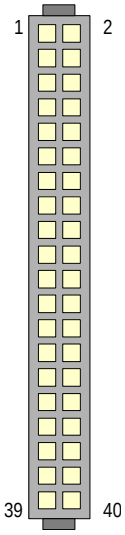
D.9 J14, SERIAL PORT 1 - RS-232

Pin Number		Top View	Pin Number	
Signal				Signal
DSR	6		1	DCD
RTS	7		2	RXD
CTS	8		3	TXD
RI	9		4	DTR
			5	GND



D.10 J17, COMPACTFLASH DISK

Pin Number		Top View	Pin Number	
Signal				Signal
DD11	1		2	GND
DD12	3		4	DD03
DD13	5		6	DD04
DD14	7		8	DD05
DD15	9		10	DD06
CS1#	11		12	DD07
DMA ACK#	13		14	CS0#
DMA_RQ	15		16	D IOR#
PDIAG#	17		18	D IOW#
IRQ15	19		20	VCC (+5V)
VCC (+5V)	21		22	VCC (+5V)
GND	23		24	GND
RESET#	25		26	GND
C Select	27		28	DA02
DA01	29		30	DASP#
DA00	31		32	I/ORDY#
DD00	33		34	DD08
DD01	35		36	DD09
DD02	37		38	DD10
IOCS16#	39		40	GND

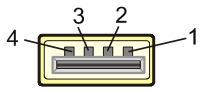


Active Low

D.11 J18, USB CONNECTORS (FACE PLATE)

Signal	Pin
VCC	1
DATA-	2
DATA+	3
GND	4

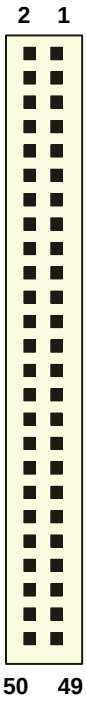
Front View



D.12 J19, MEZZANINE (PCI)

Pin Number	Signal
P64_IRQ7	2
VCC	4
P64_IRQ6	6
VCC	8
VCC	10
IDEACTP#	12
PDCS#1	14
PDA0	16
PDA1	18
IDE_IRQ14	20
PDDACK#	22
PIORDY	24
PDIOR#	26
PDIOW#	28
PDREQ	30
VCC	32
PDD0	34
PDD1	36
PDD2	38
PDD3	40
PDD4	42
PDD5	44
PDD6	46
PDD7	48
IDE_PCIRST#	50

Top View



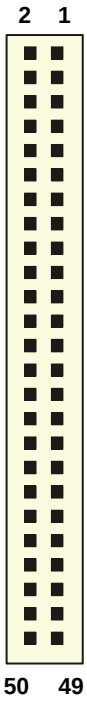
Pin Number	Signal
1	P64_IRQ9
3	P64_IRQ8
5	P64_IRQ5
7	P64_IRQ4
9	PCIRST#
11	GND
13	PDCS#3
15	PDA2
17	P66DETECT
19	SERR#
21	GND
23	ENUM#
25	M66EN
27	PERR#
29	GND
31	GND
33	PDD15
35	PDD14
37	PDD13
39	PDD12
41	PDD11
43	PDD10
45	PDD9
47	PDD8
49	GND

Active Low

D.13 J20, MEZZANINE (64-BIT/66MHZ)

Pin Number	Signal
AD3	2
AD1	4
GND	6
ACK64#	8
C/BE#4	10
C/BE#6	12
AD63	14
AD61	16
AD59	18
GND	20
AD57	22
AD55	24
AD53	26
AD51	28
AD49	30
AD47	32
GND	34
AD45	36
AD43	38
AD41	40
AD39	42
AD37	44
AD35	46
GND	48
AD34	50

Top View



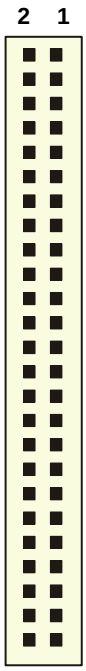
Pin Number	Signal
1	AD2
3	AD0
5	REQ64#
7	C/BE#7
9	C/BE#5
11	PAR64
13	GND
15	AD62
17	AD60
19	AD58
21	AD56
23	AD54
25	AD52
27	GND
29	AD50
31	AD48
33	AD46
35	AD44
37	AD42
39	AD40
41	GND
43	AD38
45	AD36
47	AD33
49	AD32

Active Low

D.14 J23, MEZZANINE (64-BIT/66MHZ)

Pin Number	Signal
2	AD3
4	AD1
6	GND
8	ACK64#
10	C/BE#4
12	C/BE#6
14	AD63
16	AD61
18	AD59
20	GND
22	AD57
24	AD55
26	AD53
28	AD51
30	AD49
32	AD47
34	GND
36	AD45
38	AD43
40	AD41
42	AD39
44	AD37
46	AD35
48	GND
50	AD34

Top View



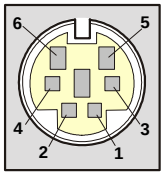
Pin Number	Signal
1	AD30
3	GND
5	CLKOUT2
7	GND
9	CLKOUT3
11	GND
13	CLKOUT1
15	GND
17	AD20
19	AD18
21	AD22
23	AD16
25	FRAME#
27	TRDY#
29	STOP#
31	PAR
33	AD15
35	GND
37	AD13
39	AD11
41	AD9
43	C/BE#0
45	AD6
47	AD4
49	

Active Low

D.15 J21, PS/2 MOUSE & KEYBOARD

Signal	Pin
KDATA	1
MDATA	2
GND	3
VCC	4
KBCLK	5
MCLK	6

Front View

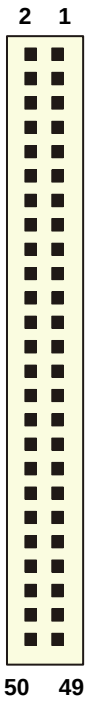


(Connector front view)

D.16 J22, MEZZANINE HA CONNECTOR

Pin Number	Signal
2	EN+GLAN
4	IPMB0_SDA
6	MS_HEALTHY#8
8	MS_HEALTHY#4
10	MS_PCI_RST#4
12	MS_BD_SEL#4
14	MS_HEALTHY#3
16	MS_PCI_RST#3
18	MS_BD_SEL#3
20	VCC3
22	P64GNT#1
24	VCC3
26	P64REQ#1
28	MS_HEALTHY#2
30	MS_PCI_RST#2
32	MS_BD_SEL#2
34	LAN2_ACT
36	LAN2_LINK
38	GND
40	RD-GLAN2_MEZ
42	RD+GLAN2_MEZ
44	GND
46	RD-LAN2_MEZ
48	RD+LAN2_MEZ
50	GND

Top View



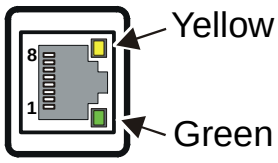
Pin Number	Signal
1	MS_PCI_RST#8
3	MS_BD_SEL#8
5	MS_HEALTHY#7
7	MS_PCI_RST#7
9	MS_BD_SEL#7
11	MS_HEALTHY#6
13	MS_PCI_RST#6
15	MS_BD_SEL#6
17	P64REQ#2
19	P64GNT#2
21	VCC3
23	P64GNT#3
25	VCC3
27	MS_HEALTHY#5
29	MS_PCI_RST#5
31	MS_BD_SEL#5
33	P64REQ#3
35	IPMB0_SCL
37	GND
39	TD-GLAN2_MEZ
41	TD+GLAN2_MEZ
43	GND
45	TD-LAN2_MEZ
47	TD+LAN2_MEZ
49	GND

Active Low

D.17 J24, ETHERNET 1 AND 2

Signal	
TX+	1
TX-	2
RX+	3
Not Connected	4
Not Connected	5
RX-	6
Not Connected	7
Not Connected	8

Top View

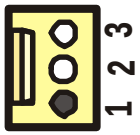


Note
These two LEDs might be reversed.

D.18 J25, HOT SWAP SWITCH

Signal	Pin
VCC3E	1
SW_OPEN#	2
GND	3

Top View



D.19 SW1 – RESET SWITCH

Signal	Pin
RESET#	1
GND	2

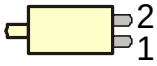
Side View



D.20 SW2 – NMI SWITCH

Signal	Pin
GND	1
NMI#	2

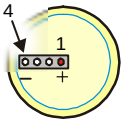
Side View



D.21 BT1, CMOS BATTERY BACKUP CONNECTOR

Signal	Pin
Battery (+)	1
Battery (-)	4

Front View



E. BIOS SETUP ERROR CODES

E.1 POST BEEP

Recoverable POST Errors
Whenever a recoverable error occurs during POST, *Phoenix* BIOS displays an error message describing the problem.
Phoenix BIOS also issues a beep code (one long tone followed by two short tones) during POST if the video configuration fails (no card installed or faulty) or if an external ROM module does not properly checksum to zero.
An external ROM module (e. g. VGA) can also issue audible errors, usually consisting of one long tone followed by a series of short tones.

Terminal POST Errors
There are several POST routines that issue a **POST Terminal Error** and shut down the system if they fail. Before shutting down the system, the terminal- error handler issues a beep code signifying the test point error, writes the error to port 80h, attempts to initialize the video, and writes the error in the upper left corner of the screen (using both mono and color adapters).
The routine derives the beep code from the test point error as follows:

1. The 8- bit error code is broken down to four 2- bit groups (Discard the most significant group if it is 00).
2. Each group is made one- based (1 through 4) by adding 1.
3. Short beeps are generated for the number in each group.

Example:
Testpoint 01Ah = 00 01 10 10 = 1- 2- 3- 3 beeps

Test Points and Beep Codes
At the beginning of each POST routine, the BIOS outputs the test point error code to I/ O address 80h. Use this code during trouble shooting to establish at what point the system failed and what routine was being performed.
If the BIOS detects a terminal error condition, it halts POST after issuing a terminal error beep code (See above) and attempting to display the error code on upper left corner of the screen and on the port 80h LED display.
If the system hangs before the BIOS can process the error, the value displayed at the port 80h is the last test performed. In this case, the screen does not display the error code.

E.2 POST MESSAGES

During the Power On Self Test (POST), if the BIOS detects an error requiring you to do something to fix, it will either sound a beep code or display a message.

If a message is displayed, it will be accompanied by:

"PRESS F1 TO CONTINUE, DEL TO ENTER SETUP".

E.3 ERROR MESSAGES

One or more of the following messages may be displayed if the BIOS detects an error during the POST.

CMOS BATTERY HAS FAILED

1. If it's the first boot, check for the onboard battery jumper W3. The board is shipped with W3 jumper set to OFF (onboard battery disconnected). This jumper must be shorted (ON) for proper battery operation.
2. CMOS battery is no longer functional. It should be replaced.

CMOS CHECKSUM ERROR

Checksum of CMOS is incorrect. This indicates that CMOS has become corrupt. This error may have been caused by a weak battery. Check the battery and replace if necessary.

DISK BOOT FAILURE, INSERT SYSTEM DISK AND PRESS ENTER

No boot device was found. This could mean either a boot drive was not detected or the drive does not contain proper system boot files. Insert a system disk into Floppy Drive A and press Enter. If you assumed the system would boot from the hard drive, make sure the controller is inserted correctly and all cables are properly attached. Also be sure the disk is formatted as a boot device. Then reboot the system.

KEYBOARD ERROR OR NO KEYBOARD PRESENT

Cannot initialize the keyboard. Make sure the keyboard is attached correctly and no keys are being pressed during the boot.

If you are purposely configuring the system without a keyboard, set the POST Errors halt condition in Setup to Disabled. This will cause BIOS to ignore all warning errors and continue the boot.

OFFENDING SEGMENT

This message is used in conjunction with the I/O CHANNEL CHECK and RAM PARITY ERROR messages when the segment that has caused the problem cannot be isolated.

PRESS F1 TO DISABLE NMI, F2 TO REBOOT

When BIOS detects a Non Maskable Interrupt condition, this will allow you to disable the NMI and continue to boot, or you can reboot the system with the NMI enabled.

F. BIOS UPDATE & EMERGENCY PROCEDURE

For BIOS update, see the procedure included in our FAQ document than can be found on the FAQ section of the FTP site under FAQ # KC_0028 at location:

ftp://ftp.kontron.ca/Support/Support_FAQ - Questions & Answers/

EMERGENCY PROCEDURE

Symptoms:

- No POST code on a power up (when using a POST card).

- Board does not boot, even after usual hardware and connection verifications.

- At power up, there is floppy disk led activity, which is one sign that the BIOS as detected a corrupted BIOS CRC prior POST and got back automatically to Emergency Recovery Mode looking for the floppy Emergency disk.

Please visit our FTP site in order to get the latest “Emergency Recovery BIOS” for your board. The BIOS maybe found at:

Ftp://Ftp.Kontron.ca/Support/BIOS_Emergency/

The Emergency Recovery Procedure is included within the downloadable Zip file of the Emergency BIOS. The latest Emergency Recovery Procedure can be found on the FAQ section of the
FTP site under FAQ # KC_0028 at location:

ftp://ftp.kontron.ca/Support/Support_FAQ - Questions & Answers/

G. GETTING HELP

At Kontron, we take great pride in our customer's successes. We strongly believe in providing full support at all stages of your product development.

If at any time you encounter difficulties with your application or with any of our products, or if you simply need guidance on system setups and capabilities, you may contact our Technical Support department at:

CANADIAN HEADQUARTERS
Tel. (450) 437-5682
Fax: (450) 437-8053

If you have any questions about Kontron, our products, or services, visit our Web site at: www.kontron.com

You can also contact us at the following address:

Kontron Canada, Inc.
616 Curé Boivin
Boisbriand, Québec
J7G 2A7 Canada

LIMITED WARRANTY

Kontron, Inc, ("The seller") warrants its boards to be free from defects in material and workmanship for a period of two (2) years commencing on the date of shipment. The liability of the seller shall be limited to replacing or repairing, at the seller's option, any defective units. Equipment or parts, which have been subject to abuse, misuse, accident, alteration, neglect, or unauthorized repair are not covered by this warranty. This warranty is in lieu of all other warranties expressed or implied.

H. Returning Defective Merchandise

If your Kontron product malfunctions, please do the following before returning any merchandise:

1) Call our Technical Support department in Canada at (450) 437-5682. Make certain you have the following at hand:
   - The Kontron Invoice number
   - Your purchase order number
   - The serial number of the defective board.
2) Give the serial number found on the back of the board and explain the nature of your problem to a service technician.
3) If the problem cannot be solved over the telephone, the technician will further instruct you on the return procedure.
4) Prior to returning any merchandise, make certain you receive an RMA number from Kontron's Technical Support and clearly mark this number on the outside of the package you are returning. To request a number, follow these steps:
   - Make a copy of the request form on the following page.
   - Fill out the form and be as specific as you can about the board's problem.
   - Fax it to us.
5) When returning goods, please include the name and telephone number of a person whom we can contact for further explanations if necessary. Where applicable, always include all duty papers and invoice(s) associated with the item(s) in question.
6) When returning a Kontron board:
   i) Make certain that the board is properly packed: Place it in an antistatic plastic bag and pack it in a rigid cardboard box.
   ii) Ship prepaid to (but not insured, since incoming units are insured by Kontron):

Kontron, Inc.
616 Curé Boivin
Boisbriand, Québec
J7G 2A7 Canada

RETURN TO MANUFACTURER AUTHORIZATION REQUEST

Contact Name : _____

Company Name :_____

Street Address : _____

City : _____ Province/State: _____

Country : _____ Postal/Zip Code: _____

Phone Number : _____ Extension : _____

Fax Number : _____

Serial Number	Failure or Problem Description	P.O. # (if not under warranty)

Fax this form to Kontron's Technical Support department in Canada at (450) 437-8053