PCI-948

MOBILE PENTIUM II/III SBC

TECHNICAL REFERENCE MANUAL	Version 1.1 September 2000

Ref. : M948_TECH

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PCI-948 – Technical Reference Manual, Rev. 1.1

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(Québec) CANADA J7G 2A7

Optional

Name _____
Company _____
Address _____
_____

ADDITIONAL COMMENTS

FCC Compliance Statement

Warning

Changes or modifications to this unit not expressly approved by the party responsible for the compliance could void the user's authority to operate this equipment.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference, in which case the user will be required to correct the interference at his or her own expense.

European Statement

Warning

This is a class B product. If not installed in a properly shielded enclosure, and used in accordance with the instruction manual, this product may cause radio interference in which case the user may be required to take adequate measures at his or her own expense.

Safety Standard

UL Recognized Component, File # E186339 Vol. 1 Section 2

Care and handling precautions for Lithium batteries

- Do not short circuit
- Do not heat or incinerate
- Do not charge
- Do not deform or disassemble
- Do not apply solder directly
- Do not mix different types or partially used batteries together
- Always observe proper polarities

READ ME FIRST

Your computer board has a standard non-rechargeable lithium battery. To preserve the battery lifetime, **the battery enable jumper is removed when you receive the board**. If you do not have any jumper cap, we suggest you to use the Watchdog Timer jumper cap.

EXERCISE CAUTION WHILE REPLACING LITHIUM BATTERY

WARNING

Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.

ATTENTION

Il y a danger d'explosion s'il y a remplacement incorrect de la batterie.

Remplacer uniquement avec une batterie du même type ou d'un type équivalent recommandé par le fabricant. Mettre au rebut les batteries usagées conformément aux instructions du fabricant.

ACHTUNG

Explosionsgefahr bei falschem Batteriewechsel. Verwenden Sie nur die empfohlenen Batterietypen des Herstellers. Entsorgen Sie die verbrauchten Batterien laut Gebrauchsanweisung des Herstellers.

ATENCION

Puede explotar si la pila no este bien reemplazada.

Solo reemplazca la pila con tipas equivalentes segun las instrucciones del manifacturo. Vote las pilas usadas segun las instrucciones del manifacturo.

POWERING-UP THE BOARD

If you should encounter a problem, verify the following items:

Make sure that all connectors are properly connected.

Check your boot diskette.

If the board still does not start up properly, you should try booting your system with the PCI-948 installed in the system, a monitor and a mouse connected to the board. This is the minimum required to verify the board's operation.

If you still are not able to verify your board, please refer to the emergency Procedure in the Appendix Section.

If you still are not able to get your board up and running, contact our Technical Support department for assistance.

PREVENTING VIRUSES

Teknor Applicom Inc. takes every precaution against computer viruses. For your protection, we have *safely sealed* all utility compact disks. If the seal is broken, **do not use the diskette**. Contact our Technical Support department for further instructions at (450) 437-5682 (Canada).

To safeguard against computer viruses in general, do not freely lend your utility diskettes and regularly perform virus scans on all your computer systems.

ADAPTER CABLES

While adapter cables are provided from various sources, the pinout is often different. The direct crimp design offered by Teknor allows the simplest cable assembly. All cables are available from Teknor Sales Department.

UNPACKING AND SAFETY PRECAUTIONS

STATIC ELECTRICITY

Since static electricity can cause damage to electronic devices, the following precautions should be taken:

1. Keep the board in its anti-static package, until you are ready to install it.
2. Always touch a grounded surface or wear a grounding wrist strap before removing the board from its package; this will discharge any static electricity that may have built up in your body.
3. Handle the board by the edges.

Storage Environment

Electronic boards are sensitive devices. Do not handle or store devices near strong electrostatic, electromagnetic, magnetic or radioactive fields.

Power Supply

Before any installation or setup, ensure that the board is unplugged from power sources or subsystems.

Unpacking

Follow these recommendations while unpacking:

1. After opening the box, save it and the packing material for possible future shipment.
2. Remove the board from its anti-static wrapping and place it on a grounded surface.
3. Inspect the board for damage. If there is any damage or missing items, notify Teknor immediately.

When unpacking you will find:

1. One PCI-948 SBC.
2. One Quick Reference sheet
3. One CDROM containing drivers.

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PART 1

1. PRODUCT DESCRIPTION

1. PRODUCT OVERVIEW
2. PCI-948 SBC TECHNICAL SPECIFICATIONS
3. POWER REQUIREMENTS

1.1. Product Overview

The PICMG compliant PCI-948 PCI/ISA Single Board Computer (SBC) is built around a Pentium®II processor running at 333 MHz, or a Pentium®III processor running either at 400 or 500 MHz. All three processors come in a Low-Power mini-cartridge package, optimizing highest performance, low-power requirement, small packaging, and long term reliable service.

The PCI-948 SBC offers the superior performance of the P6 micro-architecture meeting the unique low-power consumption and smaller package requirements of the embedded application market.

It features:

- Support for the Pentium® II processor – Low-Power 333MHz with on die 256KB 64-bit wide SPB non-blocking ECC L 2 cache
- Support for the Pentium® III processor – Low-Power 400 and 500MHz with on die 256KB 64-bit wide SPB non-blocking ECC L2 cache (advance transfer cache in the case of CuMine processors)
- CPU temperature monitoring
- Low-Power mini-cartridge package
- Intel 82440BX AGPset
- Up to 1 Gig of SDRAM distributed on four 168-pin DIMM sockets
- CPU Front Side Bus operating at 66Mhz in the Pentium® II processor and at 100 MHz in the Pentium® III processor
- Dual PCI EIDE Ultra DMA/33 interface
- Floppy disk interface supporting 360Kb to 1.44Mb format
- Two High 10Base-T/100Base-TX Ethernet controllers (Intel 82559), one supporting Wake-On-LAN
- Onboard CompactFlash™ disk support
- Two USB 1.1 ports with optional cable/assembly bracket
- Two serial ports, one parallel port, speaker port, mouse port and keyboard port
- Supports ATX power supply with SMI/SMM and ACPI power management capabilities allowing for Wake-On-LAN, Ring or Timer implementation
- Two-stage watchdog timer and power fail circuit
- System hardware monitor for voltages, temperature, fan speed and “cover open” discrete inputs accessible via on-board SMBus
- Award Elite BIOS in Boot Block Flash with recovery code
- High-performance 64-bit frame AGP video with 2MB SDRAM video memory
- Compatible with CGA, EGA, Hercules, MDA, VGA, SVGA, XGA, and SXGA

1.2. PCI-948 SBC Technical Specifications

FEATURES	DESCRIPTIONS
CPU	• Pentium II processor – Low-Power 333 MHz • Pentium III processor Low-Power 400MHz and 500MHz
Chipset	• Intel 440BX AGPset.
Cache	• 16K/16K Instruction / Data CPU-internal Level 1 • 256KB 64-bit wide on-die Level 2 pipelined burst
Memory	• Four 168-pin latching DIMM sockets, 64/72-bit • Up to 1GB of SDRAM with parity or ECC (for single bit error correction and double bit error detection)
Data Path	• 64-bit between CPU and memory • 32-bit on local PCI and AGP bus. • 16-bit on the ISA bus
Bus Interfaces	• Front Side Bus 66MHz/100MHz determined by CPU • AGP Bus, 32-bit 66MHz • PCI Bus, 32-bit 33MHz • ISA Bus, 16-bit 8MHz • PC/104-Plus (embedded PCI) • PCI-to-ISA non-transparent bridge; Intel's 82371AB • SMBus (for system management of CPU temperature monitoring, DRAM control, Clock buffers and power control)
Interrupts	• 11 edge/level sensitive and configurable • 4 PCI level sensitive, configurable to any interrupt vector for PnP compatibility
DMA Channels (ISA)	▪ Four 8-bit, three 16-bit ▪ Supports scatter / gather, Fast Type-F DMA
Flash Memory	• 256KB for BIOS field upgrade • Silicon Serial ID TAG for unique board identification accessible via software
Video	• 32-bit AGP video controller (Intel 69000) with 2MB on die 83MHz SDRAM video memory • CRT resolutions up to 1280x1024x256 colors
Clock/Calendar	• Real-time clock with (replaceable) battery backup • CMOS RAM

PCI-948 SBC Technical Specifications (continued)

FEATURES	DESCRIPTION
I/O	• SMC FDC37C672. • USB Ports : Two. • Serial Ports: Two (one RS-232, COM1, COM2 configurable as RS-232/422/485. • Parallel Port : One bi-directional with all IEEE 1284 protocols supported with BIOS selectable IRQs and addressing. • Floppy Disk: Support for two drives (360KB to 1.44MB). • EIDE: Two channels Bus Master PCI EIDE; support for two IDE drives (master/slave configuration); LBA, PIO Mode 0-4 and Ultra DMA/33. • CompactFlash™ Module: Optional bootable CompactFlash™ disk interfaces to secondary EIDE channel, user upgradeable, master/slave. • Ethernet: Two Intel 82559 Fast Ethernet controllers, PCI 10/100Base-TX ports. • PS/2 mouse, AT and PS/2 standard keyboard, speaker, reset switch and hard disk LED.
Parallel Port	• Supports multiple mode parallel port (Standard, IEEE 1284, SPP, EPP, and ECP); BIOS selectable IRQs and addressing.
BIOS Features	• Award Elite BIOS in Boot Block Flash with emergency recovery code; save CMOS in Flash option, and boot from LAN capability. • Auto configuration, extended setup. • CC000-E0000 address blocking; PnP tables. • Setup console redirection to serial port (VT100 mode) with CMOS setup access. • Software enable/disable of onboard Ethernet; hardware enable/disable of onboard video. • Diskless, keyboardless, and videoless operation extensions. • Batteryless operation with CMOS copy in flash BIOS. • System, video, and LAN BIOS shadowing system, video, LAN and option BIOS shadowing. • Programmable bus and I/0 speeds and memory wait states. • ATX support (software shut-down, Wake-on-LAN, Ring or Timer). • Advanced Configuration and Power Interface (ACPI 1.0), Advanced Power Management (APM 1.2), advanced thermal management (resume, overheat alarm and auto slow down), and Green support.

PCI-948 SBC Technical Specifications (continued)

FEATURES	DESCRIPTIONS
Supervisory	• Two-stage software programmable Watchdog timer drives NMI on first stage and system reset on second stage • Programmable CPU temperature monitor alarm • Power failure and voltage monitoring/low battery detector • LEDs: IDE activity, Ethernet activity and link status.
OS Compatibility	• MS-DOS™, Windows® 95/98, Windows® NT, VxWorks™, pSOS™, QNX™, Linux, and Solaris
PICMG compliance	• Mechanical : compliant to IEEE 1101.10; compliant to PICMG 2.0 Rev 2.1 and PICMG 2.0 R3.0 and PICMG 2.1
Form Factor	• 338 x 122 x 34 mm (13.32” x 4.80” x 1.35”)
Power Requirements	• Supply Voltages: +3.3V: ±5% +5V±5% +12V±5% • Supply Current * : 3.3V: 2.0 Amps Max 5V 5.5 Amps max. 12V: 0.75 Amps max. • Power Dissipation: 40W max. ** Pentium III processor Low-Power 500MHz with 512MB SDRAM.*
Environmental	**Operating** / **Storage and Transit** Temp.: 0-60°/32-140°F (w/ 150LFM airflow) / -40° to +70° / -40° to 158°F **When using a CompactFlash disk, must not exceed 50°C (0-50°C/32-122°C)** Humidity 5% to 95% @ 40°C/104°F non-condensing / 5% to 95% @ 40°C/104°F non-condensing Altitude 4,572m / 15,000ft Shock Designed to meet IEC 68-2-27 Vibration Designed to meet IEC 68-2-6
Reliability	• MTBF:> 100,000 hours 55°C/131°F (MIL-HDBK-217F) • Board serial number • USB, keyboard, mouse voltage protected by self-resetting fuses • 2 year limited warranty
Safety	• Designed to meet or exceed UL 1950; CSA C22.2 No 950; EN 60950; IEC950
EMI/EMC	• FCC 47 CFR Part 15/CISPR22, Class B; CE Mark to EN55022/EN50082

1.3. Power requirements

The power requirements for the PCI-948 are specified as follows:

CPU	Dixon 333	CuMine 400	CuMine 500
VCORE	1.6 V	1.35/1.6V	1.35/1.6V
Frequency (Int / Ext)	333 / 66	400 / 100	500 / 100
Power MAX 3.3V/5V/12V	22.7 / 18.8 / 0.5W	22.7 / 19.5 / 0.5W	22.7 / 27.5 / 0.5W
Power TYP 3.3V/5V/12V	15.8 / 16.35 / 0.5W	15.8 / 17.6 / 0.5W	15.8 / 22 / 0.5W
Power SUS 3.3V/5V/12V	11.5 / 11.05 / 0.5W	11.5 / 12.9 / 0.5W	11.5 / 14.65 / 0.5W
Ambient temp MAX	60°C	60°C	60°C
TEST CONDITIONS			
Power MAX	Running KPower in Windows		
Power TYP	Idle in Windows		
Power SUS	Suspend mode in Windows		
Test setup	64MB SDRAM, running Windows 98 with 3.2GB hard disk.		

Consumption 3.3V = max 4 X 256MB running SISOFT benchmark under Win98
Typ 1 X 128MB running SISOFT benchmark under win98
min 1 X 32MB DOS prompt

Take care to mention that the 3.3V power is not an addition of the 5V power, 3.3V is made from 5V. The total power needed by the Card is 5V + 12V.

PART 2

2. INSTALLING THE BOARD

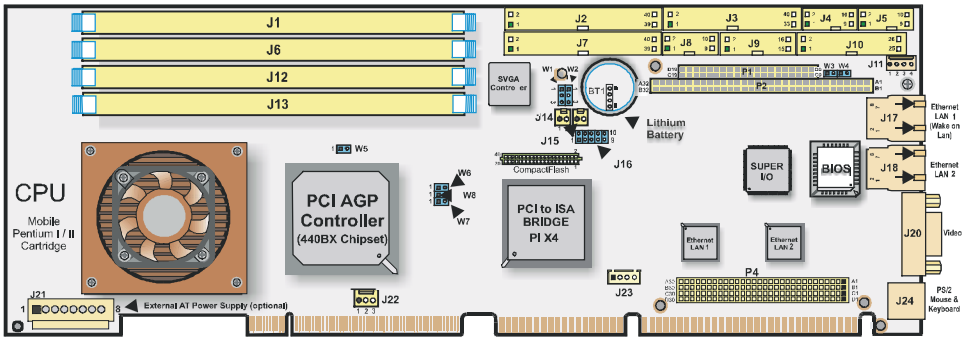
1. SETTING JUMPERS
2. REGISTER'S DESCRIPTION
3. ONBOARD INTERCONNECTIVITY
4. CUSTOMIZING THE BOARD

2.1. Setting Jumpers

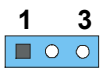
2.1.1 Jumper Description for the PCI-948 SBC

Description	Jumper Position		Designation
Power Fail Detection	1-2: User Defined	2-3: V Bat (3.08V)	**W1**
V Battery	1-2: Internal	2-3: External	**W2**
Serial Port 2 in RS-485 Mode line termination resistors	OUT: Line Termination Disabled	IN: Line Termination Enabled	**W3-W4**
VT-100 Mode: allows remote terminal connection to serial port	OUT: Disabled	IN: Enabled	**W6**
CompactFlash Configuration	OUT: Slave	IN: Master	**W7**
Front Side Bus Speed	OUT: CPU Selected	IN: Forced 66Mhz	**W8**

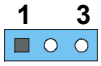
2.1.2 PCI-948 Connector and Jumper Location



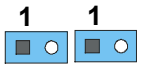
2.1.3 Jumper Configuration (Default Settings= *)



W1 - Power Fail Detection	
User Defined (Note 1)	1-2
*VBAt (3.08V)	2-3



W2 - Battery Source	
Internal	1-2
* External	2-3



W3, W4 - COM2 Terminations		
RS-422/485 modes only	W3	W4
With termination resistors	In	In
* Without termination resistors	Out	Out



W5 - Video Enable	
* Enable	Out
Disable	In



W6 - VT-100 User Defined	
* Disable - Level 1	Out
Enable - Level 0	In



W7 - CompactFlash Disk	
* Slave	Out
Master	In



W8 - Bus Speed	
* 66/100 MHz (from CPU0)	Out
66 MHz	In

Note 1
To prevent the board from spurious PFI (Power Fail Interrupt), the jumper cap must always be installed at either 1-2 or 2-3 position.

2.2. Register's Description

Although base address of Supervisor I/O register is shown here at 0x190, it can be programmed at 0x290 or 0x390.

2.2.1 Serial Port 2 Configuration

FPGA	Address	D7	D6	D5	D4	D3	D2	D1	D0
READ	0x190*	NU	NU	NU	RS485	RS232	ST1	NU	NU
WRITE	0x190*	NU	NU	NU	RS485	RS232	ST1	NU	NU

ST1	Enable RTS2 to be used as 485TX ENABLE when in 485 mode.
RS232	Enable uart2 RS232 operation.
RS485	Enable uart2 RS422 & 485 operation.
NU	Reserved.

The serial port 2 mode can be controlled by setting three bits. Here are the possibilities.

Mode	Bit RS485	Bit RS232	Bit ST1
RS-232	1	0	X*
RS-422	0	1	0
RS-485	0	1	1

** Do not care.*

2.2.2 History and Monitor Status

FPGA	Address	D7	D6	D5	D4	D3	D2	D1	D0
READ	0x191*	PBRST	NU	WDO	CPUFLT	NU	NU	NU	NU
WRITE	0x191*	NU	NU	NU	CPUFLT	NU	NU	NU	NU

PBRST	When high, indicates that the last system reset was caused by push button reset switch.
WDO	When high, indicates that the last system reset was caused by watchdog time out.
CPUFLT	When low, signals a CPU thermal alarm to the outside world on the system monitor connector. On some boards, this bit also read the old download jumper now known as reserved jumper. On some boards using high drive ISA buffer, this bit is used to control the 15-16M-memory hole.
NU	Reserved.

2.2.3 History Status

FPGA	Address	D7	D6	D5	D4	D3	D2	D1	D0
READ	0x192*	NU	NU	NU	NU	NU	WD_LOCK	NU	CLRHIS
WRITE	0x192*	NU	NU	NU	NU	NU	WD_LOCK	NU	CLRHIS

CLRHIS	When low, clear all history bits.
WD_LOCK	When high, locks the state of the enable bit for the digital watchdog.
NU	Reserved

2.2.4 Monitoring Status and I/O Access

FPGA	Address	D7	D6	D5	D4	D3	D2	D1	D0
READ	0x193*	APPFLT	GPIO2	GPIO1	NU	IDCHIP	VGA_INT	I2C_CLK	I2C_DATA
WRITE	0x193*	APPFLT	GPIO2	GPIO1	NU	IDCHIP	VGA_INT	I2C_CLK	I2C_DATA

I2C_DATA	I2C data.
I2C_CLK	I2C Clock.
IDCHIP	One-wire clock/data for silicon ID chip.
GPIO_1	General purpose I/O.
GPIO_2	General purpose I/O.
APPFLT	When low, signals an application fault to the outside world on the system monitor connector.
VGA_INT	Enable/Disable Video refresh interrupt.
NU	Reserved.

2.2.5 Registers 0x194 and 0x195

These registers are reserved.

2.2.6 Digital Watchdog

FPGA	Address	D7	D6	D5	D4	D3	D2	D1	D0
READ	0x196*	WDEN	WDD2	WDD1	WDD0	NU	NU	NU	NU
WRITE	0x196*	WDEN	WDD2	WDD1	WDD0	NU	NU	NU	NU

WDEN	Enable/disable digital watchdog.
WDD[2..0]	Duration of digital watchdog.
NU	Reserved.

The digital watchdog duration can be controlled in the following way.

WDD[2..0]	NMI(T)	RESET(T)
000	16T	NMI+T
001	64T	NMI+T
010	256T	NMI+T
011	1024T	NMI+T
100	4096T	NMI+T
101	16384T	NMI+T
110	65536T	NMI+T
111	262144T	NMI+T

Timeout selection with T = 1ms (TBC)

2.2.7 NMI Control

FPGA	Address	D7	D6	D5	D4	D3	D2	D1	D0
READ	0x197*	BATFEN	BATFLT	FANFEN	FANFLT	EXTFEN	EXTFLT	WDNMIEN	WDNMI
WRITE	0x197*	BATFEN	NU	FANFEN	NU	EXTFEN	NU	WDNMIEN	NU

WDNMI	When high, signal NMI from watchdog timeout.
WDNMIEN	Enable NMI generation from digital watchdog.
EXTFLT	When high, signal NMI from external source on monitor connector.
EXTFEN	Enable NMI generation from external source.
FANFLT	When high, signal NMI from external fan motion detector on monitor connector.
FANFEN	Enable NMI generation from fan fault on monitor connector.
BATFLT	When high, signal NMI from local RTC battery monitor.
BATFEN	Enable NMI generation for bat fault.
NU	Reserved.

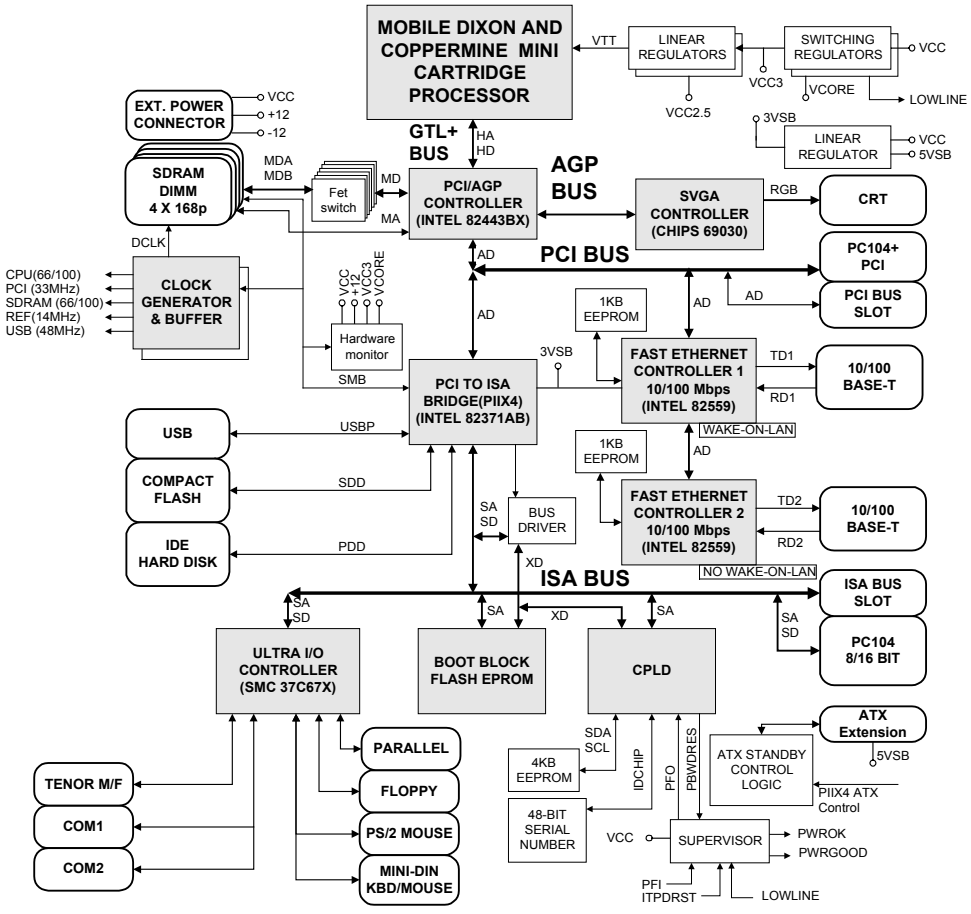
2.2.8 Register Bits Position (Summary)

CPLD	Address	D7	D6	D5	D4	D3	D2	D1	D0
READ	0x190*	NU	NU	NU	RS485	RS232	ST1	NU	NU
WRITE	0x190*	NU	NU	NU	RS485	RS232	ST1	NU	NU
READ	0x191*	PBRST	NU	WDO	CPU_FLT	NU	NU	NU	NU
WRITE	0x191*	NU	NU	NU	CPU_FLT	NU	NU	NU	NU
READ	0x192*	NU	NU	NU	NU	NU	WD_LOCK	NU	CLRHIS
WRITE	0x192*	NU	NU	NU	NU	NU	WD_LOCK	NU	CLRHIS
READ	0x193*	APP_FLT	GPIO_2	GPIO_1	STANDBY	IDCHIP	VGA_INT	I2C_CLK	I2C_DATA
WRITE	0x193*	APP_FLT	GPIO_2	GPIO_1	STANDBY	IDCHIP	VGA_INT	I2C_CLK	I2C_DATA
READ	0x194*	NU	NU	NU	NU	NU	NU	NU	NU
WRITE	0x194*	NU	NU	NU	NU	NU	NU	NU	NU
READ	0x195*	NU	NU	NU	NU	NU	NU	NU	NU
WRITE	0x195*	NU	NU	NU	NU	NU	NU	NU	NU
READ	0x196*	WDEN	WDD2	WDD1	WDD0	NU	NU	NU	NU
WRITE	0x196*	WDEN	WDD2	WDD1	WDD0	NU	NU	NU	NU
READ	0x197*	BAT_FLT_EN	BAT_FLT_STATUS	FAN_FLT_EN	FAN_FLT_STATUS	EXT_FLT_EN	EXT_FLT_STATUS	WDNMIEN	WDNMI
WRITE	0x197*	BAT_FLT_EN	NU	FAN_FLT_EN	NU	EXT_FLT_EN	NU	WDNMIEN	NU

- The base address for the Supervisor I/O Register, which is used for such functions as power fail detection and the watchdog timer can be set to 190h, 290h, and 390h (see *Chipset Features Setup*).

2.3. Onboard Interconnectivity

2.3.1 PCI-948 Block Diagram



2.3.2 Mobile Pentium® II / III Processor

Peripheral processor supports the Intel's Low-Power 333MHz Pentium® II, the low power 400MHz Pentium® III as well as the Low-Power 500MHz Pentium® III processor (higher clock speeds will be available when Intel releases the corresponding parts).

It consists of a Pentium® II / III processor core with an integrated second level cache of 256KB (on-die, full CPU speed, ECC capable) and a 64-bit high-performance 66/100MHz front side bus.

The processor interfaces to the 440BX AGPset through the 64-bit low-power GTL + data bus interface.

2.3.3 North Bridge Chipset

This chipset consist of 443BX AGPset, 64/72-bit SDRAM data interface with ECC support, Low-Power GTL Bus, five PCI arbitration channels, PCI bus rev. 2.1, Accelerated Graphics Port Interface (AGP). The bus is optimized for 100MHz operation.

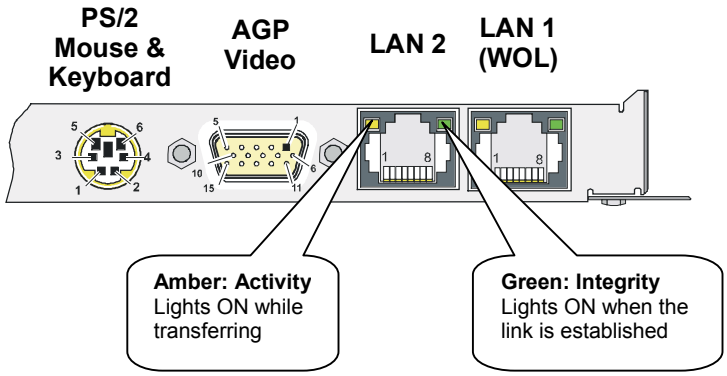
2.3.4 82371AB PCI-to-ISA Bridge / IDE Xcelerator (PIIX4E)

This Multifunction PCI-to-ISA bridge supports PCI 2.1, full ISA (EIO) Bus, 3.3V operation with 5V tolerant buffers. It provides the PCI-948 SBC with an IDE interface for up to four drives with Bus Mastering IDE, Transfer, each with independent timing and UDMA/33 capabilities. The 82371AB (PIIX4E) also supports ACPI Power Management functions and OS Directed Power Management. In addition it provides two 82C37 DMA Controllers, a 15 Interrupt Controller (two 82C59), two USB 1.1 Ports, a System Management Bus (SMB) and support for other peripherals like standard Serial and Parallel Ports, Floppy Drives, Mouse and Keyboard through the FDC37C627 super I/O controller.

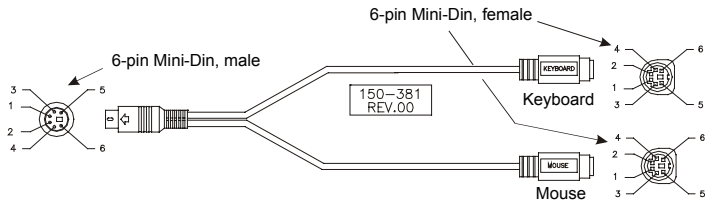
2.3.5 Onboard Connectors and Headers

Description	Comments	
DIMM Sockets	J1/J6 J12/J13	Supports 168-pin 64/72-bit DIMMs, up to 1GB of RAM
IDE	J2	Primary IDE connector
Floppy Disk	J3	
Serial Port 1	J4	NS16C550, RS-232, 9-pin DSUB connector
Serial Port 2	J5	NS16C550, configurable as RS-232, RS-422, RS-485, 9-pin DSUB connector
IDE	J7	Secondary IDE connector
USB	J8	USB 1.1 UHCI
Keyboard	J9	Keyboard/Speaker
Parallel Port	J10	Multimode IEEE 1284, EPP, ECP
Mouse	J11	PS/2 Mouse
Ethernet 1	J17	100/10 Base-T, RJ-45 with link and activity LED, Wake-On-LAN
Ethernet 2	J18	100/10 Base-T, RJ-45 with link and activity LED
CPU	J19	Pentium II/III mini-cartridge 240-pin PBGA
SVGA	J20	Standard 15-pin DSUB female connector
Ext Power	J21	External Power connector
Fan Header	J22	+12V DC CPU fan power supply
ATX Extension	J23	ATX Power Management: 5VSB, PW-OK, PS-ON
Keyboard/Mouse	J24	Mini-DIN Keyboard/Mouse connector
PCI Bus Slots	J25/J30	
ISA Bus Slots	J26 to J29	
Battery	BT1	CMOS backup battery connector.
External Battery	J14	≈ 3.6V
CompactFlash	P3	Industry-standard ATA/IDE subsystem for application, data, image, and audio storage connector

2.3.6 Front Plate Connectors and Indicators



Connector/Indicator	Description	Comments
DS (Amber)	Activity indicator	When lit, indicates that the data are being transferred
DS (Green)	Integrity indicator	When lit, indicates that the link is established
J17	Ethernet 1	RJ-45 connectors with built-in activity and link indicators
J18	Ethernet 2	RJ-45 connectors with built-in activity and link indicators
J20	VGA Video	Standard 15-pin DSUB female connector
J24	Keyboard and Mouse	To connect a keyboard and/or a mouse through this connector. If you wish to connect both a mouse and a keyboard, you need a Y shaped splitter cable (Teknor part number 150-381)



2.4. Customizing the Board

2.4.1 Processor

The PCI-948 SBC is shipped with the Mobile Pentium® II processor 333MHz or Pentium® III processor, Low-Power 400/500MHz is equipped with a passive heat sink that provides adequate cooling in a 150LFM airflow environment.

CAUTION

Since CPUs are very sensitive components, particular attention should be given while installing a processor on the board. Improper installation may damage the board and/or the CPU

Before installing a processor on your board, **you must contact our Technical Support** for the installation procedure

2.4.2 Backup Battery

An onboard 3.6V lithium battery is provided to backup BIOS setup values and the real time clock (RTC).

When replacing the battery, it must be connected as follows:

- Connect the battery to the BT1 header. The positive terminal of the battery holder is located at the bottom center.

WARNING

Danger of explosion if battery is incorrectly replaced

Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.

2.4.3 Installing the Memory

2.4.3.1. SDRAM System Memory

The PCI-948 SBC supports four industry standard 168-pin DIMMs (Dual In-Line Memory Module) sockets for memory configuration from 8MB to 1GB of Synchronous DRAM.

The memory characteristics must conform to the following:

- 1.15 inch height, 168-pin DIMM
- Standard 3.3V only,
- 64-bit and 72-bit modules, single-sided or double-sided
- Unbuffered 100MHz (SDRAM),
- Serial Presence Detect (SPD) EEPROM,
- Errors Checking and Correction (ECC) capabilities or parity bit with 72-bit modules,
- Compliant with Intel's PC SDRAM Unbuffered DIMM Specification (100MHz) Rev. 1.0.

At least 8MB of memory must be installed on the board for proper operation. Modules can be installed in any socket and order. The total system memory is equal to the sum of the memory module size installed in the four DIMM sockets.



NOTE

When populating with more than one memory module, each socket must be installed with the same memory type (64/72-bit), however the capacity of each module may be different from the other. The BIOS will take the less common denominator.

The recommended DIMM devices are listed in the table below.

Vendor's part number	DIMM's description	Vendor's Name
CTK32M/P100S	ECC SDRAM 32MB 4M*72 PC100 1.15"HT	CENTON
4X72CQ2X8S4E	ECC SDRAM 32MB 4M*72 PC100 1.15"HT	ROCKY MOUNTAIN RAM
DIM-200472V2S08G1	ECC SDRAM 32MB 4M*72 PC100 1.15"HT	SHIKATRONICS
DIM200472V5S08G	ECC SDRAM 32MB 4M*72 PC100 1.15"HT	SHIKATRONICS
CTK64M/P100S	ECC SDRAM 64MB 8M*72 PC100 1.15"HT	CENTON
8X72PC8X8S4E	ECC SDRAM 64MB 8M*72 PC100 1.15"HT	ROCKY MOUNTAIN RAM
DIM200872V4S8G1	ECC SDRAM 64MB 8M*72 PC100 1.15"HT	SHIKATRONICS
CTK128M/P100S	ECC SDRAM 128MB 16M*72 PC100 1.15"	CENTON
DIM-201672V4S08G1	ECC SDRAM 128MB 16M*72 PC100 1.15"	SHIKATRONICS
VM374S1723-GL	ECC SDRAM 128MB 16M*72 PC100 1.15"	VIRTIUM
CFHKQARV4VU420G	ECC SDRAM 256MB 32M*72 PC100 1.15"	CENTON
CTK256M/P100S	ECC SDRAM 256MB 32M*72 PC100 1.15"	CENTON
DIM203272VDS08GS	ECC SDRAM 256MB 32M*72 PC100 1.15"	SHIKATRONICS
VM374S3323-GL	ECC SDRAM 256MB 32M*72 PC100 1.15"	VIRTIUM

2.4.3.2. DIMM Installation

To install the DIMMs in the sockets, proceed as follows:

1. With the board flat on a static-free surface, turn it so that the faceplate is facing right.
2. Hold the module vertically so that the bottom connector key is at right. Install the DIMM straight down into the DIMM socket. The socket's keys will ensure a correct mating.
3. Press firmly on the top edge of the memory module to engage it into the socket. The module is fully inserted when the retaining clips snap into notches located at each end of the module.

If necessary, work your way by inserting the other modules, one by one.

To remove the DIMMs from the sockets, pull simultaneously on the retaining clips located on each side of the socket. Once the module has snapped out, pull gently on it.

WARNING

Since static electricity can cause damage to electronic devices, the following precautions should be taken:

1. Keep the board in its anti-static package, until you are ready to install it.
2. Touch a grounded surface or wear a grounding wrist strap before removing the board from its package; this will discharge any static electricity that may have built up in your body.
3. Handle the board by the edges.

2.4.4 Supervisory Features

The PCI-948 SBC provides a set of programmable I/O registers to setup the Intel PIIX4E (I/O addresses 4030h to 4037h) and the XILINX FPGA (I/O addresses programmable at 190h-197h, 290h-297h or 390h-397h using the AWARD Chipset Features Setup).

Only register bits needed to program the power fail detection and watchdog functions are described below.

2.4.5 Power Fail Monitoring

The status of the power failure detector can be read from one bit of the system register located at the address n91h (n=1, 2, or 3) Bit 0. The detection conforms to the following conditions (* = active low signal):

It always monitors the +5V power supply. When it drops below 4.65V (typical), the system is reset.
It can monitor the onboard battery. When the battery is in a low condition (below 2.9V typical), the PFO* (power fail output) signal goes low. The status of the PFO* signal can be read at I/O address 4031h, bit 1 (0 = failed, 1 = good). An interrupt handler can then service the interrupt. If you choose not to generate a NMI, you can use an algorithm to detect a low-battery condition and respond accordingly.

For more information, contact the Technical Support department (see Appendix G)

2.4.6 Watchdog

The function of a watchdog is to reset the CPU board if the processor is not able to generate a trigger for longer than the watchdog time-out period. This feature is useful in embedded systems where human supervision is not required or impossible.

The PCI-948 SBC provides a two-stage digital watchdog with software programmable time-out period.

Following a reset of any source, the watchdog is disabled. The watchdog can be enabled by software.

2.4.6.1. Dual Stage Watchdog

Enabling the Programmable Watchdog

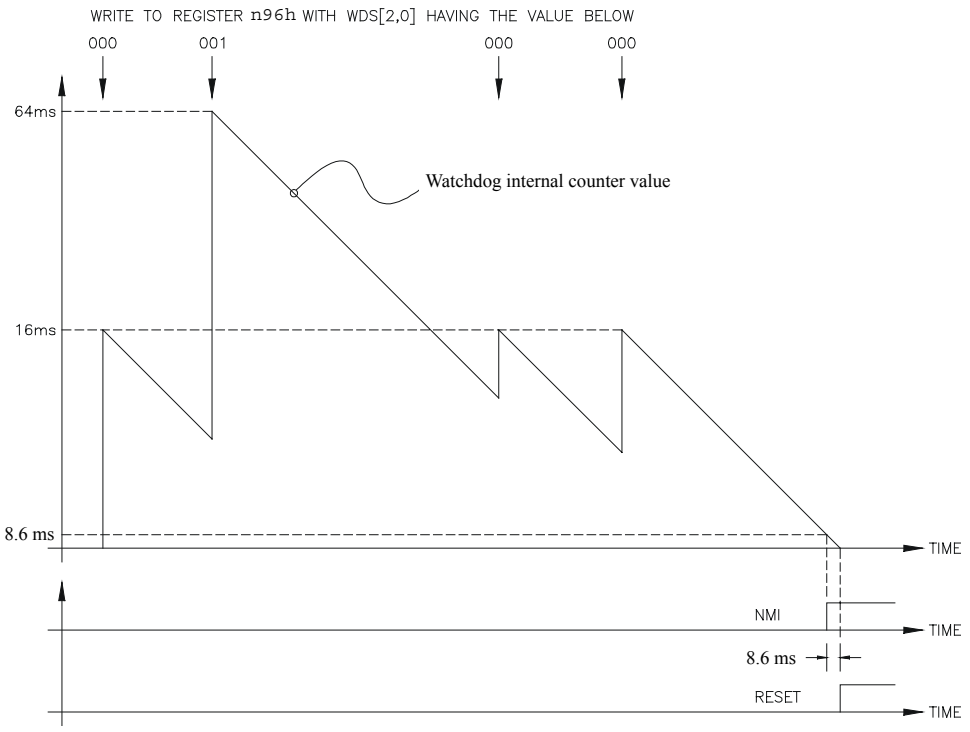
To enable the programmable watchdog, first unlock the enable bit by clearing the lock bit in register n92h (bit 2), then set the bit WDEN (bit 7) in register n96h and re-lock it by setting the lock bit in register n92h (bit 2). The following is an example in C language:

```
#define TekReg 0x190                    // define base address (0x190, 0x290 or 0x390)
void ArmWatchdog(void)
{
    outp(TekReg+2,  inp(TekReg+2) & 0xFB);     // unlock watchdog enable bit
    outp(TekReg+6,  inp(TekReg+6) | 0xF0);     // enable and trigger at max time-out
    outp(TekReg+2,  inp(TekReg+2) | 0x04);     // lock watchdog enable bit
}
```

Triggering the Programmable Watchdog

To trigger the programmable watchdog, the processor writes to register n96h (n=1, 2 or 3). The action of writing to the register is the trigger and the value written to the register tells the watchdog the current time-out to use (see register n96h description). For a fixed time-out, the software simply writes a constant in register n96h.

A variable refresh is possible as shown below:



The programmable watchdog can be viewed as a decrementing counter that is initialized by a write to register n96h (n = 1, 2 or 3). The processor must initialize the counter to prevent it from reaching count 0 (timeout).

The following C language procedure can be used to trigger the programmable watchdog.

```
#define TekReg 0x190                    // define base address (0x190, 0x290 or 0x390)
void TrigWatchdog(timeout)    // select timeout at runtime: 0x80 = 0.016s,
                               // 0x90 = 0.065s, 0xA0 = 0.261s, ...
{
   outp(TekReg+6,(inp(TekReg+6) & 0x0F) | (timeout & 0xF0));
}
```

Time-out

The programmable watchdog has two stages: the first stage has a variable time-out while the second stage has a fixed one.

The first stage time-out is chosen at runtime from eight preset values (see table below). The first stage time-out generates a NMI interrupt (if enabled in register n96h, bit 7). An appropriate NMI handler must be written, otherwise this will be treated as a parity error by the default BIOS NMI handler; see register n96h description for a suggestion on how to do this.
The second stage times-out 8.6ms ±10% (depending on the temperature) after the first one and generates a master reset.

WDD[2..0]	NMI(T)	RESET(T)
000	16T	NMI(T)+8T
001	64T	NMI(T)+8T
010	256T	NMI(T)+8T
011	1024T	NMI(T)+8T
100	4096T	NMI(T)+8T
101	16384T	NMI(T)+8T
110	65536T	NMI(T)+8T
111	262144T	NMI(T)+8T

Time-out selection with T = 1.08ms (TBC)

A reset from the programmable watchdog is latched for reset source identification.

2.4.7 Thermal Management

The thermal management is built around two digital temperature sensors and a thermal watchdog. Both devices can be programmed to set their outputs when the temperature of the processor or the ambient temperature exceeds a programmable high limit, and reset its output when the temperature is under a programmable low limit. A special routine is implemented to throttle the CPU clock until the temperature falls below the programmed low limit.

Please refer to Section 4.1.9 *CPU/Board Features Setup* for a complete information on thermal management setups.

2.4.8 Power Supply

When used as a stand-alone system, the PCI-948 must be powered through the J21 Power connector. When installed on a backplane, the power is drawn to the power lines connected to the ISA and PCI fingers of the edge connectors.

Related Jumpers
None

BIOS Settings
See Power Management options described in Section 4.1.7 *Power Management Setup.*

The power requirements are specified as follows:

CPU	Dixon 333	CuMine 400	CuMine 500
VCORE	1.6 V	1.35/1.6V	1.35/1.6V
Frequency (Int / Ext)	333 / 66	400 / 100	500 / 100
Power MAX 3.3V/5V/12V	22.7 / 18.8 / 0.5W	22.7 / 19.5 / 0.5W	22.7 / 27.5 / 0.5W
Power TYP 3.3V/5V/12V	15.8 / 16.35 / 0.5W	15.8 / 17.6 / 0.5W	15.8 / 22 / 0.5W
Power SUS 3.3V/5V/12V	11.5 / 11.05 / 0.5W	11.5 / 12.9 / 0.5W	11.5 / 14.65 / 0.5W
Ambient temp MAX	60°C	60°C	60°C
TEST CONDITIONS			
Power MAX	Running KPower in Windows		
Power TYP	Idle in Windows		
Power SUS	Suspend mode in Windows		
Test setup	64MB SDRAM, running Windows 98 with 3.2GB hard disk.		

PART 3

3. ONBOARD FEATURES

1. COMPACTFLASH INTERFACE
2. ENHANCED IDE INTERFACES
3. ETHERNET INTERFACES
4. FLOPPY DISK INTERFACE
5. PS/2 KEYBOARD AND MOUSE INTERFACE
6. PARALLEL PORT
7. POWER MANAGEMENT
8. THERMAL MANAGEMENT
9. SERIAL PORTS
10. USB INTERFACES
11. VIDEO INTERFACES
12. BATTERY

3.1. CompactFlash Interface

The PCI-948 board supports an IDE compatible flash disk by using a CompactFlash carrier module. CompactFlash (C-Flash) disks are the resident industry-standard ATA/IDE subsystem for application, data, image, and audio storage. They have the same functionality and capabilities as intelligent disk drives, but with the advantages of being very compact, rugged (typical M.T.B.F. is 1,000,000 hours) and low power. The PCI-948 supports all CompactFlash sizes presently available and future sizes when available.
The C-Flash disk connects on the PCI-948 via the onboard Flash Disk connector.

Related Jumpers
W7 to set the CompactFlash disk as secondary (IN) or slave (OUT).

BIOS Settings
Section 4.1.2 *Main Menu: IDE HDD Auto Detection* to set the type of hard disk.

The CompactFlash disk connects directly to the primary EIDE interface. It must be configured the same way as a standard hard disk using the BIOS setup program (Autodetect function).

To setup the CompactFlash disk for Master or Slave configuration, use the CompactFlash jumper (W7) located on the peripheral processor.

To locate and install this jumper, please refer to Section 2.1, *Setting Jumpers*.



NOTE

Since CompactFlash devices use the ATA/IDE interface, no specific flash disk driver is required for various operating systems.



NOTE

When using a CompactFlash disk, the operating temperature must not exceed 50°C (0-50°C/32-122°F).

3.2. Enhanced IDE Interfaces

Two IDE interfaces are provided to support up to four IDE devices, such as hard disks, CD-ROM, LS-120, ZIP drives, and CompactFlash. Connections are supported through a 40-pin dual row header.

Signal Paths

The primary IDE interface is available on the Primary (J2) and Secondary (J7) connectors, and on the Compact Flash (P3) connector.

Related Jumpers

None

BIOS Settings

Section 4.1.10 *Integrated Peripherals*.

The IDE interface supports PIO mode 4 transfers up to 14MB/sec and Bus Master IDE transfer up to 33MB/sec (Ultra-DMA 33). It does not consume any ISA DMA resources and integrates 16x32-bit buffers for optimal transfers.



CAUTION

When connecting IDE devices to the Primary IDE interface, Master and Slave devices must be shared in respect of the device allocation on both the CompactFlash and hard disk drives.

3.3. Ethernet Interface

The two Ethernet controllers are electrically connected to the Primary PCI bus. They support 10Base-T and 100Base-TX operations: 10Mbps and 100Mbps network speeds are automatically detected and switched.

Signal Path

The two Ethernet interfaces are available through the J17 and J18 RJ-45 connectors located on the edge bracket. J18 capable of Wake-on-LAN.

Related Jumpers

None.

BIOS Settings

Section 4.1.5 *BIOS Features Setup: Boot from LAN First*.

3.3.1 Boot from LAN

The Boot from LAN capability is supported. To enable the option, use the BIOS Setup program. Please refer to Section 4.1 *BIOS Setup Program*.

3.3.2 Drivers

Network Drivers for Intel 82559 are available on the CD-ROM included with the PCI-948. It contains network drivers for most common operating systems.

3.4. Floppy Disk Interface

The onboard floppy disk controller is IBM PC XT/AT compatible. It handles 3.5" and 5.25", low and high-density disks. Up to two drives are supported in any combination.

Signal Paths

The Floppy Disk Controller interface is available through J3 connector (see Section 2.4)

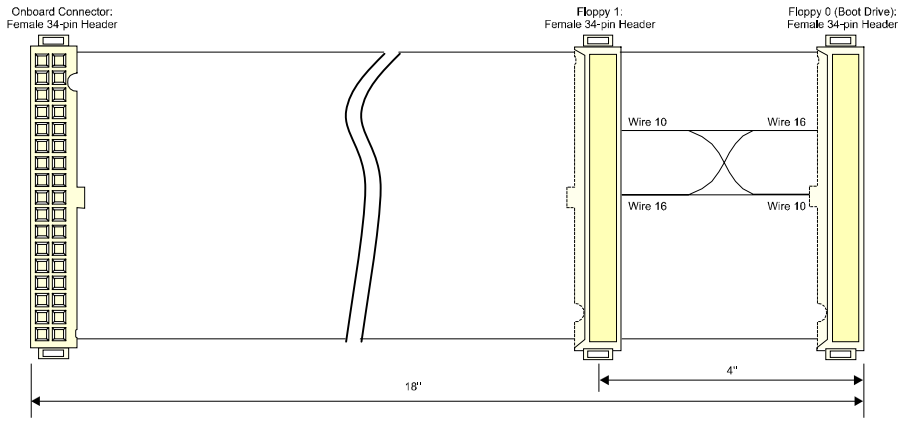
Related Jumpers

None.

BIOS Settings

Section 4.1.4 *Standard CMOS Setup: Select type of floppy*.
Section 4.1.10 *Integrated Peripherals: Enable/Disable Onboard FDC Controller*.

Two floppy disk drive units can be connected to the board through the J3 Floppy Disk connector using a standard IBM 34-pin flat ribbon cable. As illustrated below an 18" floppy disk cable is available from TEKNOR: Part number 150-051. One cable is provided with your board.



3.5. PS/2 Keyboard / PS/2 Mouse Interface

The onboard keyboard controller is Intel 8042 microcode compatible. PS/2 Keyboard and mouse signals are available through an output that supports direct connection to the interface. Since signals of both devices are combined on the same J24 connector, an Y-cable is required to split the signals and feed a standard PS/2 keyboard and a PS/2 mouse.

Signal Path

PS/2 keyboard and PS/2 mouse signals are available through J24 connector located on the edge bracket. PS/2 mouse signals are also available through J11 connector and the standard PS/2 keyboard signals are available through J9 and header 16.

Related Jumpers

None.

BIOS Settings

Section 4.1.10 *Integrated Peripherals : USB Keyboard Support,* and *PS/2 Mouse Function Control.*



CAUTION

Even though it is also possible to connect a keyboard through the multifunction header (J9), avoid connecting two keyboards simultaneously to the SBC. This can damage the keyboard interface.

3.5.1 I/O Connections

Standard AT keyboard, speaker port, reset and power buttons, and hard disk LED signals are available on the J9 Multi-Function header.

A 22” keyboard flat cable (TEKNOR part number 150-018-01) is provided with the board for connecting the respective devices.

3.6. Parallel Port

The PCI-948 features one IEEE-1854 multi-mode parallel port. It is compatible with Standard Mode IBM PC/XT, PC/AT, and PS/2 compatible bi-directional parallel port, Enhanced Parallel Port (EPP), and Enhanced Capabilities Port (ECP).

Signal Path

The Parallel Port interface is only available through J10 connector.

Related Jumpers

None

BIOS Settings

Section 4.1.10 *Integrated Peripherals*: *Onboard Parallel Port*; and *Parallel Port Mode*

The differences between Standard, EPP, and ECP modes appear in the signal assignation of the pins on the connector. Differences are described as follows:

Pin Number (J10)	Standard Mode	EPP Mode	ECP Mode
A15	SLCT	-	SLCT
B15	PE	-	PERROR[1], ACKREVERS[2]
C15	BUSY	WAIT	BUSY[1], PERIPHACK[2]
D15	/ACK	/INTR	/ACK
E16	/SLCTIN	/ADDRSTRB	/SLCTIN
B17	/INIT	-	/INIT[1], /REVERSERQST[2]
D17	/ERR	-	/FAULT[1], /PERIPHRQST[2]
A18	ALF	DATASTB	ALF[1], HOSTACK[2]
E17	PD0	PD0	PD0
C17	PD1	PD1	PD1
A17	PD2	PD2	PD2
D16	PD3	PD3	PD3
C16	PD4	PD4	PD4
B16	PD5	PD5	PD5
A16	PD6	PD6	PD6
E15	PD7	PD7	PD7

[1] Compatible mode - [2] High-speed Mode

NOTE

To operate in EPP or ECP mode, make sure and verify that the peripheral is designed to work in this mode and the BIOS setup is configured to support it.

3.6.1 Standard Mode

The Standard mode is unidirectional. It is supported to maintain the compatibility with the IBM PC standard.

3.6.2 EPP Mode

The EPP (Enhanced Parallel Port) mode consists of a hardware independent method of accessing a parallel port configured as EPP. It provides support for single I/O cycle as well as the high-performance block I/O transfers. The EPP mode always uses the optimum method for I/O transfers. For example, if the hardware supports it, EPP mode will perform 32-bit I/O block transfers.

EPP mode assumes that the parallel port can be used to connect more than one peripheral device using multiplexor or daisy chain configurations.

A multiplexor is an external device that permits up to eight parallel port devices to share a single parallel port.

A daisy chain device has two ports: input and output. The input port is connected either to the host parallel port or to the daisy chain device in front of it. The output is used to connect the next peripheral device to the daisy chain. The last device, however, can be one without daisy chain support.

3.6.3 ECP Mode

ECP (Extended Capabilities Port) works the same as EPP mode, but it will take precedence over the EPP mode when addressing multiple logical devices in a single physical product. While the EPP mode may intermix read and write operations without any overhead or protocol handshaking, the ECP mode negotiates data transfers using a request from the host and an acknowledgment from the peripheral.



NOTE

For more information on the ECP protocol, please refer to the Extended Capabilities Port Protocol and ISA Interface Standard (available from Microsoft Corporation) or contact our Technical Support department (See appendix G).

3.7. Serial Ports

Two fully functional serial ports are provided on the board for asynchronous serial communications. They are 16C550 high-speed UART compatible and support 16-byte FIFO buffers for transfer rates from 50bps to 115Kbaud.

Each serial port is specified as follows:

Designation	Communication Mode	Output Path
Serial Port 1	RS-232	J4
Serial Port 2	RS-232, RS-422 or RS-485	J5

UART registers are individually addressable and fully programmable.

3.7.1 Serial Port 1

Serial Port 1 is buffered directly for RS-232 operation. Signals include the complete signal set for handshaking, modem control, interrupt generation, and data transfer. When assigned as COM1, the port is 100% compatible with the IBM-AT serial port in RS-232 mode.

Signal Path

Serial Port 1 or COM1 signals are available on J4 connector.

Related Jumpers

None

BIOS Settings

Section 4.1.10 *Integrated Peripherals : Onboard Serial Port 1\2 Port Address of COM1*

3.7.2 Serial Port 2

The serial port 2 is buffered directly for RS-232, RS-422 or RS-485 operations and is 16C550 PC-Compatible. The interface includes the complete signal set for handshaking, modem control, interrupt generation, and data transfer.

When configured for RS-232 operation mode, the serial port 2 is 100% compatible with the IBM-AT serial port.

Signal Path
Serial Port 2 signals are available on the J5 connector

Related Jumpers
W3 and W4 to connect or disconnect Serial Port 2 line termination resistors in RS-485 operating mode. See Section 2.1– *Setting Jumpers*

BIOS Settings
Section 4.1.10 *Integrated Peripherals Setup*: *Onboard Serial Port 2*, and *Serial Port 2 Mode.*

Upon a power-up or reset, the Serial Port 2 interface circuits are automatically configured for the operation mode setup in the BIOS. The Serial Port 2 signal assignation on the J5 connector depends on the operational mode (RS-232, RS-422, or RS-485) it has been set:

Pin Number	RS-232 (J4 and J5)	RS-422 (J5)	RS-485(J5)
1	DC	/DCD	/DCD
2	RX	RX(-)	RX/TX(-)
3	TXD	TX(-)	-
4	DTR	/DTR	/DTR
5	GND	GND	GND
6	DSR	DSR	DSR
7	RTS	RX(+)	RX/TX(+)
8	CTS	TX(+)	-
9	RI	/RI	/RI

3.7.2.1. RS-232 Protocol:

When configured for RS-232 operation mode, the Serial Port 2 is 100% compatible with the IBM-AT serial port signal configuration.

3.7.2.2. RS-422 Protocol:

The RS-422 protocol (Full Duplex) uses both RX and TX lines simultaneously during a communication session.

> **CAUTION**
>
> In RS-485 mode, W3 and W4 jumpers must be installed to connect the 120 ohms line termination resistors (See Section 2.1 *Jumper Settings*)

3.7.2.3. RS-485 Protocol:

The RS-485 protocol (Full Duplex) also uses differential signals during a communication session. It differs from the RS-422 mode as it offers the ability to transmit and receive over the same pair of wires, and allows the sharing of the communication line by multiple stations. This configuration (also known as Party Line) allows only one system to take control of the communication line at the time.

In RS-485 mode, the RX lines are used as the transceiver lines, and the RTS signal is used to control the direction of the RS-485 buffer.

When set for RS-485 mode in the BIOS, upon power-up or reset, the transceiver is by default in receiver mode to prevent unwanted perturbation on the line. Party line operation mode requires termination resistors to be installed at both ends of the network.

3.8. Power Management

The PCI-948 SBC, when powered by an ATX power supply, offers the benefit of Operating System Directed Power Management (OSPM) supported by the hardware and BIOS implementation of Advanced Configuration and Power Interface (ACPI) specification.

ACPI defines the interfaces between the SBC BIOS, Chipset (PIIX4E), SMBus, peripheral devices and OSPM. It provides the BIOS with various hardware interface description Tables, a Firmware Control Structure and pseudo-code Control Methods written in ACPI Source Language (ASL) and ACPI Machine Language (AML) to empower the OSPM and device drivers.

The PIIX4E Chipset supports:

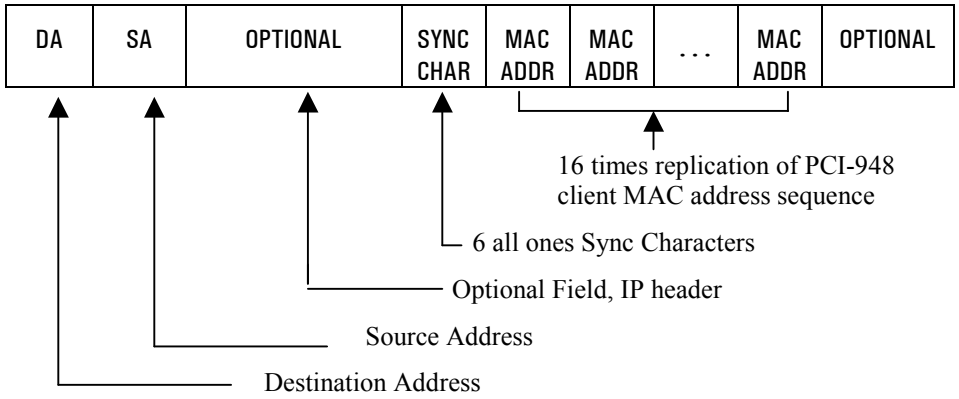
- Clock Control and Processor Complex Management
- Peripheral Device Management
- Event System Management: System Management and System Control Interrupts (SMI) and (SCI) generation and SMBus message handling
- Global System States (Working, Doze, Standby, Suspend, Hibernation, Soft Off) transition
- Device Power States (various, device specific) transition

The utilization of an OSPM pushes the limits of previous Advanced Power Management (APM) strategies to the critical requirement of the application actually running on the PCI-948 hardware. For instance, the spindle of a hard disk drive could be shut-off immediately after a save to disk operation if it is determined that an application requires little more than its timed AutoSave to disk function; a CPU speed could be reduced for an application phase requiring less computing power.

Wake-up event can be keyboard activity, mouse movement, Wake-on Timer, Wake-on-Ring, or Wake-on-LAN feature.

3.8.1 Wake-on-LAN Feature

The Wake-on-LAN feature is available with the PCI-948 SBC when it is connected as a client on a LAN and powered by an ATX power supply with auxiliary 5VSB and control signals PS-OK and PS-ON found on J23. In this case the wake-up event takes the form of an Ethernet packet of a unique format also called Magic Packet™ by AMD. Even in Soft-Off, PCI-948 soundest Sleep State, ETHERNET LAN 0 stays powered-on to monitor all incoming packets. Upon detection of its own Magic Packet, characterized by the inclusion of a 16 continuous duplication sequence of its own Media Access Control (MAC) address, the 82559 Fast Ethernet Controller issues a WOL signal to the ATX Power Supply Power-up Control which initiate the PCI-948 into a Working State. Wake-on-LAN is neither an APM or ACPI strategy.



Users already familiar with a remote wake-up from Suspend state by a modem ring (Wake-on-Ring) on a designated COM Port (Ring Indicator) can use this option on the PCI-948 SBC.

Wake-on-Event (LAN, Ring, and Timer) and Soft-Off functions are enabled in the *Power Management Setup* option of the *AWARD CMOS Setup Utility*. The PCI-948 SBC also supports SMI/SMM Power Management. It also supports APM, but its utilization is mutually exclusive with ACPI.

Signal Path

The ACPI Power Management supporting PS-OK, PS-ON signals and 5VSB voltage extension to the external ATX Power Supply are available on the J23 connector.

Related Jumpers

None, auto disabled when an ATX type Power Supply is not used

BIOS Settings

Section 4.1.7 *Power Management Setup*

3.9. Thermal Management

Two temperature sensors are provided to supervise the thermal environment. One is used to monitor the CPU die temperature, while the second one, located on the CPU casing, allows the monitoring of the ambient temperature around the CPU.

The temperature is controlled according to two temperature levels, the Low-temperature limit, which indicates normal operating conditions, and the High-temperature limit, which indicates an overheat condition.

The temperature management consists in reducing the CPU clock speed (throttling) when the temperature goes over the high limit (overheat condition) and suspending the throttling operation as soon as the temperature returns under the low-temperature limit (normal condition).

The clock speed may be throttled due to CPU overheating, maybe caused by the system cooling failure. In such a case, the temperature control is triggered as soon as the temperature reaches a high-temperature limit.

The ambient temperature of the CPU generally raises up due to an augmentation of the temperature in the casing. In that case, the clock speed will be slowed down as soon as the ambient temperature reaches the high-ambient temperature value.

Thermal management operations are controlled by the BX chipset, and settings are provided through the BIOS setup program interface, (See Section 4.1.9 *CPU/Board Feature Setup)*.

3.10. USB Interfaces

Signals for two USB ports are available on Connector J8.

USB is rapidly becoming the new peripheral interface standard. The USB advantages are: capability to daisy chain as many as 127 devices per single interface, bi-directional, isochronous/asynchronous protocol, fast 12Mbps transfer rate, and standardization of peripheral interface hardware and protocol into a single format.

Signal Paths
Both USB-0 and USB-1 interface signals are available on Connector J8.

Related Jumpers
None

BIOS Settings
4.1.8 *PnP/PCI Configuration: Assign IRQ For USB*.

The USB interface supports Plug and Play and hot swapping operations (OS level). These user-friendly features allow USB devices to be automatically attached, configured and detached, without powering down, reboot or running setup.

The PCI-948 board fully supports the standard Universal Host Controller Interface (UHCI) and uses standard software drivers that are UHCI-compatible.

3.11. Video Interface

The high-performance video capability of the board is based on Accelerated Graphics Port (AGP) technology. The video controller, a 69000 (Chips and Technologies), with its integrated 2MegaBytes of high-performance SDRAM is capable of CRT resolutions up to 1280 x 1024 x 256 colors.

The video interface features 32-bit AGP 2D GUI engine supporting CGA, EGA, Hercules, MDA, VGA, SVGA, XGA, and SXGA video display formats.

Signal Path

The video signals are available on the 15-pin VGA connector J20 located on the PCI-948 SBC edge bracket allowing direct CRT display connection.

Related Jumpers

None

BIOS Settings

4.1.8 *PnP/PCI Configuration: Init Display First,* and *Assign IRQ for VGA*

3.11.1 Supported Display Resolution and Colors

The maximum video resolution, colors displayed and performance depend directly on the Video drivers running with your application. The PCI-948 SBC Video Interface supports both Frame AGP 1x and PCI bus which enables wide range of system platforms and enables true dual display support. Resolution Refresh Rate and Number of Colors specification for the Intel HiQVideo™ Accelerator are listed below:

Resolution	Number of Colors (bpp)
1280x1024	256 (8 bits)
1024x768	64K (16 bits)
800x600	16M (24 bits)
640x480	16M (24 bits)

3.11.2 2D Graphics Engine

The 2D graphics engine is an advanced 64-bit three-operand engine that accelerates BitBLTs as line draws, polygon draw, and polygon fill. The 2D graphics engine also performs video and bitmap scaling, and data overlay.

3.12. Battery

The battery is required to keep the BIOS settings and the real-time clock stored into the CMOS RAM. The board is shipped from factory with the battery electrically disconnected from the board. Prior to first powering the board, the battery must be connected using the W2 Battery jumper.

The battery specifications are as follows: 3.6V Lithium battery, 0.37A/h

Related Jumpers

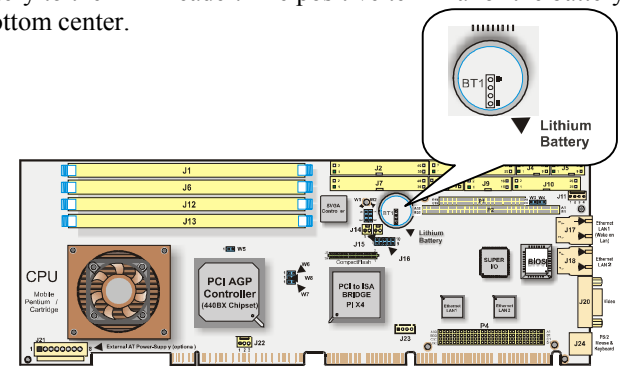
W 1	Power failed detection
W 2	Onboard/external battery jumper

Related Connectors

BT1	Polarized battery holder
J14	External battery connector

3.12.1 Installation

Connect the battery to the BT1 header. The positive terminal of the battery holder is located at the bottom center.



The onboard battery power can be replaced by an external power source by connecting a 3.6V DC to the J14 connector. When using an off board battery source, W2 must be set at position 2-3.

WARNING

Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.

PART 4

4. SOFTWARE SETUPS

1. BIOS SETUP PROGRAM
2. UPDATING OR RESTORING THE BIOS IN FLASH
3. VT100 MODE

4.1. BIOS Setup Program

All relevant information for operating the board and connected peripherals is stored in the CMOS memory (a battery-backed up memory holds this information when the board is powered off). The BIOS Setup program is required to make changes to the setup.



NOTES

Make sure you setup the BIOS Setup program prior to installing your operating system and your drivers.

For systems that need the BIOS to first attempt to boot from LAN, follow these steps:

1. Set the *Boot from LAN first* option to “Enabled” in the BIOS Setup’s *BIOS Features Setup*
2. Follow the complete procedure in the Boot from LAN utility CDROM.

4.1.1 Accessing the BIOS setup program

The system BIOS (Basic Input Output System) provides an interface between the operating system and the hardware of the PCI-948 peripheral processor. The PCI-948 uses the AWARD Setup program, a setup utility in flash memory that is accessed by pressing the DELETE key at the appropriate time during system boot. This utility is used to set configuration data in CMOS RAM.



CAUTION

Before modifying CMOS setup parameters, ensure that the W2 battery selection jumper is installed to enable the CMOS battery back up (please refer to Section 2.1).

To run the AWARD Setup program incorporated in the ROM BIOS:

- Turn on or reboot the system.
- Hit the DELETE key when the message - "Press DEL to Enter SETUP" appears near the bottom of the screen.

The main menu of the AWARD BIOS CMOS Setup Utility appears on the screen.

```
                    TEKNOR APPPLICOM T9002 BIOS VERSION 2.0
                              CMOS SETUP UTILITY
                          AWARD SOFTWARE, INC. (2A69TU00)

STANDARD CMOS SETUP                    LOAD BIOS DEFAULTS (safe)
BIOS FEATURES SETUP                    LOAD SETUP DEFAULTS (optimal)
CHIPSET FEATURES SETUP                 SUPERVISOR PASSWORD
POWER MANAGEMENT SETUP                 USER PASSWORD
PNP/PCI CONFIGURATION                  IDE HDD AUTO DETECTION
CPU/BOARD FEATURES SETUP               SAVE & EXIT SETUP
INTEGRATED PERIPHERALS                 EXIT WITHOUT SAVING

Esc     :      Quit                    ↑ ↓ → ←      :      Select Item
F10     :      Save & Exit Setup       (Shift)F2    :      Change Color

                        Time, Date, Hard Disk Type . . .
```

Whenever you are not sure about a certain setting, you may refer to the list of default values. The list of defaults is provided in the event that a value has been changed and one wishes to set this option to its original value. Loading the BIOS or SETUP defaults will affect all the options in this screen (or all parameters, except those in "standard CMOS setup", if defaults are loaded from the Main Menu) and will reset options previously altered.

The BIOS Default settings consist of the **safest** set of parameters. Use them if the system is behaving erratically. They should always work but do not provide optimal system performance.

The SETUP Default values provide **optimum performance** settings for all devices and system features.



CAUTION

These parameters have been provided to give control over the system. However, the values for these options should be changed only if the user has a full understanding of the timing relationships involved.

4.1.2 Main Menu

The Main Menu includes the following categories:

Category	Description
Standard CMOS Setup	This Setup page includes all the items in a standard, AT-compatible BIOS (date, time, hard disk type, floppy disk type, video adapter type, memory, etc.).
BIOS Features Setup	This Setup page includes all the items of AWARD's special enhanced features.
Chipset Features Setup	This Setup page includes all the items of the chipset's special features.
Power Management Setup	This Setup page sets power conservation options.
PnP/PCI Configuration	This Setup page sets Plug and Play and PCI configuration options.
CPU/Board Features Setup	This Setup page sets processor speed, thermal management and board monitoring options.
Integrated Peripherals	I/O subsystems that depend on the integrated peripherals controller in your system.
Load Bios Defaults	The BIOS defaults are **fail safe** settings, which consist of the safest set of parameters. Use them if the system is behaving erratically. They should always work but do not provide optimal system performance.
Load Setup Defaults	The Setup defaults are the **optimal** settings that provide the optimum performance for all devices and system features. **If the CMOS RAM is corrupted, the Setup defaults are loaded automatically.**
Supervisor/User Password Setting	Change, set or disable the password. It allows you to limit the access to the system and the Setup, or only to the Setup.
IDE HDD Auto Detection	Forces the detection of the IDE hard disk drives parameters and puts them in the Standard CMOS Setup page.
Save & Exit	After having modified the BIOS Setup, you can save the configuration in CMOS RAM and the Flash BIOS, by selecting this option.
Exit Without Saving	This option is used to exit AWARD Setup without saving the configuration to CMOS RAM or Flash BIOS.

4.1.3 Setups

The arrow keys (↑ ↓ → ←) are used to highlight items on the menu and the PAGEUP and PAGEDOWN keys are used to change the entry values for the highlighted item. To enter in a submenu, press the ENTER key. Also, you can press the F1 key to obtain help information or the ESC key to close a menu or to quit the program.

Key	Function
↑	Moves to previous item.
↓	Moves to next item.
←	Moves to the item at the left.
→	Moves to the item at the right.
ESC	When in the Main Menu: Quits program without saving modifications. When in other screens: Exits and returns to the Main Menu.
PAGEUP or +	Increases the numeric value or changes value.
PAGEDOWN or -	Decreases the numeric value or changes value.
F1	Help Menu
F2 / <Shift>F2	At the main menu, change the color of the menu.
F5	When in BIOS Features Setup, Chipset Features Setup, Power Management Setup, PNP/PCI Setup, Integrated Peripherals Setup or CPU Board Features: Restores the previous setup values for that setup screen only.
F6	When in BIOS Features Setup, Chipset Features Setup, Power Management Setup, PNP/PCI Setup, Integrated Peripherals Setup or CPU Board Features: Loads the BIOS Defaults for all the BIOS parameters for that setup screen only.
F7	When in BIOS Features Setup, Chipset Features Setup, Power Management Setup, PNP/PCI Setup, Integrated Peripherals Setup or CPU Board Features: Loads the Setup Defaults for the BIOS parameters for that setup screen only. If the CMOS RAM is corrupted, the Setup defaults are loaded automatically.
F10	When in the Main Menu: Saves all the CMOS changes and exit.

4.1.4 Standard CMOS Setups

Function	Description
Date/Time	The current values for each category are displayed. Enter new values through the keyboard.
Hard Disks	Two IDE controllers are defined on the board. The Primary and Secondary controllers can both have two disks: Master Disk or Slave Disk. Three settings are available for the hard disk type: Auto, User and None. Types 1 to 46 are not predefined in the system: Use auto or enter the parameters for the type in the user-defined.
Drive A / Drive B	Select the type of floppy disk installed for drive A and drive B.
Video	This option specifies the basic type of display adapter card installed in the system.
Halt on	This option specifies the type of errors that will stop the system during the BIOS booting procedure. A message asks that **you "press F1 to continue or press the DELETE key to enter Setup"**. The settings are: All errors, No errors, All but keyboard, All but diskette, and All but disk/key (default setting).
Memory	This display-only option indicates the amount of Base, Extended and other types of memory installed in the system.

4.1.5 BIOS Features Setup

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
Virus Warning	Dis.	Dis.	En. / Dis.	When Enabled, you receive a warning message if a program (specifically, a virus) attempts to write to the boot sector or the partition table of the hard disk drive. You should then run an anti-virus program. Keep in mind that this feature protects only the boot sector, not the entire hard drive. **Note: Many disk diagnostic programs and OS setups (e.g., Win95 setup), that access the boot sector table, can trigger the virus-warning message. If you plan to run such a program, we recommend that you first disable the virus warning.**
Quiet POST	Dis.	Dis.	En./Dis.	At the power on self-test (POST), only the AWARD logo and the "Press DEL to enter SETUP" message appears.
Quick Power On Self Test	Dis.	En.	En./Dis.	Select Enabled to reduce the amount of time required running the POST. A quick POST skips certain steps. We recommend that you enable quick POST to save time, since most major OS do their own tests
Full Screen Logo Show	Dis.	Dis.	En./Dis.	When enabled, a full screen bitmap (BMP) picture will appear during the POST or you can have your logo being displayed. Contact the technical Support (see Appendix G).
Boot from LAN First	Dis.	Dis.	En./Dis.	If Enabled, the BIOS will first attempt to boot from the LAN. The complete procedure for this function is available on the "Boot from LAN" utility CDROM.
Raid Card Boot First	Dis.	Dis.	En./Dis.	If Enabled, the BIOS will first attempt to boot from the RAID disk card.
Boot Sequence	A,C, SCSI	C,A, SCSI	A,C,SCSI; C,A,SCSI; C,CDROM,A; CDROM,C,A; D,A,SCSI; E,A,SCSI; F,A,SCSI; SCSI,A,C; SCSI,C,A; C only; LS/ZIP,C.	This option defines the searching order in the BIOS for the boot device(s). **Note: The Boot from LAN First and Raid Card Boot First options take precedence over this option.**
Swap Floppy Drive	Dis.	Dis.	En./Dis.	Selecting Enabled assigns physical drive B to logical drive A, and physical drive A to logical drive B.
Boot Up Floppy Seek	En.	Dis.	En./Dis.	When Enabled, the BIOS tests (seeks) floppy drives to determine whether they have 40 or 80 tracks. Only 360KB floppy drives have 40 tracks; drives with 720KB, 1.2MB, and 1.44MB capacity all have 80 tracks. Because very few modern PCs have 40 track floppy drives, we recommend that you set this field to "Disabled" to save time.
Drive A Boot Permit	En.	En.	En./Dis.	When Disabled, this option will not permit booting from Drive A.
Floppy Disk Access Control	R/W	R/W	R/W, Read Only	When Read Only, this option will not permit writing to the floppy disk.

BIOS Features Setup (Continued)

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
Report No FDD For Win 95	No	No	Yes, No	Select Yes to release IRQ6 when the system contains no floppy drive, for compatibility with Windows 95 logo certification. In the Integrated Peripherals screen, select NO on the Onboard FDC Controller option.
Hard Disk Write Protect	Dis.	Dis.	En./Dis.	When Enabled, this option will not permit writing to the hard disk.
HDD S.M.A.R.T. Capability	Dis.	En.	En./Dis.	When Enabled, the Self-Monitoring, Analysis, and Reporting Technology (S.M.A.R.T.) features of the HDD are supported. S.M.A.R.T is used for prediction of device degradation and/or faults.
Delay For HDD (Secs)	0	0	0-15	This number of seconds inserted prior to HDD initialization. 0 is disabled.
OS Select For DRAM > 64MB	Non-OS/2	Non-OS/2	Non-OS/2, OS/2	Select OS2 only if you are running OS/2 with greater than 64MB of RAM.
Gate A20 Option	Norm.	Fast	Normal, Fast	When Fast, enables fast switching of Gate A20 via the 440BX chipset, instead of the keyboard controller.
Security Option	Setup	Setup	Setup, Normal	If you have set a password, select whether the password is required every time the system boots (“System” option), or only when you enter Setup (“Setup” option).
Diskette Access For	All	All	All, Supervisor	When this option is set to Supervisor and the Security option to System, all floppy disk accesses (read/write) are limited to the Supervisor (supervisor password required).
Boot Up NumLock Status	On	On	On, Off	Controls the state of the NumLock key when the system boots. When set to “On”, the numeric keypad generates numbers instead of controlling cursor operations.
Typematic Rate Setting	Dis.	En.	En./Dis.	When Disabled, the following two items (Typematic Rate and Typematic Delay) are irrelevant. Keystrokes repeat at a rate determined by the keyboard controller in your system. When Enabled, you can select a typematic rate and a typematic delay.
Typematic Rate (Chars/s)	30	30	6-30 char/sec.	When the typematic rate setting is Enabled, you can select a typematic rate (the rate at which characters repeat when you hold down a key).
Typematic Delay (msec)	250	250	250-1000 ms	When the typematic rate setting is Enabled, you can select a typematic delay (the delay before keystrokes begin to repeat when you hold down a key).
VT100 Settings				
Comport	1	1	1,2	Use this option to select which COM port will be used for VT100
Speed	Auto	Auto	Auto, 2400, 9600, 19200, 38400, 57600, 115200	Select the baud rate off the COM port. used in VT100 mode.
Parity	None	None	None, Odd, Mark, Even, Space	Use this option to select the parity.
Data	8	8	7, 8	Use this option to specify the number of data bits being used.
Stop	1	1	1, 2	Use this option to specify the number of stop bits being used.

4.1.6 Chipset Features Setup

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
CPU Internal Cache	Dis.	En.	En./Dis.	Enables or Disables the CPU Internal Cache (L1 cache).
External Cache	Dis.	En.	En./Dis.	Enables or Disables the External Cache (L2 cache).
CPU L2 Cache ECC Checking (on CuMine PIII processor, you cannot disable ECC)	Dis.	En.	En./Dis.	Enables or Disables ECC Checking for L2 cache. **Note: processors provided by TEKNOR support ECC. However, not all Pentium® II processors support ECC. Check Intel's website to know if your processor supports ECC:** http://developer.intel.com/support/processors/pentiumII/identify.htm.
SDRAM RAS-to-CAS Delay	3	3	2, 3	**Note: Upon boot-up, the BIOS will detect and display the optimal value for the SDRAM options (three options in this menu), if it is different from the Setup value. You must enter the AWARD Setup, and set the options at the suggested value if you want the best performance.** This option inserts a timing delay between the CAS and RAS strobe signals, used when SDRAM is written to, read from, or refreshed. The number selected is the number of clocks to be inserted between a row activates command and either a read or write command.
SDRAM RAS Precharge Time	3	3	2, 3	Selects the number of CPU clocks for the RAS precharge. If an insufficient number of cycles are allowed for the RAS to accumulate its charge before SDRAM refresh, the refresh may be incomplete and the DRAM may fail to retain data.
SDRAM CAS Latency Time	3	3	2, 3	This option controls the number of clocks between when a read command is sampled by the SDRAMs and when the chipset samples read data from the SDRAMs. Select 3 for 3 DCLKs and 2 for 2 DCLKs. If a given row is populated with a registered SDRAM DIMM, an extra clock is inserted between the read command and when the chipset samples read data.
SDRAM Precharge Control	Dis.	Dis.	En./Dis.	When Enabled, all CPU cycles to SDRAM result in an All Banks Precharge Command on the SDRAM interface.
DRAM Data Integrity Mode	Non-ECC	ECC	ECC, Non-ECC	When set to ECC, allows auto-correction of the data read from memory. The ECC error flags' status register and the error pointer are updated if error correction occurs in this mode. When set to Non-Ecc, no error checking or error reporting is done.
Memory Hole At 15M-16M	Dis.	Dis.	En./Dis.	You can reserve this area of system memory for ISA adapter ROM. When this area is reserved, it cannot be cached. The user information of peripherals that need to use this area of system memory usually discusses their memory requirements.
System BIOS Cacheable	Dis.	En.	En./Dis.	Selecting Enabled allows caching of the system BIOS ROM at F0000h-FFFFFh, resulting in better system performance. However, if any program writes to this memory area, a system error may occur.
Video BIOS Cacheable	Dis.	En.	En./Dis.	Selecting Enabled allows caching of the video BIOS ROM at C0000h plus the VGA BIOS size, resulting in better video performance. However, in any program writes to this memory area, a system error may occur.
Video RAM Cacheable	Dis.	En.	En./Dis.	When Enabled, video memory region is cacheable. Some off-board video card drivers may behave strangely; in such a case, disable this option.
8 Bit I/O Recovery Time	3	1	1-8, NA	The I/O recovery mechanism adds bus clock cycles between PCI-originated I/O cycles to the ISA bus. This delay takes place because the PCI bus is much faster than the ISA bus. These two fields let you add recovery time (in bus clock cycles) for 8-bit and 16-bit I/O.
16 Bit I/O Recovery Time	2	1	1-4, NA	

Chipset Features Setup (Continued)

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
PCI/VGA Palette Snoop	Dis.	Dis.	En./Dis.	Palette snooping allows multiple VGA devices operating on different buses to handle data from the CPU on each set of palette registers. When set to Enabled, data read and written by the CPU is directed to both the PCI VGA device's palette registers and the ISA VGA device's palette registers, permitting the palette registers of both to be identical. When set to Disabled, data read and written by the CPU is only directed to the PCI VGA device's palette registers.
Passive Release	En.	En.	En./Dis.	When Enabled, CPU to PCI bus accesses are allowed during passive release otherwise the arbiter only accepts another PCI master access to local SDRAM.
Delayed Transaction	Dis.	Dis.	En./Dis.	The chipset has an embedded 32-bit posted write buffer to support delay transactions cycles. Select Enabled to support compliance with PCI specifications version 2.1.
Supervisor I/O Base Address	190h	190h	190h, 290h, 390h	This option determines the base address for the Supervisor I/O Register, which is used for such functions as power fail detection and the watchdog timer.
Power-Supply Type	AT	ATX	AT, ATX	This option selects the type of power supply.
AGP Aperture Size (MB)	64	64	4 to 256	This option selects the size in MB of the AGP Aperture.
Video BIOS Shadow	Dis.	En.	En./Dis.	Software that resides in a read-only memory (ROM) chip on a device is called *firmware*. Award permits shadowing of firmware such as the system BIOS, video BIOS, and similar operating instructions that come with some expansion peripherals. Shadowing copies from ROM into system RAM, where the CPU can read it through the 64-bit DRAM bus. Firmware not shadowed must be read by the system through the 8 or 16-bit ISA bus. Shadowing improves the performance of the system BIOS and similar firmware for expansion peripherals. Enable shadowing into each section of memory separately. Many system designers hardwire shadowing of the system BIOS and eliminate a System BIOS Shadow option. Note that on a PCI VGA card (on board or off-board), the VGA BIOS is always shadowed. Video BIOS shadows into memory area C0000 plus the VGA BIOS size. The remaining areas between C0000 and DFFFF shown on the BIOS Features Setup screen may be occupied by other expansion card firmware. If an expansion peripheral in your system contains ROM-based firmware, you need to know the address range the ROM occupies to shadow it into the correct area of RAM.
C8000-CBFFF	Dis.	En.	En./Dis.	
CC000-CFFFF	Dis.	En.	En./Dis.	
D0000-D3FFF	Dis.	En.	En./Dis.	
D4000-D7FFF	Dis.	En.	En./Dis.	
D8000-DBFFF	Dis.	En.	En./Dis.	
DC000-DFFFF	Dis.	En.	En./Dis.	

4.1.7 Power Management Setup

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
ACPI Function	Dis.	Dis.	En./Dis.	The Advanced Configuration and Power Interface (ACPI) allows Operating System Direct Power Management (OSPM) and make advanced configuration architectures possible. When Enabled, the OS supports ACPI or OSPM (e.g., Win98, Window NT 5). **Note: When Enabled, no other option in the Power Management Setup will be used.**
Power Management	User Def.	User Def.	User Define, Min Saving, Max Saving	This option allows you to select the type (or degree) of power saving for Doze, Standby, and Suspend modes. Max Saving: Maximum power savings. Inactivity period is 1 minute in each mode. Min Saving: Minimum power savings. Inactivity period is the maximum setting in each mode (1 hour for Doze, Standby and Suspend). User Define: Set each mode individually. Select time-out periods in the PM Timers section (see below).
PM Control by APM	Yes	Yes	Yes, No	If Yes, the OS will control the PM by APM calls. If No, the BIOS will control the PM and APM calls from the OS will be ignored.
Video Off Method	V/H SYNC + Blank	V/H SYNC + Blank	Blank Screen V/H SYNC+Blank, DPMS,	Determines the manner in which the monitor is blanked. V/H SYNC + Blank: System turns off vertical and horizontal synchronization ports and writes blanks to the video buffer. DPMS Support: Select this option if your monitor supports the Display Power Management Signaling (DPMS) standard of the Video Electronics Standards Association (VESA). Use the software supplied for your video subsystem to select video power management values. Blank Screen: System only writes blanks to the video buffer.
Video Off After	Standby	Stand by	NA, Suspend, Standby, Doze,	As the system moves from lesser to greater power-saving modes, select the mode in which you want the monitor to blank.
Modem Use IRQ	3	3	N/A, 3, 4, 5, 7, 9, 10, 11	Name the IRQ line assigned to the modem (if any) on your system. Activity of the selected IRQ always awakens the system.
Doze Mode	Dis.	Dis	Disable 1min to 1h	After the selected period of system inactivity (1 minute to 1 hour), the CPU clock runs at lower speed while all other devices still operate at full speed.
Standby Mode	Dis.	Dis.	Disable 1min to 1h	After entering Doze mode and the selected period of system inactivity (1 minute to 1 hour) has elapsed, the video shuts off while all other devices still operate at full speed.
Suspend Mode	Dis.	Dis.	Disable 1min to 1h	After entering Standby mode and the selected period of system inactivity (1 minute to 1 hour) has elapsed, all devices including the CPU shut off and the system waits for an event to wake them up again.
HDD Power Down	Dis.	Dis.	Disable 1-15min	After the selected period of drive inactivity (1 to 15 minutes), the hard disk drive powers down while all other devices remain active. The HDD power down mode is only available if the hard drive has this capability.
HDD Down When Suspend	En.	En.	En./Dis.	When Enabled and the system goes in Suspend Mode, the hard disk is shut down.
Throttle Duty Cycle	75.0%	75.0%	12.5%-75.0%	When the system enters Doze mode, the CPU clock runs only part of the time. You may select the percentage of time that the clock does not run.
PCI/VGA Act-Monitor	Dis.	Dis.	En./Dis.	When Enabled, continuous video activity restarts the global timer for Standby mode.
Soft-OFF by PWR-BTTN	Instant-off	Instant-off	Instant-off, Delay 4 sec.	This option only works with an ATX power supply. It allows two configurations for the power button: Instant-off for power supply on/off switch, or Delay 4 sec. for entering Suspend Mode after pressing the button at least 4 seconds.

. . .

Power Management Setup (Continued)

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
Resume by Ring	Dis.	En.	En./Dis.	When Enabled and a modem is connected to a COM port, allows a modem ring to re-activate the CPU when in Suspend mode.
IRQ 8 Break Suspend	Dis.	En.	En./Dis.	When Enabled, the RTC alarm interrupt is monitored to allow an interrupt to awaken the system when in Doze, Standby or Suspend Mode.
Resume by Alarm	Dis.	Dis.	En./Dis.	When Enabled, allows setup of a time to re-activate the CPU when in Suspend mode with the options Date (of Month) Alarm and Time (hh:mm:ss) Alarm. **Note: The IRQ 8 Break Suspend option in this setup screen must be Enabled to use the RTC alarm.**
Reload Global Timer Events:				
IRQ[3-7,9-15], NMI	Dis.	En.	En./Dis.	When any of the options below is Enabled, monitoring of the interrupt will occur to allow an interrupt to awaken the system when in Doze, Standby or Suspend Mode.
Primary IDE 0	Dis.	En.	En./Dis.	
Primary IDE 1	Dis.	En.	En./Dis.	
Secondary IDE 0	Dis.	En.	En./Dis.	
Secondary IDE 1	Dis.	En.	En./Dis.	
Floppy Disk	Dis.	En.	En./Dis.	
Serial Port	En.	En.	En./Dis.	
Parallel Port	Dis.	En.	En./Dis.	

4.1.8 PnP/PCI Configuration

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
PNP OS Installed	Yes	No	Yes, No	If the operating system (OS) is Plug and Play (for example Windows 95), select "Yes" if you want the OS to allocate resources according to Plug and Play standards, or "No" if you want the same resource allocations at every system boot-up. Select "No" when the OS is not Plug and Play (for example, DOS). **Note: When set to "Yes", only the boot devices will get an IRQ.**
Resources Controlled By	Auto	Man.	Auto, Man.	The Award Plug and Play BIOS can automatically configure all the boot and Plug and Play-compatible devices. If you select Auto, all the interrupt requests (IRQs) and DMA assignment fields disappear, as the BIOS automatically assigns them.
Reset Configuration Data	Dis.	Dis.	En./Dis.	Normally, you leave this field Disabled. Select Enabled to reset Extended System Configuration Data (ESCD) when you exit Setup if you have installed a new add-on and the system reconfiguration has caused such a serious conflict that the operating system cannot boot.
IRQ *n* Assigned To	PCI/ISA PnP	PCI/ISA PnP	PCI/ISA PnP, Legacy ISA	When resources are controlled manually, assign each system interrupt as one of the following types, depending on the type of device using the interrupt: Legacy ISA: Devices compliant with the original PC AT bus specification, requiring a specific interrupt, such as IRQ4 for serial port 1. PCI/ISA PnP: Devices compliant with the Plug and Play standard, whether designed for PCI or ISA bus architecture. When Legacy ISA is selected for an IRQ line, this resource will not be available for PCI/ISA PnP.
DMA *n* Assigned To	PCI/ISA PnP	PCI/ISA PnP	PCI/ISA PnP, Legacy ISA	When resources are controlled manually, assign each system DMA channel as one of the following types, depending on the type of device using the interrupt: Legacy ISA: Devices compliant with the original PC AT bus specification, requiring a specific DMA channel. PCI/ISA PnP: Devices compliant with the Plug and Play standard, whether designed for PCI or ISA bus architecture. When Legacy ISA is selected for a DMA channel, this resource will not be available for PCI/ISA PnP.
Init Display First	Onboard	Onboard	PCI Slot, Onboard, AGP (not supported)	Initializes the specified video display. The chosen display becomes the primary display. Other display devices are ignored by the BIOS and configured by the OS.
Assign IRQ For VGA	Dis.	Dis.	En./Dis.	When Enabled, the video card is assigned an IRQ.
Assign IRQ For USB	En.	En.	En./Dis.	When Enabled, the USB is assigned an IRQ. When Disabled, the IRQ is freed up for another purpose.
PCI Latency Timer	32	32	0-255 (integers)	This option specifies the value of the Latency Timer for the PCI bus master, in units of PCI bus clocks. Value must be a power of 2 (1, 2, 4, 8, 16, 32, 64, or 128).
Special PCI Routing	En.	En.	En./Dis.	Disable this option if the backplane into which the board is installed conforms to the PICMG specifications. When enabled the board will attempt to detect a special PCI routing configuration.
Slot [number] Use IRQ No.	Auto	Auto	Auto, 3, 4, 5, 7, 9, 10, 11, 12, 14, 15	When Auto, the BIOS automatically assigns an IRQ for the specified PCI slot number (in the option title: 1, 2, 3 or 4). When set to one of the numbers (in possible settings), that IRQ number is assigned to the PCI slot.
Used MEM Base Address	N/A	N/A	N/A, C800, CC00, D000, D400, D800, DC00	Select a base address for the memory area used by any peripheral that requires high memory.

4.1.9 CPU/Board Features Setup

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
Current Processor(s) Speed	Various, depending on the installed CPU			This option displays the current processor speed.
Front Side Bus Speed				This option displays the current FSB speed.
Thermal Management Options:				
Thermal Management	Dis.	Dis.	En./Dis.	When this option is enabled, the CPU temperature is monitored. Whenever the CPU overheats, the CPU slows down to lower the temperature.
Thermal Audio Alarm	Dis.	Dis.	En./Dis.	When the Thermal Management option and this option are enabled, a continuous audible alarm is sounded when the temperature specified in the Overheat Alarm options is reached. Such an alarm may not be supported by the Operating System.
CPU 1 Die Temp °C	-	-	Varies	Displays the current die (internal) CPU temperature, when Thermal Management is enabled.
Resume Alarm (°C)	42	42	10-70	The CPU will be slowed down (Doze mode) when it reaches the selected Overheat Alarm (°C) temperature. Full speed (Normal mode) will be resumed when the temperature comes down to the selected Resume Alarm (°C) temperature. A minimum of + 4° is automatically ensured for the Overheat Alarm temperature with reference to the Resume Alarm.
Overheat Alarm (°C)	50	50	30-90	
CPU Local Temp°C	-	-	Varies	Displays the current case (external) CPU temperature, when Thermal Management is enabled.
Save CMOS in Flash	Dis.	Dis.	En./Dis.	Saving CMOS memory content into Flash Memory will prevent to loose CMOS options when battery fails.
Watchdog Timer	Dis	Dis	En./Dis.	
Watchdog After POST	-	-	En./Dis.	This option enables Watchdog circuit after the POST sequence
Watchdog Duration (ms)	262144		64 to 262144	Use this option to setup duration time (in ms) of the Watchdog timing circuitry.

4.1.10 Integrated Peripherals

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
On-Chip Primary/ PCI IDE:	En.	En.	En./Dis.	Select Enabled to activate the Primary/Secondary IDE channel. The four options below appear only if the On-Chip Primary option is enabled.
IDE Primary Master PIO IDE Primary Slave PIO IDE Secondary Master PIO IDE Secondary Slave PIO	Auto	Auto	Auto, Modes 0-4	Use this option to set a PIO mode (0-4) for each of the onboard IDE devices. Modes 0 through 4 provide successively increased performance and speed. In Auto mode, the system automatically determines the best mode for each device. If you select a mode that the drive does not support, it may not work, so choose a lesser value or Auto to see the best mode for the drive.
IDE Primary Master UDMA IDE Secondary Master UDMA IDE Primary Slave UDMA IDE Secondary Slave UDMA	Dis.	Auto	Auto, Disabled.	Ultra DMA/33 implementation is possible only if your IDE hard drive supports it and the operating environment includes a DMA driver (Windows 95 OSR2 or a third-party IDE bus master driver). If your hard drive and your system software both support Ultra DMA/33, select Auto to enable BIOS support.
On-Chip Secondary PCI IDE:	En.	En.	En./Dis.	Select Enabled to activate the Secondary IDE channel. The four options below appear only if the On-Chip Secondary option is enabled.
IDE HDD Block Mode	Dis.	En.	En./Dis.	Block mode is also called block transfer, multiple commands, or multiple sector read/write. If your IDE hard drive supports block mode (most new drives do), select Enabled for automatic detection of the optimal number of block read/writes per sector the drive can support.
Onboard PCI SCSI Chip	En.	En.	En./Dis.	Enables/disables the onboard SCSI controller.
Ethernet Controllers #1, #2	En.	En.	En./Dis.	Enables/disables the onboard Ethernet controller.
USB Keyboard Support	Dis.	Dis.	En./Dis.	This option is for DOS and BIOS support only (Win 95 has it is own drivers). **It does not enable or disable the USB controller.**
PS/2 Mouse Function Control	Auto	Auto	Auto/Dis.	When set to Auto, the PS/2 mouse is automatically enabled, if it is present.
Onboard FDC Controller	En.	En.	En./Dis.	Select Disabled to disable the onboard floppy disk controller (FDC).
Onboard Serial Port 1/2	Auto	Auto	Dis., 3F8/IRQ4, 2F8/IRQ3, 3E8/IRQ4, 2E8/IRQ3, Auto	Select a COM port address and IRQ# for the first and second serial ports.
Serial Port 2 Mode	RS-232	RS-232	RS-232,RS-422, and RS-485	Select the operation mode for Serial Port 2.
Onboard Parallel Port	378/IRQ7	378/IRQ7	Disabled, 3BC/IRQ7, 378/IRQ7, 278/IRQ5,	Select a LPT address and IRQ# for the physical parallel (printer) port.
Parallel Port Mode	ECP + EPP1.9	ECP + EPP1.9	SPP, EPP1.9+SPP, ECP, ECP+EPP1.9, Normal, EPP1.7+SPP, ECP+EPP1.7	Select an operating mode for the onboard parallel port. Select ECP or EPP unless you are certain both your hardware and software does not support ECP or EPP mode.
ECP Mode Use DMA	3	3	1, 3	Select a DMA channel for the port.

4.2. Updating or Restoring the BIOS in Flash

4.2.1 UBIOS.EXE 4.1 - BIOS Update and Copy Utility



IMPORTANT
This utility is used to update the BIOS on Teknor's single board computer. To ensure the success of this operation, please read entirely these instructions before using this program.

You can run this utility in 2 different modes:

1. Interactive Mode: In this mode the program is menu-driven. This mode is explained in Section 4.2.4.
2. Batch Mode: It is also possible to run the program without menus by a command, which specifies the selected options and files with parameters. This mode is explained in Section 4.2.5.

4.2.2 How to Do a Successful Update

UBIOS needs to be run in DOS 3.3 or higher or compatible environment.

1. Take note of your special BIOS options such as drive settings, hard disks and custom settings. After the update, these options will be set to their default values and all changes will need to be re-entered.

2. Ensure you have the proper BIOS file required to execute the update.
   These files may be obtained from Teknor WEB site, by Teknor technical support or by UBIOS itself.
   Refer to the 'How to do a Successful Copy' for details about the last source.

3. Boot in a driver free environment. **No Hi-memory driver must be loaded**.
   To boot with a free environment, follow these steps:
   - **In DOS**:
     Boot with the F5 key pressed, this will disable config.sys and autoexec.bat interaction.
   - **In Windows 9x**:
     Boot with the F8 key pressed and choose *'safe mode command prompt only'* option.

4. Call the UBIOS program and follow the instruction menu. To do a complete BIOS update, select item 'A) Update all BIOS'.

4.2.3 How to do a Successful Copy

Follow the same procedure as above.

To do a complete BIOS copy, select item '**a) Copy all BIOS'.**

Advanced functionality

Advanced functionality is resumed in the UBIOS help mode.
To call UBIOS help page, use UBIOS /?

VT-100 mode

UBIOS can be used without a screen in Teknor's VT-100 mode. This mode transfers all screen and keyboard text activity through the serial port.

To use UBIOS in vt-100, use the /vt argument like: UBIOS /vt

In this mode, scan code keys are not transmitted. These keys include the 'home', 'end', 'Pg Up', 'Pg Dn' keys that can be useful to UBIOS. To bypass this limitation, the numerical keypad can be used.

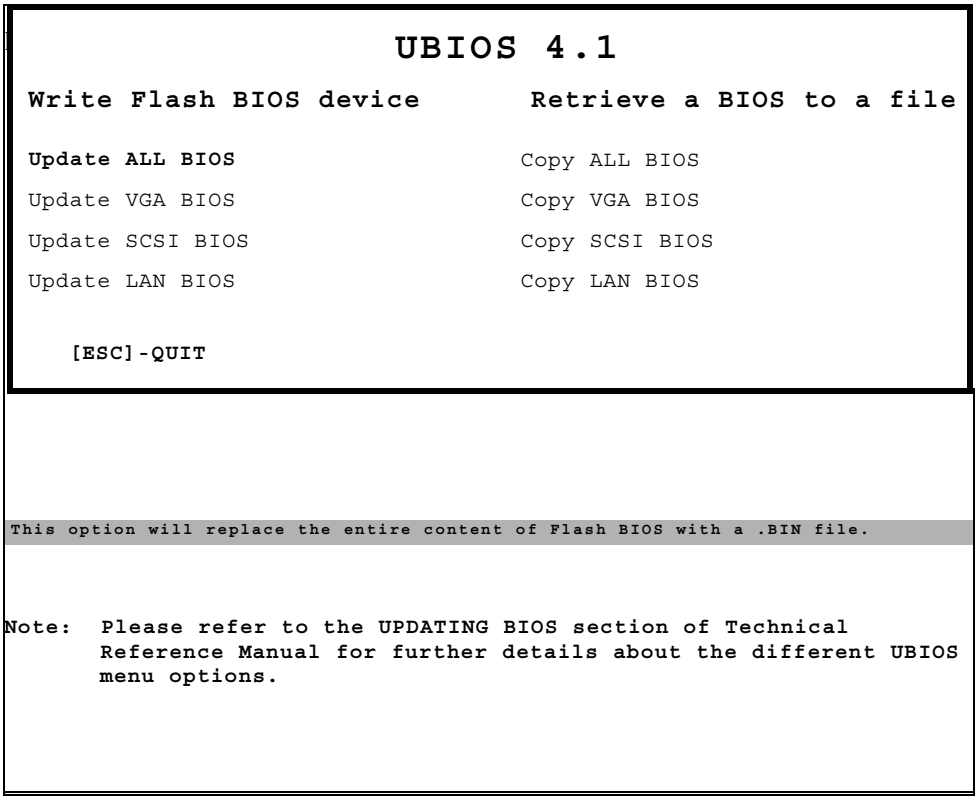
'7' will be assigned to 'home',
'8' to the up arrow,
'9' to 'Pg Dn'
…
'5' will be assigned to the 'Esc' key.

4.2.4 UBIOS - Interactive Mode

To run the program in interactive mode, type "UBIOS" from the DOS prompt and the UBIOS 4.0 presentation screen will be displayed. To continue, hit any key on the keyboard. This brings you to the main menu.

4.2.4.1. Main Menu

The main menu appears below:



The main menu displays two groups of options: Write Flash BIOS device and Retrieve a BIOS to a file. The first group allows you to update the Flash BIOS device with a BIOS file stored on disk. The second group allows you to copy the contents of the Flash BIOS device to files on disk.

In the above menu, the option **Update ALL BIOS** is highlighted and the option is described in the shaded row below. Move the arrow keys to highlight other options.

To **select** the highlighted option, press ENTER.
To **exit the program**, press the ESC key when you are in the main menu.

There are four types of BIOS files appearing on the main menu:

1. ALL BIOS File: This file combines all BIOS files contained in the Flash BIOS device in a single file. It has the .BIN extension.

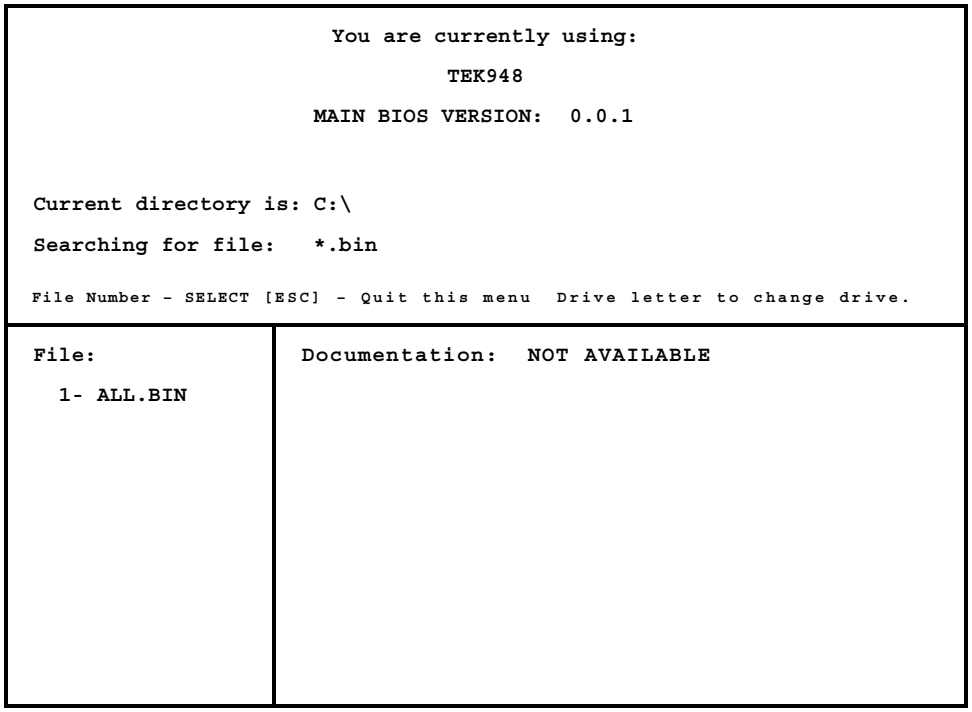
2. VGA BIOS File: This file contains the VGA BIOS section of the Flash BIOS. There are two possible types of VGA BIOS files: files with the .VGA extension (supports CRT displays only) and files with the .BFP extension (supports CRT and Flat Panel displays).

3. SCSI BIOS File: This file contains the SCSI BIOS section of the Flash BIOS. It has the .BIN or .SCS extension.

4. LAN BIOS File: This file contains the LAN BIOS section of the Flash BIOS. It has the .BIN extension.

4.2.4.2. Updating the Flash BIOS

If you select one of the **Update** options from the main menu, a screen similar to the following is displayed:

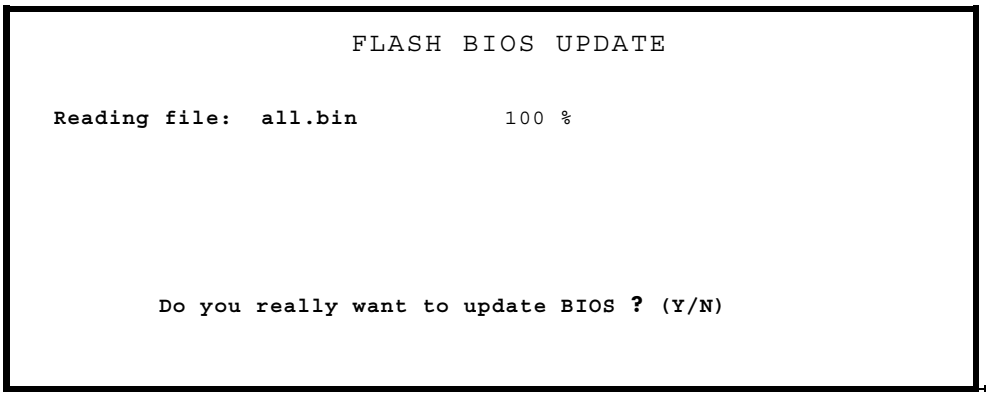


Files of the type you selected in the main menu and which are in the current directory are displayed in the **File** window.

To change directory, type the drive letter. If there are any files of the type you selected in this directory, they will be displayed in the **File** window.

The **Documentation** window displays "NOT AVAILABLE". It will be used in the future for displaying the contents of a .doc file.

If you want to return to the previous menu, press the ESC key.
To select a file from the **File** window, in order to update the Flash BIOS with this file, type the file number which appears before the filename in the list. A new screen is displayed as shown below. This is the Flash BIOS Update screen. You must first confirm if you want to update the Flash BIOS with the selected file (the filename appears next to **Reading file)**, by typing "Y" for Yes, "N" for No.



If you choose to update the file, by typing "Y", the program will write the file to Flash. The progress of the operation is indicated in percentage completed, next to **PLEASE WAIT – Writing to Flash …**

When the update is over the screen will appear as follow:

```
                    FLASH BIOS UPDATE

  Reading file:  all.bin          100 %
  PLEASE WAIT - Writing to Flash … 100 %



    Do you really want to update BIOS ? (Y/N)
```

```
Make sure that the watchdog is disabled by JUMPER DURING the next boot ONLY.
       Just to ensure a good FPGA update.
       After the next boot you can enable the watchdog.
       Please REBOOT as soon as possible …
       Note:  Please refer to the UPDATING BIOS section of Technical
              Reference Manual.



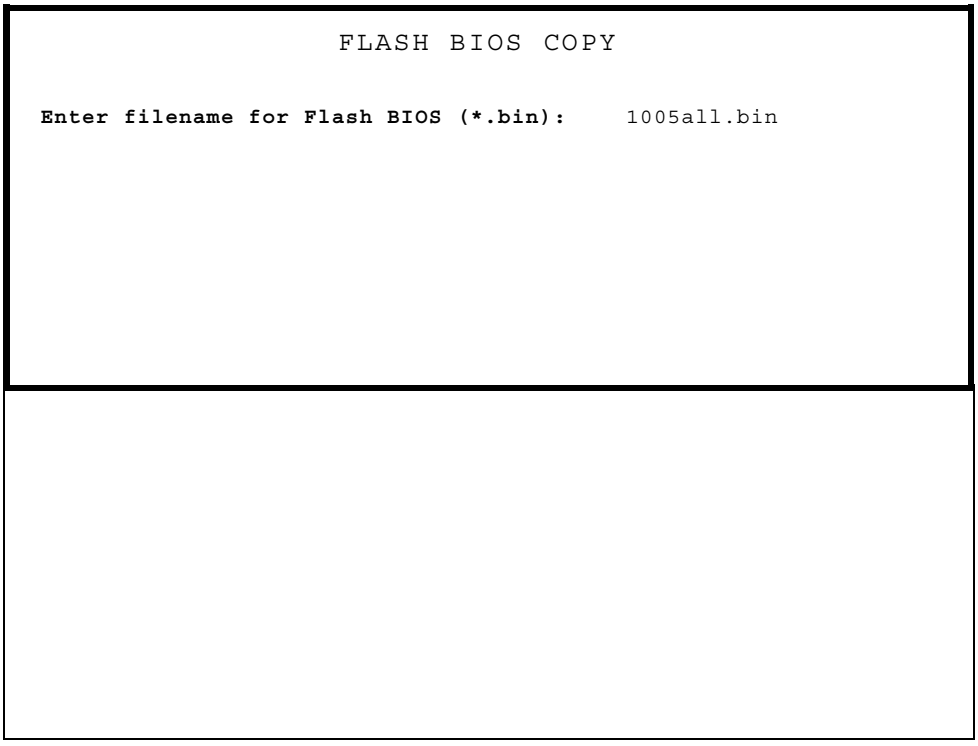
                              Hit any key to continue …
```

To return to the main menu, hit any key on the keyboard.

> **NOTE**
>
> There may be slight changes to the Flash BIOS Update screen compared to those shown here for an Update ALL BIOS operation. Also, if an error occurs, these will be indicated on the screen.

4.2.4.3. Copying Flash BIOS

If you select one of the **Copy** options from the main menu, a screen similar to the following is displayed:



You begin a Flash Copy operation, by typing a filename (including the extension) for the file you are creating. In the above example, the filename entered was "1005all.bin".

Press ENTER to proceed.

The progress of the operation will display on the screen in percentage completed. The example shown on the following page is for the Copy ALL BIOS option.

```
FLASH BIOS COPY

  Enter filename for Flash BIOS (*.bin):948all.bin
PLEASE WAIT - Writing ALL BIOS to 1005all.bin 100 %
  DONE - Press any key to continue.
```

If the filename entered for the BIOS file already exists, the following message will appear on the screen:

File already exits! Overwrite? (Y/N)

If you choose to overwrite the existing file, its content will be lost.

To return to the main menu, hit any key on the keyboard.



NOTE
There may be slight changes to the Flash BIOS Copy screen compared to those shown here for a Copy ALL BIOS operation. Also, if an error occurs, these will be indicated on the screen.

4.2.5 UBIOS – Batch Mode

While files can be manually selected using the Interactive Mode, Flash BIOS Update or Copy can be achieved through Batch Mode.

The command line format is as follows:

UBIOS /B [operation] [filetype] [filename] [options] where:

/B or /-B specifies that this is a Batch Mode command.

[operation] is the Flash BIOS operation you wish to perform, and can be replaced with one of three letters: U for Update, C for Copy, or V for Verify (used to compare the contents of the Flash BIOS device and the specified BIOS file).

[filetype] is the filetype of the BIOS file to program (with an update operation) or to create (with a copy operation), and can be replaced with one of the following:

ALL	for All BIOS files in a single file with the .BIN extension,
VGA	for VGA BIOS file with the .VGA or .BFP extension,
SCSI	for SCSI BIOS file with the .BIN extension,
LAN	for LAN BIOS file with the .BIN extension.

[filename] is the name of the BIOS file (including the extension) to program (with an update operation) or to create (with a copy operation), and can be replaced with the filename which corresponds to the filetype. For example, if "VGA" was listed as filetype, then the filename could be "FLAT.BFP".

[options] these are optional parameters that may be added:

/C This option will not clear the CMOS Setup when updating main BIOS (AWARD BIOS), however this is not recommended since the CMOS Setup should be updated when the main BIOS is changed.

/R Instructs UBIOS to reset the board upon completion of the operation.

/VT For VT100 compatibility.

/? To get a summary of the Batch Mode options from UBIOS. It will display a Batch options summary of valid UBIOS command lines. The same help information will also be displayed each time UBIOS detects an error in the command line.

4.3. VT100 Mode

The VT100 operating mode allows remote setups of the board. This configuration requires a remote terminal that must be connected to the board through a serial communication link.

4.3.1 Requirements

The terminal should emulate a VT100 or ANSI terminal. Terminal emulation programs such as Telix© or Procom© can also be used.

4.3.2 Setup & Configuration

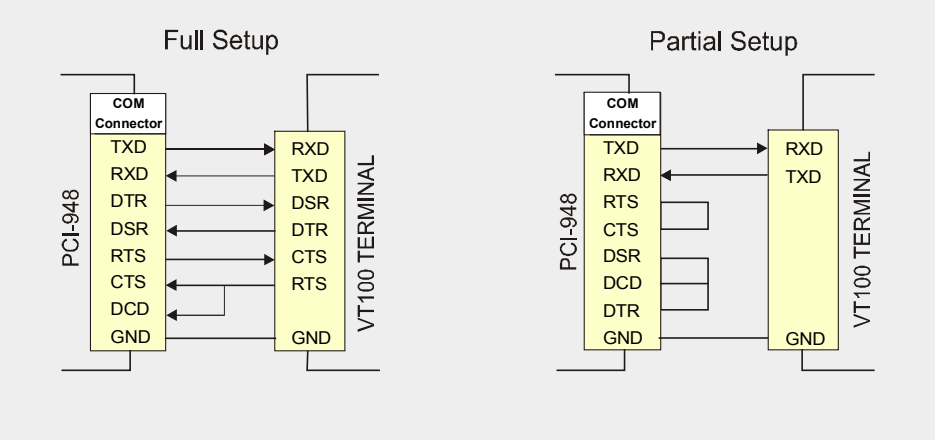
Follow these steps to set up the VT100 mode:

1. Connect a monitor and a keyboard to your board and turn on the power.
2. Enter into the CMOS Setup program in the "BIOS Feature Setup"
3. Select the VT100 mode and the appropriate COM port and save your setup.
4. Connect the communications cable as shown in the next page.

> **NOTE**
>
> If you do not require a full cable for your terminal, you can set up a partial cable by using only the TXD and RXD lines. To ignore control lines simply loop them back as shown in VT100 Partial Setup cable diagram.

5. Configure your terminal to communicate using the same parameters as in CMOS Setup.
6. Reboot the board.
7. Use the remote keyboard and display to setup the BIOS.

Save the setup, exit, and disconnect the remote computer from the board to operate in stand-alone configuration.



4.3.3 Running Without a Terminal

The board can boot up without a screen or terminal attached. If the speed is set to Auto and no terminal is connected, the speed is set to 115,200 bauds.

Furthermore, you can run without any console at all by simply not enabling VT100 Mode and by disabling the onboard video.

PART 5

APPENDICES

A. MEMORY & I/O MAPS

B. INTERRUPT LINES

C. BOARD DIAGRAMS

D. CONNECTOR PINOUTS

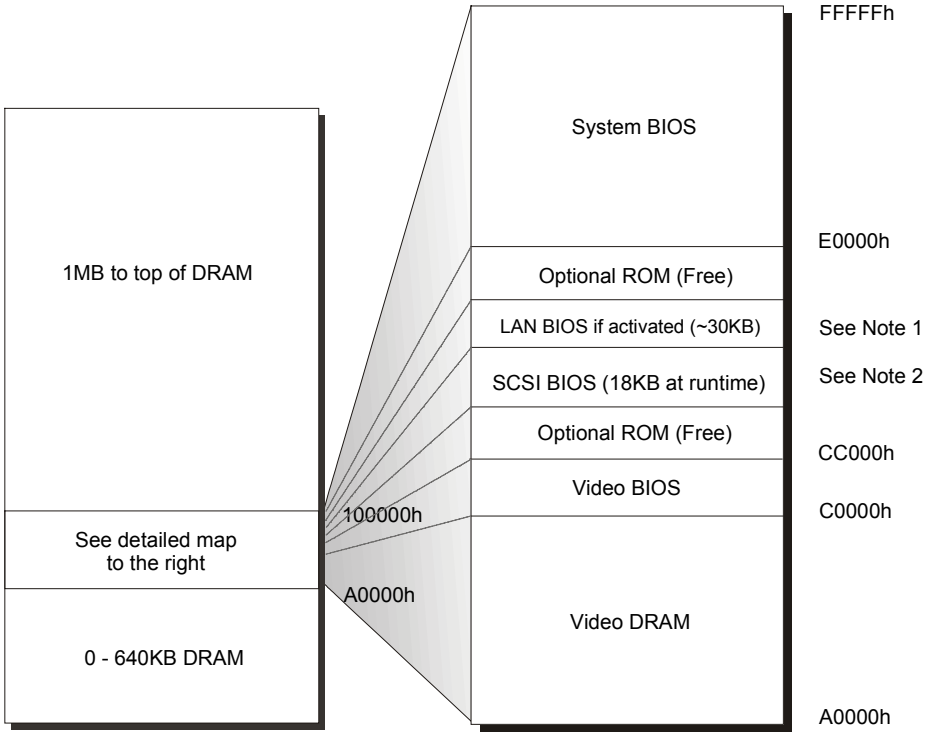
E. BIOS SETUP ERROR CODES

F. EMERGENCY PROCEDURE

G. GETTING HELP & RMA

A. MEMORY & I/O MAPS

A.1 Memory Mapping



Note 1 : LAN BIOS address may vary

Note 2 : SCSI BIOS address may vary.
Size is only 2KB if no device.

Address	Function
00000-9FFFF	0-640 KB DRAM
A0000-BFFFF	Video DRAM
C0000-CBFFF	Video BIOS
CC000-DFFFF	Optional ROM (Free)
	LAN BIOS around 30KB if activated, address may vary
	SCSI BIOS 18KB at runtime, 2KB if no device, address may vary
E0000-FFFFF	System BIOS
100000-Top of DRAM	1 MB - Top of DRAM

A.2 I/O Mapping

Address	Optional Address	Optional Address	Optional Address	Function
000-01F				DMA Controller 1
020-03F				Interrupt Controller 1
040-05F				Timer
060-06F				Keyboard
070-07F				Real-time clock
080-09F				DMA Page Register
0A0-0BF				Interrupt Controller 2
0C0-0DF				DMA Controller 2
0F0-0F1, 0F8-0FF				Math Coprocessor
x90-x9F				Teknor Control Port
1F0-1F7, 3F6				Primary IDE
3F0-3F7	370-377			Floppy Disk
378-37A	3BC-3BE	2787-27A		Parallel Port (LPT1 by default)
3F8-3FF (COM1)	2F8-2FF (COM2)	3E8-3EF (COM3)	2E8-2EF (COM4)	Serial Port 1 (COM1 by default)
2F8-2FF (COM2)	3F8-3FF (COM1)	3E8-3EF (COM3)	2E8-2EF (COM4)	Serial Port 2 (COM2 by default)
3C0-3CF, 3D0-3DF, 3B0-3BB				Graphics Controller (I2C Port)

B. IRQ AND DMA LINES

B.1 IRQ Lines

The board is fully PC compatible with interrupt steering for PCI plug and play compatibility.

Controller # 1		Controller # 2	
IRQ 0	Timer Output 0	IRQ 8	Real-Time Clock
IRQ 1	Keyboard	IRQ 9	Available [1]
IRQ 2	Cascade Controller # 2	IRQ 10	Available [1]
IRQ 3*	Serial Port 2	IRQ 11	Available [1]
IRQ 4*	Serial Port 1	IRQ 12	PS/2 Mouse
IRQ 5*	Available [1]	IRQ 13	Coprocessor Error
IRQ 6*	Floppy Controller	IRQ 14	Primary IDE or available [1]
IRQ 7*	Parallel Port 1 or Available [1]	IRQ 15	N/C

*: All functions marked with an asterisk (*) can be disabled or reconfigured.
1 Available lines service on board and external PCI/ISA PnP devices or a Legacy ISA device.

B.2 DMA Channels

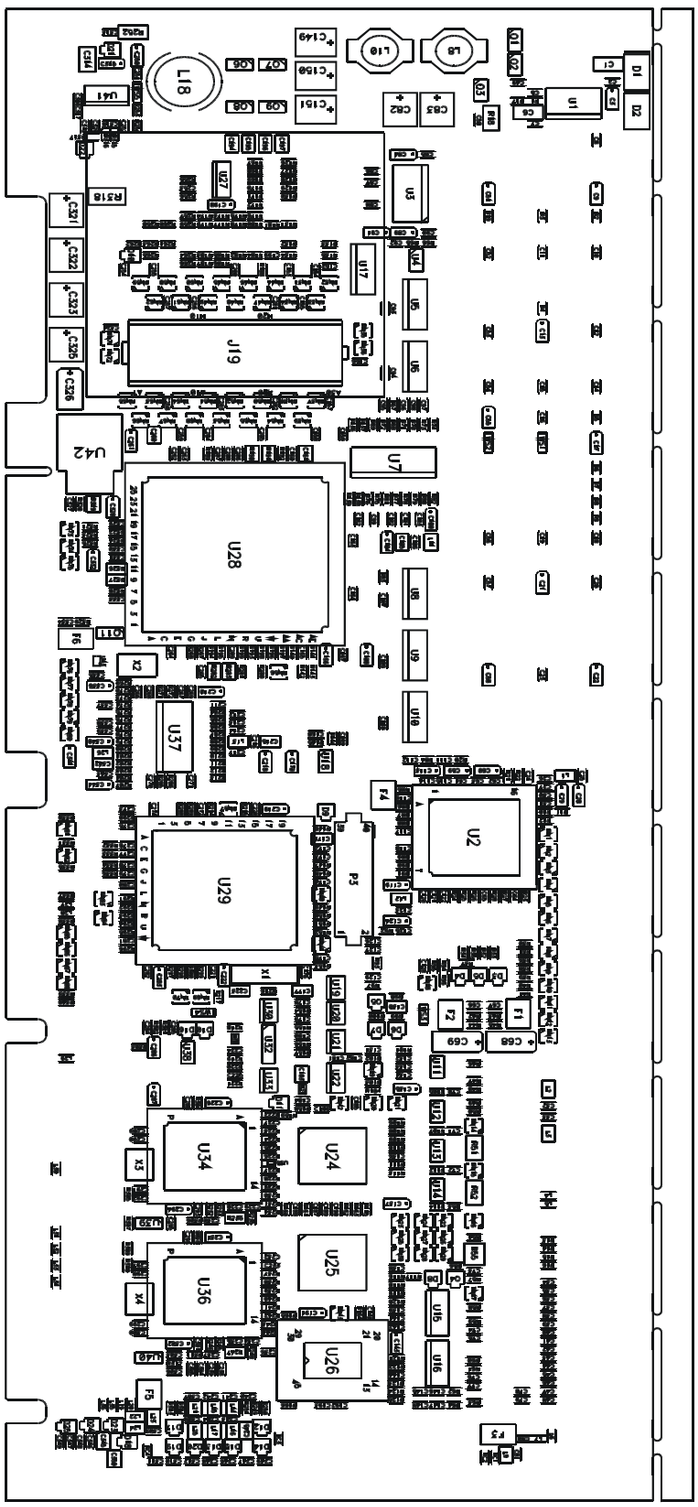
The PCI-948 integrates the functionality of two 8237 DMA controllers. Eight DMA channels are available.

According to Plug and Play standards, the system BIOS automatically allocates DMA Channel 1 or 3 for the ECP mode of the parallel port. Channel 2 is reserved for the floppy controller and Channel 4 is used to cascade Channels 0 through 7 to the microprocessor.

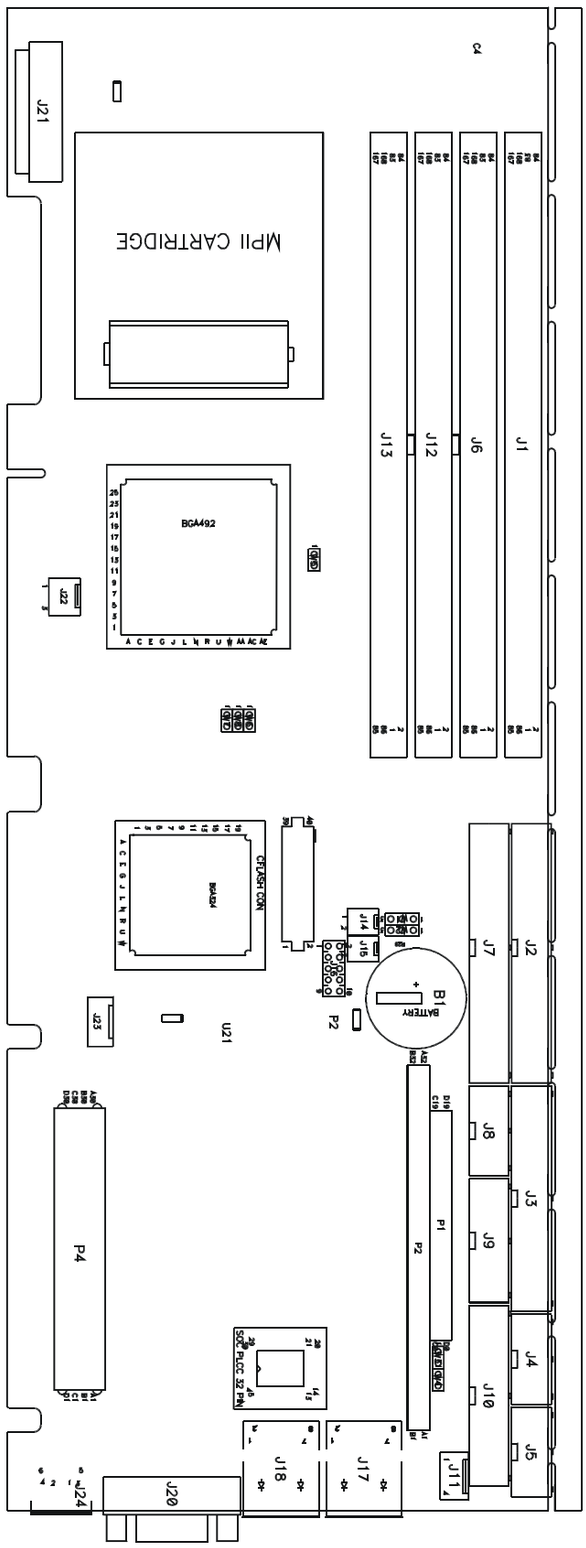
DMA Channel	Function
DMA 0	Available
DMA 1	PnP available (ECP)
DMA 2	Floppy controller
DMA 3	PnP available (ECP)
DMA 4	Cascade controller # 1
DMA 5	PnP available
DMA 6	PnP available
DMA 7	PnP available

C. BOARD DIAGRAMS

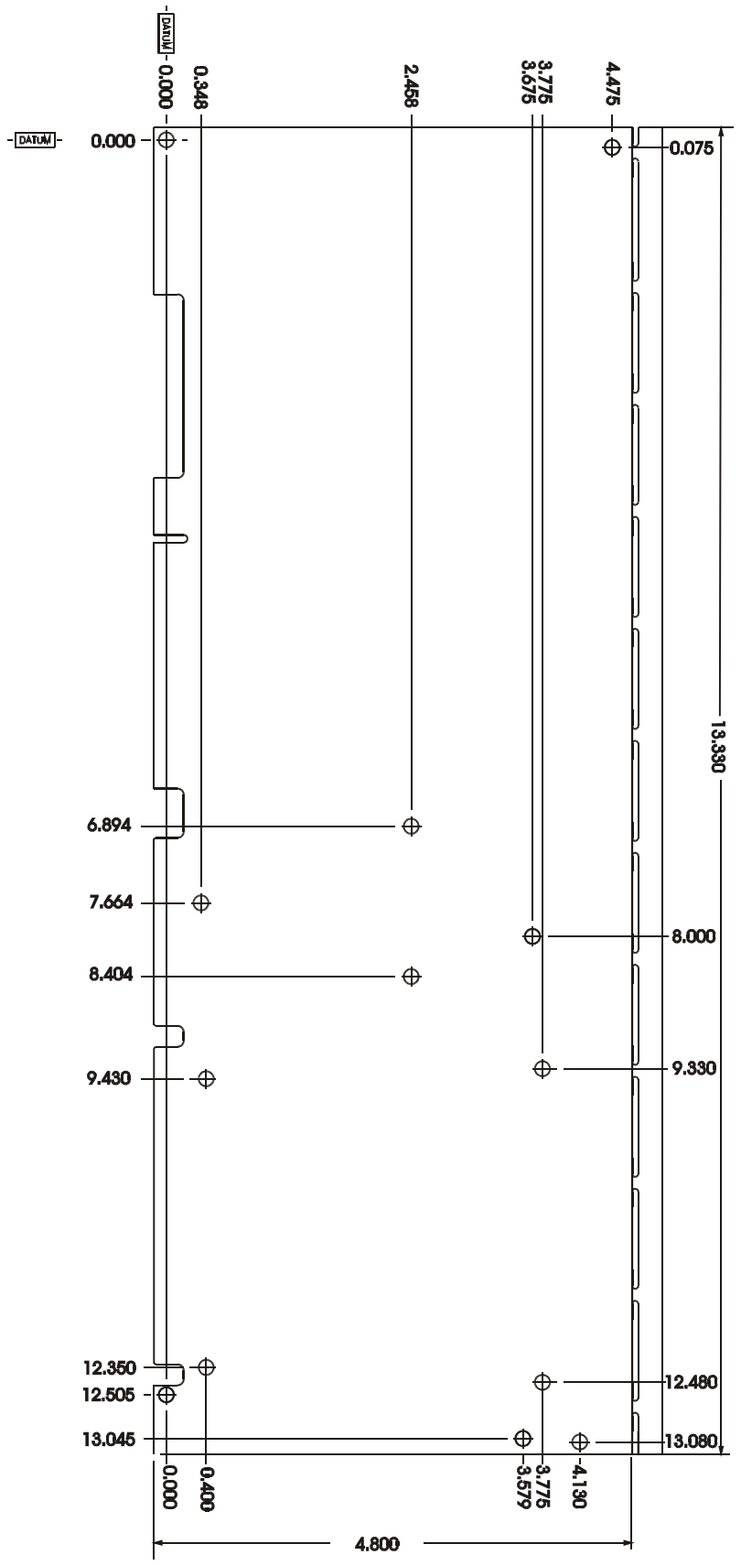
C.1 Assembly Top - PCI-948



C.2 Connector Configuration C.S. - PCI-948



C.3 Mounting Holes - PCI-948



D. CONNECTOR PINOUTS

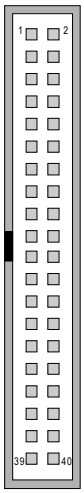
D.1 PCI-948 Connectors and Headers

Connectors and Headers on the PCI-948	
J1, J6, J12, J13	DIMM Memory
J2	Primary IDE Connector
J3	Floppy Disk Connector
J4	Serial Port 1 – RS232
J5	Serial Port 2 – RS232 / RS485
J7	Secondary IDE
J8	USB Port
J9	Keyboard / Speaker
J10	Parallel Port
J11	PS/2 Mouse (on board)
J14	External Battery
J15	Power Button Connector
J16	Hardware Monitor Header
J17	Ethernet 1 (WOL)
J18	Ethernet 2
J20	CRT VGA Connector
J21	External AT Power
J22	CPU Fan
J23	ATX Auxiliary Supply
J24	PS/2 Keyboard and Mouse
P1/P2	PC/104 Connector
P3	CompactFlash Connector
P4	PC/104 Plus Connector
BT1	CMOS Battery Backup connector

D.2 J2/J7 - Primary/Secondary IDE Connectors

Pin Number	Signal
1	RESET#
3	DD7
5	DD6
7	DD5
9	DD4
11	DD3
13	DD2
15	DD1
17	DD0
19	GND
21	DMARQ
23	DIOW#
25	DIOR#
27	IORDY
29	DMACK#
31	INTRQ
33	DA1
35	DA0
37	CS0#
39	LED (DASP#)

Top View



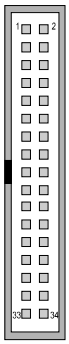
Pin Number	Signal
2	GND
4	DD8
6	DD9
8	DD10
10	DD11
12	DD12
14	DD13
16	DD14
18	DD15
20	Not Connected (KEY)
22	GND
24	GND
26	GND
28	GND (CSEL)
30	GND
32	Not Connected (IOCS16#)
34	Not Connected (PDIAG#)
36	DA2
38	CS1#
40	GND

Active Low Signal

D.3 J3 – Floppy Disk

Pin Number	Signal
1	GND
3	GND
5	GND
7	GND
9	GND
11	GND
13	GND
15	GND
17	Not Connected
19	GND
21	GND
23	GND
25	GND
27	Not Connected
29	PRESENT# (GND)
31	GND
33	Not Connected

Top View



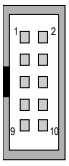
Pin Number	Signal
2	DRVEND#
4	Not Connected
6	Not Connected
8	INDEX#
10	MTR0#
12	FPDS1#
14	FPDS0#
16	MTR1#
18	FPDIR#
20	STEP#
22	WDATA#
24	WGATE#
26	TRK0#
28	WRTPRT#
30	RDATA#
32	HDSEL#
34	DSKCHG#

 # Active Low Signal

D.4 J4, J5 – Serial 1, 2 – RS232

Pin Number	Signal
1	DCD#
3	RXD#
5	TXD
7	DTR#
9	GND

Top View



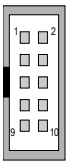
Pin Number	Signal
2	DSR#
4	RTS#
6	CTS#
8	RI#
10	Not Connected

 # Active Low Signal

D.5 J5– Serial Port 2 - RS-485

Pin Number	Signal
1	DCD#
3	RX(-)
5	TX(-)
7	DTR#
9	GND

Top View



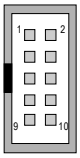
Pin Number	Signal
2	DSR#
4	RX(+)
6	TX(+)
8	RI#
10	Not Connected

 # Active Low Signal

D.6 J8 – Dual USB Header

Pin Number	Signal
1	+5V fused
3	USBP0-
5	USBP0+
7	GND
9	GND

Top View



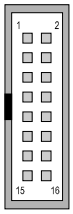
Pin Number	Signal
2	+5V fused
4	USBP1-
6	USBP1+
8	GND
10	GND

D.7 J9 – Keyboard/Speaker Header

Pin Number	Signal
1	KCLK
3	KDATA
5	+5V fused
7	SPKR
9	SOFTOFF#
11	DOWNLD#
13	PBRES#
15	HDACT#

#Active Low Signal

Top View



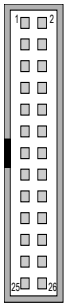
Pin Number	Signal
2	GND
4	GND
6	+5V fused
8	+5V fused
10	GND
12	GND
14	GND
16	+5V fused

D.8 J10 – Parallel Port

D.8.1 Standard Mode

Pin Number	Signal
1	STB#
3	PD0
5	PD1
7	PD2
9	PD3
11	PD4
13	PD5
15	PD6
17	PD7
19	ACK#
21	BUSY
23	PE
25	SLCT

Top View



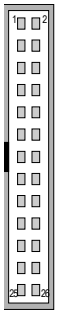
Pin Number	Signal
2	AUTOFD#
4	ERR#
6	INIT#
8	SLCTIN#
10	GND
12	GND
14	GND
16	GND
18	GND
20	GND
22	GND
24	GND
26	GND

 # Active Low Signal

D.8.2 EPP Mode

Pin Number	Signal
1	WRITE#
3	PD0
5	PD1
7	PD2
9	PD3
11	PD4
13	PD5
15	PD6
17	PD7
19	INTR
21	WAIT#
23	N.C.
25	N.C.

Top View



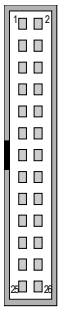
Pin Number	Signal
2	DATASTB#
4	N.C.
6	N.C.
8	ADDRSTRB#
10	GND
12	GND
14	GND
16	GND
18	GND
20	GND
22	GND
24	GND
26	GND

 # Active Low Signal

D.8.3 ECP Mode

Pin Number	Signal
1	STROBE#
3	PD0
5	PD1
7	PD2
9	PD3
11	PD4
13	PD5
15	PD6
17	PD7
19	ACK#
21	BUSY, PERIPHACK[2]
23	PERROR, ACKREVERSE[2]
25	SELECT

Top View



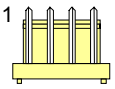
Pin Number	Signal
2	AUTOFD#, HOSTACK[2]
4	FAULT#[1], PERIPHRQST#[2]
6	
8	INIT#[1], REVERSERQST#[2]
10	
12	SELECTIN#[1,2]
14	GND
16	GND
18	GND
20	GND
22	GND
24	GND
26	GND
	GND

 # Active Low Signal, [1] Compatible Mode, [2] High-Speed Mode

D.9 J11 – PS/2 Mouse Header

Signal	Pin #
CLK	1
GND	2
DATA	3
5V fused	4

Front View



D.10 J14 – External Battery Connector

Signal	Pin #
EXTBAT	1
GND	2

Front View



D.11 J15 – Power Button Connector

Signal	Pin #
PWRBTN	1
GND	2

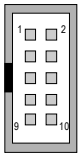
Front View



D.12 J16 - Hardware Monitor Header

Pin Number	
Signal	
GPIO1	1
APFLT#	3
EXTFLT#	5
FANFLT#	7
CHASINT#	9

Top View



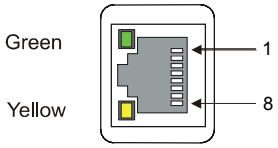
Pin Number	
	Signal
2	GPIO2
4	CPUFLT#
6	GND
8	Not Connected
10	GND

D.13 J17, J18 – Ethernet 1, 2 RJ45 Connector

Signal	
TX+	1
TX-	2
RX+	3
RJ1*	4
RJ1*	5
RX-	6
RJ2*	7
RJ2*	8

** Lines terminated with 75-ohm resistors*

Front View



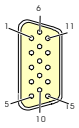
D.14 J20 - CRT VGA Connector

Signal	Pin
RED	1
GREEN	2
BLUE	3
Not Connected	4
GND	5

Signal	Pin
Analog GND	6
Analog GND	7
Analog GND	8
Not Connected	9
GND	10

Signal	Pin
Not Connected	11
SDATA	12
HSYNC	13
VSYNC	14
SCLK	15

Front View



D.15 J21 – AT Power Supply Connector (Optional)

Signal	Pin
VCC	1
VCC	2
-5V	3
GND	4

Top View

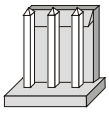


Pin	Signal
5	GND
6	GND
7	-12V
8	+12V

D.16 J22 – CPU Fan

Signal	Pin#
SENSE	1
+5V	2
GND	3

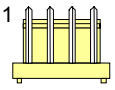
Front View



D.17 J23 – ATX Auxiliary Connector

Signal	Pin
PW-OK	1
5VSB	2
PS-ON	3
GND	4

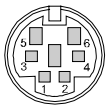
Front View



D.18 J24 – PS/2 Keyboard and Mouse Mini-DIN

Signal	Pin
KBDATA	1
MDATA	2
GND	3
5V fused	4
KBLOCK	5
MCLK	6

Front View



D.19 P3 – CompactFlash™

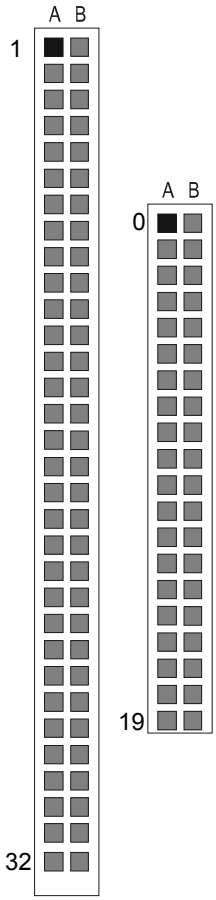
Pin #	Signal Flow	Signal	Pin #	Signal Flow	Signal
1	I/O	DD11	2	-	GND
3	I/O	DD12	4	I/O	DD3
5	I/O	DD13	6	I/O	DD4
7	I/O	DD14	8	I/O	DD5
9	I/O	DD15	10	I/O	DD6
11	O	CS1#	12	I/O	DD7
13	-	DMA ACK#	14	O	CS0#
15	-	DMA RQ	16	O	D IOR#
17	I/O	PDIAG#	18	O	D IOW#
19	I	IRQ15	20	-	VCC (+5V)
21	-	VCC (+5V)	22	-	VCC (+5V)
23	-	GND	24	-	GND
25	O	RESET#	26	-	GND
27	O	C Select	28	O	DA2
29	O	DA1	30	I	#DASP
31	O	DA0	32	-	I/ORDY
33	I/O	DD0	34	I/O	DD8
35	I/O	DD1	36	I/O	DD9
37	I/O	DD2	38	I/O	DD10
39	-	IOCS16#	40	-	GND

 # Active low signal

D.20 P1/P2 – PC/104

	A	B
1	IOCHK#	GND
2	SD7	RESET DRV
3	SD6	VCC
4	SD5	IRQ9
5	SD4	-5V
6	SD3	DRQ2
7	SD2	-12V
8	SD1	0WS#
9	SD0	+12V
10	IOCHRDY	Reserved
11	AEN	SMEMW#
12	SA19	SMEMR#
13	SA18	IOW#
14	SA17	IOR#
15	SA16	DACK3#
16	SA15	DRQ3
17	SA14	DACK1#
18	SA13	DRQ1
19	SA12	REFRESH#
20	SA11	SYSCLK
21	SA10	IRQ7
22	SA9	IRQ6
23	SA8	IRQ5
24	SA7	IRQ4
25	SA6	IRQ3
26	SA5	DACK2#
27	SA4	T/C
28	SA3	BALE
29	SA2	VCC
30	SA1	OSC
31	SA0	GND
32	GND	GND

Top View



C	D	
GND	GND	0
SBHE#	MECS16#	1
LA23	IOCS16#	2
LA22	IRQ10	3
LA21	IRQ11	4
LA20	IRQ12	5
LA19	IRQ13	6
LA18	IRQ14	7
LA17	DACK0#	8
MEMR#	DRQ0	9
MEMW#	DACK5#	10
SD8	DRQ5	11
SD9	DACK6#	12
SD10	DRQ6	13
SD11	DACK7#	14
SD12	DRQ7	15
SD13	VCC	16
SD14	MASTER#	17
SD15	GND	18
Reserved	GND	19

 # Active Low Signal – VCC: +5V

D.21 P4 – PC/104-Plus

	A	B	Top View	C	D	
1	5V_KEY	Reserved	A B C D	VCC	AD00	1
2	VI/O (5V)	AD02	1	AD01	VCC	2
3	AD05	GND		AD04	AD03	3
4	C/BE0#	AD07		GND	AD06	4
5	GND	AD09		AD08	GND	5
6	AD11	VI/O (5V)		AD10	MM66EN	6
7	AD14	AD13		GND	AD12	7
8	VCC3	C/BE1#		AD15	VCC3	8
9	SERR#	GND		SB0#	PAR	9
10	GND	PERR#		VCC3	SDONE	10
11	STOP#	VCC3		LOCK#	GND	11
12	VCC3	TRDY#		GND	DEVSEL#	12
13	FRAME#	GND		IRDY#	VCC3	13
14	GND	AD16		VCC3	C/BE2#	14
15	AD18	VCC3		AD17	GND	15
16	AD21	AD20		GND	AD19	16
17	VCC3	AD23		AD22	VCC3	17
18	IDSEL0	GND		IDSEL1	IDSEL2	18
19	AD24	C/BE3#		VI/O (5V)	IDSEL3	19
20	GND	AD26		AD25	GND	20
21	AD29	VCC		AD28	AD27	21
22	VCC	AD30		GND	AD31	22
23	REQ0#	GND		REQ1#	VI/O (5V)	23
24	GND	REQ2#		VCC	GNT0#	24
25	GNT1#	VI/O (3V)		GNT2#	GND	25
26	VCC	CLK0		GND	CLK1	26
27	CLK2	VCC		CLK3	GND	27
28	GND	INTD#		VCC	RST#	28
29	+12V	INTA#		INTB#	INTC#	29
30	-12V	Reserved	30	Reserved	3.3V_KEY	30

 # Active Low Signal – VCC: +5V – VCC3: +3.3V

E. BIOS SETUP ERROR CODES

E.1 POST Beep

POST beep codes are defined in the BIOS to provide low-level tone indication when an error occurs during the BIOS initialization.

Beep codes consist of a combination of long and short beeps. They are described as follows:

E.1.1 Beep Codes

Post code	Beep Code	Description
41	**-*	Entering the boot block recovery code (i.e. Main BIOS checksum error)

Legend * = 1 Short beep code, ** = 1 Long beep code, - = Silence

E.2 POST Messages

During the Power-On Self-Test (POST), if the BIOS detects an error requiring you to do something to fix, it will either sound a beep code or display a message.

If a message is displayed, it will be accompanied by:

"PRESS F1 TO CONTINUE, DEL TO ENTER SETUP".

E.3 Error Messages

One or more of the following messages may be displayed if the BIOS detects an error during the POST.

CMOS BATTERY HAS FAILED

1. If it is the first boot, check for the onboard battery jumper W4. The board is shipped with W4 jumper set to OFF (onboard battery disconnected). This jumper must be shorted (ON) for proper battery operation.

2. CMOS battery is no longer functional. It should be replaced.

CMOS CHECKSUM ERROR

Checksum of CMOS is incorrect. This indicates that CMOS has become corrupt. A weak battery may have caused this error. Check the battery and replace if necessary.

DISK BOOT FAILURE, INSERT SYSTEM DISK AND PRESS ENTER

No boot device was found. This could mean either a boot drive was not detected or the drive does not contain proper system boot files. Insert a system disk into Floppy Drive A and press Enter. If you assumed the system would boot from the hard drive, make sure the controller is inserted correctly and all cables are properly attached. Also, be sure the disk is formatted as a boot device. Then reboot the system.

KEYBOARD ERROR OR NO KEYBOARD PRESENT

Cannot initialize the keyboard. Make sure the keyboard is attached correctly and no keys are being pressed during the boot.
If you are purposely configuring the system without a keyboard, set the error halt condition in Setup to HALT ON ALL, BUT KEYBOARD. This will cause BIOS to ignore the missing keyboard and continue the boot.

OFFENDING SEGMENT

This message is used in conjunction with the I/O CHANNEL CHECK and RAM PARITY ERROR messages when the segment that has caused the problem cannot be isolated.

PRESS F1 TO DISABLE NMI, F2 TO REBOOT

When BIOS detects a Non-Maskable Interrupt condition, this will allow you to disable the NMI and continue to boot, or you can reboot the system with the NMI enabled.

E.4 POST Codes

POST #	Designation	Description
01	BOOT BLOCK	Boot Block in EMERGENCY: Clear Base Memory Area.
03	Initialize Chips	1. Clear CMOS shutdown byte. 2. Initialize EISA extended registers. (Not for us since we don't have EISA bus.)
04	Test Memory Refresh Toggle	RAM must be periodically refreshed in order to keep the memory from decaying.
05	Blank Video, Initialize Keyboard	1. Clear CMOS reset status byte. 2. Early Keyboard initialization. Boot Block in EMERGENCY: Initialize Keyboard Controller.
06	EPROM Checksum	1. Test F000h segment shadow readable and writeable for POST access correct. If not, show POST FE and beep continuously… 2. Autodetect Flash EPROM.
07	Test CMOS Interface and Battery Status	1. Install the Teknor segment. 2. Verifies CMOS is working correctly (walking bit test). 3. Restore CMOS from Flash if option is enabled. 4. Check for OVERRIDE KEY (INSERT key).
08	Program Chipset default	Program Chipset default (show POST BEh).
09	Early Cache Initialization	1. Check for Intel's and/or Cyrix CPU. 2. Early Cache Initialization when cache is separate from chipset. 3. Turn off Gate A20.
0A	Setup Interrupt Vector Table	1. Initialize first 120 interrupt vectors with SPURIOUS_INT_HDLR and initialize int. 00h-1Fh according to INT_TBL. 2. Early Power Management Initialization.
0B	Test CMOS RAM Checksum	1. Verify time and date for valid values. 2. If Override enabled, check for Override key. If Override key pressed, Kill CMOS checksum. 3. Check CMOS Battery (useless if save CMOS in FLASH enabled since it is already done). 4. Verify Checksum, if bad, load defaults. 5. Copy CMOS in the stack. 6. Clear CMOS Alarm date. 7. Clear HD if Hidden. 8. Clear Floppy "B" if only one drive. 9. Detect for a Math Co-processor. 10. Set Fast Gate A20 Flag in CMOS. 11. If "B" drive only is set the 2 Drive are set… 12. Program Chipset for early Power Management. 13. P6 Bios Update (if applicable). 14. Kill Onboard PnP IO. 15. PnP Early Initialization. 16. PnP System Resource: 1. Get ESCD. 2. Create default SYSTEM_MAP. 3. Decode/Record ISA ESCD resources. 4. Record I/O port for PnP operation. 17. Chipset Early Shadow.

E.4 POST Codes (continued)

POST #	Designation	Description	
0C	Initialize Keyboard	1. Open Xilinx I/O Port location to x90h (X=1,2 or 3) inside the chipset (if necessary).	Boot Block 1st : Verify BIOS checksum.
		2. Disable (if necessary). Thermal Management. 3. Disable (if necessary) Ethernet Chip.Set IDE Detect counter to 0. 4. Set CD-ROM found variable to 0. 5. Initialize zone 40:0h for the keyboard buffer.	Boot Block in EMERGENCY 2nd : Init. vector 00h through 77h.
0D	Initialize Video Interface & Chipset	1. On M1 set the cache for the memory installed. 2. On PCI, do a PCI ROM Init. 3. On P6, Init. Apic. 4. Init. Chipset. 5. Turn ON CPU Cache. 6. Set Maximum Speed. 7. Measure CPU Clock Speed. 8. Restore Speed. 9. Turn Off CPU Cache. 10. Early Video Shadow. 11. Read CMOS location 14h to find out type of video to use. Detect and initialize Video Adapter. 12. Init. T380 if necessary.	Boot Block in EMERGENCY: Try to Init. Video Card…
0E	Test Video Memory	1. If CGA or MONO, test video memory. 2. Beep the speaker. 3. Show the LOGO. 4. Install VT100 driver if necessary. 5. Write sign-on message to screen. 6. Write Copyright message to screen. 7. Write Evaluation message to screen. 8. Show CPU type and speed.	
0F	Test DMA Controller 0	Test DMA Controller 0.	
10	Test DMA Controller 1	Test DMA Controller 1.	
11	Test DMA Page Registers	Test DMA Page Registers.	
12	Reserved	Reserved for 8254 Counter 0 - Not implemented.	
13	Reserved	Reserved for 8254 Counter 1 - Not implemented.	
14	Test Timer Counter 2	Test 8254 Timer 0 Counter 2.	
15	PIC Test 8259-1 mask bits	Verify 8259 Channel 1 masked interrupts by alternately turning off and on the interrupt lines.	
16	PIC Test 8259-2 mask bits	Verify 8259 Channel 1 masked interrupts by alternately turning off and on the interrupt lines.	

E.4 POST Codes (continued)

POST #	Designation	Description
17	Test Struck 8259's Interrupt Bits	Nothing
18	Test 8259 Interrupt functionality	Force an interrupt and verify that the interrupt occurred (IRQ 0 - clock int. 8h).
19	Test Struck NMI Bits (Parity/ IO check)	Nothing.
1A-1E	Reserved	Reserved
1F	Set EISA Mode	If EISA non-volatile memory checksum is good, execute EISA initialization. If no, execute ISA test and clear EISA mode flag. Test EISA Configuration Memory integrity (checksum & communication interface).
20-2F	Enable Slots 0-15	Initialize slot 0 (System Board) to slot 15.
30	Size Base & Extended Memory	Size base memory from 256K to 640K and extended memory above 1MB.
31	Test Base & Extended Memory	1. Test base memory from 256K to 640K and extended memory above 1MB using various patterns. 2. The last test is filling memory with 0's. 3. On a quick memory test or if user press the ESC key while testing memory, only the last test is performed.
32	Test EISA Extended Memory	If EISA Mode flag is set, then test EISA memory found in slots Initialization. NOTE 1: This will be skipped in ISA mode. NOTE 2: This POST also Detect & Report I/O PORTS and also Init. Super IO.
33-3C	Reserved	Reserved
3C	Setup Enable	
3D	Initialize & Install PS/2 Mouse	Detect if mouse is present. Initialize mouse. Install interrupt vector.
3E	Setup Cache Controller	Initialize cache controller.
3F-40	Reserved	Reserved
41	Initialize Floppy Drive & Controller	1. Verify if we should enter setup. If so, enter setup. 2. Initialize floppy disk drive controller and any drive. — Boot Block in EMERGENCY: Scan for Floppy for emergency disk…
42	Initialize Hard Drive & Controller	Initialize hard drive controller and any drive. (Call HD_INSTALL).
43	Detect & Initialize Serial/Parallel/Joystick ports	Initialize any serial, parallel and game ports.
44	Reserved	Reserved
45	Detect & Initialize Math Coprocessor	Initialize Math Coprocessor.
46	Reserved	Reserved
47	Set Speed for Boot	Set Speed for Boot.
48-4C	Reserved	Reserved
4D	Init. PC-Speaker to LINE OUT	Enable access to PC-Speaker to LINE OUT and Enable/Disable it. (T934).
4E	Manufacturing POST Loop or display Messages	1. Reboot if Manufacturing POST Loop pin is set. 2. Otherwise, display any messages (i.e., any non-fatal errors that were detected during POST). 3. Enter SETUP if needed.
4F	Security Check	Ask password security if needed.
50	Write CMOS	Write all CMOS values back to CMOS-RAM and clear screen.

E.4 POST Codes (continued)

POST #	Designation	Description	
51	Pre-Boot Enable	1. Enable Parity checker. 2. Enable NMI. 3. Enable cache before boot.	
52	Initialize Option (ROM scan)	1. Call POST 81 2. Initialize any ROMs present from C8000h to DBFFFh. Disable POST code from segment E0000h. 3. Initialize any ROMs present from DC000h to E0800h. NOTE: When FSCAN option is enabled, will initialize from C8000h to F7FFFh.	
53	Initialize Time Value	Initialize Time value in 40h: BIOS area.	
54-5F	Reserved	Reserved	
60		Store boot partition of head & cylinder.	
61	Final Init	For last µs detail before boot.	
62	Num Lock ON	Put Num Lock ON and Daylight Saving.	
63	Boot Attempt	1. Call POST 82. 2. Set Low stack. 3. Boot via int 19h.	
64-7F	Reserved	Reserved	
80	Teknor Segment Move 1	Install the Teknor segment from Flash to DC00:0h.	
81	Teknor Segment Move 2	Install the Teknor segment from DC00:0h to 7000:0h.	
82	Teknor Segment Move 3	Install the Teknor segment from 7000:0h to EC00:0h.	
83	Check & Program CPLD	Check & Program CPLD for valid UserCode & IDCode.	
84	Teknor CRC Check	Check if Teknor block has a valid CRC. If not, the Emergency procedure is launched.	
85-AF	Reserved	Reserved	
B0	Spurious	If interrupt occurs in protected mode.	
B1	Unclaimed NMI	If unmasked NMI occurs, display: Press F1 to disable NMI, F2 reboot.	
B2-BD	Reserved	Reserved	
BE	Early Prog Chipset Def.	Going to early program chipset to default values (called from POST_8s).	
BF	Program Chip Set	Called early at POST 0Dh to program chipset from CT-TABLE.	
C0	Turn ON/OFF Cache	OEM Specific - Cache control.	Boot Block: First POST.
C1	Memory presence	OEM Specific - Test to size on-board memory test.	Boot Block: Search for Boot Block Signature “*BBSS*”.
C2	Early Memory Initialization	OEM Specific - Board Initialization.	
C3	Extended Memory Initialization	OEM Specific - Turn ON extended memory DRAM select.	Boot Block: Expand compressed BIOS
C4	Special Display Switch Handling	OEM Specific - Display/Video switch handling so that display switch errors never occur.	
C5	Early Shadow	OEM Specific - Early Shadow enable for fast boot.	Boot Block: Early Shadow System BIOS.
C6	Cache Programming	OEM Specific - Routine for programming which region are cacheable.	Boot Block: Cache Sizing
C7	Reserved	Reserved	
C8	Special Speed Switching	OEM Specific - Routine to handle speed switching.	
C9	Special Shadow Handling	OEM Specific - Normal Shadow routine.	

E.4 POSTCodes (continued)

POST #	Designation	Description
CA	Very Early Initialization	OEM Specific – Initialize hardware before any other hardware initialization.
CB-CF	Reserved	Reserved
D0	Power Management Full speed	Trying to go back or into full speed mode.
D1	Power Management -- Doze mode	Trying to go or in Doze mode.
D2	Power Management --Sleep mode	Trying to go or in Sleep mode.
D3	Power Management – Suspend mode	Trying to go or in Suspend mode.
D4-DF	Debug	Available POST codes for use by source code customers during development.
E0	Reserved	Reserved
E1-EE	Setup Page	Page 1 to Page 14
EF	Shadow Error	In POST 6 to signal a Shadow Error.
F0-FE	Reserved	Reserved
FF	Boot	The system is now booted or waiting for an OS.

F. EMERGENCY PROCEDURE

Follow this procedure only in case of emergency such as a critical error occurred during the Boot Block Flash BIOS update (when using UBIOS utility program or if you meet one of the following symptoms at anytime):

1. No POST code on a power up (when using a POST card).
2. System stops at POST 41(when using a POST card) and associated beep code is generated (Refer to Section E.1).
3. Board does not boot, even after usual hardware and connection verifications.

Post code	Beep Code	Description
22	*-*-*	Error when getting the boot block flash ID code
33	*-*-*-*	Error when erasing the boot block flash
44	*-*-*-*-*	Error when programming the boot block flash
55	*-*	Success of the boot block recovery code. The board is ready to be manually reset.

F.1 How to run Emergency Procedure

To run an EMERGENCY PROCEDURE, proceed as follows:

1. Remove battery jumper.
2. Disable the Power Fail Detection function.
3. Connected a 1.44MB floppy drive (drive A) to the board, and insert the EMERGENCY diskette, that you previously created, in it.
4. Power on the board. (Note that no VGA is present during this procedure.)
5. Boot block flash update will be completed when the POST code 55 is displayed (when using a POST card) or the associated beep code sounds (indicated in Section E-5).
6. After the procedure is successfully completed, power down the board, install your battery and Power Fail Detection jumpers.

The boot block flash BIOS should be correctly programmed and the system should run properly.

 NOTE See Section F.2 Generate an Emergency Floppy Diskette.

F.2 Generate an Emergency Floppy Disk

Use a system that has a 1.44 Mbytes floppy drive A.

1. Insert the Teknor Emergency Diskette in drive A:
2. Copy the two files WDISK.COM and EMERDISK.TEK from drive A: to your hard drive (those files are available on Teknor's CDROM).
3. Insert a DOS formatted floppy disk in drive A.
4. At the DOS prompt of your hard drive (same path of the two files WDISK.COM and EMERDISK.TEK), type WDISK EMERDISK.TEK then press Enter key.
5. The program may display one of the following messages:

   "Emergency Code transferred"
   The emergency diskette has been successfully created. Take the appropriate actions and restart from the step 4) when you see the following messages.

   "Write to disk failure!"
   Verify if your floppy diskette is write-protected.

   "The file to program in flash was not found"
   Be sure that EMERDISK.TEK file is in your current path.

   "Unable to read the binary file" or "Unable to close the opened file"
   Possible floppy diskette corruption or bad data transfer between floppy disk and host system.

   "Unable to allocate a memory block of 256 Kbytes"
   Not enough memory to run the WDISK program.

G. GETTING HELP

At Teknor, we take great pride in our customer's successes. We strongly believe in providing full support at all stages of your product development.

If at any time, you encounter difficulties with your application or with any of our products, or if you simply need guidance on system setups and capabilities, you may contact our Technical Support department at:

CANADIAN HEADQUARTERS
Tel. (450) 437-5682
Fax: (450) 437-8053

If you have any questions about Teknor, our products or services, you may reach us at the above numbers or by writing to:

Teknor Applicom inc.
616 Curé Boivin
Boisbriand, Québec
J7G 2A7 Canada

LIMITED WARRANTY

TEKNOR APPLICOM INC, ("The seller") warrants its boards to be free from defects in material and workmanship for a period of two (2) years commencing on the date of shipment. The liability of the seller shall be limited to replacing or repairing, at the seller's option, any defective units. Equipment or parts, which have been subject to abuse, misuse, accident, alteration, neglect, or unauthorized repair are not covered by this warranty. This warranty is in lieu of all other warranties expressed or implied.

RETURNING DEFECTIVE MERCHANDISE

If your Teknor product malfunctions, please do the following before returning any merchandise:

1) Call our Technical Support department in Canada at (450) 437-5682. Make certain you have the following at hand:

   - The Teknor Invoice number
   - Your purchase order number
   - The serial number of the defective board.

2) Give the serial number found on the back of the board and explain the nature of your problem to a service technician.

3) If the problem cannot be solved over the telephone, the technician will further instruct you on the return procedure.

4) Prior to returning any merchandise, make certain you receive an RMA number from Teknor's Technical Support and clearly mark this number on the outside of the package you are returning. To request a number, follow these steps:

   - Make a copy of the request form on the following page.
   - Fill out the form and be as specific as you can about the board's problem.
   - Fax it to us.

5) When returning goods, please include the name and telephone number of a person whom we can contact for further explanations if necessary. Where applicable, always include all duty papers and invoice(s) associated with the item(s) in question.

6) When returning a Teknor board:

   i) Make certain that the board is properly packed: Place it in an antistatic plastic bag and pack it in a rigid cardboard box.

   ii) Ship prepaid to (but not insured, since incoming units are insured by Teknor):

Teknor Applicom inc.
616 Curé Boivin
Boisbriand, Québec
J7G 2A7 Canada

RETURN TO MANUFACTURER
AUTHORIZATION REQUEST

Contact Name	:	_____			
Company name	:	_____			
Street Address	:	_____			
City	:	_____	Province/State	:	_____
Country	:	_____	Postal/Zip Code	:	_____
Phone Number	:	_____	Extension	:	_____
Fax Number	:	_____			

Serial Number	Failure or Problem Description	P.O.# (if not under warranty)

Fax this form to Teknor's Technical department in Canada at (450) 437-8053