V1553B

MIL-STD-1553 Interface Module
for the VMEbus

User's Manual
Publication No. 12961
Issue 1

Unpacking and Special Handling Instructions

This PepCard product has been carefully designed for a long and a fault-free life; however, its life expectancy can be drastically reduced or even diminished to none by improper treatment at the unpacking or first-use stage.

We therefore ask you to read this manual carefully before unpacking the module or fitting it into your VMEbus or IIOC/Eurobus system.

If the product contains primary or secondary batteries for RTC or memory back-up purposes, extra care is required not to place the board on conductive surfaces; including anti-static plastic or sponge, which can cause shorts and lead to damage to the batteries or the tracks on the board.

Further, please do not exceed the operational temperature ranges given in the specifications for the board version you ordered. Where batteries are present, their temperature restrictions must also be taken into account.

When fitting the board into a system, remove all power by turning off the power mains. Do not disconnect the mains however, since grounds connection prevents chassis floating with static voltages, which could damage the board as you push it home.

Keep all of the original packaging material for future storage or warranty shipments of the board. If it is necessary to store or ship the board, please repack the board in the same way it was originally packaged.

We wish you, your application, and your PepCard a long and successful life. We are certain that if you take the time to read through this manual first, you will most probably save yourself time and aggravation later.

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Revision History				
Manual/Product Title	V1553B User's Manual			
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Date of issue = the release date of the issue. This date does not necessarily reflect the date the improvements were first made.

A thick bar to the left of any text indicates that the text has changed from the previous issue of the manual.

A double thin bar to the left of any text indicates that new text (paragraphs) has been added.
Changes and additions to drawings and boxed text, such as notes or jumper setting tables, cannot be marked in the above way; therefore this marking system is used only for changes to "normal" body text.

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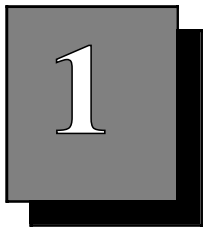
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1. INTRODUCING THE V1553B

1.1 Product Overview

The V1553B circuit card assembly is a 3U VME compatible A24/D16 interrupt capable board with one or two separate dual redundant MIL-STD-1553-B interfaces. Each 1553 interface has the capability to time-tag incoming messages. A 16-bit programmable register can be either clocked internally or via an external oscillator source connected through the front panel. The internal clock source is accurate to within 2µs. Each 1553 interface has an 8 kByte dual-ported RAM buffer that is accessible by a host processor on the VME interface.

The V1553B offers the user all the functions he requires, to be able to use his VMEbus in a Bus Controller (BC), Remote Terminal Unit (RTU) and bus Monitor (MT) mode in conjunction with this DoD standardized bus.

The V1553B module with its interfaces, transformers and transceivers provides serial communication to either this Military standard bus, or to field busses on a Manufacturing Automation Protocol (MAP) network.

Further to its roles in military or naval systems, applications for this bus are found in harsh environments such as oil drilling industry where it could be used to monitor drill bit conditions down the well, the nuclear reactor industry for critical process control etc.

1.2 Ordering Information

The V1553B is available as a single slot PepCard module operating within the E2 (-40ºC to +85ºC) temperature range.

Table 1.2 V1553B Ordering Information

Product	Description	Order No.
V1553B	VMEbus to 1553A/B bus single board interface, with two separate dual redundancy serial interfaces and full status control LEDs	11263
V1553B	VMEbus to 1553A/B bus single board interface, with two dual redundancy serial ports and full status control LEDs.	11264
V1553-DS	V1553B MIL-STD-1553 components: Data-sheet for BU61580, BU29854 and user's guide for BU61580	12980
V1553B-LIB	V1553B MIL-STD-1553 interface library for easy programming of the V1553B board in Bus Controller, Remote Terminal and Bus Monitor modes.	12979

V1553B is also available with a 6U Front panel, to be fitted into double-height systems.

1.3 Specifications of the V1553B

Controller:	BU61580 from DDC
Protocol Modes:	Bus-Controller (BC)
	Remote Terminal Unit (RTU)
	Bus Monitor (MT)
Mode Selection:	Software programmable
RAM Size:	4k x 16 Shared RAM
Oscillator Frequency:	16.0 MHz
MIL-STD-1553 Channels:	One / two serial, dual-redundancy, channels (A & B) each with their own connectors for standard Twin-axial cable, using Trompeter BJ77 connectors.
Interfacing to 1553 Bus:	Jumper Selectable, for short stub (direct coupled) or for long stub (transformer coupled).
Time Tag Counter:	16-Bit read/write counter with 2, 4, 8, 16, 32 or 64µs per LSB resolution. May be clocked externally or may be incremented per software.
Command Illegalization:	Software programmable.
Interrupts (VMEbus):	Software programmable
Levels:	IRQ1* to IRQ7*
Address Modifier:	Supports Standard and Short Defined AM codes.
VMEbus Interface:	A24:D16 Slave
Power Requirements: (25% Duty Cycle)	+5V DC (±5%), (500 mA max.) < 5W -12V DC (±10%), (200 mA max.) < 5W
Temperature Ranges Operating:	 -25° to +85°C (extended E2)
Storage:	-55° to +165°C
Operating Humidity:	0 to 95% (non-condensing)
Board Size:	Single-height Eurocard 100 x 160mm (4 x 6 1/4")
VMEbus Connector:	DIN 41612 style C, 96 contacts, P1 connector
Front Panel Width:	4 HP (20.3mm), 1 slot
Front Panel Functions:	Two / four Twin-axial 1553 standard connectors; input for external Time-Tag clock.
On-Board LEDs	Fail indicator (Red LED) Bus Active indicator (Yellow LED) Power ON indicator (Green LED)

* Active low signals,

1.4 Related Publications

For more information regarding the V1553B, and VMEbus products in general, please refer to the VMEbus Specifications.

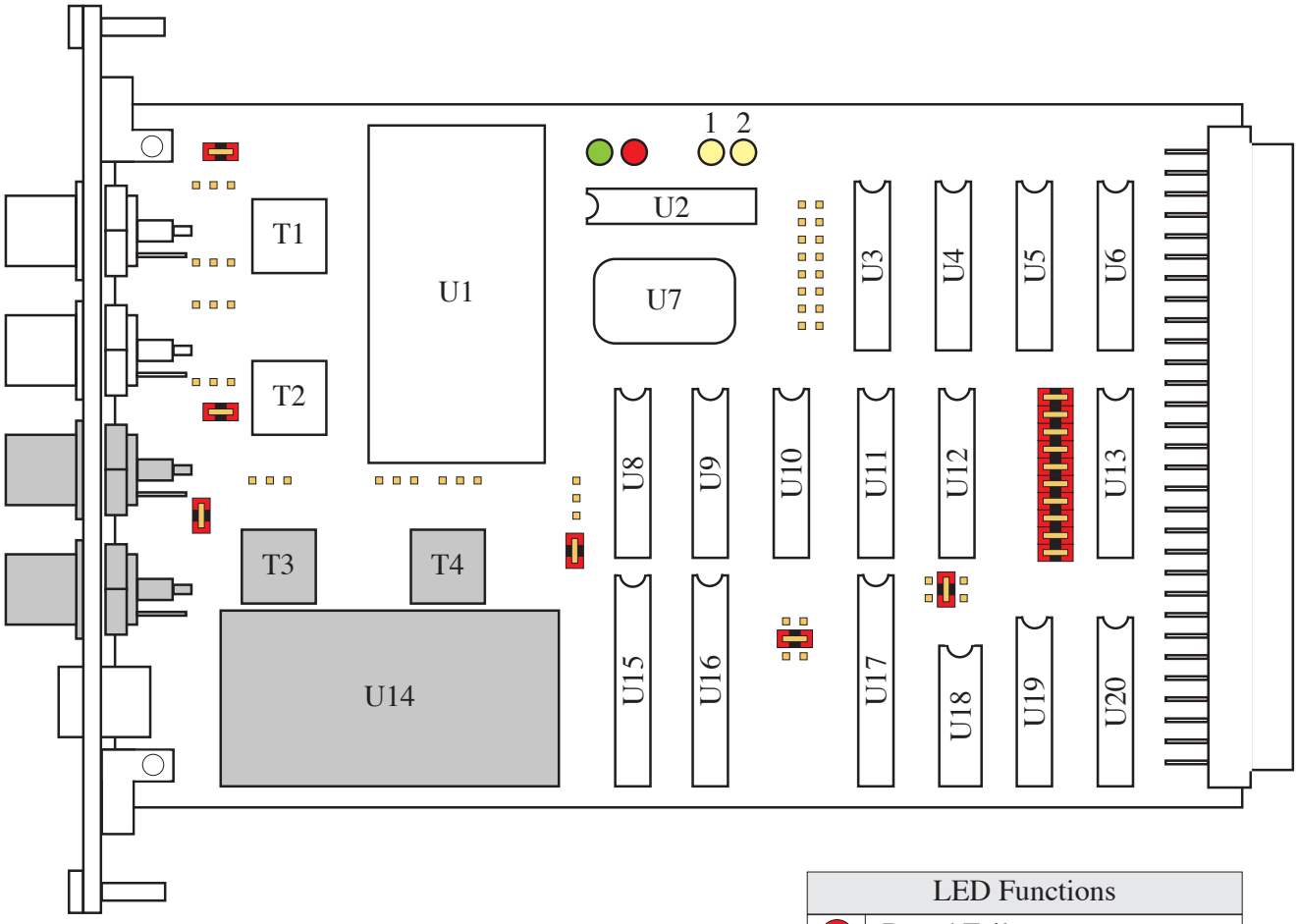
For information about the 1553 bus, please refer to the ANSI specifications or the DDC designers guide.

For information about the BU61580 chip, please refer to the data sheet or to the designers guide available from DDC.

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1.5 Board Overview

Figure 1.5 V1553B Board Overview



LED Functions	
	Board Failure
	Board Power ON
	Bus 1 Active
	Bus 2 Active

Items marked on order are only available number 11263

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A considerable amount of the V1553B's circuits are contained in the BU61580 Advanced Communication Engine (ACE) hybrid device.

Two "BNC" style twin-axial connectors per channel give an easy "bayonet lock" connection of the shielded-twisted-pair leads, having in each, a male and a female pin for the differential serial signals. The connector bodies are isolated from the front panel and each other with isolation washers.

Behind each pair of the two front-panel twin-axial connectors of the V1553B, are two transformers providing an option for balanced line transformer isolation, for improved noise immunity, etc. An option allows the center tap of the output winding of either to be connected to the shield of their respective leads.

Four status LEDs on the circuit board provide status information of the V1553B.

An on-board mounted 16 MHz crystal oscillator allows an option for the V1553B to function independently of the VMEbus SYSCLK signal, if desired, by simple jumper selection.

1.6 Features of the V1553B Module

The V1553B utilizes the BU61580 Hybrid module to meet the needs of Military specifications/applications.

The 1553 bus offers very fast (1MHz) Manchester II, Pulse Coded Modulation (PCM) on a serial bus, over shielded twisted pair cables thus presenting a simplified interconnection, together with rigid standards, ensuring high noise immunity and high degrees of fault isolation for military LAN's, test and control systems, etc.

The single-height* size of this module and other PepCards allows a very compact VMEbus system to be created, and if necessary, contained in smaller "Tempest" cabinets than many of its contemporary 6U modules leading to a considerable saving in both cost and size/weight.

1.7 Typical V1553B Applications

In conjunction with PEP's single board computers, e.g. the VSBC-4, the V1553B may be used as a very compact control or monitoring computer in vehicle, ship, or aircraft-based applications.

Connecting VMEbus hardware and peripherals to 1553 systems in order to analyze or develop hardware/software solutions between these two standards.

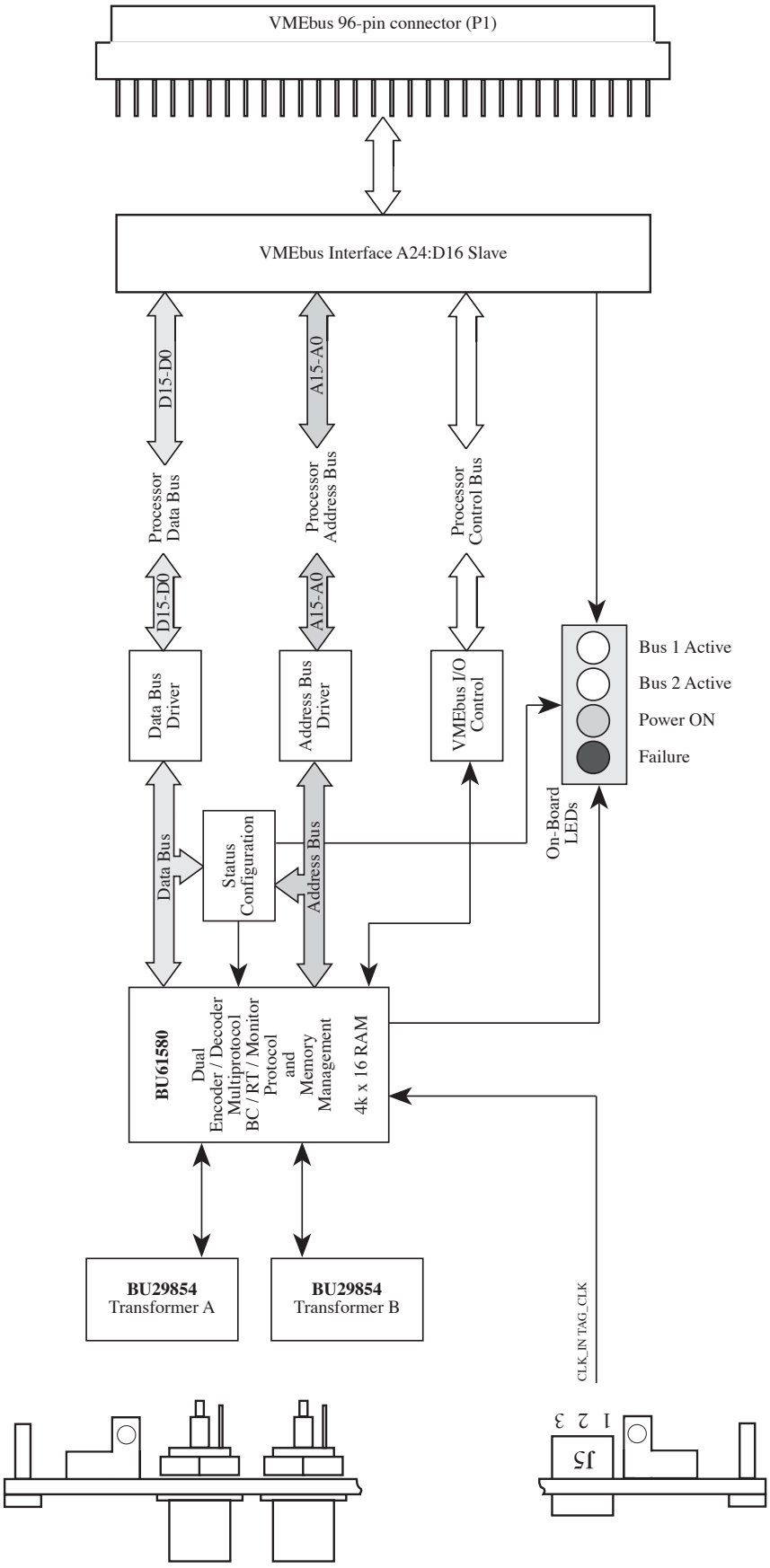
Providing VMEbus Interface to 1553 "field bus" in MAP LAN networks.

Providing long sensor paths to "down hole" sensors in the oil drilling industry, where wear sensors encapsulated into drilling bits can feed back data on the bit condition and/or geological data, such as changes in rock hardness, etc.

*An optional 6U front panel permitting the V1553B to be used in double-height systems is available on request.

1.8 Functional Block Diagram of the V1553B

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VMEbus 96-pin connector (P1)
VMEbus Interface A24:D16 Slave
D15-D0
A15-A0
Processor Data Bus
Processor Address Bus
Processor Control Bus
D15-D0
A15-A0
Data Bus Driver
Address Bus Driver
VMEbus I/O Control
Bus 1 Active
Bus 2 Active
Power ON
Failure
On-Board LEDs
Data Bus
Status Configuration
Address Bus
BU61580
Dual Encoder / Decoder Multiprotocol BC / RT / Monitor Protocol and Memory Management
4k x 16 RAM
BU29854
Transformer A
BU29854
Transformer B
CLK_IN TAG_CLK
J5
1 2 3

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2. FUNCTIONAL DESCRIPTION

2.1 Definition

The V1553B fully implements the 1553 A and B bus protocol with slave and interrupt capability together with the utilization of shared RAM on the 1553 interface chip to buffer 1553 bus data. The board also has miscellaneous control/status registers, status LEDs, and configuration jumpers.

2.2 Characteristics

2.2.1 Performance Characteristics

2.2.1.1 1553 Bus Interface

The 1553 bus interface equipped with a BU61580 interface control circuit performs either the Bus Controller, Monitor Terminal, or the Remote Terminal functions. The operating modes of the BU61580 are described in detail in the "BU-61580 ADVANCED COMMUNICATION ENGINE" data sheet from Data Device Corporation (DDC). The V1553B is fully compatible with MIL-STD-1553 revision A and B with time stamps required for each frame of data received over the 1553 bus. The time-tag register is incremented by either the V1553B on-board oscillator, or by a clock input via the front panel J5 connector. The 1553 interface transformers can be configured for either short or long stub coupling via jumpers J10-J13 for channel 1 and J17-20 for channel 2. The center tap of the 1553 transformers can be connected to ground by installing J14, J15 for channel 1 and J21, J22 for channel 2.

2.2.1.2 VMEbus Interface

The V1553B has a A24/D16 VME slave interface with interrupt capability and is addressable in either short supervisory, short non-privileged, standard supervisory data, standard non privileged data or user defined data space (J6). The VME base address is jumper programmable via J8 and the VME interrupt level is programmable between IRQ 1,2,3,4,5,6, and IRQ7 from the VMEbus.

2.2.1.3 Shared RAM

Each BU61580 has 4k by 16 bits of internal shared RAM which is accessible by both the BU61580 and the VMEbus CPU.

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2.2.1.4 Control/Status Registers, Jumpers and LEDs

The V1553B possesses two configuration/status registers, the VME Configuration Register (VCR) and the 1553 Bus Configuration Register (BCR). The VME interrupt vector (b15-b9), and the IRQ level (b7-b5 for IRQ1 through IRQ7) are selectable by writing to the VCR, while the Board revision (b7-b5) and configuration (b4-b0) can be accessed through a read of the VCR. Board revision and configuration are selectable through jumper J9. Bit definitions for the VCR are in Tables 2.2.1.4a and 2.2.1.4b.

Table 2.2.1.4a VME Configuration Register (VCR) - Word Write

Bits b8, b3, b2, b1, b0 : Spare

Setting	Name	Description
b8, b3, b2, b1, b0	N/A	Not used

Bit b4 : Fail LED Control

Setting	Name	Description
0	*FAIL_LED*	*LED ON (default)*
1		LED OFF

Bits b7 - b5 : VME Interrupt Priority Level

Setting	Name	Description
0	IP_LV(2..0)	*Disabled (default)*
1		IRQ1*
2		IRQ2*
3		IRQ3*
4		IRQ4*
5		IRQ5*
6		IRQ6*
7		IRQ7*

Bits b15 - b9 : VME Interrupt Vector

Setting	Name	Description
0	*I_VEC(7..0)*	*The number stored in this register will be presented to the bus master when an interrupt from the V1553B is acknowledged. Default is a value of 00.*

Table 2.2.1.4b VME Configuration Register (VCR) - Word Read

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Bits b4 - b0 : 1553 Configuration

Setting	Name	Description
	BRD_CFG(4..0)	This value is jumper selectable via J9

Bits b7 - b5 : 1553 Revision Number

Setting	Name	Description
	BRD_REV(2..0)	This value is jumper selectable via J9

Bits b15 - b8 : Spare

The Remote Terminal (RT) address (b7-b2) and the sub-system flag (b0) are write only bits on the BCR. The RT address consists of 5 address bits (b6-b2) and one odd parity bit (b7). Bit definitions for the BCR are in Tables 2.2.1.4.c and 2.2.1.4d.

Table 2.2.1.4c 1553 Bus #1 Configuration Register (BCR1) - Word Write

Bit b0 : Bus #1 Sub-System Flag Control

Name	Description
SSFLG1*	

Bit b1 Spare

Bits b6 - b2 : Remote Terminal Address for Bus #1

Name	Description
RT1_AD(4..0)	When used as a Remote Terminal on the 1553 bus, this value represents the RT's address.

Bit b7 : RT Address Parity for Bus #1

Name	Description
RT1ADP	This bit MUST be set to ODD parity

Table 2.2.1.4d 1553 Bus #2 Configuration Register (BCR2) - Word Write

Bit b0 : Bus #2 Sub-System Flag Control

Name	Description
SSFLG2	

Bit b1 Spare

Bits b6 - b2 : Remote Terminal Address for Bus #2

Name	Description
RT2_AD(4..0)	When used as a Remote Terminal on the 1553 bus, this value represents the RT's address.

Bit b7 : RT Address Parity for Bus #2

Name	Description
RT2ADP	This bit MUST be set to ODD parity

Jumpers J10-13 and J17-20 are for selecting long or short 1553 stubs for channels 1 and 2, respectively. Jumpers J14, J15 and J21, J22 are for selecting grounded or not grounded center tap for A and B busses on channels 1 and 2. The board has status LEDs to indicate Channel 1 and Channel 2 1553 active, power on, and fail. The fail LED is controlled by bit b4 of the VCR. Table 2.2.1.4e has jumper definitions with defaults shown in italics.

Table 2.2.1.4e Jumper Definitions

Jumper J6 : Address Modifier Select

Setting	Description
1-2	AM3
3-4	AM4
5-6	AM5

Default is for these jumpers not to be set for standard/user/data (HEX 39/3A/3D/3E)

Jumper J7 : Dual Channel Select

Setting	Description
1-2	Single 1553 Mode
3-4	*Dual 1553 Mode*
5-6	Single 1553 Mode

Jumper J8 : Address

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Setting	Description	
1-2	A14	
3-4	A15	
5-6	A16	
7-8	A17	
9-10	A18	
11-12	A19	
13-14	A20	
15-16	*A21*	*This provides the default address of $87FE0000. Setting 19-20 is only useful in single channel mode*
17-18	*A22*	
19-20	*A23*	

Jumper J9 : Board Revision / Configuration

Setting	Description
1-2	C0
3-4	C1
5-6	C2
7-8	C3
9-10	C4
11-12	R0
13-14	R1
15-16	R2

Jumper J10 : 1553 Channel 1A + Coupling Mode

Setting	Description
1-2	*Long Stub*
2-3	Short Stub

Jumper J11 : 1553 Channel 1A - Coupling Mode

Setting	Description
1-2	*Long Stub*
2-3	Short Stub

Jumper J12 : 1553 Channel 1B + Coupling Mode

Setting	Description
1-2	*Long Stub*
2-3	Short Stub

Jumper J13 : 1553 Channel 1B - Coupling Mode

Setting	Description
1-2	*Long Stub*
2-3	Short Stub

Jumper J14 : 1553 Channel 1 XFMR A Center Tap

Setting	Description
Present	Center Tap grounded
Absent	*Center Tap floating*

Jumper J15 : 1553 Channel 1 XFMR B Center Tap

Setting	Description
Present	Center Tap grounded
Absent	*Center Tap floating*

Jumper J17 : 1553 Channel 2A + Coupling Mode

Setting	Description
1-2	*Long Stub*
2-3	Short Stub

Jumper J18 : 1553 Channel 2A - Coupling Mode

Setting	Description
1-2	*Long Stub*
2-3	Short Stub

Jumper J19 : 1553 Channel 2B + Coupling Mode

Setting	Description
1-2	*Long Stub*
2-3	Short Stub

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Jumper J20 : 1553 Channel 2B - Coupling Mode

Setting	Description
1-2	*Long Stub*
2-3	Short Stub

Jumper J21 : 1553 Channel 2 XFMR A Center Tap

Setting	Description
Present	Center Tap grounded
Absent	*Center Tap floating*

Jumper J22 : 1553 Channel 2 XFMR B Center Tap

Setting	Description
Present	Center Tap grounded
Absent	*Center Tap floating*

2.2.1 Internal Interface Description

Each BU61580 contains 4k words of shared RAM. This RAM can be accessed by either the BU61580 or the VME master processor. For a detailed description of the internal workings of the BU61580 see the "BU61580 BC/RT/MT ADVANCED COMMUNICATION ENGINE 'ACE'" data sheet from Data Device Corporation.

2.2.2 External Interface Description

The V1553B connects to the VMEbus via the P1 backplane. The base memory address is jumper programmable. Table 2.2.3a shows an address map of the V1553B.

Table 2.2.3a VME Address Map

Address	Function
XXXX XXXX XX00 0000 0000 0000	Base Address - see J8
Base + 0000 (hex)	VME Configuration Reg. (word)
Base + 0002 (hex)	1553 Configuration #1 Reg. (word)
Base + 0004 (hex)	1553 Configuration #2 Reg. (word)
Base + 1000 - 103E (hex)	BU61580 #1 Config. Reg. (word)
Base + 2000 - 3FFE (hex)	BU61580 #1 Shared Ram (word)
Base + 5000 - 503E (hex)	BU61580 #2 Config. Reg. (word)
Base + 6000 - 7FFF (hex)	BU61580 #2 Shared Ram (word)

The 1553 bus signals are input/output via front panel connectors J1 (Channel 1, Bus A) , J2 (Channel 1, Bus B), J3 (Channel 2, Bus A), and J4 (Channel 2, Bus B). There is also a front panel time tag connector, J5. Table 2.2.3b lists the 1553 bus pinouts, Table 2.2.3c lists the signals on the time tag connector.

Table 2.2.3b 1553 Connector Pinouts (J1 - Bus 1A, J2 - Bus 1B, J3 - Bus 2A, J4 - Bus 2B)

Pin Number	Pin Function
1	1553 Bus -, Input to Transceiver
2	1553 Bus + Input to Transceiver
3	Bus Shield (to GND)

Table 2.2.3c Time Tag Connector Pinouts (J5)

Pin Number	Function
1	TCLK_RTN, Return for external Time-Tag clock, signal GND
2	1000PPS, External Time-Tag clock, TTL buffered input
3	Spare

Power is provided via the VMEbus P1 connector. The V1553B shall require the following DC voltages:

+5V DC (500 mA max.)
-12V DC (200 mA max.)

Total power dissipation is less than 5 watts given a 25% 1553 bus duty cycle.

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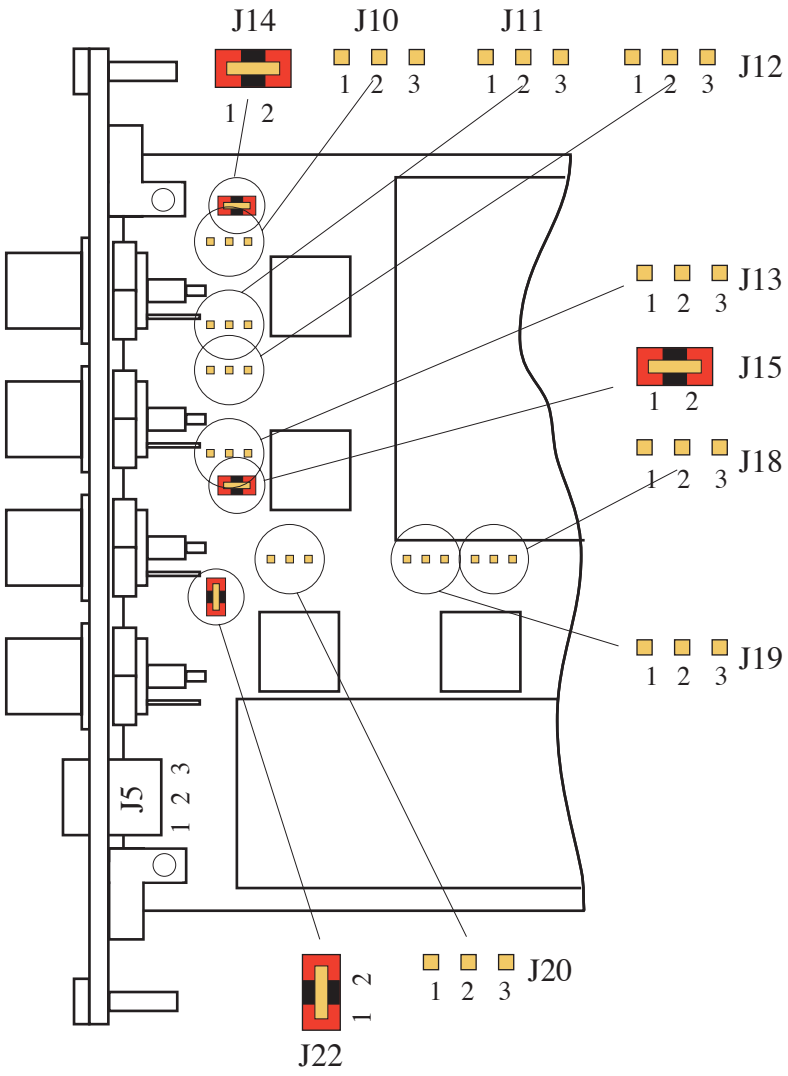
3. CONFIGURING THE V1553B MODULE

3.1 Jumper locations and functions

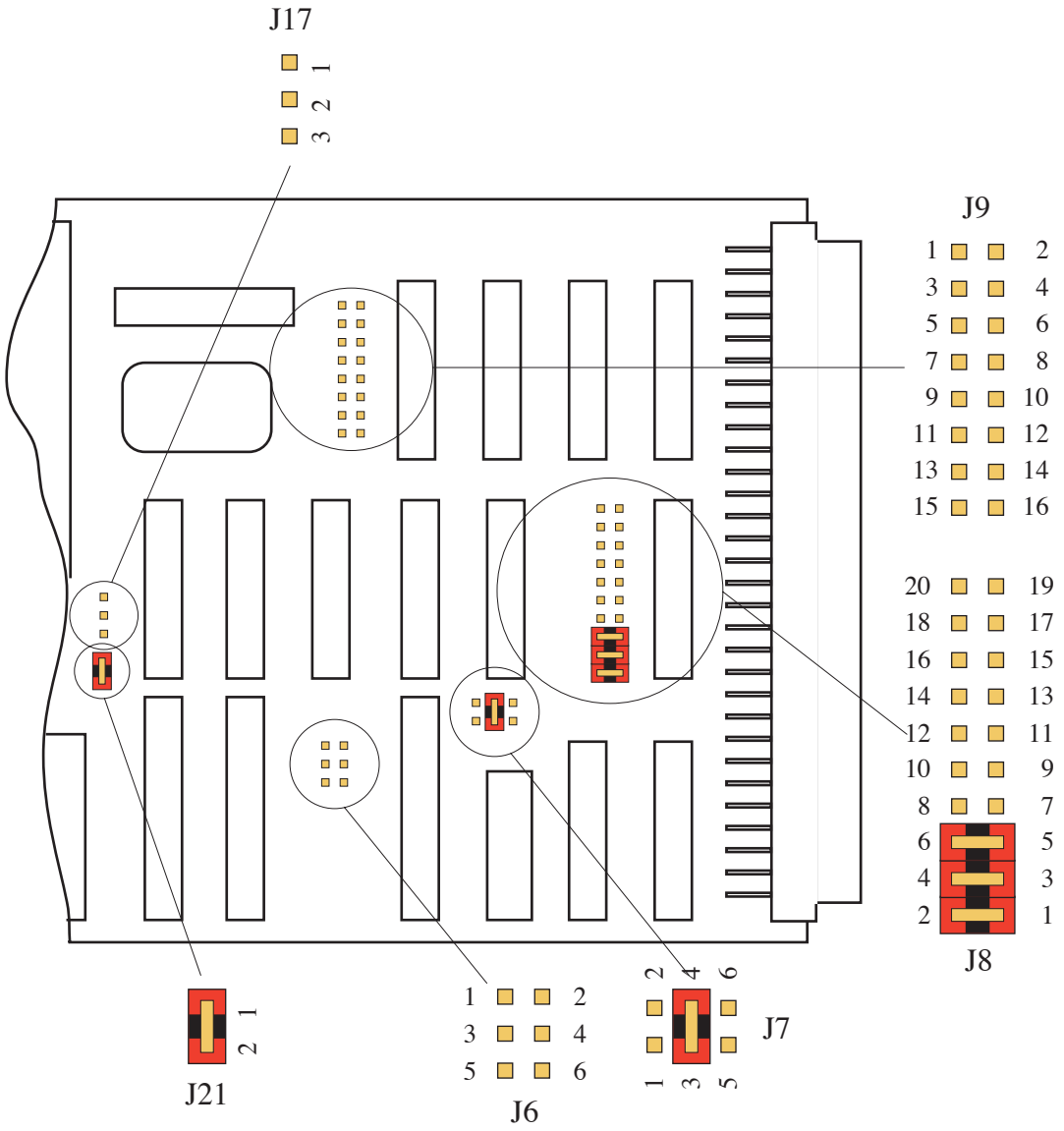
The V1553B possesses some sixteen jumper selectable options that allow address configuration, channel selection and modes of operation.

The V1553B is factory tested for full functionality, and is delivered in the configuration which best suits the majority of users (default settings), see table 3.1 on the next page. You are strongly recommended to check these delivered settings against the function set you desire thus ensuring that the V1553B and your system will function correctly.

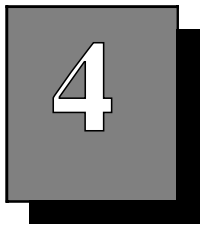
Figure 3.1 Jumper Locations Overview



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4. INSTALLING THE V1553B CPU MODULE

This chapter gives a detailed description of the installation procedure for fitting the V1553B module into a VMEbus system and also provides some general tips on system usage and trouble shooting guidelines.

4.1 Preparation of the V1553B (VMEbus functions)

The task of preparing the V1553B for installation into a VMEbus system must be undertaken (as described in chapter 3 [setting jumpers]) before the module is installed into the rack.

4.1.1 Preparation of the VMEbus and/or the VME/IIOCbus

The VMEbus system into which the V1553B is to be fitted, must be turned off prior to fitting (or removing) any module. If this VMEbus is connected through a VIOC to an IIOC system, then this system and it's peripherals must also be powered down. Further, it is recommended to power-down all other 1553 devices to which the V1553B is to be connected.

The V1553B's channel interfaces are fully isolated, (in transformer coupled mode) from the rest of the V1553B's and VMEbus's circuits, however it is still recommended that these connectors be unpowered (all 1553 devices turned off) at physical time of connection.

Further, the 1553 busses should only be mated to their respective connectors once the V1553B board has been installed into the VMEbus rack.

Note

The outer case of the twin-axial connector (similar to a BNC plug, but with two internal pins) must remain isolated from the front panel of the V1553B module. Therefore, please do not remove the isolation washers fitted to the V1553B's socket or add clips or covers/caps, etc. which may be connected together and thereby cause risk of ground loops and increased/unwanted noise.

If necessary, the existing modules should be moved to suit new layout needs recognizing that the V1553B may be fitted into any desired VMEbus slot except the one which is reserved for the system controller (VMEbus CPU).

4.2 Chronological Installation Procedure

1/. Inspect the 96 way VMEbus Interface connector for clean straight pins.

2/. Check the desired jumper settings.

3/. Ensure all power is off, including that to the other devices connected to the 1553 bus.

4/. Choose the desired slot for the V1553B and if necessary, reposition the other modules.

5/. Place the PCB into the card guides for the desired slot.

6/. Push the module into position carefully. Once the insertion force of the 96 way VMEbus connector has been overcome, the front panel securing screws can be tightened.

7/. Now connect the MIL-STD-1553 interfaces to the front panel connector. Noting that Port B is the upper most on the front panel.

8/. Restore power only when all the modules are correctly fitted and all external connections have been correctly made.

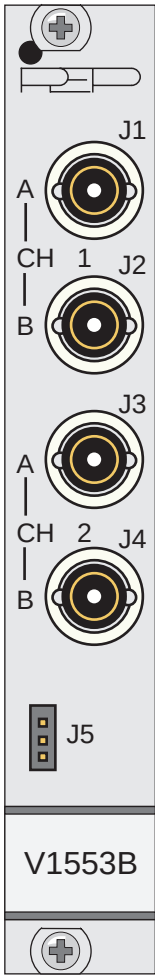
Removing the V1553B (or any other VME boards) is virtually the reverse procedure, where it is especially important to remember when removing any module with on-board connectors, e.g. VSBC-4, VM42, VSCSI, etc. to only pull the module out enough to be able to disconnect these connectors, otherwise damage to the system leads and even the modules connectors may result.

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4.3 Front Panel Functions

The front-panel itself has no status LEDs or other interfaces other than those shown in figure 4.3. The jumper description for J5 may be found in the previous chapter.

Figure 4.3 V1553B Standard Front-Panel Layout



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