Kontron Solutions GmbH
Gutenbergstr. 15 * D-76437 Rastatt
Postfach 2144 * D-76411 Rastatt

☎ +49.7222.1008-0
FAX +49.7222.1008-10

VisionCompact IIa

VC3-CPU	**No. 000212**
VC2-I/O	**No. 000193**
VC3-PWR	**No. 000214**
VC1-BS	**No. 000185**

User's Manual

PC-Based Compact Control

Preface

The purpose of this manual is to support the user during the installation, application, and modification of the hardware and software described in the following chapters. The processes are explained from various technical aspects to simplify the individual steps.

In case of problems, it is helpful to try to identify the error in a reproducible way, and to compare the settings of all DIP switches, jumpers, and connector pin assignments, as well as parameter settings (software), etc., with the specifications in this manual, **before** you call us.
The product you purchased is versatile and complex, and even a small oversight can effect overall performance.

Although the information in this document has been carefully reviewed, Kontron Solutions does not warrant it to be free of errors or omissions. We apologize for any mistakes and would greatly appreciate your comments and suggestions.

Kontron Solutions reserves the right to make any changes to the hardware or software to improve functionality or simplify operation. These changes will not be documented in all instances.

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This manual was written and printed by

Kontron Solutions GmbH
Gutenbergstr. 15 * D-76437 Rastatt, Germany
Postfach 2144 * D-76411 Rastatt, Germany
☎ +49.7222.1008-0
Fax +49.7222.1008-10
E-mail: info@rotec.com
http://www.rotec.de

Corina Wessbecher

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Revisions

Revisions to the User's Manual are briefly listed here by index:

Index	Revision	Chapter	Date	Author	Reason
01	Creation		02/16/00	C.W.	
02	Default of register changed in 0000h;	5.3.3	03/12/02	C.W.	Higher flexibility in ressource sharing, if CAN IRQs are disabled by default;

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Conventions and Symbols

Unless otherwise defined, bit groups are specified in binary format and identified by a subsequent „b.“ Example: 101b

Unless otherwise defined, addresses and register contents are specified in hexadecimal format and identified by a subsequent „h;“ alphanumeric hexadecimal numerals are written in capital letters. Example: EF002h

B is the abbreviation for byte; b, for bit.

k denotes the factor 400h (1024 decimal).

M denotes the factor 100 000h (1 048 576 decimal).

 Stop! Important information. Failure to follow instructions could result in malfunction or destruction.

 Important information. Follow instructions in order to ensure proper operation.

 General additional information.

1. Introduction

The following „Introduction“ provides an outline of the performance of the **VisionCompact® IIa** compact control and its specifications.

Chapter 2, „Functional Description“, describes the tasks and functions of the various **VisionCompact® IIa** components. This chapter provides a better understanding of the interrelated functions of the **VisionCompact® IIa** compact control prior to initial operation.

Chapter 3, „Safety Instructions“ with regard to operation and maintenance, describes potential error sources. It is therefore essential that you read this chapter.

Chapter 4, „Installation“, contains the entire information essential for initial installation and subsequent configuration. A brief, clear overview provides setting options for configuring the modules for operation. Depending upon the module, steps that may be necessary for installing the driver are listed as well.
This chapter contains important instructions for the **VisionCompact® IIa** configuration and initial installation. It is therefore essential that you read this chapter prior to operating the **VisionCompact® IIa** !

Chapter 5, „Programming Model“, describes the **VisionCompact® IIa** memory areas and registers and follows the PC architecture by examining the I/O area separately from the memory areas.
This chapter is an essential reference for the software developer.

Chapter 6 provides several examples of commonly used kernel routines for initialization, data transfers and interrupt handling.

Chapter 7, „Diagnostics“, describes the troubleshooting methods, as well as tools and possible solutions.

Chapter 8 contains codes for new and repeat orders. Use this information to check the correct delivery of your **VisionCompact® IIa**.

The appendix provides a comprehensive reference. ***Recommended Literature*** provides recommended readings for reinforcing basic and special information. Finally, a pre-formatted ***Error Report*** enables the fast processing of possible errors.

1.1. General Description

VisionCompact® IIa is the cost-effective compact solution for control systems. The modular I/O concept allows for individual customization for your machine with local and remote extendible I/Os.

In the hierarchy of automation, the **VisionCompact® IIa** compact control can be viewed as a link between the control level and the sensor/actor level. In dedicated automation systems, **VisionCompact® IIa** assumes data processing and analysis for I/O groups in the physical process; at the same time, **VisionCompact® IIa** communicates with higher-level control entities via the Local Area Network (LAN). The variable field bus, as well as the network connection, ensures optimal communications between the **VisionCompact® IIa** and other automation components.

The compact control makes visualization easy. The powerful graphics interface allows simultaneous operation of a LCD and a CRT monitor. LCD distances of up to 10 m are made possible by a PanelLink interface. For true color displays (16.7 million colors), the graphics controller supports LCDs with a resolution of up to 1280 x 1024 pixels.
Kontron Solutions also offers the necessary components: industrial TFT LCD terminal, robust industrial keyboard, and industrial pointing devices.

PC compatibility allows the use of standard operating systems and application software. Kontron Solutions offers pre-installed systems with Windows 95, Windows NT, and VxWorks. The **VisionControl®** software package [1] provides a platform for control system tasks that enables easy visualization design, standardized field bus protocols, multitasking, real-time capabilities, and modern programming techniques according to IEC 1131-1.

1.2. Features

Base Station:

- Front connections: CRT, PanelLink (TMDS), floppy (FDD), LPT, COM1/2, keyboard+mouse (K+M), Ethernet Cheapernet / twisted pair (Net), variable field bus connection CAN, Profibus or Interbus-S (field bus), SCSI, one digital input and one digital output each, usable for reset output (DI, DO)
- Lateral: variable field bus port: Standard CAN or direct port for I/O terminals (by Weidmüller)
- Easy installation without tools (35 mm DIN rail)
- Intel® Pentium® II processor with 266/300/333/366/400 MHz
- Pipeline burst SRAM L2 cache, 256kByte or 512kByte (dependent of processor)
- Up to 256 MByte main memory on-board
- 3.3V SDRAM DIMM module
- Intel 440BX AGP chip set: 82443BX host bridge and 82371EB southbridge (PIIX4E)
- Fast access data memory with 256 KB SRAM (power failure proof)
- Real-time clock with calendar and alarm
- integrated IDE interface on PCI bus
  An external hard-disk connection is not planned.
- “General Software” Bios through software update
- Mass storage:
  Hard-disk with more than 3GByte
  Silicon disk with 32Mbyte or more flash memory, each IDE-compatible
- External floppy disk drive with up to 2.88 MB
- Super VGA with PCI interface, resolution 1024 x 768 / 64 K colors / 85 Hz (max. 1280 x 1024 / 256 colors / 60 Hz)
- CRT and PanelLink direct connection, simultaneous modes possible
  LCD through PanelLink transmitter module on-board of the **VisionCompact® IIa**
  Receiver module integrated in panel or as separate adapter
- Two serial ports (COM1/COM2), NS16550-compatible, optionally opto-isolated, transmission standard RS232 (default), alternatively RS422 or RS485
- Parallel port (LPT1), ECP, EPP, high-speed mode
- PS/2 keyboard and mouse
- Universal Serial Bus interface, lateral

- Ethernet with 10Base-2 and 10Base-T network connection, conforming to IEEE802.3
- External Ultra SCSI interface (8 bit) with up to 20 MB/s
- Up to 2 PC/104-*Plus* slots for ISA and PCI bus extension
- PC card slot, conforming to PCMCIA2.1 and JEIDA4.1 (card types I, II)
- ISA bus on 96-pin DIN connector
- Direct connection for Weidmüller WINbloc modules (no cables required)
- Field bus interface(s) for CAN, alternatively Profibus-DP or Interbus-S
- Watchdog timer function for monitoring local software and hardware
- Supply voltage monitoring (24V, 3.3V)
- Temperature measurement (2 measuring points through internal SMBus)
- Fan monitoring (CPU fan constantly, case fan optionally)
- Real-time capability supported through hardware: NMI timer and interrupt mapping
- NMI triggering at voltage drop, temperature overrange (programmable range), fan failure or digital input signal (ext. connector)
- 1 isolated digital output
  programmable through registers in FPGA, also usable as reset output
- 1 isolated digital input
  readable through a register in FPGA, can be mapped to NMI
- Industrial case (EMV!), CE-compliant design
- LED status display, diagnostic port, voltage monitoring, watchdog timer, HDD access (configurable), network activity (configurable), fan failure (configurable)

1.3. Function Blocks

The modular **VisionCompact® IIa** design provides several different extension options. Additional required functions can be added to the base station locally or remotely.

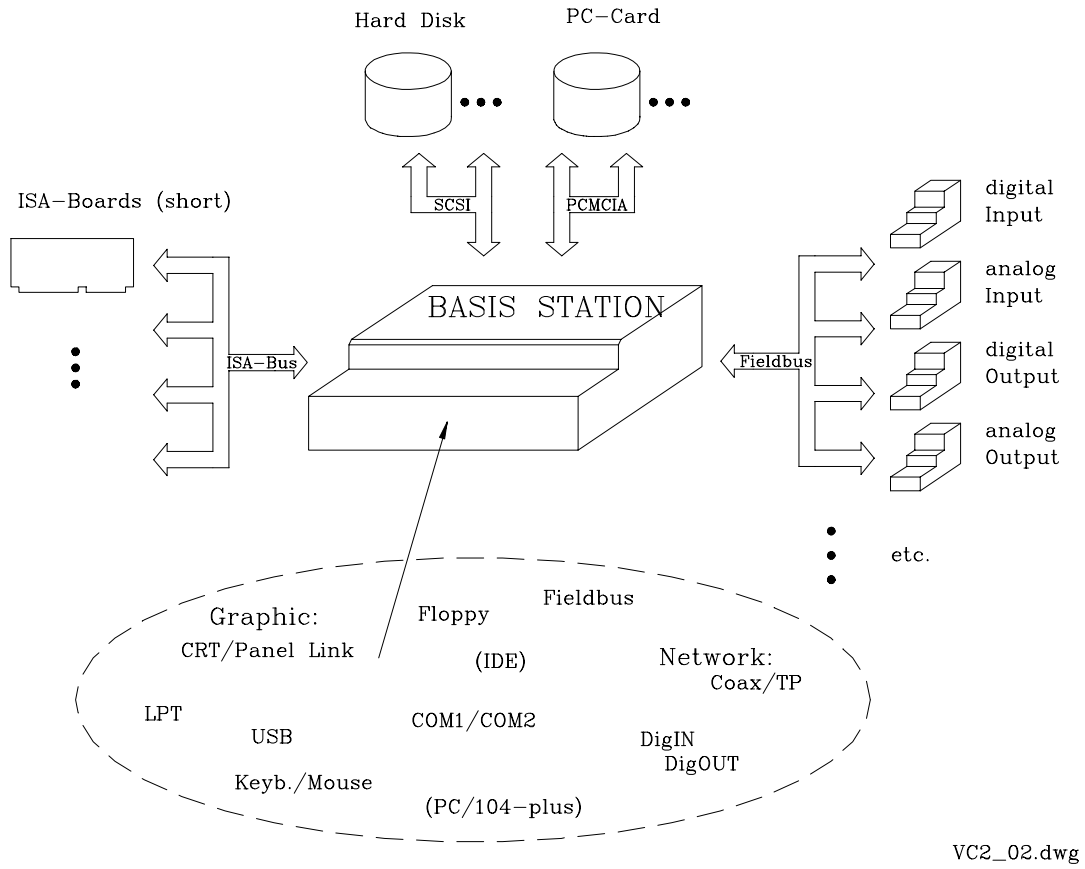


Figure 1: **VisionCompact® IIa** Base Station with Optional Extensions

For a local **VisionCompact® IIa** extension, the base station provides one or two PC/104-*plus* slots, depending upon the case option.

Furthermore, extension modules, mounted analogous to the base system on a DIN rail, can be plugged into the lateral ISA bus interface.

The connection between base station and local CAN bus I/O modules (WINbloc modules) can be made directly via the lateral bus slide.
Some of the functions provided by local I/Os:

- Digital inputs * 8-, 16-, or 32-fold * plus-switching * 24 VDC nominal voltage
- Analog inputs * 4-fold * 12-bit resolution * input ranges ±10V, 0..10V, 0..20mA, 4..20mA
- Digital outputs * 4-, 8-, 16-, or 32-fold * 24 V nominal voltage or relay output * maximum current 0,5 or 2 A * short-circuit-proof
- Analog outputs * 4-fold * 12-bit resolution * output ranges ±10V, 0..10V, 0..20mA, 4..20mA

Remote I/O extensions for the Interbus-S, Profibus-DP, or CAN bus field bus systems can be utilized via the field bus connector located at the front even when physically separated from the base station.

1.4. Technical Data

Field Bus Interface CAN	9-pin D-Sub connector (male)
Controller	SJA1000 (Philips)
Physical interface	ISO DIS 11898, opto-isolated
Transmission rate	max. 1 Mbaud
Field Bus Interface Profibus	9-pin D-Sub connector (female)
Controller	ASPC-2 (Siemens)
Physical interface	DIN 19245, opto-isolated
Transmission rate	max. 12 Mbaud
Field Bus Interface InterBus-S	9-pin D-Sub connector (female)
Controller	MC68332 + ASIC (Phoenix Contact)
Physical interface	DIN E 19258, opto-isolated
Transmission rate	max. 0.5 Mbaud
LAN Ethernet Interface	BNC (RG58) and Western (RJ45)
Controller	CS8900 (Crystal)
Physical interface	IEEE 802.3, twisted pair (10Base-T), coax (10Base-2)
Transmission rate	max. 10 Mbaud
Graphics Output	15-pin HD-D-Sub connector (female) (CRT) 8-pin RJ45 connector (female) (PanelLink)
Controller	CT69000 (C&T)
Physical interface	for CRT monitors (analog) for LCDs (digital: serial via PanelLink)
Resolution	max. 1280 x 1024
Color depth / Image buffer	24 bit, true color / 2MB

Serial Ports COM1/2	9-pin D-Sub connector (male)
Controller	PC97307 (National Semiconductor), NS16550-compatible UARTs
Physical interface	EIA RS232, alternatively EIA RS422 or EIA RS485, optionally opto-isolated
Transmission rate	115.2 Kbaud in 16550 or 16450 mode, 1.5 Mbaud in extended mode
Parallel LPT Port	25-pin D-Sub connector (female)
Controller	PC97307 (National Semiconductor),
Physical interface	IEEE1284-A, ECP and EPP support
Transmission rate	max. 2 MB/s
Ultra SCSI Interface	Centronic connector (female) (8 bit SCSI, 50-pin)
Controller	AIC-7860 (Adaptec)
Physical interface	SCSI-2 interface, A-cable, single-ended, active termination, transmission distance max. 6 m
Transmission rate	Ultra SCSI with up to 20 MB/s
PCMCIA Slot	68-pin contact strip
Controller	PD6722 (Cirrus Logic)
Physical interface	PCMCIA 2.1 and JEIDA 4.1, card types I and II (depending upon case option)
Universal Serial Bus (optional)	4-pin contact strip
Controller	82371EB PIIX4E (Intel)
Physical interface	Series A connector (male), 2 USB connections possible
Transmission rate	12Mbit/s or 1.5 Mbit/s
PS/2 Keyboard and Mouse	6-pin mini DIN connector (female)
Controller	PC97307 (National Semiconductor)
Physical interface	PS/2 Keyboard+Mouse combination connection
Floppy Connection	26-pin mini delta ribbon connector (female)
Controller	PC97307 (National Semiconductor), DP8473- and Intel 82077-compatible
Physical interface	26-pin mini delta ribbon connector (female)
Transmission rate	250 KB/s, 300 KB/s, 500 KB/s, and 1 MB/s

Digital Input DI	2-pin terminal strip
Physical interface	Isolated, reverse-connect protection
Input voltage for signal „0“	0...2.5 V
Input voltage for signal „1“	5...24 V
Digital Output DO	2-pin terminal strip
Physical interface	Isolated
Nominal value	100 mA @ 24 V
Additional Interfaces	
PC/104-*plus* (inside case)	Max. 2 slots 3.3V PCI-bus / 5V ISA-bus
Fast IDE interface on PCI bus (inside case)	82371EB PIIX4E (Intel), PIO and bus master IDE with up to 14MB/s Ultra DMA/33 with up to 33MB/s
ISA bus, 16 bit (extension connector on the left side panel)	82371EB PIIX4E (Intel)
Power Supply	2-pin plug-in type terminal strip
Nominal value	24 VDC
Admissible voltage range	18..36 VDC (21.6..26.4 VDC for directly connected WINbloc modules)
Ripple and noise	5% @ 5V
Power consumption	max. ???A @ 24 VDC (Version VC220-??: keyboard, floppy, and CRT monitor connected)
Ambient Conditions	
Operating (storage) temperature	0..+50° C @ max. 15°/h (-40..+70° C @ max. 30°/h)
Operating (storage) vibration	Versions with silicon disk: 5g (5g) DIN IEC 68, Part 2-6 sine, 12..300 Hz, 1Oct/min., 1h / axis Other versions: 0,5g (5g) sine, 5..500 Hz
Operating (storage) shock (permanent)	Versions with silicon disk: 15g (15g) DIN IEC 68, Part 2-29 Half sine, 11 ms, 1000 per direction and axis

Operating (storage) shock (single)	Versions with silicon disk: 40g (40g) DIN IEC 68, Part 2-27 Half sine, 6 ms, 3 per direction and axis Other versions: 10g (70g) half sine, 11 ms, 2 per minute
Operating (storage) humidity	10..80% (5..90%)non-condensing
Operating (storage) altitude	-300..+3000 m (-400..+15000 m) above sea level
Dimensions / Weight	
Width / Height / Depth	272mm / 160mm / 81mm (standard case) 272mm / 160mm / 96mm (case for 2x PC/104*plus*)
Weight	approx. ? kg (Version VC200-???)
Electromagnetic Compatibility	
Emitted interference	Limits and operation DIN EN 55022-, DIN EN 50081-1-compliant
Interference immunity	Limits and operation DIN EN 50082-2-compliant
Protection & Safety	
Safety	Limits and operation DIN EN 60950-compliant
Protection	IP20 acc. to DIN 40050

Table 1: Technical Data

☞ Depending on the **VisionCompact® IIa** version, some features may not be available. Subject to corrections and technical changes.

2. Functional Description

Despite its small size, the **VisionCompact® IIa** integrates all standard industrial PC functions, including the usual COM1 and COM2 serial ports, a parallel LPT port, and a PS/2 interface for the keyboard and mouse. For service and diagnostic purposes, an external floppy disk drive can be connected directly without additional power supply.
The compact control includes one or two PC/104-*plus* slots (16 bit ISA), depending upon the case option.

The modular design allows for additional extension modules to be installed in the system. Communication of these extensions with the base station is accomplished through the ISA bus interface.

The entire computer system fits into a rugged case (WxHxD = 272x160x81 mm). The industrial aluminum case guarantees CE conformity in accordance with the EMV directives and is ideally suited for harsh control-cabinet environments.

2.1. Base Station

2.1.1. Front

Eight LEDs display the current status of the compact control. One LED (*WDOG*) indicates the watchdog activity. Two LEDs (*Power* and *VCC*) indicate the power supply status. LEDs *P04* and *P03* are user-programmable and indicate the bit pattern stored in diagnostic port bits 4 and 3. The LEDs *P02..P00* have two functions. After a system reset (default), *P00* is used to indicate hard-disk accesses, *P01* to indicate network activity, and *P02* to indicate fan failure. As an alternative to indicating fan failure, HDD and network activity, the pattern stored in the diagnostic port in bit2..bit0 can be output to the LEDs. (For details, see the description of the DIAG register in Chapter 5, „Programming Model“.)

LED *Power*: Indicates drop of external power supply below 18.5 Volt.
LED *VCC*: Indicates drop of one of the internal power supply voltages.

The following connections are accessible from the front:

- Connector for external power supply (24 V) (Power)
- CRT and PanelLink (TMDS)
- Floppy (FDD), LPT, PS/2 keyboard and mouse (K+M), COM1, COM2
- SCSI
- Ethernet Cheapernet, twisted pair (Net)
- Field bus
- Digital input and digital output (DI, DO)



Figure 2: **VisionCompact® IIa** Front Panel

2.1.2. Functional Units

The base station includes the following essential functions:

- Computer core with processor, memory, etc.
- Power supply input for 24 VDC
- Field bus interface for CAN, Profibus-DP or Interbus-S
- CAN interface for WINbloc (optionally standard CAN)
- Serial COM1 and COM2 ports (default RS232)
- Parallel LPT Port
- Graphics output with connectors for CRT and PanelLink
- Ethernet controller with network connection (TP and Cheapernet)
- Status display on 8 LEDs (green)
- PCMCIA slot for card types I and II
- SCSI controller

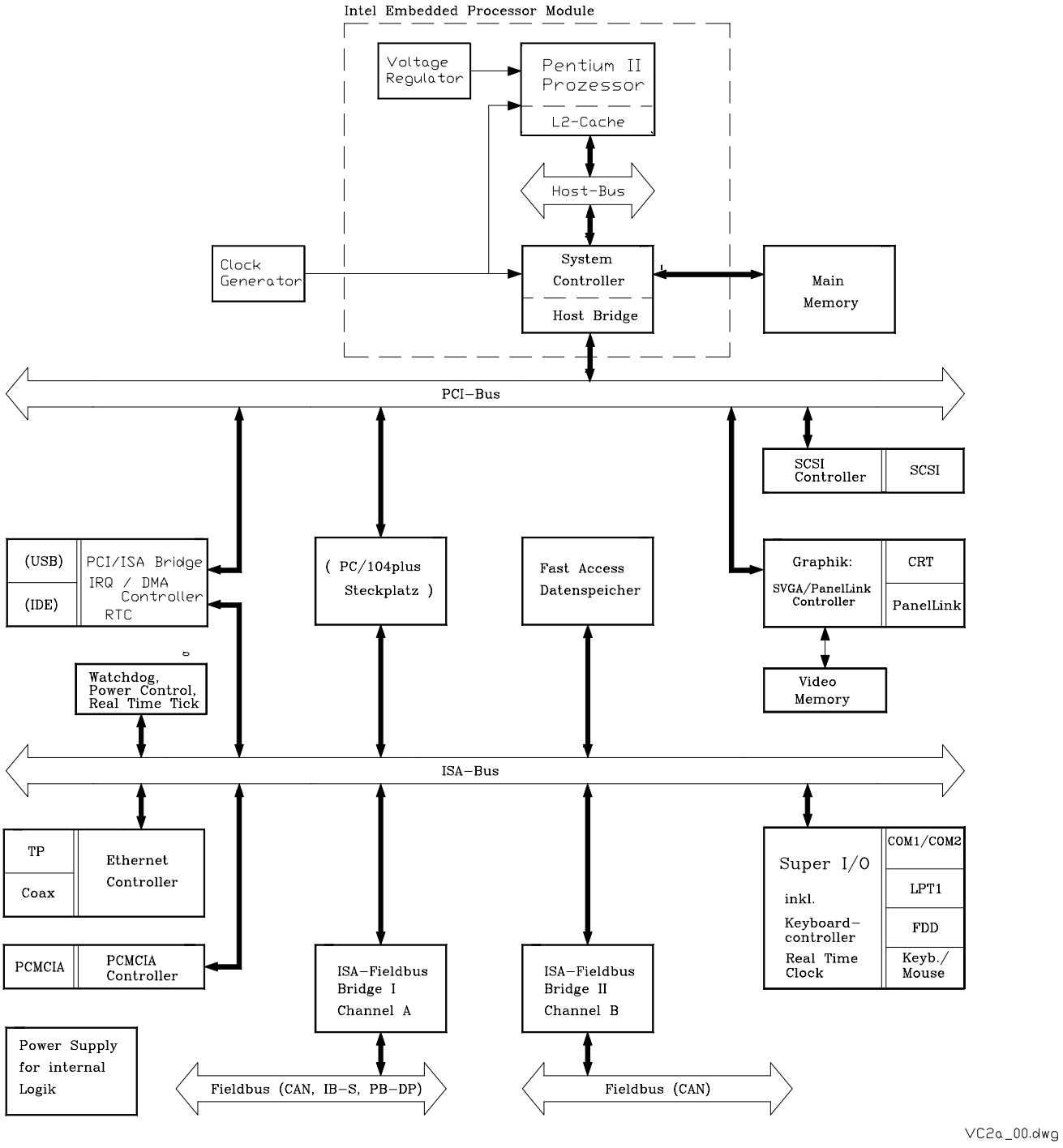


Figure 3: Functional Units of the Base Station

2.1.2.1. Processor and Chip Set

The factory-installed Intel® Pentium® II processors with a clock frequency of at least 266 MHz and MMX™ ensure complete compatibility with MS-DOS X.XX, MS-Windows XX, and OS/2 X.X, as well as other common operating systems. Energy-saving 3.3V technology assures low power loss.

In addition to the L1 cache, the **VisionCompact® IIa** compact control includes a 256kByte or 512 KB L2 cache (dependent of processor).

The 440BX AGP chip set by Intel consisting of

- 82443BX system controller (Northbridge)
- 82371EB PCI/ISA Xcelerator (PIIX4E)

ensures 100% PC compatibility.

The chip set includes the following main functions:

82443BX (Northbridge)
Host-to-PCI bridge
DRAM controller
AGP interface

82371EB (PIIX4E)
PCI-to-ISA bridge
Universal Serial Bus host controller
Integrated IDE controller
DMA controller
Interrupt controller
Real-time clock

Recommended literature:
PC Hardware Basics [5], PC System Programming [6] [7], ISA Bus Basics [1] [2] [3], PC/104 [4].

2.1.2.2. Interrupt Structure

The usual PC-AT hardware interrupts in the **VisionCompact® IIa** are managed by the Intel 82371EB PCI ISA Xcelerator:

Interrupt	Usual PC-AT Architecture Function	VisionCompact IIa
IRQ8	Real-time clock	Same
IRQ9	Redirected to IRQ2	graphic / USB (*)
IRQ10	User-definable	Fieldbus channel A (*)
IRQ11	User-definable	Fieldb. Channel B / SCSI (*)
IRQ14	Hard disk	Same
IRQ15	User-definable	Same
IRQ12	PS/2 mouse	Same
IRQ1	Keyboard	Same
IRQ3	COM2	Same
IRQ4	COM1	Same
IRQ5	LPT2, user-definable	Ethernet (*)
IRQ6	Floppy drive	Same
IRQ7	LPT1	Same

Table 2: Groups of Usual PC-AT Hardware Interrupts

(*) Default! Differences are possible for customer specific solutions.

2.1.2.3. Main Memory, SIMM, EDO

The main memory is a 168-pin **DIMM** module. It is mounted on-board and available in 32, 64, 128 MB and 256MB (registered SDRAM).

There will be used 3.3V unbuffered and registered SDRAM modules (66MHz).

2.1.2.4. Ethernet

The CS8900 Ethernet controller by Crystal can be accessed in I/O or memory mode. The initialization data are stored in a serial EEPROM, making switches and jumpers superfluous. Users can connect the network to a 8-pin RJ45 (10Base-T) or a BNC (10Base2) female connector.

Factory-set default:

ISA interrupt IRQ5

I/O address 300h

2.1.2.5. Graphics

The graphics component with a 32-bit PCI interface consists of the CT69000 graphics controller with an integrated DA converter for connecting a VGA monitor (RAMDAC) and a programmable color look-up table (CLUT) for the display color space adjustment. In addition to the analog CRT interface, the graphics controller includes a LCD interface that is software-configurable and supports virtually all major LCD data formats for color models up to 24 bits. The graphics controller is a 100% VGA-compatible, high-performance CT69000 chip set by Chips & Technologies, which is also found in premium notebooks. It supports popular SVGA modes, such as 800 x 600 and 1024 x 768 pixels, with ergonomic refresh rates of up to 85 Hz. The built-in hardware accelerator enables particularly fast frame rates in Windows applications. A hardware cursor further simplifies image management.

The **VisionCompact® IIa** VGA controller can control popular VGA monitors (Multiscan), as well as LCD, EL, or plasma flat-panel displays. The image can be simultaneously displayed on an analog monitor (CRT) and a flat-panel display (e.g. LCD).

VGA monitors allow for „true color“ display with 16.7 million colors. On color LCDs, the maximum display is 256 K colors on passive and 16.7 million colors on active (TFT) panels. Monochrome LCDs allow 64 gray levels that can be virtually increased through dithering and frame rate control.

The graphic supports power management for the CRT connection according to the VESA-DPMS standard.

Flat-panel displays are connected to the **VisionCompact® IIa** through the PanelLink interface in the form of an 8-pin RJ45 female connector.

The PanelLink interface reliably transmits LCD signals over longer distances (up to 10m). This is realized using a CT65100 (or SIL100) High Speed Serial Transmitter and a CT65101 (or SIL101) Receiver.

2.1.2.6. Fieldbus

VisionCompact® IIa includes two field bus interfaces:

a) CAN Bus Slide, Direct Connection for I/O Terminals

CAN WINbloc modules by Weidmüller can be inserted directly into the interface on the right side panel of the compact control, without additional installation steps. The number of connectable I/O modules is limited to ten. The bus slide supplies the operating voltage of 24 VDC (see also WINbloc data sheets) for the modules.

If the CAN WINbloc modules are operated on the **VisionCompact® IIa** side panel, the system power supply must be between 21.6 VDC and 26.4 VDC. Exceeding this voltage range can damage the WINbloc modules.

Optionally, the above interface is available as standard CAN with 9-pin D-Sub male connector.

b) Front Field Bus Connection, 9-pin D-Sub

The front connection can be a CAN, Profibus, or Interbus-S interface (specified in the order information).

CAN Bus:

The on-board CAN interface is a SJA1000 controller by Philips. The physical interface is opto-isolated in accordance with ISO DIS 11898.

Profibus-DP:

The Profibus interface is using a PC/104 slot (upgradable). The Siemens ASPC-2 controller is mounted on the PC/104 board. The interface is opto-isolated in accordance with DIN 19245.

Interbus-S:

The Interbus-S interface is located on a PC/104 board (upgradable) (MC68332 + ASIC by Phoenix Contact). The interface is opto-isolated and designed in accordance with DIN E 19258.

2.1.2.7. Mass Storage

IDE-compatible 2.5„ hard disks with a capacity of more than 2 GB or 3 GB are used for mass storage. Alternatively, IDE-compatible silicon disks of 32MB or more can be used in harsh environments. If a silicon disk is used for mass storage, the maximum number of write cycles is currently restricted to 300,000 per memory cell, due to flash technology. For that reason, particular caution is indicated with respect to programs which swap out temporary files to the „hard disk“.

2.1.2.8. Fast Access Memory

The **VisionCompact® IIa** is equipped with fast access data memory (SRAM) and permits real-time storage of data being scanned at high speed. The 256 KB SRAM memory is battery-backed to prevent a loss of stored machine parameters after a power outage.

The fast access data memory of the **VisionCompact® IIa** can be accessed in two ways:

- **I/O Access:**

  Access is handled via special IN/OUT CPU instructions. The PC address space is limited to 64 KB I/O ports, and only 16 address lines are activated.

  However, the SRAM covers a larger area (256 KB) and requires more than „only“ 16 address lines, necessitating an expansion of missing addresses. Four address lines (SAQ17..SAQ14) were expanded for the **VisionCompact® IIa**. These can be used to select 2^4 = 16 windows. For each window, an I/O area of 16 KB can be addressed (C000h...FFFFh).

  (For details, see the description of the ADR register in Chapter 5, „Programming Model“.)

- **MEM Access**

  In PC architecture, general memory cycles (MEM access) must be differentiated with respect to REAL mode and PROTECTED mode addressing.

  REAL Mode:

  In REAL mode, an address space of only 1MB can be addressed, and only 20 address lines are activated. The space reserved for expansions in the 1 MB address space is limited.

  Similar to I/O mode, addressing is also accomplished through 16 windows of 16 KB each. (The windows are addressed through the ADR register as well.) In REAL mode, the address space for mapping the window could be D0000h-D3FFFh.

PROTECTED Mode:

Theoretically, PROTECTED-mode addressing provides all 32 bits. However, since the ISA bus contains only 24 address bits, the 16 MB of the ISA bus address space is mirrored 256 times (where the low memory area has allocated max. 128 MB of the memory and, hence, is not available for the ISA bus). The address mapping is 1:1, i.e., the SRAM is addressed directly by ISA bus addresses without using an intermediate address register.

2.1.2.8. Real Time Tick, NMI

The compact control includes an NMI timer for cyclical and deterministic hardware interrupts of the operating system. Time slices from 0.1 ms to 100 ms can be programmed.

In addition, the following events can be redirected to the NMI (non-maskable interrupt):

- Any ISA interrupt
- Real time tick (see above)
- Power failure (voltage drop)
- Temperature overrange (at 1 of 2 measuring points)
- Fan failure (1 CPU fan, 2 case fans)
- Digital input signal (at terminal strip „DI“)

2.1.2.9. Watchdog

The watchdog increases system security by monitoring programs and detecting software errors, e.g. endless loops, that jeopardize the system’s real-time capability. If the watchdog does not trigger within the hardware-configured time-out period, the watchdog „attacks“ and triggers a reset.

Watchdog trigger time:

- Normal operation: t = 400 ms
- Immediately after reset: t = 1.6 s

In case of an error, the potential-free watchdog resets the external field bus I/O modules and protects the system against damage.

The MAX691 watchdog ensures reliable processor operation, due to the integrated voltage-monitor function and dead man's circuit (watchdog). The WDOG LED in the case cover indicates whether the watchdog function is enabled. The watchdog is software-enabled (see „Programming Model").

If the internal power supply drops below 3.3V –5%, the voltage monitor triggers a PC reset.

2.1.2.10. System Management Bus

To ensure safe operation of the **VisionCompact® IIa**, the system is equipped with a temperature sensor and a hardware monitor (incl. temperature sensor). Both components are controlled through the SMB host of the Southbridge .

The hardware monitor (LM80) and the temperature sensor (on the processor module) are used for checking the temperature. In addition the LM80 is able to check the speed of all fans.

The sensors are placed in the warmest areas of the device (under the processor, at the power supply).

In addition to the temperature sensor and the LM80, the SMB host can address another device: a digital potentiometer. The digital potentiometer (X9221) can be set in steps of 31.25 Ω. The PanelLink interface can be adjusted by varying the resistance.

Factory-set SMB addresses of the devices are listed below:

Device	SMB Address
Thermal sensor (on processor module)	Pentium II: 1001 1100 = 9Ch (Write) 1001 1101 = 9Dh (Read) Pentium III: 0111 1100 = 7Ch (Write) 0111 1101 = 7Dh (Read)
LM80	0101 0010b = 52h (Write) 0101 0011b = 53h (Read)
X9221	0101 0100b = 54h

Table 3: SMB Addresses of Devices

2.1.2.11. Universal Serial Bus

The Universal Serial Bus is attached to a Series A connector, that is available on the left side of the case. The 82371EB PCI-to-ISA Xcelerator (PIIX4E) supports up to 2 USB connections.

2.1.2.12. Ultra SCSI Interface

The SCSI interface enables, for example, the connection of a CD-ROM drive to the **VisionCompact® IIa**.

The BIOS for the SCSI controller is available at Kontron Solutions GmbH.

2.1.2.13. PCMCIA Interface

The **VisionCompact® IIa** supports the following PCMCIA card types:

Type I: Height of plug-in card: 3.3 mm

Type II: Height of plug-in card: 5 mm

The PD6722 component by Cirrus Logic® is the host adapter and enables communications between PCMCIA cards and the ISA bus. Hard disks, modems or memory cards can be inserted as PCMCIA plug-in cards. The PCMCIA slot is located on the bottom side panel.

2.1.2.14. Digital Inputs and Outputs

VisionCompact® IIa is equipped with 8 digital inputs and 8 digital outputs.

The status of inputs DI7..DI0 can be read in bits 7..0 of the DIGIO register (address 7F00h). The outputs can be read or written in bits 15..8 of the register (DO7..DO0).

One digital input and output each are opto-isolated connections on the front (DI and DO). The remaining seven inputs and outputs are located internally on a contact strip (not opto-isolated). Optionally, the inputs and outputs can be placed on the left side of the case. (Isolation of inputs and outputs upon request!)

On the one hand, the front output DO is addressed by the WDOG reset and, on the other hand, by bit 0 of the DIGIO register. (Disable, if reset or bit 0 is set to LOW.).

3. Safety

3.1. Handling

This module contains mechanically and electrically sensitive, high-quality electronics and should be carefully unpacked.
Thoroughly inspect the module for damage that might have occurred during shipment. In case of transport damage, do not install the module or apply power. Contact our technical support.

Electrostatic discharge can destroy integrated function blocks.
Avoid direct contact with integrated function blocks and unprotected contacts when opening the case. To avoid damages, installations should only be made by trained personnel at a designated, static-free workplace.

Prior to installation or disassembly, disconnect all power to the device and any connected components. Components must also be de-energized before connecting them to built-in interfaces.

Verify all connections before starting the system. Check for inadvertently switched cables.

Verify correct polarity when connecting power.



Failure to comply with these safety precautions can destroy the module!

3.2. Circuitry

The **VisionCompact® IIa** is equipped with several independent safety features:

- **Voltage Monitoring**

  The Power LED goes out when the external power supply drops below 18.5 V.

  The VCC LED goes out when a logic determines a drop of one of the internal voltage supplies (5V, 3.3V and 2.5V). As an option, a non-maskable interrupt (NMI) on the ISA bus can be triggered when this drop occurs. When the voltage supply drops below 3.135V (3.3V –5%) the **VisionCompact® IIa** is reset.

- **Program Run Time Monitoring**

  A watchdog timer monitors the CPU program run time. The watchdog must be software-enabled after booting.

  The WDOG LED lights up, if the watchdog has been software-enabled.

- **Temperature Monitoring**

  Two temperature sensors that are addressed by the SMBus are used for monitoring the temperature. Each temperature sensor monitors its ambient temperature and activates its control output (software-enabled), if the temperature exceeds the permissible maximum value. The permissible maximum value is stored in a sensor register.

  The control outputs of both temperature sensors can be redirected to an NMI (non-maskable interrupt).

- **Fan Monitoring**

  The CPU fan and both case fans can be monitored by the LM80 hardware monitor which is also attached to the SMBus. The CPU fan is monitored constantly, while both case fans are monitored alternatingly [1] (Note: cyclical switching between both case fans through software).

  If the CPU or case fans fall below the permissible minimum speed, the hardware monitor (if it is software-initialized) activates its fan control output.

  The fan control output can be redirected to an NMI (non-maskable interrupt).

[1] Switching between both casing fans occurs through GPIO10 of the Super I/O *PC97307*. Depending upon the level applied to GPIO10, fan 0 or 1 is switched to the LM80. (Software-) switching is described in „Super I/O: GPIO Port Control."

Safety advantages for you:

- **Potentially weak points of the system (e.g., overloaded or incorrect power supply) are recognized immediately through visual inspection.**

- **The watchdog trigger circuit stops (dangerous) processes triggered by software errors.**

- **An unintentionally disabled watchdog is detected through visual inspection.**

- **Destruction of modules due to excessive generation of heat (e.g., fan standstill) is prevented.**

4. Installation

4.1. Preparation and Requirements

Minimum requirements for initial start-up and software installation/operation:

- Power supply with 24 VDC
- MultiSync monitor or LCD panel
- Keyboard
- Adapter cable (Part No. RTC-K092) for keyboard/mouse connection
- External floppy disk drive (Part No. EXFD, 3.5", 1.44MB), if no operating system is pre-installed
- External parallel port CD-ROM drive (Part No. CDR.LPT_01 or CDR.LPT_02), if software is to be installed from CD-ROMs
- 230 V AC (required for CD-ROM drive only)

VisionCompact® IIa can be mounted without any tools onto a 35mm TS DIN rail.

For the safe operation of the **VisionCompact® IIa**:

* the DIN rail must be grounded, and
* the maximum permissible ambient temperature must not be exceeded.

4.2. Mounting

VisionCompact® IIa is simply snapped onto a DIN rail (35mm).

4.2.1. PC/104 - Modules



The modules must conform to the PC/104 standard.

The following dimensions should not be exceeded:

* max. permissible component height on the component side: 0.435“ (11.05 mm)
* maximum permissible component height on the solder side: 0.1” (2.54 mm)

Failure to comply with the PC/104 standard can result in mounting problems.

The steps for mounting one/two PC/104 module(s) are as follows:
First, open the case. To remove the bottom of case, open the countersunk screws on the side panels and remove the bottom of the case from the cover. When removing the bottom of the case, all connectors connecting the bottom with the „remaining unit“ must be removed (hard-disk cable, bus slide connection, and fan voltage supply).
Finally, the PC/104 module(s) can be mounted.

For system extensions via the PC/104 slot, two technical scenarios must be distinguished:

- Case option A: Mounting one PC/104 module
- Case option B: Mounting one or two PC/104 modules.

4.2.1.1. Case Option A

The PC/104 module is mounted by simply plugging the module into the back of the computer system. The PC/104 board snaps into place in the factory-provided spacers with locking device. Two openings for 25-pin D-Sub connectors for potential connections are provided on the left side panel.

4.2.1.2. Case Option B

When using two PC/104 modules, the PC/104 modules are mounted using 13 mm and 15 mm long spacers. The spacers are provided with a threaded stem on one side and a female thread on the other.

The mounting elements are factory-assembled in the correct order. In order to mount one or two PC/104 modules, the mounting elements must be correctly disassembled (see Figure „Case Option B: PC/104 Module Mounting“).



Figure 4: Case Option B: PC/104 Module Mounting

4.2.2. WINbloc Module

WINbloc modules are either connected through the front 9-pin D-Sub connector (labeled „Fieldbus“) or through the bus slide connection on the right-hand side panel.

Please note the following when connecting WINbloc modules to the bus slide:

To ensure the correct module mounting, the bus slide (BS) must be removed from the WINbloc module and inserted into the **VisionCompact® IIa** . The WINbloc module is then inserted into the bus slide.

4.3. Terminal Assignments

The **VisionCompact® IIa** is equipped with the following connections on the front panel...

- Power : 24 VDC power supply
- CRT : CRT monitors
- TMDS : LCD interface (serial PanelLink data transmission)
- FDD : Connection for external floppy disk drive
- LPT : Parallel port for external CD-ROM or other drive
- K+M : Combination connection for PS/2 keyboard and mouse
- COM1 : Serial port 1
- COM2 : Serial port 2
- Fieldbus : Field bus connection for CAN, Interbus-S or Profibus
- SCSI : SCSI interface
- Net : Ethernet connection for twisted pair
- Net : Ethernet connection for coaxial cable
- DI : Digital input
- DO : Digital output (optionally reset output)

4.3.1. Field Bus Interfaces

As mentioned earlier, **VisionCompact® IIa** is equipped with two field bus interfaces, one on the front and the other on the right-hand side panel.

4.3.1.1. Front Field Bus Interface

Name: : Fieldbus

Location : Front panel

Physical implementation : 9-pin D-Sub connector (male)
Usage of one gender for Interbus-S and Profibus-DP

Field Bus Interface			
Pin	CAN	Interbus-S	Profibus-DP
1	n.c.	DO	SHLD
2	CAN Low	DI	Auxiliary power
3	GND	GND	RxD/TxD-P
4	n.c.	n.c.	RCtrl-P
5	n.c.	VCC	GND
6	GND	/DO	VCC
7	CAN High	/DI	Auxiliary power
8	n.c.	n.c.	RxD/TxD-N
9	n.c.	RBSTI	RCtrl-N

Table 4: Signal Assignments for ‘Fieldbus’ Interface (Front)

4.3.1.2. Lateral Field Bus Interface

Name: : -

Location : right-hand side panel

Physical implementation : 10-pin direct plug-in connection via PC board

Field Bus Interface	
Pin	CAN
1	SHLD
2	M0V
3	M0V
4	Tx1
5	Rx0
6	Rx1
7	Tx0
8	M24V
9	M24V
10	SHLD

Table 5: Signal Assignments for Field Bus Interface on Right-Hand Side Panel

Upon request, the above field bus interface, in the form of a standard CAN can be connected using a 9-pin D-Sub connector (male). In this case, the pin assignments in Table 4 under 'CAN' are used.

4.3.2. Serial Ports (RS232)

Name: : COM1 or COM2

Location : Front panel

Physical implementation : 9-pin D-Sub connector (male)

COM1 / COM2			
Pin	RS232	RS422	RS485
1	DCD	TxD-	TxD-
2	RxD	TxD+	TxD+
3	TxD	RxD+	RxD+
4	DTR	RxD-	RxD-
5	GND	GND	GND
6	DSR	RTS-	n.c.
7	RTS	RTS+	n.c.
8	CTS	CTS+	n.c.
9	RI	CTS-	n.c.

Table 6: Signal Assignments for Serial Ports 'COM1', 'COM2'

The connections

TxD+ and RxD+

TxD- and RxD-

required for transmission standard RS485 have been integrated on-board.

4.3.3. Parallel Port

Name: : LPT

Location : Front panel

Physical implementation : 25-pin D-Sub connector (female)

Parallel Port		
Pin	Mnemonic	Signal Description
1	/STB	Strobe
2	D0	Data Bit 0
3	D1	Data Bit 1
4	D2	Data Bit 2
5	D3	Data Bit 3
6	D4	Data Bit 4
7	D5	Data Bit 5
8	D6	Data Bit 6
9	D7	Data Bit 7
10	/ACK	Acknowledge
11	BUSY	Busy
12	PE	Paper End
13	SLCT	Select
14	/ALFD	Auto Feed
15	/ERROR	Error / Fault
16	/INIT	Printer Init
17	/SLCT IN	Printer Select
18-25	GND	Ground

Table 7: Signal Assignments for Parallel ‘LPT’ Port

4.3.4. SCSI Interface

Name: : SCSI

Location : Front panel

Physical implementation : 50-pin SCSI-2 high-density connector (female)

Ultra SCSI Interface		
Pin	Signal	Mnemonic
13	n.c.	Not connected
26	#DB0	Data Bit 0
27	#DB1	Data Bit 1
28	#DB2	Data Bit 2
29	#DB3	Data Bit 3
30	#DB4	Data Bit 4
31	#DB5	Data Bit 5
32	#DB6	Data Bit 6
33	#DB7	Data Bit 7
34	#DBP	Parity Bit
38	TRMPWR	Terminator Power
41	#ATN	Attention
43	#BSY	Busy
44	#ACK	Acknowledge
45	#RST	Reset
46	#MSG	Message
47	#SEL	Select
48	#C/D	Command / Data
49	#REQ	Request
50	#I/O	Input / Output
12, 14, 37, 39	Res.	Reserved
1..11, 15..25, 35, 36, 40, 42	GND	Ground

Table 8: Terminal Assignments for Ultra SCSI Interface

4.3.5. PCMCIA Slot

Name: : -

Location : bottom side panel

Physical implementation : 68-pin contact strip

PCMCIA Interface			
Pin	Signal	Mnemonic	I/O
2	D3	Data Bit 3	I/O
3	D4	Data Bit 4	I/O
4	D5	Data Bit 5	I/O
5	D6	Data Bit 6	I/O
6	D7	Data Bit 7	I/O
7	#CE1	Card Enable 1	I
8	A10	Address Bit 10	I
9	#OE	Output Enable	I
10	A11	Address Bit 11	I
11	A9	Address Bit 9	I
12	A8	Address Bit 8	I
13	A13	Address Bit 13	I
14	A14	Address Bit 14	I
15	#WE/PGM	Write Enable	I
16	RDY/BSY	Ready / Busy (EEPROM)	O
18	VPP1	Progr. Voltage 1 (EPROM)	
19	A16	Address Bit 16	I
20	A15	Address Bit 15	I
21	A12	Address Bit 12	I
22	A7	Address Bit 7	I
23	A6	Address Bit 6	I
24	A5	Address Bit 5	I
25	A4	Address Bit 4	I
26	A3	Address Bit 3	I
27	A2	Address Bit 2	I
28	A1	Address Bit 1	I
29	A0	Address Bit 0	I

30	D0	Data Bit 0	I/Ow
31	D1	Data Bit 1	I/O
32	D2	Data Bit 2	I/O
33	WP	Write Protect	O
36	#CD1	Card Detect 1	O
37	D11	Data Bit 11	I/O
38	D12	Data Bit 12	I/O
39	D13	Data Bit 13	I/O
40	D14	Data Bit 14	I/O
41	D15	Data Bit 15	I/O
42	#CE2	Card Enable 2	I
43	RFSH	Refresh (DRAM)	I
46	A17	Address Bit 17	I
47	A18	Address Bit 18	I
48	A19	Address Bit 19	I
49	A20	Address Bit 20	I
50	A21	Address Bit 21	I
52	VPP2	Progr. Voltage 2 (EPROM)	
53	A22	Address Bit 22	I
54	A23	Address Bit 23	I
55	A24	Address Bit 24	I
56	A25	Address Bit 25	I
61	#REG	Register Select	I
62	BVD2	Battery Voltage Detect 2	O
63	BVD1	Battery Voltage Detect 1	O
64	D8	Data Bit 8	I/O
65	D9	Data Bit 9	I/O
66	D10	Data Bit 10	I/O
67	#CD2	Card Detect 2	O
44, 45, 57..60	RFU	Reserved	
1, 34, 35, 68	GND	Ground	
17, 51	VCC	5 V	

Table 9: Terminal Assignments for PCMCIA Slot

4.3.6. Universal Serial Bus

Name: : USB

Location : left side panel

Physical implementation : 4-pin contact strip

Universal Serial Bus		
Pin	Mnemonic	Signal Description
1	VBus	+ 5 V Cable Power
2	D -	Data -
3	D +	Data +
4	GND	Cable Ground

Table 10: Terminal Assignments for Universal Serial Bus

4.3.7. PS/2 Keyboard and Mouse Connection

Name: : K+M

Location : Front panel

Physical implementation : 6-pin mini DIN connector (female)

Keyboard & Mouse		
Pin	Mnemonic	Signal Description
1	KBData	Keyboard Data
2	MData	Mouse Data
3	GND	Ground
4	VCC	+5 Volt
5	KBClk	Keyboard Clock
6	MClk	Mouse Clock

Table 11: Signal Assignments for 'K+M' Keyboard & Mouse Interface



Connecting

- a PS/2 mouse
- or a PS/2 keyboard and a PS/2 mouse (parallel operation)

requires an adapter (Part No. RTC-K-092).

A PS/2 keyboard can be connected directly.

An AT keyboard requires an off-the-shelf PS/2 adapter.

4.3.8. Floppy Connection

Name: : FDD

Location : Front panel

Physical implementation : 26-pin mini delta ribbon connector (female)

Floppy		
Pin	Mnemonic	Signal Description
1,10,13,20	GND	Ground
2	VCC	+5 V
3-5,16,18,19	n.c.	
6	#DRV0	Drive Select
7	#MTR0	Motor on
8	FDDIR	Direction Select
9	#WDATA	Write Data
11	FDD11	Multifunction[1)]
12	#RDATA	Read Data
14	FDD14	Multifunction[1)]
15	FDD15	Multifunction[1)]
17	#INDEX	Index
21	#STEP	Step
22	#WGATE	Write Gate
23	#TRK0	Track 0
24	#WRTPRT	Write Protect
25	HDSEL	Side One Select
26	FDD26	Multifunction[1)]

Table 12: Signal Assignments for 'FDD' Floppy Interface

The PC must be turned off, before the floppy disk drive is connected. Failure to comply with the instructions can permanently damage the unit.

[1)] Pin assignment dependent upon floppy drive type

4.3.9. Network Connection (Twisted Pair)

Name: : Net

Location : Front panel

Physical implementation : 8-pin RJ45 connector (female)

10Base-T		
Pin	Mnemonic	Signal Description
1	TD+	Transmit Data +
2	TD-	Transmit Data -
3	RD+	Receive Data +
4	n.c.	
5	n.c.	
6	RD-	Receive Data -
7	n.c.	
8	n.c.	

Table 13: Signal Assignments for 10BaseT 'Net' Interface

4.3.10. Network Connection (Coax)

Name: : Net

Location : Front panel

Physical implementation : RG58 BNC connector (female)

10Base-2		
Pin	Mnemonic	Signal Description
1	CDS	Collision Detect Sense
2	TXO/RXI	Transmitter/Receiver

Table 14: Signal Assignments for 10Base2 'Net' Interface

4.3.11. Graphics Interface for Analog Monitors

Name: : CRT

Location : Front panel

Physical implementation : 15-pin HD-D-Sub connector (female)

The pin assignment is compatible with off-the-shelf (S)VGA boards.

Analog Monitors	
Pin	Mnemonic
1	RED
2	GREEN
3	BLUE
4	n.c.
5	GND
6	AGND
7	AGND
8	AGND
9	n.c.
10	GND
11	n.c.
12	n.c.
13	Hsync
14	Vsync
15	n.c.

Table 15: Signal Assignments for ‘CRT’ Graphics Interface

4.3.12. Graphics Interface for LCD Panels (PanelLink)

Name: : TMDS

Location : Front panel

Physical implementation : 8-pin RJ45 connector (female)

The PanelLink connection is Kontron Solutions -specific.

LVDS	
Pin	Mnemonic
1	TXC+
2	TXC-
3	TX0+
4	TX1-
5	TX1+
6	TX0-
7	TX2+
8	TX2-

Table 16: Signal Assignments for 'LVDS' Graphics Interface

The LCD connection is used for controlling several panel classes that differ in timing, resolution, and pinning. The adaptation for various interfaces is achieved through graphics controller programming (through graphics BIOS). The LCD data lines of the graphics controller are mapped to the TFT signals according to the panel class.

In the **VisionCompact® IIa**, a panel interfacing is not directly connected to the LCD data lines of the graphics controller. Instead, the LCD data signals are sent via the PanelLink 65100 transmitter (C&T) that converts the LCD data signals into a serial data stream. (For pinning, see above.)

To convert the serial data stream into parallel (into TFT signals), a PanelLink receiver module is required. The output signals of the receiver are directly connected to the TFT signals.
Information on mapping the PanelLink output signals to the TFT signals is available, upon request, from Kontron Solutions.

4.3.13. Power Supply

Name: : Power
Location : Front panel
Physical implementation : 2-pin plug-in type terminal strip

Power supply		
Pin	Mnemonic	Signal Description
- (Minus)	0V	Reference potential
+ (Plus)	24V	24 VDC

Table 17: Signal Assignments for Power Supply Connection

4.3.14. Digital Output

Name: : DO

Location : Front panel

Physical implementation : 2-pin plug-in type terminal strip

Reset		
Pin	Mnemonic	Signal Description
1	C	Collector
2	E	Emitter

Table 18: Signal Assignments for Digital Output ‘DO’

4.3.15. Digital Input

Name: : DI

Location : Front panel

Physical implementation : 2-pin plug-in type terminal strip

Reset		
Pin	Mnemonic	Signal Description
1	A (+)	Anode
2	K (-)	Cathode

Table 19: Signal Assignments for Digital Input ‘DI’

The thresholds of the digital input are as follows:

Voltage on U_{AK}	Internal Level	Reg. DIGIO, Bit0
0...2.5 V	LOW	0
5...24 V	HIGH	1

Table 20: ‘DI’ Digital Input Thresholds

4.3.16. ISA Bus Connection (Internal)

Name: : ISA bus

Location : left side panel

Physical implementation : 96-pin DIN connector

ISA Bus			
Pin	Row A	Row B	Row C
1	GND	#I_MASTER	#I_IOCHCK
2	I_RESETDRV	I_SD15	I_SD07
3	VCC	I_SD14	I_SD06
4	I_IRQ09	I_SD13	I_SD05
5	#I_MEMR	I_SD12	I_SD04
6	I_DRQ02	I_SD11	I_SD03
7	M0V	I_SD10	I_SD02
8	#I_ENDXFR	I_SD09	I_SD01
9	M24V-EX	I_SD08	I_SD00
10	GND	#I_SBHE	I_IOCHRDY
11	#I_SMEMW	I_LA23	I_AEN
12	#I_SMEMR	I_LA22	I_SA19
13	#I_IOW	I_LA21	I_SA18
14	#I_IOR	I_LA20	I_SA17
15	#I_DACK03	I_LA19	I_SA16
16	I_DRQ03	I_LA18	I_SA15
17	#I_DACK01	I_LA17	I_SA14
18	I_DRQ01	#I_DACK07	I_SA13
19	#I_REFRESH	I_DRQ07	I_SA12
20	I_SYSCLK	#I_DACK06	I_SA11
21	I_IRQ07	I_DRQ06	I_SA10
22	I_IRQ06	#I_DACK05	I_SA09
23	I_IRQ05	I_DRQ05	I_SA08
24	I_IRQ04	#I_DACK00	I_SA07
25	I_IRQ03	I_DRQ00	I_SA06
26	#I_DACK02	#I_MEMCS16	I_SA05
27	I_TC	#I_IOCS16	I_SA04

28	I_BALE	I_IRQ15	I_SA03
29	VCC	I_IRQ14	I_SA02
30	I_OSC	I_IRQ12	I_SA01
31	#I_MEMW	I_IRQ11	I_SA00
32	GND	I_IRQ10	GND

Table 21: Signal Assignments for ISA Bus Connection

4.4. Settings

4.4.1. BIOS

The BIOS comprises numerous functions, including:

- Automatic detection of processor type
- Automatic detection and testing of main memory size and organization
- Automatic detection and testing of cache size and organization
- Support of non-standardized systems
- Support of several parallel and serial ports
- Password support
- Hard disk analysis
- Video and system BIOS shadowing



The BIOS Setup factory settings are correct and should normally not be modified by the customer!

The SYSTEM BIOS includes extensive SETUP capabilities.

The BIOS SETUP is accessed by pressing the **<del>** function key during boot-up. The parameter settings are self-explanatory.

It may be necessary to modify certain settings in order to configure the **VisionCompact® IIa** according to customer requirements. Utmost care is necessary when modifying configuration settings. Some configuration settings are factory settings and should not be modified by the customer.

4.5. Software Installation

4.5.1. Graphics Drivers

Graphics Driver Installation for Windows 95:

The following steps are required to install the graphics drivers for Windows 95:

* In the Windows 95 „Start“ menu, select „Settings“ and then „Control Panel“.
* Select „Display“.
* In „Display“, select the submenu „Settings“ and click on the button „Change Configuration“.
* In the menu „Change Configuration“, click on „Change“ for the graphics card.
* In the window „Select Model“, click on „Have Disk“.
* Insert the diskette with the graphics drivers into the floppy disk drive. In the window „Install from disk“, click „OK“.
* In the menu „Select Model“, select the type „Chips and Technologies Accelerator (new)“ and click „OK“.

The installation process is starting. The required files are copied to the hard disk.

After copying is completed, perform the following steps:

* Close the submenu „Change Configuration“.
* Close the menu „Display Properties“.

In order for the changes to take effect, reboot the computer after the installation process is completed.

For installation or reinstallation, Windows must be operated with a standard VGA driver.

The **VisionCompact® IIa** graphics function works with the Windows drivers VGA 640x480x16 as well as with SVGA 800x600x16.



For SVGA 800x600x16, the LCD panel must provide the required resolution for simultaneous or LCD stand-alone operation. However, this resolution is generally suited only for sole operation with a CRT monitor, since these panels are still rare.
The popular LCD panels with 640 x 480 may only be used with the VGA driver.

Higher resolutions require the Chips & Technologies® driver that have been supplied. If the screen resolution is higher than can be displayed on the LCD panel, the highest displayable physical resolution is used. Invisible areas of the screen can be reached through panning. Panning is initiated by moving the mouse to the edge of the screen.

If sole operation with a CRT monitor is intended, it is recommended to select this mode with the Chipscpl utility in order to display the full image with the desired resolution. It is also possible to generate a customer-specific Bios version where only the CRT mode is active.

4.5.1.1. Chipscpl Utility

The Chipscpl utility is integrated into the system control during automatic installation.. This utility enables direct switching between the different operating modes, for example:

- Panel mode
- CRT mode
- Simultaneous mode

Caution:
This option is only available by manually installing the manufacturer’s original drivers; the drivers supplied with Windows 95 do not offer this option.

4.5.2. Ethernet Drivers

Ethernet Driver Installation for Windows 95:

The following steps are required to install the Ethernet drivers for Windows 95:

* In the Windows 95 „Start“ menu, select „Settings“ and then „Control Panel“.
* Select „Network“.
* In „Network“, select the submenu „Configuration“ and click on the button „Add“.
* In „Select Network Component“, select the setting „Network Card“ and the click on „Add“.
* Click on „Have Disk“.
* Insert the disk with the Ethernet drivers into the floppy disk drive and click „OK“(or specify the corresponding path).
* „Select Network Card“ is displayed. Select „Crystal Semiconductor“ (manufacturer) and then „Crystal LAN™ CS8900 Ethernet Adapter“ (network card). Click on „OK“.
* Close „Network“ by clicking „OK“.
* In „Properties of Crystal LAN™ CS8900 Ethernet Adapter“, set the I/O address range 300 and interrupt 5.
* The corresponding files are copied to the hard disk (the corresponding source directories may have to set). During this installation, several Windows 95 installation files are required.
* In order for the changes to take effect, reboot the computer after successful installation.

The computer may only be connected to the network through the 10Base-T or 10Base-2 interface.

Network Configuration Setup:

The factory default settings for the network adapter are as follows:

Product ID	CS8900
Adapter Serial Number	00000009 [1)]
Ethernet Address	00:20:34:20:00:09 [1)]
EEPROM	64 Bytes
I/O Port Base Address	300
Interrupt Request Level	5
Shared Memory	Disabled [2)]
Boot PROM	Disabled
OS Optimization	DOS
Transmission Control	Auto Negotiate
Connector Type	Auto Detect [3)]

Table 22: Ethernet Adapter Configuration

If possible, the factory settings should remain unchanged.

Use the CS8900 setup utility program „setup.exe“ to change the network configuration. The program is located on the network driver floppy disk supplied by Kontron Solutions. The settings can be changed with „Manual Configure“ in the submenu „Adapter“.

Only the settings in the „gray“ areas listed in the above table can be reconfigured; the settings in the „light“ areas cannot be changed.

[1)] Address and serial number dependent upon system. The above numbers are only examples.

[2)] If memory accesses instead of I/O accesses are to be used for network communications, the base address D8000h must be entered here (setting is possible for DOS, Windows 3.11, and Windows 95). However, please note that this operating mode is not supported for Windows NT 4.0! In this case, setting a memory range can result in malfunction.

[3)] If only one of the two network connections works, check that the entry „Connector Type“ is set to „Auto Detect“.



It is recommended to change only the base address and the interrupt request level.

The factory settings for Boot PROM, OS Optimization, Transmission Control, and Connector Type must not be changed. When changing the „Shared Memory“ configuration, please note footnote 2); however, it is advisable to keep the default setting „disabled“.

5. Programming Model

5.1. Memory Range

The 4 GB CPU address space is structured as follows:

Adresse		Belegung	
0000.0000h - 000F.FFFFh	0000.0000h – 0007.FFFFh	PC-RAM	0K...512K
	0008.0000h – 0009.FFFFh	Optional Memory Hole	512K...640K
	000A.0000h – 000B.FFFFh	Video Buffer	640K...768K
	000C.0000h – 000D.FFFFh	ISA Expansion Area	768K...896K
	000E.0000h – 000F.FFFFh	(Extended) System BIOS	896K...1M
0010.0000h - Top of Main Memory	0010.0000h – 00EF.FFFFh	DRAM	1M...15M
	00F0.0000h – 00FF.FFFFh	Optional Memory Hole	15M...16M
	0100.0000h – Top of Main Memory	DRAM	16M..ToMM
Top of Main Memory - FFFF.FFFFh	Top of Main Memory- FFDF.FFFFh	PCI Memory, inkl. AGP Memory Window,	ToMM... (4G-2M)
	FFE0.0000h – FFFF.FFFFh	PCI Memory, high BIOS Area	(4G-2M)...4G

Table 23: **VisionCompact® IIa** Address Space

5.2. I/O Range

The CPU I/O range (**VisionCompact® IIa** base station) is functionally divided into three areas:

- Standard PC I/O ports
- Special chip set register
- Special I/O registers

Address	Mapping	Mnemonic
0300h – 030Fh	Ethernet	
4000h – 40FFh	Card / IOCHCK Enable	ENABLE
5000h – 50FFh	CAN Channel A	
5100h – 51FFh	CAN Channel B	
5200h – 52FFh	CAN Interr. Register	CAN_IRQ
7000h – 70FFh	Address Register	ADR
7500h – 75FFh	Watchdog Trigger	WDOG
7600h – 76FFh	Configuration Port	KONFIG
7700h / 7701h	Reserved	
7900h – 79FFh	IRQx to NMI	IRQ_NMI
7B00h – 7BFFh	NMI reason	NMI_RS
7D00h – 7DFFh	Real Time Tick	RTT
7E00h – 7EFFh	Diagnostic port	DIAG
7F00h – 7FFFh	digit. I/O register	DIGIO
C000h – FFFFh	SRAM	

Table 24: Special Base Station I/O Registers

The registers of the graphic adapter are mapped to the following address space. A detailed description is in the datasheet of the C&T 69000 (by request at Kontron Solutions obtainable).

Address	Mapping	Mnemonic
03B0h – 03DFh	Graphic controller	

Table 25: Graphics I/O Registers

The following table shows the required chipset registers to control the system management bus. (→ datasheet "82371EB PCI-to-ISA/IDE Xcelerator)

Adresse	Belegung	Mnemonic
Base[1)] + (00h)	SMB Host Status Register	SMBHSTSTS
Base + (01h)	SMB Slave Status Register	SMBSLVSTS
Base + (02h)	SMB Host Control Register	SMBHSTCNT
Base + (03h)	SMB Host Command Register	SMBHSTCMD
Base + (04h)	SMB Host Address Register	SMBHSTADD
Base + (05h)	SMB Host Data 0 Register	SMBHSTDAT0
Base + (06h)	SMB Host Data 1 Register	SMBHSTDAT1
Base + (07h)	SMB Block Data Register	SMBBLKDAT
Base + (08h)	SMB Slave Control Register	SMBSLVCNT
Base + (09h)	SMB Shadow Command Reg.	SMBSHDWCMD
Base + (0Ah)	SMB Slave Event Register	SMBSLVEVT
Base + (0Ch)	SMB Slave Data Register	SMBSLVDAT

Table 26: SMBus I/O-Register

[1)] The SMB base of the VC2a is located at address 10A0h. (Assignment through the system BIOS).

5.3. Register Mapping

Only special I/O registers and the CAN controller registers, are discussed here. For information about Ethernet registers, see the Crystal network controller CS8900 data sheet.

5.3.1. ENABLE

Address: 4000h-40FFh

Read access:

Reading the ENABLE register I/O sets the CRD bit in the KONFIG register.

CRD must be set for the following actions:

- SRAM access (protected, segment, I/O);
- Register access to ADR, WDOG, IRQ_NMI, NMI_RS, RTT, DIAG, and DIGIO;

The following registers can be accessed independently of CRD:

- KONFIG, CAN_IRQ

Write access:

Writing to the ENABLE register I/O sets the NMI EN bit in the KONFIG register.→ Global enabling of an NMI (fan failure, tick, etc.)

5.3.2. CAN

Address: 5000h-50FFh (CAN channel A, front connection)
5100h-51FFh (CAN channel B, lateral connection)

The CAN controller SJA1000 programming model is listed in the following table. A detailed register description can be found in the data book[1)] or is available, upon request, from Kontron Solutions.

[1)] Bibliography sources [14]

Offset (hex.). to Base Address	Segment	Operating Mode		Reset Mode	
		Read	Write	Read	Write
00	Control	Control		Control	
01		Command		Command	
02		Status	-	Status	-
03		Interrupt	-	Interrupt	-
04		(FFh)	-	Acceptance Code	
05		(FFh)	-	Acceptance Mask	
06		(FFh)	-	Bus Timing 0	
07		(FFh)	-	Bus Timing 1	
08		(FFh)	-	Output Control	
09		Test		Test	
0A		Identifier 10..3		(FFh)	-
0B	Transmit Buffer	Identifier 2..0, RTR, DLC		(FFh)	-
0C		Byte 1		(FFh)	-
0D		Byte 2		(FFh)	-
0E		Byte 3		(FFh)	-
0F		Byte 4		(FFh)	-
10		Byte 5		(FFh)	-
11		Byte 6		(FFh)	-
12		Byte 7		(FFh)	-
13		Byte 8		(FFh)	-
14	Receive Buffer	Identifier 10..3		Identifier 10..3	
15		Identifier 2..0, RTR, DLC		Identifier 2..0, RTR, DLC	
16		Byte 1		Byte 1	
17		Byte 2		Byte 2	
18		Byte 3		Byte 3	
19		Byte 4		Byte 4	
1A		Byte 5		Byte 5	
1B		Byte 6		Byte 6	
1C		Byte 7		Byte 7	
1D		Byte 8		Byte 8	
1E		(FFh)	-	(FFh)	-
1F		Clock Divider		Clock Divider	

Table 27: Register Map of CAN Controller SJA1000

5.3.3. CAN_IRQ

Address: 5200h-52FFh

The ISA interrupt level of both CAN controllers is selected by initializing the CAN_IRQ register accordingly. The levels for the CAN channels must be different.

Read access:

0	0	0	0	0	IB2	IB1	IB0	0	0	0	0	0	IA2	IA1	IA0
D15							D08	D07							D00

Write access:

x	X	x	X	x	IB2	IB1	IB0	x	x	x	x	X	IA2	IA1	IA0
D15							D08	D07							D00

IAx: CAN Channel A – Interrupt Select Bits 2..0

IA2	IA1	IA0	ISA Interrupt	
0	0	0	disabled	Default
0	0	1	I_IRQ05	
0	1	0	I_IRQ09	
0	1	1	I_IRQ10	
1	0	0	I_IRQ11	
1	0	1	I_IRQ12	
1	1	0	I_IRQ15	
1	1	1	Disabled	

Ibx: CAN Channel B – Interrupt Select Bits 2..0

IB2	IB1	IB0	ISA Interrupt	
0	0	0	disabled	Default
0	0	1	I_IRQ05	
0	1	0	I_IRQ09	
0	1	1	I_IRQ10	
1	0	0	I_IRQ11	
1	0	1	I_IRQ12	
1	1	0	I_IRQ15	
1	1	1	Disabled	

Default state after system reset:

0000h

5.3.4. ADR

Address: 7000h-70FFh

The address register enables I/O (C000h-FFFFh) or MEM access to the SRAM (256 K sizes) in real mode (default: D0000h- D3FFFh). The address register sets 16 pages with 16 K each.

Read/write access:

X	x	x	x	x	x	A17	A16	A15	A14	x	x	x	x	x	x
D15							D08	D07							D00

Default state after system reset:

0000h

The SRAM memory map is listed in the following table:

Protected Mode	Initialisation ADR-Reg.	I/O-Access	Segm.-Access
FBFFFFh FBC000h...	Page 15 : Value 03C0h	FFFFh C000h...	D3FFFh D0000h...
FBBFFFh FB8000h...	Page 14 : Value 0380h	FFFFh C000h...	D3FFFh D0000h...
FB7FFFh FB4000h...	Page 13 : Value 0340h	FFFFh C000h...	D3FFFh D0000h...
FB3FFFh FB0000h...	Page 12 : Value 0300h	FFFFh C000h...	D3FFFh D0000h...
FAFFFFh FAC000h...	Page 11 : Value 02C0h	FFFFh C000h...	D3FFFh D0000h...
FABFFFh FA8000h...	Page 10 : Value 0280h	FFFFh C000h...	D3FFFh D0000h...
FA7FFFh FA4000h...	Page 9 : Value 0240h	FFFFh C000h...	D3FFFh D0000h...
FA3FFFh FA0000h...	Page 8 : Value 0200h	FFFFh C000h...	D3FFFh D0000h...
F9FFFFh F9C000h...	Page 7 : Value 01C0h	FFFFh C000h...	D3FFFh D0000h...
F9BFFFh F98000h...	Page 6 : Value 0180h	FFFFh C000h...	D3FFFh D0000h...
F97FFFh F94000h...	Page 5 : Value 0140h	FFFFh C000h...	D3FFFh D0000h...
F93FFFh F90000h...	Page 4 : Value 0100h	FFFFh C000h...	D3FFFh D0000h...
F8FFFFh F8C000h...	Page 3 : Value 00C0h	FFFFh C000h...	D3FFFh D0000h...
F8BFFFh F88000h...	Page 2 : Value 0080h	FFFFh C000h...	D3FFFh D0000h...
F87FFFh F84000h...	Page 1 : Value 0040h	FFFFh C000h...	D3FFFh D0000h...
F83FFFh F80000h...	Page 0 : Value 0000h	FFFFh C000h...	D3FFFh D0000h...

Table 28: SRAM Memory Map

5.3.5. WDOG

Address: 7500h-75FFh

Read access:

Reading the WDOG register I/O activates the watchdog and sets the WD bit in the DIAG register.

When this condition is satisfied, the LED in the front panel lights for visual control.

Write access:

Writing to the WDOG register I/O deactivates the watchdog and clears the WD bit in the DIAG register.

For version „**VisionCompact® IIa** -...“, the watchdog must be constantly re-triggered within a 400 ms interval through read-access to the WDOG I/O address. If this trigger interval is exceeded, a system RESET is automatically triggered. The watchdog trigger time can be set by the customer.

5.3.6. KONFIG

Address: 7600h-76FFh

Register and SRAM access is enabled or disabled via the interface configuration register. KONFIG register access is possible prior to read access to 40xxh that is required for I/O register enabling.

Read access:

CRD	x	CS3	CS2	CS1	I/O	SEG	PRO	CRD	X	x	NMI EN	x	I/O	SEG	PRO
D15							D08	D07							D00

Write access:

X	x	CS3	CS2	CS1	x	X	x	CRD	X	x	NMI EN	x	I/O	SEG	PRO
D15							D08	D07							D00

CRD: Card Enable

CRD = 0: Register access (to special I/O registers) disabled

CRD = 1: Register access to special I/O registers enabled

CSx: Segment select bits 3..1 (segmented SRAM addressing)

CS3	CS2	CS1	Segment	
0	0	1	C8	
0	1	0	D0	Default
0	1	1	D8	
1	0	0	E0	
1	0	1	E8	

I/O: SRAM I/O access enable

I/O = 0: I/O access (to SRAM) disabled

I/O = 1: I/O access (to SRAM) enabled

SEG: SRAM segment access enable

SEG = 0: Segment access (to SRAM) disabled

SEG = 1: Segment access (to SRAM) enabled

PRO: SRAM access enable in protected mode

PRO = 0: SRAM access in protected mode disabled

PRO = 1: SRAM access in protected mode enabled

NMI EN: #IOCHCK enable

NMI EN = 0: NMI triggering globally disabled

NMI EN = 1: NMI triggering enabled

Default state after system reset:

1202h

5.3.7. IRQ_NMI

Address: 7900h-79FFh

The events triggering an NMI can be selected in register IRQ_NMI.

The following events can result in an NMI:

- ISA bus interrupt („n out of m“ selection)
- Drop in power (power failure)
- Exceeding a temperature limit set in LM75 or LM80
- Fan failure of the CPU fan or one of the case fans
- Digital input signal (DI0) to X17

Read access:

DIN	TMP	PFO	FAN	0	I15	I14	I12	I11	I10	I09	I07	I06	I05	I04	I03
D15							D08	D07							D00

Write access:

DIN	TMP	PFO	FAN	x	I15	I14	I12	I11	I10	I09	I07	I06	I05	I04	I03
D15							D08	D07							D00

DIN: Digital input 0 (to X17)

DIN = 0: Digital input 0 has no effect on NMI

DIN = 1: Setting digital input 0 results in NMI

TMP: Temperature overrange in LM75 or LM80

TMP = 0: Temperature overrange has no effect on NMI

TMP = 1: Temperature overrange results in NMI

PFO: Power failure

PFO = 0: Power failure has no effect on NMI

PFO = 1: Power failure results in NMI

FAN: Fan failure

FAN = 0: Fan failure has no effect on NMI

FAN = 1: Fan failure results in NMI

Ix: ISA bus interrupt

Ix = 0: ISA bus interrupt Ix has no effect on NMI

Ix = 1: ISA bus interrupt Ix results in NMI

Default state after system reset:

0000h

5.3.8. NMI_RS

Address: 7B00h-7BFFh

The cause of the NMI can be determined by reading register NMI_RS (NMI reason). If the NMI was triggered by the timer or an ISA bus interrupt, the NMI is not disabled until after reading the NMI_RS register.

Read access:

DIN	TMP	PFO	FAN	RTT	I15	I14	I12	I11	I10	I09	I07	I06	I05	I04	I03
D15							D08	D07							D00

DIN: Digital input 0 (to X17)

DIN = 0: Digital input 0 was not set

DIN = 1: Digital input 0 was set (HIGH) and has triggered NMI

TMP: Temperature overrange in LM75 or LM80

TMP = 0: Temperature OK

TMP = 1: Temperature overrange

PFO: NMI triggered by power failure

PFO = 0: Power OK

PFO = 1: Power failure

FAN: NMI triggered by fan failure

FAN = 0: Fan OK

FAN = 1: Fan failure

RTT: NMI triggered by timer

RTT = 0: NMI not triggered by timer

RTT = 1: NMI triggered by timer

Ix: ISA bus interrupt

Ix = 0: NMI not triggered by ISA bus interrupt Ix

Ix = 1: NMI triggered by ISA bus interrupt Ix

Write access:

N/A

Default state after system reset:

0000h

5.3.9. RTT

Address: 7D00h-7DFFh

The time base for the tick is set to 0.1 ms via the RTT (real time tick) register. The tick set in RTT triggers an NMI only when bit 4 is set in register KONFIG (global NMI enabling). A tick that occurs during a disabled NMI is stored and triggers an NMI immediately after re-enabling.

Read access:

0	0	0	0	0	0	RT9	RT8	RT7	RT6	RT5	RT4	RT3	RT2	RT1	RT0
D15							D08	D07							D00

Write access:

X	x	x	x	x	x	RT9	RT8	RT7	RT6	RT5	RT4	RT3	RT2	RT1	RT0
D15							D08	D07							D00

RT9..0: Time base selection for tick

The tick is calculated as follows:

TICK = RT9..0 * 0.1 ms

Default state after system reset:

0000h

5.3.10. DIAG

Address: 7E00h-7EFFh

The DIAG (diagnostic port) register represents one part of the **VisionCompact® IIa** status display. Bit 5 (WD) displays the current watchdog status. The bit pattern stored in diagnostic port bits 4 and 3 is displayed on the LED array (P04 and P03).
Bits DG2...DG0, however, have no meaning after a reset and are not displayed on the LED array. Instead, LED „P00“ is used to indicate hard-disk access and LED „P01“ to indicate network activity (network on interrupt level 5). A fan failure is indicated, when LED „P02“ illuminates. In order to represent bits DG2...DG0 (same as DG4 and DG3) on the LED array, the corresponding bit must set in the DIAG register. If bit DG2, DG1 or DG0 were set to 1 at one point, it is not possible to switch back to displaying fan failure, HDD accesses or network activity (→ reset is required). If the default state is to be kept after system reset (display of fan failure, HDD accesses or network accesses), bit 0...bit 2 (DG0..DG2) can only be set to 0.

Read access:

X	x	WD	DG4	DG3	DG2	DG1	DG0
D07							D00

Write access:

X	x	x	DG4	DG3	DG2	DG1	DG0
D07							D00

WD: Watchdog status

WD = 0: Watchdog turned off

WD = 1: Watchdog turned on

DG4..3: Diagnostic bits 4..3

The diagnostic bits are displayed on the status display LEDs P04..P03.

DGx = 0: LED P0x turned off

DGx = 1: LED P0x turned on

DG2: Diagnostic bit 2

After system reset:

DG2 = 0, the diagnostic bit is not displayed on the LED display;

after having been set to 1:

DG2 = 0: LED P02 turned off

DG2 = 1: LED P02 turned on

DG1: Diagnostic bit 1

After system reset:

DG1 = 0, the diagnostic bit is not displayed on the LED display;

after having been set to 1:

DG1 = 0: LED P01 turned off

DG1 = 1: LED P01 turned on

DG0: Diagnostic bit 0

After system reset:

DG0 = 0, the diagnostic bit is not displayed on the LED display;

after having been set to 1:

DG0 = 0: LED P00 turned off

DG0 = 1: LED P00 turned on

Default state after system reset:

00h

5.3.11. DIGIO

Address: 7F00h-7FFFh

The DIGIO register is used to set or clear the digital outputs DO0..DO7. In addition, the state of the digital inputs DI0..DI7 and of the above-mentioned digital outputs can be determined. One opto-isolated digital input and one opto-isolated digital output are available:

- Input DI0 is controlled by the 2-pin terminal strip ‘DI’.
- Output DO0 is connected to the terminal strip ‘DO’.

Read access:

DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0	DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
D15							D08	D07							D00

Write access:

DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0	x	x	x	X	x	x	x	x
D15							D08	D07							D00

DI7...DI1: Digital input No. 7...1

DIx = 0: Digital input cleared

DIx = 1: Digital input set

DI0: Digital input No. 0

DI0 = 0: Digital input cleared

Level of U = 0...2.5 V is applied to ‘DI’

DI0 = 1: Digital input set

Level of U = 5...14 V is applied to ‘DI’

DO7...DO1: Digital output No. 7...1

DOx = 0: Digital output cleared

DOx = 1: Digital output set

DO0: Digital output No. 0

DOx = 0: Digital output cleared

Output ‘DO’ disabled

DOx = 1: Digital output set

Output ‘DO’ switched through

Default state after system reset:

0001h

6. Application

6.1. Enabling/Disabling the Watchdog

The code listed below contains extracts from a program for:

- Enabling and triggering the watchdog
- Disabling the watchdog

```
/*    Definition of constants                                    */
      #define ENABLE 0x4000
      #define WDOG 0x7500

/*    Enabling register access to special I/O registers          */
      inport (ENABLE);

/*    Enabling and triggering the watchdog                       */
      do
            {
            inport (WDOG);
            }
      while (?);              /* Triggering until event ? occurs  */

/*    Disabling the watchdog                                     */
      outport (WDOG, 0x0000);
```

6.2. SRAM Access through I/O Cycle

The following lists an example for a SRAM access through I/O cycle.

```
/*    Definition of constants                                          */
      #define ENABLE 0x4000
      #define ADR 0x7000
      #define KONFIG 0x7600

/*    Enabling register access to special I/O registers                */
      inport (ENABLE);

/*    Enabling SRAM access through I/O cycle                           */
      outportb (KONFIG, 0x87);

/*    Selection of page 1                                              */
/*    i.e., I/O address C000h corresponds to physical address F84000h  */
      outport (ADR, 0x0040)

/*    Reading a word from SRAM, ISA address F84002h                    */
      inport (0xC002)

/*    Selection of page 5                                              */
/*    i.e., I/O address C000h corresponds to physical address F94000h  */
      outport (ADR, 0x0140)

/*    Reading a word from SRAM, ISA address F94002h                    */
      inport (0xC002)
```

6.3. Control of the SMBus Host Controller

To access a SMBus device with the host controller of the Southbridge, you have to follow the following instructions:

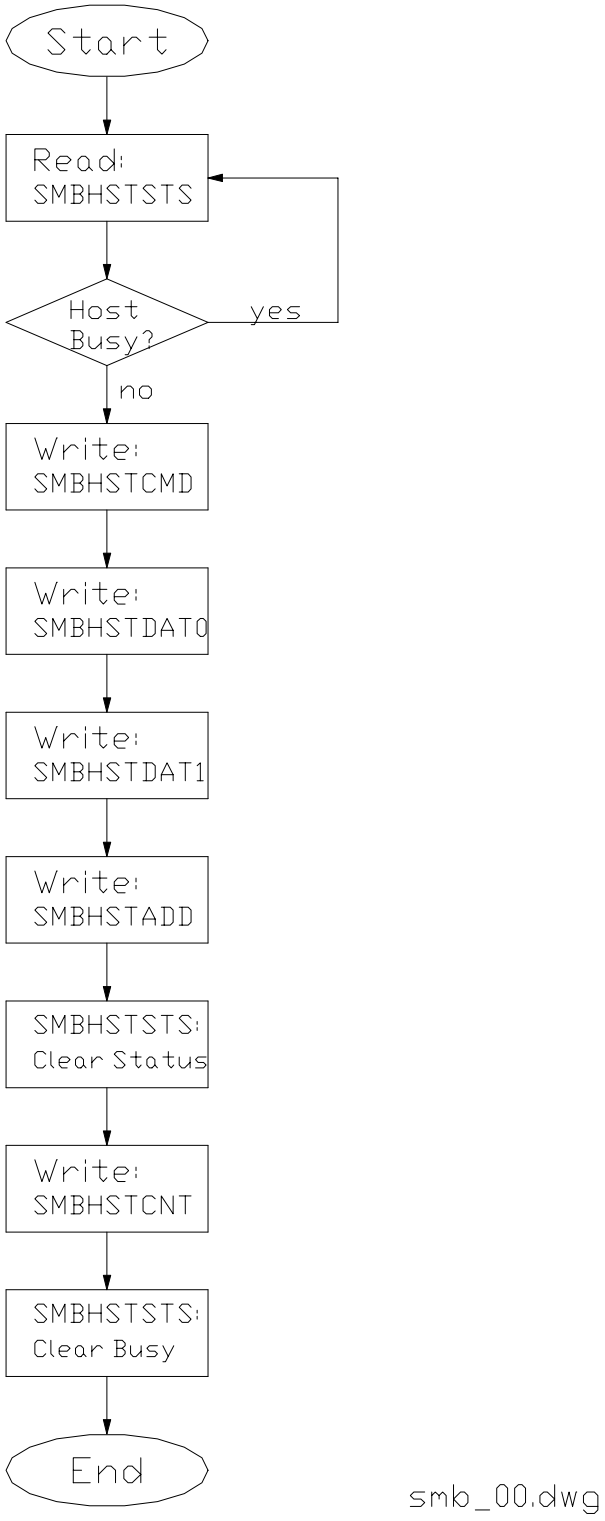


Figure 5: Access a SMBus device

6.4. Super I/O: GPIO Port Control

As previously mentioned, the selection between the two case fans occurs through GPIO10 (general purpose I/O port 10). The port pins are controlled as follows:

```
/*-------- Definitions ----------------------------------------------------------------------*/
#define IND_REG     0x2E            // Super I/O PC97307 index register
#define DAT_REG     0x2F            // Super I/O PC97307 data register


/*-------- Variables ------------------------------------------------------------------------*/
unsigned int base_MSB;              // Base address MSB of the GPIO ports
unsigned int base_LSB;              // Base address LSB of the GPIO ports
unsigned int base;                  // Base address of the GPIO ports


/*-------- Super I/O GPIO10 Initialization --------------------------------------*/

outportb(IND_REG,0x07);             // Address PnP Reg. Logical Device Select
outportb(DAT_REG,0x07);       // Selection of Log. Device 7 (GPIO Ports)

outportb(IND_REG,0x30);             // Addressing the Activate Register
wert = inportb(DAT_REG);
wert = wert || 0x01;                // Set bit 0 (Device Enable) selectively
outportb(IND_REG,0x30);
outportb(DAT_REG,wert);             // Back to Act. Reg.

outportb(IND_REG,0x01);             // Addressing FER2 (function enable reg.)
wert = inportb(DAT_REG);
wert = wert || 0x80;                // Set bit 7 (Port 1+2 Enable) selectively
outportb(IND_REG,0x01);
outportb(DAT_REG,wert);             // Back to FER2
```

```
outportb(IND_REG,0x60);          // Base address MSB of the GPIO ports
determination
base_MSB = inportb(DAT_REG);
outportb(IND_REG,0x61);          // Base address LSB of the GPIO ports
determination
base_LSB = inportb(DAT_REG);
base_MSB = base_MSB << 8;        // Shift 8 bits to the left
base_LSB = base_LSB & 0xF8;      // Clear bit 2..0
base = base_MSB + base_LSB;      // Base address of the GPIO ports

outportb((base+0x03), 0xFE);     // Port1, Pull-Up Control, GPIO10 turn off
outportb((base+0x01), 0x01);     // Port1, Direction, GPIO10 = Output

outportb(base, 0x00);            // Clear GPIO10, set LOW
```

or

```
outportb(base, 0x01);            // Set GPIO10, set HIGH
```

7. Diagnostics

7.1. POST Codes

POST_STATUS_CPUTEST	01h	CPU register test about to start.
POST_STATUS_DELAY	02h	NMIs are disabled; delay starts.
POST_STATUS_DELAYDONE	03h	power-on delay finished.
POST_STATUS_KBDBATRDY	04h	kbd BAT done; reading kbd SYS bit.
POST_STATUS_DISABSHADOW	05h	disabling shadowing & cache.
POST_STATUS_CALCCKSUM	06h	calcing ROM cksum, wait kbd ctrlr.
POST_STATUS_CKSUMGOOD	07h	cksum okay, kbd ctrllr free.
POST_STATUS_BATVRFY	08h	verifying BAT cmd to kbd ctrllr.
POST_STATUS_KBDCMD	09h	issuing kbd ctrllr cmd byte.
POST_STATUS_KBDDATA	0ah	issuing kbd ctrllr data byte.
POST_STATUS_BLKUNBLK	0bh	issuing pin 23,24 blocking & unblocking.
POST_STATUS_KBDNOP	0ch	issuing kbd ctrllr NOP cmd next.
POST_STATUS_SHUTTEST	0dh	testing CMOS RAM shutdown register.
POST_STATUS_CMOSDIAG	0eh	checking CMOS cksum, updating DIAG byte.
POST_STATUS_CMOSINIT	0fh	initializing CMOS (if req'd every boot).
POST_STATUS_CMOSSTATUS	10h	init CMOS status reg for date/time.
POST_STATUS_DISABDMAINT	11h	disabling DMA, interrupt ctrllrs.
POST_STATUS_DISABPORTB	12h	disabling Port B, disabling video display.
POST_STATUS_BOARD	13h	init board, start auto-mem detect.
POST_STATUS_TESTTIMER	14h	starting timer tests.
POST_STATUS_TESTTIMER2	15h	testing 8254 T2, for spkr, part B.
POST_STATUS_TESTTIMER1	16h	testing 8254 T1, for refresh.
POST_STATUS_TESTTIMER0	17h	testing 8254 T0, for 18.2Hz.
POST_STATUS_MEMREFRESH	18h	starting memory refresh.
POST_STATUS_TESTREFRESH	19h	testing memory refresh.
POST_STATUS_TEST15US	1ah	testing 15usec refresh ON/OFF time.
POST_STATUS_TESTDATA	1ch	testing data lines.
POST_STATUS_TESTADDR	20h	testing address lines.
POST_STATUS_TESTPARITY	21h	testing parity (toggling).
POST_STATUS_TESTMEMRDWR	22h	base 64KB mem read/write test.
Now we have memory, so we can use a stack to use Pcall, not Rcall.		
POST_STATUS_SYSINIT	23h	system init before vector table init.
POST_STATUS_INITVECTORS	24h	init vector table.
POST_STATUS_8042TURBO	25h	reading 8042 for turbo switch setting.
POST_STATUS_POSTTURBO	26h	initializing turbo data.
POST_STATUS_POSTVECTORS	27h	any init after vector table init is next.
POST_STATUS_MONOMODE	28h	setting monochrome mode.
POST_STATUS_COLORMODE	29h	setting color mode.
POST_STATUS_TOGGLEPARITY	2ah	toggle parity before optional video ROM test.
POST_STATUS_INITBEFOREVIDEO	2bh	init before video ROM check.
POST_STATUS_VIDEOROM	2ch	control passed to video ROM.
POST_STATUS_POSTVIDEO	2dh	video ROM returned control.
POST_STATUS_CHECKEGAVGA	2eh	checking for EGA/VGA adapter found.
POST_STATUS_TESTVIDEOMEMORY	2fh	no EGA/VGA found, r/w test of video memory.

POST_STATUS_RETRACE	30h	looking for video retrace signal.
POST_STATUS_ALTDISPLAY	31h	retrace failed, checking alt. display.
POST_STATUS_ALTRETRACE	32h	alt found, checking video retrace signal.
POST_STATUS_VRFYSWADAPTER	33h	compare switches w/actual adapter type.
POST_STATUS_SETDISPMODE	34h	setting display mode.
Now we have a display. All code that outputs codes at 35h and above can use INT 10h to display messages.		
POST_STATUS_CHECKSEG40A	35h	check ROM BIOS data area at seg 40h.
POST_STATUS_SETCURSOR	36h	setting cursor for power-on msg.
POST_STATUS_PWRONDISPLAY	37h	displaying power-on message.
POST_STATUS_SAVECURSOR	38h	save cursor position.
POST_STATUS_BIOSIDENT	39h	display BIOS ident. string.
POST_STATUS_HITDEL	3ah	display "Hit <DEL> to ..." msg.
POST_STATUS_VIRTUAL	40h	preparing vm test. vrfy from display memory.
POST_STATUS_DESCR	41h	preparing descriptor tables.
POST_STATUS_ENTERVM	42h	enter virtual mode for memory test.
POST_STATUS_ENABINT	43h	enable ints for diagnostics mode.
POST_STATUS_CHECKWRAP1	44h	init data for checking wraparound at 0:0.
POST_STATUS_CHECKWRAP2	45h	checking for wrap, find total memory size.
POST_STATUS_HIGHPATTERNS	46h	write extended memory test patterns.
POST_STATUS_LOWPATTERNS	47h	write conventional memory test patterns.
POST_STATUS_FINDLOWMEM	48h	finding low memory size from patterns.
POST_STATUS_FINDHIMEM	49h	finding high memory size from patterns.
POST_STATUS_CHECKSEG40B	4ah	check ROM BIOS data area again.
POST_STATUS_CHECKDEL	4bh	check for <DEL>, clear low mem for soft reset.
POST_STATUS_CLREXTMEM	4ch	clearing ext mem for soft reset.
POST_STATUS_SAVEMEMSIZE	4dh	saving memory size.
POST_STATUS_COLD64TEST	4eh	on cold boot, display 1st 64KB memtest.
POST_STATUS_COLDLOWTEST	4fh	on cold boot, test all of low memory.
POST_STATUS_ADJUSTLOW	50h	adjust memsize for 1K usage.
POST_STATUS_COLDHITEST	51h	on cold boot, test high memory.
POST_STATUS_REALMODETEST	52h	prepare for shutdown to real-mode.
POST_STATUS_ENTERREAL	53h	saved regs & memsize, entering real-mode.
POST_STATUS_SHUTDOWN	54h	shutdown successful, restoring codepath.
POST_STATUS_DISABA20	55h	disabling A20 line.
POST_STATUS_CHECKSEG40C	56h	checking ROM BIOS data area again.
POST_STATUS_CHECKSEG40D	57h	checking ROM BIOS data area some more.
POST_STATUS_CLRHITDEL	58h	clear the "Hit <DEL>" message.
POST_STATUS_TESTDMAPAGE	59h	test DMA page register.
POST_STATUS_VRFYDISPMEM	60h	verify from display memory (???).
POST_STATUS_TESTDMA0BASE	61h	test DMA0 base register.
POST_STATUS_TESTDMA1BASE	62h	test DMA1 base register.
POST_STATUS_CHECKSEG40E	63h	checking ROM BIOS data area again.
POST_STATUS_CHECKSEG40F	64h	checking ROM BIOS data area some more.
POST_STATUS_PROGDMA	65h.	programming DMA ctrllrs 0 & 1.
POST_STATUS_INITINTCTRL	66h	initializing INT ctrllrs 0 & 1.
POST_STATUS_STARTKBDTEST	67h	starting keyboard test.
POST_STATUS_KBDRESET	80h	issuing reset cmd & clring output buffer.
POST_STATUS_CHECKSTUCKKEYS	81h	check for stuck keys & issue test cmd.
POST_STATUS_INITCIRCBUFFER	82h	initializing circular buffer.
POST_STATUS_CHECKLOCKEDKEYS	83h	check for locked keys.
POST_STATUS_CHECKMEMSIZEMISMATCH	84h	check for memsize mismatch (CMOS/BIOSDATA).

POST_STATUS_PASSWORD	85h	check for pswd or bypass setup.
POST_STATUS_BEFORESETUP	86h	pswd checked. do pgming before setup.
POST_STATUS_CALLSETUP	87h	call the setup module.
POST_STATUS_POSTSETUP	88h	back from setup, clr screen.
POST_STATUS_DISPPWRON	89h	display power-on screen message.
POST_STATUS_DISPWAIT	8ah	display "Wait..." message.
POST_STATUS_ENABSHADOW	8bh	do system & video BIOS shadowing.
POST_STATUS_STDCMOSSETUP	8ch	load standard setup params into BIOSDATA.
POST_STATUS_MOUSE	8dh	check and initialize mouse.
POST_STATUS_FLOPPY	8eh	check floppy disks.
POST_STATUS_CONFIGFLOPPY	8fh	configure floppy drives.
POST_STATUS_DIE	90h	check hard disks.
POST_STATUS_CONFIGIDE	91h	configure IDE drives.
POST_STATUS_CHECKSEG40G	92h	checking ROM BIOS data area again.
POST_STATUS_CHECKSEG40H	93h	checking ROM BIOS data area some more.
POST_STATUS_SETMEMSIZE	94h	setting base & ext mem sizes.
POST_STATUS_SIZEADJUST	95h	memsize adjusted for 1K, verifying disp mem.
Initialize any ROM BIOS extensions.		
POST_STATUS_INITBEFOREC8000	96h	initialization before calling C800h.
POST_STATUS_CALLC8000	97h	call ROM BIOS extension at C800h.
POST_STATUS_POSTC8000	98h	processing after extension returns.
Setup serial ports, parallel ports, NPX, keyboard, cache, wait states.		
POST_STATUS_TIMERPRNBASE	99h	configuring timer data area, printer base addr.
POST_STATUS_SERIALBASE	9ah	configuring serial port base addrs.
POST_STATUS_INITBEFORENPX	9bh	initialization before coprocessor test.
POST_STATUS_INITNPX	9ch	initializing the coprocessor.
POST_STATUS_POSTNPX	9dh	processing after coprocessor initialized.
POST_STATUS_CHECKLOCKS	9eh	check ext kbd, kbdID, numlock settings.
POST_STATUS_ISSUEKBDID	9fh	issue keyboard ID command next.
POST_STATUS_RESETID	0a0h	kbd ID flag reset.
POST_STATUS_TESTCACHE	0a1h	do cache memory test.
POST_STATUS_DISPSOFTERR	0a2h	display any soft errors.
POST_STATUS_TYPEMATIC	0a3h	set keyboard typematic rate.
POST_STATUS_MEMWAIT	0a4h	program memory wait states.
POST_STATUS_CLRSCR	0a5h	clear screen.
POST_STATUS_ENABPTYNMI	0a6h	enable parity and NMIs.
Initialize ROM BASIC if available.		
POST_STATUS_INITBEFOREE000	0a7h	initialization before calling E000h.
POST_STATUS_CALLE000	0a8h	call ROM BIOS extension at E000h.
POST_STATUS_POSTE000	0a9h	processing after extension returns.
Boot operating system.		
POST_STATUS_DISPCONFIG	0b0h	display system config box.
POST_STATUS_INT19BOOT	00h	call INT 19h bootstrap loader.
Additional paths.		
POST_STATUS_LOWMEMEXH	0b1h	test low memory exhaustively.
POST_STATUS_EXTMEMEXH	0b2h	test extended memory exhaustively.
POST_STATUS_PCIENUM	0b3h	enumerate PCI space.

7.2. Frequently Asked Questions

7.2.1. Operating System

Question 1: How can I install the operating system ?

Answer: When first running the PC without the operating system use the following steps:

1. Boot the computer with a MSDOS boot diskette
2. Set up the desired hard disk partitions with *fdisk*
3. Format the hard disk
4. Copy the installation files from the parallel port CDROM to the hard disk e.g. with: *xcopy32 source directory C:\target directory /E*
5. Run the SETUP program on the hard disk

to Point 1.)

When booting from diskette, you have to load the drivers for the CDROM connected to the parallel port. Therefore you have to do some entries in *autoexec.bat* / *config.sys*. The entries are dependent from the type of CDROM. Kontron Solutions delivers to different types of CDROMs:

a) Parallel port CDROM with IDE interface (Freecom):

entry in *autoexec.bat*: *A:\MSCDEX /D:FCCD001 /M:20 /L:D /V*

entry in *config.sys*: *LASTDRIVE=Z*

DEVICE=A:\POWER-CD.SYS /d:fccd001 /m:f8

b) Parallel port CDROM with SCSI interface (Trantor)

entry in *autoexec.bat*: *A:\MSCDEX.EXE /D:ASPICD0 /M:80 /L:D /V /E*

entry in *config.sys*: *LASTDRIVE=Z*

DEVICE=A:\MA358.SYS /m14

DEVICE=A:\ASPICD.SYS /D:ASPICD0

Special considerations for different operating systems:

a) Windows NT (4.0)

Before Win NT can be installed from hard disk, the hard disk have to be made bootable (command: *sys C:*).

By calling *WINNT /B /S:\source directory* WinNT can be installed without using the setup diskettes.

☝ It is recommended to install the actually Service Pack !

b) Win9x

(no particularities)

c) VxWorks

- VxWorks doesn't run on PCs with hard drives that have been previously organised as FAT32. → New organisation as FAT16 necessary !
- For the VxWorks operating system, the operating system files must be stored in consecutive clusters on the hard disk. Otherwise the system crashes! Therefore, a DOS defragmentation program, for instance, should be run after reinstalling the operating system.

Question 2: What is the reason for the following WinNT error message ?

"Setup has encountered a fatal error that prevents it from continuing. Contact your product support representative for assistance. The following status codes will assist them in diagnosing the problem: <0x4,0,0,0>

Setup cannot continue. Power down or reboot your computer now."

Answer: One possible reason is a boot sector virus (*ANTIEXE*, *Parity-Boot*, etc.) that can be removed using anti-virus programs, e.g. *MCAfee*.

7.2.2. Ethernet

Question 1: The **VisionCompact® IIa** network interface doesn't work with other computers although the network driver has been correctly installed.

Answer: There are a few possible reasons for this problem:

a) The "connector type" setting in the configuration program *setup.exe* doesn't match with the used interface. (look at chapter *4.5.2 Ethernet Drivers*).

b) If the **VisionCompact® IIa** is connected to a computer with a 10/100Mbit/s interface, it may be necessary to disable the automatic baud rate detection for this computer and select a baud rate of 10Mbit/s.

c) A **VisionCompact® IIa** with Windows 9x is connected to a network. However, when searching the network, no other computers were found. A work group different from the one used in the network may be specified in the "identification" menu panel (see "control panel" under "network").

d) Incorrectly physically connection:

When connecting only two computers in a network, check the following:

- 10Base-2: Terminators must be used on both ends of the BNC cable.
- 10Base-T: A crossover twisted pair cable must be used.

7.2.3. Connection of peripheral equipment

Question 1: Is it possible to connect a PS/2 mouse after booting the computer ?

Answer: A PS/2 mouse connected after booting will not work. If a PS/2 mouse is not connected to the computer when booting, the mouse cannot be initialized. The same is true for a PS/2 mouse that is disconnected during operation and then reconnected.

Question 2: Is it possible to connect a keyboard after booting the computer ?

Answer: Yes. The **VisionCompact® IIa** works in this case like a standard PC. Depending on the operating system, the keyboard is fully funcional or functions with the exception of special keys.

Operating system	Keyboard
DOS	OK without special keys
WIN9x	OK with special keys
WIN9x (DOS-Fenster)	OK without special keys
WINNT4.0	OK without special keys
WINNT4.0 (DOS-Fenster)	OK without special keys
OS/2	OK with special keys

8. Order Information

Type Codes, **VisionCompact® IIa**:

Type Code	Description
VC200-…	Compact PC VisionCompact IIa * Pentium II Processor * Fast access data memory: 256 KB SRAM * 1st field bus interface: CAN * Graphics with 2 MB image buffer * Ethernet: Coax + TP * Power supply: 24 VDC nominal voltage * Ambient temperature range, during operation: T_A=(0)5 ... 50° C * Processor, main memory and mass storage, 2nd field bus interface and case optional
VC220-…	Same as VC200, however, with on-board PC card drive (PCMCIA, type I+II), and on-board SCSI (requires case option „B“ with 2x PC/104-Plus)
	Processor
D	Pentium II @ 266MHz
E	Pentium II @ 300MHz
F	Pentium II @ 333MHz
G	Pentium II @ 366MHz
H	Pentium II @ 400MHz
	Main memory
2	32 MB
4	64 MB
6	128 MB
	Mass storage
A	HDD, small capacity (currently > 2 GB)
B	HDD, large capacity (currently > 3 GB)
Z	4 MB Silicon disk
X	20 MB Silicon disk
W	40 MB Silicon disk
V	80 MB Silicon disk
T	100 MB Silicon disk
S	220 MB Silicon disk
	2. Field Bus Interface
A	CAN (on-board controller)
B	Interbus-S master (IBS PC104 SC-T)

C	Profibus-DP master (CIF 104-DPM)
D	CAN, intelligent (CIF 104-CAN)
	Case
A	Standard case, 1 PC/104-Plus module (plug-in)
B	Case for 2 PC/104-Plus modules
	Power supply
A	24 VDC (18..36 V)
	Customer specific configurations
00	Standard configuration

Tools and Drivers	
Part # **Type Code**	**Description**
SP-VC2-0002 BSP/Win95/VC2	Board support package for Windows 95 on VisionCompact II * Supports VisionCompact hardware components: NMI timer, watchdog, fast access data memory, diagnostics LEDs, Ethernet, graphics, PC card, SCSI * drivers or sample programs * One-time license, incl. documentation * 3 months support via e-mail
SP-VC2-0003 NMI/WinNT4/VC2	Board support package for Windows NT 4.0 on VisionCompact II * Supports VisionCompact hardware components: NMI timer, watchdog, fast access data memory, diagnostics LEDs, Ethernet, graphics, PC card, SCSI * drivers or sample programs * One-time license, incl. documentation * 3 months support via e-mail
SP-VC2-0004 NMI/VxW/VC2	Board support package for VxWorks 5.3 on VisionCompact II * Supports VisionCompact hardware components: NMI timer, watchdog, fast access data memory, diagnostics LEDs, Ethernet, graphics, SCSI * drivers or sample programs * One-time license, incl. documentation * 3 months support via e-mail

Service, Diagnostics, and Assembly	
Part # **Type Code**	**Description**
EXFD AS-40 External floppy	External floppy disk drive for VisionCompact PCs * Incl. cable (approx. 1 m)
RTC-K-092 Y-Adapter	Keyboard/mouse adapter incl. cable (approx. 20 cm) * for standard MF2 keyboard and PS/2 mouse

Documentation	
Part # **Type Code**	**Description**
VC2a-UM User's Manual, German	VisionCompact IIa User's Manual * German * Hard copy
VC2a-UM/E User's Manual, English	VisionCompact IIa User's Manual * English * Hard copy
VC-UM-CD Documentation	Complete documentation for VisionCompact PCs on CD-ROM * German + English * .pdf format

9. Index

tbd.

10. Appendix

10.1. Literature

ISA Bus

[1] A.Stiller: c't 11/1991, Page 336ff "AT-Bus" (Introduction)
1991, Heise-Verlag

[2] A.Stiller: c't 12/1991, Page 313ff "AT-Bus-Timing"
1991, Heise-Verlag

[3] E.Solari: AT BUS Design IEEE P996 Compatible (Standard text)
Anabooks San Diego

[4] IEEE P996.1 /D1
October 1993

PC Hardware:

[5] H.-P.Messmer: PC-Hardwarebuch, Addison-Wesley

[6] Intel: Intel® 440BX AGPset

[7] Intel: Intel® 440BX AGPset: 82443BX Host Bridge/Controller

[8] Intel: 82371AB PCI-TO-ISA/DIE Xcelerator (PIIX4)

See the following sources for advanced information about the components used in the VisionCompact® IIa:

PC Programming:

[9] H.-P.Messmer: PC-Hardwarebuch, Addison-Wesley

[10] M.Tischer: PC-Intern
newest edition
Data Becker

VGA Programming:

[11] R.F.Ferraro: Programmer's Guide to the EGA und VGA Cards
1990, Addison-Wesley

[12] M.Tischer: PC-Intern, Data Becker

CAN Interface:

[13] H.-C. Reuss: Controller Area Network (CAN), A Powerful Solution for Fieldbus Applications; Appl. Note HKI/AN 92 001, Philips Semiconductor

[14] Philips: SJA1000, Stand-alone CAN-controller Data Sheet, 1996

[15] Philips: PCA82C250T, Preliminary Device Specification, 1992

Ethernet Interface:

[16] Crystal: CS8900 Ethernet Controller Developer`s Kit Version 1.0, August 1995

System Management Bus:

[17] Intel: 82371AB PCI-TO-ISA/IDE Xcelerator (PIIX4)

[18] National Semicond. LM75, Data Sheet, October 1997

[19] National Semicond. LM80, Data Sheet, February 1998

[20] XICOR X9221 Data Sheet, XICOR Data Book July 1995

10.2. Error Report

O Single Module **O** Software **O** System

Product_____

Serial No. or

System No._____

Company_____

Address _____

_____

_____

_____

Contact person_____

Telephone_____

To be completed by Kontron Solutions:

Date _____

R-No._____

Processed by:

O Production

O Development

O Sales

O Software

O Service

Product	:	**O**	Single Module	**O**	Software
		O	System	**O**	Documentation
Malfunction occurs	:	**O**	Sporadically	**O**	Regularly

Error description:_____

_____

_____

_____

_____

_____

_____

Please send this error description to:

Kontron Solutions GmbH

Department HE

Gutenbergstr. 15 * D-76437 Rastatt, Germany

Fax: 07222 / 1008-10 (in urgent cases)

10.3. Component Mounting Diagrams

10.3.1. VC3-CPU

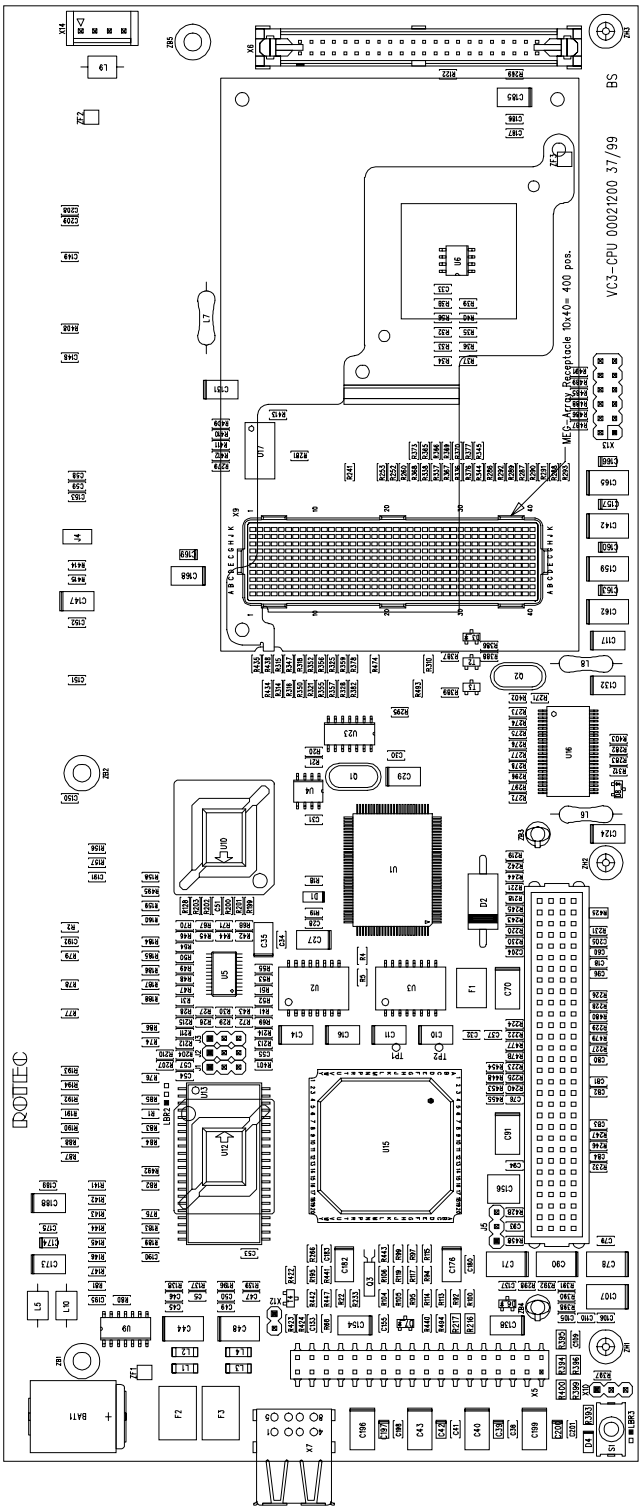


Figure 6: CPU Board Component Side

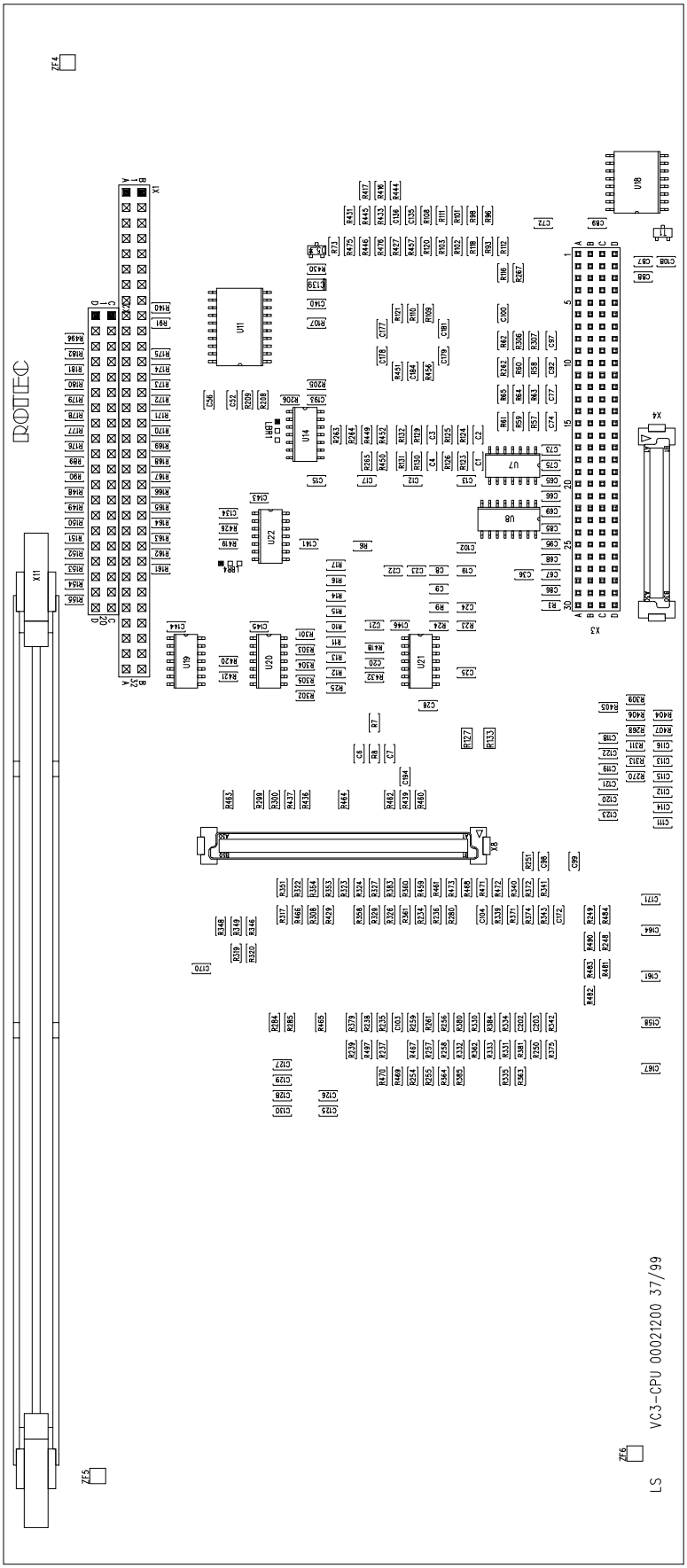


Figure 7: CPU Board Solder Side

10.3.2. VC2-I/O

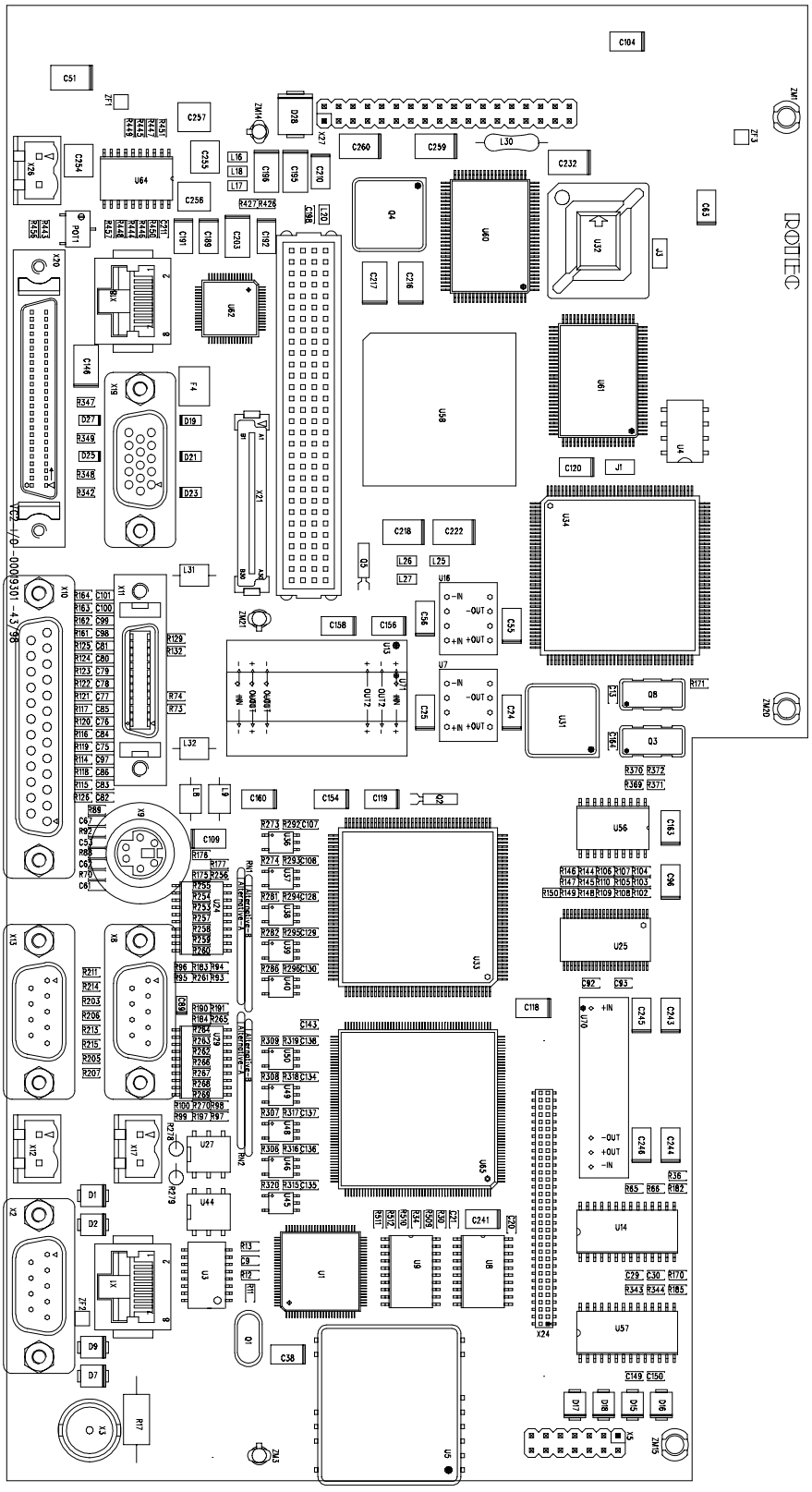


Figure 8: I/O Board Component Side

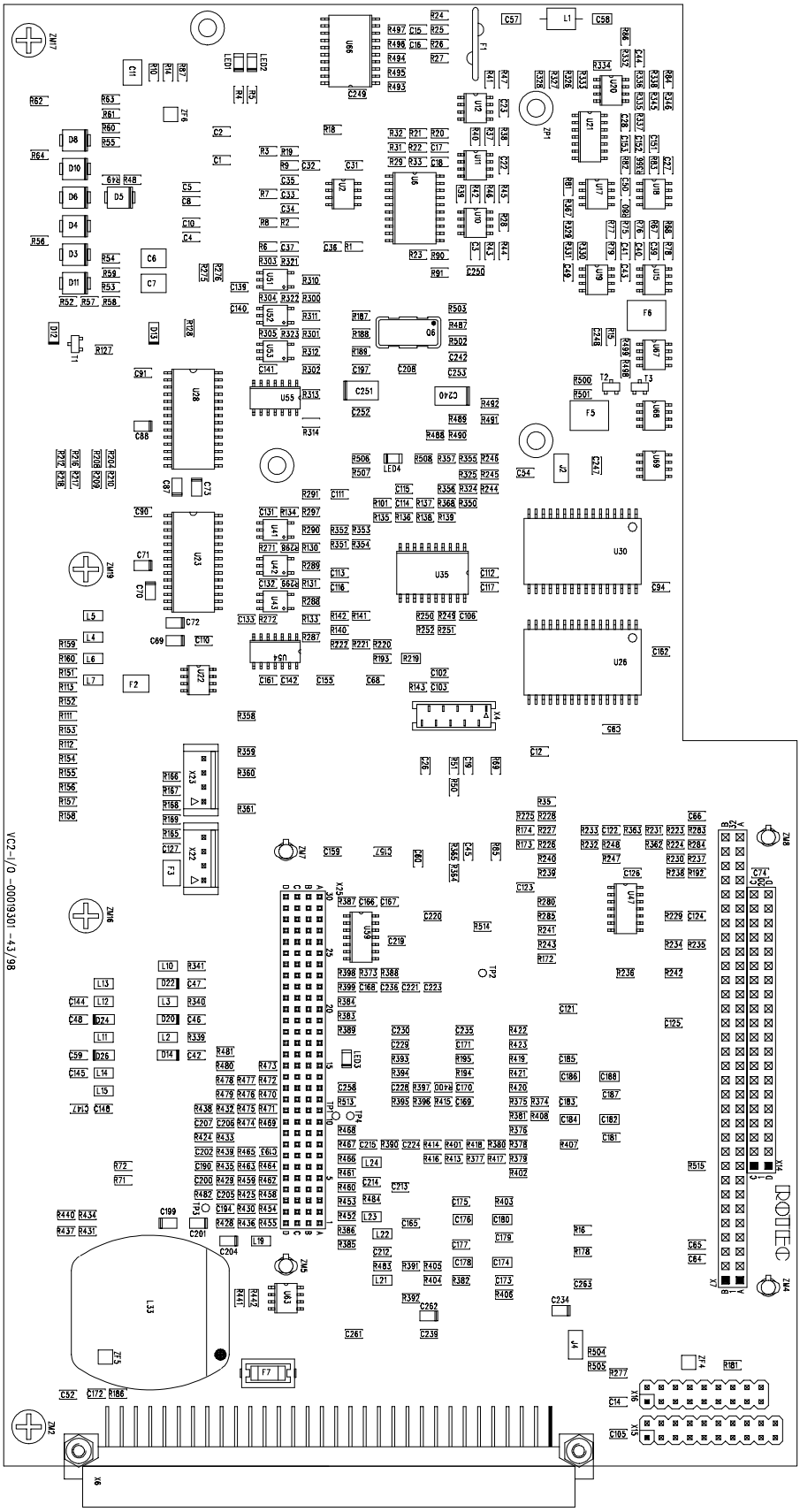


Figure 9: I/O Board Solder Side

10.3.3. VC3-PWR

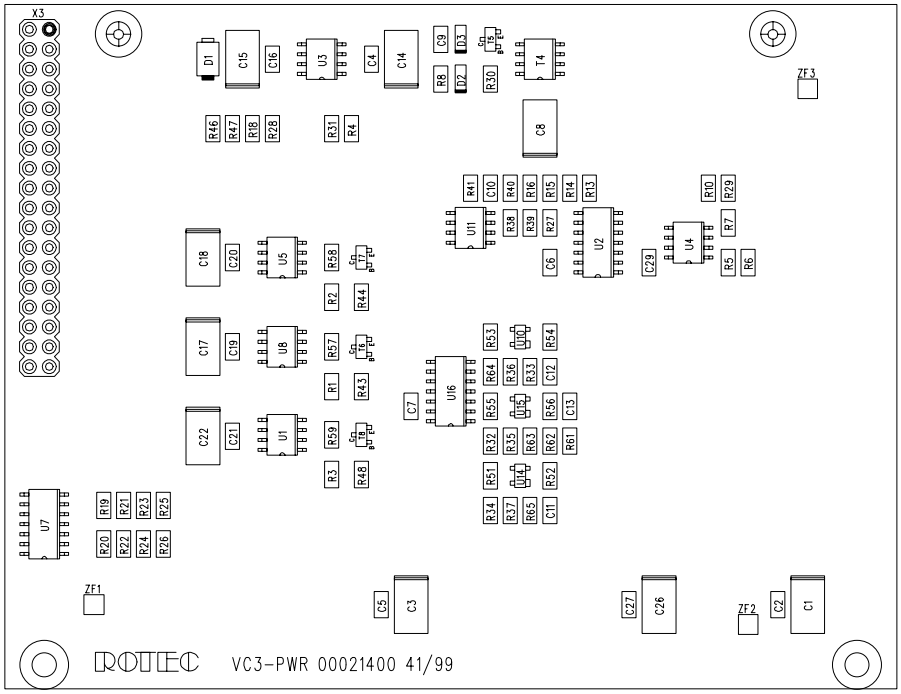


Figure 10: Power Board Component Side

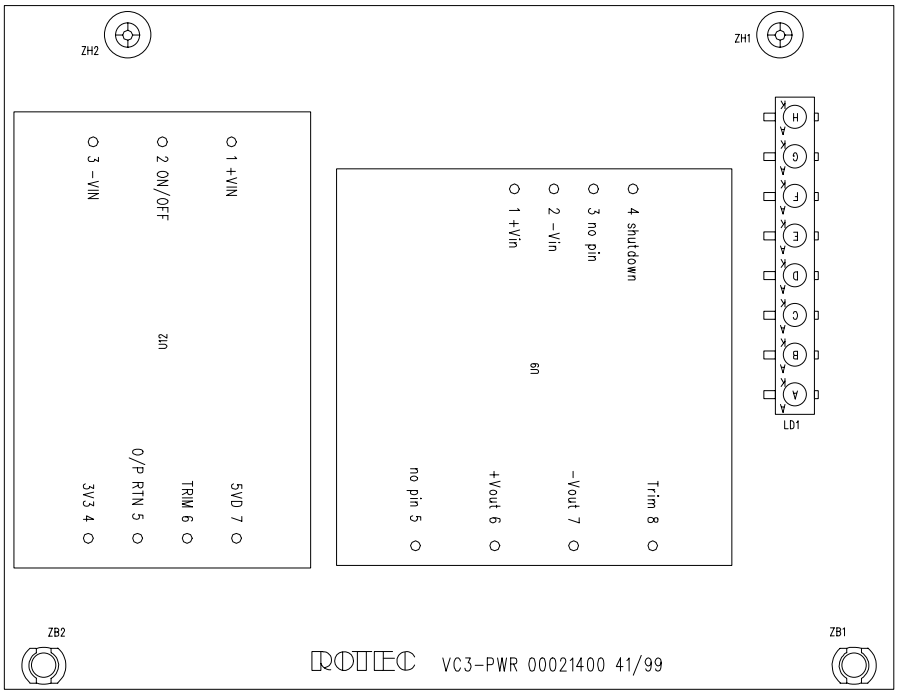


Figure 11: Power Board Solder Side