VIPer-825

Industrial PC – Pentium Based

Technical Reference Manual
Version 1.4, February 2003

Note: The latest releases of the Technical Reference Manuals are available at:
ftp://ftp.kontron.ca/support/Product_manuals/



www.kontron.com

Ref. : M825_TECH (Board Rev. 1)

FOREWORD

The information in this document is provided for reference purposes only. Kontron does not assume any liability for the application of information or the use of products described herein.

This document may contain information or refer to products protected by the copyrights or patents of others and does not convey any license under the patent rights of Kontron, nor the rights of others.

Printed in Canada.
Copyright 2003 by Kontron Inc., Boisbriand, Qc J7G 2A7.

DOCUMENTATION SURVEY

VIPer825 – Technical Reference Manual

Your comments are valuable for us and will contribute to improve the quality of this product by complementing and returning this form.

1. Overall rating of the Technical Reference Manual: ❑ Excellent ❑ Satisfactory ❑ Fair ❑ Poor
2. Was the information you were seeking easy to find? ❑ Yes ❑ No
   If no, can you comment? _____
3. What section of this manual do you refer to the most? _____
4. How can you rate this manual?
   In terms of clarity of information: ❑ Excellent ❑ Satisfactory ❑ Fair ❑ Poor
   Comments: _____
   _____
   In terms of complexity: ❑ Too technical ❑ Just OK ❑ Not technical enough
   Comments: _____
   _____
   In terms of classification of information: ❑ Excellent ❑ Satisfactory ❑ Fair ❑ Poor
   Comments: _____
   _____
5. Is there any missing information? ❑ Yes ❑ No
   If yes, what information is missing?_____
   _____
6. Is some information not properly or clearly explained? ❑ Yes ❑ No
   If yes, can you comment?_____
   _____
7. Additional comments (any changes or modifications to this manual): _____
   _____
   _____

Please send your comments to:

Kontron Inc
Technical Writing dept.
616 Curé Boivin, Boisbriand
(Québec) CANADA J7G 2A7

Name _____
Company _____
Address _____
_____
Optional

ADDITIONAL COMMENTS

FCC Compliance Statement

Warning

Changes or modifications to this unit not expressly approved by the party responsible for the compliance could void the user's authority to operate this equipment.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference, in which case the user will be required to correct the interference at his or her own expense.

European Statement

Warning

This is a class B product. If not installed in a properly shielded enclosure, and used in accordance with the instruction manual, this product may cause radio interference in which case the user may be required to take adequate measures at his or her own expense.

Safety Standard

UL Recognized Component, File # E186339 Vol. 1 Section 2

Care and handling precautions for Lithium batteries

- Do not short circuit
- Do not heat or incinerate
- Do not charge
- Do not deform or disassemble
- Do not apply solder directly
- Do not mix different types or partially used batteries together
- Always observe proper polarities

READ ME FIRST

EXERCISE CAUTION WHILE REPLACING LITHIUM BATTERY



WARNING

Danger of explosion if battery is incorrectly replaced.

Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.



ATTENTION

Il y a danger d’explosion s’il y a remplacement incorrect de la batterie.

Remplacer uniquement avec une batterie du même type ou d’un type équivalent recommandé par le constructeur. Mettre au rebut les batteries usagées conformément aux instructions du fabriquant.



ACHTUNG

Explosionsgefahr bei falschem Batteriewechsel.

Verwenden Sie nur die empfohlenen Batterietypen des Herstellers. Entsorgen Sie die verbrauchten Batterien laut Gebrauchsanweisung des Herstellers.



ATENCION

Puede explotar si la pila no este bien reemplazada.

Solo reemplazca la pila con tipas equivalentes segun las instrucciones del manifacturo. Vote las pilas usadas segun las instrucciones del manifacturo.

OTHER WARNINGS

Please heed the following warnings concerning the VIPer825 board:

PROCESSOR VOLTAGE

Faulty jumper settings on the Voltage Regulator Module will damage the processor. Please read pages 6-10 and 6-11 in the VIPer825 Technical Reference Manual carefully, if you need to install or replace the processor.

IMPORTANT INFORMATION

Before operating your Single Board Computer, please note the following:

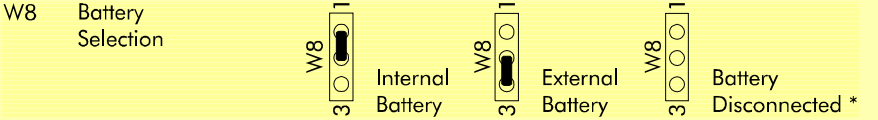
ADAPTER CABLES

When connecting Serial Ports, the use of Taiwanese adapter cables is not recommended, since the pinout is often incorrect. The direct crimp design offered allows the simplest cable assembly. All these cables are available by contacting the Sales department.

BATTERY CONFIGURATION

Your computer board is equipped with a standard non-rechargeable lithium battery. To preserve the useful life of the battery, **the W8 jumper, which enables the battery, is not installed when you receive the board**. If you need a jumper cap, we suggest you use the one on the Watchdog Timer jumper since it is rarely needed; if you wish to purchase jumper caps, you can contact our Sales department to order them.

Jumper settings for the W8 jumper appear below (* = initial setting):





POWERING UP THE SYSTEM

If you should encounter a problem, verify the following items:

- Make sure that all connectors are properly connected. On the standard flat ribbon cable used for the floppy connector, pin 1 is indicated by small red stripe. Verify that this red stripe is located on the appropriate side of the connector.
- Verify your boot diskette. It must be a system disk and it must be in proper working order.
- If the system still does not start up properly, you should try booting your system with only the power cord and video monitor connected to the board (this is the minimum required to see if the board is working).
- If you still are not able to start up your system, please refer to the Emergency Procedure in Appendix G.
- If you still are not able to get your board up and running, contact our Technical Support department for assistance.



PREVENTING VIRUSES

We take every precaution against computer viruses. For your protection, we have *safety sealed* all utility diskettes. If the seal is broken, **do not use the diskette**. Destroy the diskette immediately and contact our Technical Support department for further instructions at (450) 437-5682 (Canada) or at +49 811 / 600 15-0 (Germany).

To safeguard against computer viruses in general, do not freely lend your utility diskettes and regularly perform virus scans on all your computer systems.

UNPACKING AND SAFETY PRECAUTIONS

Static Electricity

Since static electricity can cause damage to electronic devices, the following precautions should be taken:

1. Keep the board in its anti-static package, until you are ready to install it.
2. Always touch a grounded surface or wear a grounding wrist strap before removing the board from its package; this will discharge any static electricity that may have built up in your body.
3. Handle the board by the edges.

Storage Environment

Electronic boards are sensitive devices. Do not handle or store devices near strong electrostatic, electromagnetic, magnetic or radioactive fields.

Power Supply

Before any installation or setup, ensure that the board is unplugged from power sources or subsystems.

Unpacking

Follow these recommendations while unpacking:

1. After opening the box, save it and the packing material for possible future shipment.
2. Remove the board from its anti-static wrapping and place it on a grounded surface.
3. Inspect the board for damage. If there is any damage or missing items, notify immediately.

When unpacking you will find:

1. One SBC.
2. One Quick Reference sheet
3. One CDROM containing drivers.

TABLE OF CONTENTS

PART 1 – PRODUCT DESCRIPTION

1. PRODUCT OVERVIEW 1-1

2. FEATURES 2-1

3. COMPATIBILITY WITH OUR SBC PRODUCTS 3-1

4. STATIC ELECTRICITY PRECAUTIONS 4-1

5. UNPACKING 5-1

6. QUICK INSTALLATION 6-1

6.1. INSTALLING SYSTEM MEMORY 6-1

6.1.1 72-Pin Sockets Location 6-1

6.1.2 Supported System Memory Configurations 6-2

6.1.3 SIMM Installation 6-2

6.2. SETTING JUMPERS 6-3

6.2.1 Connecting the Battery 6-3

6.2.2 Jumper Settings on the VIPer825 SBC 6-3

6.2.3 Jumper Settings on the Voltage Regulator Module 6-7

6.3. CONNECTING & POWERING UP THE BOARD 6-9

6.3.1 Installing VIPer825 Board in a System..... 6-9

6.3.2 Connecting a Floppy Disk.....6-10

6.3.3 Connecting Interface Devices (Keyboard, Speaker, Reset, LED).....6-12

6.3.4 Connecting a Mouse 6-14

6.3.5 Powering Up the System 6-15

6.3.6 Troubleshooting 6-16

7. INSTALLING & WORKING WITH SYSTEM COMPONENTS..... 7-1

7.1. INSTALLING PROCESSOR & FAN..... 7-1

7.1.1 Installing Processor..... 7-1

7.1.2 Fan Connectors..... 7-3

7.2. ENABLING CACHE MEMORY..... 7-3

7.3. ALLOCATING DMA CHANNELS..... 7-4

7.4. ALLOCATING IRQ LINES..... 7-5

7.5. INSTALLING SUPERVISOR UTILITIES..... 7-5

7.5.1 Power Fail Detection..... 7-5

7.5.2 Watchdog Timer..... 7-7

7.6. SYSTEM POWER MANAGEMENT 7-8

7.7. READING THE UNIQUE SERIAL NUMBER 7-8

8. INSTALLING STORAGE DEVICES 8-1

8.1. FLOPPY DEVICES 8-1

8.1.1 Floppy Connector 8-1

8.2. ENHANCED IDE DEVICES 8-2

8.2.1 EIDE Connector 8-2

8.3. COMPACTFLASH™ DISK 8-3

8.3.1 CompactFlash IDE Connector 8-4

8.3.2 Installing CompactFlash™ Disks on CompactFlash™ Module 8-5

8.3.3 Working with a COMPACTFLASH™ Disk 8-6

9. INSTALLING PERIPHERALS 9-1

9.1. SERIAL PORTS 9-1

9.1.1 Serial Port Connectors 9-1

9.2. PARALLEL PORT 9-6

9.2.1 Parallel Port Connector 9-6

9.2.2 Parallel Port Modes 9-7

10. SOFTWARE SETUP 10-1

10.1. THE AWARD SETUP PROGRAM 10-1

10.1.1 Accessing the AWARD Setup Program 10-1

10.1.2 Using AWARD Setup 10-2

10.1.3 Saving Configurations & Exiting AWARD Setup 10-4

10.1.4 Standard CMOS Setup 10-4

10.1.5 BIOS Features Setup 10-5

10.1.6 Chipset Features Setup 10-9

10.1.7 Power Management Setup 10-13

10.1.8 PnP/PCI Configuration 10-16

10.1.9 Integrated Peripherals 10-19

11. UPDATING OR RESTORING BIOS IN FLASH 11-1

11.1. USING THE UBIOS UTILITY TO UPDATE BIOS 11-1

11.1.1 Introduction 11-1

11.1.2 UBIOS - Interactive Mode 11-3

11.1.3 UBIOS – BATCH MODE 11-10

12. VT100 MODE 12-1

12.1. VT100 REQUIREMENTS 12-1

12.2. VT100 SETUP & CONFIGURATION 12-2

12.3. RUNNING WITHOUT A TERMINAL 12-2

PART 4 – APPENDICES

A. BOARD SPECIFICATIONS A-1

A.1 ELECTRICAL A-1
A.2 MECHANICAL A-1
A.3 ENVIRONMENTAL A-1
A.4 RELIABILITY A-1

B. BOARD DIAGRAMS B-1

B.1 VIPER825 BLOCK DIAGRAM B-1
B.2 VIPER825 ASSEMBLY DIAGRAM B-1
B.3 VIPER825 CONFIGURATION DIAGRAM B-3
B.4 VIPER825 MECHANICAL SPECIFICATIONS DIAGRAM B-5
B.5 VOLTAGE REGULATOR MODULE ASSEMBLY DIAGRAMS B-5
B.6 VOLTAGE REGULATOR MODULE MECHANICAL SPECIFICATIONS DIAGRAM . B-6

C. CONNECTOR LOCATION & PINOUTS C-1

C.1 LOCATION OF CONNECTORS ON THE VIPER825 & THE VOLTAGE REGULATOR MODULE C-1
C.2 CONNECTOR PINOUTS C-2

D. LIST OF APPROVED VENDORS D-1

D.1 RECOMMENDED DRAM DEVICES D-1
D.2 INTERFACE CONNECTORS D-2

E. MEMORY & I/O MAPS E-1

E.1 MEMORY MAP E-1
E.2 I/O MAP E-2

F. BIOS SETUP ERROR CODES F-1

F.1 POST MESSAGES F-1
F.2 POST BEEP F-1
F.3 ERROR MESSAGES F-2
F.4 POST CODES F-5

G. EMERGENCY PROCEDURE G-1

G.1 SYMPTOMS G-1
G.2 GENERATE AN EMERGENCY FLOPPY DISKETTE G-2
G.3 EMERGENCY PROCEDURE G-3

H. GETTING HELP H-1

PART 1

PRODUCT DESCRIPTION

1. PRODUCT OVERVIEW
2. FEATURES
3. COMPATIBILITY WITH OUR SBC PRODUCTS

1. PRODUCT OVERVIEW

The VIPer825 is a PC/AT industrial Single Board Computer (SBC) based on the Intel Pentium® (Socket 7) processor and the Intel 430HX chipset.

The VIPer825 is based on the half size PC/AT card format and can be installed into a standard passive ISA backplane. The SBC and backplane assembly is used as a substitute for the standard PC motherboard, and in general includes all of the standard interfaces and peripherals that are normally included in a top of the line PC. This compact solution allows an industrial user the possibililty of designing a system that uses standard x86 software and peripherals, but in an industrial environment where reliability, integration and service are of major concern.

The VIPer825 can also be used without a backplane, as a stand-alone computer: in such a case, it is powered through the external power connector and expansion is possible through the PC/104 and PC/104-*Plus* connectors.

2. FEATURES

The VIPer825 includes the following features:

- **Microprocessor Support:** The following processors are supported (maximum internal CPU clock speed indicated):
  - Intel Pentium®: 75, 90, 100, 120, 133, 150, 166, 200 and 233 MHz.
  - Intel Pentium® MMX: 150, 166, 200 and 233 MHz.
  - AMD K6: 166, 200 and 233 MHz.
- **External Cache:** Pipelined burst cache: 512 KB standard, 256 KB option.
- **System Memory:**
  - Two vertical 72-pin SIMM sockets support DRAM memory configurations from 8 to 256 MB.
  - Uses standard 5V, 70ns/60ns single-sided or double-sided 72-pin FPM or EDO SIMMs.
  - Supports 4MB, 8MB, 16MB, 32MB, 64MB and 128MB SIMM modules (32-bit and 36-bit).
- **CompactFlash Disk:** This module is a daughterboard with available capacities of 4, 10, 15, 30, 40 or 48 MB. It connects to the secondary IDE channel, is bootable and completely user upgradable (will support higher capacities when available).
- **Floppy Interface:** Supports two N82077 software compatible disks from 360KB to 2.88MB.
- **Enhanced IDE Interface:** Enhanced IDE controller can drive up to two enhanced IDE devices with transfer rates up to 22MB/s.
- **Bus Support:**
  - ISA Bus (IEEE P966 Specification).
  - PCI Local Bus Specification, Revision 2.1.
- **PC/104 and PC/104-*Plus* Connectors:** Allows peripheral expansion with a compact format. Both ISA and PCI-ISA modules are supported.
- **Serial Ports:** Supports two RS-232 serial ports, with RS-422/RS-485 available on Serial Port 2.
- **Parallel Port:** supports multiple modes (Standard, EPP and ECP).
- **Operating Systems:** Supports all operating systems developed for x86 and Pentium processors: PC and MS-DOS™, Windows® 3.X, Windows® 95, Windows® 98, Windows® NT, OS/2® Warp, SCO UNIX™, QNX™, and NOVELL™.

- **Boot Block Flash BIOS:** 256KB device contains all the board's BIOS, and is used for nonvolatile configuration storage required for the Plug and Play BIOS. Protected boot block section allows for reprogramming of BIOS, even in the case of an inadvertent corruption of the Flash contents.
- **BIOS** License**:** AWARD CPU BIOS.

3. COMPATIBILITY WITH OUR SBC PRODUCTS

The VIPer825 board is a low-cost version of the VIPer821 industrial single board computer. Compared to the VIPer821, the VIPer825 does not have onboard video, Ethernet, USB and the 4KB user serial EEPROM device. Added features for the VIPer825 are direct connection to the parallel port and the serial port 1 on the board's bracket, and the PC/104-*Plus* connector.

PART 2

CONNECTING & INSTALLATION

4. STATIC ELECTRICITY PRECAUTIONS
5. UNPACKING
6. QUICK INSTALLATION
7. INSTALLING & WORKING WITH SYSTEM COMPONENTS
8. INSTALLING STORAGE DEVICES
9. INSTALLING PERIPHERALS

4. STATIC ELECTRICITY PRECAUTIONS

Since static electricity can damage a board, the following precautions should be taken whenever you handle the VIPer825:

- Keep the board in its antistatic package, until you are ready to install it.
- Touch a grounded surface before removing the board from its package or wear a grounding wrist strap; this will discharge any static electricity that may have built up on your body.
- Handle the board by the edges.

5. UNPACKING

Follow these recommendations while unpacking:

- Observe the Static Electricity Precautions (Section 4).
- After opening the box, save it and the packing material for possible future shipment.
- Remove the board from its antistatic wrapping and place it on a grounded surface.

Inspect the board for damage. If there is any damage, or items are missing, notify immediately.

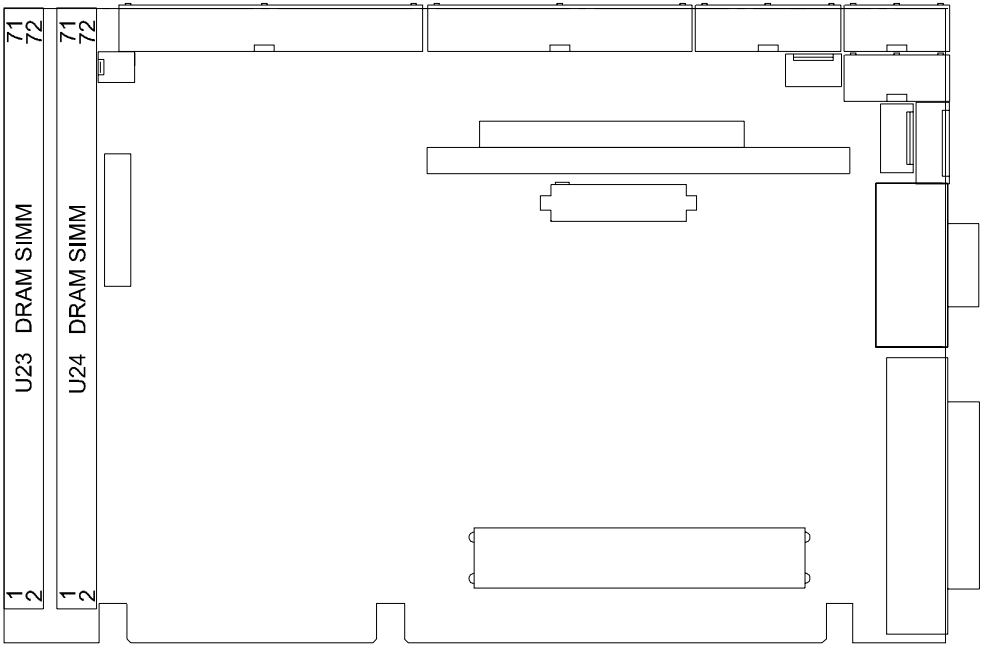
6. QUICK INSTALLATION

6.1. INSTALLING SYSTEM MEMORY

6.1.1 72-Pin Sockets Location

The location of the two 72-pin vertical SIMM (Single In-line Memory Module) sockets appears on Diagram 6-1 and they are labeled U23 and U24.

DIAGRAM 6-1: SIMM Sockets Location



6.1.2 Supported System Memory Configurations

At least 8MB of system memory must be installed on the VIPer825 for proper operation. System Memory can be configured from 8 to 256 MB. SIMM modules must be installed in both sockets (U23 and U24) and must be of the same capacity. The following SIMM modules are supported: 4MB (1Mx32/36), 8MB (2Mx32/36), 16MB (4Mx32/36), 32MB (8Mx32/36), 64MB (16Mx32/36) and 128MB (32Mx32/36).

The VIPer825 supports the following:

- Standard 5V, 70ns/60ns single-sided or double-sided SIMMs.
- 32-bit and 36-bit SIMMs.
- Fast Page Mode (FPM) and Extended Data Out (EDO) SIMMs.
- Error Checking and Correction (ECC) or parity bit with 36-bit SIMMs.

TABLE 6-1: VIPer825 System Memory Configuration: 8MB - 256MB

SYSTEM MEMORY	U23	U24
8MB	4MB (1Mx32/36)	4MB (1Mx32/36)
16MB	8MB (2Mx32/36)	8MB (2Mx32/36)
32MB	16MB (4Mx32/36)	16MB (4Mx32/36)
64MB	32MB (8Mx32/36)	32MB (8Mx32/36)
128MB	64MB (16Mx32/36)	64MB (16Mx32/36)
256MB	128MB (32Mx32/36)	128MB (32Mx32/36)

6.1.3 SIMM Installation

When you are ready to install the SIMMs in the sockets, follow the steps outlined below:

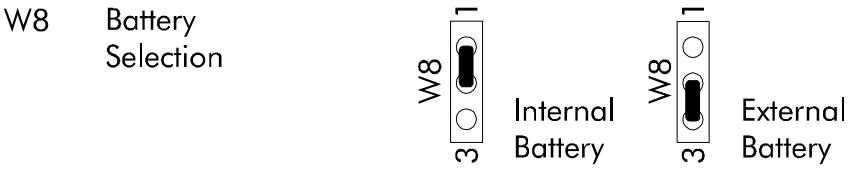
- With the board flat on the table, turn it so that the sockets are at the end of the board farthest from you.
- Hold the module with the notch on the bottom left facing you, and insert the connector into the socket at a 70º angle from the board. Always start inserting the module in the socket nearest the center of the board. Then insert the other module near the edge of the board.
- Snap the modules to a vertical position in the socket. The module is fully inserted when the retaining pegs snap into the holes at each end of the module.

To remove the SIMMs from the sockets, pull on the retaining pegs situated on each side of the SIMM socket. Once the module has snapped out of the socket, pull gently on it.

6.2. SETTING JUMPERS

6.2.1 Connecting the Battery

To enable the internal battery, you must short pins 1 and 2 on jumper W8. An external battery may be used. In such a case, pins 2 and 3 of jumper W8 should be shorted.



NOTE

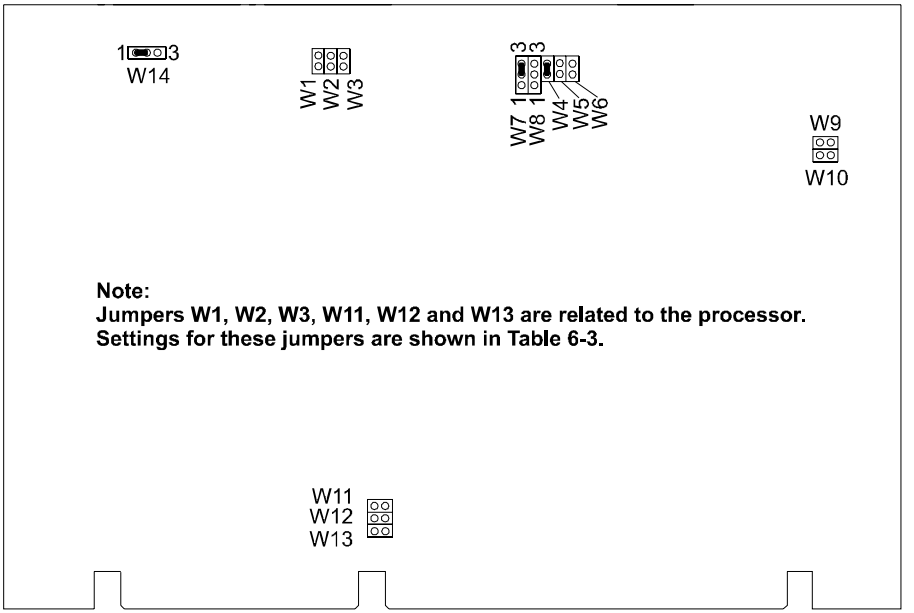
Removing the W8 jumper has the same effect as putting the battery in storage; the board is always shipped with the battery jumper removed in order to increase the life of the battery.

6.2.2 Jumper Settings on the VIPer825 SBC

Diagram 6-2 shows the jumper locations on the VIPer825 board. The jumpers appear as rectangular boxes containing small circles which represent the pins. Pins on the ends or corners are numbered on the diagram.

The jumpers are shown with default settings (the black strips over the pins indicate that those pins are shorted by jumper caps).

DIAGRAM 6-2: Jumper Locations With Default Settings



Tables 6-3 and 6-4 on the following pages show all jumper settings (default settings are indicated with an *).

Note that the jumpers on the TEK-067 power supply daughterboard are shown in Section 6.2.3.

TABLE 6-2: Jumper Settings: W1-W3, W11-W13

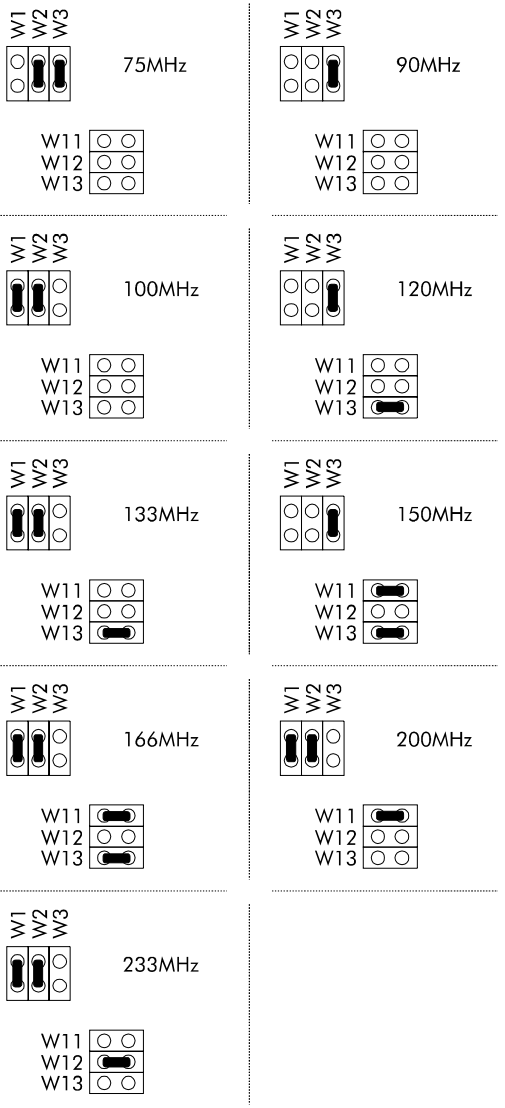
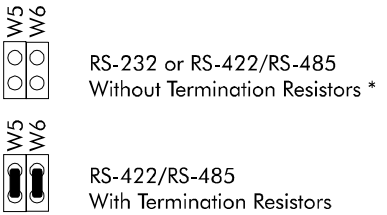
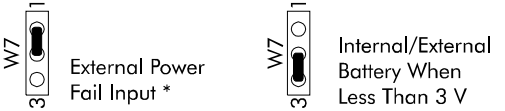
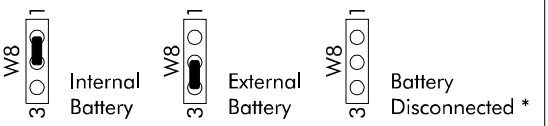
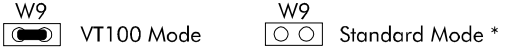
NAME	FUNCTION	CONFIGURATION (INITIAL SETTING: *)
W1 W2 W3 W11 W12 W13	Internal CPU Clock Speed	

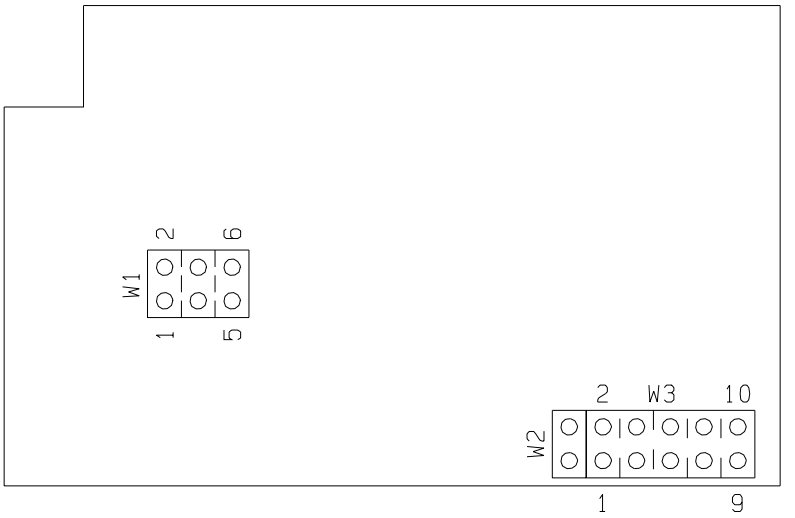
TABLE 6-3: Jumper Settings: W4-W10, 14

NAME	FUNCTION	CONFIGURATION (INITIAL SETTING: *)
W4	Watchdog Timer	
W5 W6	Serial Port 2 Termination Resistors	
W7	Power Fail Detection Source	
W8	Battery Selection	
W9	VT100 Mode	
W10	Non Maskable Interrupt on Power Fail Output	
W14	Voltage Selection For CPU Fan Connector	

6.2.3 Jumper Settings on the Voltage Regulator Module

The Voltage Regulator Module, which is installed on the VIPer825's P3 connector, has three jumpers (W1,W2 and W3) for setting the processor voltage.

DIAGRAM 6-3: Voltage Regulator Module Jumpers



These jumpers are very important and must be carefully configured. If you ordered your VIPer825 with a processor on board, then the Voltage Regulator Module jumpers will already be set. Do not modify these settings!

WARNING

Processor voltage must be configured as specified by processor manufacturer, otherwise damage to the processor can result.

See Table 6-6 for jumper settings.

Single-voltage Pentium processors must be set for 3.3 V only. In the case of split-core technology (Pentium MMX or K6), you must select the right core voltage for your particular processor. For example, Pentium MMX processors running at 166MHz, 200MHz and 233MHz require 2.8 V core voltage. Be sure you know the specified core voltage for your processor when it is a split-core technology!

TABLE 6-4: Voltage Regulator Module Jumper Settings: W1 - W3

Processor	W1	W2	W3					Comments
			1-2	3-4	5-6	7-8	9-10	
Pentium-100	1-3, 2-4	IN	IN	OUT	IN	IN	OUT	
Pentium-120	1-3, 2-4	IN	IN	OUT	IN	IN	OUT	
Pentium-133	1-3, 2-4	IN	IN	OUT	IN	IN	OUT	Single plane
Pentium-150	1-3, 2-4	IN	IN	OUT	IN	IN	OUT	Vcore=Vio=3.3V
Pentium-166	1-3, 2-4	IN	IN	OUT	IN	IN	OUT	
Pentium-200	1-3, 2-4	IN	IN	OUT	IN	IN	OUT	
MMX-166	3-5, 4-6	OUT	OUT	OUT	OUT	IN	OUT	Split plane
MMX-200	3-5, 4-6	OUT	OUT	OUT	OUT	IN	OUT	Vcore=2.8V, Vio=3.3V
MMX-233	3-5, 4-6	OUT	OUT	OUT	OUT	IN	OUT	
K6-166	3-5, 4-6	OUT	IN	OUT	OUT	IN	OUT	Split plane
K6-200	3-5, 4-6	OUT	IN	OUT	OUT	IN	OUT	Vcore=2.9V, Vio=3.3V
K6-233	3-5, 4-6	OUT	OUT	OUT	IN	IN	OUT	Split plane Vcore=3.2V, Vio=3.3V

6.3. CONNECTING & POWERING UP THE BOARD

6.3.1 Installing VIPer825 Board in a System

The VIPer825 is fully IBM AT compatible and, as such, can be installed on any standard ISA passive backplane. The available slots on the backplane will then provide the possibility of expansion through add-on cards.

Since the VIPer825 also has power connectors for an external power supply, it can also be used as part of a stand-alone system. The board's PC/104 and PC/104-*Plus* connectors will then provide any needed expansion through stackable PC/104 and PC/104-*Plus* mezzanine cards.

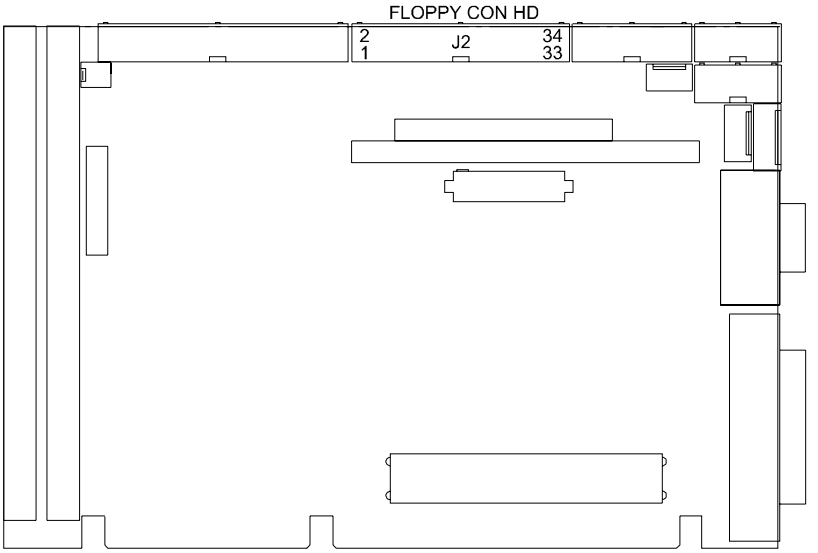
Mounting holes on the VIPer825 are plated and connected to the VIPer board's chassis ground. If you need to isolate the board, insert plastic washers (or washers made with some other electrically isolating material) between the screws and the mounting holes.

The VIPer825 can also operate without any mechanical drives by performing disk operations on solid-state disks (user CompactFlash disk). A CompactFlash disk is a read/write disk that can be accessed via the MS-DOS commands.

6.3.2 Connecting a Floppy Disk

The Floppy connector appears on Diagram 6-4 at J2.

DIAGRAM 6-4: Floppy Connector Location



The installation of the floppy drives is done via a standard IBM 34-pin flat ribbon cable that connects to J2.

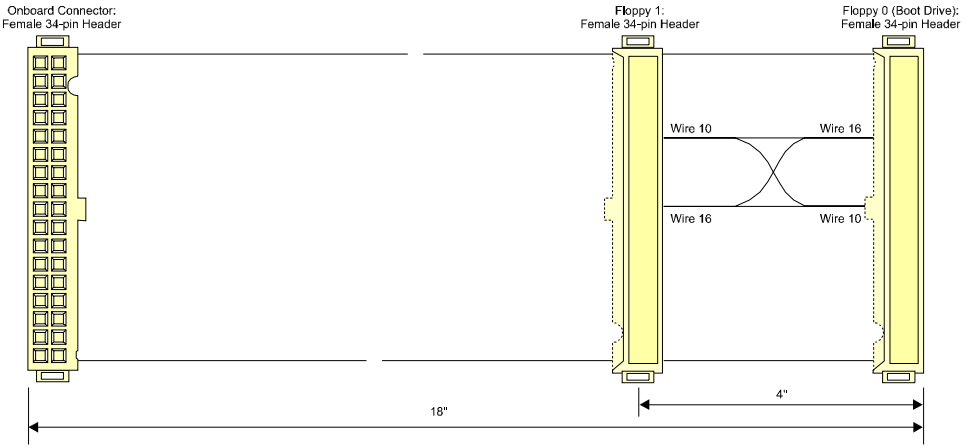
An 18” floppy disk cable is available and referred to as part number 150-051.

You may want to create your own cable. The following list includes approved vendors for the J2 connector’s mating parts:

Amp 746285-8 [optional strain relief: 499252-6],
Robinson Nugent IDS-C34PK-TG,
Thomas & Betts 622-3430 [optional strain relief: 622-3441].
(34-pin flat cable connector).

Diagram 6-5 shows a floppy disk cable with Floppy 1 and Floppy 0 mating connectors. Note those Wires 10 to 16 are twisted between the Floppy 1 and Floppy 0 connectors.

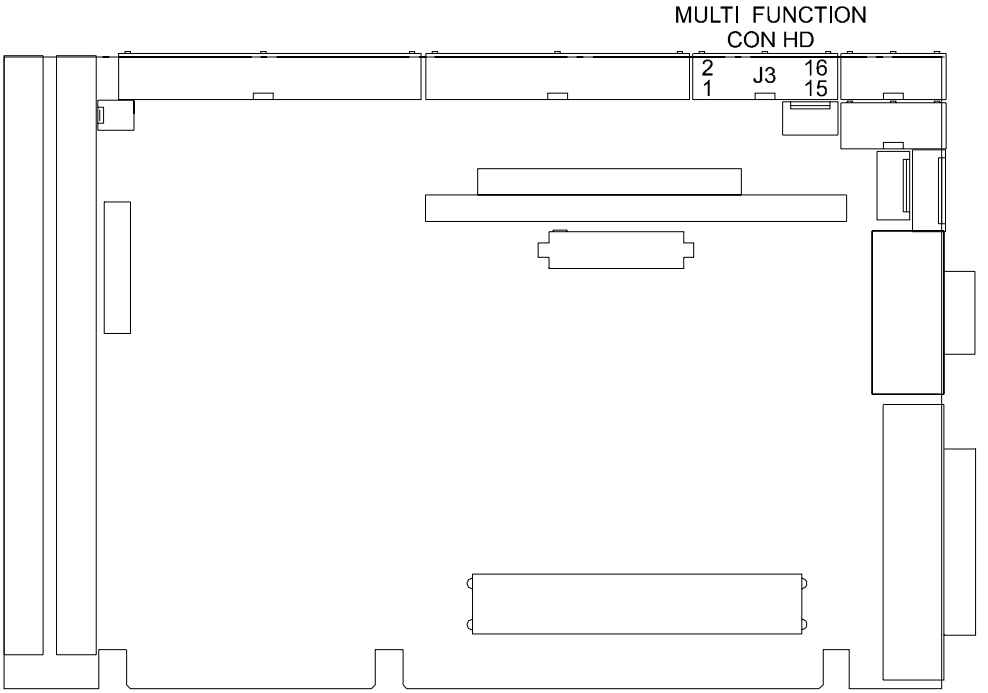
DIAGRAM 6-5: Floppy Disk Cable



6.3.3 Connecting Interface Devices (Keyboard, Speaker, Reset, LED)

Connector J3 provides all the necessary signals for connecting the keyboard, speaker, reset, and keylock interface devices. The Multi Function connector appears on Diagram 6-6 at J3.

DIAGRAM 6-6: Multi Function Connector Location



The cable used for connecting the interface device is the 22" keyboard cable: our part number 150-018-01.

Though we supply a cable for the J3 connector, you can build your own. The following list includes approved vendors for the J3 connector's mating parts:

Amp 746285-3 [optional strain relief: 499252-8],
Robinson Nugent IDS-C16PK-TG,
Thomas & Betts 622-1630 [optional strain relief: 622-1641].
(16-pin flat cable connector).

The following functions are available on the J3 connector:

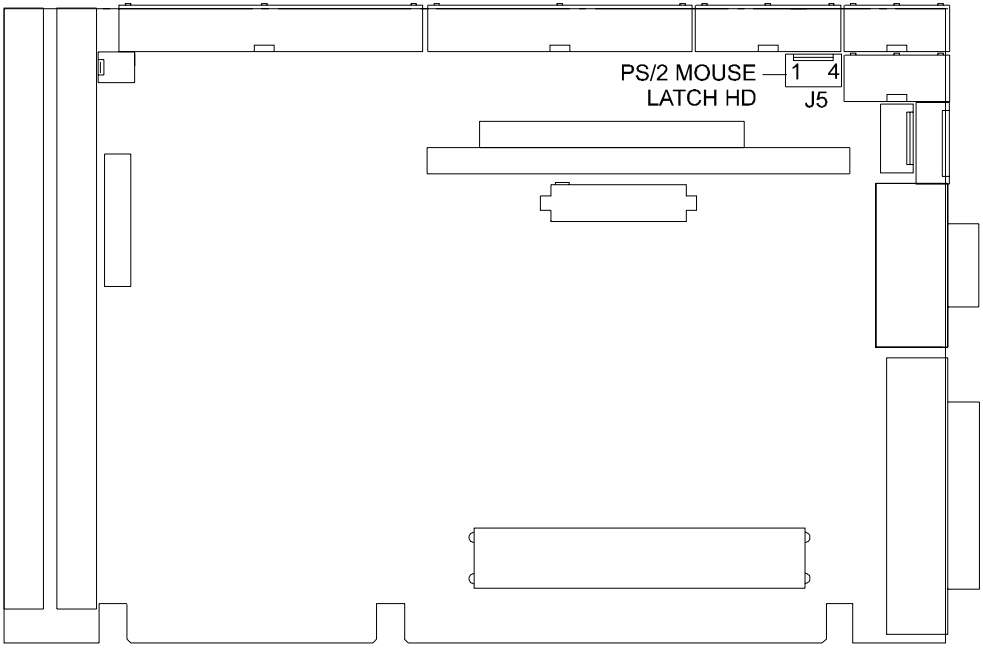
• Standard AT Keyboard:	Use the keyboard DIN connector on the keyboard cable: part number 150-018-01.
• Speaker:	An 8-ohm speaker can be directly connected to pins 7 and 8 of J3. All necessary drivers are on the board.
• Keyboard Disable:	The keyboard can be disabled or locked up by shorting pins 9 and 10 of J3.
• Hard Disk LED:	The onboard IDE interface activates an external LED. The LED must be connected, anode on pin 16 (J3) and cathode on pin 15 (J3). No external current limiting resistor is required since one is already present on the board.
• Push Button Reset:	Short pin 13 and pin 14 to reset the computer board.

6.3.4 Connecting a Mouse

The board supports a mouse, through the PS/2 connector at J5. With the PS/2 Mouse Cable (available and referred to as part number 150-337-00), this feature is compatible with the standard IBM PS/2 mouse. The cable may be ordered by contacting our Sales department.

The Mouse connector appears on Diagram 6-7 at J5.

DIAGRAM 6-7: Mouse Connector Location



You may want to create your own cable for the mouse header. The following list includes approved vendors for the J5 connector's mating parts:

Molex 22-01-3047 (connector),
Molex 08-50-0114 (crimp).

6.3.5 Powering Up the System

6.3.5.1. Power Sources for the VIPer825

The VIPer825 Single Board Computer is powered via the ISA bus when it is installed on a passive backplane or via the VIPer825's external power connector(s).

The external power connectors are:

J8 - Power A Connector: for +5V, +12V, -12V and Ground.

J9 - Power B Connector: for +5V and Ground.

Power B is a +5V supply input to be used when Power A supply is not enough (for example, when using PC/104 modules or processors with higher current requirements, such as the Pentium MMX or K6).

Power A and Power B Connector pinouts are given in Appendix C.

> **NOTE**
>
> When connecting external power to boards with a Pentium MMX or an AMD K6 processor, both the J8 Power A connector and the extra J9 Power B connector need to be used because of higher current requirements.

6.3.5.2. Power Up Procedure

You are now ready to power up your system.

1. Insert a bootable diskette in drive A to start your system with DOS.
2. Hit the DELETE key before or when this message appears near the bottom of the screen: ″Press **DEL** to enter SETUP″. This will bring you to the Main Menu of the AWARD BIOS CMOS Setup Utility. Use the arrow keys to select among the items and press ENTER to accept.
   - Select ″STANDARD CMOS SETUP″ to set the date and time.
     More detail on the AWARD Setup is given in Section 10.1 of this manual.
   - Select ″LOAD SETUP DEFAULTS″ to reset the setup.
   - Select ″SAVE & EXIT SETUP″ to continue the boot procedure.
3. Once the boot procedure is completed, reboot the system to make sure everything works properly.

6.3.6 Troubleshooting

If you should encounter a problem, verify the following items:

- Make sure that all connectors are connected properly. On the standard flat ribbon cable used for the floppy connector, pin 1 is indicated by small red stripe. Verify that this red stripe is located on the appropriate side of the connector.
- Verify your boot diskette. It must be a system disk and it must be in proper working order.
- If the system still does not start up properly, you should try booting your system with only the power cord and video monitor connected to the board (this is the minimum required to see if the board is working).
- If you still are not able to start up your system, please refer to the Emergency Procedure in Appendix G.
- If you still are not able to get your board up and running, contact our Technical Support department for assistance.

7. INSTALLING & WORKING WITH SYSTEM COMPONENTS

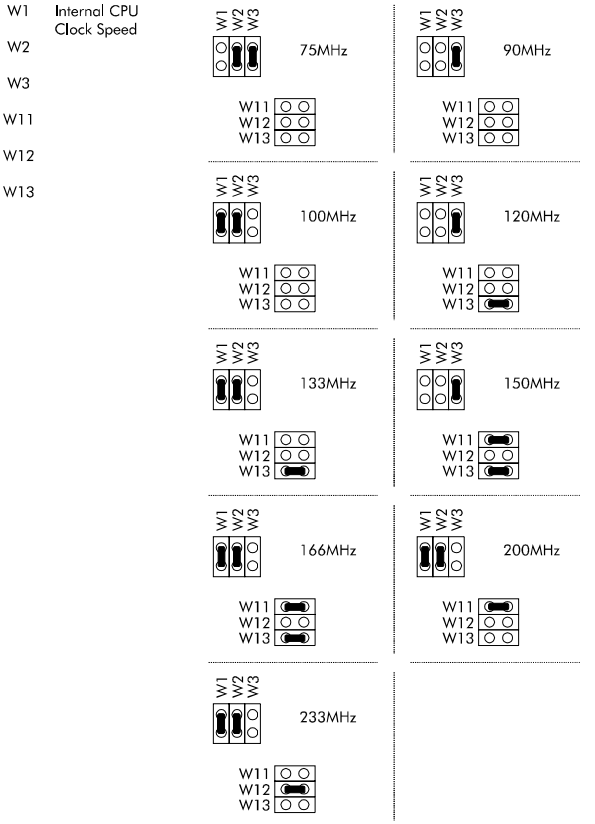
7.1. INSTALLING PROCESSOR & FAN

Normally, your VIPer825 will be ordered with one of the available processors and a cooling system. However, it may be necessary to reinstall or reconfigure these components.

7.1.1 Installing Processor

The following jumpers on the VIPer825 board are related to the processor: W1, W2, W3, W11, W12 and W13. They are configured together depending on the internal processor clock speed, as shown on Diagram 7-1.

DIAGRAM 7-1: Processor Related Jumpers on the VIPer825



The Voltage Regulator Module that is installed on the VIPer825's P3 connector has three jumpers (W1,W2 and W3) for setting the CPU voltage.

These jumpers are very important and must be carefully configured. If you ordered your VIPer825 with a processor on board, then the Voltage Regulator Module jumpers will already be set. Do not modify these settings!

See Table 7-1 for jumper settings.

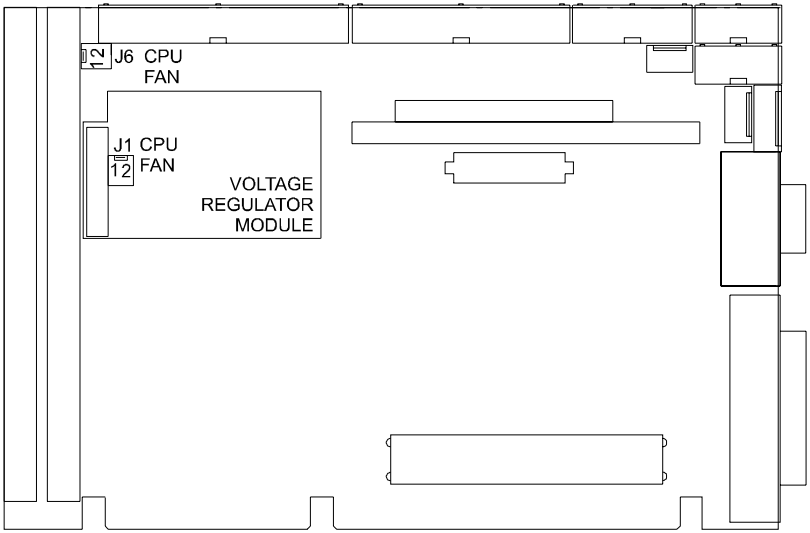
TABLE 7-1: Voltage Regulator Module Jumper Settings: W1 - W3

Processor	W1	W2	W3					Comments
			1-2	3-4	5-6	7-8	9-10	
Pentium-100	1-3, 2-4	IN	IN	OUT	IN	IN	OUT	Single plane Vcore=Vio=3.3V
Pentium-120	1-3, 2-4	IN	IN	OUT	IN	IN	OUT	
Pentium-133	1-3, 2-4	IN	IN	OUT	IN	IN	OUT	
Pentium-150	1-3, 2-4	IN	IN	OUT	IN	IN	OUT	
Pentium-166	1-3, 2-4	IN	IN	OUT	IN	IN	OUT	
Pentium-200	1-3, 2-4	IN	IN	OUT	IN	IN	OUT	
MMX-166	3-5, 4-6	OUT	OUT	OUT	OUT	IN	OUT	Split plane Vcore=2.8V, Vio=3.3V
MMX-200	3-5, 4-6	OUT	OUT	OUT	OUT	IN	OUT	
MMX-233	3-5, 4-6	OUT	OUT	OUT	OUT	IN	OUT	
K6-166	3-5, 4-6	OUT	IN	OUT	OUT	IN	OUT	Split plane Vcore=2.9V, Vio=3.3V
K6-200	3-5, 4-6	OUT	IN	OUT	OUT	IN	OUT	
K6-233	3-5, 4-6	OUT	OUT	OUT	IN	IN	OUT	Split plane Vcore=3.2V, Vio=3.3V

7.1.2 Fan Connectors

For a +12V fan, use the VIPer825 J6 connector (with the W14:1-2 jumper installed). For a +5V fan, use the VIPer825 J6 connector (with W14:2-3 jumper installed) or the J1 connector on the Voltage Regulator Module (VRM). Both connectors appear on Diagram 7-2.

DIAGRAM 7-2: VIPer825 J6 Fan Connector & VRM J1 Fan Connector



The following list includes approved vendors for the fan connector's mating parts:

Leoco 2530 S020013 (housing),
Leoco 2533 TCB00A0 (crimp);

Molex 22-01-3027 (housing),
Molex 08-50-0114 (crimp).

7.2. ENABLING CACHE MEMORY

There are two separate caches in the host subsystem: internal cache and external cache. The cache inside the processor (internal cache) is referred to as the first level cache (also primary cache). The external cache (called system cache in this manual) comprises the System Controller's cache control circuitry and associated external memory array; it is referred to as the second level cache (also secondary cache). The second level cache is unified, which means that both processor data and instructions are stored in the cache.

System cache is enabled and configured in the AWARD Setup program.

7.3. ALLOCATING DMA CHANNELS

The VIPer825 integrates the functionality of two 8237 DMA controllers. Eight DMA channels are available.

According to Plug and Play standards, the system BIOS automatically allocates DMA Channel 1 or 3 for the parallel port's ECP mode. Channel 2 is reserved for the floppy controller and Channel 4 is used to cascade Channels 0 through 7 to the processor.

TABLE 7-2: DMA Channels

DMA Channel	Function
DMA 0	Available
DMA 1	PnP available (ECP)
DMA 2	Floppy controller
DMA 3	PnP available (ECP)
DMA 4	Cascade controller # 1
DMA 5	PnP available
DMA 6	PnP available
DMA 7	PnP available

7.4. ALLOCATING IRQ LINES

TABLE 7-3: IRQ Lines

Controller # 1		Controller # 2	
IRQ 0	Timer 0	IRQ 8	Real-time clock
IRQ 1	Keyboard	IRQ 9	Available [1]
IRQ 2	Cascade controller # 2	IRQ 10	Available [1]
IRQ 3	COM 2 *	IRQ 11	Available [1]
IRQ 4	COM 1 *	IRQ 12	PS/2 Mouse Interface
IRQ 5	LPT2 * or available [1]	IRQ 13	Coprocessor Error
IRQ 6	Floppy controller *	IRQ 14	Primary IDE * or available [1]
IRQ 7	LPT1 * or available [1]	IRQ 15	Secondary IDE * or available [1]

* All functions marked with an asterisk (*) can be disabled or reconfigured.
[1] Available lines service on board and external PCI/ISA PnP devices or a Legacy ISA device.

7.5. INSTALLING SUPERVISOR UTILITIES

7.5.1 Power Fail Detection

The power fail circuit can be used to determine if a voltage crosses a pre-determined threshold. The output of the power fail circuit can be connected to the IOCHK* line to generate a non-maskable interrupt (NMI) when the monitored voltage crosses this threshold.

Power fail monitoring is enabled by shorting the W10 jumper.

The power failure detector, which generates a NMI when a failure occurs, provides a 1.25V threshold for DC power fail warning when the system monitors:

- Low-battery detection, or
- A power supply other than +5V DC.

There are three ways to set the Power Fail and Battery circuit:

- **Using Internal Battery & Monitoring External Source:**
  Internal Battery (set by W8 jumper with pins 1-2 shorted) and External Power Fail Input (set by W7 jumper with pins 1-2 shorted).

  The power detection input can only accept DC voltage. The line is monitored via a resistor network made up of a user-defined resistor (R24) and a fixed 1KΩ resistor connected to GND. The junction of these two resistors is connected to the input of the power fail circuit, which has its threshold set to 1.25V. R24 can be calculated as follows:

  $$R24 = 1K\Omega \frac{(VI-1.25)}{1.25}$$ where VI is input voltage

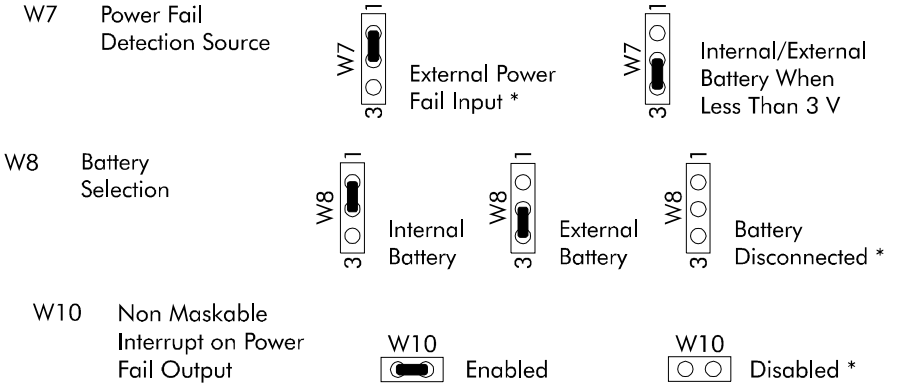
- **Using Internal Battery & Monitoring Internal Battery:**
  Internal Battery (set by W8 jumper with pins 1-2 shorted) and Power fail detect when battery is less than 3V (set by W7 jumper with pins 2- 3 shorted).

  When the internal battery is selected as being the source of the power fail circuit, it is set to trip when the battery goes lower that 3V.

- **Using External Battery & Monitoring External Battery:**
  External Battery (set by W8 jumper with pins 2-3 shorted) and Power fail detect when battery is less than 3V (set by W7 jumper with pins 2-3 shorted).

  When the external battery is selected as being the source of the power fail circuit, it is set to trip when the battery drops below 3V.

Related jumpers appear below (* = initial setting).



7.5.2 Watchdog Timer

The Watchdog Timer is extremely useful in embedded systems where human supervision is not required.

Jumper W4 must be installed to permit activation of the Watchdog. If jumper W4 is removed, the Watchdog is disabled. The W4 settings are shown below (* = initial setting):

W4 Watchdog Timer



The Watchdog must also be enabled and refreshed by software. To enable the Watchdog by software, first write 01h at I/O address E0h (selects Index-01), then write "0" at I/O address E1h bit 1.

When enabled, the microprocessor must refresh the Watchdog. To do this, first write 01h at I/O address E0h (selects Index-01), then write alternatively "0" and "1" at I/O address E1h bit 2.

Following a reset, the Watchdog is always disabled.

If a hardware or software failure occurs such that the Watchdog is not refreshed, a reset pulse is generated by the Watchdog to restart the processor.

The default timeout period is 1.6 seconds; however, the timeout period can be changed. Shorting C249 and leaving R171 opened changes the timeout to 100 ms. Shorting R171 and installing a capacitor at C249 will change the timeout period according to the following formulae:

$$\text{Timeout (milliseconds)} = \frac{400}{47\text{pF}} \times C \qquad \text{or} \qquad C249 = \frac{\text{Timeout (milliseconds)} \times 47\text{pF}}{400\text{ms}}$$

For instance, an external capacity of 100pF will lengthen the timeout to 851ms and a 1000pF will bring it to 8.5 seconds.

Note: R171 and C249 are located on the Bottom assembly.

7.6. SYSTEM POWER MANAGEMENT

System Power Management is software configurable through the AWARD Setup program.

For a description of power management modes and setup options available through the AWARD Power Management Setup, see Section 12.1.7 - Power Management Setup.

7.7. READING THE UNIQUE SERIAL NUMBER

The 48-bit serial number device located at U18 (under the CPU) contains the board's unique serial number. The number can be read by software.

For instructions on accessing this device, contact our Technical Support department.

8. INSTALLING STORAGE DEVICES

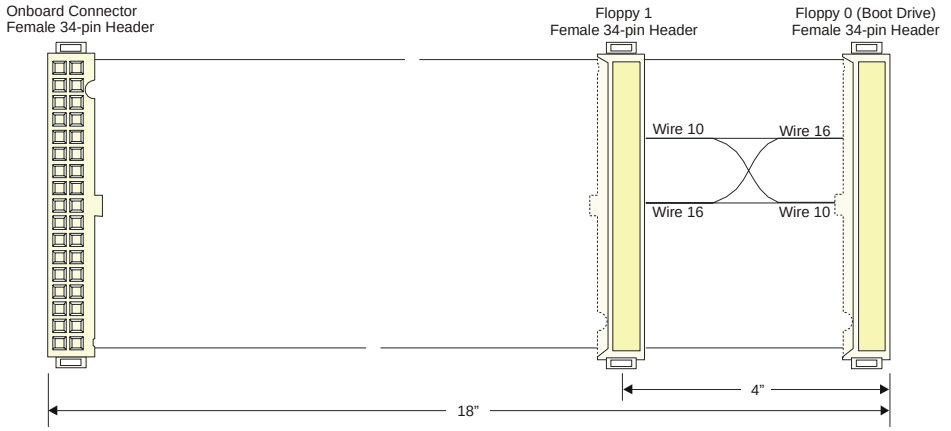
8.1. FLOPPY DEVICES

8.1.1 Floppy Connector

Two floppy disk drive units can be connected to the board through the J2 Floppy Disk connector using a standard IBM 34-pin flat ribbon cable. An 18” floppy disk cable is available from Kontron: part number 150-051-xx.

The floppy disk cable is illustrated below:

DIAGRAM 8-1: FLOPPY Disk Cable

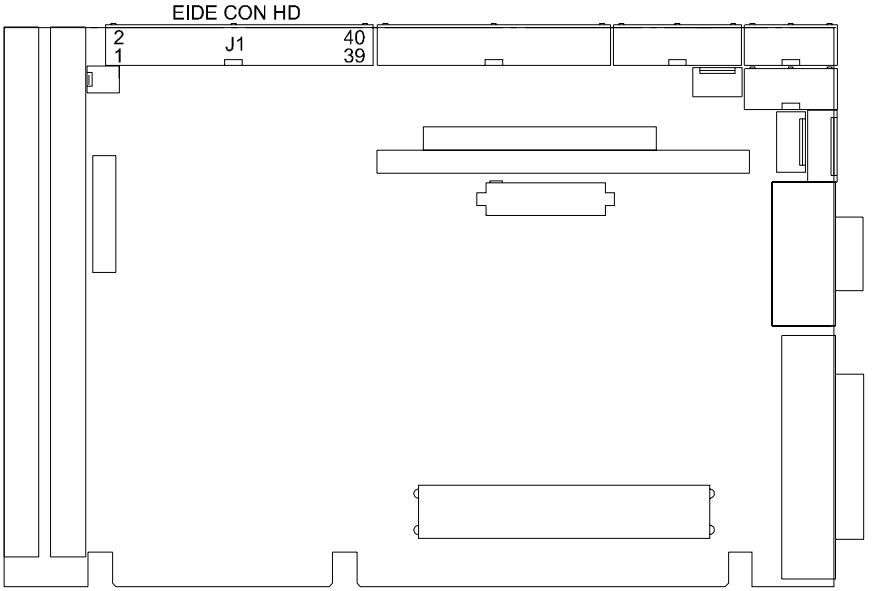


8.2. ENHANCED IDE DEVICES

8.2.1 EIDE Connector

The Enhanced IDE connector appears on Diagram 8-1 at J1.

DIAGRAM 8-2: Enhanced IDE Connector (J1) Location

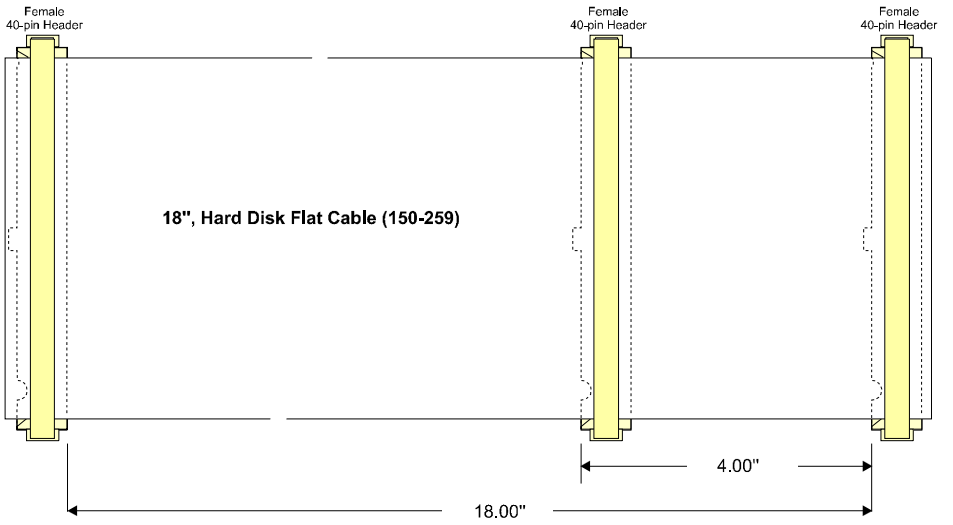


The cable needed to hook up the IDE connector is a 40-pin flat ribbon cable (shown in Diagram 8-2). This cable connects directly to the J1 IDE 40-pin connector and allows two IDE devices to be connected. It handles all command, data and status I/O lines. Its recommended maximum length is 18 inches from the IDE device to the 40-pin connector. The cable is available and referred to as part number 150-259.

You may want to make your own cable with a 40-pin flat ribbon cable and 40-pin flat cable mating connectors. The following is a list of approved vendors for the mating 40-pin flat cable connector:

AMP 746285-9 [optional strain relief: 499252-1],
Robinson Nugent IDS-C40PK-TG,
Thomas & Betts622-4030 [optional strain relief: 622-4041].

DIAGRAM 8-3: IDE Hard Disk Cable



8.3. COMPACTFLASH™ DISK

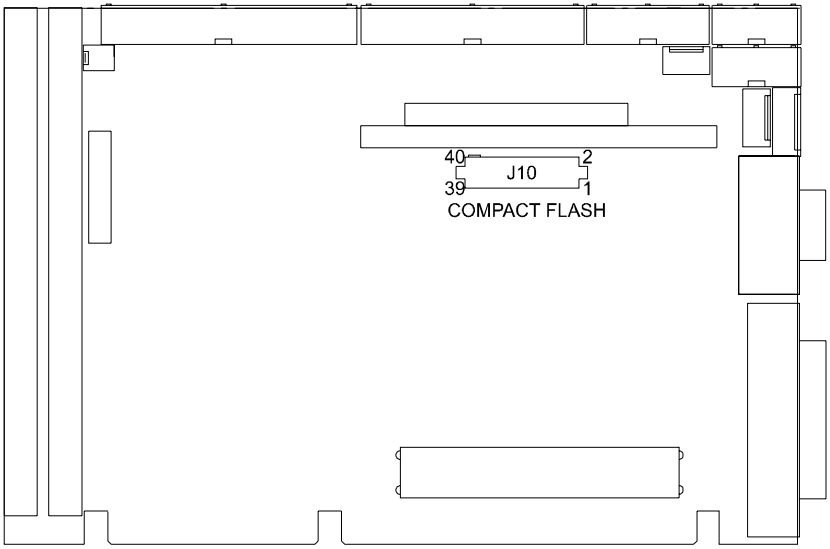
The VIPer825 may be ordered with an IDE compatible flash disk installed on the CompactFlash module. Available capacities are 4, 10, 15, 30, 40 or 48 MB. This module will support higher capacities when available. The flash disk connects to the secondary IDE channel, is bootable and completely user upgradeable.

CompactFlash disks are the world's smallest resident industry-standard ATA/IDE subsystems for application, data, image, and audio storage. They have the same functionality and capabilities as intelligent IDE disk drives, but with the advantages of being very compact solid-state disks and removable.

8.3.1 CompactFlash IDE Connector

The CompactFlash Disk's IDE connector is located at J10.

DIAGRAM 8-4: CompactFlash Disk IDE Connector (J10) Location



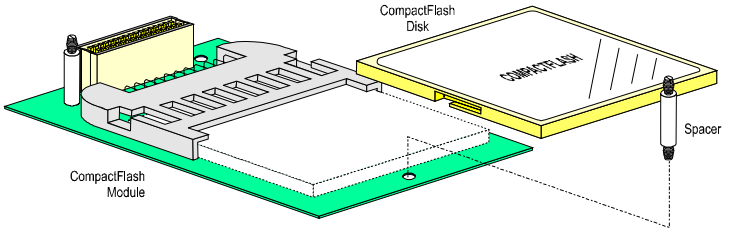
8.3.2 Installing CompactFlash™ Disks on CompactFlash™ Module

Installing a Compact Flash disk on the VIPer825 requires the CompactFlash module that connects to the VIPer825 board's J10 CompactFlash connector.

If the CompactFlash module is already installed on your VIPer825 board, you must first remove it prior to installing or replacing a CompactFlash disk on the module.

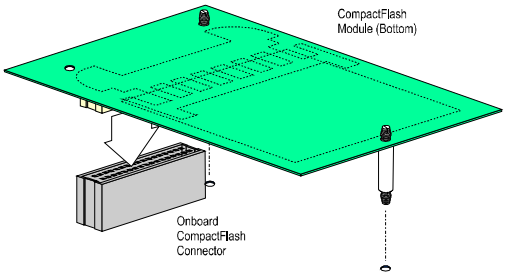
Follow this procedure to install a CompactFlash disk on the CompactFlash module and to install the module on the VIPer825:

1. Slide the Compact Flash disk into its receptacle and press gently to ensure a good insertion and connection.



2. Clip the spacers into their mounting holes: one is located close to the interface connector, and another is located near the flash disk (see drawing above). The spacer located near the flash disk acts as a retention mechanism to the flash disk and prevents it from accidentally sliding out.

3. To connect the module to the VIPer825, simply line up the J10 connector and the interface connector, then press the daughterboard firmly into the Single Board Computer's connector to engage the connector and the spacers.



8.3.3 Working with a COMPACTFLASH™ Disk

A Compact Flash disk connects directly on the secondary IDE interface and must be declared the same way as a standard IDE hard disk using the AWARD Setup program.

Since data is accessed like it would on an IDE drive, no specific flash disk driver is required for various operating systems.

9. INSTALLING PERIPHERALS

9.1. SERIAL PORTS

There are two 16C550 compatible serial ports. These have internal 16-byte FIFO buffers for more efficient data transfers.

For information on the programming of serial ports with the use of FIFO buffers, you can ask for Application Note # AN93007 from our Technical Support department.

9.1.1 Serial Port Connectors

Serial Port 1 and Serial Port 2 connectors appear on Diagram 9-1 at J7, J11 (Serial Port 1) and J4 (Serial Port 2).

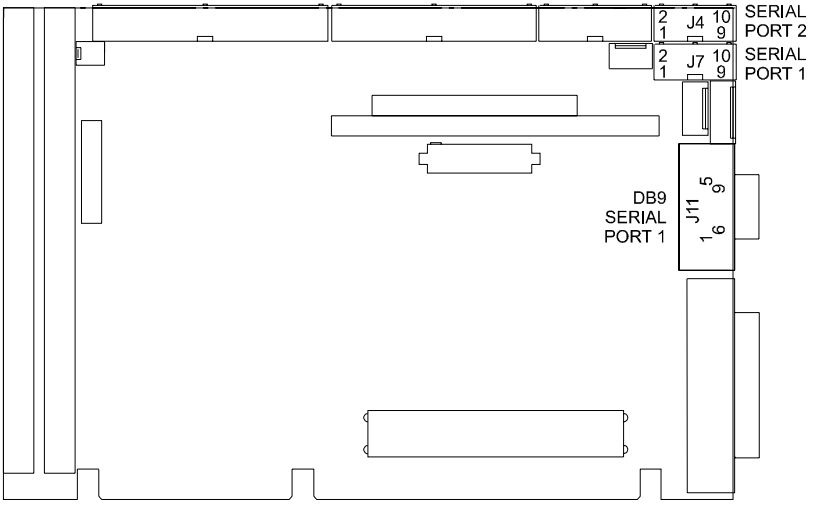


DIAGRAM 9-1: Serial Ports Location

The following list includes approved vendors for the J4 and J9 connectors' mating parts:

Amp 746285-1 [optional strain relief: 499252-5],
Robinson Nugent IDS-C10PK-TG,
Thomas & Betts 622-1030 [optional strain relief: 622-1041].
(10-pin flat cable connector).

9.1.1.1. Serial Port 1 (J7) RS-232

The Serial Port 1 is configured as RS-232. With the IBM 9-pin DSUB Standard, Serial Port 1 is 100% compatible with the IBM-AT serial port. The cable and connector pinouts appear in Diagram 10-2.

We offer a 10-pin header to 9-pin DSUB cable for PC-AT compatibility. This can be purchased (part number 150-019) or a cable can be made with a flat cable, a 10-pin flat cable crimp header and a 9-pin DSUB flat cable crimp connector.



CAUTION

The use of Taiwanese adapter cables is not recommended, since the pinout is often incorrect. The direct crimp design offered allows the simplest cable assembly. All these cables are available by contacting the Sales department.

9.1.1.2. Serial Port 1 (J11) RS-232 – Standard DB9 Serial Port

Serial Port 1 can use either the J7 connector (10-pin) which was described on page 9-2, or the J11 connector (9-pin) described on this page, however the board supports only one at a time.

Like Serial Port 1 – J7, Serial Port 1 – J11 is configured as RS-232. But most importantly, the J11 connector is a standard DB9 serial port, needing no additional adapter cables to be 100% PC-AT compatible.

9.1.1.3. Serial Port 2 (J4) RS-232

The Serial Port 2 can be configured as RS-232 in the AWARD Setup program. Select the desired operation mode for Serial Port 2 in AWARD's Integrated Peripherals screen and the COM2 Operation Mode option: RS-232.

As a RS-232 port, and with the IBM 9-pin DSUB Standard, Serial Port 2 is 100% compatible with the IBM-AT serial port.

We offer a 10-pin header to 9-pin DSUB cable for PC-AT compatibility. This can be purchased (part number 150-019) or a cable can be made with a flat cable, a 10-pin flat cable crimp header and a 9-pin DSUB flat cable crimp connector.



CAUTION

The use of Taiwanese adapter cables is not recommended, since the pinout is often incorrect. The direct crimp design offered allows the simplest cable assembly. All these cables are available by contacting the Sales department.

9.1.1.4. Serial Port 2 (J4) RS-422 and RS-485

Serial Port 2 (J4) can be configured for RS-422 or RS-485 operation in the AWARD Setup program. Select the desired operation mode for Serial Port 2 in AWARD's Integrated Peripherals screen and the COM2 Operation Mode option: RS-422 or RS-485.

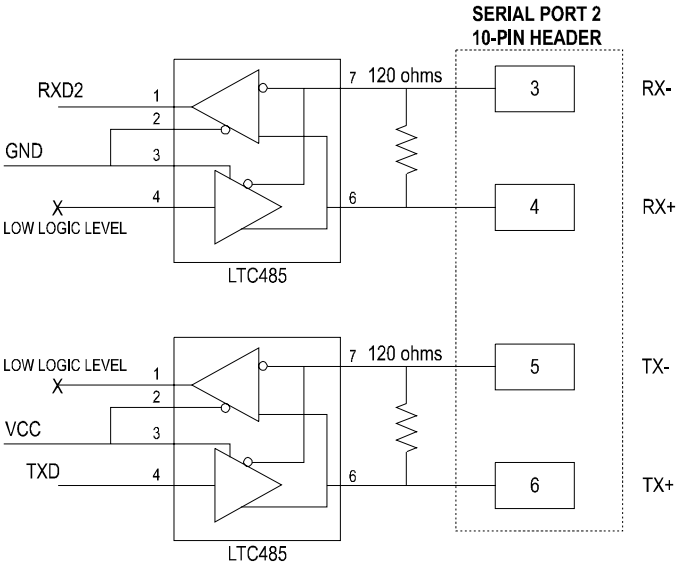
In RS-422 and RS-485 modes, the J4 serial port can transmit and receive differential signals, in either full-duplex (RS-422) or party line (RS-485) communication.

Communicating with differential signals requires one pair of wires for RS-485 and two pairs for RS-422 (one for transmission, one for reception).

For a better noise rejection, the use of twisted pair cable is highly recommended. This will enable faster serial transmissions over greater distances than with the common RS-232 protocol.

RS-422 - Full Duplex Operation: The RS-422 protocol uses both RX and TX lines during a communication session. Upon power-up or reset, the Serial Port 2 interface circuits are automatically configured for full duplex operation. Pins 3 and 4 of J4 act as the receiver lines and pins 5 and 6 act as the transmitter lines, as shown below.

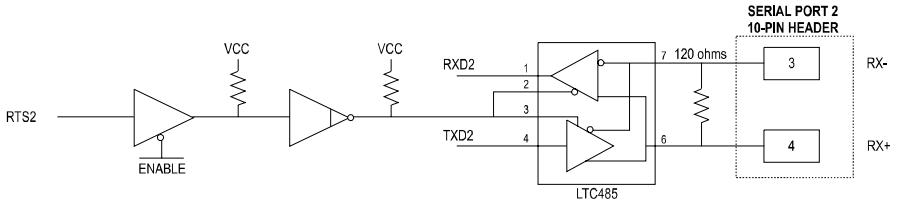
DIAGRAM 9-2: RS-422 Signals



In RS-422 mode, software should not use the handshake signals (e.g., DSR, DTR), since they are not connected. However, software handshaking can be used (e.g., XON-XOFF).

RS-485 - Party Line Operation: The RS-485 offers the ability to transmit and receive over the same pair of wires (RX outputs: pins 3 and 4 as shown below), and share the same communication line with multiple stations.

DIAGRAM 9-3: RS-485 Signals

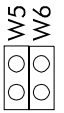


To ensure this configuration, only one system takes control of the communication at a time.

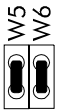
Upon power-up or reset, the transceiver is by default in "receiver mode" in order to preventing unwanted perturbation on the line.

In RS-485 mode, only both ends of the network must be terminated (120 ohms resistors). Termination resistors (R9 and R25) are available on the VIPer825. If the board is installed at the end of the network, use the W5 and W6 jumpers to connect the RS-485 termination resistors.

W5 Serial Port 2 Termination
W6 Resistors



RS-232 or RS-422/RS-485
Without Termination Resistors *



RS-422/RS-485
With Termination Resistors

* = initial setting

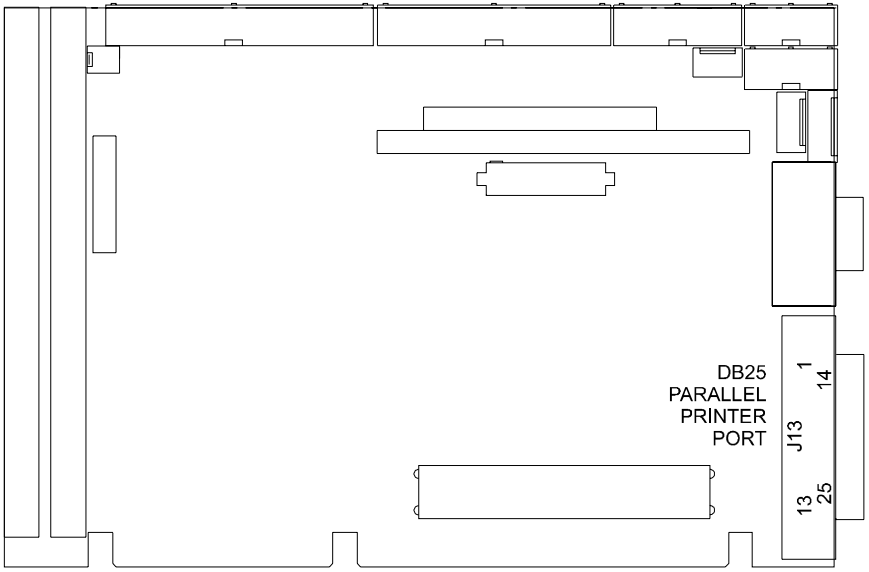
The RS-485 protocol offers some advantages such as increased speed over long distances, improved reliability over similar RS-232 setups, ability to share transmission line, less cabling requirements than the RS-422 protocol.

9.2. PARALLEL PORT

9.2.1 Parallel Port Connector

The Parallel Port connector is a DB25 female connector located on the board's bracket at J13.

DIAGRAM 9-4: Parallel Port Location



9.2.2 Parallel Port Modes

9.2.2.1. Standard Mode

The Standard Mode is an unidirectional parallel port. It is used for compatibility with the IBM PC standard.

9.2.2.2. EPP (Enhanced Parallel Port) Mode

To operate in EPP mode, the peripheral must be designed to operate in this mode and the BIOS setup must be configured to support it.

The EPP mode consists of a hardware independent method of accessing a parallel port. It provides support for single I/O cycle as well as high-performance block I/O transfers.

9.2.2.3. ECP (Extended Capabilities Port) Mode

To operate in ECP mode, the peripheral must be designed to operate in this mode and the BIOS setup must be configured to support it.

While the EPP mode may intermix read and write operations without any overhead or protocol handshaking, the ECP mode negotiates data transfers using a request from the host and an acknowledgement from the peripheral.



NOTE

For more information on the ECP protocol, please refer to the Extended Capabilities Port Protocol and ISA Interface Standard (available from Microsoft Corporation) or contact our Technical Support department.

PART 3

SOFTWARE & ONBOARD FEATURES

10. SOFTWARE SETUP

11. UPDATING OR RESTORING BIOS IN FLASH

12. VT100 MODE

10. SOFTWARE SETUP

10.1. THE AWARD SETUP PROGRAM

10.1.1 Accessing the AWARD Setup Program

The system BIOS (Basic Input Output System) provides an interface between the operating system and the hardware of the VIPer825 single board computer. The interface provided by AWARD is 100% IBM AT compatible. All functions accept similar inputs as IBM and provide the same results, although the program code itself is different.

The VIPer825 uses the AWARD Setup program, a setup utility in ROM that is accessed by pressing the DELETE key at the appropriate time during system boot. This utility is used to set configuration data in CMOS RAM.

> **CAUTION**
> Before modifying CMOS setup parameters, insure that the W8 battery selection jumper is installed to enable the CMOS battery backup (settings in Section 6.2).

To run the AWARD Setup program incorporated in the ROM BIOS:

1. Turn on or reboot the system.
2. Hit the DELETE key before or when the message - "Press DEL To Enter SETUP" appears near the bottom of the screen.
3. The main menu of the AWARD BIOS CMOS Setup Utility appears on the screen.

ROM PCI/ISA BIOS (2A59FI3C)
CMOS SETUP UTILITY
AWARD SOFTWARE, INC.

STANDARD CMOS SETUP	INTEGRATED PERIPHERALS
BIOS FEATURES SETUP	SUPERVISOR PASSWORD
CHIPSET FEATURES SETUP	USER PASSWORD
POWER MANAGEMENT SETUP	IDE HDD AUTO DETECTION
PNP/PCI CONFIGURATION	HDD LOW-LEVEL FORMAT
LOAD BIOS DEFAULTS	SAVE & EXIT SETUP
LOAD SETUP DEFAULTS	EXIT WITHOUT SAVING
Esc : Quit F10 : Save & Exit Setup	↑↓→← : Select Item (Shift)F2 : Change Color
Time, Date, Hard Disk Type . . .	

10.1.2 Using AWARD Setup

The arrow keys (↑ ↓ → ←) are used to highlight items on the menu and the PAGEUP and PAGEDOWN keys are used to change the entry values for the highlighted item. To select an entry, press the ENTER key. Also, you can press the F1 key to obtain help information or the ESC key to leave an option, close a menu or to quit the program.

Table 10-1 provides more details on how to navigate in the Setup program:

TABLE 10-1: Using AWARD Setup Program

Key	Function
↑	Moves to previous item.
↓	Moves to next item.
←	Moves to the item in the left hand.
→	Moves to the item in the right hand.
ESC	When in the Main Menu: Quits program (Answer 'Y' to save changes into CMOS). When in other screens: Exits and returns to the Main Menu.
PAGEUP or +	Increases the numeric value or changes value.
PAGEDOWN or -	Decreases the numeric value or changes value.
F5	When in the Main Menu: Restores the previous setup values from the BIOS Default Table for all the BIOS parameters. When in BIOS Features Setup, Chipset Features Setup, Power Management Setup, PNP/PCI Setup or Integrated Peripherals Setup: Restores the previous setup values from the BIOS Default Table for that setup screen only.
F6	When in the Main Menu: Loads the default setup values from BIOS Default Table for all the BIOS parameters. When in BIOS Features Setup, Chipset Features Setup, Power Management Setup, PNP/PCI Setup or Integrated Peripherals Setup: Loads the default setup values from BIOS Default Table for all the BIOS parameters for that setup screen only.
F7	When in the Main Menu: Loads the default setup values from Setup Default Table for all the BIOS parameters. When in BIOS Features Setup, Chipset Features Setup, Power Management Setup, PNP/PCI Setup or Integrated Peripherals Setup: Loads the default setup values from Setup Default Table for all the BIOS parameters for that setup screen only.
F10	When in the Main Menu: Saves all the CMOS changes.

The Main Menu includes the following categories:

Standard CMOS Setup	This Setup page includes all the items in a standard, AT-compatible BIOS (date, time, hard disk type, floppy disk type, video adapter type, memory...).
BIOS Features Setup	This Setup page includes all the items of AWARD's special enhanced features.
Chipset Features Setup	This Setup page includes all the items of the chipset's special features.
Power Management Setup	This Setup page sets power conservation options.
PnP/PCI Configuration	This Setup page sets Plug and Play and PCI Local Bus configuration options.
Integrated Peripherals	I/O susbsystems that depend on the integrated peripherals controller in your system.
Supervisor/User Password Setting	Change, set, or disable password. It allows you to limit access to the system and the Setup, or just to the Setup.
IDE HDD Auto Detection	Automatically detect and configure hard disk parameters. This ability is included in the event you are uncertain of your hard disk's parameters.
HDD Low-Level Format	This option does not appear in many BIOS versions. Most manufacturers of IDE hard drives strongly recommend that you do not run a low-level format on their drives, because of the danger that the bad-track table may be over-written. Award supplies this utility for service personnel only. ***If you need to run a low-level format on your hard drive, contact your drive manufacturer for instructions!***
Load Bios Defaults	The BIOS defaults represent settings which provide the minimum requirements for your system to operate.
Load Setup Defaults	The chipset defaults are settings which provide for maximum system performance.

10.1.3 Saving Configurations & Exiting AWARD Setup

Use one of the following options available from the Main Menu:

Save & Exit — After having modified the AWARD Setup, you can save the configuration in CMOS RAM, by selecting this option. To also update the values in the Flash BIOS when using this option, set the "Save CMOS in Flash" option from the BIOS Features Setup screen to "Enabled".

Exit Without Saving — This option is used to exit AWARD Setup without saving the configuration to CMOS RAM.

10.1.4 Standard CMOS Setup

This part of the setup allows you to set the time, date, hard disk type, types of floppy drives and video type.

Date/Time — The current values for each category are displayed. Enter new values through the keyboard.

Hard Disks — Two IDE controllers are defined on the VIPer825 board (Primary and Secondary). The Primary controller can have two disks: Master Disk or Slave Disk. The Secondary controller is dedicated to the IDE CompactFlash disk. The disks are bootable in this order: 1) IDE-1 Master, 2) IDE-1 Slave, 3) IDE-2 Master (CompactFlash).

Drive A / Drive B — Select the type of floppy disk installed for drive A and drive B.

Video — This option specifies the basic type of display adapter card installed in the system.

Halt on — This option specifies the type of errors that will stop the system during the BIOS booting procedure. A message asks that you press F1 to continue or press the DELETE key to enter Setup. The settings are: All errors, No errors, All but keyboard (default setting), All but diskette, and All but disk/key.

Memory — This display-only option indicates the amount of Base, Extended and other types of memory installed in the system.

10.1.5 BIOS Features Setup

This part of the setup handles options and features such as boot sequence, NUM LOCK, security options, shadowing, ...

Whenever you are not sure about a certain setting, you may refer to the list of default values. The list of defaults is provided in the event that a value has been changed and one wishes to set this option to its original value. Loading the BIOS or SETUP defaults will affect all the options in this screen (or all parameters if defaults are loaded from the Main Menu) and will reset options previously altered.

The BIOS default settings consist of the safest set of parameters. Use them if the system is behaving erratically. They should always work but do not provide optimal system performance.

The SETUP default values provide optimum performance settings for all devices and system features.

TABLE 10-2: BIOS Features Setup

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
Virus Warning	Disabled	Disabled	Enabled, Disabled	When Enabled, you receive a warning message if a program (specifically, a virus) attempts to write to the boot sector or the partition table of the hard disk drive. You should then run an anti-virus program. Keep in mind that this feature protects only the boot sector, not the entire hard drive. **Note: Many disk diagnostic programs and OS setups (e.g., Win95 setup), that access the boot sector table, can trigger the virus-warning message. If you plan to run such a program, we recommend that you first disable the virus warning.**
CPU Internal Cache	Disabled	Enabled	Enabled, Disabled	Enables or Disables the CPU Internal Cache (L1 cache).
External Cache	Disabled	Enabled	Enabled, Disabled	Enables or Disables the External Cache (L2 cache).

TABLE 10-2: BIOS Features Setup (Continued)

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
Quick Power-On Self-Test	Disabled	Enabled	Enabled, Disabled	Select Enabled to reduce the amount of time required running the power-on self-test (POST). A quick POST skips certain steps. We recommend that you enable quick POST to save time, since most major OS do their own tests
Boot Sequence	A, C, SCSI	C, A, SCSI	A, C, SCSI; C, A, SCSI; C, CDROM, A; CDROM, C, A; D, A, SCSI; E, A, SCSI; F, A, SCSI; SCSI, A, C; SCSI, C, A; C only	This option defines the searching order in the BIOS for the boot device(s).
Swap Floppy Drive	Disabled	Disabled	Enabled, Disabled	Selecting Enabled assigns physical drive B to logical drive A, and physical drive A to logical drive B. If there is only one floppy on the system, it could be assigned to B with this option.
Boot Up Floppy Seek	Enabled	Disabled	Enabled, Disabled	When Enabled, the BIOS tests (seeks) floppy drives to determine whether they have 40 or 80 tracks. Only 360KB floppy drives have 40 tracks; drives with 720KB, 1.2MB, and 1.44MB capacity all have 80 tracks. Because very few modern PCs have 40 track floppy drives, we recommend that you set this field to "Disabled" to save time.
Boot Up NumLock Status	Off	Off	On, Off	Toggle between On or Off to control the state of the NumLock key when the system boots. When toggled On, the numeric keypad generates numbers instead of controlling cursor operations.
Boot Up System Speed	High	High	Low, High	Select High to boot at the default CPU speed; select Low to boot at the speed of the AT bus. Some add-in peripherals or old software (such as old games) may require a slow CPU speed. The default setting is High.
Typematic Rate Setting	Disabled	Disabled	Enabled, Disabled	When Disabled, the following two items (Typematic Rate and Typematic Delay) are irrelevant. Keystrokes repeat at a rate determined by the keyboard controller in your system. When Enabled, you can select a typematic rate and a typematic delay.

TABLE 10-2: BIOS Features Setup (Continued)

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
Typematic Rate (Chars/Sec)	30	30	6, 8, 10, 12, 15, 20, 24, 30 char per second	When the typematic rate setting is Enabled, you can select a typematic rate (the rate at which characters repeat when you hold down a key.
Typematic Delay (Msec)	250	250	250, 500, 750, 1000 ms	When the typematic rate setting is Enabled, you can select a typematic delay (the delay before keystrokes begin to repeat).
Security Option	Setup	Setup	Setup, System	If you have set a password, select whether the password is required every time the system boots (“System” option), or only when you enter Setup (“Setup” option).
OS Select For DRAM > 64MB	Non-OS2	Non-OS2	Non-OS/2, OS/2	Select OS2 only if you are running an OS/2 operating system with greater than 64MB of RAM.
Save CMOS in Flash	Disabled	Disabled	Enabled, Disabled	When this option is set to “Enabled”, the CMOS RAM Setup will be restored from the Flash BIOS at each power up. If the battery fails, only the date and time could be lost.

TABLE 10-2: BIOS Features Setup (Continued)

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
Video BIOS Shadow	Disabled	Enabled	Enabled, Disabled	Software that resides in a read-only memory (ROM) chip on a device is called *firmware*. Award permits shadowing of firmware such as the system BIOS, video BIOS, and similar operating instructions that come with some expansion peripherals. Shadowing copies from ROM into system RAM, where the CPU can read it through the 64-bit DRAM bus. Firmware not shadowed must be read by the system through the 8 or 16-bit ISA bus. Shadowing improves the performance of the system BIOS and similar firmware for expansion peripherals. Enable shadowing into each section of memory separately. Many system designers hardwire shadowing of the system BIOS and eliminate a System BIOS Shadow option. Note that on a PCI VGA card (onboard or offboard), the VGA BIOS is always shadowed. Video BIOS shadows into memory area C0000 plus the VGA BIOS size. The remaining areas between C0000 and DFFFF shown on the BIOS Features Setup screen may be occupied by other expansion card firmware. If an expansion peripheral in your system contains ROM-based firmware, you need to know the address range the ROM occupies to shadow it into the correct area of RAM.
CC000-CFFFF Shadow	Disabled	Disabled	Enabled, Disabled	
D0000-D3FFF Shadow	Disabled	Disabled	Enabled, Disabled	
D4000-D7FFF Shadow	Disabled	Disabled	Enabled, Disabled	
D8000-DBFFF Shadow	Disabled	Disabled	Enabled, Disabled	
DC000-DFFFF Shadow	Disabled	Disabled	Enabled, Disabled	

10.1.6 Chipset Features Setup

This part of the setup allows you to define chipset-specific options and features.

Whenever you are not sure about a certain setting, you may refer to the list of default values. The list of defaults is provided in the event that a value has been changed and one wishes to set this option to its original value. Loading the BIOS or SETUP defaults will affect all the options in this screen (or all parameters if defaults are loaded from the Main Menu) and will reset options previously altered.

The BIOS default settings consist of the safest set of parameters. Use them if the system is behaving erratically. They should always work but do not provide optimal system performance.

The SETUP default values provide optimum performance settings for all devices and system features.

> **CAUTION**
> These parameters have been provided to give control over the system. However, the values for these options should be changed only if the user has a full understanding of the timing relationships involved.

TABLE 10-3: Chipset Features Setup

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
Auto Configuration	Enabled	Enabled	Enabled, Disabled	Auto Configuration selects predetermined optimal values of chipset parameters. When Disabled, chipset parameters revert to setup information stored in CMOS. Many fields in this screen are not available when Auto Configuration is Enabled.
DRAM Timing	70 ns	70 ns	70 ns, 60 ns	The value in this field depends on performance parameters of the installed memory chips (DRAM). Do not change the value from the factory setting unless you install new memory that has a different performance rating than the original DRAMs.

TABLE 10-3: Chipset Features Setup (Continued)

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
DRAM RAS# Precharge Time	4	4	4, 3	Select the number of CPU clocks allocated for the Row Address Strobe (RAS#) signal to accumulate its charge before the DRAM is refreshed. If insufficient time is allowed, refresh may be incomplete and data lost.
DRAM R/W Leadoff Timing	7/6	7/6	7/6, 6/5	Select the combination of CPU clocks the DRAM on your board requires before each read from or write to the memory. Changing the value from the setting determined by the board designer for the installed DRAM might cause memory errors.
Fast RAS# to CAS# Delay	3	3	3, 2	When DRAM is refreshed, both rows and columns are addressed separately. This setup item allows you to determine the timing of the transition from RAS to Column Address Strobe (CAS).
DRAM Read Burst (EDO/FPM)	x333/ x444	x333/ x444	x444/ x444, x333/ x444, x222/ x333	Sets the timing for reads from EDO (Extended Data Output) or FPM (Fast Page Mode) memory. The lower the numbers, the faster the system addresses memory. Selecting timing numbers lower than the installed DRAM is able to support can result in memory errors.
DRAM Write Burst Timing	x333	x333	x444, x333, x222	Sets the timing for writes to memory. The lower the timing numbers, the faster the system addresses memory. Selecting timing numbers lower than the installed DRAM is able to support can result in memory errors.
Turbo Read Leadoff	Disabled	Disabled	Enabled, Disabled	Select Enabled to shorten the leadoff cycles and optimize performance in cacheless, 50-60 MHz, or one-bank EDO DRAM systems.
DRAM Speculative Leadoff	Disabled	Disabled	Enabled, Disabled	A read request from the CPU to the DRAM controller includes the memory address of the desired data. When Enabled, Speculative Leadoff lets the DRAM controller pass the read command to memory slightly before it has fully decoded the address, thus speeding up the read process.
Turn-Around Insertion	Disabled	Disabled	Enabled, Disabled	When Enabled, the chipset inserts one extra clock to the turn-around of back-to-back DRAM cycles.

TABLE 10-3: Chipset Features Setup (Continued)

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
ISA Clock	PCI CLK/ 4	PCI CLK/ 4	PCI CLK/ 4, PCI CLK/ 3	You can set the speed of the AT bus at one-third or one-fourth of the PCI clock speed (60 or 66 MHz).
System BIOS Cacheable	Disabled	Enabled	Enabled, Disabled	Selecting Enabled allows caching of the system BIOS ROM at F0000h-FFFFFh, resulting in better system performance. However, if any program writes to this memory area, a system error may occur.
Video BIOS Cacheable	Disabled	Enabled	Enabled, Disabled	Selecting Enabled allows caching of the video BIOS ROM at C0000h to C7FFFh, resulting in better video performance. However, in any program writes to this memory area, a system error may occur.
8 Bit I/O Recovery Time	3	1	1, 2, 3, 4, 5, 6, 7, 8, NA	The I/O recovery mechanism adds bus clock cycles between PCI-originated I/O cycles to the ISA bus. This delay takes place because
16 Bit I/O Receiving Time	2	1	1, 2, 3, 4, NA	the PCI bus is so much faster than the ISA bus. These two fields let you add recovery time (in bus clock cycles) for 16-bit and 8-bit I/O.
Peer Concurrency	Enabled	Enabled	Enabled, Disabled	Peer concurrency means that more than one PCI device can be active at a time.
Chipset Special Features	Enabled	Enabled	Enabled, Disabled	When Disabled, the chipset behaves as if it were the earlier Intel 82430FX chipset.
DRAM ECC/PARITY Select	Parity	Parity	ECC, Parity	Set this option according to the type of DRAM installed in your system: error-correcting code (ECC) or parity (default).
Memory Parity/ECC Check	Auto	Auto	Enable, Disable, Auto	In Auto mode, the BIOS enables memory checking automatically when it detects the presence of ECC or parity DRAM.
Single Bit Error Report	Enabled	Enabled	Enabled, Disabled	If ECC is enabled, selecting Enabled here tells the system to report an error when a correctable single-bit error occurs.
Chipset NA# Asserted	Enabled	Enabled	Enabled, Disabled	When Enabled, the chipset will use the NA (Next Address) protocol with the CPU to enable cache bursting.

TABLE 10-3: Chipset Features Setup (Continued)

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
Pipeline Cache Timing	Faster	Faster	Faster, Fastest	For a secondary cache of 256KB (one bank), select Faster. For a secondary cache of 512KB (two banks), the system designer must select Faster (3-1-1-1, 2-1-1-1) or Fastest (3-1-1-1, 1-1-1-1). Cache timing 3-1-1-1 is at the CPU access speed. It requires special SRAMs because the 3-1-1-1 timing is at the CPU clock rate.
Passive Release	Enabled	Enabled	Enabled, Disabled	When Enabled, CPU to PCI bus accesses are allowed during passive release otherwise the arbiter only accepts another PCI master access to local DRAM.
Delayed Transaction	Disabled	Enabled	Enabled, Disabled	The chipset has an embedded 32-bit posted write buffer to support delay transactions cycles. Select Enabled to support compliance with PCI specifications version 2.1.
Memory Hole Location	None	None	512K-640K, 15M-16M, None	You can reserve this area of system memory for ISA adapter ROM. When this area is reserved, it cannot be cached. The user information of peripherals that need to use this area of system memory usually discusses their memory requirements.

10.1.7 Power Management Setup

This part of the setup sets power conservation options.

Whenever you are not sure about a certain setting, you may refer to the list of default values. The list of defaults is provided in the event that a value has been changed and one wishes to set this option to its original value. Loading the BIOS or SETUP defaults will affect all the options in this screen (or all parameters if defaults are loaded from the Main Menu) and will reset options previously altered.

The BIOS default settings consist of the safest set of parameters. Use them if the system is behaving erratically. They should always work but do not provide optimal system performance.

The SETUP default values provide optimum performance settings for all devices and system features.

TABLE 10-4: Power Management Setup

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
Power Management	Disable	Disable	Min Saving, Max Saving, User Define, Disable	This option allows you to select the type (or degree) of power saving for Doze, Standby, and Suspend modes. Max Saving: Maximum power savings. Inactivity period is 1 minute in each mode. Min Saving: Minimum power savings. Inactivity period is the maximum setting in each mode (1 hour for Doze, Standby and Suspend). User Define: Set each mode individually. Select time-out periods in the PM Timers section (see below).
PM Control by APM	Yes	Yes	Yes, No	If Advanced Power Management (APM) is installed on your system, selecting Yes gives better power savings. This enables power management control by an external program (generally the operating system).

TABLE 10-4: Power Management Setup (Continued)

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
Video Off Method	V/H SYNC+Blank	V/H SYNC+Blank	V/H SYNC+Blank, DPMS, Blank Screen	Determines the manner in which the monitor is blanked. V/H SYNC + Blank: System turns off vertical and horizontal synchronization ports and writes blanks to the video buffer. DPMS Support: Select this option if your monitor supports the Display Power Management Signaling (DPMS) standard of the Video Electronics Standards Association (VESA). Use the software supplied for your video subsystem to select video power management values. Blank Screen: System only writes blanks to the video buffer.
Modem Use IRQ	3	3	N/A, 3, 4, 5, 7, 9, 10, 11	Name the IRQ line assigned to the modem (if any) on your system. Activity of the selected IRQ always awakens the system.
PM Timers:				The following modes are Green PC power saving functions. They are user-configurable only during User Defined Power Management mode.
Doze Mode	Disable	Disable	1, 2, 4, 6, 8, 10, 20, 30, 40 mins, 1 hour, Disable	When the selected period of system inactivity prior to Doze mode (1 minute to 1 hour) has elapsed, the CPU clock runs at lower speed while all other devices still operate at full speed.
Standby Mode	Disable	Disable	1, 2, 4, 6, 8, 10, 20, 30, 40 mins, 1 hour, Disable	After entering Doze mode, when the selected period of system inactivity prior to Standby mode (1 minute to 1 hour) has elapsed, the fixed disk drive and the video shut off while all other devices still operate at full speed.
Suspend Mode	Disable	Disable	1, 2, 4, 6, 8, 10, 20, 30, 40 mins, 1 hour, Disable	After entering Standby mode, when the selected period of system inactivity prior to Suspend mode (1 minute to 1 hour) has elapsed, all devices except the CPU shut off.
HDD Power Down	Disable	Disable	1, 2, 3, (...), 15 mins, Disable	When the selected period of drive inactivity prior to HDD power down (1 to 15 minutes) has elapsed, the hard disk drive powers down while all other devices remain active. The HDD power down mode is only available if the hard drive has this capability.

TABLE 10-4: Power Management Setup (Continued)

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
Wake Up Events In Doze & Standby			On, Off	When the system is in Doze or Standby mode, you may disable activity monitoring of some common interrupt requests (IRQ3/4/8/12) so they do not wake the system. The default wake-up event is keyboard activity. In these wake-up event fields, you can turn On or Off four commonly used interrupts. For example, if you have a modem on IRQ3, you can turn on IRQ3 as a wake-up event, so an interrupt from the modem can wake up the system. Or you may wish to turn Off IRQ12 (the PS/2) mouse as a wake-up event, so accidentally brushing the mouse does not awaken the system.
IRQ3 (Wake-Up Events)	Off	On		
IRQ4 (Wake-Up Events)	Off	On		
IRQ8 (Wake-Up Events)	Off	On		
IRQ12 (Wake-Up Events)	Off	On		
Power Down and Resume Events:			On, Off	You may disable monitoring of common interrupt requests so they do not reset activity timers.
IRQ3 (COM 2)	Off	On		
IRQ 4 (COM 1)	Off	On		
IRQ 5 (LPT 2)	Off	On		
IRQ 6 (Floppy Disk)	Off	Off		
IRQ 7 (LPT 1)	Off	On		
IRQ 8 (RTC Alarm)	Off	Off		
IRQ 9 (IRQ2 Redir)	Off	On		
IRQ 10 (Reserved)	Off	On		
IRQ 11 (Reserved)	Off	On		
IRQ12 (PS/2 Mouse)	Off	On		
IRQ 13 (Coprocessor)	Off	On		
IRQ 14 (Hard Disk)	Off	On		
IRQ 15 (Reserved)	Off	On		

10.1.8 PnP/PCI Configuration

This part of the setup sets PnP/PCI options.

Whenever you are not sure about a certain setting, you may refer to the list of default values. The list of defaults is provided in the event that a value has been changed and one wishes to set this option to its original value. Loading the BIOS or SETUP defaults will affect all the options in this screen (or all parameters if defaults are loaded from the Main Menu) and will reset options previously altered.

The BIOS default settings consist of the safest set of parameters. Use them if the system is behaving erratically. They should always work but do not provide optimal system performance.

The SETUP default values provide optimum performance settings for all devices and system features.

TABLE 10-5: PnP/PCI Configuration

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
PnP OS Installed	No	No	Yes, No	If the operating system (OS) is Plug and Play (for example Windows 95), select “Yes” if you want the OS to allocate resources according to Plug and Play standards, or “No” if you want the same resource allocations at every system boot-up. Select “No” when the OS is not Plug and Play (for example, DOS).
Resources Controlled By	Auto	Manual	Auto, Manual	The Award Plug and Play BIOS can automatically configure all the boot and Plug and Play-compatible devices. If you select Auto, all the interrupt requests (IRQs) and DMA assignment fields disappear, as the BIOS automatically assigns them.
Reset Configuration Data	Disabled	Disabled	Enabled, Disabled	Normally, you leave this field Disabled. Select Enabled to reset Extended System Configuration Data (ESCD) when you exit Setup if you have installed a new add-on and the system reconfiguration has caused such a serious conflict that the operating system cannot boot.

TABLE 10-5: PnP/PCI Configuration (Continued)

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
IRQ *n* Assigned To		IRQ-3, IRQ-4: Legacy ISA All other: PCI/ISA PnP	PCI/ISA PnP, Legacy ISA	When resources are controlled manually, assign each system interrupt as one of the following types, depending on the type of device using the interrupt: Legacy ISA: Devices compliant with the original PC AT bus specification, requiring a specific interrupt, such as IRQ4 for serial port 1. PCI/ISA PnP: Devices compliant with the Plug and Play standard, whether designed for PCI or ISA bus architecture. When Legacy ISA is selected for an IRQ line, this resource will not be available for PCI/ISA PnP.
DMA *n* Assigned To		PCI/ISA PnP	PCI/ISA PnP, Legacy ISA	When resources are controlled manually, assign each system DMA channel as one of the following types, depending on the type of device using the interrupt: Legacy ISA: Devices compliant with the original PC AT bus specification, requiring a specific DMA channel. PCI/ISA PnP: Devices compliant with the Plug and Play standard, whether designed for PCI or ISA bus architecture. When Legacy ISA is selected for a DMA channel, this resource will not be available for PCI/ISA PnP.
PCI IRQ Activated By	Level	Level	Level, Edge	Leave the IRQ trigger set at *Level* unless the PCI device assigned to the interrupt specifies Edge-triggered interrupts.
PCI IDE IRQ Map To	PCI-Auto	PCI-Auto	PCI-Auto, ISA, PCI-SLOT1, PCI-SLOT2, PCI-SLOT3, PCI-SLOT4	This field lets you select PCI IDE IRQ mapping or PC AT (ISA) interrupts. If your system does not have one or two PCI IDE connectors on the system board, select values according to the type of IDE interface(s) installed in your system (PCI or ISA). Standard ISA interrupts for IDE channels are IRQ14 for primary and IRQ15 for secondary.

TABLE 10-5: PnP/PCI Configuration (Continued)

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
Primary IDE INT#	A	A	A, B, C, D	Each PCI peripheral connection is capable of activating up to four interrupts: INT# A, INT# B, INT# C and INT# D. By default, a PCI connection is assigned INT# A. Assigning INT# B has no meaning unless the peripheral device requires two interrupt services rather than just one. Because the PCI IDE interface in the chipset has two channels, it requires two interrupt services. The primary and secondary IDE INT# fields default to values appropriate for two PCI IDE channels, with the primary PCI IDE channel having a lower interrupt than the secondary.
Secondary IDE INT#	B	B	A, B, C, D	
Used Mem Base Address		N/A	N/A, C800, CC00, D000, D400, D800, DC00	Select a base address for the memory area used by any peripheral that requires high memory.
Used Mem Length			8K, 16K, 32K, 64K	Select a length for the memory area specified in the previous field. This field does not appear if no base address is specified.

10.1.9 Integrated Peripherals

This part of the setup sets Integrated Peripherals options.

Whenever you are not sure about a certain setting, you may refer to the list of default values. The list of defaults is provided in the event that a value has been changed and one wishes to set this option to its original value. Loading the BIOS or SETUP defaults will affect all the options in this screen (or all parameters if defaults are loaded from the Main Menu) and will reset options previously altered.

The BIOS default settings consist of the safest set of parameters. Use them if the system is behaving erratically. They should always work but do not provide optimal system performance.

The SETUP default values provide optimum performance settings for all devices and system features.

TABLE 10-6: Integrated Peripherals

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
IDE HDD Block Mode	Disabled	Enabled	Enabled, Disabled	Block mode is also called block transfer, multiple commands, or multiple sector read/write. If your IDE hard drive supports block mode (most new drives do), select Enabled for automatic detection of the optimal number of block read/writes per sector the drive can support.
PCI Slot IDE 2nd Channel	Enabled	Enabled	Enabled, Disabled	You may separately disable the second channel on an IDE interface installed in a PCI expansion slot.
On-Chip Primary/ Secondary PCI IDE	Enabled	Enabled	Enabled, Disabled	The integrated peripheral controller contains an IDE interface with support for two IDE channels. Select Enabled to activate each channel separately.
IDE Primary/ Secondary Master/ Slave PIO	Auto	Auto	Mode 0, Mode 1, Mode 2, Mode 3, Mode 4, Auto	The four IDE PIO (Programmed Input/Output) fields let you set a PIO mode (0-4) for each of the four IDE devices that the onboard IDE interface supports. Modes 0 through 4 provide successively increased performance and speed. In Auto mode, the system automatically determines the best mode for each device. If you select a mode that the drive does not support, it may not work, so choose a lesser value or Auto to see the best mode for the drive.

TABLE 10-6: Integrated Peripherals (Continued)

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
USB Controller & Keyboard	Disabled	Disabled	Enabled, Disabled	Select Enabled, if your system contains a Universal Serial Bus (USB) controller and you have USB peripherals. This chipset supports USB keyboards.
Onboard FDC Controller	Enabled	Enabled	Enabled, Disabled	Select Enabled if your system has a floppy disk controller (FDC) installed on the system board and you wish to use it. If you install an add-in FDC or the system has no floppy drive, select Disabled in this field.
Onboard Serial Port 1/2	Auto	Auto	Disabled, 3F8/IRQ4, 2F8/IRQ3, 3E8/IRQ4, 2E8/IRQ3, Auto	Select a COM port address and IRQ# for the first and second serial ports.
Serial Port 2 Mode	RS-232	RS-232	RS-232, RS-422, RS-485	Select the operation mode for Serial Port 2.
VT100 Mode on Serial Port 1 or 2	1	1	1, 2	Selects the communication port for VT100 mode: Serial Port 1 or 2.
Onboard Parallel Port	378/IRQ7	378/IRQ7	378/IRQ7, 278/IRQ5, 3BC/IRQ7, Disabled	Select a LPT address and IRQ# for the physical parallel (printer) port.
Parallel Port Mode	Normal	ECP+EPP1.9	ECP+EPP1.9, Normal, EPP1.7+SPP, ECP+EPP1.7, SPP, EPP1.9+SPP, ECP	Select an operating mode for the onboard parallel port. Select ECP or EPP unless you are certain both your hardware and software does not support ECP or EPP mode.
ECP Mode Use DMA		3	1, 3	Select a DMA channel for the port.

11. UPDATING OR RESTORING BIOS IN FLASH

11.1. USING THE UBIOS UTILITY TO UPDATE BIOS

11.1.1 Introduction

BIOS UPDATE PROCEDURE

The BIOS update procedure can be found with the Emergency Recovery procedure on our ftp site: ftp://ftp.kontron.ca/Support in the FAQ section:

Download the FAQ# KC_0028 at location:

ftp://ftp.kontron.ca/Support/Support_FAQ - Questions & Answers/

EMERGENCY PROCEDURE

Symptoms:

- No POST code on a power up (when using a POST card).
- Board does not boot, even after usual hardware and connection verifications.
- At power up, there is floppy disk led activity, which is one sign that the BIOS as detected a corrupted BIOS CRC prior POST and falled back automatically to Emergency Recovery Mode looking for the floppy Emergency disk.

Please go on our FTP site in order to get the latest Emergency Recovery BIOS for that specific product.

BIOS maybe found at: Ftp://Ftp.Kontron.ca/Support/BIOS_Emergency/

Emergency Recovery Procedure is included within the Zip file of the Emergency BIOS to download. Latest Emergency Recovery procedure can be found on the FAQ section of the FTP site under FAQ # KC_0028 at location:

ftp://ftp.kontron.ca/Support/Support_FAQ - Questions & Answers/

UBIOS 4.x is a utility that allows you to take BIOS files from a disk and update the Flash BIOS device with them.

It also allows BIOS files in the Flash BIOS device to be saved to disk.

The program can be executed in one of two modes:

- Interactive Mode: In this mode the program is menu-driven. This mode is explained in Section 11.1.2.
- Batch Mode: It is also possible to run the program without menus by a command that specifies the selected options and files with parameters. This mode is explained in Section 11.1.3.



NOTE

Using UBIOS, will clear the CMOS Setup in Flash BIOS. Therefore, it is recommended that you take note of your Setup parameters (especially Hard Disk parameters), so you can reset them afterwards.



NOTE

To update BIOS files, these files must be in the same directory as the UBIOS.EXE program. Therefore, prior to running the program, make sure the files you wish to update and the UBIOS program file are in the same directory.

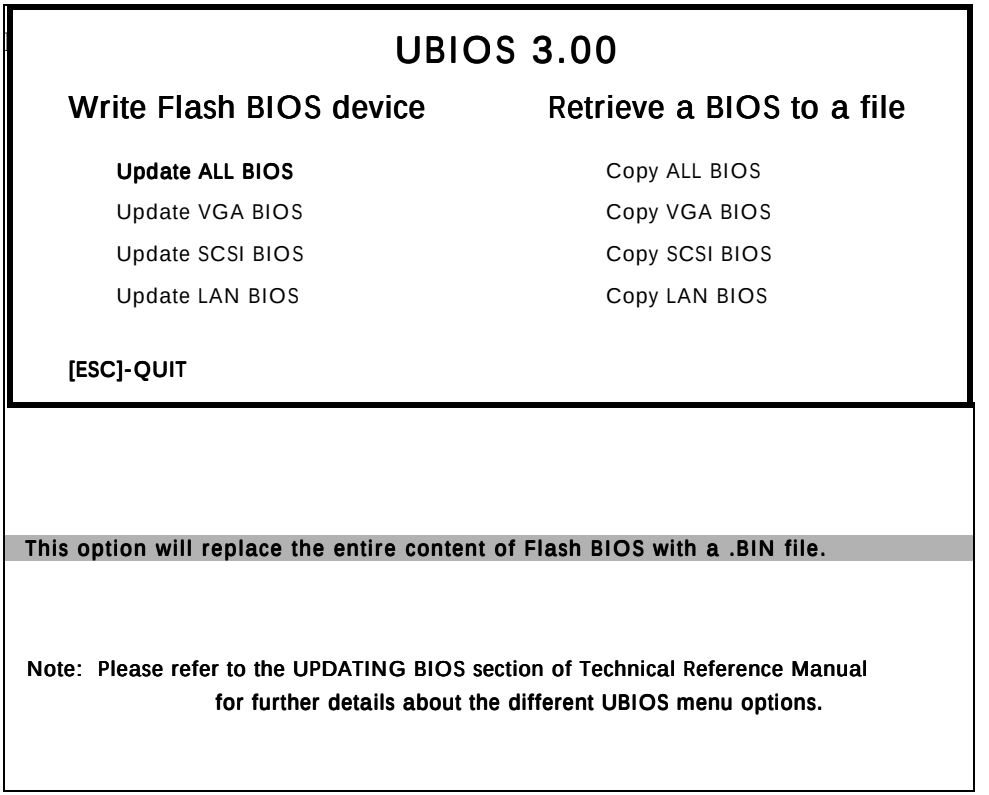
When you enter UBIOS, only the current directories are available. Within the UBIOS program, you can change the drive, but not the directory.

11.1.2 UBIOS - Interactive Mode

To run the program in interactive mode, type "UBIOS" from the DOS prompt and the UBIOS 3.0 presentation screen will be displayed. To continue, hit any key on the keyboard. This brings you to the main menu.

11.1.2.1. Main Menu

The main menu appears below:



The main menu displays two groups of options: Write Flash BIOS device and Retrieve a BIOS to a file. The first group allows you to update the Flash BIOS device with a BIOS file stored on disk. The second group allows you to copy the contents of the Flash BIOS device to files on disk.

In the above menu, the option **Update ALL BIOS** is highlighted and the option is described in the shaded row below. Move the arrow keys to highlight other options.

To select the highlighted option, press ENTER.

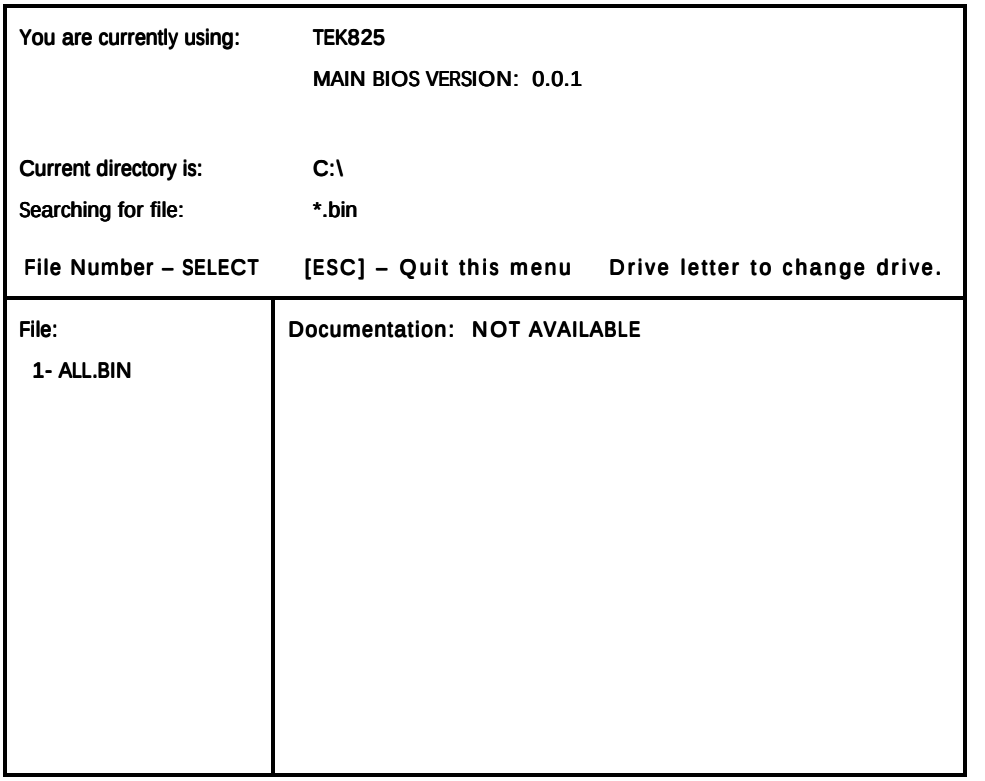
To exit the program, press the ESC key when you are in the main menu.

There are four types of BIOS files that appear on the main menu:

- **ALL BIOS File:** This file combines all BIOS files contained in the Flash BIOS device in a single file. It has the .BIN extension.
- **VGA BIOS File:** This file contains the VGA BIOS section of the Flash BIOS. It is not available on the VIPer825.
- **SCSI BIOS File:** This file contains the SCSI BIOS section of the Flash BIOS. It is not available on the VIPer825.
- **LAN BIOS File:** This file contains the LAN BIOS section of the Flash BIOS. It is not available on the VIPer825.

11.1.2.2. Updating Flash BIOS

If you select one of the **Update** options from the main menu, a screen similar to the following is displayed:



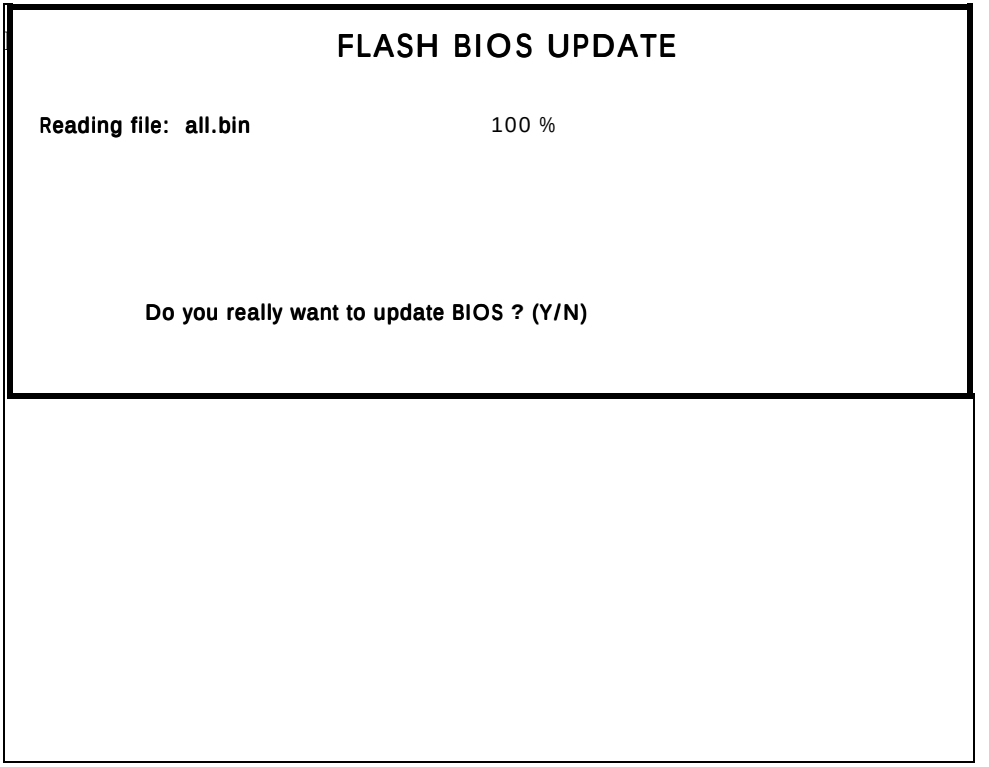
Files of the type you selected in the main menu and which are in the current directory are displayed in the **File** window.

To change directory, type the drive letter. If there are any files of the type you selected in this directory, they will be displayed in the **File** window.

The **Documentation** window displays "NOT AVAILABLE". It will be used in the future for displaying the contents of a .doc file.

If you want to return to the previous menu, press the ESC key.

To select a file from the **File** window, in order to update the Flash BIOS with this file, type the file number which appears before the filename in the list. A new screen is displayed as shown below. This is the Flash BIOS Update screen. You must first confirm if you want to update the Flash BIOS with the selected file (the filename appears next to **Reading file)**, by typing "Y" for Yes, "N" for No.



If you choose to update the file, by typing "Y", the program will write the file to Flash. The progress of the operation is indicated in percentage completed, next to **PLEASE WAIT – Writing to Flash …**

When the update is over the screen will appear as follow:

```
                    FLASH BIOS UPDATE

  Reading file:  all.bin                    100 %
  PLEASE WAIT – Writing to Flash ...        100 %



     Do you really want to update BIOS ? (Y/N)
```

```
        Make sure that the watchdog is disabled by JUMPER DURING the next boot
ONLY.
        Just to ensure a good CPLD update.
        After the next boot you can enable the watchdog.
        Please REBOOT as soon as possible ...
        Note:  Please refer to the UPDATING BIOS section of Technical Reference
Manual.




        Hit any key to continue ...
```

To return to the main menu, hit any key on the keyboard.

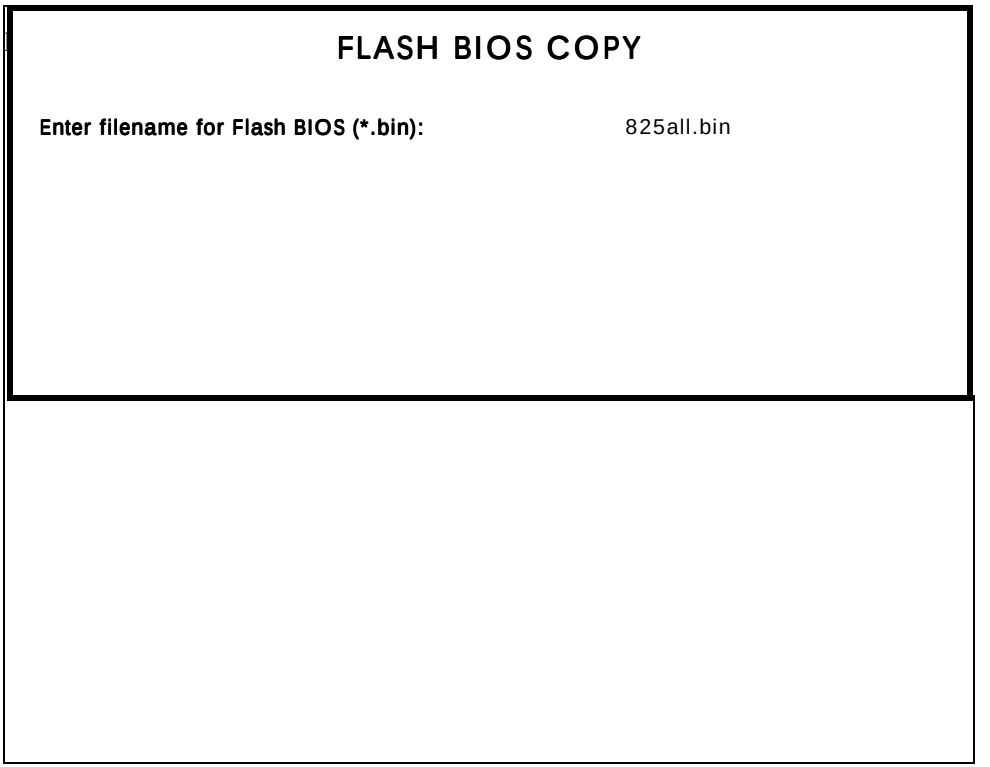
NOTE

There may be slight changes to the Flash BIOS Update screen compared to those shown here for an Update ALL BIOS operation. Also, if an error occurs, these will be indicated on the screen.

The above screen mentions disabling the watchdog, this is done by removing the W4 jumper. Installing the W4 jumper enables the watchdog timer.

11.1.2.3. Copying Flash BIOS

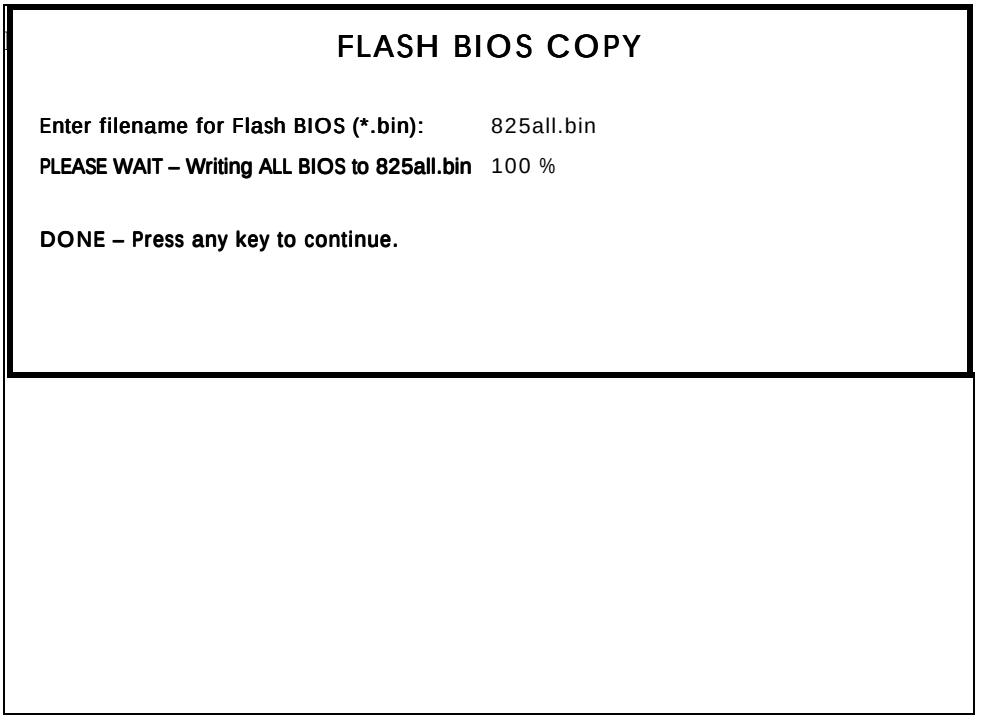
If you select one of the **Copy** options from the main menu, a screen similar to the following is displayed:



You begin a Flash Copy operation, by typing a filename (including the extension) for the file you are creating. You must use the same extension as the one indicated in parentheses on the screen. In the above example, the filename entered was “825all.bin”.

Press ENTER to proceed.

The progress of the operation will display on the screen in percentage completed. The example shown on the following is for the Copy ALL BIOS option.



If the filename entered for the BIOS file already exists, the following message will appear on the screen:

File already exits! Overwrite? (Y/N)

If you choose to overwrite the existing file, its content will be lost.

To return to the main menu, hit any key on the keyboard.

NOTE

There may be slight changes to the Flash BIOS Copy screen compared to those shown here for a Copy ALL BIOS operation. Also, if an error occurs, these will be indicated on the screen.

11.1.3 UBIOS – BATCH MODE

While files can be manually selected using the Interactive Mode, Flash BIOS Update or Copy can be achieved through Batch Mode.

The command line format is as follows:

UBIOS -B [operation] [filetype] [filename] [options] where:

-B specifies that this is a Batch Mode command.

[operation] is the Flash BIOS operation you wish to perform, and can be replaced with one of three letters:
- U for Update,
- C for Copy, or
- V for Verify (used to compare the contents of the Flash BIOS device and the specified BIOS file).

[filetype] is the filetype of the BIOS file to program (with an update operation) or to create (with a copy operation), and can be replaced with one of the following:
- ALL for All BIOS files in a single file with the .BIN extension.

[filename] is the name of the BIOS file (including the extension) to program (with an update operation) or to create (with a copy operation), and can be replaced with the filename which corresponds to the filetype. For example, if "ALL" was listed as filetype, then the filename could be "825ALL.BIN".

[options] these are optional parameters that may be added:

- /C This option will not clear the CMOS Setup when updating main BIOS (AMIBIOS), however this is not recommended since the CMOS Setup should be updated when the main BIOS is changed.
- /R Instructs UBIOS to reset the board upon completion of an operation.
- /? To get a summary of the Batch Mode options from UBIOS. It will display a Batch options summary of valid UBIOS command lines. The same help information will also be displayed each time UBIOS detects an error in the command line.

12. VT100 MODE

The VIPer825 utilizes a feature known as VT100 mode. This mode enables your single board computer to run without a local keyboard or screen. That is, operation can be controlled via a remote terminal supporting VT100 mode or a computer with a terminal emulation program (for example, Telix, Procomm).

> **NOTE**
>
> With the VIPer825 running in VT100 mode, the user can access the BIOS Setup program on his terminal.

12.1. VT100 REQUIREMENTS

The terminal you are using should emulate a VT100 or ANSI terminal. Although this is not an absolute requirement, strange characters may appear on screen if it does not. This occurs because the VT100 recognizes these control characters, and causes them to perform a specific function, for example, screen erase, cursor position, and so on.

12.2. VT100 SETUP & CONFIGURATION

Follow these steps for setting up VT100 Mode:

- Power on your VIPer825 and run the AWARD Setup program by hitting the DELETE key, before or when you see the message "Press DEL To Enter SETUP" at the top of the screen. On the Integrated Peripherals screen, set the "VT100 Mode Serial Port 1 or 2" option to the desired communication port (1 or 2). VT100 mode runs on Serial Port 1 or Serial Port 2.
- Power off your VIPer825 and install jumper W9 to enable VT100 Mode.
- Connect the communications cable as shown in Diagram 12-1. Note: If you do not require a full cable for your terminal, you can set up a partial cable by using only the TXD and RXD lines. The control lines can be ignored by looping them back as shown in Diagram 12-2.
- The BIOS Setup will automatically detect the user terminal speed and set the communication port speed likewise. These speeds are supported: 2400, 9600, 19200, 38400, 57600 and 115200 baud. If the terminal is set at another speed or if it is powered off, the BIOS Setup sets the port at 115200 by default.
- You must respect this protocol:
  8 Bits
  No Parity
  1 Stop Bit
  Echo Off.

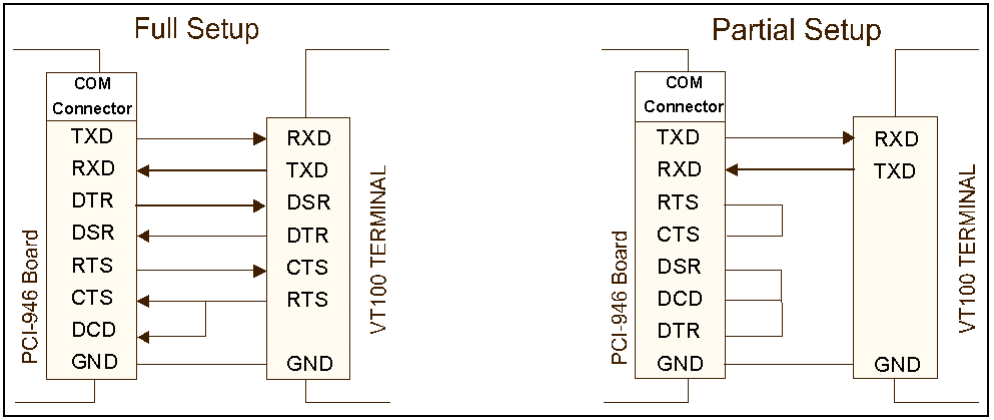
  If you are running a terminal emulation program, these parameters must be set in it.

12.3. RUNNING WITHOUT A TERMINAL

The VIPer825 can boot up without a screen or terminal attached. Wiring the system according to Diagram 12-2 allows the lines to remain active. This does not apply if the VT100 jumper is not set.

Furthermore, you can run without any console at all by simply not enabling VT100 Mode and by disabling the video interface.

DIAGRAM 12-1: VT100 Full/Partial Setup



PART 4

APPENDICES

A. BOARD SPECIFICATIONS

B. BOARD DIAGRAMS

C. CONNECTOR LOCATION & PINOUTS

D. LIST OF APPROVED VENDORS

E. MEMORY & I/O MAPS

F. BIOS SETUP ERROR CODES

G. EMERGENCY PROCEDURE

A. BOARD SPECIFICATIONS

A.1 ELECTRICAL

- Conforms to the electrical specifications in the IEEE P996 Bus Specification (PC/AT) and the PCI Local Bus Specification Revision 2.1.
- Supply Current:

TABLE A-1: Supply Current

Supply Current *	Pentium 100MHz	Pentium 133MHz	Pentium 166MHz	Pentium MMX 200MHz	Pentium MMX 233MHz
+5V Typical	1.71A	1.79A	2.05A	2.34A	2.62A
+12V Typical	40mA	161mA	111mA	138mA	165mA

* Measured with 16MB System DRAM memory, 512KB cache memory, keyboard, floppy and hard disk.

A.2 MECHANICAL

- Please refer to Mechanical Specifications in Appendix C Board Diagrams.
- Dimensions: 7.125 in. x 4.80 in. x 1.35 in. / 181 mm x 122 mm x 34mm with CPU and fan assembly.

A.3 ENVIRONMENTAL

Environmental	Operating	Storage / Transit
Temperature	0 to 60 °C / 32 to 140 °F with airflow	-40 to +70 °C / -40 to 158 °F
Humidity	5 to 95% @ 40 °C / 104 °F non condensing	0 to 95% @ 40 °C / 104 °F non condensing
Altitude	4,572 m / 15,000 feet	15,240 m / 50,000 feet
Shock	5 G, each axis	-
Vibration	1.5 G, each axis	-

A.4 RELIABILITY

- MTBF (Mean Time Between Failure) is estimated at over 120 000 hours @ 20°C / 68 °F (MIL-HDBK-217F).

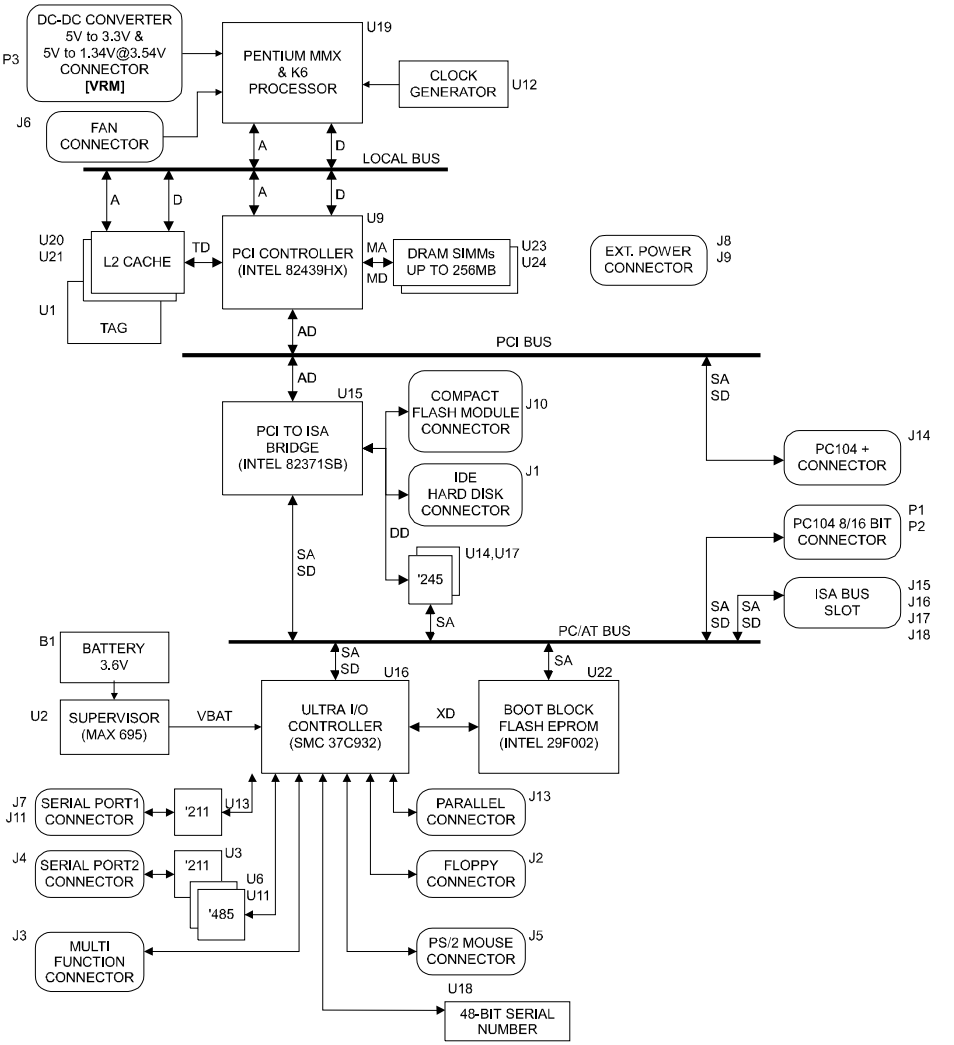
- Designed to meet or exceed:

Safety
UL 1950
CSA C22.2 No 950
EN 60950
IEC950

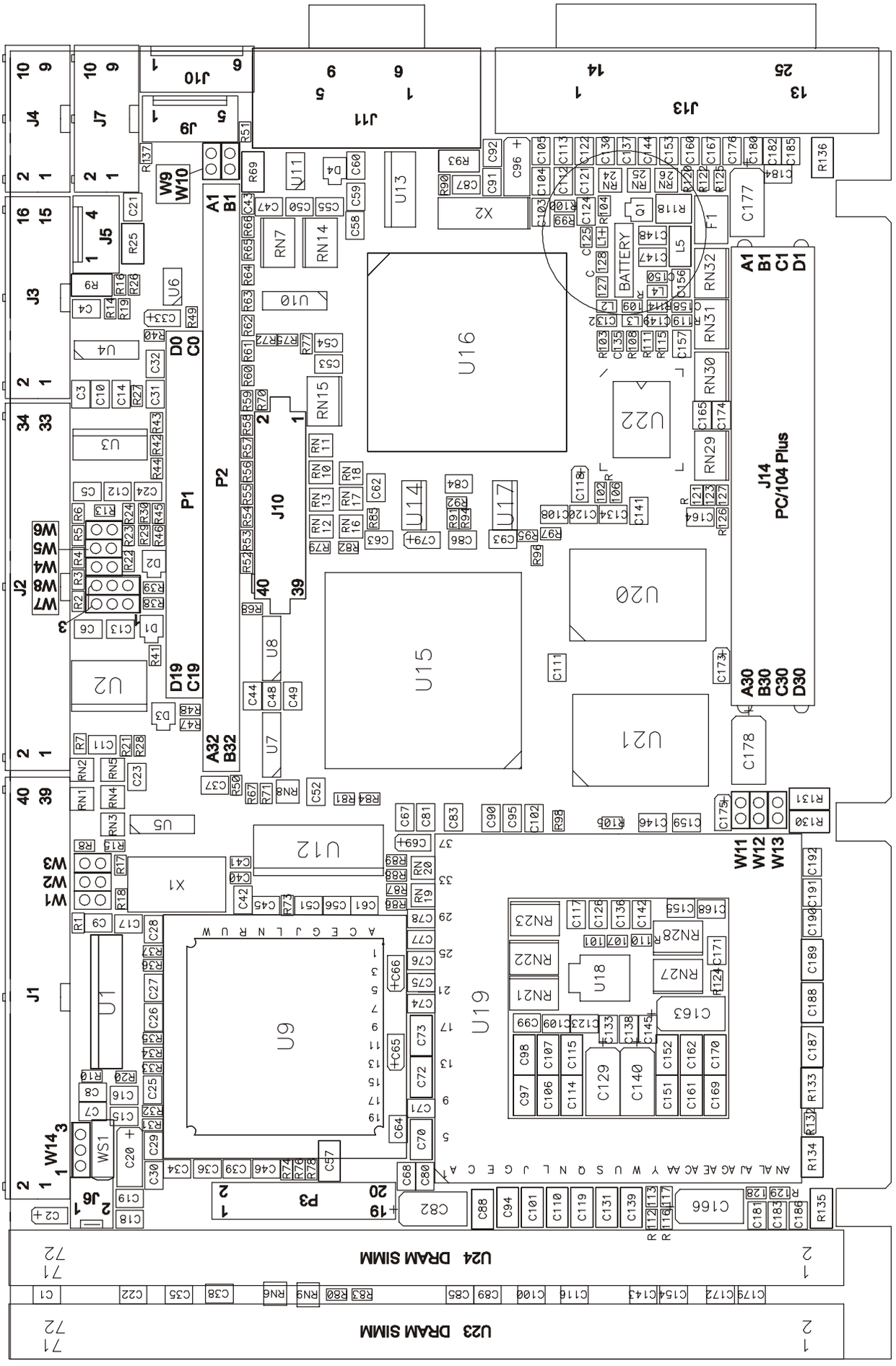
EMI/EMC
FCC 47 CFR Part 15 / CISPR22
CE Mark to EN55022 / EN50082

B. BOARD DIAGRAMS

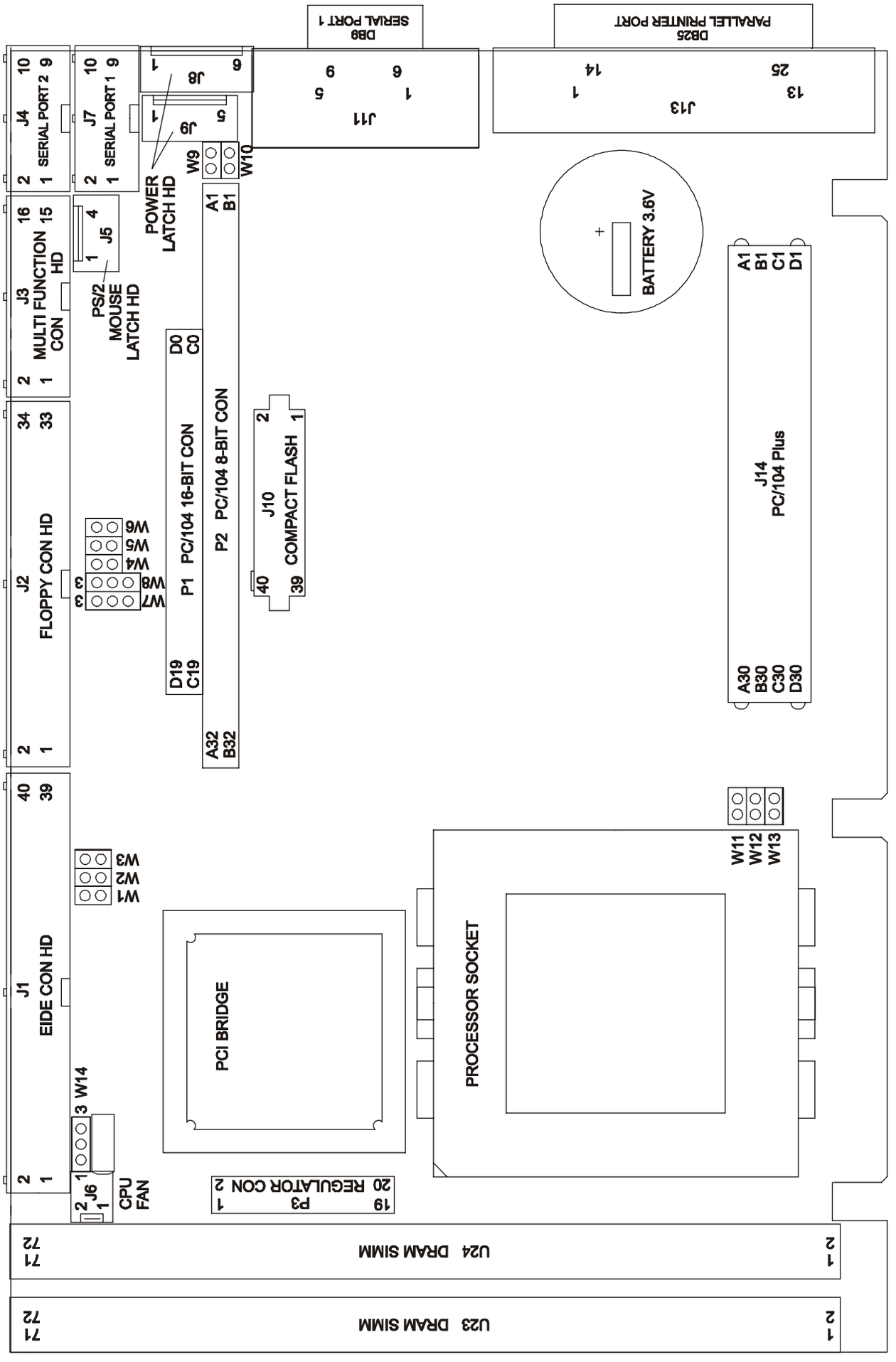
B.1 VIPer825 BLOCK DIAGRAM



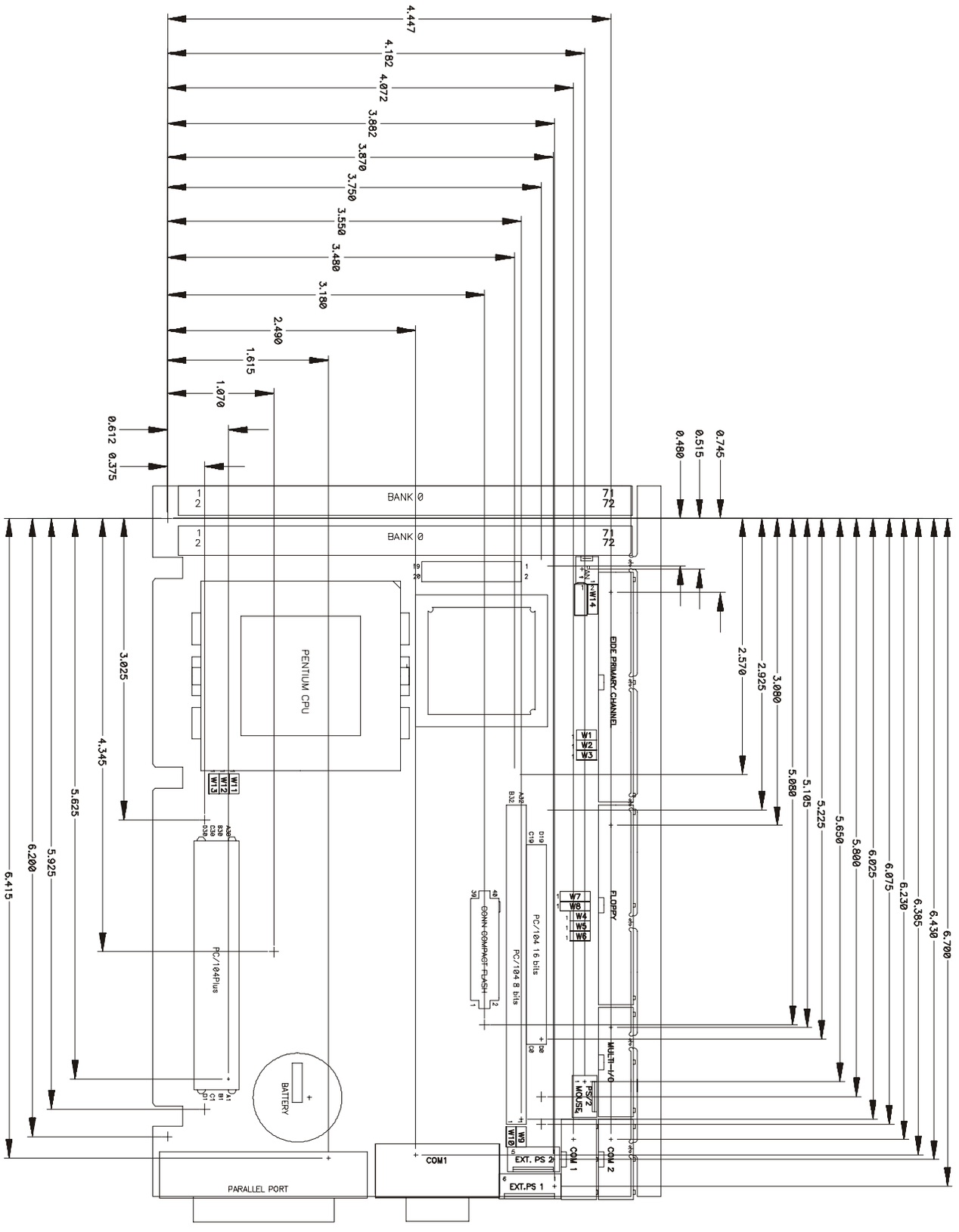
B.2 VIPer825 ASSEMBLY DIAGRAM



B.3 VIPer825 CONFIGURATION DIAGRAM

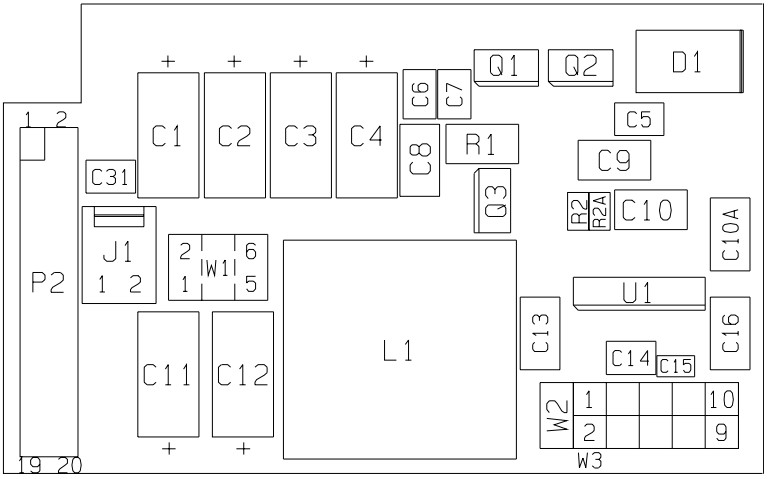


B.4 VIPer825 MECHANICAL SPECIFICATIONS DIAGRAM

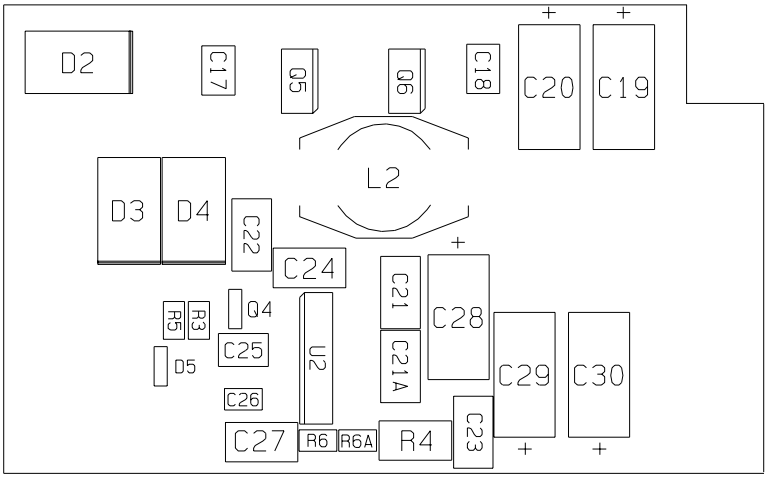


B.5 VOLTAGE REGULATOR MODULE ASSEMBLY DIAGRAMS

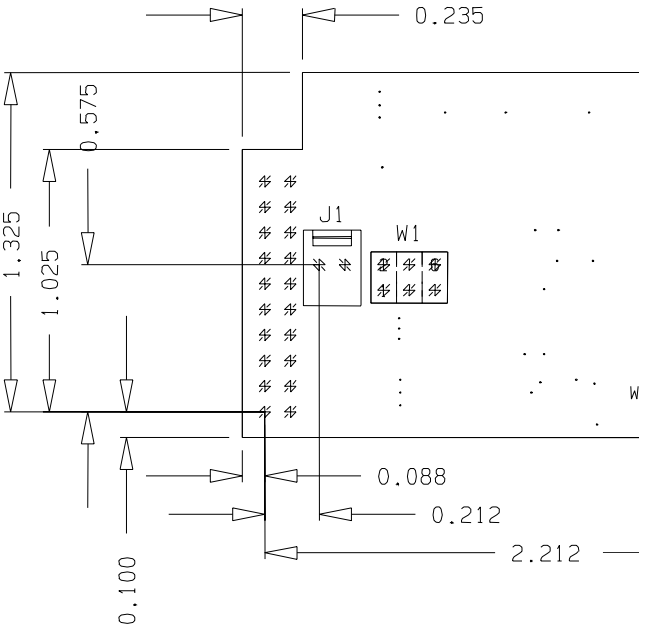
TOP



BOTTOM



B.6 VOLTAGE REGULATOR MODULE MECHANICAL SPECIFICATIONS DIAGRAM



C. CONNECTOR LOCATION & PINOUTS

C.1 LOCATION OF CONNECTORS ON THE VIPer825 & THE VOLTAGE REGULATOR MODULE

Diagram C-1 shows the connector locations on the VIPer825 and Diagram C-2 shows the Voltage Regulator Module (VRM) connector.

DIAGRAM C-1: VIPer825 Connector Locations

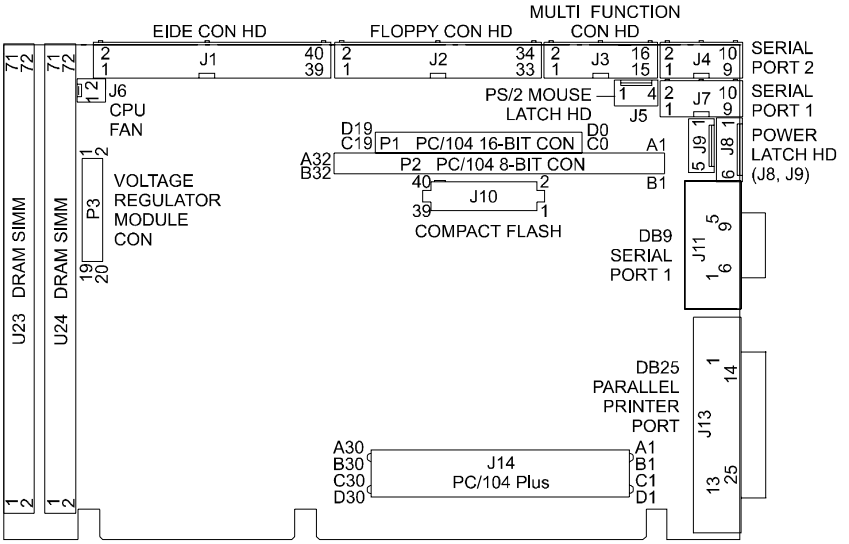
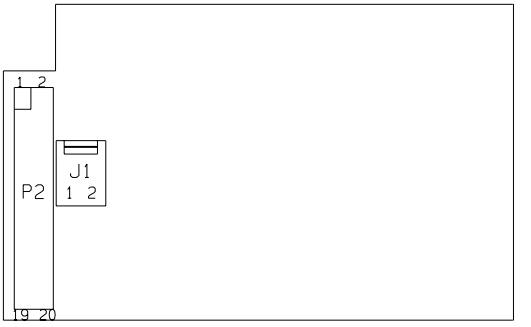


DIAGRAM C-2: Voltage Regulator Module Connector Location



C.2 CONNECTOR PINOUTS

TABLE C-1: Enhanced IDE Connector (J1) - Pinout

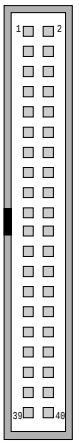
Pin Number		Top View	Pin Number	
Signal				Signal
RST#	1		2	GND
D7	3		4	D8
D6	5		6	D9
D5	7		8	D10
D4	9		10	D11
D3	11		12	D12
D2	13		14	D13
D1	15		16	D14
D0	17		18	D15
GND	19		20	N.C.
DRQ	21		22	GND
IOW#	23		24	GND
IOR#	25		26	GND
IORDY	27		28	BALE
DACK#	29		30	GND
IRQ14	31		32	N.C.
A1	33		34	GND
A0	35		36	A2
CS1#	37		38	CS3#
ACT#	39		40	GND

TABLE C-2: Floppy Disk Connector (J2) - Pinout

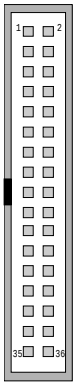
Pin Number		Top View	Pin Number	
Signal				Signal
GND	1		2	DRVEND#
GND	3		4	N.C.
GND	5		6	N.C.
GND	7		8	INDEX#
GND	9		10	MTR0#
GND	11		12	DSEL1#
GND	13		14	DSEL0#
GND	15		16	MTR1#
N.C.	17		18	DIR#
GND	19		20	STEP#
GND	21		22	WDATA#
GND	23		24	WGATE#
GND	25		26	TRK0#
N.C.	27		28	WRPROT#
N.C.	29		30	RDATA#
GND	31		32	HDSEL#
N.C.	33		34	DSKCHG#

TABLE C-3: Multi Function Connector (J3) - Pinout

Pin Number			Pin Number	
Signal				Signal
KB:CLK	1		2	GND
KB:DATA	3		4	GND
VCC	5		6	VCC
SPEAKER	7		8	VCC
KBDINH#	9		10	GND
RSV	11		12	GND
PBRES#	13		14	GND
IDE:ACT#	15		16	VCC

Active low signal

TABLE C-4: Serial Port 2 - (J4) RS-232 - Pinout

Pin Number			Pin Number	
Signal				Signal
DCD	1		2	DSR
RXD	3		4	RTS
TXD	5		6	CTS
DTR	7		8	RI
GND	9		10	N.C.

TABLE C-5: Serial Port 2 - (J4) RS-422/RS-485 - Pinout

Pin Number			Pin Number	
Signal				Signal
RSV	1		2	RSV
RX(-)	3		4	RX(+)
TX(-)	5		6	TX(+)
RSV	7		8	RSV
GND	9		10	N.C.

TABLE C-6: PS/2 Mouse Connector (J5) – Pinout

Pin Number Signal	
MOUSE:CLOCK	1
GND	2
MOUSE:DATA	3
VCC	4

Front View

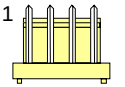


TABLE C-7: Fan Connector (J6 on VIPer825, J1 on VRM) - Pinout

Pin Number	Signal
1	+12V (J6 with W14:1-2 installed) or +5V (J6 with W14:2-3 installed or J1 on TEK-067)
2	GND

TABLE C-8: Serial Port 1 - (J7) RS-232 - Pinout

Pin Number Signal			Pin Number Signal	
DCD	1	2	DSR	
RXD	3	4	RTS	
TXD	5	6	CTS	
DTR	7	8	RI	
GND	9	10	N.C.	

TABLE C-9: External Power A Connector (J8) - Pinout

Signal	Pin Number
VCC	1
GND	2
GND	3
+12V	4
-12V	5
Power Fail Detect.	6

Front View

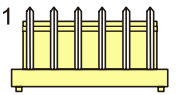


TABLE C-10: External Power B Connector (J9) - Pinout

Signal	Pin Number
VCC	1
GND	2
GND	3
VCC	4
VCC	5

Front View

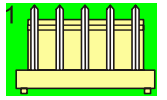


TABLE C-11: CompactFlash IDE Connector (J10) - Pinout

Pin Number	Signal		Top View		Pin Number	Signal
D11		1	1	2	2	GND
D12		3			4	D3
D13		5			6	D4
D14		7			8	D5
D15		9			10	D6
CS1#		11			12	D7
DMACK#		13			14	CS0#
DMARQ		15			16	IOR#
PDIAG#		17			18	IOW#
IRQ15		19			20	VCC
VCC		21			22	VCC
GND		23			24	GND
RESET#		25			26	GND
CSEL		27			28	A2
A1		29			30	DASP#
A0		31			32	IORDY
D0		33	39	40	34	D8
D1		35			36	D9
D2		37			38	D10
IOCS16#		39			40	GND

TABLE C-12: Serial Port 1 (J11) RS-232 –Standard DB9 Serial Port

Pin Number	Signal		Pin Number	Signal
DCD	1	2	RXD	
TXD	3	4	DTR	
GND	5	6	DSR	
RTS	7	8	CTS	
RI	9			

TABLE C-13: Parallel Port Connector (J13) - Standard Mode - Pinout

Pin Number	Signal	Pin Number	Signal
1	STB#	14	ALF#
2	D0	15	ERR#
3	D1	16	INIT#
4	D2	17	SLCTIN#
5	D3	18	GND
6	D4	19	GND
7	D5	20	GND
8	D6	21	GND
9	D7	22	GND
10	ACK#	23	GND
11	BUSY	24	GND
12	PE	25	GND
13	SLCT		

Active low signal

TABLE C-14: Parallel Port Connector (J13) - EPP Mode - Pinout

Pin Number	Signal	Pin Number	Signal
1	WRITE#	14	DATASTB#
2	PD0	15	N.C.
3	PD1	16	N.C.
4	PD2	17	ADDRSTRB#
5	PD3	18	GND
6	PD4	19	GND
7	PD5	20	GND
8	PD6	21	GND
9	PD7	22	GND
10	INTR	23	GND
11	WAIT#	24	GND
12	N.C.	25	GND
13	N.C.		

Active low signal

TABLE C-15: Parallel Port Connector (J13) - ECP Mode - Pinout

Pin Number	Signal Flow	Signal	Pin Number	Signal Flow	Signal
1	O	STROBE*	14	O	AUTOFD*, HOSTACK[2]
2	I/O	PD0	15	I	FAULT*[1], PERIPHRQST*[2]
3	I/O	PD1	16	O	INIT*[1], REVERSERQST*[2]
4	I/O	PD2	17	O	SELECTIN*[1,2]
5	I/O	PD3	18	-	GND
6	I/O	PD4	19	-	GND
7	I/O	PD5	20	-	GND
8	I/O	PD6	21	-	GND
9	I/O	PD7	22	-	GND
10	I	ACK*	23	-	GND
11	I	BUSY, PERIPHACK[2]	24	-	GND
12	I	PERROR, ACKREVERSE[2]	25	-	GND
13	I	SELECT			

* Active low signal
1 Compatible Mode
2 High-Speed Mode

NOTE

For more information on the ECP protocol, please refer to the Extended Capabilities Port Protocol and ISA Interface Standard (available from Microsoft Corporation) or contact our Technical Support department.

TABLE C-16: PC/104 Plus Connector (J14) – Pinout

A Side			**B Side**	
I/O Pin	**Signal Name**		**I/O Pin**	**Signal Name**
A1	5V_KEY		B1	Not Connected
A2	VI/O		B2	AD2
A3	AD5		B3	GND
A4	C/BE0#		B4	AD7
A5	GND		B5	AD9
A6	AD11		B6	VI/O
A7	AD14		B7	AD13
A8	+3.3V		B8	C/BE1#
A9	SERR#		B9	GND
A10	GND		B10	PERR#
A11	STOP#		B11	+3.3V
A12	+3.3V		B12	TRDY#
A13	FRAME#		B13	GND
A14	GND		B14	AD16
A15	AD18		B15	+3.3V
A16	AD21		B16	AD20
A17	+3.3V		B17	AD23
A18	IDSEL0		B18	GND
A19	AD24		B19	C/BE3#
A20	GND		B20	AD26
A21	AD29		B21	VCC
A22	VCC		B22	AD30
A23	REQ0#		B23	GND
A24	GND		B24	REQ2#
A25	GNT1#		B25	VI/O
A26	VCC		B26	CLK0
A27	CLK2		B27	VCC
A28	GND		B28	INTD#
A29	+12V		B29	INTA#
A30	-12V		B30	N.C.

Active low signal

TABLE C-17: PC/104-Plus Connector (J14) – Pinout (Continued)

C Side		D Side	
I/O Pin	**Signal Name**	**I/O Pin**	**Signal Name**
C1	VCC	D1	AD0
C2	AD1	D2	VCC
C3	AD4	D3	AD3
C4	GND	D4	AD6
C5	AD8	D5	GND
C6	AD10	D6	N.C. (MM66EN)
C7	GND	D7	AD12
C8	AD15	D8	+3.3V
C9	SB0#	D9	PAR
C10	+3.3V	D10	SDONE
C11	LOCK#	D11	GND
C12	GND	D12	DEVSEL#
C13	IRDY#	D13	+3.3V
C14	+3.3V	D14	C/BE2#
C15	AD17	D15	GND
C16	GND	D16	AD19
C17	AD22	D17	+3.3V
C18	IDSEL1	D18	IDSEL2
C19	VI/O	D19	IDSEL3
C20	AD25	D20	GND
C21	AD28	D21	AD27
C22	GND	D22	AD31
C23	REQ1#	D23	VI/O
C24	VCC	D24	GNT0#
C25	GNT2#	D25	GND
C26	GND	D26	CLK1
C27	CLK3	D27	GND
C28	VCC	D28	RESET#
C29	INTB#	D29	INTC#
C30	N.C.	D30	3.3V_KEY

Active low signal

TABLE C-18: PC/104 Card Connector (P2)

A Side			B Side	
I/O Pin	**Signal Name**		**I/O Pin**	**Signal Name**
A1	IOCHK#		B1	GND
A2	SD7		B2	RESET DRV
A3	SD6		B3	VCC
A4	SD5		B4	IRQ9
A5	SD4		B5	-5V
A6	SD3		B6	DRQ2
A7	SD2		B7	-12V
A8	SD1		B8	OWS#
A9	SD0		B9	+12V
A10	IOCHRDY		B10	N.C.
A11	AEN		B11	SMEMW#
A12	SA19		B12	SMEMR#
A13	SA18		B13	IOW#
A14	SA17		B14	IOR#
A15	SA16		B15	DACK3#
A16	SA15		B16	DRQ3
A17	SA14		B17	DACK1#
A18	SA13		B18	DRQ1
A19	SA12		B19	REFRESH#
A20	SA11		B20	SYSCLK
A21	SA10		B21	IRQ7
A22	SA9		B22	IRQ6
A23	SA8		B23	IRQ5
A24	SA7		B24	IRQ4
A25	SA6		B25	IRQ3
A26	SA5		B26	DACK2#
A27	SA4		B27	T/C
A28	SA3		B28	BALE
A29	SA2		B29	VCC
A30	SA1		B30	OSC
A31	SA0		B31	GND
A32	GND		B32	GND

Active low signal

TABLE C-19: PC/104 Card Connector (P1)

C Side		D Side	
I/O Pin	**Signal Name**	**I/O Pin**	**Signal Name**
C0	GND	D0	GND
C1	SBHE#	D1	MEMCS16#
C2	LA23	D2	IOCS16#
C3	LA22	D3	IRQ10
C4	LA21	D4	IRQ11
C5	LA20	D5	IRQ12
C6	LA19	D6	IRQ15
C7	LA18	D7	IRQ14
C8	LA17	D8	DACK0#
C9	MEMR#	D9	DRQ0
C10	MEMW#	D10	DACK5#
C11	SD8	D11	DRQ5
C12	SD9	D12	DACK6#
C13	SD10	D13	DRQ6
C14	SD11	D14	DACK7#
C15	SD12	D15	DRQ7
C16	SD13	D16	VCC
C17	SD14	D17	MASTER#
C18	SD15	D18	GND
C19	N.C.	D19	GND

Active low signal

TABLE C-20: Voltage Regulator Module Connector (P3 on VIPer825 and P2 on VRM) - Pinout

Pin Number	Signal	Pin Number	Signal
1	VCC	2	VCC
3	VCC	4	VCC
5	VCC	6	VCC
7	GND	8	GND
9	GND	10	GND
11	VCC3[1]	12	VCC3[1]
13	GND	14	GND
15	+12V	16	VCORE[2]
17	VCORE[2]	18	VCORE[2]
19	VCORE[2]	20	VCORE[2]

1 +3.34V

2 Voltage varies between 1.34V and 3.54V depending on the VRM W3 jumper setting (Section 6.2.3)

TABLE C-21: PC Bus Connector

A Side			B Side	
I/O Pin	**Signal Name**		**I/O Pin**	**Signal Name**
A1	IOCHK#		B1	GND
A2	SD7		B2	RESET DRV
A3	SD6		B3	VCC
A4	SD5		B4	IRQ9
A5	SD4		B5	-5V
A6	SD3		B6	DRQ2
A7	SD2		B7	-12V
A8	SD1		B8	OWS#
A9	SD0		B9	+12V
A10	IOCHRDY		B10	GND
A11	AEN		B11	SMEMW#
A12	SA19		B12	SMEMR#
A13	SA18		B13	IOW#
A14	SA17		B14	IOR#
A15	SA16		B15	DACK3#
A16	SA15		B16	DRQ3
A17	SA14		B17	DACK1#
A18	SA13		B18	DRQ1
A19	SA12		B19	REFRESH#
A20	SA11		B20	SYSCLK
A21	SA10		B21	IRQ7
A22	SA9		B22	IRQ6
A23	SA8		B23	IRQ5
A24	SA7		B24	IRQ4
A25	SA6		B25	IRQ3
A26	SA5		B26	DACK2#
A27	SA4		B27	T/C
A28	SA3		B28	BALE
A29	SA2		B29	VCC
A30	SA1		B30	OSC
A31	SA0		B31	GND

Active low signal

TABLE C-22: PC Bus Connector

C Side			D Side	
I/O Pin	**Signal Name**		**I/O Pin**	**Signal Name**
C1	SBHE#		D1	MEMCS16#
C2	LA23		D2	IOCS16#
C3	LA22		D3	IRQ10
C4	LA21		D4	IRQ11
C5	LA20		D5	IRQ12
C6	LA19		D6	IRQ15
C7	LA18		D7	IRQ14
C8	LA17		D8	DACK0#
C9	MEMR#		D9	DRQ0
C10	MEMW#		D10	DACK5#
C11	SD8		D11	DRQ5
C12	SD9		D12	DACK6#
C13	SD10		D13	DRQ6
C14	SD11		D14	DACK7#
C15	SD12		D15	DRQ7
C16	SD13		D16	VCC
C17	SD14		D17	MASTER#
C18	SD15		D18	GND

Active low signal

D. LIST OF APPROVED VENDORS

The following is list of recommended devices and connectors for use on the VIPer825. Many other modes are available and function equally well. Users are encouraged to check with their local distributors for comparable substitutes.

D.1 RECOMMENDED DRAM DEVICES

Recommended DRAM devices for the U23 and U24 72-pin sockets come with page mode at 70ns maximum access time.

For the latest list of tested DIMMs devices please consult our FTP site at :

ftp://ftp.kontron.ca/Support/Product_Memory_AVL_Approved%20Vendor%20List/

D.2 INTERFACE CONNECTORS

The following connectors are recommended for interfacing with the I/O devices. The parts shown here do not have a strain relief but one may be added.

Connector	Recommended Mating Part
IDE (J1)	Amp 746285-9 [499252-1*], Robinson Nugent IDS-C40PK-TG, Thomas & Betts 622-4030 [622-4041*]. (40-pin flat cable connector).
Floppy Disk (J2)	Amp 746285-8 [499252-6*], Robinson Nugent IDS-C34PK-TG, Thomas & Betts 622-3430 [622-3441*]. (34-pin flat cable connector).
Multi Function (J3)	Amp 746285-3 [499252-8*], Robinson Nugent IDS-C16PK-TG, Thomas & Betts 622-1630 [622-1641*]. (16-pin flat cable connector).
Serial Ports 2 & 1 (J4 & J7)	Amp 746285-1 [499252-5*], Robinson Nugent IDS-C10PK-TG, Thomas & Betts 622-1030 [622-1041*]. (10-pin flat cable connector).
PS/2 Mouse Connector (J5)	Molex 22-01-3047 (connector) Molex 08-50-0114 (crimp)
Fan Connector (J6)	Leoco 2530 S020013 (housing) Leoco 2533 TCB00A0 (crimp) Molex 22-01-3027 (housing) Molex 08-50-0114 (crimp)
Power Connector (J8)	Our part #150-348 (6-pin flat cable connector)
Power Connector (J9)	Our part #150-333 (5-pin flat cable connector)

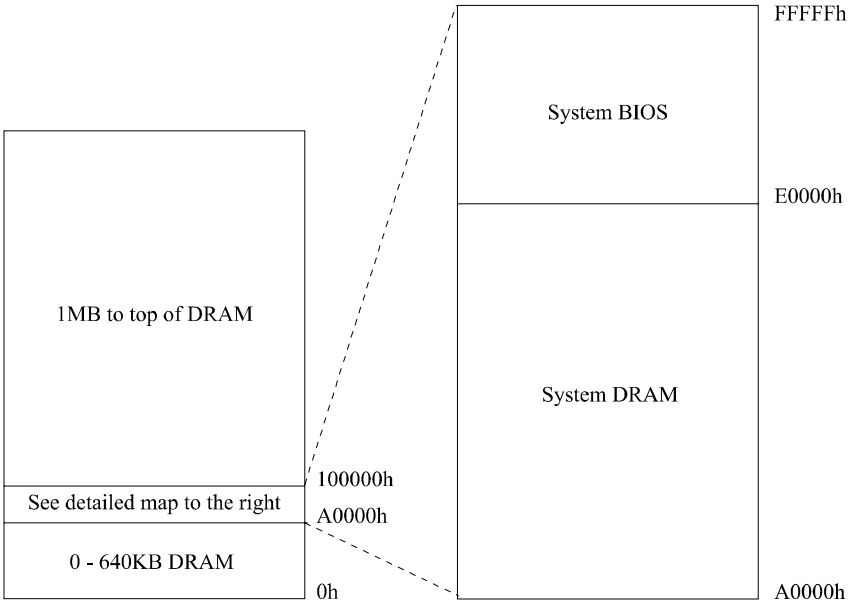
- optional strain relief part number shown in square brackets

E. MEMORY & I/O MAPS

E.1 MEMORY MAP

In this appendix, the Memory Map Diagram, as well as the Memory Map and I/O Map tables, are included.

DIAGRAM E-1: Memory Map Diagram



In Table E-1, the memory map is displayed in a table format.

TABLE E-1: Memory Map

Address	Function
00000-9FFFF	0-640 KB DRAM
A0000-FFFFF	System DRAM
100000-Top of DRAM	1 MB - Top of DRAM

E.2 I/O MAP

TABLE E-2: I/O Map

Address	Optional Address	Optional Address	Optional Address	Function
000-01F				DMA Controller 1
020-03F				Interrupt Controller 1
040-05F				Timer
060-06F				Keyboard
070-07F				Real-time clock
080-09F				DMA Page Register
0A0-0BF				Interrupt Controller 2
0C0-0DF				DMA Controller 2
0F0-0F1, 0F8-0FF				Math Coprocessor
1F0-1F7, 3F6				Primary IDE
170-177, 376				Secondary IDE
3F0-3F7	370-377			Floppy Disk
378-37A	3BC-3BE	278-27A		Parallel Port (LPT1 by default)
3F8-3FF (COM1)	2F8-2FF (COM2)	3E8-3EF (COM3)	2E8-2EF (COM4)	Serial Port 1 (COM1 by default)
2F8-2FF (COM2)	3F8-3FF (COM1)	3E8-3EF (COM3)	2E8-2EF (COM4)	Serial Port 2 (COM2 by default)

F. BIOS SETUP ERROR CODES

F.1 POST MESSAGES

During the Power-On Self-Test (POST), if the BIOS detects an error requiring your attention, it will either sound a beep code, display a message, or both.

If a message is displayed, it will be accompanied by:
"PRESS F1 TO CONTINUE, DEL TO ENTER SETUP".

F.2 POST BEEP

Currently there is only one beep code in the Main BIOS (more in Emergency Procedure, Appendix J.3). This code indicates that a video error has occurred and BIOS cannot initialize the video screen to display any additional information. This beep code consists of a single long beep followed by two short beeps.

F.3 ERROR MESSAGES

One or more of the following messages may be displayed if the BIOS detects an error during the POST.

CMOS BATTERY HAS FAILED

CMOS battery is no longer functional and should be replaced, or battery jumper is removed and should be installed.

CMOS CHECKSUM ERROR

Checksum of CMOS is incorrect. This can indicate that CMOS has become corrupt. This error may have been caused by a weak battery. Check the battery and replace it if necessary. It can also happen if the battery jumper is removed: in such a case, it should be installed.

DISK BOOT FAILURE, INSERT SYSTEM DISK AND PRESS ENTER

No boot device was found. This could mean either a boot drive was not detected or the drive does not contain proper system boot files. Insert a system disk into Drive A and press Enter. If you assumed the system would boot from the hard drive, make sure the controller is inserted correctly and all cables are properly attached. Also be sure the disk is formatted as a boot device. Then reboot the system.

DISKETTE DRIVES OR TYPES MISMATCH ERROR - RUN SETUP

Type of diskette drive installed in the system is different from CMOS definition. Run Setup to reconfigure the drive type correctly.

DISPLAY TYPE HAS CHANGED SINCE LAST BOOT

Since last powering off the system, the display adapter has been changed. You must configure the system for the new display type.

ERROR ENCOUNTERED INITIALIZING HARD DRIVE

Hard drive cannot be initialized. Be sure the adapter is installed correctly and all cables are correctly and firmly attached. Also be sure the correct hard drive type is selected in Setup.

ERROR INITIALIZING HARD DRIVE DISK CONTROLLER

Cannot initialize controller. Make sure the cord is correctly and firmly installed on the CPU board. Be sure the correct hard drive type is selected in Setup. Also check to see if any jumper needs to be set on the hard drive.

FLOPPY DISK CNTRLR ERROR OR NO CNTRLR PRESENT

Cannot find or initialize the floppy drive controller. Make sure the controller is installed correctly and firmly. If there are no floppy drives installed, be sure the Diskette Drive selection in Setup is set to NONE.

KEYBOARD ERROR OR NO KEYBOARD PRESENT

Cannot initialize the keyboard. Make sure the keyboard is attached correctly and no keys are being pressed during the boot.

If you are purposely configuring the system without a keyboard, set the error halt condition in Setup to HALT ON ALL, BUT KEYBOARD. This will cause BIOS to ignore the missing keyboard and continue the boot.

MEMORY ADDRESS ERROR AT ...

Indicates a memory address error at a specific location. You can use this location along with the memory map for your system to find and replace the bad memory.

MEMORY PARITY ERROR AT ...

Indicates a memory parity error at a specific location. You can use this location along with the memory map for your system to find and replace the bad memory.

MEMORY VERIFY ERROR AT ...

Indicates an error verifying a value already written to memory. You can use this location along with the memory map for your system to find and replace the bad memory.

OFFENDING SEGMENT

This message is used in conjunction with the I/O CHANNEL CHECK and RAM PARITY ERROR messages when the segment that has caused the problem cannot be isolated.

PRESS A KEY TO REBOOT

This will be displayed at the bottom of the screen when an error occurs that requires you to reboot. Press any key and the system will reboot.

PRESS F1 TO DISABLE NMI, F2 TO REBOOT

When BIOS detects a non-maskable interrupt condition during boot, this will allow you to disable the NMI and continue to boot, or you can reboot the system with the NMI enabled.

RAM PARITY ERROR - CHECKING FOR SEGMENT ...

Indicates a parity error in Random Access Memory.

F.4 POST CODES

> **NOTE**
>
> ISA POST codes are output to port address 80h.

TABLE F-1: POST Codes

POST (hex)	Name	Description	
01	BOOT BLOCK	Boot Block in EMERGENCY : Clear Base Memory Area.	
03	Initialize Chips	1. Clear CMOS shutdown byte. 2. Initialize EISA extended registers. (Not for us since we don't have EISA bus.)	
04	Test Memory Refresh Toggle	RAM must be periodically refreshed in order to keep the memory from decaying.	
05	Blank Video, Initialize Keyboard	1. Clear CMOS reset status byte. 2. Early Keyboard initialization.	Boot Block in EMERGENCY: Initialize Keyboard Controller.
06	EPROM Checksum	1. Test F000h segment shadow readable and writable for POST access correct. If not, show POST FE and beep continuously… 2. Auto-detect Flash EPROM.	
07	Test CMOS Interface and Battery Status	1. Install the segment. 2. Verifies CMOS is working correctly (walking bit test). 3. Restore CMOS from Flash if option is enabled. 4. Check for OVERRIDE KEY (INSERT key).	
08	Program Chipset default	Program Chipset default (show POST BEh).	
09	Early Cache Initialization	1. Check for Intel's and/or Cyrix CPU. 2. Early Cache Initialization when cache is separate from chipset. 3. Turn off Gate A20.	
0A	Setup Interrupt Vector Table	1. Initialize first 120 interrupt vectors with SPURIOUS_INT_HDLR and initialize int. 00h-1Fh according to INT_TBL. 2. Early Power Management Initialization.	

TABLE F-1: POST Codes (Continued)

POST (hex)	Name	Description	
0B	Test CMOS RAM Checksum	1. Verify time and date for valid values. 2. If Override enabled, check for Override key. If Override key pressed, Kill CMOS checksum. 3. Check CMOS Battery (useless if save CMOS in FLASH enabled since it's already done). 4. Verify Checksum, if bad, load defaults. 5. Copy CMOS in the stack. 6. Clear CMOS Alarm date. 7. Clear HD if Hidden. 8. Clear Floppy "B" if only one drive. 9. Detect for a Math Co-processor. 10. Set Fast Gate A20 Flag in CMOS. 11. If "B" drive only is set the 2 Drive are set… 12. Program Chipset for early Power Management. 13. P6 Bios Update (if applicable). 14. Kill Onboard PnP IO. 15. PnP Early Initialization. 16. PnP System Resource: 1. Get ESCD. 2. Create default SYSTEM_MAP. 3. Decode/Record ISA ESCD resources. 4. Record I/O port for PnP operation. 17. Chipset Early Shadow.	
0C	Initialize Keyboard	1. Open Xilinx I/O Port location to x90h (X=1,2 or 3) inside the chipset (if necessary). 2. Disable (if necessary). Thermal Management. 3. Disable (if necessary) Ethernet Chip.Set IDE Detect counter to 0. 4. Set CD-ROM found variable to 0. 5. Initialize zone 40:0h for the keyboard buffer.	Boot Block 1st : Verify BIOS checksum. Boot Block in EMERGENCY 2nd : Init. vector 00h through 77h.

TABLE F-1: POST Codes (Continued)

POST (hex)	Name	Description	
0D	Initialize Video Interface & Chipset	1. On M1 set the cache for the memory installed. 2. On PCI, do a PCI ROM init. 3. On P6, Init. Apic. 4. Init. Chipset. 5. Turn ON CPU Cache. 6. Set Maximum Speed. 7. Measure CPU Clock Speed. 8. Restore Speed. 9. Turn Off CPU Cache. 10. Early Video Shadow. 11. Read CMOS location 14h to find out type of video to use. Detect and initialize Video Adapter. 12. Init. T380 if necessary.	Boot Block in EMERGENCY: Try to init. Video Card…
0E	Test Video Memory	1. If CGA or MONO, test video memory. 2. Beep the speaker. 3. Show the LOGO. 4. Install VT100 driver if necessary. 5. Write sign-on message to screen. 6. Write Copyright message to screen. 7. Write Evaluation message to screen. 8. Show CPU type and speed.	
0F	Test DMA Controller 0	Test DMA Controller 0.	
10	Test DMA Controller 1	Test DMA Controller 1.	
11	Test DMA Page Registers	Test DMA Page Registers.	
12	Reserved	Reserved for 8254 Counter 0 - Not implemented.	
13	Reserved	Reserved for 8254 Counter 1 - Not implemented.	
14	Test Timer Counter 2	Test 8254 Timer 0 Counter 2.	
15	PIC Test 8259-1 mask bits	Verify 8259 Channel 1 masked interrupts by alternately turning off and on the interrupt lines.	
16	PIC Test 8259-2 mask bits	Verify 8259 Channel 1 masked interrupts by alternately turning off and on the interrupt lines.	
17	Test Struck 8259's Interrupt Bits	Nothing	
18	Test 8259 Interrupt functionality	Force an interrupt and verify that the interrupt occurred (IRQ 0 - clock int. 8h).	
19	Test Struck NMI Bits (Parity/ IO check)	Nothing.	
1A	Reserved	Reserved	
1B	Reserved	Reserved	
1C	Reserved	Reserved	
1D	Reserved	Reserved	
1E	Reserved	Reserved	

TABLE F-1: POST Codes (Continued)

POST (hex)	Name	Description
1F	Set EISA Mode	If EISA non-volatile memory checksum is good, execute EISA initialization. If no, execute ISA test and clear EISA mode flag. Test EISA Configuration Memory integrity (checksum & communication interface).
20	Enable Slot 0	Initialize slot 0 (System Board).
21	Enable Slot 1	Initialize slot 1.
22	Enable Slot 2	Initialize slot 2.
23	Enable Slot 3	Initialize slot 3.
24	Enable Slot 4	Initialize slot 4.
25	Enable Slot 5	Initialize slot 5.
26	Enable Slot 6	Initialize slot 6.
27	Enable Slot 7	Initialize slot 7.
28	Enable Slot 8	Initialize slot 8.
29	Enable Slot 9	Initialize slot 9.
2A	Enable Slot 10	Initialize slot 10.
2B	Enable Slot 11	Initialize slot 11.
2C	Enable Slot 12	Initialize slot 12.
2D	Enable Slot 13	Initialize slot 13.
2E	Enable Slot 14	Initialize slot 14.
2F	Enable Slot 15	Initialize slot 15.
30	Size Base & Extended Memory	Size base memory from 256K to 640K and extended memory above 1MB.
31	Test Base & Extended Memory	1. Test base memory from 256K to 640K and extended memory above 1MB using various patterns. 2. The last test is filling memory with 0's. 3. On a quick memory test or if user press the ESC key while testing memory, only the last test is performed.
32	Test EISA Extended Memory	If EISA Mode flag is set, then test EISA memory found in slots Initialization. NOTE 1: This will be skipped in ISA mode. NOTE 2: This POST also Detect & Report I/O PORTS and also Init. Super IO.
33	Reserved	Reserved
34	Reserved	Reserved
35	Reserved	Reserved
36	Reserved	Reserved
37	Reserved	Reserved
38	Reserved	Reserved
39	Reserved	Reserved
3A	Reserved	Reserved
3B	Reserved	Reserved

TABLE F-1: POST Codes (Continued)

POST (hex)	Name	Description
3C	Setup Enable	
3D	Initialize & Install PS/2 Mouse	Detect if mouse is present. Initialize mouse. Install interrupt vector.
3E	Setup Cache Controller	Initialize cache controller.
3F	Reserved	Reserved
40	Reserved	Reserved
41	Initialize Floppy Drive & Controller	1. Verify if we should enter setup. If so, enter setup. 2. Initialize floppy disk drive controller and any drive. Boot Block in EMERGENCY: Scan for Floppy for emergency disk…
42	Initialize Hard Drive & Controller	Initialize hard drive controller and any drive. (Call HD_INSTALL).
43	Detect & Initialize Serial/Parallel/Joystick ports	Initialize any serial, parallel and game ports.
44	Reserved	Reserved
45	Detect & Initialize Math Coprocessor	Initialize Math Coprocessor.
46	Reserved	Reserved
47	Set Speed for Boot	Set Speed for Boot.
48	Reserved	Reserved
49	Reserved	Reserved
4A	Reserved	Reserved
4B	Reserved	Reserved
4C	Reserved	Reserved
4D	Init. PC-Speaker to LINE OUT	Enable access to PC-Speaker to LINE OUT and Enable/Disable it. (T934).
4E	Manufacturing POST Loop or display Messages	1. Reboot if Manufacturing POST Loop pin is set. 2. Otherwise display any messages (i.e., any non-fatal errors that were detected during POST). 3. Enter SETUP if needed.
4F	Security Check	Ask password security if needed.
50	Write CMOS	Write all CMOS values back to CMOS-RAM and clear screen.
51	Pre-Boot Enable	1. Enable Parity checker. 2. Enable NMI. 3. Enable cache before boot.
52	Initialize Option (ROM scan)	1. Call POST 81 2. Initialize any ROMs present from C8000h to DBFFFh. Disable POST code from segment E0000h. 3. Initialize any ROMs present from DC000h to E0800h. NOTE: When FSCAN option is enabled, will initialize from C8000h to F7FFFh.
53	Initialize Time Value	Initialize Time value in 40h: BIOS area.
54	Reserved	Reserved
55	Reserved	Reserved
56	Reserved	Reserved

TABLE F-1: POST Codes (Continued)

POST (hex)	Name	Description
57	Reserved	Reserved
58	Reserved	Reserved
59	Reserved	Reserved
5A	Reserved	Reserved
5B	Reserved	Reserved
5C	Reserved	Reserved
5D	Reserved	Reserved
5E	Reserved	Reserved
5F	Reserved	Reserved
60		Store boot partition of head & cylinder.
61	Final Init	For last µs detail before boot.
62	Num Lock ON	Put Num Lock ON and Daylight Saving.
63	Boot Attempt	1. Call POST 82. 2. Set Low stack. 3. Boot via int 19h.
64	Reserved	Reserved
65	Reserved	Reserved
66	Reserved	Reserved
67	Reserved	Reserved
68	Reserved	Reserved
69	Reserved	Reserved
6A	Reserved	Reserved
6B	Reserved	Reserved
6C	Reserved	Reserved
6D	Reserved	Reserved
6E	Reserved	Reserved
6F	Reserved	Reserved
70	Reserved	Reserved
71	Reserved	Reserved
72	Reserved	Reserved
73	Reserved	Reserved
74	Reserved	Reserved
75	Reserved	Reserved
76	Reserved	Reserved
77	Reserved	Reserved
78	Reserved	Reserved
79	Reserved	Reserved
7A	Reserved	Reserved
7B	Reserved	Reserved
7C	Reserved	Reserved
7D	Reserved	Reserved
7E	Reserved	Reserved
7F	Reserved	Reserved
80	Segment Move 1	Install the segment from Flash to DC00:0h.
81	Segment Move 2	Install the segment from DC00:0h to 7000:0h.
82	Segment Move 3	Install the segment from 7000:0h to EC00:0h.

TABLE F-1: POST Codes (Continued)

POST (hex)	Name	Description
83	Check & Program CPLD	Check & Program CPLD for valid UserCode & IDCode.
84	CRC Check	Check if block have a valid CRC. If not, the Emergency procedure is launched.
85	Reserved	Reserved
86	Reserved	Reserved
87	Reserved	Reserved
88	Reserved	Reserved
89	Reserved	Reserved
8A	Reserved	Reserved
8B	Reserved	Reserved
8C	Reserved	Reserved
8D	Reserved	Reserved
8E	Reserved	Reserved
8F	Reserved	Reserved
90	Reserved	Reserved
91	Reserved	Reserved
92	Reserved	Reserved
93	Reserved	Reserved
94	Reserved	Reserved
95	Reserved	Reserved
96	Reserved	Reserved
97	Reserved	Reserved
98	Reserved	Reserved
99	Reserved	Reserved
9A	Reserved	Reserved
9B	Reserved	Reserved
9C	Reserved	Reserved
9D	Reserved	Reserved
9E	Reserved	Reserved
9F	Reserved	Reserved
A0	Reserved	Reserved
A1	Reserved	Reserved
A2	Reserved	Reserved
A3	Reserved	Reserved
A4	Reserved	Reserved
A5	Reserved	Reserved
A6	Reserved	Reserved
A7	Reserved	Reserved
A8	Reserved	Reserved
A9	Reserved	Reserved
AA	Reserved	Reserved
AB	Reserved	Reserved
AC	Reserved	Reserved
AD	Reserved	Reserved
AE	Reserved	Reserved
AF	Reserved	Reserved
B0	Spurious	If interrupt occurs in protected mode.

TABLE F-1: POST Codes (Continued)

POST (hex)	Name	Description	
B1	Unclaimed NMI	If unmasked NMI occurs, display: Press F1 to disable NMI, F2 reboot.	
B2	Reserved	Reserved	
B3	Reserved	Reserved	
B4	Reserved	Reserved	
B5	Reserved	Reserved	
B6	Reserved	Reserved	
B7	Reserved	Reserved	
B8	Reserved	Reserved	
B9	Reserved	Reserved	
BA	Reserved	Reserved	
BB	Reserved	Reserved	
BC	Reserved	Reserved	
BD	Reserved	Reserved	
BE	Early Prog Chipset Def.	Going to early program chipset to default values (called from POST_8s).	
BF	Program Chip Set	Called early at POST 0Dh to program chipset from CT-TABLE.	
C0	Turn ON/OFF Cache	OEM Specific - Cache control.	Boot Block: First POST.
C1	Memory presence	OEM Specific - Test to size on-board memory test.	Boot Block: Search for Boot Block Signature “*BBSS*”.
C2	Early Memory Initialization	OEM Specific - Board Initialization.	
C3	Extended Memory Initialization	OEM Specific - Turn ON extended memory DRAM select.	Boot Block: Expand compressed BIOS
C4	Special Display Switch Handling	OEM Specific - Display/Video switch handling so that display switch errors never occur.	
C5	Early Shadow	OEM Specific - Early Shadow enable for fast boot.	Boot Block: Early Shadow System BIOS.
C6	Cache Programming	OEM Specific - Routine for programming which region are cacheable.	Boot Block: Cache Sizing
C7	Reserved	Reserved	
C8	Special Speed Switching	OEM Specific - Routine to handle speed switching.	
C9	Special Shadow Handling	OEM Specific - Normal Shadow routine.	
CA	Very Early Initialization	OEM Specific – Initialize hardware before any other hardware initialization.	
CB	Reserved	Reserved	
CC	Reserved	Reserved	
CD	Reserved	Reserved	
CE	Reserved	Reserved	
CF	Reserved	Reserved	
D0	Power Management Full speed	Trying to go back or into full speed mode.	
D1	Power Management -- Doze mode	Trying to go or in Doze mode.	
D2	Power Management --Sleep mode	Trying to go or in Sleep mode.	

TABLE F-1: POST Codes (Continued)

POST (hex)	Name	Description
D3	Power Management – Suspend mode	Trying to go or in Suspend mode.
D4	Debug	Available POST codes for use by source code customers during development.
D5	Debug	Available POST codes for use by source code customers during development.
D6	Debug	Available POST codes for use by source code customers during development.
D7	Debug	Available POST codes for use by source code customers during development.
D8	Debug	Available POST codes for use by source code customers during development.
D9	Debug	Available POST codes for use by source code customers during development.
DA	Debug	Available POST codes for use by source code customers during development.
DB	Debug	Available POST codes for use by source code customers during development.
DC	Debug	Available POST codes for use by source code customers during development.
DD	Debug	Available POST codes for use by source code customers during development.
DE	Debug	Available POST codes for use by source code customers during development.
DF	Debug	Available POST codes for use by source code customers during development.
E0	Reserved	Reserved
E1	Setup Page	Page 1
E2	Setup Page	Page 2
E3	Setup Page	Page 3
E4	Setup Page	Page 4
E5	Setup Page	Page 5
E6	Setup Page	Page 6
E7	Setup Page	Page 7
E8	Setup Page	Page 8
E9	Setup Page	Page 9
EA	Setup Page	Page 10
EB	Setup Page	Page 11
EC	Setup Page	Page 12
ED	Setup Page	Page 13
EE	Setup Page	Page 14
EF	Shadow Error	In POST 6 to signal a Shadow Error.
F0	Reserved	Reserved
F1	Reserved	Reserved
F2	Reserved	Reserved
F3	Reserved	Reserved
F4	Reserved	Reserved

TABLE F-1: POST Codes (Continued)

POST (hex)	Name	Description
F5	Reserved	Reserved
F6	Reserved	Reserved
F7	Reserved	Reserved
F8	Reserved	Reserved
F9	Reserved	Reserved
FA	Reserved	Reserved
FB	Reserved	Reserved
FC	Reserved	Reserved
FD	Reserved	Reserved
FE	Reserved	Reserved
FF	Boot	The system is now booted or waiting for an OS.

G. EMERGENCY PROCEDURE

Follow this procedure only in case of emergency such as a critical error during the boot block flash BIOS update (when using UBIOS utility program or saving AWARD parameters in flash) or if you meet one of the following symptoms at anytime:

G.1 SYMPTOMS

- No POST code on a power up (when using a POST code card).
- System stops at post 41(when using a POST code card; see Table F-1 in previous section), associated beep code is generated (see Table G-2) and the system tries to read from the floppy drive.
- Board does not boot, even after following all the steps indicated in the Read Me First section (Powering Up the System).

G.2 GENERATE AN EMERGENCY FLOPPY DISKETTE

Use a system that has a 1.44-MB floppy drive A.

1. Insert the EMERGENCY diskette in drive A:
2. Copy the two files WDISK.COM and EMERDISK.TEK from drive A: to your hard drive (those files are available in your diskette package).
3. Remove the EMERGENCY diskette.
4. Format a diskette in drive A:.
5. At the DOS prompt of your hard drive (the same directory as the two files WDISK.COM and EMERDISK.TEK), type WDISK and then press Enter.
6. The program may display one of the following messages:

   "Emergency Code transferred"
   The emergency diskette has been successfully created.

   Take the appropriate actions and restart from the step 4 when you see the following messages.

   "Write to disk failure!"
   Verify if your floppy diskette is write-protected.

   "The file to program in flash was not found"
   Be sure that EMERDISK.TEK file is in your current path.

   "Unable to read the binary file" or **"Unable to close the opened file"**
   Possible floppy diskette corruption or bad data transfer between floppy disk and host system.

   "Unable to allocate a memory block of 256 Kbytes"
   Not enough memory to run the WDISK program.

G.3 EMERGENCY PROCEDURE

Running an EMERGENCY PROCEDURE.

1. Remove battery jumper W8 even if it is set to internal or external.
2. Install the EMERGENCY diskette in the floppy drive A (1.44 MB) connected to the VIPer825 board.
3. Power on the board. (Nothing appears on the screen.)
4. Boot block flash update will be completed when you will see POST code 55 (when using a POST code card; see Table G-1) or hear the associated beep code (see Table G-2) or when the floppy drives stops. If you see POST code 22, 33 or 44, an error has occurred. You should repeat the emergency procedure. If repeated attempts at updating the boot block flash fail, that is, you are unable to generate POST code 55, contact our Technical Support department.
5. After the procedure is successfully completed, power down the board, set your battery jumper and Supervisor I/O base address as it was previously and power up the board. Your VIPer825 boot block flash BIOS should be correctly programmed and the system should run properly.



NOTE

If the emergency disk has been lost, see Section G.2: Generate an Emergency Floppy Diskette.

TABLE G-1: Emergency Procedure POST Codes

Post Code	Description
Xx	Post code counter displaying emergency file block number loaded from floppy.
11	Begin the flash reprogramming process.
22	Error when getting the boot block flash ID code.
33	Error when erasing the boot block flash.
44	Error when programming the boot block flash.
55	Success of the boot block recovery code.

TABLE G-2: Emergency Procedure Beep Codes

Post Code	Beepcode	Description
41	**-*	Entering the boot block recovery code (i.e. Main BIOS checksum error).
22	*-*-*	Error when getting the boot block flash ID code.
33	*-*-*-*	Error when erasing the boot block flash.
44	*-*-*-*-*	Error when programming the boot block flash.
55	*-*	Success of the boot block recovery code. The board is ready to be manually reset.

* 1 Beep code
\- Silence

H. GETTING HELP

We take great pride in our customer's successes. We strongly believe in providing full support at all stages of your product development.

If at any time, you encounter difficulties with your application or with any of our products, or if you simply need guidance on system setups and capabilities, you may contact our Technical Support department at:

CANADIAN HEADQUARTERS
Tel. (450) 437-5682
Fax: (450) 437-8053

If you have any questions about our products or services, you may reach us at the above numbers or by writing to:

616 Curé Boivin
Boisbriand, Québec
J7G 2A7 Canada

LIMITED WARRANTY

We ("The seller") warrant our boards to be free from defects in material and workmanship for a period of two (2) years commencing on the date of shipment. The liability of the seller shall be limited to replacing or repairing, at the seller's option, any defective units. Equipment or parts, which have been subject to abuse, misuse, accident, alteration, neglect, or unauthorized repair are not covered by this warranty. This warranty is in lieu of all other warranties expressed or implied.

RETURNING DEFECTIVE MERCHANDISE

If your product malfunctions, please do the following before returning any merchandise:

1) Call our Technical Support department in Canada at (450) 437-5682. Make sure you have the following at hand:

- The Invoice number
- Your purchase order number
- The serial number of the defective board.

2) Give the serial number found on the back of the board and explain the nature of your problem to a service technician.

3) If the problem cannot be solved over the telephone, the technician will further instruct you on the return procedure.

4) Prior to returning any merchandise, make sure you receive an RMA number from our Technical Support and clearly mark this number on the outside of the package you are returning. To request a number, follow these steps:

- Make a copy of the request form on the following page.
- Fill out the form and be as specific as you can about the board's problem.
- Fax it to us.

5) When returning goods, please include the name and telephone number of a person whom we can contact for further explanations if necessary. Where applicable, always include all duty papers and invoice(s) associated with the item(s) in question.

6) When returning a board:

   i) Make sure that the board is properly packed: Place it in an antistatic plastic bag and pack it in a rigid cardboard box.

   ii) Ship prepaid to (but not insured):

616 Curé Boivin
Boisbriand, Québec
J7G 2A7 Canada



RETURN TO MANUFACTURER AUTHORIZATION REQUEST

Contact Name	:			
Company name	:			
Street Address	:			
City	:		**Province/State**	:
Country	:		**Postal/Zip Code**	:
Phone Number	:		**Extension**	:
Fax Number	:			

Serial Number	Failure or Problem Description	P.O.# (if not under warranty)

Fax this form to our Technical department in Canada at (450) 437-8053.