VMEM-F1

FLASH Memory Module

Manual Order Nr. 16313

User's Manual

Issue 1

Preface

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Unpacking and Special Handling Instructions

This PEP product is carefully designed for a long and fault-free life; nonetheless, its life expectancy can be drastically reduced by improper treatment during unpacking and installation.

Observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory back-up, ensure that the board is not placed on conductive surfaces, including anti-static plastics or sponges. These can cause shorts and damage to the batteries or tracks on the board.

When installing piggybacks, switch off the power mains.

Furthermore, do not exceed the specified operational temperature ranges of the board version ordered. If batteries are present, their temperature restrictions must be taken into account.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the board, re-pack it as it was originally packed.

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Revision History

Issue	Brief Description of Changes	Index	Date of Issue
1	First Issue	0	February, 1997

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1.1 Product Overview

The VMEM-F1 is a FLASH memory module with a maximum capacity of up to 192 Mbyte. The module is split into a base board containing 64 Mbytes and an optional FLASH Extension Board containing up to 128 Mbyte. Both, base board and Extension Board cover a single 3U VMEbus slot.

The VMEM-F1 has 48 memory banks , each with a size of 4 Mbyte. The FLASH is built up with AMDs 29F016 chips forming a 16 bit wide data path.

The VMEM-F1 occupies a programmable address range of 4Mbyte within the VMEbus A24/D16 and User Defined address spaces.

FLASH memory enabled status and FLASH Busy/Ready status are displayed by two LEDs on the front panel. Additionally, a general Write Protection can be selected via a front panel switch.

A small EEPROM on the base board as well as on the extension board can be used for storing board specific (board Id) and application specific parameters.

1.2 Ordering Information

Product	Description	Order Nr.
VMEM-F1	Base board with 64 MByte FLASH	15311
VMEM-F1-PB1	FLASH extension board with 128 MByte FLASH	15312

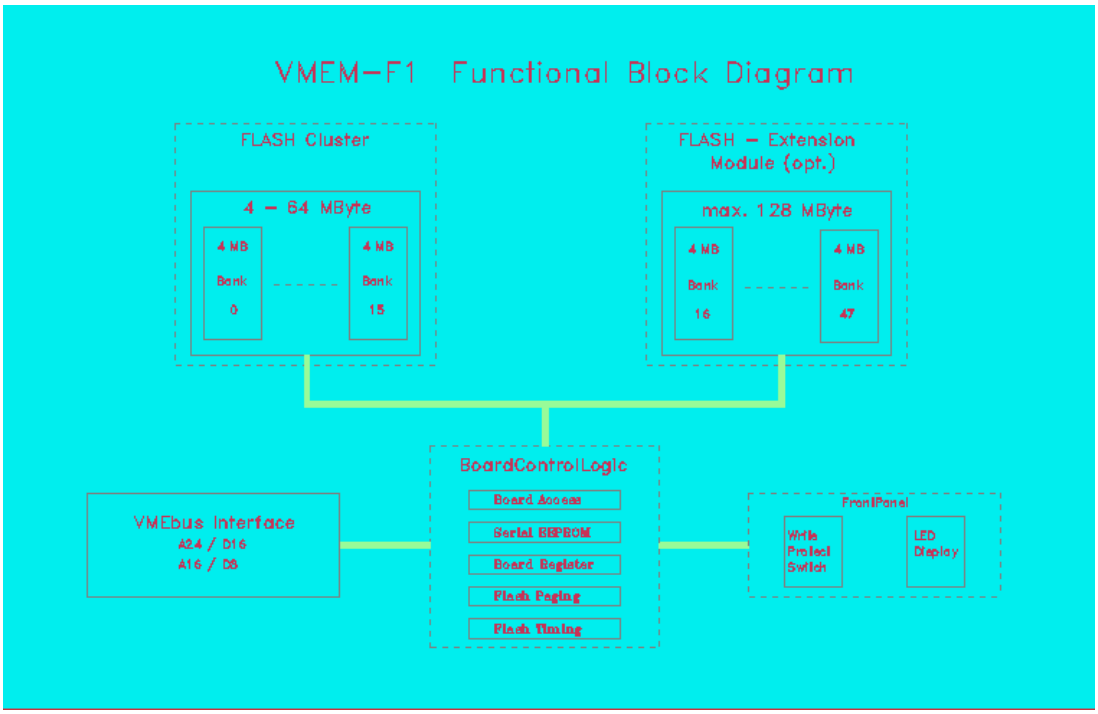
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1.3 Specifications

Storage capacity	192 MByte
Base Board	64 MByte max.
FLASH extension board	128 MByte max.
FLASH memory	
Devices	AMD 29F016, CMOS 5.0 Volt only
Access time	120ns
Write/erase cycles per device	100 000 min
Sectors per device	32
Sector size	64 kByte
Organisation	16 bit, 2 chips @ 8 bit per bank
Number of banks	48
Size of bank	4 MByte
VMEbus interface	
Type of configuration space	A16/D8 (Short I/O), jumper selectable base address, 4 kByte size, AM codes 2D/29
Type of memory space	A24/D16, programmable base address
Page size (linear mapped memory)	4 MByte, programmable 8-bit page register
Address modifier	A24/D16 supervisory program/data (3E/3D) A24/D16 supervisory/non-privil. prog/data (3E/3D/3A/39) A24/D16 user defined (1F-18) A24/D16 user defined (17-10)
Interrupt	Busy-to-Ready transition, programmable Level 2, vector programmable
Front panel functions	General Write Protection switch Busy LED (*yellow*) Enable LED (*green*)
Special functions	General Enable (boot memory select) Serial EEPROM (2kbit) for board/applic. specific data
Power requirements	*To be defined*
Temperature range	*To be defined*

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1.4 VMEM-F1 Base Board Block Diagram



1.5 Board Overview

Please refer to the attached board overview

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1.6 Features

- *Very large FLASH size per board.*
- *Compact 3U form factor.*
- *Single slot solution up to 192 MByte.*
- *FLASH sector erase architecture.*
- *Very low power consumption.*
- *Embedded erase/program algorithms.*
- *Programmable VMEbus base address and AM codes, configuration through short I/O.*
- *Programmable Busy-To-Ready transition interrupt.*
- *General hardware write protection.*
- *General board enable (boot memory support).*
- *Serial EEPROM for board/application specific data.*

1.7 Typical Applications

- *Hard disk replacement in harse environments (shock and vibration, extended temperature).*
- *Data storage i.e. speech processing.*

1.8 Related Publications

- *VITA* *VMEbus Specifications VME64.*
- *AMD* *AM29F016-120 data sheet.*
- *XICOR* *X25C02 SPI serial EEPROM data sheet.*

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Chapter 2

Functional Description

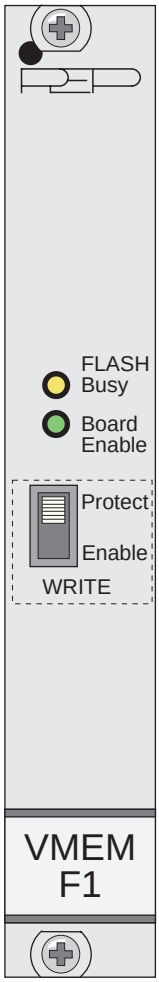
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2.1 Front Panel Functions



2.1.1 LEDs

Green LED on

Memory enabled, base address of the board is initialized or general board enable is selected.

Yellow LED on

FLASH is in busy status, chip embedded erase/program algorithms are active.

2.1.2 Switch

Switch up

Complete FLASH memory write protected. Read only function.

Switch down

FLASH memory can be read, programmed or erased.

2.2 Addressing Board Configuration Registers

The VMEM-F1 occupies 4 kByte in the VMEbus A16 address space (Short I/O) where the board configuration registers are situated. The base address of this 4 kByte block is selected using a jumper (see Chapter 3 *Configuration* for more details). It can be accessed in A16 supervisory or A16 non-privaleged address space.

Memory base address, size, AM code and some board control/status functions can be programmed via the board configuration registers. The memory base address register must be initialized before FLASH memory access is enabled.

2.2.1 Board Configuration Register Address Map

General Board Registers Area

Name	Access Type	Read/Write	Address Offset (HEX)
Serial EEPROM control register	Byte	R/W	(A16 base) + 3
Memory base address register	Byte	R/W	(A16 base) + 7
Base address mask register	Byte	R/W	(A16 base) + B
Address modifier code register	Byte	R/W	(A16 base) + F

Special Board Registers Area

Name	Access Type	Read/Write	Address Offset (HEX)
Flash page register	Byte	R/W	(A16 base) + 81
Board status register	Byte	R/W	(A16 base) + 83
Interrupt vector register	Byte	R/W	(A16 base) + 85
Interrupt control register	Byte	R/W	(A16 base) + 87

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2.3 Addressing Memory

The VMEM-F1 occupies 4 MByte of the VMEbus A24/D16 address space. The base address is programmable in 4 MByte blocks via the board base address register (see ...)

In order to reach the whole of the 192 MByte, the area is paged in blocks of 4 MByte.

On the VMEM-F1, one page represents one FLASH bank, which is physically built up of a pair of FLASH chips. Within one page, the whole memory can be linearly addressed. The FLASH page is selected via the FLASH page register (see...).

Before addressing memory, the following configuration registers must be initialized:

- *Memory base address register*, which defines the FLASH memory address.
- *Memory address mask register*, which defines the FLASH page size.
- *Memory address modifier code register*, which defines the board address modifier codes.
- *Memory page register*, which defines the currently used FLASH page.

2.3.1 Memory Base Address Register

Address: Jumper selected A16 base address + HEX 7

Format: Byte

Access: Read and write

Value after Reset: HEX 00

Register Description:

7	6	5	4	3	2	1	0
A23	*A22*	*Reserved*	*Reserved*	*Reserved*	*Reserved*	*Reserved*	*Reserved*

A23	A22	Memory Base Address (HEX)
0	0	00 00 00
0	1	40 00 00
1	0	80 00 00
1	1	C0 00 00

2.3.2 Memory Address Mask Register

Address: Jumper selected A16 base address + HEX B

Format: Byte

Access: Read and write

Value after Reset: HEX 00

Register Description:

7	6	5	4	3	2	1	0
MA23	*MA22*	*Reserved*	*Reserved*	*Reserved*	*Reserved*	*Reserved*	*Reserved*

This register must be set to 00 HEX, as by default the VMEM-F1 occupies 4 MByte of address space (reserved for future extensions when using different Extension Modules).

MA23	MA22	Memory SIze (HEX)
0	0	4 MByte

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2.3.3 Memory Address Modifier Code Register

Address: Jumper selected A16 base address + HEX F

Format: Byte

Access: Read and write

Value after Reset: HEX 00

Register Description:

7	6	5	4	3	2	1	0
Reserved	*Reserved*	*Reserved*	*Reserved*	*Reserved*	*AMC2*	*AMC1*	*AMC0*

AMC2	AMC1	AMC0	AM Codes (HEX)	Type
0	0	0	3E/3D/3A/39	A24 supervisory/non privaleged program/data access
0	0	1	3E/3D	A24 supervisory program/data access
0	1	0	10-17	User defined, A24 supervisory/non-privaleged program data access
0	1	1	14-17	User defined, A24 supervisory program/data access
1	0	0	18-1F	User defined, A24 supervisory/non-privaleged program data access
1	0	1	1C-1F	User defined, A24 supervisory program/data access

Note

The full address of the host CPU has to be set accordingly.

***VM42 Example**: the base address is set to $82xxxxxx for user defined AM code 10 HEX - 17 HEX.*

2.3.4 FLASH Page Register

Address: Jumper selected A16 base address + HEX 81

Format: Byte

Access: Read and write

Value after Reset: HEX 00

Register Description:

7	6	5	4	3	2	1	0
Reserved	Reserved	PAG5	PAG4	PAG3	PAG2	PAG1	PAG0

Notes

This register contains the currently used FLASH page, which represents a unique FLASH chip pair. The VMEM-F1 board that offers 64 MBytes of FLASH memory has 16 pages, starting at page 0 up to page F HEX.

The VMEM-F1-PB1 (FLASH Extension Module), offering 128 MBytes of FLASH memory has 32 pages, starting with page 10 HEX up to page 2F HEX.

It is important that the user does not program pages that are not available!

2.4 Addressing the Serial EEPROM

The VMEM-F1 base board, as well as the FLASH Extension Module, is fitted with a serial EEPROM that stores board specific data. The first half of the 2 kbit device is reserved for production data and the board ID. The second half is available for the application, for example, to record the number of write cycles to the various FLASH banks.

The serial EEPROMS are interfaced with the serial EEPROM control register. The timing is completely software controlled (see below).

Note

For more information on the EEPROM, please refer to the XICOR X25C02 data sheet.

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2.4.1 Serial EEPROM Control Register

Address: Jumper selected A16 base address + HEX 3

Format: Byte

Access: Read and write

Value after Reset: HEX 00

Register Description:

7	6	5	4	3	2	1	0
Reserved	*Reserved*	*Reserved*	*Reserved*	*EEP_CS1*	*EEP_CS0*	*EEP_CLK*	*EEP_DAT*

EEP_DAT	Serial Data (SDI or SDO), VMEM-F1 and VMEM-F1-PB1
EEP_CLK	Serial Clock (SCK), VMEM-F1 and VMEM-F1-PB1
EEP_CS0	Chip Select (CS), VMEM-F1
EEP_CS1	Chip Select (CS), VMEM-F1-PB1

2.5 Default FLASH Enable

Default FLASH Enable is jumper selectable (J5). If selected, the VMEM-F1 responds to the A24 address without being initialized. The default base address is 00 00 00 HEX in address space. The default page is 0. The Default FLASH Enable function may be useful if the FLASH contains a CPU startup code.

Notes

The board can be initialized at any time to a different base address and AM codes, regardless of whether Default FLASH Enable is selected.

The jumper position for the Default FLASH Enable can be read back via the board status register. The green front panel LED displays the board enabled status if selected by default or after the base address register of the board has been initialized.

2.6 Ready-to-Busy Transition Interrupt

In some cases, it may be more effective to interrupt the CPU instead of polling the end of an erase or program operation. The VMEM-F1 therefore provides a facility to generate a VME Level 2 interrupt request each time the FLASH memory changes from busy to ready status. The interrupt function is controlled by the interrupt control register and interrupt vector register.

Notes

This function is based on the Ready/Busy output of each FLASH chip. All of the pins are connected as wired-OR. This means that only one FLASH bank should be busy at any one time in order to fetch each busy-to-ready transition for the interrupt.

With respect to the Ready/Busy status, the whole FLASH is spilt into three 64 MByte clusters. The corresponding wired-OR Ready/Busy signals can be read from the board status register.

2.6.1 Interrupt Control Register

Address: Jumper selected A16 base address + HEX 87

Format: Byte

Access: Read and write

Value after Reset: HEX 00

Register Description:

7	6	5	4	3	2	1	0
Reserved	*Reserved*	*Reserved*	*Reserved*	*Reserved*	*Reserved*	*Reserved*	*IRQEN*

IRQEN	
0	Ready-to-busy transition disabled
1	Ready-to-busy transition enabled

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2.6.2 Interrupt Vector Register

Address: Jumper selected A16 base address + HEX 85

Format: Byte

Access: Read and write

Value after Reset: HEX 00

Register Description:

7	6	5	4	3	2	1	0
IRQV7	*IRQV6*	*IRQV5*	*IRQV4*	*IRQV3*	*IRQV2*	*IRQV1*	*IRQV0*

2.6.3 Board Status Register

Address: Jumper selected A16 base address + HEX 83

Format: Byte

Access: Read

Value after Reset: -

Register Description:



Bit	Value	Description
F_EN	0 1	FLASH memory access disabled FLASH memory access enabled
F_GWP	0 1	General write protection switch is in OFF position Geberal write protection switch is in ON position -> FLASH write protected
F_DEN	0 1	Default FLASH enable not selected, jumper J5 open Default FLASH enable selected, jumper J5 set
F_BUSY	0 1	FLASH memory is ready, no erase or programming operation in progress FLASH memory is busy, erase or programming operation is in progress
F_EXT	0 1	No FLASH Extension Module (VMEM-F1-PB1) assembled FLASH Extension Module (VMEM-F1-PB1) is assembled
RY_BY2	0 1	FLASH cluster 2 is ready (bank number 20 to 2F HEX) FLASH cluster 2 is busy (bank number 20 to 2F HEX)
RY_BY1	0 1	FLASH cluster 1 is ready (bank number 10 to 1F HEX) FLASH cluster 1 is busy (bank number 10 to 1F HEX)
RY_BY0	0 1	FLASH cluster 0 is ready (bank number 0 to F HEX) FLASH cluster 0 is busy (bank number 0 to F HEX)

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Chapter 3

Configuration

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3.1 Default Jumper Settings

The PS-860 has five wire jumpers which can be configured by the user. Additionally, the VMEM-F1 has a set of solder jumpers which are factory set. The list of default settings are shown below.

3.1.1 Jumper Default Settings (Component Side)

Jumper	Default Setting	Description
J1 - J4	Set	A16 base address is 00 00 HEX
J5	Open	Default FLASH enable not selected

3.1.2 Jumper Default Settings (Solder Side)

Jumper	Default Setting	Description
J6	Open	Serial EEPROM not write protected
J7	Open	Permanent FLASH write protection not selected

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3.2 Jumper Description (Component Side)

Figure 3.1 VMEM-F1 Jumper Layout (Component Side)

Please refer to the attached board layout

3.2.1 Jumpers J1 - J4: A16 Base Address

J4	J3	J2	J1	A16 Base Address (HEX)
Set	*Set*	*Set*	*Set*	*00 00 Default*
Set	Set	Set	Open	10 00
Set	Set	Open	Set	20 00
Set	Set	Open	Open	30 00
Set	Open	Set	Set	40 00
Set	Open	Set	Open	50 00
Set	Open	Open	Set	60 00
Set	Open	Open	Open	70 00
Open	Set	Set	Set	80 00
Open	Set	Set	Open	90 00
Open	Set	Open	Set	A0 00
Open	Set	Open	Open	B0 00
Open	Open	Set	Set	C0 00
Open	Open	Set	Open	D0 00
Open	Open	Open	Set	E0 00
Open	Open	Open	Open	F0 00

3.2.2 Jumper J5: Default FLASH Enable

Jumper	Setting	Description
J5	*Open*	*FLASH not enabled by default Default*
	Set	Onboard RESET generator to VME

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3.3 Jumper Description (Solder Side)

Figure 3.2 VMEM-F1 Jumper Layout (Solder Side)

Please refer to the attached board layout

3.3.1 Jumper J6: Serial EEPROM Write Protection

Jumper	Setting	Description
J6	*Open*	*Serial EEPROM not write protected* *Default*
	Set	Serial EEPROM write protected

3.3.2 Jumper J7: Permanent FLASH Write Protection

This jumper has priority over the front panel which also allows the user to select FLASH write protection.

Jumper	Setting	Description
J7	*Open*	*Permanent FLASH write protection not selected* *Default*
	1-3	Permanent FLASH write protection selected

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