Errata 1

Manual: 26037

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1. Reference: Page 4 - 13, Chapter 4.3.4.9, Table 4-14

The referenced information (table) is superseded by the following table.

Table 4-14: Control Register

Register	Address	MSB	6	5	4	3	2	1	LSB
Control	FFe0 001a	RS_CTL	Res.	VRST_DIS	S_RST	Res.	I_DEL	LED2*	LED1*

2. Reference: Page 4 - 13, Chapter 4.3.4.9, Text

The referenced information (text) is revised as follows.

The text:

- Bits 2 – 3 are reserved

is changed to read:

- Bit 2: Set this bit in combination with the solder jumper J10 and bootstraploader versions newer than qg00 to provide E2 capability of the VMP1 (additional WAIT before initialization process starts). For E2 versions, J10 must be set. For non-E2 versions, J10 must be removed.
- Bit 3: Reserved

The text:

- Bits 5 – 6 are reserved

is changed to read:

- Bit 5: Set this bit to protect the VME bus from resetting if the RST button of a slave CPU is pressed or the Watchdog counter generates a local reset. Avoiding a reset generation on the VME bus is necessary for using the VMP1 as a slave CPU in a VME system.
- Bit 6: Reserved

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3. Reference: Page 4 - 13, Chapter 4.3.4.10, Text

The referenced information (text) is revised as follows.

The text:

- Bit WD is used to indicate that a watchdog overrun has occurred (logic 1 if condition has occurred)

is changed to read:

- Bit WD is used to indicate that a watchdog overrun has occurred (logic 1 if condition has occurred). Bit WD is valid only if the Watchdog is configured for NMI.

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